STRATEGIES AND METHODOLOGIES FOR LOW POWER INVERTER DESIGN

A DISSERTATION REPORT

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OF

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IN

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SUBMITTED BY:

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CANDIDATE'S DECLARATION

I, Deaverchit Singh Baghel, Roll No.2K22/VLS/04, student of M.Tech(VLSI Design & Embedded System), hereby declare that the Project Dissertation titled **"STRATEGIES AND METHODOLOGIES FOR LOW POWER INVERTER DESIGN"** which is submitted by me to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not derived from any source without appropriate citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

Place: Delhi

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CERTIFICATE

I here by certify that the Project Dissertation titled **"STRATEGIES AND METHODOLOGIES FOR LOW POWER INVERTER DESIGN"** which is submitted by Deaverchit Singh Baghel, Roll No. 2K22/VLS/04 Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi

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Prof.Poornima Mittal
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ABSTRACT

The growing need for electronics that consume less energy has led to notable developments in low power design techniques. This abstract offers a thorough synopsis of the methods used in contemporary electronic devices to reduce power consumption, covering a range of fields including software optimization, system architecture, and integrated circuit (IC) design.
In order to minimize the environmental impact of large-scale data centres, reduce heat dissipation, and increase the battery life of portable devices, low power design is essential. Voltage scaling, clock gating, power gating, and dynamic voltage and frequency scaling (DVFS) are important methods in this field. While clock gating reduces dynamic power consumption by turning off the clock signal to inactive circuit sections, voltage scaling reduces power consumption quadratically by lowering the supply voltage.

By cutting off the power to inactive blocks, power gating effectively lowers leakage power. Multi-threshold CMOS technology, which employs transistors with various threshold voltages within a single chip to balance performance and power consumption, is another tool utilized in advanced low power design. To further reduce overall power consumption, energy-efficient communication protocols and ultra-low-power memory technologies must be developed.
Software-level tactics are just as important; they include energy-efficient coding techniques and power-aware algorithms that complement hardware capabilities. Power consumption is being optimized in operating systems and apps more and more through adaptive performance tuning and intelligent resource management.
In order to meet the strict power needs of modern electronic systems, these strategies must be integrated into a coherent design framework. Prospective research avenues encompass investigating innovative materials and device configurations, optimizing energy harvesting techniques, and creating increasingly complex power management algorithms.

All things considered, low power design is a vital area of innovation in the electronics sector, propelling developments that help high-performance and environmentally friendly technology solutions proliferate.

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LIST OF ABBREVIATIONS

S.no	Abbreviation	Full Form
1	NMOS	N channel Metal Oxide Semiconductor
2	PMOS	P channel Metal Oxide Semiconductor
3	CMOS	Complementary Metal Oxide Semiconductor
4	MOSFET	Metal Oxide Semiconductor Field Effective Transistor
5	SNM	Noise Margin
6	℃	Celsius
7	V	Volts
8	nA	Nano Ampere
9	uW	Microwatt

CHAPTER 1

INTRODUCTON

1.1 OVERVIEW

Moore's law suggests that the channel length of a MOSFET is halved every two years but to double the density that then requires a halving of the channel length of each device used requires more than a simple scaling of the manufacturing technology. Due to usage of power within VLSI circuits plays a significant role, low power integrated circuit design emerged as one of the key focuses in the past few decades. In cordless telephone communication, biomedical uses, computers, processors and other electronics and communication applications, the modern electronics industry is experiencing an aggressive downsization of these components. It is getting increasingly more challenging to carry out the design and generation of complex, analog circuits in order to define them as highly efficient when it comes to make supply voltage smaller. The aspect of the circuits analog is however still a matter of concern in CMOS technologies because the threshold voltages of the technologies are not always assurance to drop further down than what can be accessed currently. It has been deemed a challenge to package and cool such CMOS devices, and while the convoluted cooling and packing solutions do little to address the issue because the packaging of the current chips increases its power consumption. One major problem of using CMOS circuits is reliability; or lack thereof and this is most often proportional to the costs. Since the number of circuits in a single chip is doubling approximately every two years to yield higher performance, performance reduction is one of the most challenging topics. Power consumption is a major concern especially in the high performance digital VLSI systems namely the microprocessors, digital signal processors, and other portable systems including the telecommunication mobile phones , notebook computers , and personal

digital assistants (PDAs). Increased power consumption is not sustainable for batteries and needs more cooling and housing 1 En2 costs. Therefore, input path is explicitly avoided and rise/fall time is set to be longer while, in the circuit under development, both input and free up are designed to have equal delay, which, in the short run, decreases power consumption at least 10 times lesser than the total power consumption power. The energy consumption incidental to the alteration of operation is another aspect of the technological process in a size greater than 1 nm..As the technology matures into the deep submicron region, transistors become smaller in size and thus the load capacitance decreases.

1.2 POWER DISSIPATION IN CMOS

Power dissipation has emerged as a key design limitation for microelectronic circuits, specifically in the domains of devices, computing components, and wireless mobile applications. The equation explains the sources of power dissipation in CMOS circuitry.

$$P=1/2*C*VDD\hat{}2.f*N+I_{leak}*VDD+Q_{sc}*VDD*f*N \quad (1)$$

Where VDD stands for the supply voltage, P stands for the total power dissipated, and denotes the operating frequency. The power needed to charge and discharge the circuit nodes is indicated by the first term. The node's capacitance is C. The switching action, or factor N, determines how many gate transitions occur at the output during a clock cycle. The static power dissipation resulting from the leakage current Ileak is indicated by the second part in Equation 1.

The third component in Equation 1 represents power dissipation during output changeovers brought on by a short circuit current flowing from the VDD to ground. The amount of charge that the circuit's short circuit current carries throughout each transition is represented by the term QSC.

1.3 SUBTHRESHOLD LEAKAGE

When the MOSFET is working in weak inversion mode, the source to drain current is known as the sub threshold current. The following variables interfere with the circuits threshold voltage and leakage current:

- Drain Induced Barrier Lowering(DIBL):

Short channel length device MOSFET is defined when the channel's length equal the source/drain junction's order of depletion breadth. When the time taken to sweep the channel is minimized in a long channel device and the gate voltage is made sufficiently lower than the threshold voltage, then there exists a potential barrier at the source to channel junction which will prevent the electrons from the source area from inflowing into the channel. However, for the short-channel devices, the drain electric field reduces this band and thus leads to electrons getting drifted into the channel at some point. The resulting drain current increases as the electrons in the channel move, leading to increases in static leakage power and subthreshold leakage current. As indicated, when channel doping is raised in short channel devices, the effect of a DIBL is always well-ordered as shown above; nevertheless, this enhanced doping depresses the carrier mobility and as a result the drain current.

Body Bias Effect:

The threshold voltage for substrate bias in expression (2) is characterized as follows:

$$VT(V_{SB}) = V_{TO}+\gamma[(|2¢_F|+V_{SB})½-(|2¢_F|)½] \quad (2)$$

Where γ denotes the substrate bias coefficient with values usually ranging between 0 and 1.4 and 0.5 volts, $¢_F$ stands for Fermi potential and VT(VSB) refers to the substrate bias potential at zero threshold voltage. Therefore the leakage current and threshold voltage of the circuit slump with a drop in body bias and supply voltage.

- Effect of temperature:

The sub-threshold leakage current is influenced by temperature, which also impacts the threshold voltage. The temperature sensitivity of threshold voltage is 8 mV/ºC [8].

1.4 THE PROBLEM STATEMENT

Low power inverter circuits, which are essential elements of digital logic architecture, must be developed in response to the growing demand for energy-efficient electronic products. As the most basic type of logic gate, inverters are widely used in many digital applications, and their power efficiency has a direct effect on the total power consumption of integrated circuits. This issue statement has dedicated hardships and approaches along with vital strategies of low power inverter.
Key Issue:

1. Dynamic Power Consumption:
   Capacitive switching: This energy is the energy used up in a clock cycle for each transition from a logic state to the opposite state through the process of load capacitance charging and discharging .

   Frequency Dependency: In normal power dissipation, the dynamic aspect is produced with the rise of operating frequencies along with the switching activity.

2.Static Power Requirement:
Current Leakage: Leakage currents like subthreshold leakage current, gate oxide leakage current, and junction leakage current are some of the factors that have become main contributors of static power consumption in the more advanced submicron technology.

3.Power, Performance, and Area (PPA) Trade-offs:
Striking a balance between cutting down on power usage, keeping up good performance, and minimising the inverter circuit's area.

1.5 MOTIVATION

Numerous compelling issues across the technological, economic, environmental domains motivate the study of low power inverter design ideas and methodologies.

1. Essential Building Block:

The most basic and basic parts of digital circuits are inverters, which serve as the building blocks for more intricate logic gates and circuits. Improving power usage has a cascading effect that raises system efficiency as a whole.

2. Taking on New Challenges:

Power dissipation problems become more noticeable as semiconductor technology approaches nanoscale dimensions. Managing the entire power budget of integrated circuits requires addressing power inefficiencies at the inverter level.

3. Performance and Reliability:

When optimized appropriately, power-specific designs can help reduce the required operating temperature and subsequently contribute to a higher reliability and lifetime of electronic components.

1.6 OBJECTIVE

This work sought at defining the optimal inverter configuration for the static and dynamic tests across delay, noise margin and power consumption metrics. Thus, the study's goals included the recommendation of the most suitable inverter layout and the examination of pertinent attributes as well as performance indices of preferred configurations.

This paper has explored and scrutinized the numerous techniques presented by the scientists towards mitigating the leakage current for this purpose. These strategies include: Drain Gating: A method to decrease wastage by putting off the channeling ports of the transistors when it is not in operation.

For tackling with leakage currents in lower supply voltage scenario, a run-time body bias adjustment technique namely GALEOR (Gate Level Body Biassing for Energy Optimization) is adopted.

LECTOR (Leakage regulate Transistor): Another method of controlling leakage channels that also uses transistors and does not seem to bring about a significant compromise in performance.

Besides these strategies, the aspect ratios of the PMOS and NMOS transistors formed an important paradigm of the study. The intended goal of the research was to identify the best design approach based on the width to length ratio to enhance the dimensions and nature of each of these inverter configurations. This research provides a thorough analysis that will hopefully direct future design efforts by providing insightful information about the advantages and disadvantages of each configuration. This thorough analysis highlights practical methods for cutting power consumption without sacrificing desired performance features, which advances the design of low power inverters.

1.7 THESIS ORGANIZATION

There are 6 chapters in this thesis. Types of power consumption is explained in Chapter 1 as an introduction to the MOSFET. The problem statement, motivation, objective, and thesis organization are also included in Chapter 1. The literature review and the technology gap are discussed in Chapter 2. The third chapter discusses about existing power reduction techniques. Chapter 4 examines the proposed inverter as well as consists of a table comparing all the parameters of inverter. Chapter 5 depicts the difference in properties of silicon and GaN based device . The conclusion and future scope are presented in Chapter 6.

• CHAPTER 1- Provides a brief introduction of MOSFET as well as their power dissipation. Thesis's objective, motivation, problem statement, and thesis organization is covered in this chapter.

• CHAPTER 2- The prior research on power reduction techniques was detailed in

this chapter. According to published work, many power reduction techniques improves the power but its adverse effect is visible in noise margin and delay values. This chapter also consists of technical gap, which gives a fair idea about the dependency between the power dissipation and transistor number and size.

• CHAPTER 3- This chapter consists of all the existing power reduction techniques. This technique is implemented in the inverter and its dynamic, static as well as output characteristics is examined. Total 12 existing power reduction technique is simulated in Ltspice and its waveform is examined.

• CHAPTER 4- This chapter covers the analysis of proposed inverter. Static, dynamic and output characteristics is studied. This chapter also consists of the table which contains the information about delay, noise margin and power dissipation of all the existing techniques as well as the proposed one.

• CHAPTER 5- This chapter illustrates the difference in the properties of GaN and silicon as substrate. It also consists of a table which states difference in the property of GaN and silicon as substrate. At last simulated waveform and structure of GaN and MOSFET is studied.

• CHAPTER 6- This chapter includes the future work as well as the significant results from each chapter.

CHAPTER 2

LITERATURE REVIEW

It is always required to review the reported work. A literature review seeks to: Provide a baseline of information on the subject. Determine prior knowledge areas to reduce duplication and to acknowledge the contributions of other academics. Identify prior research, inconsistencies, knowledge gaps, primary research disputes, and unresolved issues. Two sections make up this chapter: (1) previously published work; and (2) technical gaps.

2.1 PREVIOUS REPORTED WORK:

Hyo-Sig Won Kyo-Sun Kim Kwang-Ok Jeong Ki-Tae Park Kyu-Myung Choi Jeong-Taek Kong[2], The Multi-Threshold CMOS (MTCMOS) technology was the main focus of this work as it offers a solution to the modem designs' high performance and low power design criteria. The intended function is implemented by low Vth transistors, and the leakage current is stopped by high Vth transistors.

Jieyu Li , Zihan Lian , Hao Zhang , Weifeng He , Yanan Sun , and Mingoo Seok[13], study crossed many technological nodes from TSMC 180 nm bulk CMOS to 7 nm FinFET Plus process, examining the leakage suppression capabilities, performance, and reliability of feedforward leakage self-suppression logic (FLSL) and dynamic leakage suppression logic (DLSL) approaches.

Rohit Lorenzo , Saurabh Chaudhury[14], proposed a unique transistor-level strategy for leakage minimization known as the leakage control NMOS transistor (LCNT). The suggested method inserts two N-type leakage control transistors into a conventional CMOS logic circuit. The pull-up transistors' drain is linked to the gate terminal of the leakage control transistors.

Ch. Suneetha, M. Veena, N. Anurag, M. Tarun Reddy[15], To improve the power efficiency of the logic gates, two cutting-edge techniques are used: the stackly arranged low power ON transistor (SAPON) and the leakage control NMOS transistor (LCNT). By raising resistance along the circuit between the supply voltage (Vdd) and ground (GND), the LCNT approach reduces power consumption. However, SAPON further lowers power consumption in the logic gate circuits by preventing leakage current during the changeover step.

Ashly Thomas , Sheela Devi Aswathy Chandran[16], High performance and low power full adders based on the ONOFIC technique have been developed in the proposed study. The suggested approach speeds up the complete adder circuit and lowers power dissipation. The On/Off logic (ONOFIC) solution uses a straightforward, single threshold voltage circuit level technique to decrease leakage current and leakage power. This method effectively lowers the leakage current in the logic circuit's active and standby modes.

Woo Wei Kai , Nabihah binti Ahmad , Mohamad Hairol bin Jabbar[18], The present study employed the Variable Body Biasing (VBB) approach to mitigate static power usage in the design of VLSIs. The VBB method effectively controlled the threshold voltage by applying a DC bias at the body terminal.

Srikanth Katrue, Dhireesha Kudithipudi[20], The leakage current that passes through the circuits is decreased by the suggested static power reduction method, called GALEOR (GAted LEakage TransistOR). Two gated leakage transistors are added between the NMOS and PMOS circuits of the current circuit in the suggested leakage power strategy, with the gates of the additional transistors linked to their corresponding drain areas.

Se Hun Kim, Vincent J. Mooney III[22], suggested a cutting-edge method known as

the "sleepy keeper," which lowers leakage current while maintaining precise logic state. Sleepy Keeper saves state during sleep mode by using two extra transistors in addition to conventional sleep transistors, which are powered by a gate's previously determined output. Applying dual Vth values to sleepy keeper can significantly lower subthreshold leakage current.

Narender Hanchate, Nagarajan Ranganathan[23], suggested a cutting-edge method for creating CMOS gates dubbed LECTOR that dramatically reduces leakage current without raising dynamic power dissipation. The suggested method includes the introduction of two leakage control transistors (a p-type and an n-type) inside the logic gate, each of whose gate terminal is controlled by the other's source.

S Pousia1 and K Murugan[24], Low power, fast CMOS design was achieved with the help of the suggested power gating approach. Using the recently suggested power gating approach, the xor, xnor, half adder, and 6T sram are described for a low power, high speed architecture.

2.2 TECHNICAL GAPS

These work mainly focussed in cutting down on power usage but at the same time influence some of the other parameters which are cardinal towards delivery such as circuit area, noise margins and comprehensive delay. Initially, there is no doubt that reduced supply voltage are within the scope of power-consumption reduction techniques which are familiar to everyone. These approaches minimize power consumption to a reasonably good level but at the same time, augment the number of times of propagation delay in circuits. It exists because the operating speed of the logic gates will always be dictated by the low drive strength of transistors that results from low voltages. It is also desirable to notice that low power procedures can have negative impact on the noise margin of the circuit such as variable threshold CMOS (VTCMOS) and multi-threshold CMOS (MTCMOS). Although, these techniques do help in reducing the leakage power, they will make a person slightly sensitive to

noise as well. Many of the low power design techniques also specify requirements such as the need to include more devices like nMOS and pMOS transistor, when it is necessary to incorporate certain features like power gating and the usage of dual threshold transistors. These overall increase in transistor increases the complexity as well as area of the overall logic circuit. These extra transistors can be reduced by using a technique which uses lesser transistor or by using different device which help in reducing the power of the overall circuit in device level.

CHAPTER 3

PERFORMANCE ANALYSIS OF EXISTING INVERTER CONFIGURATION

3.1 CMOS INVERTER

A CMOS inverter is a field effect transistor, or FET, made up of a semiconductor and a metal gate positioned on top of the oxygen insulating layer. The majority of electrical equipment that are responsible for producing data in tiny circuits employ these inverters [1]. As shown in Fig. 2.1(a), when the low input voltage is given to the MOS inverter, the PMOS transistor will turn ON, and the NMOS transistor will turn OFF by allowing electrons to flow through the gate terminal and providing high logic.

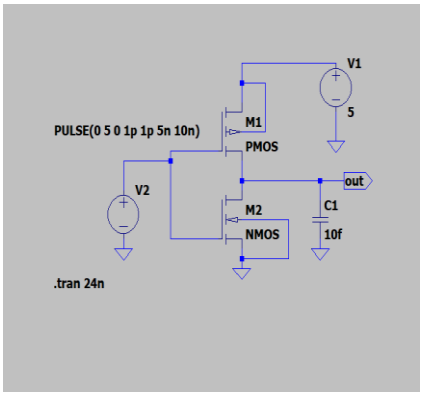

Fig.3.1(a) Circuit schematic of CMOS inverter

3.1.1 STATIC ANALYSIS

This analysis is done by plotting between input voltage and output voltage. As we can see from the Fig.3.1(b) ,for the lower value of input voltage output will be high whereas for higher value of input voltage output will be low. Because of its greater accuracy in turning ON/OFF transitions, the VTC can be thought of as an inverted step function. It is indicated that the transition region is of high quality by clearly defined slopes that allow fast changeover. One might determine the noise tolerance by comparing the highest output value with the lowest input value within each ON or

OFF operating area. This noise tolerance limit is called as noise margin. Its value was calculated as 0.2

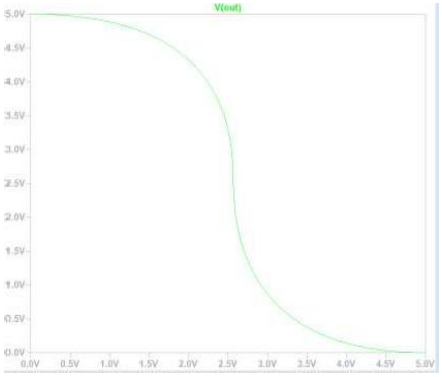

Fig.3.1(b) VTC of CMOS inverter

3.1.2 DYNAMIC ANALYSIS

Dynamic analysis is done by taking input and output into consideration with respect to time. It is done for calculating delay of the circuit as well as to check the functionality of the logic.It is done by taking 10fF capacitor at the output. As the value of the capacitor increases delay will increase. Delay value is calculated as 0.167ns.

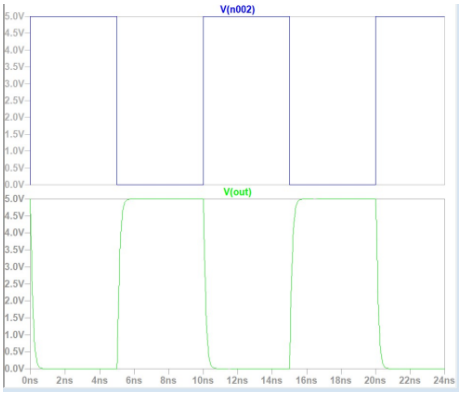

Fig.3.1(c)Input and output pulse of CMOS inverter

3.1.3 POWER ANALYSIS

As examined earlier that the power dissipation in the CMOS is more due to high static and dynamic power dissipation. The power calculated as 328uW.

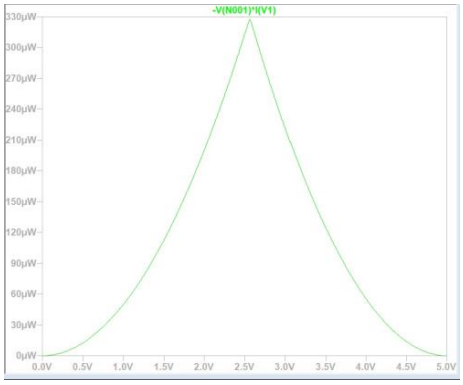

Fig.3.1(d) Power curve of CMOS inverter

Its fan-out potential is incredibly large (>50). Extremely high margin and immunity to noise. Higher expense as a result of more processing stages. However, this is being fixed.

3.2 MTCMOS

In Multi Threshold Complementary MOS circuits, a gating high threshold voltage transistor (NMOS) is placed between the ground terminal and the pull-down network to minimize leakage current. In order to minimize leakage dissipation and effectively isolate the logic gates in standby, high-VT transistors are used, while low-VT transistors are employed for logic gates where switching speed is crucial. The pass-transmission gates incorporate low-VT logic gate transistors where the high-VT transistors are turned on in the active mode allowing little propagation delay as well as negligible switching power dissipation. During Stand-by mode, the high VT transistors are turned off andathe conduction paths for any substrate

leakage currents that may be induced by the internal low VT network are effectively shutdown [2].

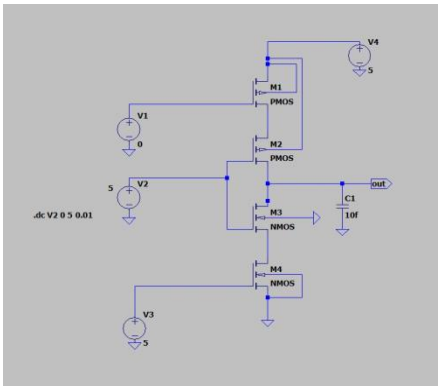

Fig.3.2(a) Circuit schematic of MTCMOS based inverter

3.2.1 STATIC ANALYSIS

This analysis is done by plotting between input voltage and output voltage. As we can see from the Fig.3.2(b) ,for the lower value of input voltage output will be high whereas for higher value of input voltage output will be low. Its noise margin will always be higher than the CMOS inverter because of more number of transistors. Its noise margin is calculated as 0.002. Which is very less as compare to CMOS inverter.

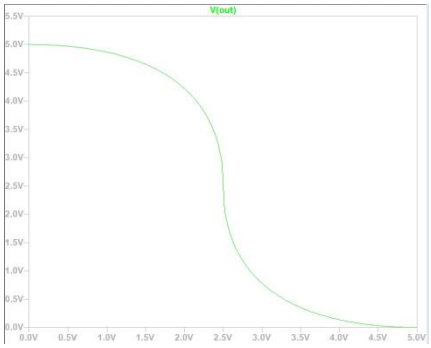

Fig.3.2(b) VTC of MTCMOS based inverter

3.2.2 DYNAMIC ANALYSIS

Dynamic analysis is done by taking input and output into consideration with respect to time. It is done for calculating delay of the circuit as well as to check the functionality of the logic.It is done by taking 10fF capacitor at the output. As the value of the capacitor increases delay will increase. Delay value is calculated as 0.209ns.The delay of the circuit also depends upon the number of trasistors used.

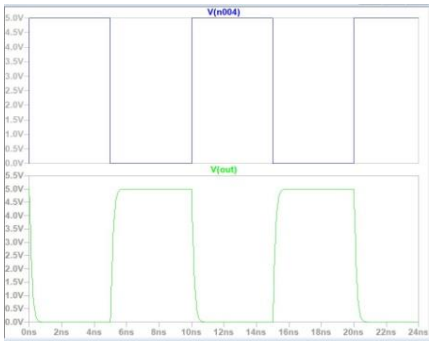

Fig.3.2(c) Input and output pulse of MTCMOS based inverter

3.2.3 POWER ANALYSIS

The main purpose of using this approach is for reducing the power dissipation. Its power is found out to be 328uW which is 9% less than the CMOS power dissipation.

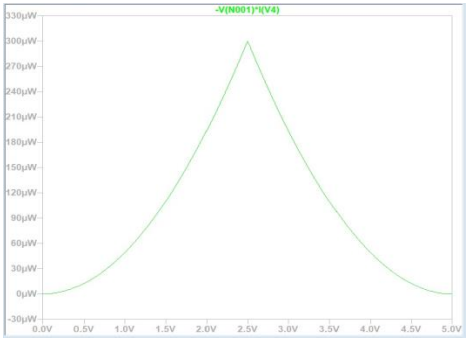

Fig.3.2(d) Power curve of MTCMOS based inverter

To prevent powering the circuit in standby mode, a high threshold voltage gating transistor PMOS is inserted between VDD and the pull down network. The data output previously will be lost while the MTCMOS circuit is in sleep mode. Setting the time for these sleep signals proved challenging for intricate circuits with several inputs. The size of the transistors determines the threshold voltage; in complex circuits with numerous transistors, this might be challenging.

3.3 LECTOR

The technology proposed to reduce leakage power is known as LECTOR and it goes to reduction of leakage in an integrated circuit by stacking of transistors in a way from supply voltage to ground. Between the pull-up and pull-down networks within the logic gate two pass-transistor leakage control devices consisting of one NMOS for pull-down and one PMOS for pull-up are incorporated. In one leakage control transistor (LCT), the source is used to control the gate terminal of the other Leakage control transistor. This configuration is useful because one of the LCTs will always be near its cutoff region. The name “self-controlled stacked transistors” means that in every LCT, the gate terminal is connected to the source in the next LCT.. Due to LCTs' self-control, the sleep transistor technique's drawback has been resolved as no external circuit is required. By adding LCTs, the leakage current is decreased since the path from Vdd to Gnd is more resistant[23].

In the logic circuit below, M2 and M3 transistors are linked between M1 and M4. The M2 and M3 leakage control MOSFETS remain closed at all times when the threshold voltage is reached.

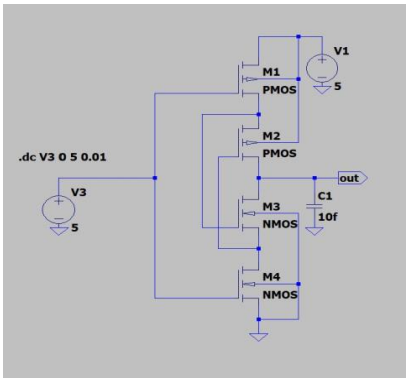

Fig.3.3(a) Circuit schematic of LECTOR inverter

3.3.1 STATIC ANALYSIS

The upper value of output voltage at lowest input voltage is said to be $V_{OH,}$ and the value of output at highest value of input is said to be $V_{OL.}$ Similarly we can find V_{IL} and V_{IH} while plotting the plot of dVout/dVin , the value of Vin at which slope is -1.Its noise margin is calculated as 0.002 which is similar at MTCMOS.

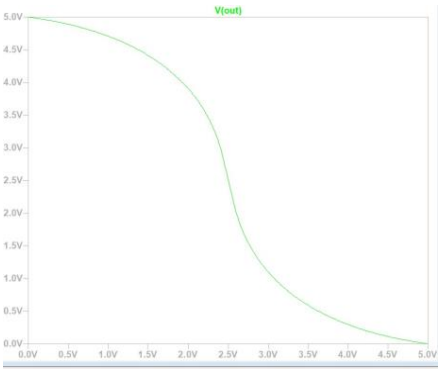

Fig.3.3(b) VTC of LECTOR inverter

3.3.2 DYNAMIC ANALYSIS

Transient analysis was performed and it was found out that the delay is 0.2169ns, which is lower than the CMOS inverter as LECTOR uses 4 transistors as compared to 2 transistors of CMOS inverter.

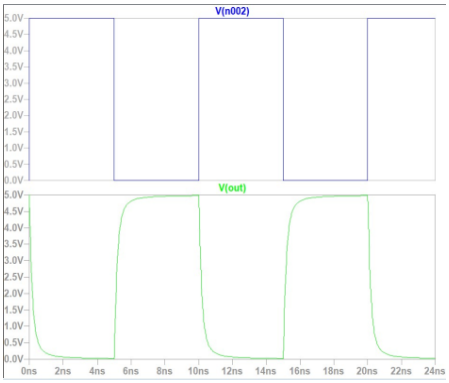

Fig.3.3(c) Input and output of LECTOR inverter

3.3.3 POWER ANALYSIS

The foremost purpose of using this approach is for reducing the power dissipation. Its power is found out to be 304uW which is 7.3% less than the CMOS power dissipation.

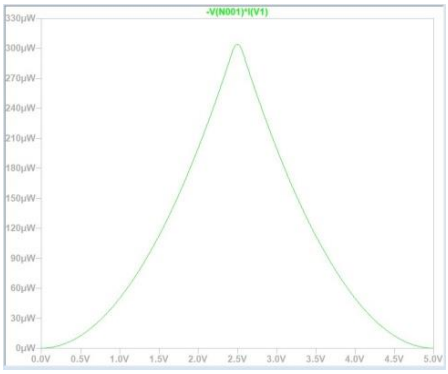

Fig.3.3(d) Power curve of LECTOR inverter

Significant leakage reduction results from the inclusion of M1 and M3 Leakage Control Transistors, which increases path resistance.
The signal's quality is poor. Because increasing the size of the transistors to lower the delay would raise the area overhead, this arrangement of self-controlled devices includes a trade-off between propagation delay and area overhead.

3.4 SLEEPY KEEPER APPROACH

According to Figure 2.4(a), the NMOS and PMOS assistance transistors are connected in opposition to the pull up and pull down networks, respectively. These are employed to provide feedback to the output in order to maintain its state after emerging from sleep mode. Traditional CMOS technology has a fundamental flaw in that it only uses transistors in their most effective, naturally inverting configurations, where NMOS transistors are connected to GND and PMOS transistors are connected to VDD. It is commonly known that NMOS transistors are inefficient at passing VDD, and that PMOS transistors are inefficient at passing GND[22].
However, the sleepy keeper solution uses this output value of "1" and an NMOS transistor linked to VDD to maintain output value equal to "1" when in sleep mode. This is because the "1" value has already been calculated.

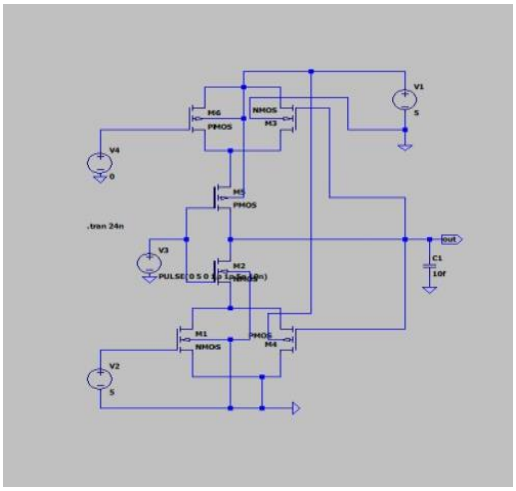

Fig.3.4(a) Circuit schematic of sleepy keeper inverter

3.4.1 STATIC ANALYSIS

The noise margin of the inverter based on sleepy keeper approach was found out to be 0.02 which is more than MTCMOS and LECTOR but it is less than the CMOS inverter

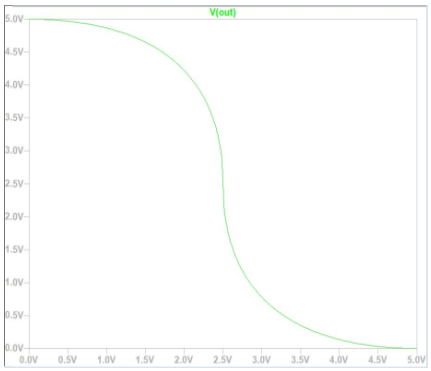

Fig.3.4(b)VTC of sleepy keeper inverter

3.4.2 DYNAMIC ANALYSIS

The dynamic or transient analysis of Sleepy keeper based inverter was performed and it was found out that the delay of the circuit is 0.20885ns which is lesser than the MTCMOS and LECTOR . As it uses extra voltage source and the extra transistor is controlled by it so the dependency of input to that extra transistor gets reduced.Hence the overall delay reduces.

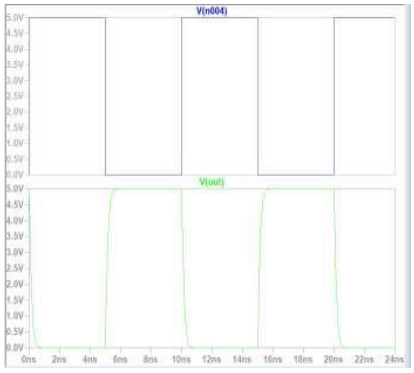

Fig.3.4(c) Input and output pulse of sleepy keeper inverter

3.4.3 POWER ANALYSIS

The DC analysis of the sleepy keeper inverter is performed and it was out that the power dissipation is 300uW, which is 9% less than the CMOS inverter. The reduce in the power dissipation is due to the use of sleep transistor.

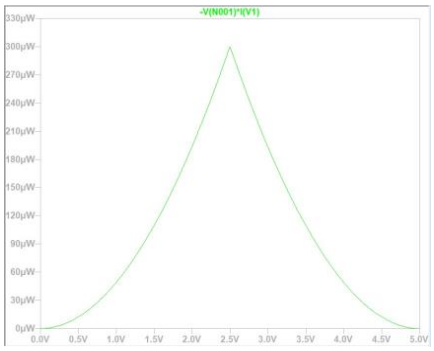

Fig.3.4(d) Power curve of sleepy keeper inverter

In contrast to the leakage feedback method, these helper transistors are directly switched from the output. Therefore, an output inverter is not required. Pull up and pull down networks are cut off from the VDD rails during sleep mode, however helper transistors allow the output to remain in its prior condition. Sleep transistors that are controlled outside. Lack of Control over Dissipation of Dynamic Power. Because of the increased static power dissipation in standby mode, the battery may run out.

3.5 SLEEP CIRCUITRY EMBEDDED CMOS CIRCUIT

Pull up and pull down networks are coupled in parallel with PMOS and NMOS sleep transistors in this network. The pull-up and output are connected in series with one more PMOS sleep transistor. With this configuration, leakage is eliminated in standby mode and reduced in active mode. The middle sleep transistor reduces operating delay by quickly switching its output due to its forward body biasing[19].

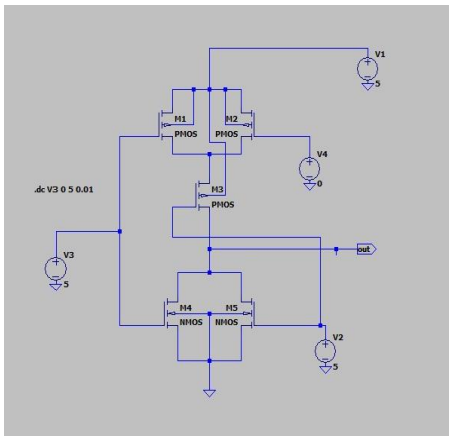

Fig.3.5(a) Circuit schematic of Sleep circuitry inverter

3.5.1 STATIC ANALYSIS

This analysis is done by plotting between input voltage and output voltage. As we can see from the Fig.3.5(b) ,for the lower value of input voltage output will be high whereas for higher value of input voltage output will be low. Its noise margin will always be higher than the CMOS inverter because of more number of transistors.

Its noise margin is calculated as 0.024. Which is very less as compare to CMOS inverter.

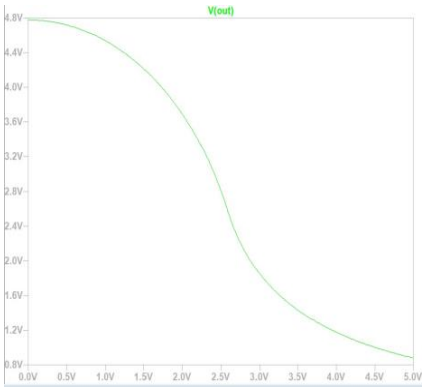

Fig.3.5(b) VTC of Sleep circuitry inverter

3.5.2 DYNAMIC ANALYSIS

Dynamic analysis is done by taking input and output into consideration with respect to time. It is done for calculating delay of the circuit as well as to check the functionality of the logic.It is done by taking 10fF capacitor at the output. As the value of the capacitor increases delay will increase. Delay value is calculated as 0.202ns which is more than the CMOS inverter.

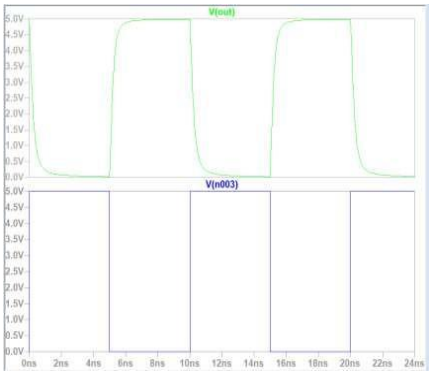

Fig.3.5(c)Input and output pulse of Sleep circuitry inverter

3.5.3 POWER ANALYSIS

The DC analysis of the sleepy keeper inverter is performed and it was out that the power dissipation is 268uW, which is 18% less than the CMOS inverter. The reduce in the power dissipation is due to the use of 2 extrabsleep transistor.

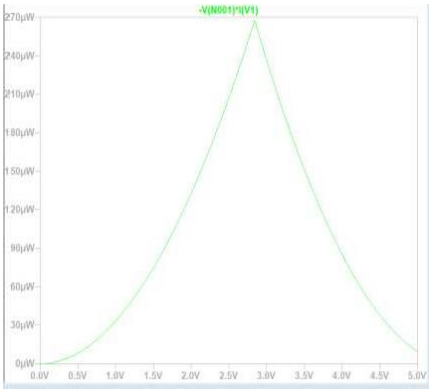

Fig.3.5(d)Power curve of Sleep circuitry inverter

It operates in standby mode with zero leakage current at varying temperatures. In standby mode, the battery is not drained.

Leakage current is 0 in sleep mode and increases in active mode, which results in increased power dissipation.

3.6 GALEOR

The leakage current that passes through the circuits is decreased via the static power reduction method known as GALEOR (GAted LEakage TransistOR). 2 gated leakage transistors are added between the NMOS and PMOS circuits of the existing circuit in this leakage power approach, with their gates coupled to the corresponding drain regions. By creating stack effect, the suggested GALEOR approach lowers the leakage current passing through the inverter in all conceivable configurations[20]. The GALEOR approach applied to an inverter is displayed in Figure 3.6(a).A gated leakage PMOS transistor is placed between the output and the pull-down circuitry in the GALEOR approach, and a gated leakage NMOS transistor is inserted between the output and the pull-up circuit. The pull up and pull down networks are coupled to the leakage reduction transistors M3 and M2.

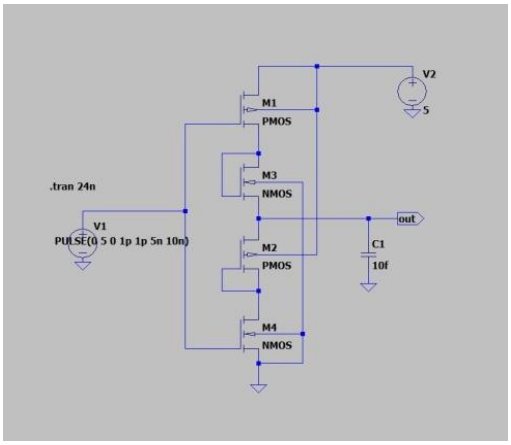

Fig.3.6(a) Circuit schematic of GALEOR

3.6.1 STATIC ANALYSIS

The upper value of output voltage at lowest input voltage is said to be $V_{OH.}$ and the value of output at highest value of input is said to be $V_{OL.}$ Similarly we can find V_{IL} and V_{IH} while plotting the plot of dVout/dVin , the value of Vin at which slope is -1.Its noise margin is calculated as 0.003.

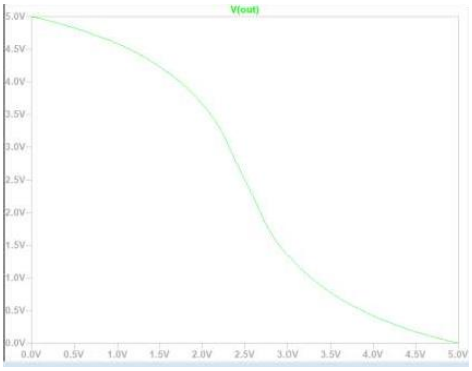

Fig.3.6(b)VTC of GALEOR

3.6.2 DYNAMIC ANALYSIS

Dynamic analysis is performed for the GALEOR based inverter by taking 10fF as reference capacitor at the output and it was found out that the delay of the logic is 0.2114ns. Which is more than the CMOS and comparable with the other inverter approaches.

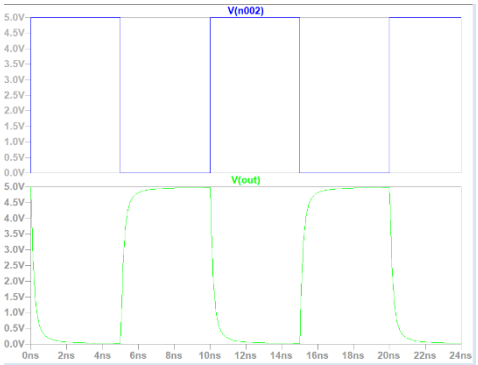

Fig.3.6(c) Input and output pulse of GALEOR

3.6.3 POWER ANALYSIS

DC analysis of the GALEOR based inverter is performed by sweeping input voltage from 0 to 5V and noticing the current flowing through the circuit. The power consumption of this approach was calculated as 288uW which is 12% less than the CMOS inverter

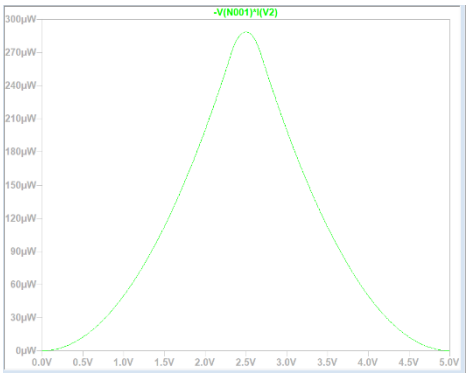

Fig.3.6(d) Power curve of GALEOR

Leakage is successfully minimized by this strategy. Nevertheless, the output signal levels are off since logic 0 is higher than ground and logic 1 is lower than Vdd. The absence of a precise definition for the predicted binary states might result in serious problems with circuit performance. Inadequate signal levels might lead to circuit faults in later stages, making the circuit unreliable to operations.

3.7 DRAIN GATING

The drain gated technique is used to address the issue when the output voltage level in the first two operations is marginally different from the input voltage level. The recommended circuit family, which may prevent problems and maintain the original signal quality, will be covered in this section. More sleep transistors provide less leakage current and can be placed between the pull up and pull down circuits. As depicted in fig3.7(a) For NMOS sleep transistor control, it is connected between the

pull-down and the network output while the PMOS sleep transistor is connected between the pull-up network and the network output. This has the advantage of minimizing the path resistance, needed to be conducted during sleep, hence enhancing the performance of the circuit. Since both sleep transistors are turned off during standby mode, leakage current is reduced substantially while increasing the resistance of the stack circuit to ground. [19].

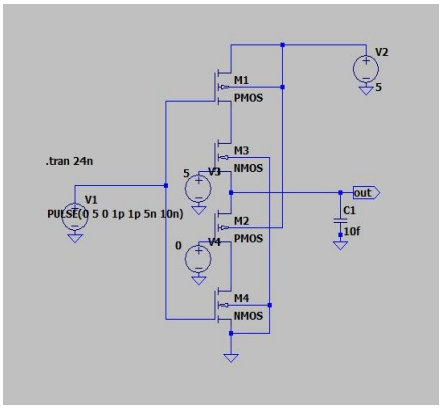

Fig.3.7(a) Circuit schematic of Drain gating inverter

3.7.1 STATIC ANALYSIS

This analysis is done by plotting between input voltage and output voltage. As we can see from the Fig.3.7(b) ,for the lower value of input voltage output will be high whereas for higher value of input voltage output will be low. Its noise margin will always be higher than the CMOS inverter because of more number of transistors. Its noise margin is calculated as 0.007. Which is very less as compare to CMOS inverter

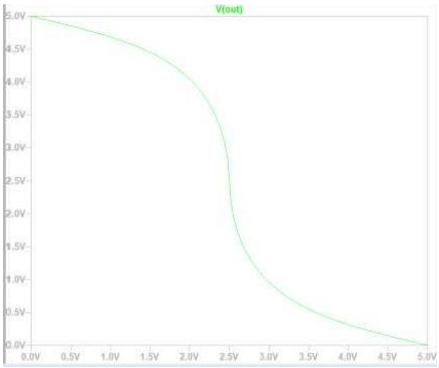

Fig.3.7(b)VTC of Drain gating inverter

3.7.2 DYNAMIC ANALYSIS

Dynamic analysis is performed for the drain gating based inverter by taking 10fF as reference capacitor at the output and it was found out that the delay of the logic is 0.198ns. Which is more than the CMOS and lesser than the other approaches.

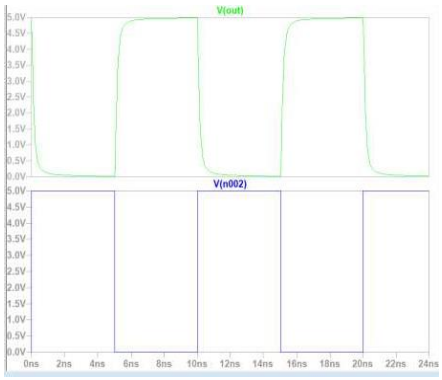

Fig.3.7(c) Input and output pulse of Drain gating inverter

3.7.3 POWER ANALYSIS

DC analysis of the GALEOR based inverter is performed by sweeping input voltage from 0 to 5V and noticing the current flowing through the circuit. The power utilization of this approach was calculated as 311uW which is 5% less than the CMOS inverter

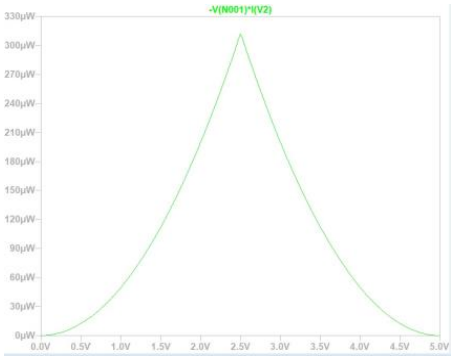

Fig.3.7(d) Power curve of Drain gating inverter

Since the sleep signal is now ‘on’, you need to free the processor from both the pull-up and pull-down networks. Off mode for the sleep signal diminishes the leakage current with the help of stacking effect caused by drain gating transistors. The consumption rate of dynamic power is lower. Switching pull-up and pull-down networks takes place even when the nets aren’t connected to the output thereby implying that the dissipation of power takes place constantly. The other one is the increased total dissipation of power.

3.8 VARIABLE BODY BIASING METHOD

Traditionally, the body terminals of PMOS are linked to Vdd while the body terminals of the NMOS are connected to ground to keep the threshold voltage (Vth) in a static CMOS arrangement.The PMOS body is coupled to a positive body biased (+VBB) in the VBB approach, increasing the PMOS's Vth when in standby mode. Due to the body-bias effect in static mode, NMOS body was linked in negative body biased (-VBB) to boost the Vth.Raising the threshold voltage will have an impact on performance, and the VBB approach controls the body to apply a different input voltage supply, resulting in a smaller reverse bias during active operation and a larger reverse bias during standby. Consequently, it may be lowering the static power dissipation and sub-threshold leakage current[18].

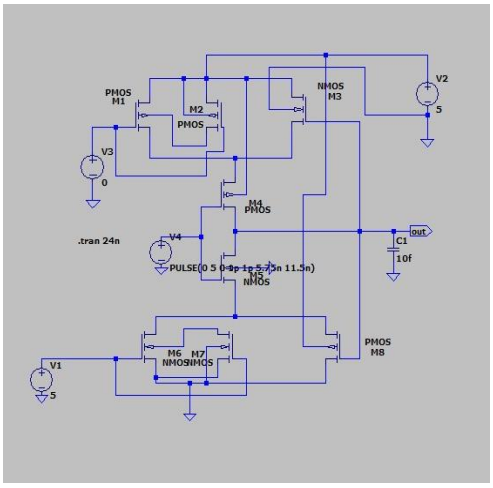

Fig.3.8(a) Circuit schematic of Variable body biasing based inverter

3.8.1 STATIC ANALYSIS

DC analysis is performed by sweeping input voltage from 0 to 5V and Vout vs Vin plot is studied and the noise margin value was calculated as 0.002 which is similar is MTCMOS and LECTOR but quite low as compare to CMOS inverter.

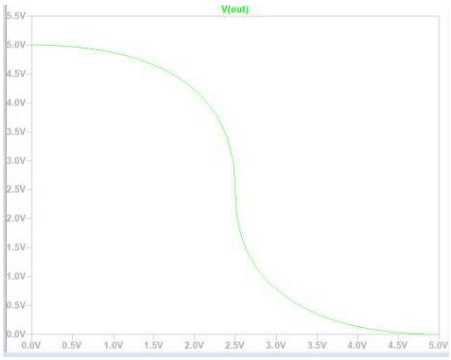

Fig.3.8(b)VTC of Variable body biasing based inverter

3.8.2 DYNAMIC ANALYSIS

Dynamic analysis is performed for the variable body biasing based inverter by taking 10fF as reference capacitor at the output and it was found out that the delay of the logic is 0.2090ns. Which is more than the CMOS and comparable with the other inverter approaches.

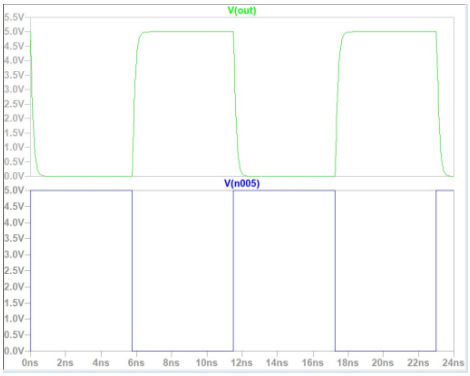

Fig.3.8(c)Input and output pulse of Variable body biasing based inverter

3.8.3 POWER ANALYSIS

This technique uses the concept of body biasing for reducing power consumption.The power dissipation is calculated and the value is 300uW which is about 9% less than the CMOS inverter .

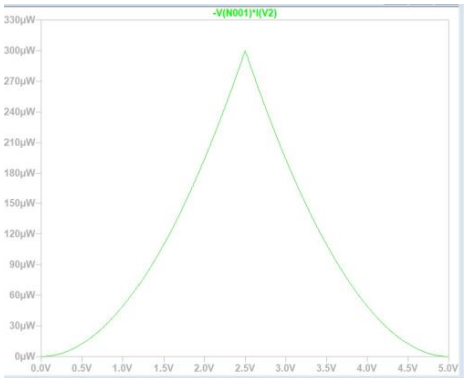

Fig.3.8(d) Power curve of Variable body biasing based inverter

The sub threshold leakage current is reduced as a result of increasing threshold voltages caused by variations in the sleep transistors' base voltages. The circuit's area will be comparatively larger as its complexity increases.Additionally, there is a propagation delay at the output of the VBB approach. The increase in standby mode delay is caused by a decrease in output driving capability as a result of the device's threshold voltage being raised through the usage of the VBB approach.

3.9 ON/OFF LOGIC APPROACH (ONOFIC)

Leakage current in logic circuits operating in both active and standby modes is effectively decreased using the ONOFIC technique. In order to reduce leakage, it included additional logic between pull-up and pull-down networks. This newly added logic circuit is known as On/Off logic (ONOFIC) The circuit. This is ONOFIC phase explores one NMOS transistor and one PMOS transistor . This circuit is known as ONOFIC as that will maintain a state of on or off to each of the output logic level. This logic directly impacts the propagation delay and power consumption in the otherwise complex logic circuit. The leakage current is

controlled through Force Stacking logic of ONOFIC circuit, to offer the maximum resistance when ONOFIC blocks is off and minimum resistance when the block is on. In the ONOFIC block, PMOS transistor gates the NMOS transistor from operation. Based on the output logic, ONOFIC NMOS or PMOS transistors need to operate either in linear mode and/or cut-off mode. In the current mode, the drain of the transistor PMOS is connected to the gate of the transistor NMOS; the output signal of the block ONOFIC is connected to the gate of transistor PMOS. The circuit's VDD link to the source terminal of the PMOS transistor and, on the other side, the source of the NMOS transistor links to the pull-down network drain. On this case ONOFIC transistors are both in a cut-off region, while the ONOFIC logic is off; And the linear region when ONOFIC's logic is ON .In both active and standby modes, this lowers leakage current while maintaining an accurate logic level at the output[16].

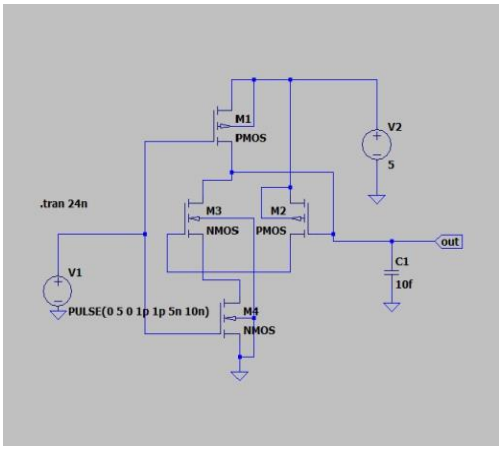

Fig.3.9(a) Circuit schematic of ONOFIC inverter

3.9.1 STATIC ANALYSIS

This analysis is done by plotting between input voltage and output voltage. As we can see from the Fig.3.9(b) ,for the lower value of input voltage output will be high whereas for higher value of input voltage output will be low. Its noise margin will always be higher than the CMOS inverter because of more number of transistors. The noise margin was calculated as 0.03 which is lower than the CMOS.

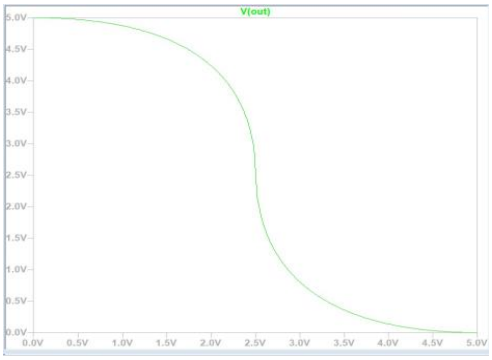

Fig.3.9(b) VTC of ONOFIC inverter

3.9.2 DYNAMIC ANALYSIS

Dynamic analysis is performed for the variable body biasing based inverter by taking 10fF as reference capacitor at the output and it was found out that the delay of the logic is 0.2029ns. Which is more than the CMOS and comparable with the other inverter approaches.

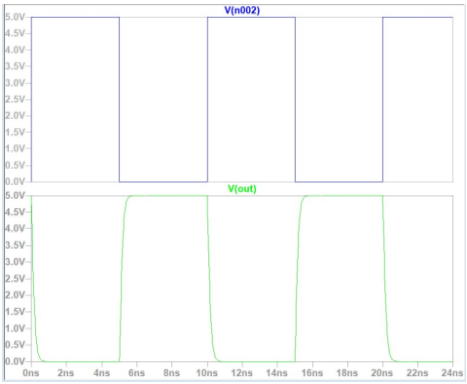

Fig.3.9(c) Input and output pulse of ONOFIC inverter

3.9.3 POWER ANALYSIS

The DC analysis of ONONFIC based inverter is performed and it was found out that the value of power dissipation is 312uW which is about 4.8% lesser as compare to the CMOS inverter.

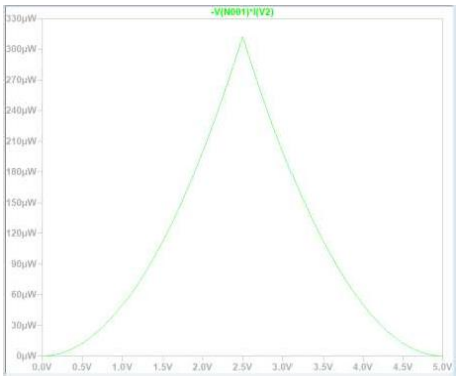

Fig.3.9(d) Power curve of ONOFIC inverter

The On/Off logic (ONOFIC) approach uses a straightforward, single threshold voltage circuit level approach to reduce leakage current and leakage power. Leakage current in logic circuits operating in both active and standby modes is effectively decreased using the ONOFIC technique. The logic circuit's propagation latency and power dissipation are directly impacted by this logic. The ONOFIC approach can enhance the functionality of logic circuits by maintaining a constant threshold voltage across the whole block.Straightforward construction in the pullup and pulldown paths, a single NMOS. Due to a single additional transistor (NMOS) in the pullup and pulldown network's path, there is also reduced delay. Reduction of leakage is not very good.

3.10 DYNAMIC LOGIC SUPPRESSION

The DLSL inverter in Figure 2.10(a) uses two additional leakage suppression transistors, namely MNT (NMOS, which is connected between PMOS and Vdd) and MPB (PMOS, which is connected between NMOS and ground), to achieve fW/gate leakage power. DLSL is a logic-level leakage reduction technique. Feedforward

leakage suppression logic (FLSL), which uses an input-forward method and dual-rail logic style, was developed as a way to improve the switching speed of DLSL[13-14]. The circuit uses M1 and M4 to feed back the output voltage. Vout=5V is given to M4, which causes the M3 transistor to switch off when V2=0 output voltage leaks via the pull-down channel. The output, which is 0V when Vin=VDD, is sent back to M1, and M4 links the output to the ground channel. However, because the pull-up path is in the cut-off state , the leakage current is reduced.

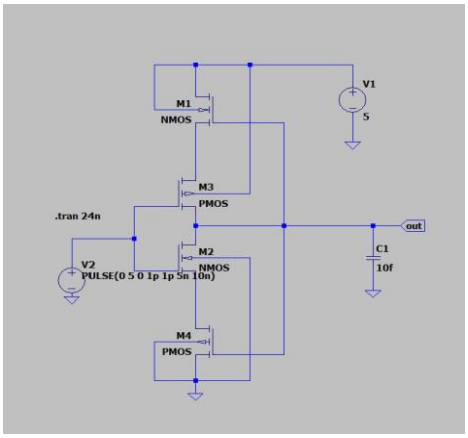

Fig.3.10(a) Circuit schematic of Dynamic logic suppression inverter

3.10.1 STATIC ANALYSIS

Just like other approaches this approach also shows low value of noise margin which means it is more susceptible to noise. After doing DC analysis of the circuit it was found out that the value of noise margin is 0.008 which is quite low.

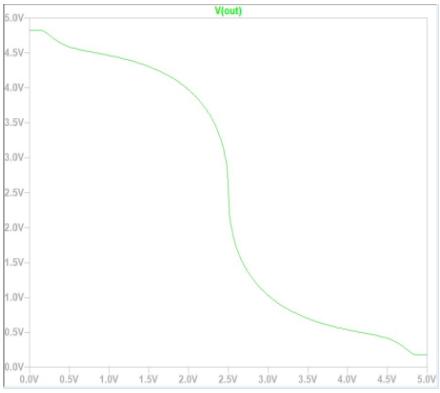

Fig.3.10(b) VTC of Dynamic logic suppression inverter

3.10.2 DYNAMIC ANALYSIS

Transient analysis is performed and input and output signal is plotted with respect to time.10fF reference capacitor is taken as reference load at the output. After the analysis it was found out that the value of delay is 0.2233ns which is more than other approaches.

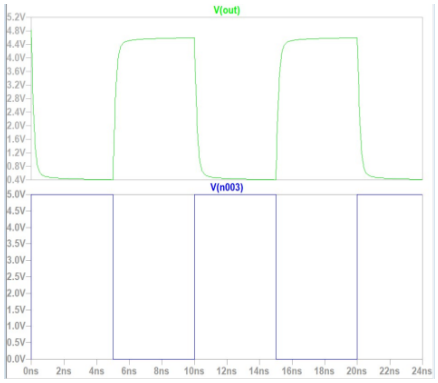

Fig.3.10(c) Input and output pulse of Dynamic logic suppression inverter

3.10.3 POWER ANALYSIS

This approach shows the best performance in terms of power dissipation. DC analysis is performed by sweeping input voltage and calculating the current through the circuit.The value of power dissipation was found out to be 186uW which is about 43% less than the CMOS inverter.

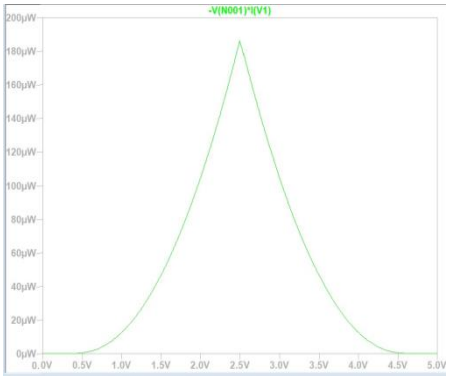

Fig.3.10(d) Power curve of Dynamic logic suppression inverter

Its architecture is straightforward. The varied rise and fall times for input and output are caused by an increase in the static noise margin as a result of the cut off. While DLSL exhibits excellent self-suppression of leakage at 180 and 130 nm, its capacity to suppress leakage is somewhat reduced between 28 and 7 nm, and its ability to suppress leakage is severely hampered in the remaining technology nodes. With the advancement of technology , DLSL performs much better. This is particularly true for 28 nm FinFET and HPC technology , where it operates 2-3 orders of magnitude quicker than in 180 nm. Nevertheless, when constructing circuits based on DLSL, it is important to keep in mind that DLSL are susceptible to changes in temperature and process.

3.11 LEAKAGE CONTROL NMOS TRANSISTOR(LCNT)

This technique minimizes the leakage current in CMOS logic gates at the circuit level.With this method, an extra NMOS transistor is inserted after the pull-down part. This extra NMOS transistors is used to significantly reduce leakage power. Notably, there is no need for any extra inputs because the inserted NMOS transistor acts as a self-controlled element. All that is needed is for the NMOS transistor to get feedback from the output. This process is known as NMOS transistor leakage control (LCNT). Considering that, as seen in Fig. 4, it makes use of 2 N-type leakage control transistor, LCT1 and LCT2, which are placed between pullup network and pull down network. Both LCT1 and LCT2's gate terminals are connected to NP, the output node.The sleep transistors in the sleep-related approach must be able to separate the gate's power source or/and ground from the other transistors. They must thus be made bigger in order to dissipate more dynamic power. This cancels out the savings that occur from the circuit being idle. The input vector-dependent sleep transistor technology requires extra circuitry to monitor and regulate the sleep transistor switch, which uses power in the idle and active modes. By contrast, LC nMOS is vector independent and produces the necessary control signals inside the gate[15].

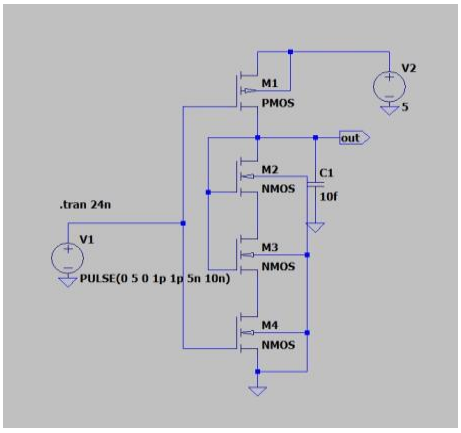

Fig.3.11(a) Circuit schematic of LCNT inverter

3.11.1 STATIC ANALYSIS

DC analysis is performed by sweeping input voltage from 0 to 5V and Vout vs Vin plot is studied and the noise margin value was calculated as 0.365 which is the best than the other approaches. Hence it has the highest marign in terms of susceptibility to noise.

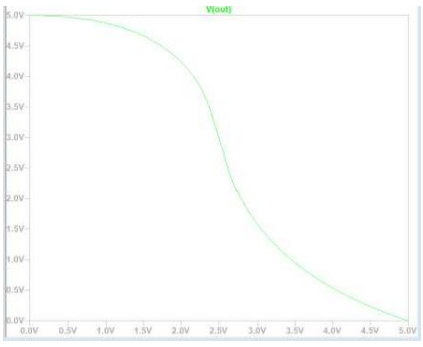

Fig.3.11(b)VTC of LCNT inverter

3.11.2 DYNAMIC ANALYSIS

Dynamic analysis is performed for the leakage control NMOS transistor based inverter by taking 10fF as reference capacitor at the output and it was found out that the delay of the logic is 0.2122ns. Which is more than the CMOS and comparable with the other inverter approaches.

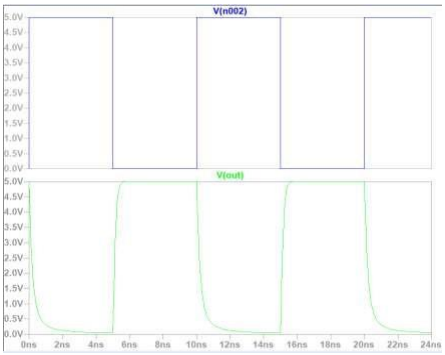

Fig.3.11(c) Input and Output pulse of LCNT inverter

3.11.3 POWER ANALYSIS

Power analysis is performed by studying DC analysis of the circuit. Input voltage is sweeped from 0 to 5V , current through the circuit vs input voltage is plotted and it is used to calculate the power dissipation. Power was found out to be 300uW, which is about 9% less than the CMOS inverter.

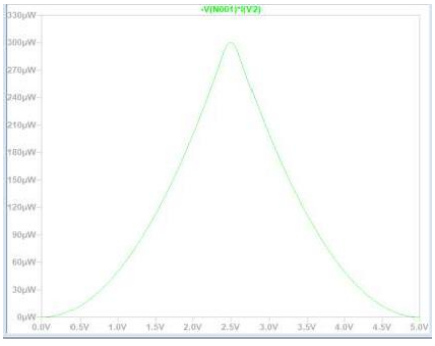

Fig.3.11(d) Power curve of LCNT inverter

The logic high in the case of LCNT is good and getting close to optimal transfer qualities. But the logic here is weak. The primary benefit of the LCNT approach over other methods is that it does not require any extra circuitry for control or monitoring, which minimizes both the space and the amount of power dissipated when the technique is operating.

Minimal leakage because NMOS transistors are stacked in a pull-down route, they offer strong resistance to leakage current. There is no usage of standby mode of operation.By employing this method, area is increased. Because of these intermediary leakage transistors, the output delay increases.

3.12 HYBRID POWER GATING

The lector technique and the drowsy stack keeper technique from before are combined to create the new method. In this case, the pull-up and pull-down networks are positioned above and below the sleep PMOS and sleep NMOS transistors (S & S Bar). The purpose of stacking the pull up and pull down devices is to reduce the circuit's leakage power. Because NMOS operates more quickly than PMOS, its aspect ratio (W/L) is lower.The keeper circuit's gate terminal is connected to the output port, and it is positioned in parallel with the sleep transistor (S & S Bar). When the sleep transistors (S & S Bar) are given the logic '0' and '1' in the active mode (AM), they both turn on. Virtual nodes (Vdd) and Vss are drawn up to the power potential and down to the ground potential, respectively. In this case, the pull-up and pull-down devices have very little resistance from either sleep transistor. It will be possible to reduce power supply fluctuations by combining sleepy and stack transistors. Here, the keeper circuit is used to increase the CMOS circuit's speed. Both the sleep PMOS and NMOS transistors are off during sleep mode (SM). Both the virtual Vdd node potential and the virtual Vss node potential are isolated from the power potential and the ground potential, respectively. In this case, the pull-up and pull-down devices are highly resistant to both sleep transistors. This pull-up network and pull-down device give very high resistance while in sleep mode and have no connecting path. Using the power gating approach, a high-speed, low-power CMOS circuit with increased performance is envisioned[17][24].

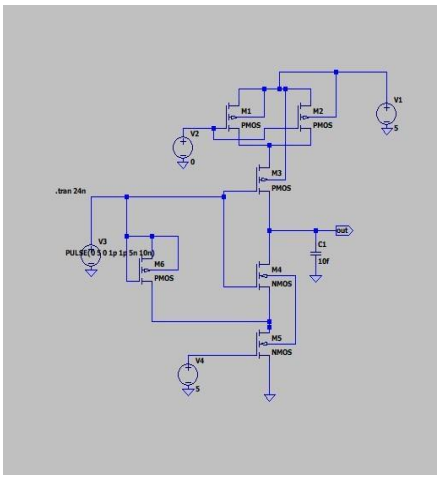

Fig.3.12(a) Circuit schematic of Hybrid power gating based inverter

3.12.1 STATIC ANALYSIS

This analysis is done by plotting between input voltage and output voltage. As we can see from the Fig.3.12(b), for the lower value of input voltage output will be high whereas for higher value of input voltage output will be low. Its noise margin will always be higher than the CMOS inverter because of more number of transistors. The noise margin was calculated as 0.03 which is lower than the CMOS.

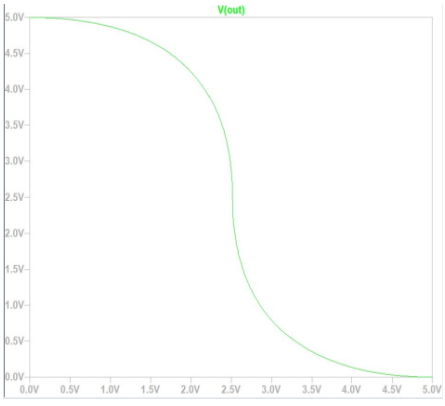

Fig.3.12(b)VTC of Hybrid power gating based inverter

3.12.2 DYNAMIC ANALYSIS

Transient analysis is performed and input and output signal is plotted with respect to time.10fF reference capacitor is taken as reference load at the output. After the analysis it was found out that the value of delay is 0.2071ns which is less than other approaches.

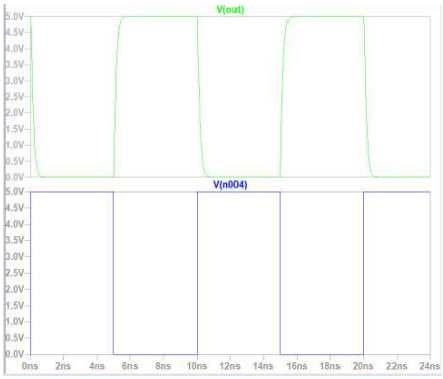

Fig.3.12(c) Input and Output pulse of Hybrid power gating based inverter

3.12.3 POWER ANALYSIS

This approach shows the best performance in terms of power dissipation. DC analysis is performed by sweeping input voltage and calculating the current through the circuit.The value of power dissipation was found out to be 186uW which is about 43% less than the CMOS inverter.

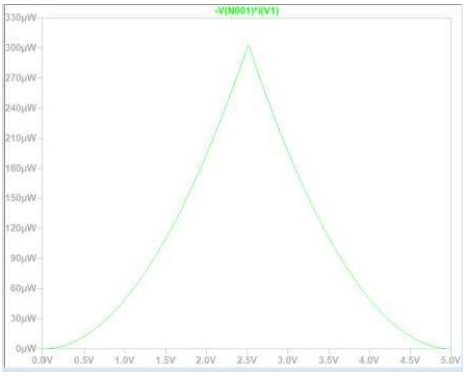

Fig.3.12(d)Power curve of Hybrid power gating based inverter

Through a PMOS feedback MOSFET, leakage current from the pull-down network is sent back into the pull-up network. By feeding back the ON-state leakage current, it reduces the dynamic power dissipation. Switching speed is increased at the pull-up network side by parallel linked PMOS. The circuit's area is comparatively larger. The circuit's Output Delay rise.

CHAPTER 4

DESIGN AND ANALYSIS OF LOW POWER CMOS INVERTER

4.1 MY PROPOSED DESIGN

This method is created by fusing two already-existing strategies, stacking and hybrid power gating. The pull up network and Vdd are connected to the two NMOS transistors that are connected in parallel. Switching speed is increased at the pull-up network side by parallel linked NMOS. In contrast, the pull-down network is coupled to the PMOS transistor. The pull-down NMOS is coupled in series with the PMOS transistor, which functions as a stacked transistor. When more than one transistor in a stack of series-connected transistors is turned off, the sub-threshold leakage current through the stack drops. The term "stacking effect" or "self reverse bias" refers to this phenomenon. The voltage at each of the transistor's four terminals determines the leakage currents in NMOS or PMOS transistors exponentially. The intermediate voltage drops when the transistor M2 is turned off.Due to a tiny drain current and PMOS, which is connected between NMOS(M2) and ground, the node is positive. There will be a tiny voltage loss between NMOS (M2) and ground because PMOS has a modest on resistance as long as it is constantly on (M4). The intermediate node's positive potential has the following three effects:

The sub-threshold current significantly decreases as a result of transistor M2's gate to source voltage (VGS2) being negative due to its positive source potential.

Transistor M2 experiences a negative body to source potential (VBS2) when VM > 0, which raises M2's threshold voltage (bigger body effect) and lowers sub-threshold leakage. As a result of VM> 0, transistor M1's drain to source potential (VDS2) drops, increasing M2's threshold voltage (less DIBL) and lowering sub-threshold leakage.

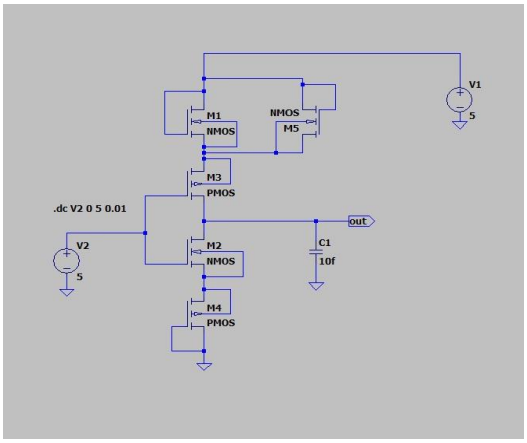

Fig.4.1(a) Circuit schematic of proposed inverter

4.1.1 STATIC ANALYSIS

Plotted between input voltage (Vin) and output voltage (Vout), the voltage transfer curve, or VTC , is a commonly used tool for evaluating the quality of an inverter. The static characteristics can be used to to determine device parameters like as gain, noise tolerance, operating logic levels, and noise. Fig4.1(b) shows the static characteristic plot of the proposed inverter. It can be seen that, for lower value of Vin the output voltage (Vout) is high whereas for higher value of input voltage (Vin) the output voltage is low. The value of VOH can be found out by taking the value of Vout when Vin is 0 whereas VOL can find out by taking the value of Vout when Vin is high or Vdd. After the calculation of VOH and VOL, VIL and VIH can be found out by plotting dVout/dVin vs Vin and by taking the value of Vin where dVout/dVin is -1. Hence noise margin can be calculated by taking the difference between NMH i.e., difference between VOH and VIH and NML i.e., difference between VIL and VOL.Noise margin of the proposed inverter is calculated as 0.2V. Noise margin of this inverter is comparable with CMOS inverter which is a good thing as it is more susceptible to the noise.

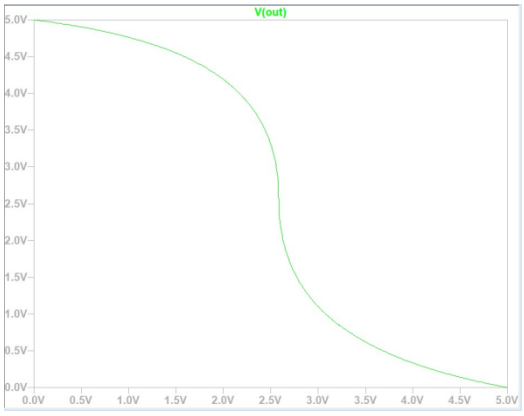

Fig.4.1(b) VTC of proposed inverter

4.1.2 DYNAMIC ANALYSIS

Dynamic analysis is performed for calculating the delay of a logic circuit. The difference in time (measured at 50% of input-output transition) when the output switches following the application of input is know as propagation delay of a logic gate. Other parameter can be find out using this analysis such as rise time ,fall time etc.The delay was calculated as 0.1954 which is best while comparing with other approaches other than CMOS inverter.

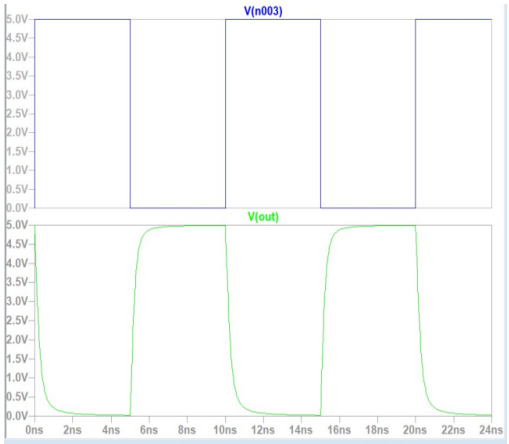

Fig.4.1(c)Input and Output pulse of proposed inverter

4.1.3 POWER ANALYSIS

The power dissipation is one of the most important parameters in a logic circuit. As the devices are narrowing down day by day which reduces the threshold voltage and due to that leakage power is increases. All the approaches is studied and was found out that the dynamic logic suppression has the best numbers in terms of power. Whereas the proposed design has a power dissipation of 200uW which is the second best among all. It has 39% power dissipation less than the CMOS inverter.

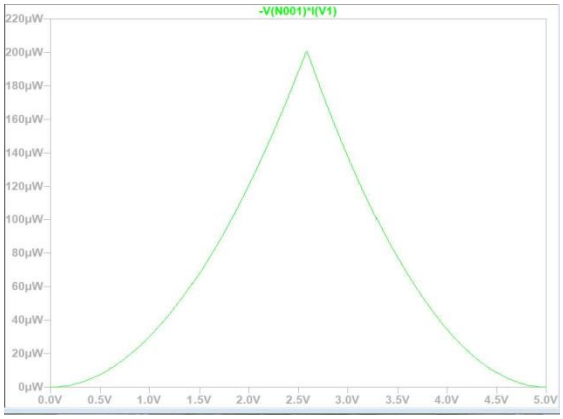

Fig.4.1(d) Power curve of proposed inverter

TABLE4.1 COMPARISON OF DIFFERENT INVERTER CONFIGURATION

Circuit name	Transistor count	Max power dissipation(u W)	Delay(ns) (CL=10f F)	NMh	NMl	Integration of power curve
CMOS inverter	2	328.05001	0.167	1.791	1.961	109.72µW
MTCMOS	4	300.06	0.2090	1.872	1.874	101.03µW
LECTOR	4	304.054	0.2169	1.754	1.756	104.09µW
Sleepy keeper approach	6	300.06	0.20885	1.872	1.874	99.03µW
Sleep Circuitry Embedded CMOS Circuit.	5	268.3605	0.20265	1.874	1.85	100.23uw
GALEOR	4	288.46	0.2114	1.645	1.648	103.57µW
Drain Gating	4	311.935	0.19815	1.909	1.916	104.17µW
Variable Body biasing method	8	300.06	0.2090	1.872	1.874	101.03µW

On/Off logic approach (ONOFIC)	4	312.3675	0.20295	1.846	1.876	105.17µW
Dynamic Logic Suppression Logic	4	186.24	0.2233	1.829	1.82115	49.853µW
LCNT	4	300	0.2122	1.511	1.876	104µW
Hybrid power gating(HPG)	6	302.41	0.2071	1.857	1.891	101.79µW
Proposed inverter	5	200.29107	0.1954	1.794	2.020	67.052µW

CHAPTER 5

GaN vs Silicon based device

Silicon has been the cornerstone of semiconductor technology for around 50 years. Nevertheless, during the course of nearly 50 years, experts and manufacturers have made enormous advancements in silicon production, semiconductor applications, and integrated circuit design. Researchers are getting close to the theoretical limit of silicon-based semiconductors, based on Moore's Law. For a variety of reasons, researchers and for a long time, semiconductor producers have searched for more dependable substitutes for silicon, even though silicon semiconductor substrate is ideal for a wide range of electronics applications. Gallium nitride, or GaN, has become a formidable rival to silicon, despite the fact that these researchers have had differing degrees of success throughout the previous few decades[26].

5.1 GALLIUM NITRIDE CRYSTAL STRUCTURE

Gallium nitride is a semiconductor with a wurtzite crystal structure that is produced using metal-organic chemical vapour deposition (MOCVD). This structure is exceptionally solid and includes a tall softening point, 4531 °F, building it reasonable for semiconductor base materials in high-temperature settings.GaN's structure will acknowledge magnesium to create an n-type semiconductor. Gallium and nitrogen come together in this step to produce the crystal.There are many other combinations for this synthesis, however one example of GaN synthesis uses trimethyl gallium as the source of gallium and ammonia(NH3) as the nitrogen source. The crystalline structure of GaN exhibits some nonuniformity, with a few million flaws per centimetre at times. But the most advanced MOCVD methods can now generate and use larger GaN crystals as wafers because they can lower the number of flaws per centimetre to anywhere from 110 to 1010. When GaN is synthesised with a low degree of error, it possesses certain unique crystalline features that make it a desirable molecule for semiconductor applications[26].

5.2 BANDGAP OF SEMICONDUCTOR

Gallium nitride's bandgap, which provides it with a variety of electrical properties that prepare it for greater power applications, is one of its greatest benefits over silicon. The bandgap of silicon is only 1.1 eV, whereas that of gallium nitride is 3.2 eV. With a bandgap about three times larger than silicon's, GaN needs a lot more energy in order to excite a valence electron into the conducting band of the semiconductor. Due to this characteristics, Gan cannot be used in very low voltage applications, but at higher temperatures, it permits GaN to have bigger breakdown voltages and greater thermal stability[26].

5.3 GaN BREAKDOWN FIELD

The breakdown field of silicon is 0.3MV/cm, whereas the breakdown field of GaN is 3.3MV/cm. Gallium nitride can therefore withstand high voltage devices ten times longer before failing. Gallium nitride is better than silicon in high voltage circuits, such as high-power devices. GaN has a far reduced environmental impact and can be used in comparable voltage applications by engineers and manufacturers. In contrast, silicon has a power density that is far higher[26].

5.4 SILICON vs GaN ELECTRON MOBILITY

Gallium nitride exhibits a 2010 cm2/Vs electron mobility balanced to 1510 cm2/Vs for silicon. As a result, gallium nitride crystals' electrons can move more than 31% more quickly than those of silicon. Because of its greater electron mobility compared to silicon, gallium nitride has a clear advantage when it comes to RF components.

5.5 THERMAL CONDUCTIVITY COMPARISION

This makes the heat dissipation of gallium nitride worse than that of silicon, which is one of the cons. In their performance characteristics, gallium nitride has a high thermal conductivity of 1. Here most metals have the heat conductivity of 1.31 W/cmK, while silicon has only 1.50 W/cmK. At higher comparison voltages the efficiency of the GaN reduces the thermal loads induced by the circuit, though it may not be as well equipped to handle thermal loads as silicon in the same way that

silicon is not as well equipped to handle high voltages as GaN. Here's an illustration of the thermal conductivity difference in action: EPC Corporation compares a MOSFET with a 12V/12A GaN FET at 120V and shows a 40% reduction in power loss. Thus, the GaNFET consumes less energy and operates at a temperature that is almost ten degrees lower[26].

5.6 MANUFACTURIBILITY OF SILICON AND GaN

The manufacturing method of gallium nitride is a technological hindrance, particularly in comparison to the extensively used and commoditized silicon manufacturing process. For instance, a large number of crystal flaws are distributed across a limited area in gallium nitride. In contrast, silicon has a low defect density of up to 100 per square centimetre. Engineers had never been able to produce GaN substrates with less than one billion defects/cm until this century. Clearly, considering the majority of semiconductor manufacturing design requirements, this enormous number of defects/area is quite useless. Even though the amount of flaws has decreased to more efficient levels because to improved production procedures, the cost of producing the same quantity of GaN wafers is still higher than that of silicon[26].

TABLE5.1 COMPARISON OF PREOPERTIES OF GaN AND SILICON

Silicon vs Gallium Nitride		
Properties	Silicon	Gallium Nitride
Thermal conductivity	150 to 200 W/m.K	100 to 180 W/m.K
e- mobility	1500 cm2/Vs	800 to 2000 cm2/Vs
Breakdown voltage	600 to 900 V/μm	600 to 1200 V/μm
Bandgap	1.1eV	3.4eV
Power density	low	High
Switching speed	Slow	Fast

5.7 SIMULATED SILICON BASED DEVICE

Electronic signals can be amplified or switched using a transistor called a metal-oxide-semiconductor field-effect transistor (MOSFET). A conducting channel between the source and drain contacts of a MOSFET can be induced by a voltage applied to the oxide-insulated gate electrode. The channel is referred to as a nMOSFET or a pMOSFET depending on whether it is n-type or p-type. Modern electronics relies heavily on Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), which are silicon-based devices. Thus, by using TCAD tools, including Silvaco TCAD, different characteristics of these devices can be simulated, which can lead to the optimization of their performance. The procedure of simulating a silicon-based MOSFET with the help of Silvaco TCAD involves the following steps: setting of electrical simulations, definition of a physical structure of the device, and the analysis of results. You can also adjust the features of a device progressively in accordance with specific performance characteristics. This process is crucial when it comes to the realization of innovative semiconductors devices for the electronics industry.

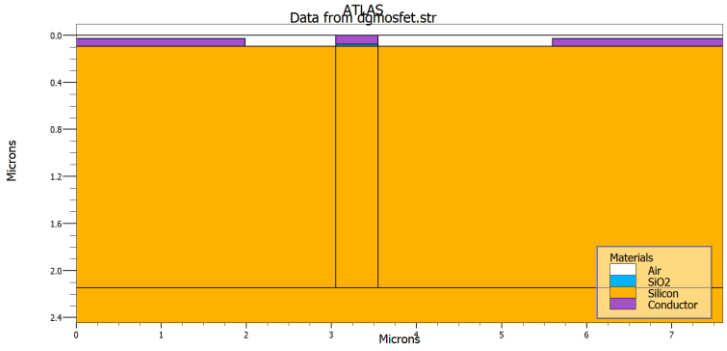

Fig.5.7(a) Structure of simulated NMOS using TCAD

The device is having channel length of 0.5um or 500nm.The device is simulated by taking doping concentration of 2*e16. The electrode materiel which is used in gate source and drain is having a work function of 5.15 eV.As the doping concentration of the mosfet increases , it increases the current through it.

5.7.1 OUTPUT CHARACTERISTICS

The conduction is carried out by the flow of electrons where they are attracted to the surface when the voltage at the top contact (the gate) is increased. The value of the electron concentration at the SB is higher than the hole concentration at a definite value of the voltage. Just beneath it, or directly at the gate voltage, the surface has switched from the p-type substrate of the original Si to the formation of an n-type inversion layer or inversion region. This inversion zone, which is the equivalent of a charge sheet at the gate interface, has a very small thickness. This is the voltage at which the surface inversion layer is formed in a field-effect transistor and is known as Vth; threshold voltage.

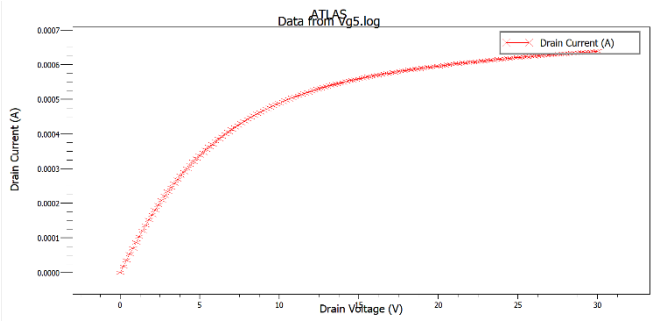

Fig.5.7.1(a) Output characteristics of NMOS using TCAD

The device is simulated for Gate voltage of 16V and drain voltage is sweeped from 0 to 30V.The uneven graph is due to model difference and meshing.

5.8 SIMULATED GAN BASED DEVICE

This device has been adapted from [25]. Due to the remarkable parameters of GaN materials and the high sheet concentration of 2DEG as a result of the polarisation effect, a alot of interest has been focused on the development of AlGaN/GaN-Based MISFETs since the last few years. In addition, GaN HEMTs have the features of low ON- resistance, high switching speed, high breakdown voltage, and thus they are recognized as good devices when constructing power converters with high conversion efficiency. Obtaining still higher breakdown voltage (BV) with a low on-resistance (Ron) remains a challenge.

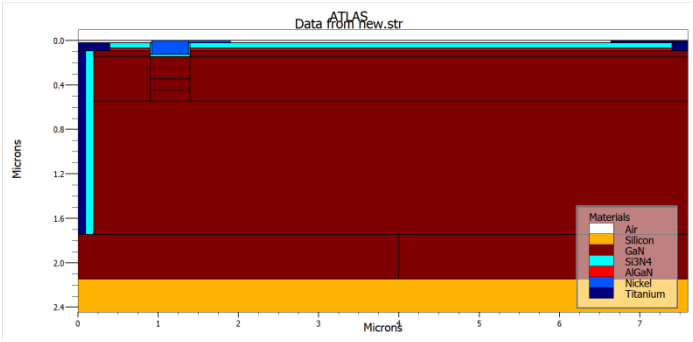

Fig.5.8(a) Structure of simulated NMOS using TCAD

Similar features is taken from the above silicon based NMOS such as channel length doping and gate work function.

5.8.1 OUTPUT CHARACTERISTICS

The output characteristic of the GaN based devuce is shown in fig 5.8.2(a).The threshold voltage of this device as seen from the simulation is between 2.5V to 2.9V, depending upon different tools and models. The higher Vth is due to higher band energy level under the gate induced by the floating top p- buried layer.

Similarly GaN based PMOS device is also simulated using the same features and it is simulated for Vgs=-16V and Vds is sweeped from 0 to -30V.

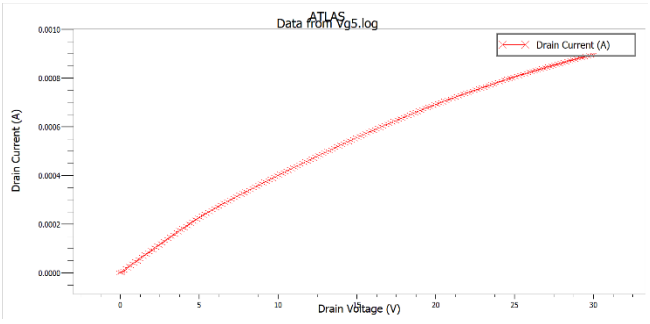

Fig.5.8.1(a) Output characteristics of GaN based NMOS using TCAD

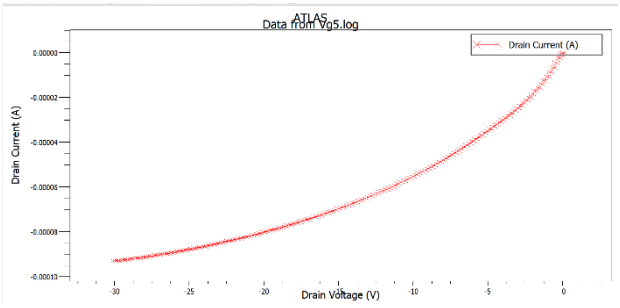

Fig.5.8.1(b) Output characteristics of GaN based PMOS using TCAD

CHAPTER 6

CONCLUSION AND FUTURE SCOPES

6.1 CONCLUSION

Leakage power is now a more significant portion of total power consumption in nanoscale CMOS circuits. Conventional CMOS circuit design results in significant increases in delay and high power dissipation. Several methods are used in the design of the CMOS circuit to get around the problem. The novel method is used to outline the CMOS circuit and analyze its power and delay. It was discovered in this work that the inverter's configuration and performance of various methods had been observed. The suggested design has the least amount of power after dynamic logic suppression technique. Dynamic logic suppression has the lowest power usage. Better in terms of delay and noise margin is the CMOS inverter which is quite obvious as the number of transistor is least. However, alternative layouts can be employed in applications where power is a critical component. As the number of transistor is increasing then device change comes in the picture. GaN and silicon based transistor properties has been observed and compared. It was found out that threshold voltage pf GaN device was between 2.5V-2.9V.

The different graphs were discovered with the use of LTspice.

6.2 FUTURE SCOPE

Minimizing electronic circuits is the goal of electronic design, which lowers power dissipation. Leakage power increases as a result of the technology node reduction due to reduce in threshold voltage.

It is evident from the comparison table above that the suggested design performs poorly in terms of noise margin, latency, and power dissipation. However, it is not the worst strategy out of the rest. Thus, future work can be done on the device level by using the device which has higher threshold voltage . As threshold voltage is inversely proportional to leakage power, so using a device having higher threshold

voltage can significantly decrease the power dissipation. The MOSFET has the threshold voltage of about 0.7V to 1.5V, using GaN device increases the threshold to 2.5V-2.9V.Using this device in the proposed inverter design can produce the power dissipation less than the designs using NMOS and PMOS.

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