A 12-Bit 1.2-GS/s Current-Steering DAC in 45-nm CMOS Technology

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I, Tarun Gupta**(2K22/VLS/22)**, a student of M.Tech **(VLSI Design & Embedded Systems)**, hereby declare that the project dissertation titled **"A 12-Bit 1.2-GS/s Current-Steering DAC in 45-nm CMOS Technology"** which is submitted by me to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other title or recognition.

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CERTIFICATE

I hereby certify that the Project Dissertation titled**"A 12-Bit 1.2-GS/s Current-Steering DAC in 45-nm CMOS Technology"** which is submitted by **Tarun Gupta (2K22/VLS/22)** in the partial fulfillment of the requirement for the award of Master of Technology in **VLSI Design & Embedded Systems** to the Electronics & Communication Engineering Department,Delhi Technological University,Delhi ,is a bonified work of the student carried out under my supervision.

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ABSTRACT

This research paper presents a 12-bit 8-4 segmented current-steering DAC (Digital-to-analog converter) that offers notable advantages, particularly in terms of its reduced power consumption compared to other similar designs. The exceptional performance of our DAC can be attributed to two key factors: the use of a thermometer encoder and efficient digital input bit segmentation. These features contribute to enhanced precision and reduced power requirements, setting our DAC apart from existing solutions in the field. DACs are the essential component that bridge gap between the advancing methods of digital signal processing and analog signal transmission in advance communication systems. A 8-4 segmented current steering architecture is proposed where 8 most significant bits (MSB) are implemented using thermometer encoded current cell array while 4 least significant bits (LSB) are implemented using binary weighted current cell architecture. Major sub-components of circuit involve inverter, logic gates for binary -to-thermometer encoder, latch, switch driver and multiple current sources. The designing and simulation of the circuit is done using Cadence Virtuoso and Power Dissipation is compared with other existing DAC designs in literature.These enhancements significantly reduce glitches and improve the accuracy of the DAC's output.DAC dissipates a total power of about 44.95 mW when running at a sample rate of 1.2 GHz with CMOS technology of 45nm. While the supply input voltage is held constant at 1.2 V, the DAC’s digital input is pulsating in nature in which the ON voltage is 1V and OFF voltage is 0V. Also, the DAC has a spurious-free dynamic range (SFDR) of 41.77 dB .

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LIST OF ABBREVIATIONS

ADC	Analog to Digital Converter
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital to Analog Converter
DSP	Digital Signal Processing
LSB	Least Significant Bit
MS	Master Slave
MSB	Most Significant Bit
RF	Radio Frequency
SFDR	Spurious Free Dynamic Range
Tplh	Propagation Delay for low to high output level
Tphl	Propagation Delay for high to low output level

CHAPTER 1
INTRODUCTION

1.1 Overview of DAC

A data converter known as a Digital to analog converter(DAC) transforms discrete N-bit data representations into physical quantities such as voltage or current. Fig.1.1 depicts the fundamental design of an Radio Frequency(RF) transceiver. High-quality Digital to Analog circuits are widely employed in transmission. The analog to digital converter is used in the reception path to transform the radio signal into a digital format that the Digital Signal Processing(DSP) can process. The DAC receives digital data from the DSP during transmission and transforms it into an analog signal that can be amplified and sent.

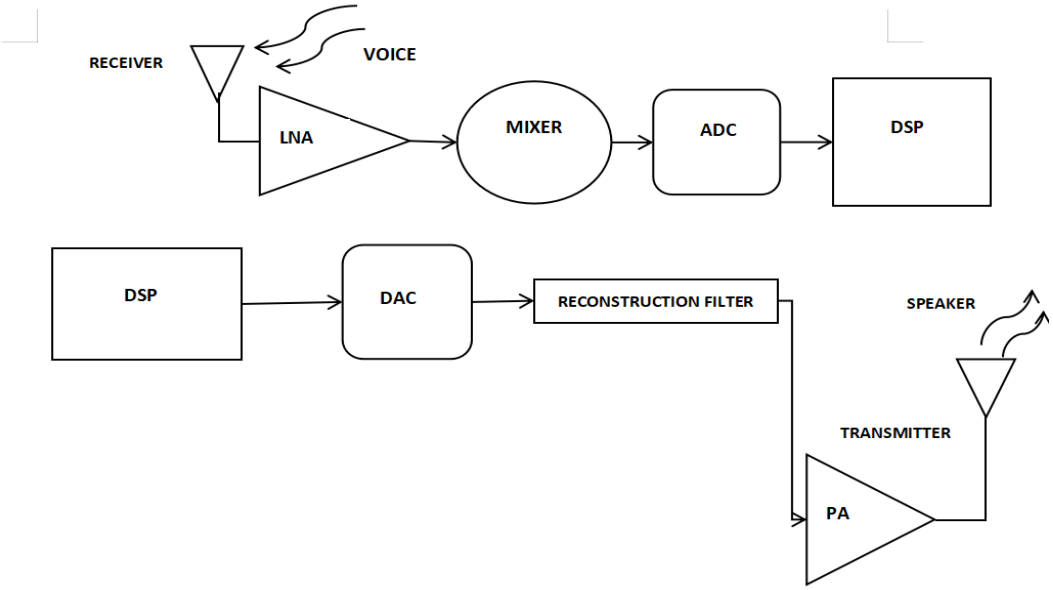

Fig.1.1: Basic representation of transceiver

An N-bit discontinuous representation of data can be converted to a physical quantity, such as current or voltage, using a data converter called DAC. A basic RF transceiver topology is shown above. High- quality DAC circuits are widely employed in RF transmission. In order to transform the radio signal into a digital format that the DSP can process, the receiver path uses an ADC. While in transmission, the DAC receives digital data from the DSP and transforms it into an analog signal

that can be transmitted and amplified.

1.2 DAC Architectures

A variety of circuits and architectures have been suggested for DACs throughout the years; a few of the widely used designs in the industry are covered below. Any design's primary goal is to map every input code exactly to an electrical output levels.

1.2.1 Resistor String DAC

It is the most straightforward construction to make advantage of the potential divider circuit principle. An entire set of 2M resistors are connected in series with one end grounded and the other connected to a reference voltage for an M-bit DAC [1]-[4]**.** These resistors are then linked to switches, the action of which is managed by the M:2M encoder for a 3-Bit DAC that is depicted in Fig.1.2. A potential divider voltage is seen at the output whenever a switch is turned on. The design's main advantages are its simplicity and good monotonicity; but, because of its many switches, mismatched resistors, and huge space need, it has a high parasitic capacitance.

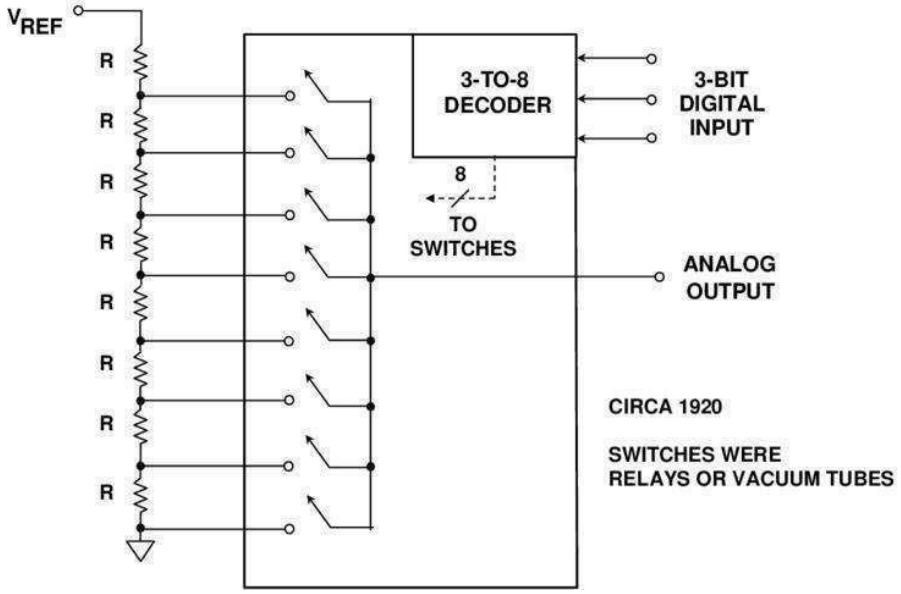

Fig.1.2: 3-Bit resistor string DAC

1.2.2 Binary Weighted Resistor String DAC

It is the most straightforward construction to make advantage of the potential divider circuit

principle. An entire set of 2M resistors are connected in series with one end grounded and the other connected to a reference voltage for an M-bit DAC [5]-[8].

These resistors are then linked to switches, the action of which is managed by the M:2M encoder for a 3-Bit DAC that is depicted in Fig.1.3. A potential divider voltage is seen at the output whenever a switch is turned on. The design's main advantages are its simplicity and good monotonicity; but, because of its many switches, mismatched resistors, and huge space need, it has a high parasitic capacitance.

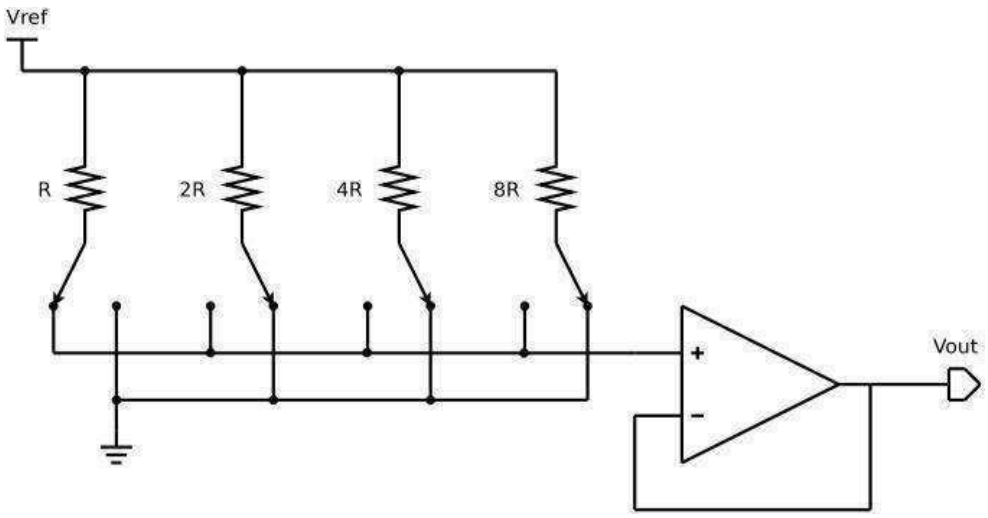

Fig.1.3: 4-Bit binary weighted resistor string DAC

1.2.3 R-2R DAC

This design, known as the R-2R ladder DAC because it only needs two resistance values, is an advance over the prior version. Comparing to the preceding two systems, an M-bit DAC requires less area to build since just 2M resistors are needed[9]-[12]. Depending on where the reference voltage is placed, the structure can be executed in voltage or current mode. R resistor is used to build the ladder, while 2R is used to form the rungs. At the structure, the resistance of Thevenin remains equal to R. An R-2R ladder for a 4-Bit DAC that operates in the present state is depicted in Fig.1.4, where switches are positioned between the output and ground and the resistance ladder is coupled to the reference voltage.

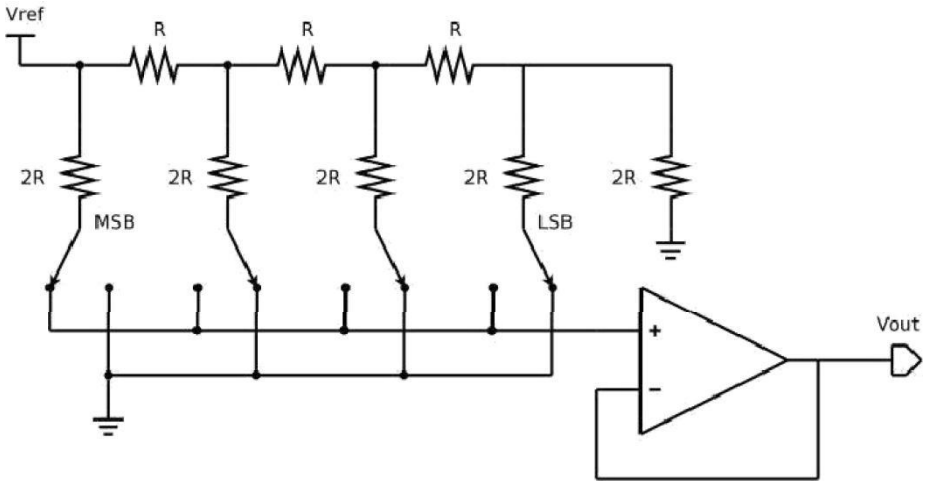

Fig.1.4: 4-Bit R-2R Ladder DAC

1.2.4 Current Steering DAC

In the proposed work, this topology-also known as a circuit designed for all seasons has been implemented. Because the architecture maintains a fast sample rate while in operation, it is most suitable for high-speed applications. Because of its higher output impedance and lack of need for a buffer, this kind of DAC performs better in static settings. Currently, steering topologies as shown in Figure 1.5 come in three varieties: segmented, unary weighted, and binary weighted. These all function by combining the current from every source of current. Digital logic activates a CS, allowing current to pass past the load opposition and sink into the CS. Voltage is created by doing this to the current. By using the voltage division rule, an analog signal gets generated across a load resistance.

Each current source in a unary DAC architecture is equivalent to one LSB, and a total of 2M current supplies are needed to build an M-bit DAC. In contrast, an M-bit DAC using binary weighted DAC requires M sources of current, each of which is a multiple of two of the preceding CS. Regarding area and accuracy, respectively, both binary and unary DACs are inferior. Therefore, segmented DACs that use both binary and unary current guiding components are proposed in order to find a balance. The ideal segmented ratio is 30:70, meaning that binary architecture is used to accomplish 30% of the overall resolution and unary architecture to implement 70% of it. In unary DAC, thermometer-encoded bits are utilized only to reduce static error.

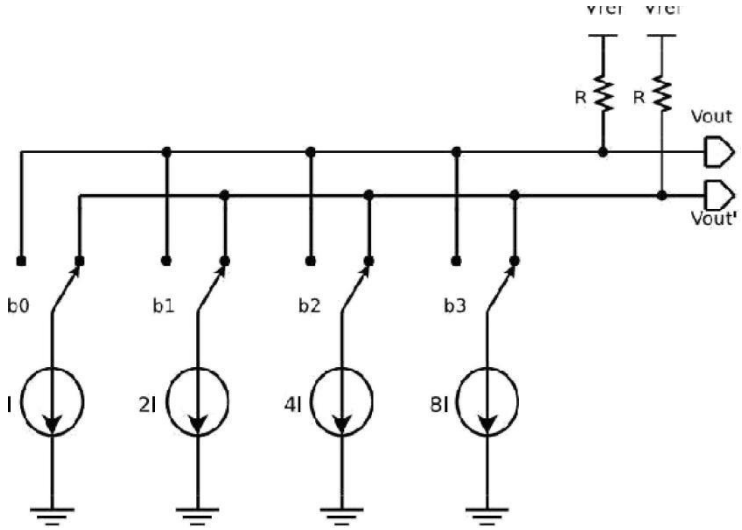

Fig.1.5: 4-Bit binary current steering DAC

Digital to analog transmission devices, or the DACs, are essential components of contemporary electronic systems because they can accurately transform digital input and output data into signals that are analog in nature. The preciseness of digital data reconstruction is largely dependent on the accuracy and granularity of the DAC, which in turn affects the system's overall performance. High-speed data converters[13]-[14] used to frequently use SiGe or GaAs technologies. These technologies did, however, come with several disadvantages, like high cost of manufacture and significant power consumption. High-speed and accurate digital to analog converters (DACs) are widely used in communication systems[15]-[16], instrumentation, and direct digital synthesizers. Due to differences in the fabrication process, the increasing resistor values in alternative DAC architectures, such as the weighed resistor DACs, increasing resolution poses alignment issues. Moreover, the issue of resistor mismatch still exists in R-2R configurations.

Researchers exploring various DAC technologies have focused a lot of attention on steering the digital-to-analog converter [17] because of its inherent advantages, which include great resolution, low noise, rapid settle times, and low power consumption. he DAC's steering architecture. To operate, one only needs to add the currents from the various current sources to the current steering architecture. Categorized, binary- weighted, and unary-weighted are the three types of steering DAC topologies that are now in use [18]-[20]. Since just 'n' switches and current sources are needed in the segmented architecture, binary-weighted current steering can be implemented with ease. However, the disadvantage of binary DAC is that it produces a significant glitch when numerous current sources switch at the same time. Glitch reduction can be accomplished with unary weighted current supply. One issue with the

unary balancing DAC is that its unary design consumes up a lot of storage and needs a lot of current assets to execute.Thus, there is a balance between space, speed, and design complexity in the segmented architecture. In the proposed DAC, the input bits are divided into two groups based on the segmented architecture: MSBs and LSBs. In this segmented architecture, the lower- order bits (4 Bits) are processed using binary balanced DAC and the MSBs (8 Bits) using unary weighted DAC. Thermometer MSBs are implemented using encoded bits in unary DACs, which reduce static error further because only one bit changes value for each code, improving accuracy. The 8-4 segment current steered DAC structure is shown in Fig. 1.6. To get the finest glitch-free performance, input digital bits are divided. Despite having appropriate dynamic characteristics, the designs in [21]-[22] consume more power. Even if the DAC in [23] has a 12-bit resolution, the rate of sampling is much lower.

Analog to Digital Conversion The current Steering system enables quicker conversion times and higher resolution. Usually, the Current-Steered (CS-DAC) is employed to increase the current sources' matching precision. Current steered differential amplifiers are divided into two primary groups: binary and unary weighted, depending on the types of current sources. An N-bit DAC required N current sources in the first scenario. One of its benefits is that it has fewer current sources, although large-bit transitions can result in noticeable errors.N bits must be converted into the analog signal in an unary DAC using 2N -1 sources of current. Every current source in this case has the same value at the moment.

The advantage here is that since there is only a single bit shift, there will not be any hiccups. But a bigger region emerges from a requirement for more recent sources.A 12-bit steered DAC with a segmented design is suggested in the work that follows. Using 45nm technology, it is carefully examined to improve spurious free range of dynamics (SFDR) performance and power efficiency. The amount of binary data transitions determines the number and size of glitches. There are a growing amount of switch state modifications with more transitions. A 12-bit binary weighted DAC exhibits a severe glitch when the input undergoes 12 transitions, changing from 011111111111 to 100000000000.

Because unary-weighted DACs just have a 1-bit transition-that is, no glitches-they require higher current sources. The thermometer code controls the switches. Nevertheless, in order to translate binary code into thermometer codes, additional circuitry is needed. With a 45 nm tech node, we can achieve a lower SFDR of 41.77Db and a power reduction of 44.95 mW in this work, using a rate of sampling of 1.2 GS/s.

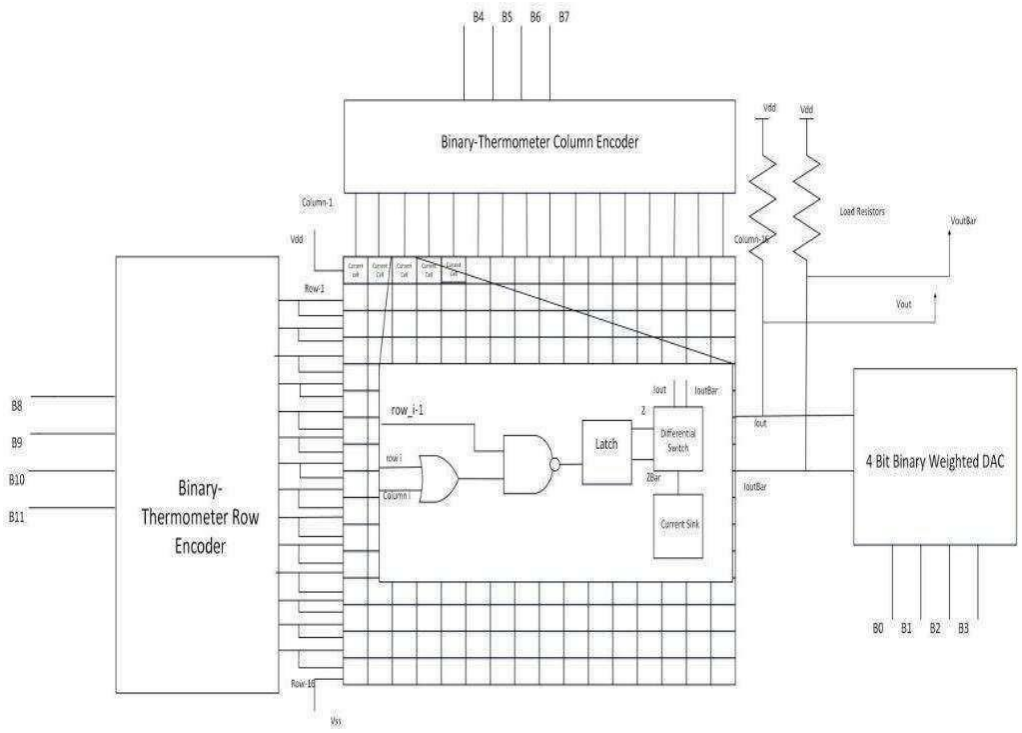

Fig.1.6: 12 Bit 8-4 segmented current steering DAC's Block Diagram

1.3 Research Problem Formulation

Since current directional DACs are so quick and effective, they are employed extensively. The design of a 12-bit current steering digital-to-analog converter has notable obstacles concerning linearity, power consumption, and spurious free dynamic range.The literature's main conclusions include the fact that while designs have improved in both power and speed economy, SFDR is still a problem. DACs with low power consumption and high frequency operation are essential for many applications in contemporary communication systems. Power consumption and linearity are trade-offs as increasing one frequently has a negative impact on the other.

Additionally, it is difficult to eliminate errors resulting from the while still considering a resolution increase of, say, 12 bits. In order to lessen this glitch issue, each current cell uses a unary balanced current-steering DAC, providing only one current. In contrast to binary encoders, which only transition one bit at a time, thermometer encoders only transition one bit at a time, which prevents glitches and allows for the precise delivery of control signals to unary current cells. Nevertheless, the logic gates that are part of the thermometer encoder also add to the complexity and draw additional power. Thus, two sub-DACs in a segmented design are employed. Also to have better linearity the proposed architecture has a unary current source architecture in which there is switching of only one

current source at a time which in tum prevents the output waveforms to become nonlinear. Inside each unary current cell of the current cell array, a local decoder is there that gets the output from the two thermometer encoders. This local decoder is placed in each current cell and generates logic using thermometer-encoded bits. After the logic is decoded, it is delivered to a latch, whose output drives the reduced swing switching logic that controls current flow between the two differential outputs, lout and lout'. In other words, the latch essentially drives the current switches. The switch driver receives the latch's output, which lessens the effect of current cell glitches. The two sub- DAC's output currents are connected.

1.4 Research Objective

This research aims to develop innovative design strategies and optimization techniques to enhance the performance of 12-bit (CS-DACs) to meet the stringent demands of modem applications.

The primary goal is to create a high-performance 12-bit CS-DAC that effectively addresses critical challenges related to power consumption,SFDR, linearity, and resolution. This involves investigating the causes of non-linearity and SFDR limitations in current designs and applying advanced calibration techniques to mitigate these issues. Design optimizations and the utilization of high-speed transistor technologies will be explored to enhance the speed and resolution of the DAC.

The research will integrate these advancements into a comprehensive design methodology. This methodology will be validated through simulation and experimental measurements, leading to the development of a prototype that showcases significant improvements over existing designs. The results will be documented, published, and shared to contribute to the advancement of DAC technology in both academic and industrial fields.

To address the SFDR issue, the proposed design features a segmented architecture with an 8:4 ratio, combining binary-weighted and unary-weighted current-steering architectures. For linearity improvements, the design includes a unary current source architecture, which switches only one current source at a time, preventing nonlinear output waveforms. The objective is to achieve a resolution of 12 bits while maintaining linearity, minimizing power consumption, and achieving a low SFDR.

1.5 Research Methodology

The development methodology for a high-performance 12-bit 1.2 GS/s DAC using 45 nm CMOS technology follows a detailed and structured approach. This process is divided into several key phases: literature review, design, and simulation.Initially, an extensive review of existing current-steering DAC designs was conducted, particularly focusing on those with 12-bit resolution and operating speeds of 1 GS/s or higher. This review aimed to establish a comprehensive understanding of the state-of-the-art, identify existing challenges, and highlight gaps in the current research.

The study then examined the impact of CMOS scaling on DAC performance, specifically analyzing linearity, power consumption, SFDR, and resolution. State-of-the-art techniques were identified to enhance DAC performance, including methods to improve linearity, SFDR, and power efficiency.

To address the identified challenges and achieve the desired specifications, a suitable DAC architecture was chosen, incorporating differential and segmented current-steering techniques to optimize performance. Key sources of non-linearity, such as mismatch errors, were addressed through the development of calibration techniques and the implementation of dynamic element matching and other compensation methods. The transistor sizing and layout were optimized to minimize parasitic capacitances and enhance speed, utilizing high-speed CMOS transistors available in the 45 nm technology to meet the 1.2 GS/s target.

The design and simulation were carried out using the industry-standard CAD tool, Cadence Virtuoso. DC analysis was performed to determine the net power consumption, and signal power in decibels was calculated to evaluate the SFDR. The sampling rate was determined by analyzing the largest frequency component of the digital signal and doubling it to find the required sampling rate.

CHAPTER 2
LITERATURE SURVEY

2.1 Synthesizing Prior Research:

Current-steering digital-to-analog converters (CS-DAC's) are crucial for modern digital communication systems, enabling efficient signal processing in various applications, including wireless communication, digital television, and high-speed data transmission. Recent advancements focus on achieving higher sampling rates, improved resolution, and enhanced linearity while maintaining power efficiency and reducing distortion. This survey examines significant designs and innovations in CS-DAC technology implemented using advanced CMOS processes.

2.1.1 High-Performance CS-DAC Designs

Wang et al. (2019) - In [24], a 3GS/s 12-bit CS-DAC in 55 nm CMOS Technology Wang et al. presented a 3 gigasamples per second (GS/s) 12-bit CS-DAC designed in 55 nm CMOS technology. The design prioritizes high-speed operation and high resolution, employing optimized current cell design and layout techniques to minimize glitches and improve linearity. This makes the DAC suitable for high-frequency signal processing applications .

Wang et al.(2020)- In [25], a 2GS/s 14-bit CS-DAC in 45 nm CMOS Technology Another design by Wang et al. features a 2GS/s 14-bit CS-DAC in 45 nm CMOS technology, targeting a high output third-order intercept point (OIP3) of 25 dBm. The design uses advanced calibration techniques to enhance linearity and dynamic performance, which are critical for applications that require high signal fidelity, such as communication transmitters .

Aboobacker et al. (2013) - In [26], Design and Comparison of 8-bit 100 MHz CS-DACs Aboobacker et al. designed, implemented, and compared 8-bit CS-DACs operating at 100 MHz. This study focuses on optimizing performance parameters such as linearity and power efficiency. The comparative analysis provides insights into different design approaches and their impacts on overall DAC performance, highlighting the importance of careful design choices to meet specific application requirements .

Zhu et al. (2018) -In [27], a 10-bit Dual-Channel CS-DAC in 40 nm Technology Zhu et al. introduced a 10-bit dual-channel CS-DAC in 40 nm CMOS technology. This design targets

integrated circuit (IC) applications requiring multiple channels of high-speed analog output. The dual-channel configuration allows for flexible signal generation and processing capabilities, with particular attention to minimizing crosstalk and inter-channel interference through careful layout and shielding techniques .

Yuan et al. (2007) - In [28], 10-bit 2 GHz CS-DAC Yuan and colleagues designed a 10-bit CS-DAC capable of operating at 2 GHz. This high-speed DAC uses a current-steering architecture to achieve high resolution and rapid sampling rates. The design focuses on optimizing dynamic performance and power efficiency, making it suitable for high-frequency applications where precise and fast signal conversion is necessary .

Palmers and Steyaert et al. (2010) - In [31], a 10-bit 1.6-GS/s CS-DAC in 130 nm CMOS Palmers and Steyaert designed a 10-bit 1.6-GS/s CS-DAC using 130 nm CMOS technology, achieving low power consumption of 27 mW and an SFDR of 54 dB up to a 550 MHz bandwidth. This design emphasizes efficient power usage and high SFDR, making it suitable for high-speed applications .

Chang et al. (2018) - In [32], a 2 GS/s 14-bit CS-DAC in 65 nm CMOS Chang et al. presented a 2 GS/s 14-bit CS-DAC in 65 nm CMOS technology for wireless transmitters. The DAC achieves the high resolution and sampling rates needed for modern wireless communication standards, focusing on optimizing linearity and dynamic performance for high signal fidelity .

Moody et al. (2015) -In [33], a 10-bit 1.2 GS/s CS-DAC in 90 nm CMOS Moody's design of a 10-bit 1.2 GS/s CS-DAC in 90 nm CMOS technology addresses the challenges of balancing high speed and accuracy. The design optimizes current source matching and reduces layout-induced errors, which are critical for maintaining performance at high sampling rates .

Deveugele and Steyaert et al. (2006) - In [34], a 10-bit 250 MS/s Binary-Weighted CS-DAC Deveugele and Steyaert developed a 10-bit 250 MS/s binary-weighted CS-DAC, highlighting the use of a binary-weighted architecture to simplify the design and improve linearity. Despite being implemented in an older technology node, this design showcases techniques for achieving high linearity and low distortion .

Elkafrawy et al. (2013) - In [35],designed a current-steering DAC tailored for integration with a high-speed current mode successive approximation register (SAR) ADC. This design is optimized for rapid conversion times, enhancing the efficiency and speed of the SAR ADC. Utilizing a current-steering architecture, the DAC achieves high-speed performance and precise accuracy, making it well-suited for high-performance ADC applications .

Razavi (2018) - In [36],Overview of Current-Steering DAC Razavi provided a comprehensive overview of the current-steering DAC, discussing its principles, applications, and key performance metrics. This overview serves as a valuable resource for understanding the fundamental concepts and design considerations for CS-DACs .

McDonnell et al. (2017) - In [37], Compensation and Calibration Techniques for CS-DACs McDonnell et al. explored various compensation and calibration techniques to enhance the performance of CS-DACs. These techniques are critical for addressing non-idealities and improving the overall accuracy and linearity of high-speed DACs .

Lin and Kuo (2012) - In [38], Random Rotation-Based Binary-Weighted Selection in CS-DAC Lin and Kuo presented a compact CS-DAC design with improved dynamic performance using random rotation-based binary-weighted selection. This technique enhances linearity and reduces distortion, demonstrating an effective approach to optimizing CS-DAC performance .

Chen and Chang (2012) - In [39], 6-bit CS-DAC with Compound Current Cells Chen and Chang introduced a 6-bit CS-DAC that employs compound current cells designed for both communication and rail-to-rail voltage-source applications. This DAC emphasizes high linearity and low power consumption, making it versatile for a wide range of applications. The compound current cells approach allows the DAC to achieve high performance by improving current matching and minimizing errors, which is crucial for maintaining signal integrity in high-speed communication systems .

Luo et al. (2012) - In [40], 11-bit High-Speed CS-DAC Luo et al. designed an 11-bit high-speed CS-DAC, focusing on achieving high sampling rates and low power consumption. The design addresses key challenges in high-speed digital-to-analog conversion and demonstrates significant improvements in performance metrics .

Kim et al. (2016) -In [41], SUC-Based Full-Binary 6-bit 3.1-GS/s CS-DAC Kim and colleagues designed a 6-bit CS-DAC using a Successive-Approximation (SUC) based full-binary architecture, achieving a sampling rate of 3.1 gigasamples per second (GS/s). The DAC, implemented in a compact 0.038 mm^2 area, operates at 17.7 mW. This design focuses on balancing high-speed performance with power efficiency and compactness, making it suitable for applications with stringent size and power requirements .

2.2 Comparison

Table 2.1 :Literature Survey Comparison

References	Advantages	Limitations
[24] CS-DAC (2019)	Resolution is high (12 bits) Sampling rate is high (3 GS/s)	High Power Consumption (495 mW)
[25] CS-DAC (2020)	Resolution is high (14 bits) Sampling rate is high (2 GS/s)	High Power Consumption (276 mW)
[26] CS-DAC (2013)	Sampling rate is high (20 GS/s)	Low resolution (8 bits)
[27] Dual Channel CS-DAC (2018)	Low power consumption (6mW)	Low resolution (10 bits)
[28] CS-DAC (2007)	High sampling Rate (2 GS/s)	High Power Consumption (790mW)
[31] CS-DAC (2018)	Low SFDR (54dB)	Low sampling rate (1.6 GS/s) Resolution is low(10bits)
[32] CS-DAC (2018)	High Resolution (14 bits)	High Power Consumption (490 mW)
[33] CS-DAC (2015)	Low Power Consumption (43mW)	Low resolution (10 bits)
[34] CS-DAC (2006)	Low Power consumption (4mW)	Low sampling rate (250 MS/s)
[35] CS-DAC (2013)	Good SFDR throughout.	Low resolution (10 bits)
[37] CS-DAC (2017)	High Resolution (14 bits)	Low sampling Rate (130 MS/s)
[38] CS-DAC (2012)	High Resolution (12 bits)	Low Sampling Rate (500MS/s)
[39] CS-DAC (2012)	Low Power Consumption(8.32mW) High Sampling Rate (3GS/s)	Low Resolution (6 bits)
[40] CS-DAC (2012)	High Resolution (11 bits)	Low Sampling Rate (200MS/s)

The surveyed literature demonstrates significant progress in CS-DAC design, particularly in enhancing resolution, linearity, and power efficiency. These improvements are crucial for modern communication systems and high-speed applications requiring precise signal conversion.

Future research should focus on further enhancing power efficiency, integrating advanced on-chip calibration and compensation circuits, and exploring new materials and architectures to advance CS-DAC performance. Continued innovation in CMOS technology and design methodologies will likely drive further improvements in this vital component of digital signal processing systems.

CHAPTER 3
PROPOSED METHODOLOGY

3.1 Proposed Design

This work uses a segmented current steering architecture of 8-4 to implement a 12-bit DAC. It is seen that higher resolution DAC of over 12-bit DAC have limitations in tenns of speed i.e., samples per second. The motivation behind choosing a 12-bit current-steering(CS) architecture is to strike a balance between speed and resolution. In my system, there are two DACs used to segment the bits. It is simple to create a binary-weighted DAC,i.e., only n numbers of current sources as well as switches for n bits are required. However, the primary issue with binary weighted current steering architecture is that when many current cells are switched at once, a sizable glitch may appear at the output.

So, to reduce such problem of glitch a unary weighted CS-DAC is used in every current cell giving only I current. A thermometer encoder is used to deliver accurate control signals to the unary current cells which eliminates the problem of glitches as compared to binary encoders because, in the thermometer encoder, only 1-bit makes a transition at a time as compared to binary encoders. However, the thermometer encoder increases the complexity as well and more power is consumed by the logic gates present in the thermometer encoder. So, a segmented architecture of two sub-DACs is used as shown in Fig. 3.1. To a binary weighted sub- DAC are supplied the principal LSB bits D0, D1, D2, and D3. However, a thermometer-encoded unary weighted sub-DAC is used to transform the MSB bits (D4-D11).

The LSB bits are sent to a dummy decoder followed by a 4-bit binary weighted DAC which has the output current value (l,2I,41,8I) corresponding to the input code. The purpose of the dummy decoder is to match the delay between binary and unary current cells. The most vital bits (MSB) of the current cells are arranged in a matrix style. With eight MSB bits (four for each thermometer encoder), the current cell array has 255 unary cells in total, as may be seen below. As seen in Fig. 3.2, such unary current units are set up in the current unit matrix in a 16x16 layout. Two thermometer encoders are present; one is utilized to address the current cell array's matrix columns, and the other one addresses the array's rows.Inside each unary current cell of the current cell array, a local decoder is there that gets the output

from the two thermometer encoders. This local decoder is placed in each current cell and generates logic using thermometer-encoded bits.

After the logic is decoded, it is delivered to a latch, whose output drives the reduced swing switching logic that controls current flow between the two differential outputs, Tout and Tout'. In other words, the latch essentially drives the current switches. The switch driver receives the latch's output, which lessens the effect of current cell glitches. The two sub-DAC's output currents are connected. Ultimately, the connected output current is converted to voltage by the load resistors. This occurs because one end of the two load resistors is linked to the power supply Vdd, and the other end is connected to the current cells. As a result, by the voltage division, we get the output voltage. The output of both unary and binary DAC is summed, and analog voltage is obtained across the load resistors using Equation 1.

$$Vout = Vdd - lout\,R \tag{1}$$

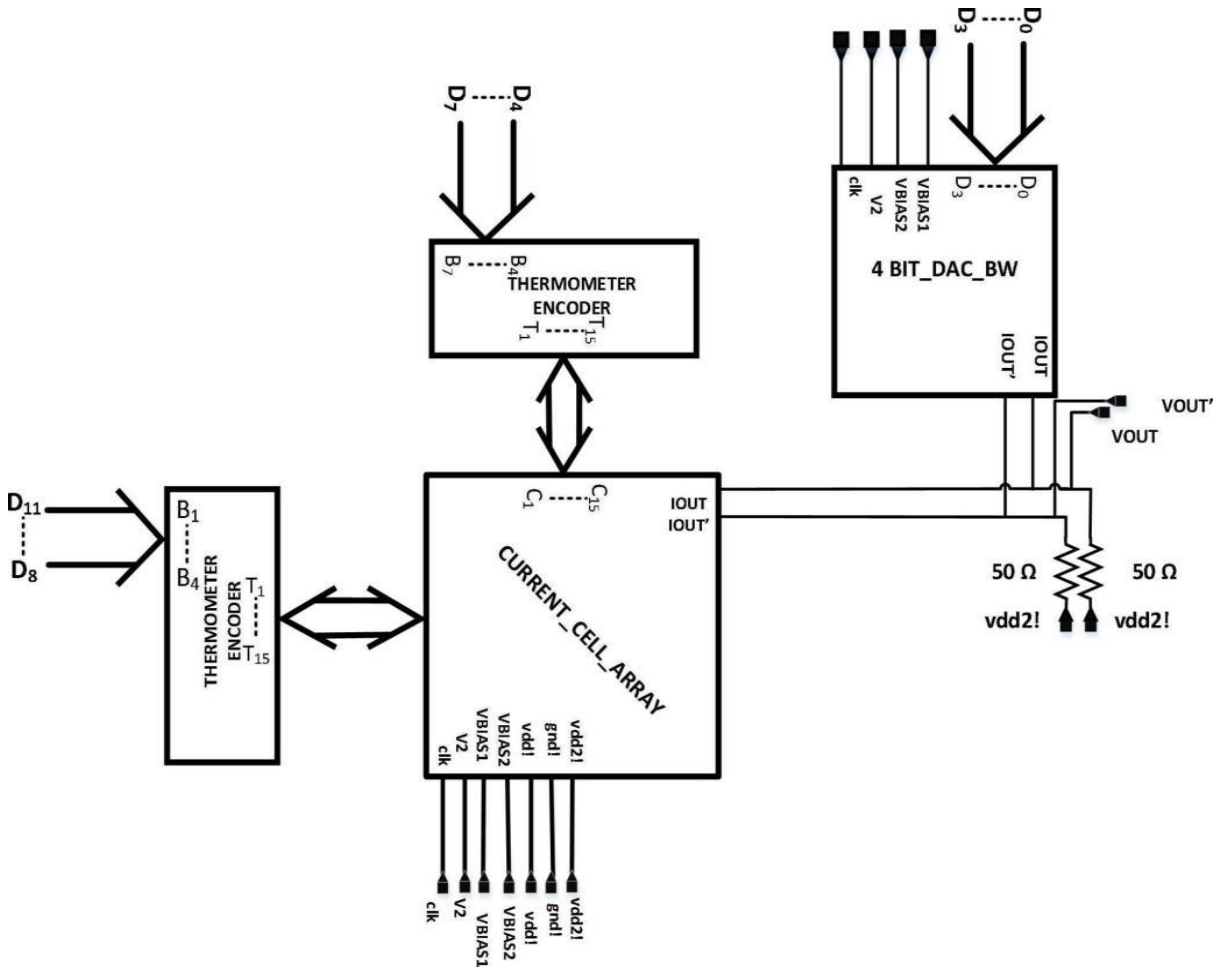

Fig.3.1: Proposed DAC's Schematic

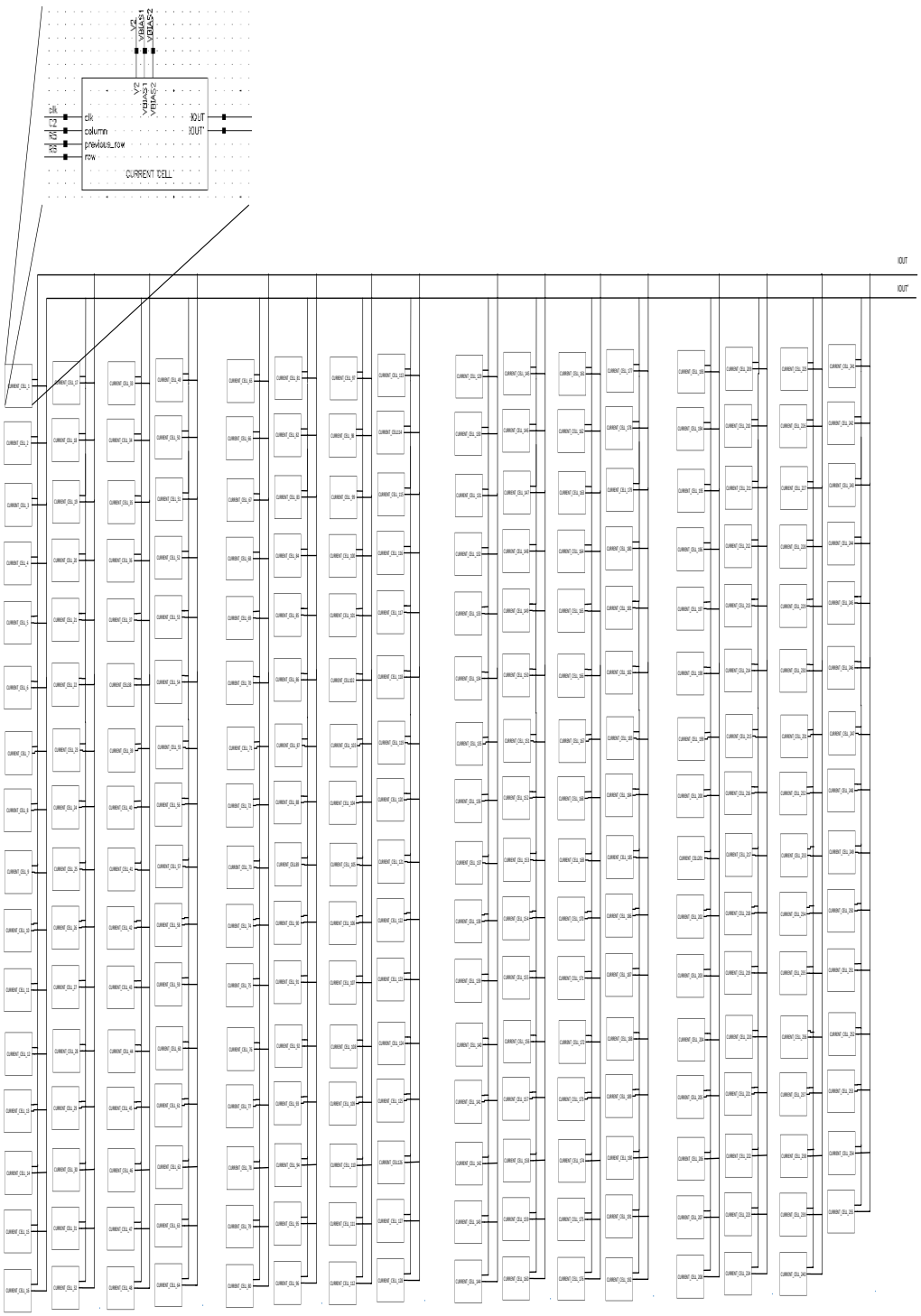

Fig.3.2: Unary current cell Array Schematic

Fig. 3.3 depicts the schematic for a 4-bit weighted binary DAC; the currents generated by each current cell (I, 21, 41, and 81) are 0.34 A, 0.68 A, 1.36 A, 2.72 A, and 161 for unary current cells of 5.44 A, respectively. The load resistance is assumed to

be 50 ohms, and the output full-scale voltage and current are 70 mV and 1.4 mA, respectively.

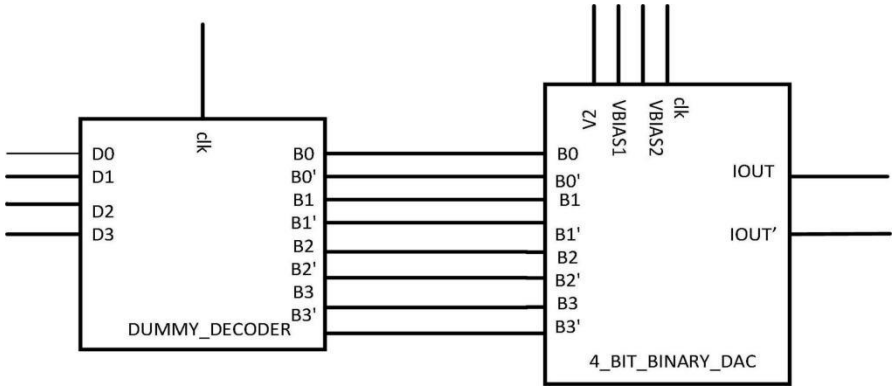

Fig.3.3: Binary weighted 4-bit DAC schematic

3.2 Thermometer Encoder

The idea behind thermometer encoding is that only a one-bit value will change corresponding to each input code [29]-[30]. This type of encoding reduces glitches and makes the digital circuit more accurate at the cost of the increasing area. A 1-D or 2-D implementation of the thermometer encoder is possible. A single encoder is used in the one-dimensional design to address each current cell and transform the binary bits.

TABLE 3.1-Boolean expression for 4-bit thermometer encoder

ENCODER OUTPUT	KMAP REDUCTION POS
Tl	(A+B+C+D)
T2	(A+B+C)
T3	(A+B+C)(A+B+D)
T4	(A+B)
T5	(A+B)(A+C+D)
T6	(A+B)(A+C)
T7	(A+B)(A+C)(A+D)
T8	(A)
T9	(A)(B+C+D)
Tl0	A(B+C)
Tll	A(B+C)(B+D)
Tl2	(A)(B)
T13	(A)(B)(C+D)
Tl4	(A)(B)(C)
Tl5	(A)(B)(C)(D)

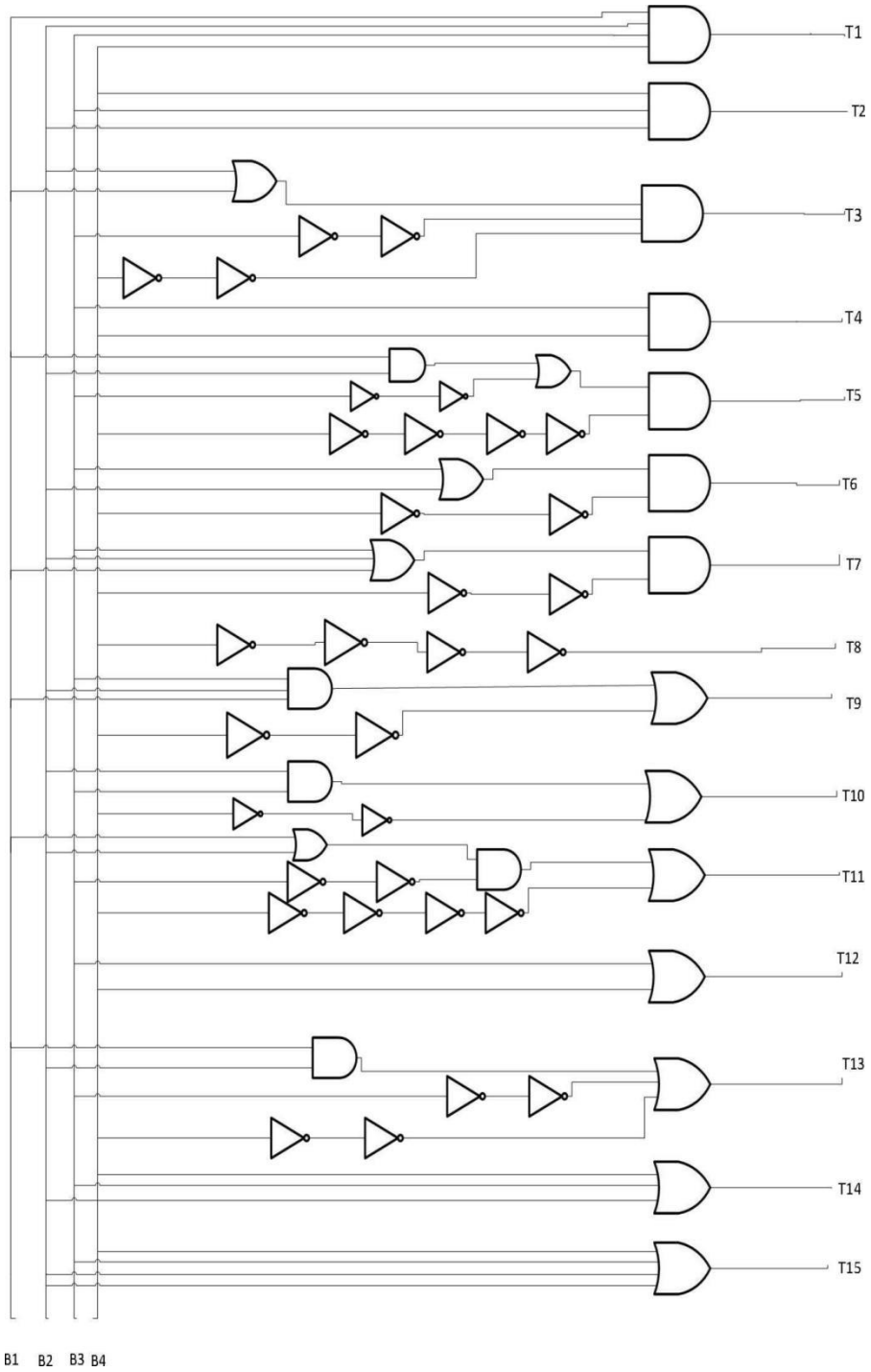

Fig.3.4: Gate level schematic of 4:15 thermometer encoder

The two-dimensional encoder enables the matrix placement of the current cells. To manage columns and rows in the current cell combinations, two encoders are required. This method is recommended because it can reduce the complexity of the thermometer encoder by using a 2-D design. An M-bit encoder will produce 2M - 1 output bits. With the aid of K-Map, the logic expression for these bits can be discovered.

The equations for output bits Tl-Tl5 utilizing the input bits A (MSB), B, C, and D (LSB) are shown in Table 3.1 obtained from K-Map. Fig. 3.4 displays the temperature encoder's gate level schematic.

3.3 Current Cell Decoder

The thermometer encoder sends its encoded output to the nearby decoder, which makes use of the current-cells. Each cell is uniquely recognized by both its col-(j) and row-(i) numbers. The inputs of the adjacent decoder consist of row-(i), col-(j), row-(i- 1) in addition for an OR gate and a gate with NAND. The activation state of the present cell is ascertained using these inputs. To manage the differential current switches, differential outputs are generated using an inverter. These outputs are subsequently routed to a master-slave latch, ensuring the synchronization of all input signals from the neighboring decoder. The neighboring decoder's schematic is depicted in Fig. 3.5.

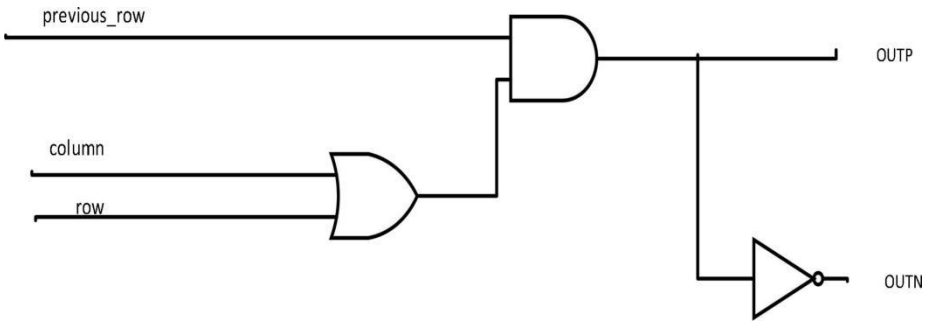

Fig.3.5: Schematic of current cell decoder

3.4 Latch

To synchronize the input with clock frequency, the latch is installed between the switching driver circuit and the current cell decoder. The schematic for the realized master-slave latch based on the proposed architecture is illustrated in Fig. 3.6. The use of MS Latch is intended to loosen the timing restrictions placed on the thermometer encoder since, in MS, the inputs to the latch must be received before the change in clock edge. The corrosponding output waveforms for the latch is shown in Fig. 3.7.

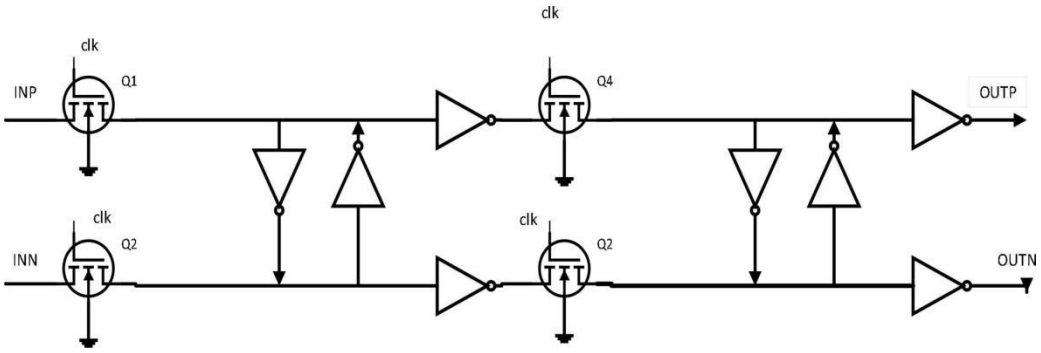

Fig.3.6: Schematic of Latch

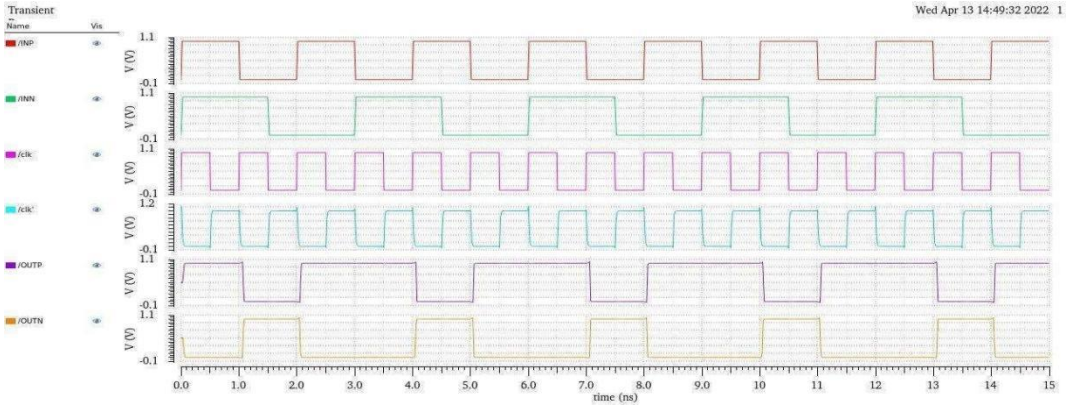

Fig.3.7: Output of latch at 1GHz clock frequency

3 5. Switch Driver

The switching driver circuit is used to adjust the control signal's crossover points in order to fix problems in the current cell. This can be accomplished by modifying the signals' rising time or voltage swing [27]. In this investigation, we choose a method that entails raising the control signal's logic low voltage. Fig. 3.8 displays the switch driver circuit's schematic diagram. The switch driver incorporates two n-MOSFETs which are managed by the latch's digital output.

Switch driver's output always stays at Vdd, even when the inputs are at a low level of logic (0), which puts the transistor in an inactive state. On the other hand, the transistor activates when the input voltage has been set to a high level of logic (1), allowing current to flow via the resistor and resulting in a decrease in the current is sourced. As a result, the voltage at the output decreases as a result of these events.

3.6. Current Source

The current source needs to be designed such that it has high output impedance and low parasitic capacitance. High impedance ensures a lower variation of current in the saturation region of the MOSFET. This can be obtained using a cascade current source as shown in Fig. 3.9. In cascade design, there is a limitation of voltage headroom which is tweaked by using thick gate oxide transistors[28].

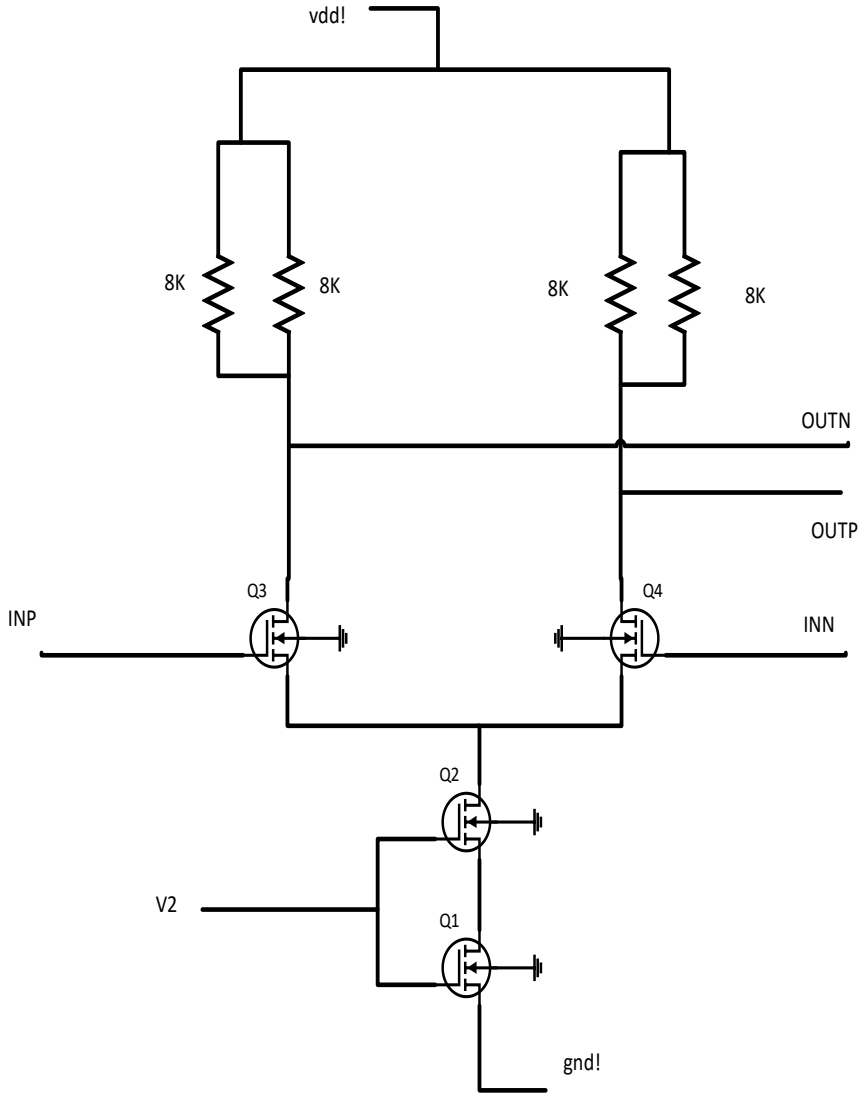

Fig.3.8: Schematic of Switch Driver Circuit

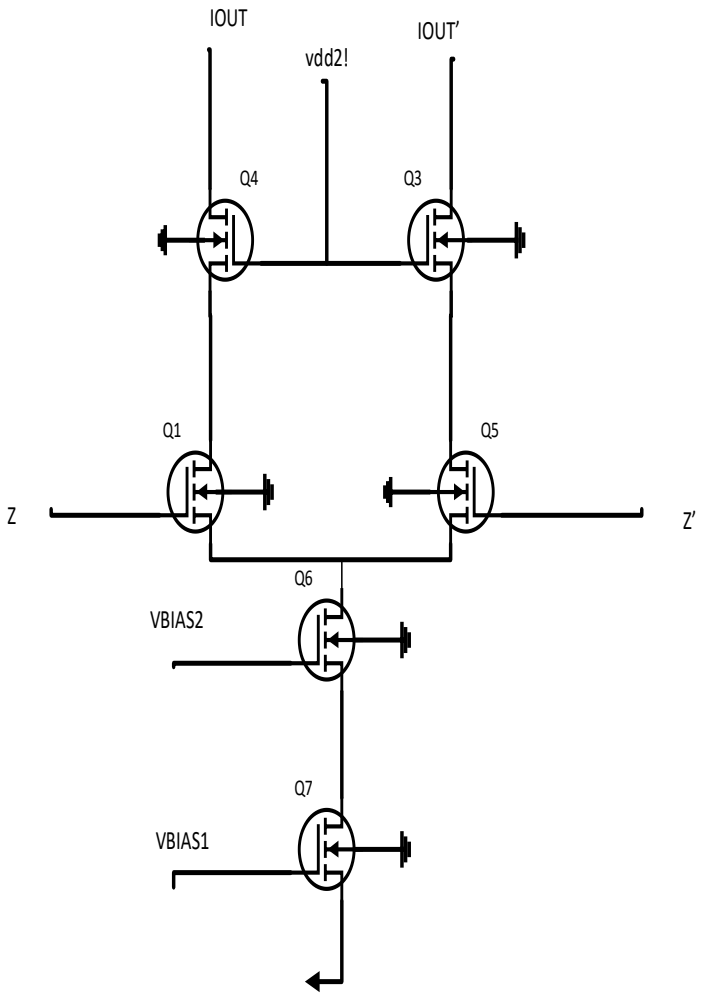

Fig.3.9: Schematic of Unary Current Source

The complete block diagram of a current cell which is replicated to form the 16 x 16 current cell array is shown in Fig. 3.10.

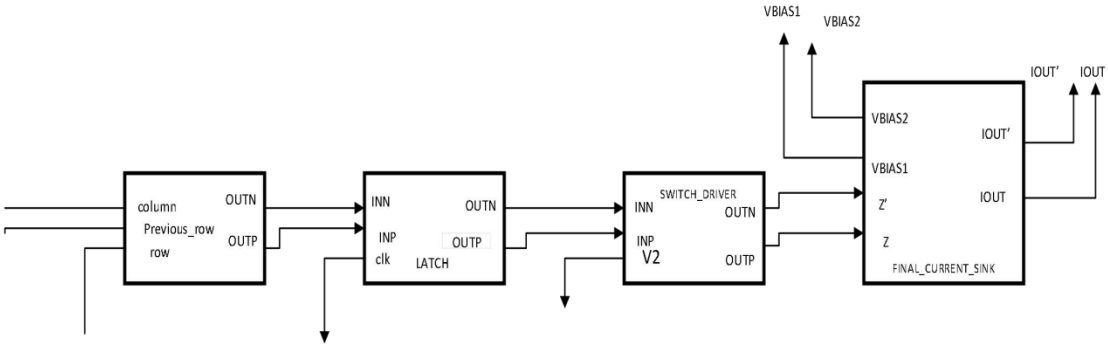

Fig.3.10: Block diagram of an individual current cell

3 .7 Binary Weighted DAC

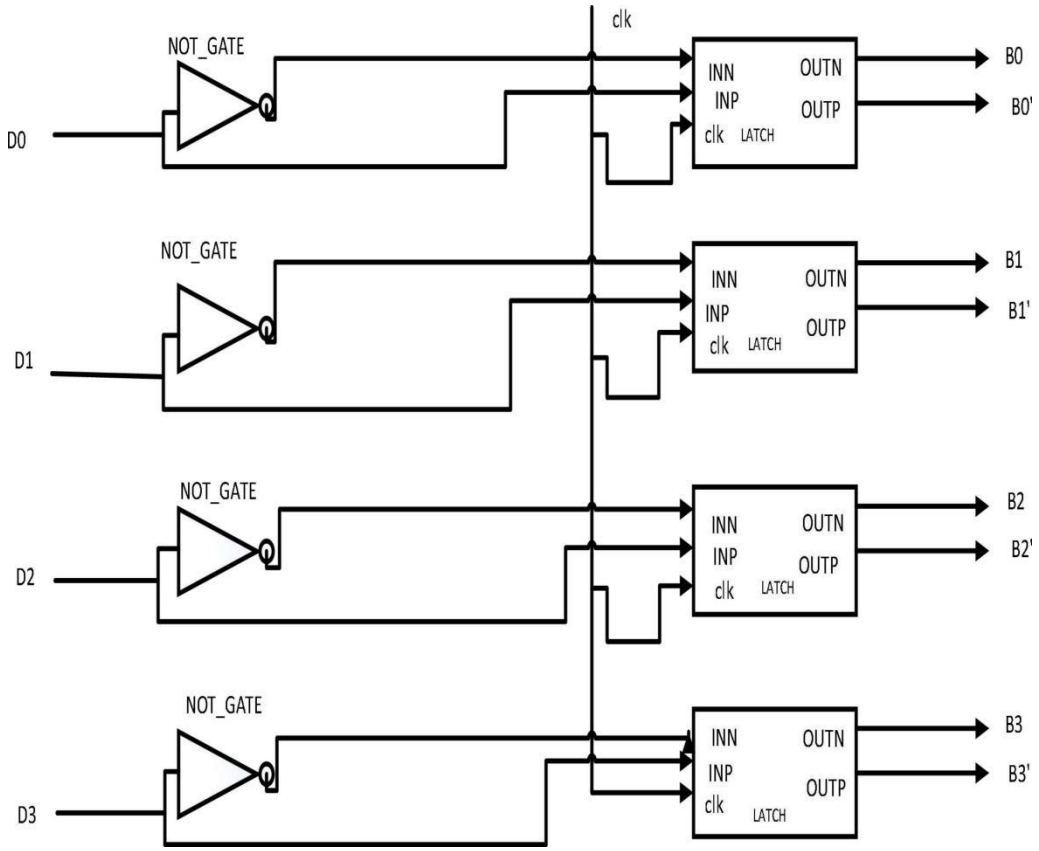

Fig.3.11: Schematic of dummy decoder used in binary DAC

The proposed structure uses a 4-bit weighted binary DAC too, the DAC is made with four current cell units as described, and each cell unit is weighted in a binary fashion where I,21,41, and 81 as output currents. The input signal's Least Significant Bit is first fed into a dummy decoder as shown in Fig. 3.11. This helps in maintaining the same delay across both the segmented units.

Figure 3.12 illustrates the inner block of the binary DAC. It shows that current is directed through the current source to obtain value at lout whenever an input bit is logic high.

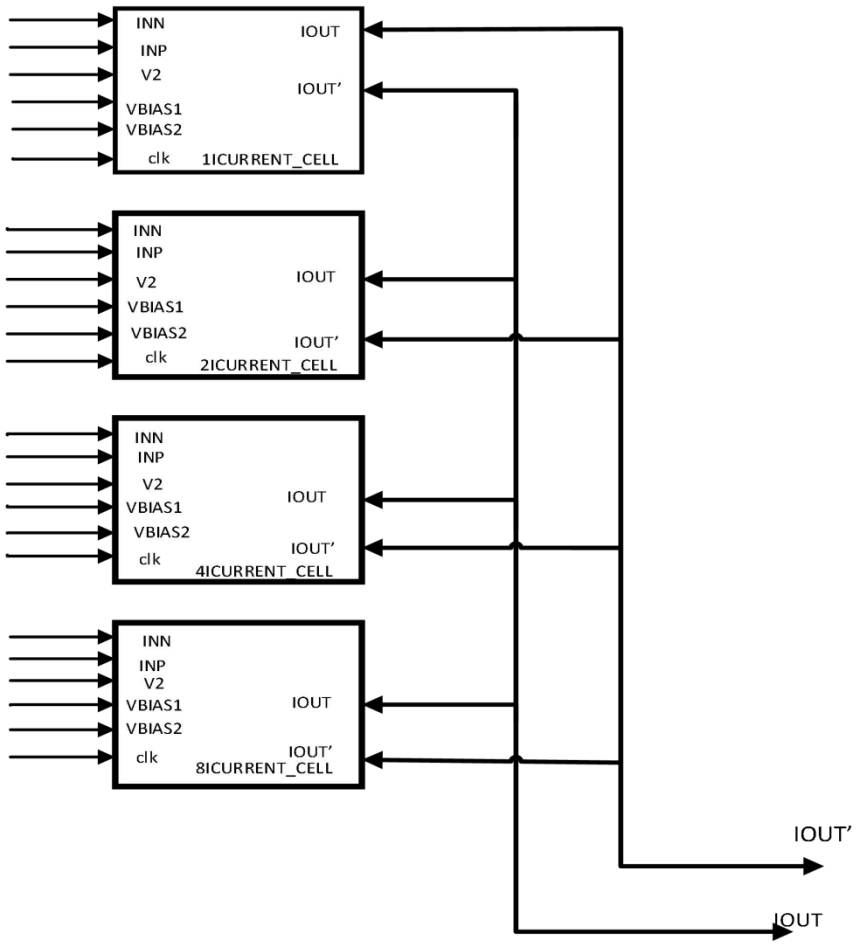

Fig.3.12: Binary weighted current steering 4-bit DAC's Block Diagram

CHAPTER 4
RESULTS

4.1 Simulated Results

Here, 45nm CMOS technology was used for the simulation, and Fig.4.2 shows the DAC's output. The mean power dissipation of various digital sub-circuits must be assessed in order to calculate the electrical power usage of the DAC. The average power consumption of the temperature encoder is 11.2458uW, the regional decoder is 0.06nW, the latch is 6.4uW, and the switch's driver is 47.6uW. Depending on the block's complexity, various blocks have variable power usage. Because of this, the local decoder uses a lot less energy than other blocks. These circuits are now widely employed in architecture; Table 4.1 lists the overall power consumption of all digital circuits.

The switch driver has the most power consumption of all the digital circuits since there is a driver for every current cell. The total power consumption of the DAC is estimated as 44.95 mW. A SFDR dynamic performance test, which yields a value of 41.77 dB, is likewise displayed in Fig.4.3.

The cell's delay may be calculated using the following equation: (tphl + tplh)/2, where tphl represents the propagation delay during high-to-low output switching and tplh represents the propagation delay during low-to-high output switching for various digital inputs and analog output. The maximum delay is 248 ns and corresponds to the D4 bit, indicating the highest possible delay for the combined 8-bit unary weighted and 4-bit binary weighted DAC.

Fig.4.1 displays the waveform of the digital input. Each of the digital inputs, which range from D0 to Dl , has an ON signal of 1V and an OFF signal of 0V. The rise and fall times for each of these inputs are one second, correspondingly.As can be seen in Fig.4.1 the time periods for D0, Dl, D2, and D3 are 2ns, 4ns, 16ns, 32ns, 64ns, 128ns, 256ns, 5l2ns,1024ns, 2048ns, and 4096ns, respectively. In terms of time, the output shown in Fig.4 is attained different combinations of digital inputs using pulsating signals with different time periods. Here output voltage was measured at the terminal which produces a negative voltage level and therefore the output voltage here ranges between two negative voltage levels i.e. between 650mV and 480mV. The output voltage is a proper analog signal with respect to digital input.

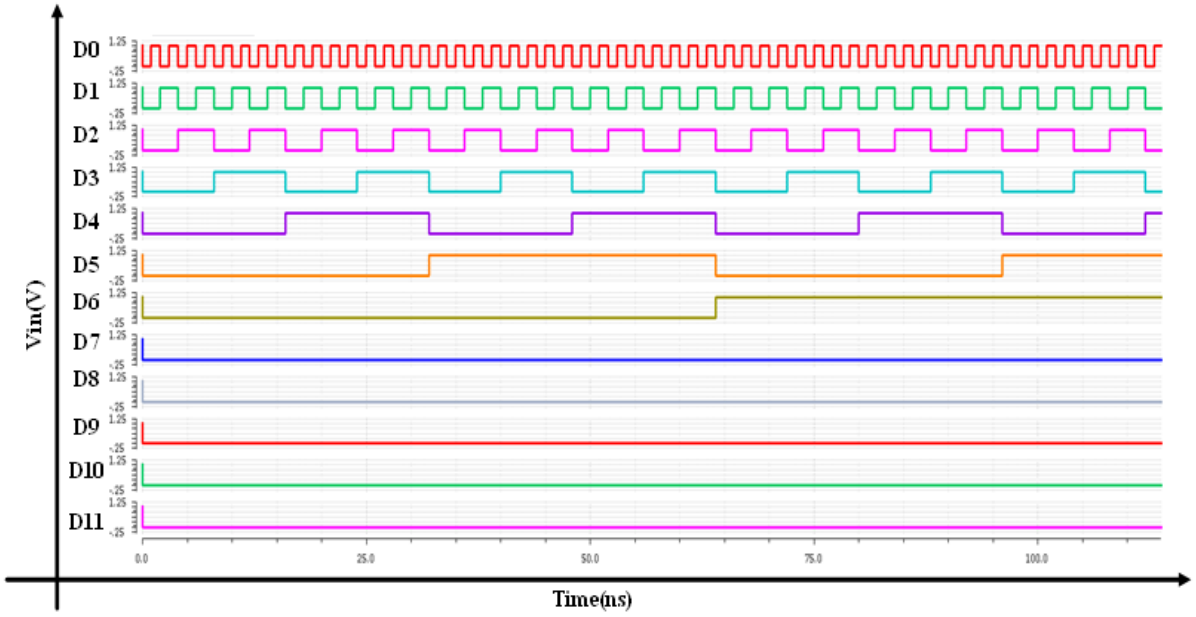

Fig.4.1: Input of 8-4 Segmented 12-Bit DAC

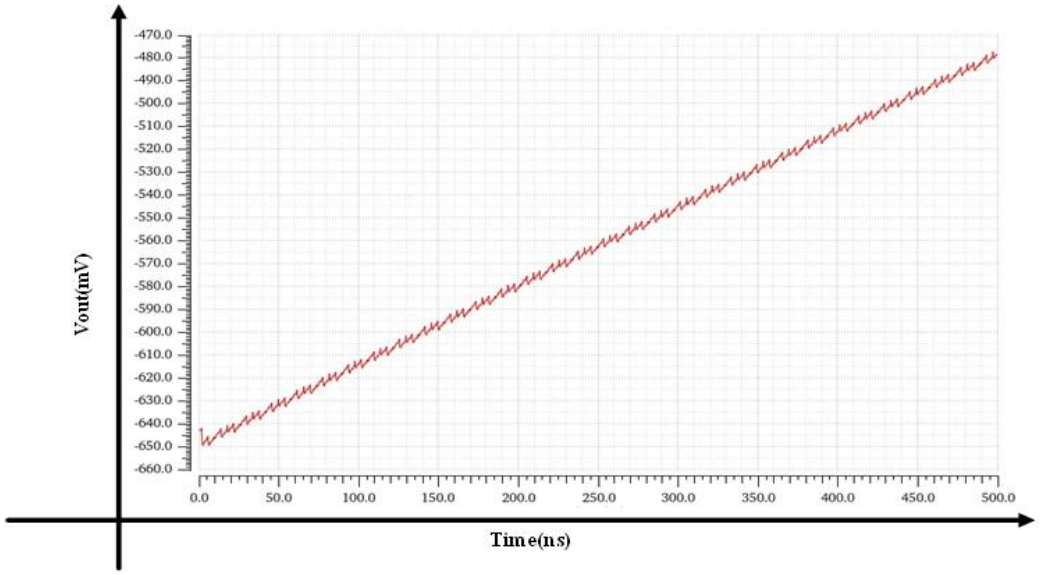

Fig.4.2: Output of 8-4 Segmented 12-Bit DAC

TABLE 4.1 DAC Average Power

Circuit	Quantity	Average Power
Thermometer Encoder	2	22.4916uW
Latch	259	1.6mW
Local Decoder	259	0.0156uW
Switch Driver	259	12.33mW
Current Cell	-	31mW

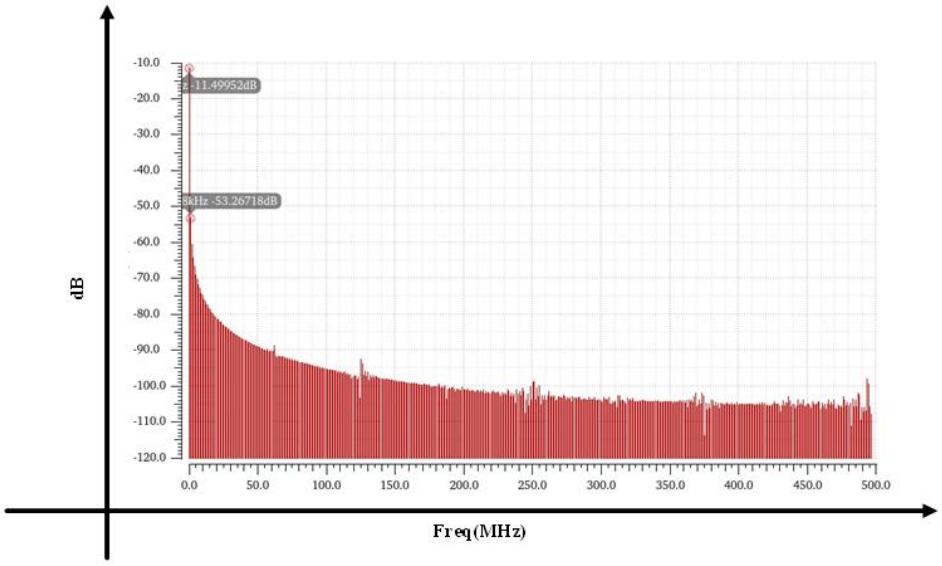

Fig.4.3: Spurious Free Dynamic Range Simulation

4.2 Comparison

In this section, a comparison of different approaches to make an efficient DAC is made. Table 4.2 presents performance comparison of high-speed DAC architecture. In [14] a 12- bit current steering architecture with a partial randomization dynamic element matching (PRDEM) method was used to reduce the harmonic distortion which uses a 55nm technology node with a sampling rate of 3 GS/s and with a power consumption of 495 mW. In [15] with 45 nm technology node sampling rate is 2GS/s with power consumption of 276 mW but increased resolution of 14 bits.

Then in [16] a 12-bit resolution on 40nm technology node with 40 mW and 70dBc SFDR. In [17], a 10-bit current steering DAC is presented with only a 10-bit resolution. However, the power consumption is reduced to 6mW but with SFDR 71.35dBc. In [18] with a technology node of 90 nm, a 12-bit DAC is designed to obtain SFDR of 60 to 65 dB. In [19] a 110 dB SNR and 1.4mW current-steering audio (CSA) DAC were implemented in 45nm CMOS. However, in this work, an 8-4 segmented current steering 12-bit DAC has been presented to obtain a sample rate of 1.2GS/s along with SFDR of 41.77dB and power dissipation of 44.95 mW.The parameters and specifications for a segmented DAC design are typically chosen based on the specific requirements. Here's how they are typically determined:

1. Application Requirements:

   The first step is to clearly understand the application for which the DAC will be used. This includes factors like required resolution, speed, linearity, and power consumption.

2. Resolution:

   The required resolution is a key parameter. It determines the number of bits in the DAC, and thus, the number of segments in a segmented DAC.

3. Speed:

   The desired update rate or sampling frequency plays a crucial role in determining the architecture and specifications. Faster applications may require high-speed DACs.

4. Linearity:

   Linearity and distortion specifications are important, especially in precision applications. This can influence the choice of segment architecture.

5. Power Consumption:

   Power constraints are essential, particularly in portable devices. Lower power consumption may drive the choice of DAC topology and segmentation.

6. Technology and Process Constraints:

   The technology used for fabrication and process limitations can influence the design para--meters.

TABLE 4.2 Performance comparison of high-speed DAC architecture

	[18] CS-DAC (2019)	**[19]** CS-DAC (2020)	**[20]** DEMDRZ Technique (2014)	**[21]** Dual-Channel CS-DAC (2018)	**[22]** CS-DAC (2006)	**[23]** CS-DAC With GDI technique (2014)	**This Work** Segmented CS-DAC (2023)
Technology (nm)	55	45	40	40	90	45	45
Supply Voltage	-	2.5V and l.2V	1.2V	1.1V	1.2V	1V and 3.3V	1.2V
Sample Rate	3GS/s	2GS/ s	l.6GS/ s	32MS/s	-		1.2GS/s
Resolution	12	14	12	10	12	10	12
SFDR	74.64 dBc (at low freq) 50 dBc (1.5 GHz)	-	70dBc	71.35dB	60 to 65 dB	42dB	41.77dB
Power Dissipation(mW)	495	276	40	6	-	1.4	44.95

CHAPTER 5
CONCLUSION AND FUTURE SCOPE

5.1 Conclusion

An 8-4 segment current steered 12-bit DAC is being presented in 45nm CMOS technology.The design procedure of the converter, which guarantees its accuracy and speed, was demonstrated. There was discussion on the thermostat encoder, current cells, switch the driver and current sink, local decoder, and other subcircuits. The DAC can operate at 1.2 GS/s sample rate in 45nm CMOS technology, resulting in an overall power dissipation of around 44.95 mW. The DAC's digital input is pulsating, with an ON voltage of 1V and an OFF voltage of 0V, while the source input voltage is maintained constant at 1.2 V. The DAC also attains a SFDR of 41.77 dB.

5.2 Future Scope

In order to increase the sampling rate of this architecture, interleaved techniques could be incorporated. This architecture could also be further enhanced for lower power by using a low-power technique such as clock gating.

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APPENDIX A (LIST OF PUBLICATIONS)

DETAIL OF PUBLICATION:

Below is the list of published research article in SCOPUS indexed Journal proceedings along with the proofs of publications.

1) Gupta, Tarun & Bhandari, Sonalika & Taran, Sachin & Gupta, Rahul. (2024). A 12-bit 1.2GS/s Current-Steering DAC in 45nm CMOS Technology. Journal of Circuits, Systems and Computers. 10.1142/S0218126624502566 **(SCI-E).**

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A 12-Bit 1.2-GS/s Current-Steering DAC in 45-NM CMOS Technology*

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This research paper presents a 12-bit 8–4-segmented current-steering DAC (digital-to-analog converter) that offers notable advantages, particularly in terms of its reduced power consumption compared to other similar designs. The exceptional performance of our DAC can be attributed to two key factors: the use of a thermometer encoder and an efficient digital input bit segmentation. These features contribute to enhanced precision and reduced power requirements, setting our DAC apart from the existing solutions in the field. These enhancements significantly reduce glitches and improve the accuracy of the DAC's output. DAC dissipates a total power of about 44.95 mW when running at a sample rate of 1.2 GHz with the CMOS technology of 45 nm. While the supply input voltage is held constant at 1.2 V, the DAC's digital input is pulsating in nature in which the ON voltage is 1 V and OFF voltage is 0 V. Also, the DAC has a spurious-free dynamic range (SFDR) of 41.77 dB.

Keywords: Current-steering DAC; low power consumption; spurious-free dynamic range (SFDR).

1. Introduction

Digital-to-analog converters (DACs) are essential in modern electronic systems because they accurately convert digital data into analog signals. The accuracy of the original digital data reproduction depends on the precision and resolution of the DAC, which affects the system's overall performance. In the past, SiGe or GaAs technologies were used with high-speed data converters.[1,2] The disadvantages

*This paper was recommended by Regional Editor Giuseppe Ferri.
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APPENDIX B (PLAGRISM REPORT)

Similarity Report

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