ROUTER 1x3 RTL DESIGN PACKET BASED PROTOCOL USING VERILOG HDL

A Dissertation Report

Submitted In Partial Fulfillment Of The

Requirements For The Award Of The Degree

Of

MASTER OF TECHNOLOGY

in

VLSI DESIGN & EMBEDDED SYSTEMS

Submitted By

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CANDIDATE'S DECLARATION

I, **Shubham Aggarwal (2K22/VLS/17)**, a student of MTech (**VLSI Design and Embedded Systems**), hereby declare that, in partial fulfilment of the requirements for the award of a Master of Technology degree, we have submitted a Project report on **ROUTER 1x3 RTL DESIGN PACKET BASED PROTOCOL USING VERILOG HDL** To the Department of Electronics and Communication Engineering at Delhi Technological University. This material is original and not something that was copied from any source without appropriate citation. There has never been a degree, certificate, associateship, fellowship, or other title or honor that is comparable to this one awarded for the work done here.

PLACE: Delhi Shubham Aggarwal
DATE:31/05/2024

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CERTIFICATE

I hereby attest that the project report on the topic **Router 1x3 RTL Design Packet Based Protocol Using Verilog HDL**, submitted by **SHUBHAM AGGARWAL (2K22/VLS/17)** of the Electronics and Communication Department at Delhi Technological University, Delhi, partially fulfills the requirements needed to be awarded a Master of Technology degree. The report is a record of the project work that the student completed under my supervision. To the best of my knowledge, neither this university nor any other has accepted this work in whole or in part for a degree or diploma.

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M.TECH: VLSI Design & Embedded System

(2022-24)

ABSTRACT

Routers forward data packets between computer networks. It is a routing device at OSI Layer 3. It uses the address field in the packet header to direct an incoming packet to an output channel. Routing allows communications to travel from one computer to another and ultimately reach the target device by shifting data packets traveling from one place to another Routers are networking devices that route data packets across computer networks. Unlike a network switch, which joins data lines from server l networks, it is connected to two or more data lines from separate networks. This focuses mostly on the study of the router device, its top level architecture, and the synthesizing, simulating, and connecting of its many sub-modules, such as Register, FIFO, FSM, and Synchronizer, to its top module. Sending and receiving packets through routing The IP address of the destination network packet determines how the packet is routed and passed either one of the results ports to the input port. An error detection method called parity checking verifies the integrity of digital data transferred between server and client device networks. By using this method, data transmitted from the server network device to the client network device is guaranteed to arrive undamaged. It is an active low synchronous IP that, upon performing specific tasks, causes the router to reset. Under test conditions, the router FIFOs are empty, and the low valid output signals imply that no valid packets have been found on the output data bus.

Existing methodology

High Power 1x3 router In order to route data in a network that is using a lot of power due to the use of switches and bridges between various devices, switches and routers are the only essential components of a successful network and architecture. Clocking gates are not used in this high power 1x3 router since it increases dynamic power dissipation.

Proposed methodology

A router is a basic hardware device that uses a network to transport data packets from one place to another. It is situated at gateways, which are the locations where two or more networks converge, and is connected to a minimum of two networks, usually two LANs or WANs, or a LAN and the network of its ISP. It is an OSI routing device at layer 3.

Based on the length of the incoming packet and the IP address elements in the packet header, it sends the packet to an output network.

Routing is the process of moving a data packet from a source to a destination, enabling messages to move between computers until they arrive at their intended destination. A router is a networking device for computers that makes it easier for data packets to move between networks. Unlike a network switch, which links data lines from several networks together, it has two or more data lines from different networks connected to it. This research examines both the synthesis and top-level layout of the network device, simulation, and coupling of the Synchronizer and sub-modules such as FIFO, FSM, and Register are sent to the top module. Three output ports are available for sending the packet. The package is divided into three sections. The three components are the header, the data, and the frame check sequence. The length of the packet to be transmitted may vary from 1 to 63 bytes, with an 8-bit packet width. Packets are directed to the correct ports via the switch based on their intended addresses. Each output has an own eight-bit port address. If the intended recipient address and port address of the packet match, the switch transmits it to the output port. It has an 8-bit data length. In this proposed research, synthesis and simulation are performed using the Xilinx ISE IDE Tool. Because there are fewer states in the FSM in the suggested architecture, it takes less time to produce a response, which clearly improves frequency.

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CHAPTER-1

INTRODUCTION

Routers, often known as networking devices, forward data packages between each other computer computer networks. A router establishes connections to several Rather of a network converter connecting to a single network, data cables connect from multiple networks[1]. When incoming data packets arrive on the router examines the address data on one of the lines to ascertain their final destination. Following that, It uses data from its routing database or routing policy to route the message to the following network on its path. A network with an overlay is created as a result. Routers on the Internet conduct "traffic directing" functions. Typically, a packet of information is routed from a single router to a different one through the different networks that make up onto the web before to its final destination [3]. A network device is a sort of networking equipment that can send and receive sent via data packets across computer networks. An example of a network switching device is a router, which connects two or more data lines between one network to another. The router checks the address information before delivering data packets from one of the lines and determines their eventual destination. If it uses its routing policy or routing database, it will send the packet to the next network along its path. These packet types construct an overlay internet work[6]. On the Internet, routers perform a variety of functions, including "traffic redirection." Studying computer networking is crucial. It is necessary for a wide range of applications and industries. Computer networking is essential for sectors including finance, healthcare, and education as it allows for communication, data transfer, and remote access. With the use of the hardware description language Verilog RTL, designers may specify how digital circuits behave and confirm that they work properly before putting them into physical implementation. The objective is to create an affordable, dependable, and effective router that can manage large amounts of network traffic—a crucial feature for numerous sectors and uses. My project may contribute to enhancing the dependability and effectiveness of network communication, which is crucial for numerous sectors and uses. It may also have an impact on upcoming advancements in digital circuit design and computer-networking.

Objective

The project's goal was to create a Verilog RTL router that could route data packets to three distinct client networks from a single source network. to create a Verilog RTL router that can be used to route data packets between three distinct client networks and one source network[3]. to create a register module that has the capacity to temporarily store data packets before transferring them to three distinct FIFO memory. to put in place a Finite State Machine (FSM) that is capable of controlling internal signals in order to carry out the activities required for data packet routing. to create a synchronizer that can guarantee the router's signals are timed and synchronized correctly. to use Xilinx ISE and ISIM to simulate the Verilog RTL router in order to verify its performance and functioning. to use ISim to analyze the design's code coverage. must test the router in a UVM-based environment in order to confirm its operation.

Theoretical Background

A router is an equipment which transmits information packets. between networks and is usually found at gateways where two or more networks link. It links two networks, usually two local area networks (LANs), wide area networks (WANs), or perhaps one LAN and the network of an Internet service provider (ISP). Routers, which are part of the Open Systems Interconnection (OSI) architecture and operate at layer 3, establish connections between nodes using protocols, and determine the best way to route packets by analyzing headers and forwarding tables. The first MOS integrated circuit was created by General Microelectronics in 1963., which signified a tremendous achievement. paving the way for Very Large Scale Integration (VLSI) in the years that followed. This technique advanced from 10,000 MOS transistors per chip to hundreds of thousands, then millions. Initially, semiconductor chips had two transistors apiece, but as the number of transistors increased, additional systems and functions could be integrated. Early integrated circuits might have one or more logic gates made up of 10 diodes, transistors, resistors, and capacitors.

Literature Survey

Typically, simulation is used for performance evaluations at the transaction level (TL) or register transfer level (RTL). RTL offers more accurate findings in a shorter amount of time than other simulation methods, which is crucial for NoC design. However, using RTL simulation to characterize a large NoC's performance takes a lot of effort and several hours of computing. Performing a NoC's performance evaluation directly on hardware, such as FPGA, rather than through simulation models, might help expedite the process [5]. By using VLSI architectural principles to router design for networking systems, we aim to develop a networking solution in this study that offers intelligent control over the network. We try to address the constrained input/output configurations of modern networking routers by implementing bridging loops to lower latency and address security issues. We also investigate other methods, such as using several protocols. We try to use a protocol switching mechanism that is built into the router engine itself to address the security and latency issues. SIn which signified a tremendous achievement. paving the way for Very Large Scale Integration (VLSI) in the years that followed. This technique advanced from 10,000 MOS transistors per chip to hundreds of thousands, then millions. Initially, semiconductor chips had two transistors apiece, but as the number of transistors increased, additional systems and functions could be integrated [4]. Early integrated circuits might have one or more logic gates made up of 10 diodes, transistors, resistors, and capacitors. The hardware IP router implementation is our primary concern. With this method, the router may handle several incoming IP packets—for example, IPv4 and IPv6—with various protocol versions at the same time. The method will result in quicker routing and packet switching for both existing trending protocols, which we believe will considerably benefit networking systems.

Existing methodology

High power 1x3 router In order to route data in a network that is using a lot of power due to the use of switches and bridges between various devices, Routers and switches constitute the only required components for a good network and design. Clocking gates are not used in this high power 1x3 router since it increases dynamic power dissipation.

Proposed methodology

A router is a basic hardware equipment so it uses a network to transport information packets from one place to another. It is situated at opening, which are the locations where converge, and often It is device at layer 3. Based on the length of the incoming packet and the IP address elements in the packet header, it sends the packet to an output network.

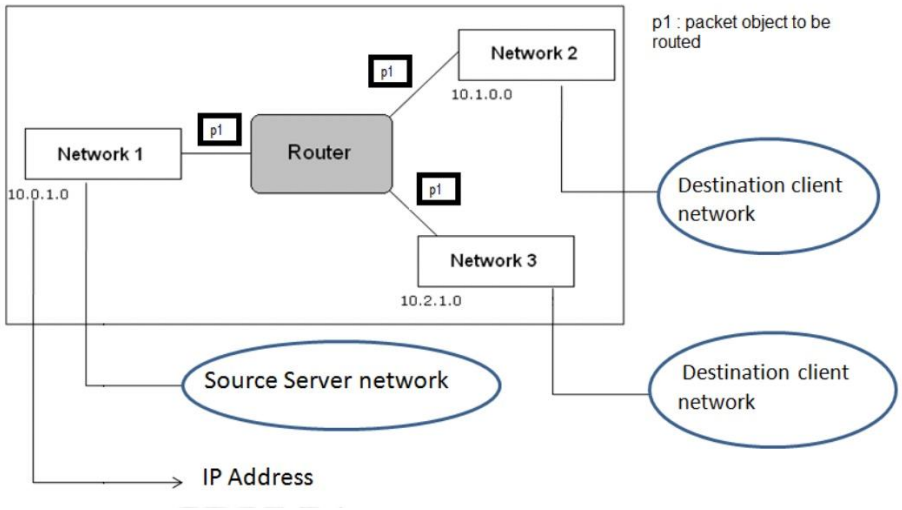


Fig 1 Router and Networks

CHAPTER-2

ROUTER DESIGN

Router- Top Level Block

There are six primary blocks in this design. which are 3 fifo, ff_sync, router_reg, and fsm_router. The fifo and router_reg modules receive their control signals from the fsm_router block.

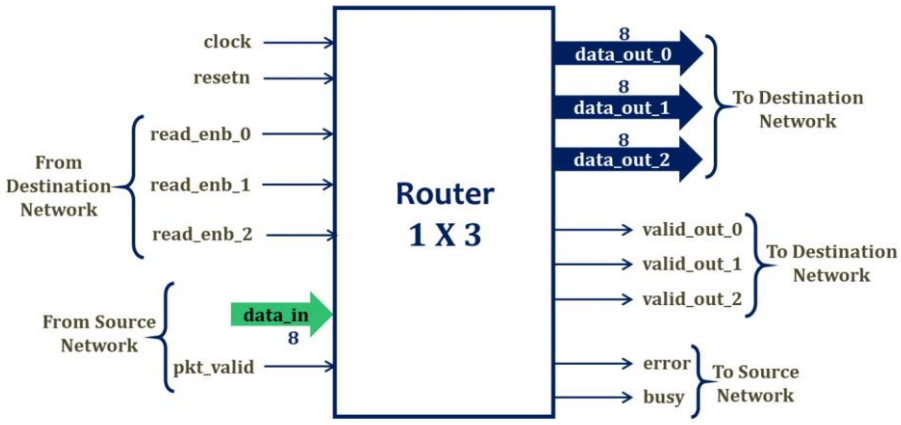


Fig 2 Router top level block

Router- Interface

clock	Active high clocking event
pkt_valid	Pkt_valid is an active high input signal that detects an arrival of a new packet from a source network
reset	Active low synchronous reset
data_in	8 bit input data bus that transmits the packet from source network to router
read_enb_0	Active high input signal for reading the packet through output data bus data_out_0
read_enb_1	Active high input signal for reading the packet through output data bus data_out_1
read_enb_2	Active high input signal for reading the packet through output data bus data_out_2
data_out_0	8 bit output data bus transmits the packet from the route to destination client network
data_out_1	8 bit output data bus transmits the packet from the route to destination client network 2
data_out_2	8 bit output data bus transmits the packet from the route to destination client network 3
vld_out_0	Active high signal that detects that a valid byte is available for destination client network 1
vld_out_1	Active high signal that detects that a valid byte is available for destination client network 2
vld_out_2	Active high signal that detects that a valid byte is available for destination client network 3
busy	Active high signal that detects a busy state for the router that stops accepting any new byte
error	Active high signal that detects the mismatch between packet parity and internal parity

Router top - Overview

- The Router 1x3 design employs a packet-based protocol to accept network packets from a source LAN through the data_in input as well as analyse them byte by byte on the rise edge of the clocks. The resetin signal denotes a synchronized reset with an active-low state.

- The beginning of a new packet be marked by asserting pkt_valid and conclusion of the packet gets indicated by de-asserting pkt_valid. The architecture keeps the incoming packet within a FIFO as per the destination address of the packet. The design has had 3 FIFO's for appropriate destination LANs.

- During packet read procedure, the destination LANs monitors vld_out_x (x might be 0,1 , or 2), and then asserts read_enb_x. The packet is read by the target LAN's via the channels data_out_x

- Sometimes, router might come into a busy condition which is represented by the signal busy. The busy signal is delivered back to the source LAN in order to ensure the source needs to wait to transmit the next byte of the packet.

- To ensure the validity of the packet, acquired by the router, we implemented a failure detection technique i.e parity check. If the result is a disparity in the parity byte transmitted by the source LAN and the internal parity computed by the router, therefore the error signal is asserted. This signal of error is transmitted back to the source LAN so that if the monitoring shows the same, the source LAN may resend the packet.

- The system can receive just 1 packet at a time, however 3 packets may be read concurrently

Router- 1x3 Features

- Packet The routing process: The packet is pushed via the initial port then directed any of the consequent ports dependant on the network's target address.
- Parity checking is a technique of identifying mistakes used to verify the correctness of digital information that is being transferred throughout a connection between a client and server. This strategy assures that the client internet gets the data sent by the server network undamaged.Reset: The router is reset using an Strong minimum synchronised input. Once the router is reset, the frame-in-frame (FIFO) gets vanished and the authorised towards signal goes low, signalling that there are no acceptable packets are discovered At the final information bus.
- To send a packet, see the router input protocol.
- Examining the packet: Consult the router output protocol

Router- Packet

The packet format is comprised of three components: the header, payload, and parity. Each component has a width of eight bits, and the payload's length can range from one byte to sixty-three bytes.

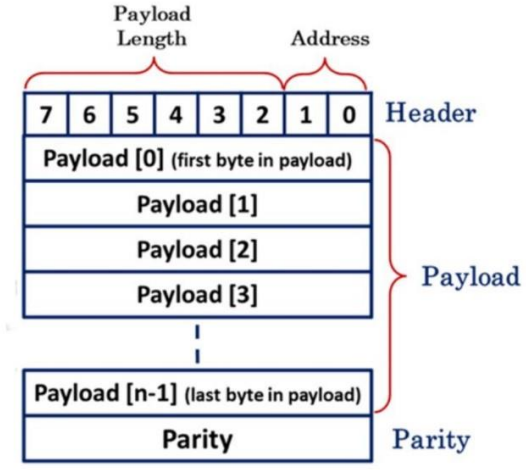


Fig: packet format

- The header: The package header includes two fields such as length as well as DA.

- DA: Its packet's addresses for the the destination comprised of two bytes. The network device transmits the packet to the right port depending on its Targeting Location. Every output port has an individual ip number. consisting of two bits. If the intended location and port addresses match, the router routes send the data packet to the resultant connection.

- Length: The information is six bits long. It indicates how many bytes of data there are. A packet's data size can range from one byte at the lowest to 63 bytes at the highest.

- If Length = 1, so the information length is one byte.

- If duration equals 63, the information is 63 bytes long.

- The information data is the carrier. The bits should be employed to represent data.

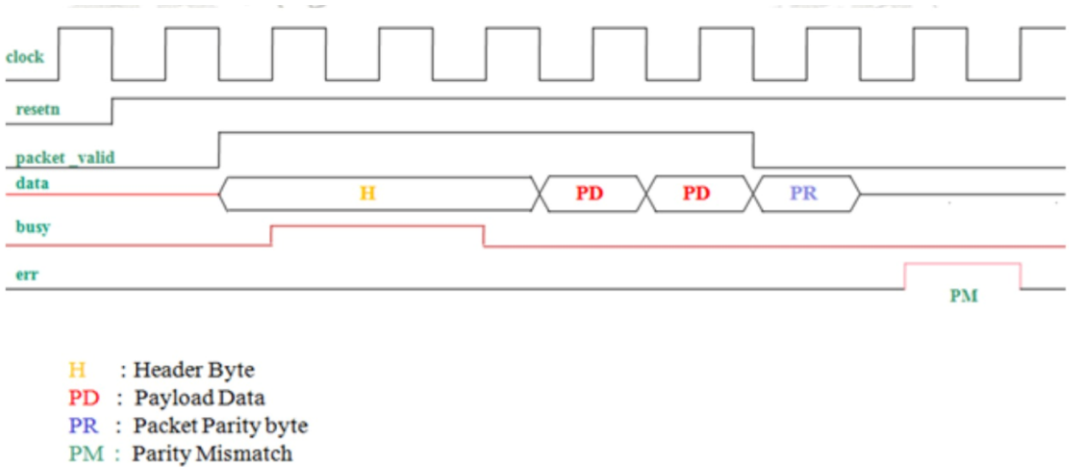
- Parity: This place contains the packet's security check. As mentioned below, it is determined as bitwise parity between each packet's header in addition to load byte values.

CHAPTER-3

ROUTER - INPUT & OUTPUT PROTOCOL

Router – Input Protocol

Fig 4



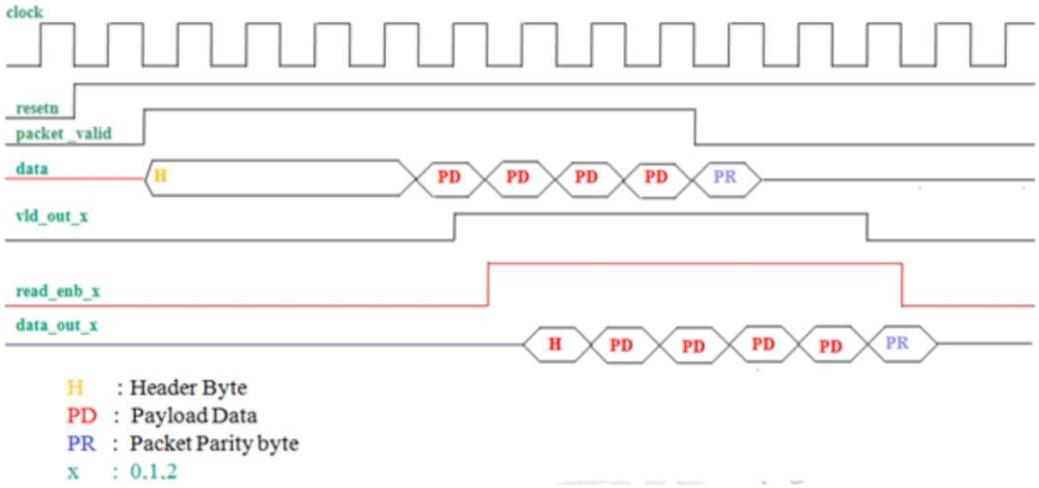
DUT entry method has the following features:

- Test bench note: All input signals are synced to the clock's falling edge and are active high, with the exception of the active low reset. This is a result of the DUT router's sensitivity to The clock's increasing tip. Driving input signals on the falling edge of the test bench therefore guarantees proper setup and hold durations. However, the clocking block in the SV/UVM-based testbench may be used to drive inputs on the clock's positives edge, so preventing metastability.
- When the header bit is transmitted to the information entering the bus, the packet_valid signals becomes true on the same clock edge.
- The address provided in the header byte tells the router what kind of output channel the packet ought to be routed through.
- With respect to each new falling edge generated by the clock, drive the payload's subsequent bytes following the header byte from the input component of the data bus.
- The packet parity byte must be driven after the final payload byte, and the packet

with the valid signal must be distributed on the next falling clock. This signifies that the package is complete.

- When a busy signal is detected, the test bench should keep the previous driven value rather than driving any bytes..
- When the busy signal is asserted, any incoming data byte is dropped.
- When a packet parity mismatch is found, the err signal is asserted.

Router- Output Protocol



- The following are the features of the output protocol
- Note for Testbench : Every output signal is synced with the clock's rising edge and is active high. The output port data_out_X gets buffered by a 16x9 FIFO.
- When it receives valid data, the router asserts the vld_out_x signal. This is a signal that the Data is provided on a specific Data is output from the bus to be processed by the the recipient's client.
- The packet receiver will then react with the read_enb_X signal assertion once it has had adequate room to retain the packet's data.
- When reading data on the data_out_x bus, the read_enb_x input signal might be asserted when the clock is on its falling edge.
- To prevent a time-out and reset the FIFO, assert read_enb_X within 30 clock cycles after asserting vld_out_x. Whenever a packet's bit gets deleted because of an expiration time, the data_out_x bus enters a tristate.

CHAPTER-4

ROUTER TOP ARCHITECTURE AND SUB BLOCKS

Router top- Sub blocks

The following six sub blocks make up the top level block module:

- Register
- Synchronizer
- Finite state machine
- 3 FIFOs

Top Router- Block level architecture

The diagram below depicts the router's top-level architecture, including input and output. signals between various components such as FIFO, Register, synchronizer, and FSM.

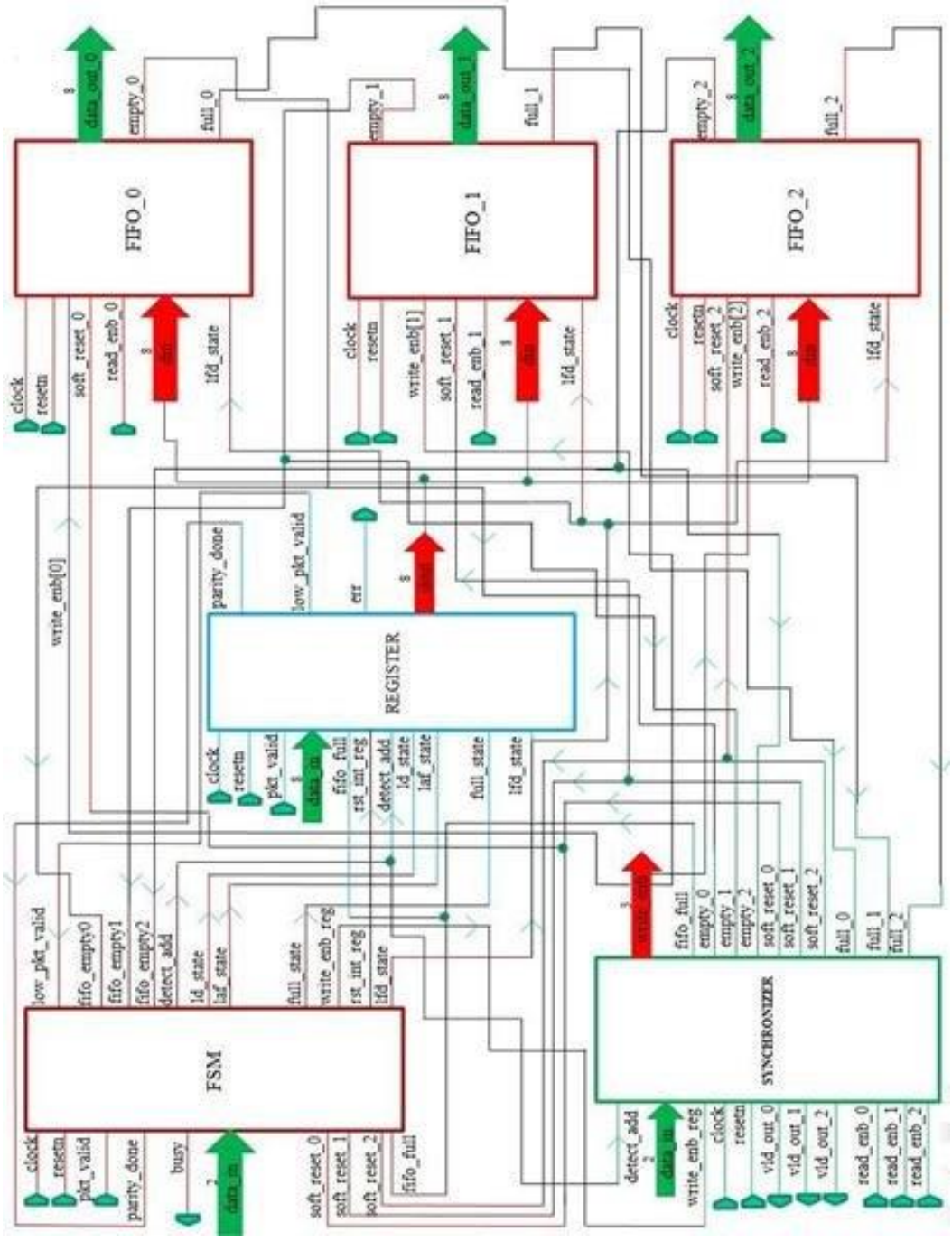


Fig 6: Router top block level architecture

Router- FIFO

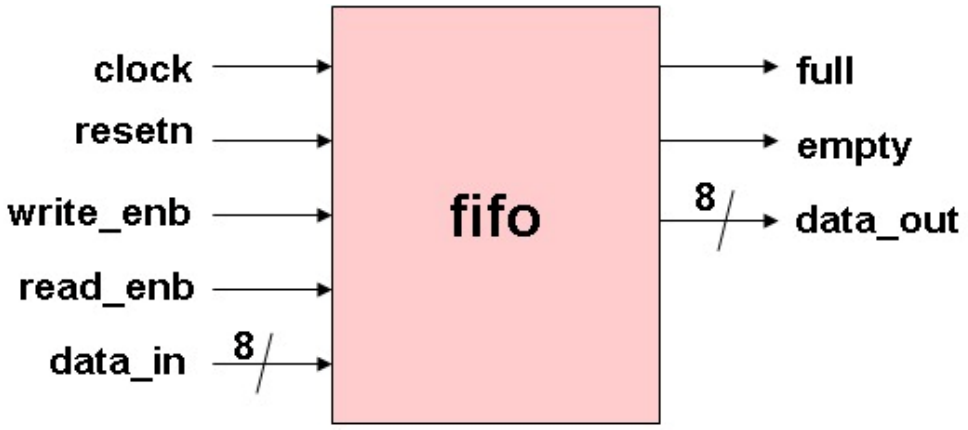


Fig 7: FIFO

Functionality:

FIFO Block: Every output port has three FIFOs that store information coming from the input port using Control signals are sent given by the 'fsm_routermodule'. When 'fresetn' is low, the file in memory (FIFO) is reset by setting 'full' to 0, 'empty' to 1, and 'data_out' to zero. Data entering 'data_in' will be sampled on the clock's rising edge whenever on the clock's rising edge when'read_enb' is high as well as the FIFO is not empty. Read and write activities can take place concurrently. Full Indicator: The 'full' signal signifies places Within the confines of the FIFO was the case completed written.

If reset_n is minimal, then full = 0, empty = 1, and data_out = zero.

The FIFO memory size is 16 x 9. The additional bit in the data width is used to detect the header byte. Ifd_state detects a packet's header. The ninth bit is set to one for the header byte and zero for the subsequent bytes.

Write operation:

- Whenever value of read_enb does high, signal data_in is collected on the clock's rising edge.
- To prevent an overrun issue, write operations are only executed when FIFO is not full.

Read operation:

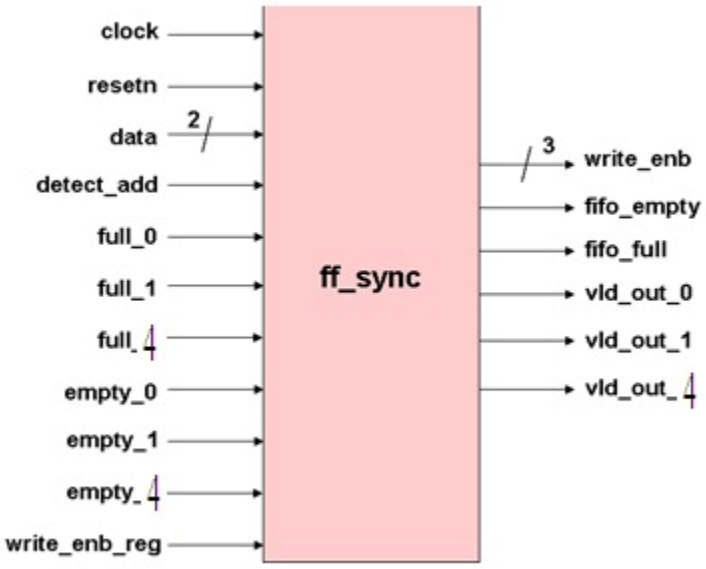
- Every time read_enb has become high, information is read through data_out near the clock's rising edge.
- Read operations may only occur if the FIFO is not empty to prevent underruns.
- The context of the time-out circumstance, full = 0 and empty = 1.

1. In two cases, Data_out is pushed into a the HIGH impedance state:
2. Following the full reading of the FIFO memory

- Whenever the router goes into timeout mode.
- Full-FIFO status, denoting that every location inside FIFO has been recorded.
- **Empty:** This FIFO state signifies that every FIFO location has been read and become empty.

It is possible to conduct read and write operations at the same time.

Router- Synchronizer



Functionality:

The FF_sync module allows an input port to successfully communicate with three output ports by synchronising the fsm_router module using three FIFOs. This module maintains consistent communication with both the fsm and FIFO modules, allowing for smooth interaction It determines the channel address and stores data in the channel's FIFO utilising address or write_enb_sel to do so.

The output signal fifo_full is generated When the current FIFO=full, the output signal fifo_full is generated; when it is empty, the signal fifo_empty is generated. Specifically:

- For data = 00, fifo_full = full_0 & fifo_empty = empty_0.
- For data = 01, fifo_full = full & fifo_empty = empty_1.
- For data = 10, fifo_full = full_2 & fifo_empty = empty_2
- Otherwise, fifo_full = 1 as well as fifo_empty = 0.
- The value of the vld_out signal is created whenever the current FIFO's empty signal goes low, signaling that the FIFO is prepared to be read:
- vld_out_0 = ~empty_0
- vld_out_2 = ~empty_2

- vld_out_1 = ~empty_1

The write_enb signal associated with the selected FIFO, which is decided by the current address, is created using the FSM's write_enb_reg signal. This synchronisation module provides consistent The connection between the single input port as well as the three ports that output by picking a FIFO with the detect_add and data_in signals and routing packets for that FIFO until completion.

- The claim that the presence of the fifo_full signal generally conditional on the whole condition of one The FIFO method_0, FIFO_1, or FIFO_2.
- Whenever data_in matches 2'b00, fifo_full = full_0.
- Whenever data_in matches 2'b01, fifo_full = full_1.
- In the event data_in = 2'b10, set Fifo_full to full_2; alternatively, set it to 0.
- As shown below, the production of the vld_out_x signal is depending on the FIFO's empty condition.
- Vld_out_0 = ~void_0; • ^empty_1 = Vld_out_1.
- Make use of the write_enb_reg signal that create the write_enb signal during the given FIFO's write operation.
- Each FIFO carries three internal resetting signals, in sequence. If read_enb_X does not get asserted inside 30 clock cycles of vld_out_x, both internal restart signals go high.

Router- Controller

Functionality

FSM: The "fsm_router" module contains the router's controller circuit.When a new packet is transferred Other modules utilise these control signals to write data into the fifo by delivering data to its output.

The controlling circuit for the router is housed in the FSM module. this module generates all control signals. Additional design features use these command signals to direct the packet to its destination port.

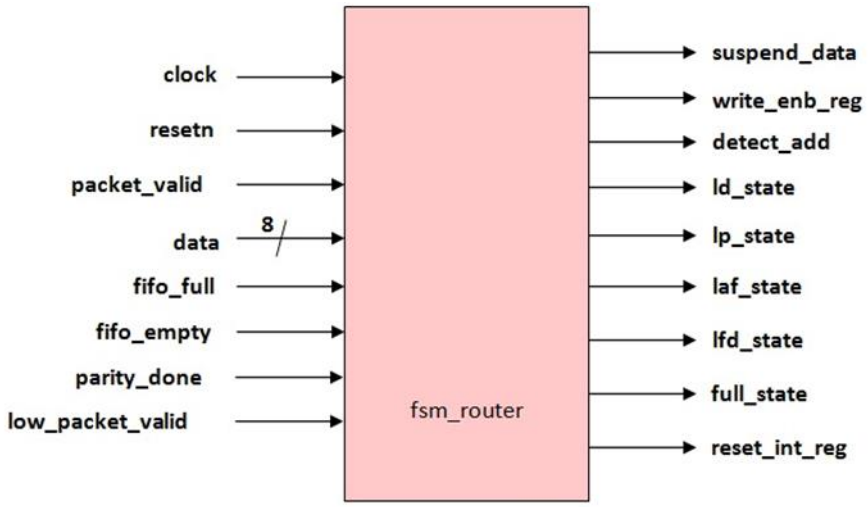


Fig 10: FSM Block

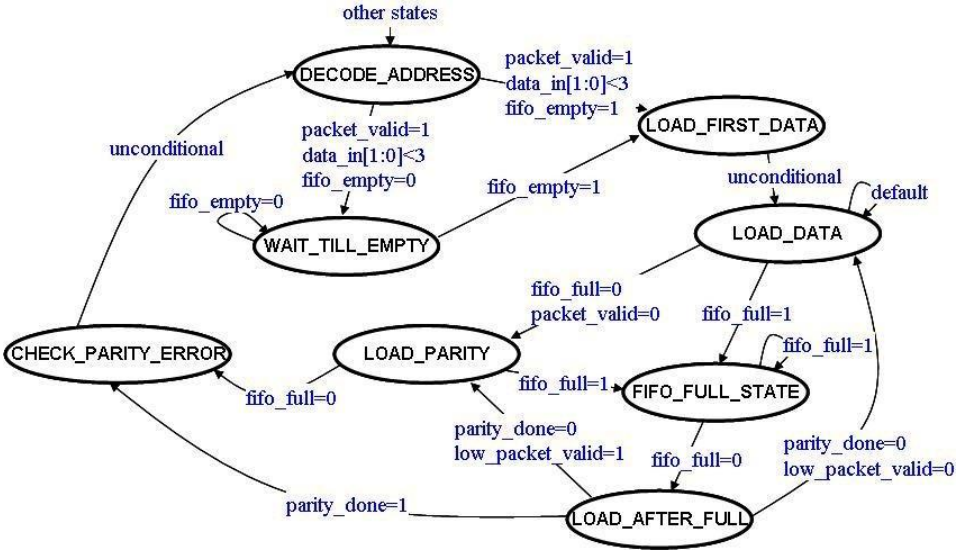


Fig 12: State Diagram

STATE_DECODE_ADDRESS

- This is the starting point of the reset.
- In this state, the signal detect add function, which detects incoming packets, is asserted. The first byte is also regarded as head bit.

STATE-LOAD_FIRST_DATA

- To load the first data bytes through the FIFO, assert any signal lfd_state.
- To prevent the already-latched header byte of being updated to an alternative value for that particular packet, signal busy is additionally asserted.

- Throughout the following clock cycle, the current state gets unconditionally transformed into the LOAD_DATA state.

STATE-LOAD_DATA

• The following state includes the assertion of the ld_state signal, which loads the payloads content inside the FIFO.

• Under such mode, the signal occupied is desserted, enabling the router to acquire new data through the input sources each clock cycle.

• under order to transfer the packet contents to the specified FIFO, indicator write_enb_reg is asserted under this circumstance.

• When pkt_valid is deleted, this state shifts to LOAD_PARITY, as well as whenever the FIFO is full, it switches to FIFO_FULL_STATE.

STATE-LOAD_PARITY

- The parity byte, the final byte, is latched in this state.
- It transitions to the state with no conditions. CHECK_PARITY_ERROR
- When the router receives a signal busy, it stops accepting new data.
- In order to latch the parity byte to the FIFO, Write_enb_reg is set high.

STATE-FIFO_FULL_STATE

- The previously write_enb_reg indication is set to low, but the busy signal becomes set to high.
- The Signal full_state recognizes the FIFO full state as well as asserts it.

STATE-LOAD_AFTER_FULL

- Laf_state, whose captures data after FIFO_FULL_STATE, has been claimed at this point.
- Both write_enb_reg and signal_busy are enabled. When the parity_done signal is high, it means that the LOAD_PARITY requirement has been discovered and the process has moved on to the

DECODE_ADDRESS step.

- The state transitions to LOAD_PARITY. assuming low_pkt_valid is a high number; otherwise, it continues to LOAD_DATA.

STATE-WAIT_TILL_EMPTY

- The write_enb_reg signal has been set low, while the busy signal assumed to set high state.

STATE- CHECK_PARITY_ERROR

- The low_pkt_valid signal is reset in this condition by the generation of the rst_int_reg signal.
- When the FIFO becomes not completely full, this issue state produces DECODE_ADDRESS; when FIFO is full, then converts into FIFO_FULL_STATE.
- In this stage, Busy is affirmed

Router-Register

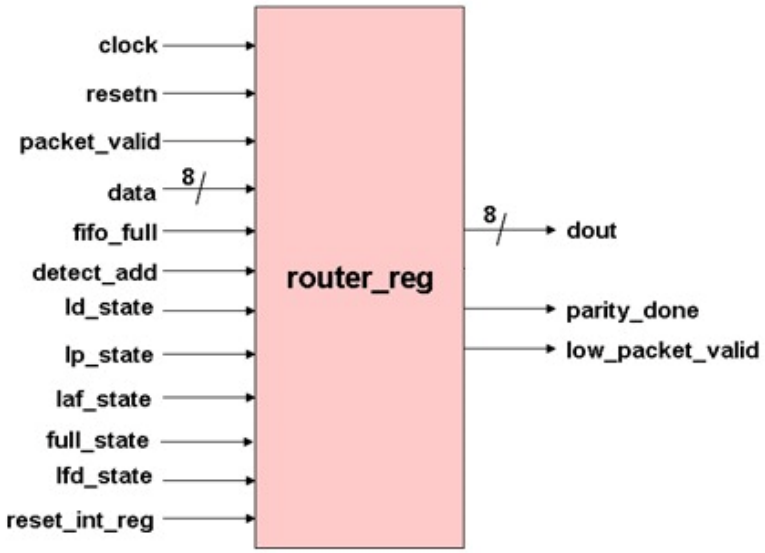


Fig 13: Router Register Block

Functionality:

Router_reg: The router_reg section holds the router_1x3's information, parity,

as well as status registers.Its fsm_router's control signals are used to set these registers to new status or input data . The position, information, and integrity registers are needed by the router are present here.The registers that are included here all latching onto the rising edge of the clock signal. In compliance with condition and status signals for control, information registers latching knowledge obtained from data input along with store it. In addition, information is fed into the parity registers allowing parity calculation, and this information will be evaluated with each packet's parity byte. If the packet parity varies from the calculated parity, an error signal is generated.This module uses four internal registers to record bytes for the header, FIFO full status, packet parity as well as internal parity. This module's registers are all latching onto the clock signal's rising edge. All of the signals—err, low_pkt_valid, parity_done, and dot—will be low if resetn is low. When the conditions listed below are met, the signal parity_done increases.

- When there are no signals and the signal ld_state is high
    - In the case where The prior measurement for parity_done was low. as well as The signals laf_state and low_pkt_valid have been set high as well.
    - Its low_pkt_valid signal gets reset via the Rst_int_reg signal.
    - To reset the parity_done signal, use the detect_add signal.
    - If the ld_state is high but pkt_valid is low, the signal low_pkt_valid is high, indicating that the present packet's pkt_valid was actually abandoned.
- Whenever the packet parity varies from the interior parity, the error is computed following the time the packed parity arrives and becomes high.

CHAPTER-5

SIMULATION AND SYNTHESIS

RTL design procedure

- Check that the RTL is functioning
- Synthesize the RTL
- Implement the top modules in accordance with the architecture and initiate all lower level modules.

Software and system

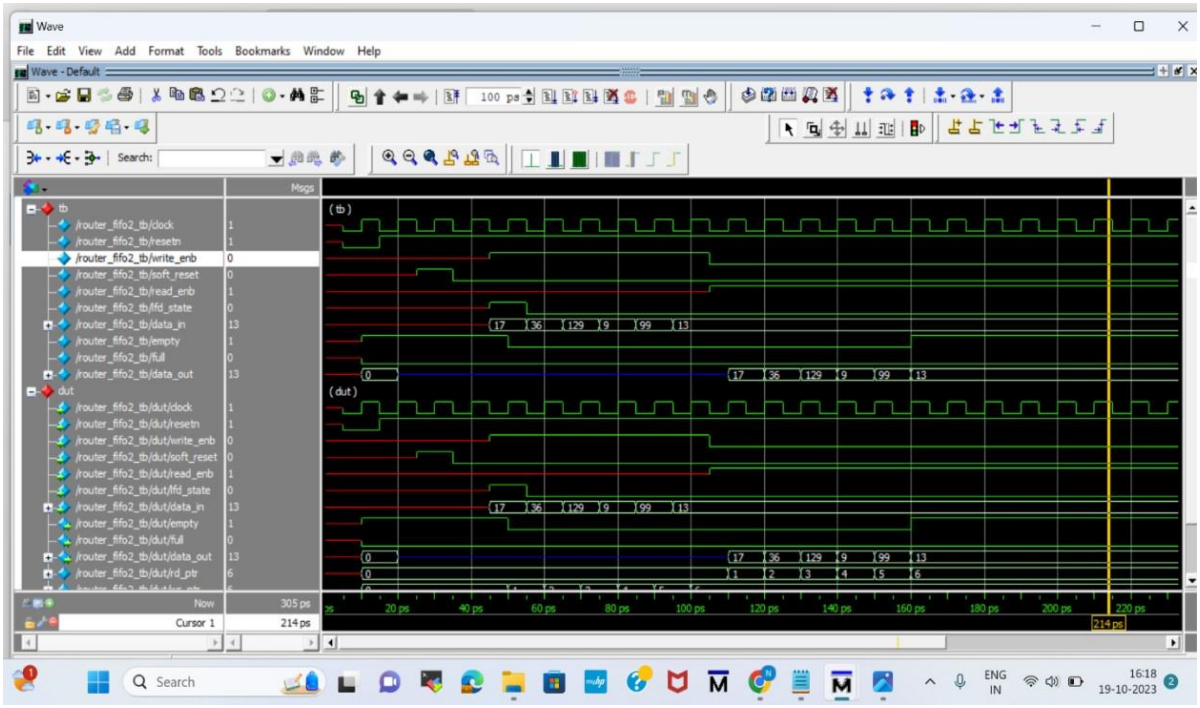
Xilinx 14.7 A software package called Xilinx ISE 14.7 is used to design and test circuits for FPGA and CPLDs. Leading supplier of programmable logic chips and associated software tools, Xilinx, Inc., is behind its development. The most recent version of the ISE design suite, Xilinx ISE 14.7, offers a wealth of features and tools for FPGA and CPLD design. A few of ISE 14.7's main characteristics are as follows:

1. Design entry: A variety of design entry techniques, including as text editors, schematics, and graphical design input tools, are available in ISE 14.7.
2. Synthesis: An excellent synthesis engine built into the program is capable of optimizing and converting a design description into an optimal netlist.
3. Simulation: ISE 14.7 comes with a robust simulator that can replicate and confirm designs prior to their hardware implementation..

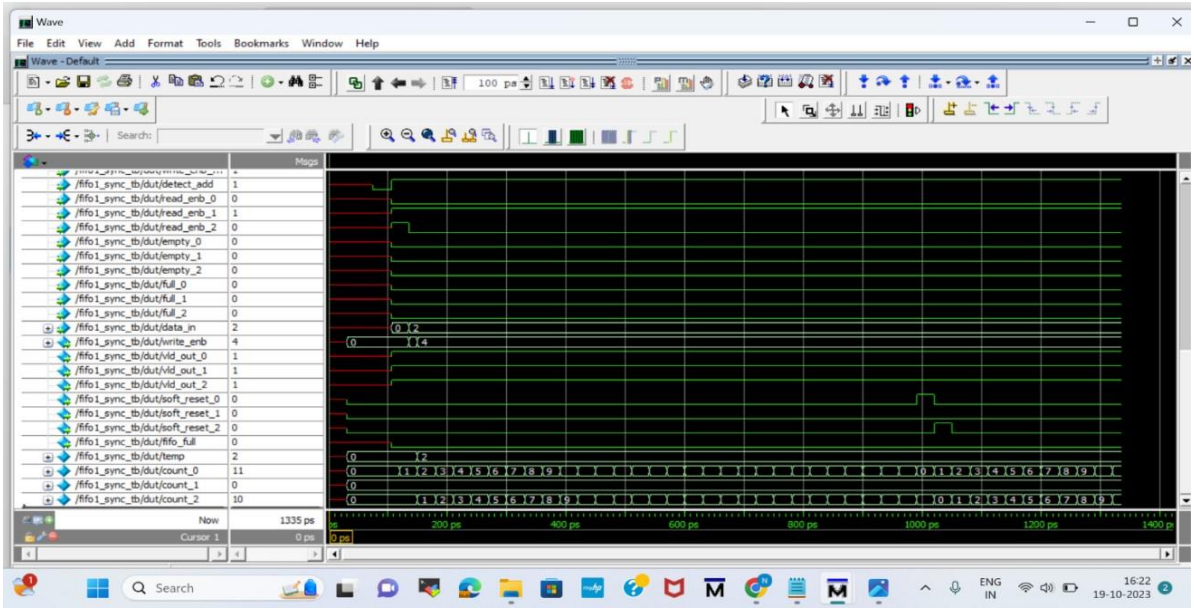
4. Implementation: Advanced placement and routing algorithms included in the software package can optimize designs for certain FPGA devices and target technologies.

5. Timing analysis: Tools for generating timing constraints for a design and performing static timing analysis (STA) are included in ISE 14.7.
6. Debugging: A wide range of debugging tools are included in the program, such as the ability to inspect waveforms, signal values, and other design data. It offers a variety of features and tools that may be applied at every stage of the design process, from the first design entry to the latter stages of implementation and verification. The program is a well-liked option for many in the industry and has been extensively utilized by FPGA and CPLD designers for many years.

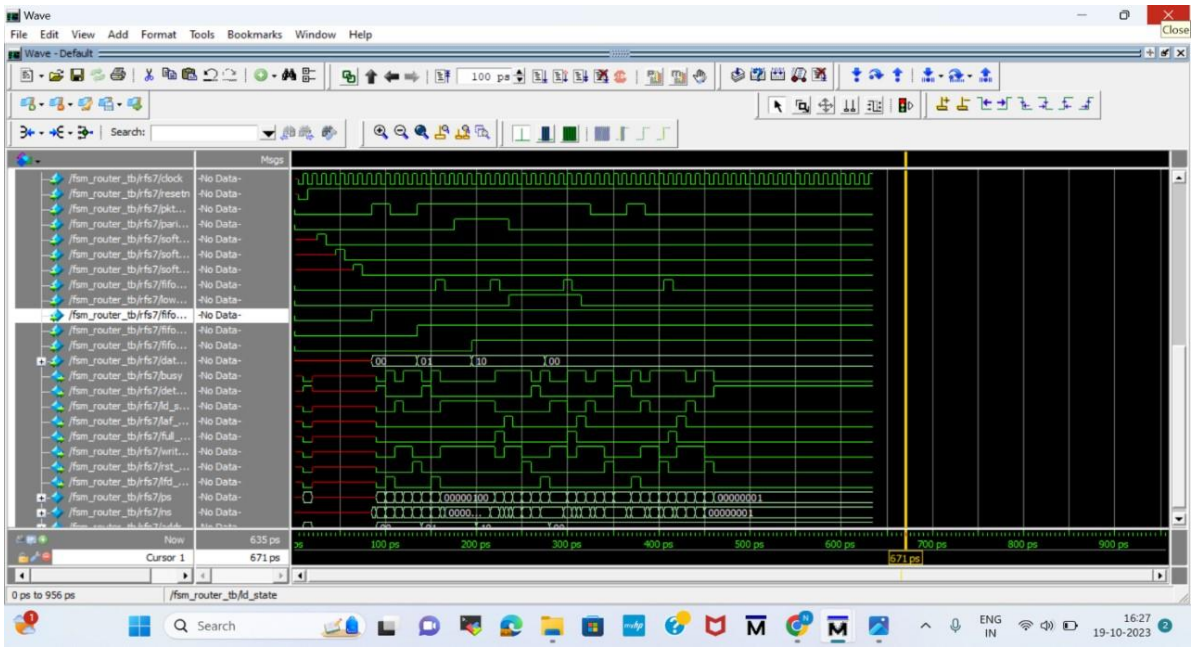
Simulation Waveform FIFO :



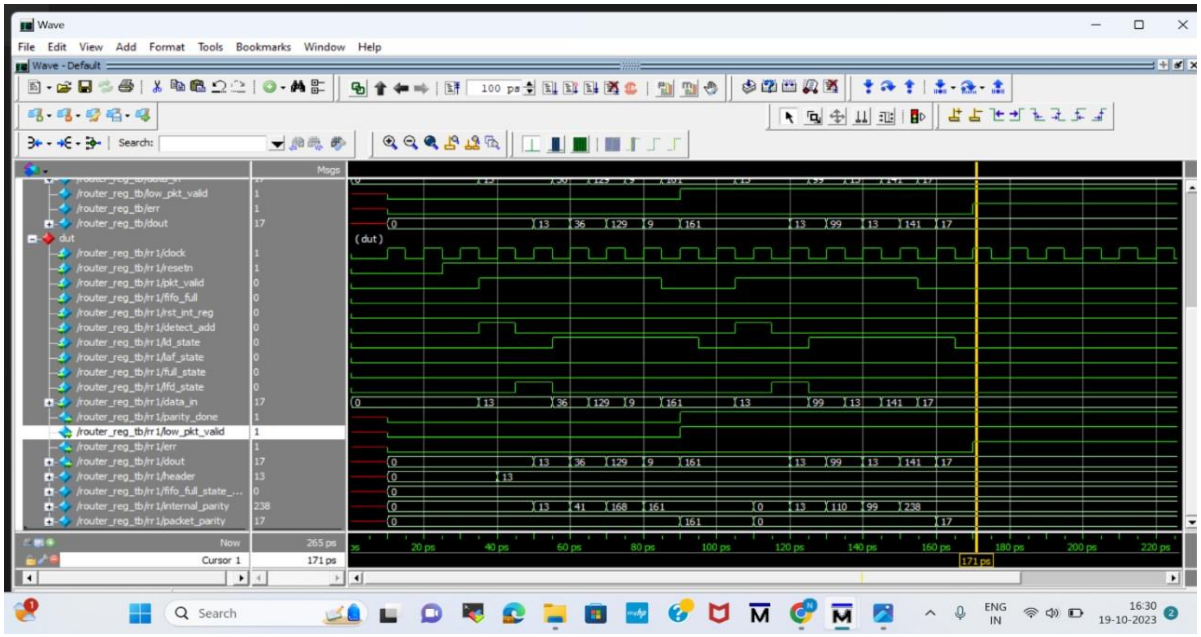
Simulation Waveform SYNCRONIZER:



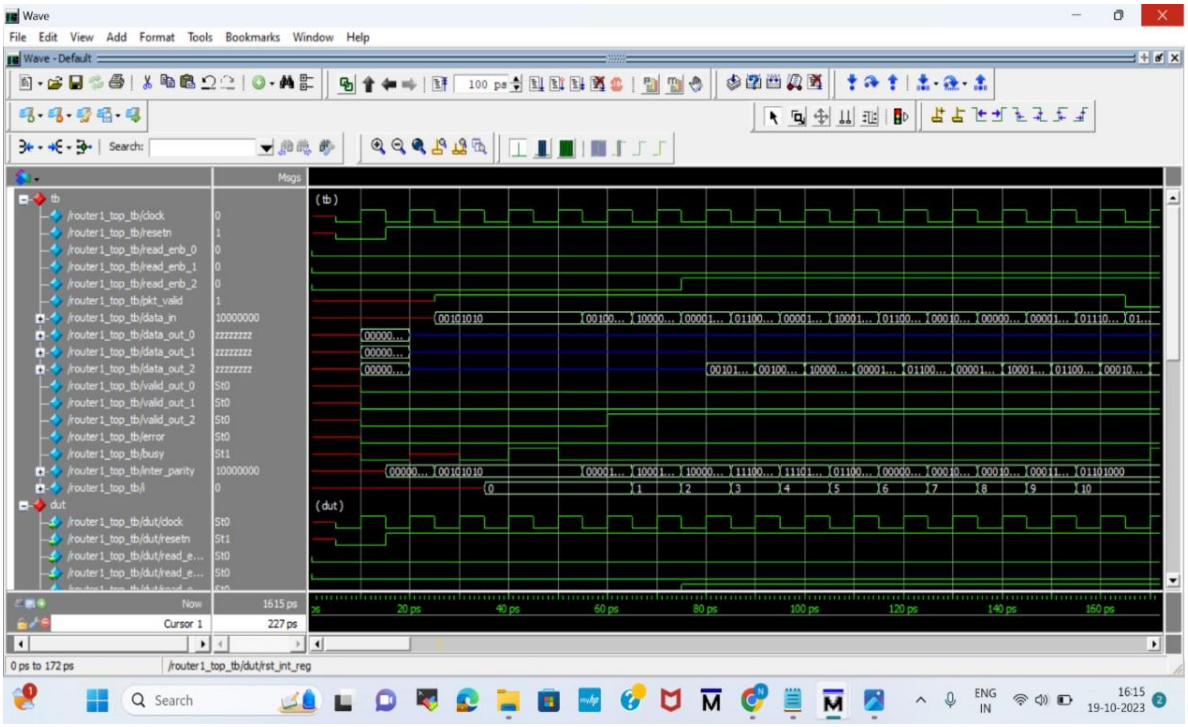
Simulation Waveform FSM :

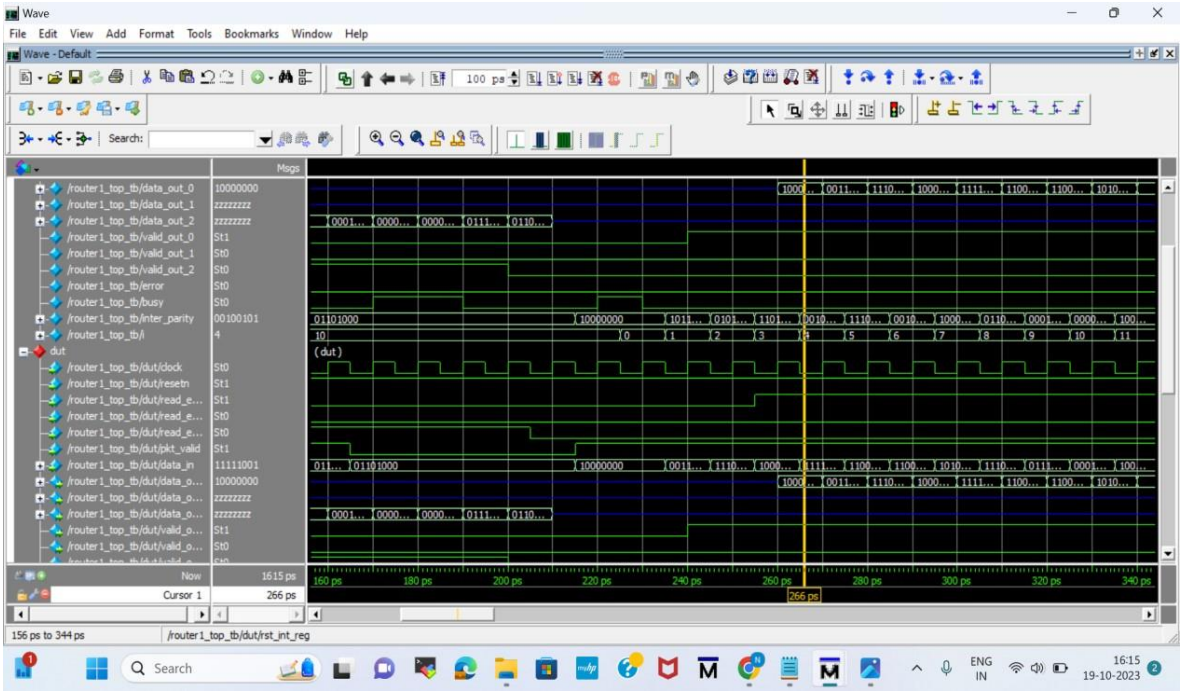


Simulation Waveform REGISTER :

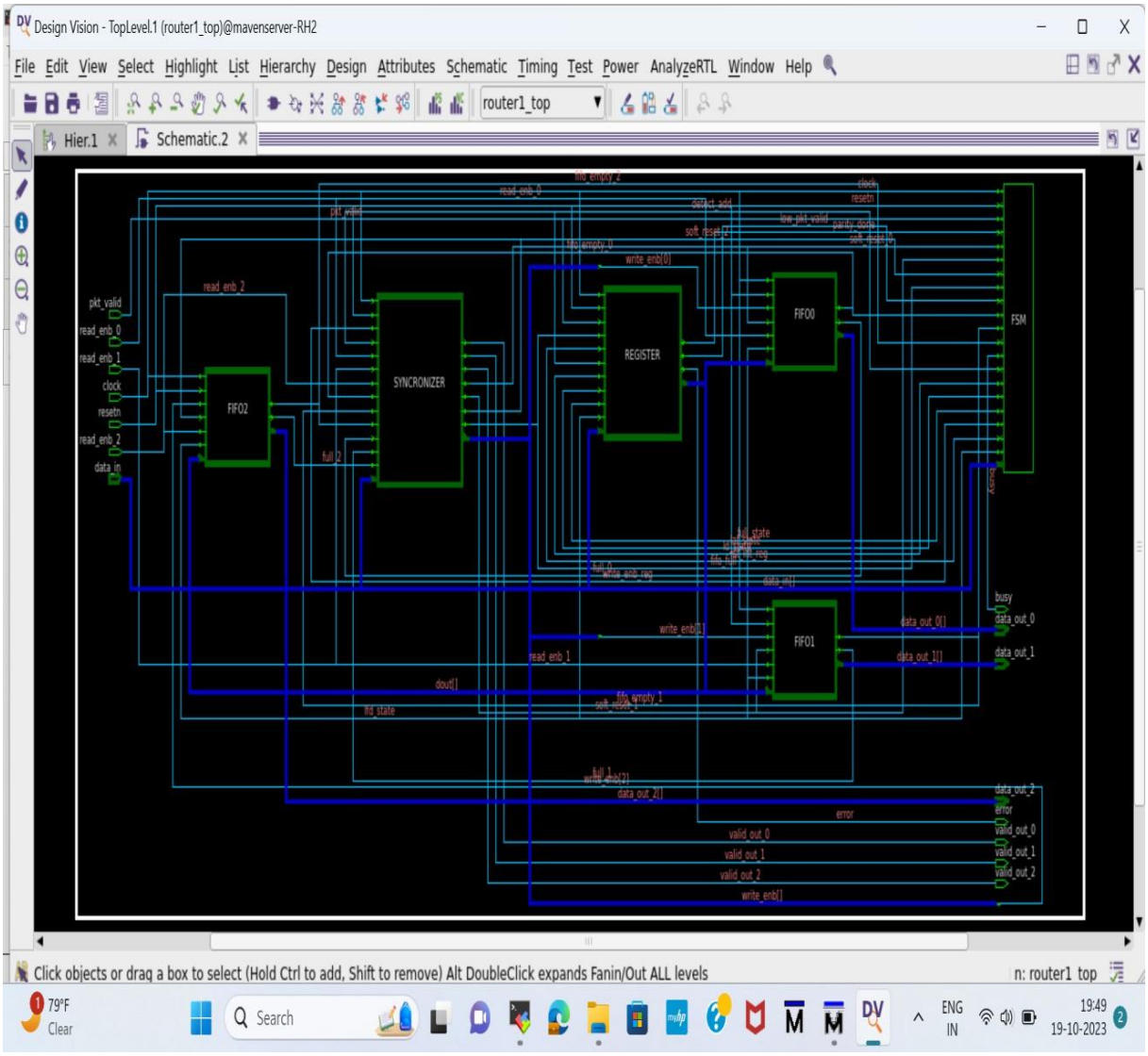


Simulation TOP MODULE:





SYNTHESIS:


Design Vision - TopLevel.1 (router1_top)@mavenserver-RH2
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window Help
router1_top
Hier.1
Schematic.2
pkt_valid
read_enb_0
read_enb_1
clock
resetn
read_enb_2
data_in
FIFO2
SYNCRONIZER
REGISTER
FIFO0
FIFO1
FSM
busy
data_out_0
data_out_1
data_out_2
error
valid_out_0
valid_out_1
valid_out_2
write_enb[]
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove) Alt DoubleClick expands Fanin/Out ALL levels
n: router1 top
79°F
Clear
Search
ENG
IN
19:49
19-10-2023

CHAPTER-6

CONCLUSION AND FUTURE SCOPE

Using the Xilinx ISE IDE Tool to synthesize and simulate the router device, the project successfully met its goals. Response time and frequency were increased when the Finite State Machine was implemented with fewer states. Depending on the destination addresses of the data packets, the router device might route them to one of three output ports. Nevertheless, there were some restrictions and difficulties with the project, such the requirement for rigorous testing and verification to guarantee the network device is operating correctly. The usefulness and efficiency of the router device may be improved with more study and development, for example, by adding security measures. The design and verification of the Router1X3 are successful. Verification involves debugging and fixing a lot of coding problems. Situations such as packets with an 8-byte payload length

- Good packet
- Never-read packet
- read/write operation happens at the same time
- 14 byte
- 16 byte
- 17 byte
- FIFO full state(observing busy signal)
- Bad packet/corrupt packet

were extracted onto the evaluation bench to measure the design's robustness. In order to evaluate the reliability of the design, testbench samples of long and variable payload packets were used. These examples covered instances in which a 14- or 16-byte packet was created, a FIFO was noticed (i.e., a busy signal was observed), and a packets observed while a read/write operation was performed concurrently. The Questasim coverage report, This contains 100% FSM condition inspection, 81.23% FSM transition coverage, 93.41% switch coverage, including 92.40% declaration coverage. showed that everything was running smoothly. It has been demonstrates that the router 1x3 is exceptionally best way created with a low Steady through using the resources provided.

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