DESIGN AND ANALYSIS OF A 45NM LOW-POWER HIGH-STABLE PROPOSED 8T SRAM CELL AND ARRAY

Thesis Submitted
In Partial Fulfilment Of The Requirements For The Degree of

MASTER OF TECHNOLOGY

in

VLSI DESIGN & EMBEDDED SYSTEMS

by

Bhuvnesh Singh
(2K22/VLS/03)

Under The Supervision Of

Prof. Alok Kumar Singh
(Prof. ECE Department, DTU)

Department Of Electronics and Communication Engineering

DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi 110042

MAY, 2024

ELECTRONICS AND COMMUNICATION ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Bawana Road, Delhi-110042

CANDIDATE'S DECLARATION

I, **Bhuvnesh Singh (2K22/VLS/03)**, a student of MTech (**VLSI Design and Embedded Systems**), hereby declare that, in partial fulfilment of the requirements for the award of a Master of Technology degree, we have submitted a Project report on **Design and Analysis of a 45nm Low-Power High-Stable Proposed 8T SRAM Cell and Array** to the Department of Electronics and Communication Engineering at Delhi Technological University. This material is original and not something that was copied from any source without appropriate citation. There has never been a degree, certificate, associateship, fellowship, or other title or honour that is comparable to this one awarded for the work done here.

PLACE: Delhi Bhuvnesh Singh

DATE: 31/05/2024

ELECTRONICS & COMMUNICATION ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Bawana Road, Delhi-110042

CERTIFICATE

I hereby attest that the project report on the topic **Design and Analysis of a 45nm Low-Power High-Stable Proposed 8T SRAM Cell and Array**, submitted by **Bhuvnesh Singh (2K22/VLS/03)** of the Electronics and Communication Department at Delhi Technological University, Delhi, partially fulfils the requirements needed to be awarded a Master of Technology degree. The report is a record of the project work that the student completed under my supervision. To the best of my knowledge, neither this university nor any other has accepted this work in whole or in part for a degree or diploma.

PLACE: Delhi

DATE: 31/05/2024

Prof. Alok Kumar Singh

SUPERVISOR

ELECTRONICS AND COMMUNICATION ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Bawana Road, Delhi-110042

ACKNOWLEDGEMENT

I would like to convey my sincere thanks and debt of gratitude to my very recognised and valued mentor, **Prof. Alok Kumar Singh**, for proposing the subject of my Project Report and for granting me all autonomy and adaptability in my work. Their encouragement has been tremendously inspiring and encouraging, and it has always gotten stronger over time. I could not have attempted this Report without their unwavering support and direction.

Bhuvnesh Singh

2K22/VLS/03

M.TECH: VLSI Design & Embedded System

(2022-24)

ABSTRACT

***Abstract* — The goal of this project is to carry out the new Proposed 8T SRAM cell and also design the array memory of 8-row by the 8-column with technology of 45nm node. Suggested proposed technique to reduce the current of short circuit leakage for that purpose just increases the path resistance of circuit from Vdd to GND. To access the SRAM array there is a 3-to-8 decoder that uses 3-bit address lines. The SRAM cells have been optimised to run read-write operation at cycles 100 MHz frequency while taking less power and maintaining a sufficient static noise margin. Software simulations are used to create and configure both the decode and array of SRAM by using Cadence Virtuoso (ADE) tool. The HSNM increases by 12.42% and The WSNM increases by 18.13% when moving from a 6T to an 8T configuration. The Proposed 8T configuration exhibits a 24.06% decrease in read total power and slight decrease of 1.06% in write total power. It also achieves a 30.20% reduction in write dynamic leakage power and 40.43% reduction in read dynamic leakage power indicating better efficiency during dynamic operations. The recommended technique appears to have a better Static Noise margin and Power Consumption than the standard approach, based on the data.**

keywords — Cadence Virtuoso, 8T SRAM cell, SNM, SRAM Array, Decoder, Layout.

Table Of Contents

LIST OF FIGURES

LIST OF TABLES

CHAPTER 01 INTRODUCTION

1.1 Introduction

Throughout history, semiconductor memories have been a crucial component of computer storage systems. Since random-access memories (RAMs) have faster read and write rates than other memory types, the constant demand for increasing storage capacity with lower power consumption and space usage drives advancement in this area. The two most popular RAM kinds are dynamic RAMs and static RAMs[1].

The proposed system employs SRAM architecture, which was chosen because of its quicker performance than DRAMs, compatibility with CMOS chip technology, and independence from refreshing periodic circuits to ensure the integrity of data throughout the power delivery[1][4]. However, SRAMs often take up more area and are more expensive. SRAM operates as a memory unit without the need for periodic refreshing, allowing each bit to be accessed independently (read/write). It is an important component in low-power VLSI systems. It is notable for its ability to transport data quickly, consume minimal power, and not require periodic refreshes[2][3].

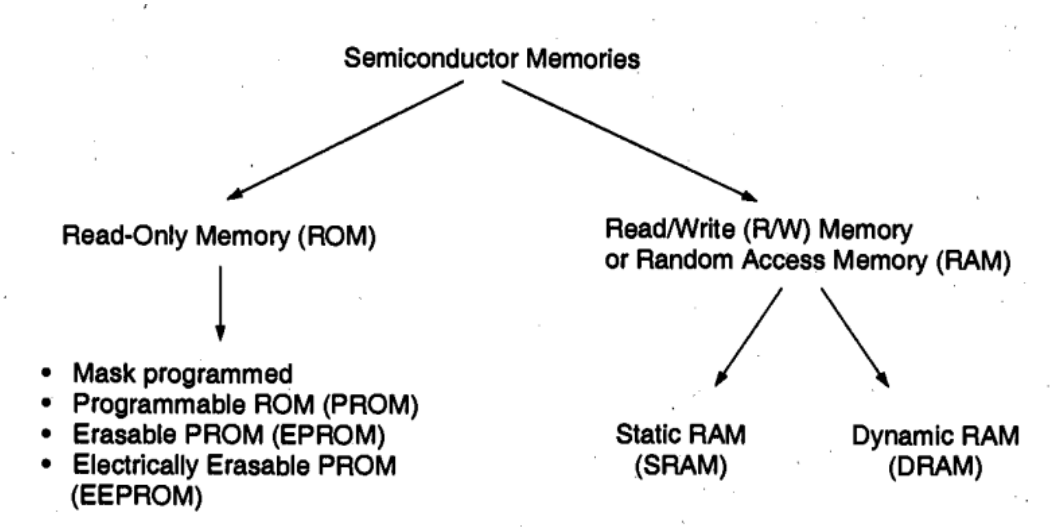


Figure 1.1. semiconductor memory types

The primary design factor which establishes the total storage capacity and, consequently, the cost of per bit of the memory array is the area efficiency, or the quantity of stored data bits per unit area. Memory access time, or the amount of time needed to save and/or retrieve a specific data bit from the memory array, is another

crucial factor. One crucial memory array performance requirement is memory speed, which is determined by the access time. Lastly, given the growing significance of low-power applications, the memory array's static and dynamic power consumption is an important design consideration. In the sections that follow, we will examine various MOS memory array types and go into great length on the issues of space, speed, and power consumption specific to each kind of circuit. Memory circuits are often categorised based on the kind of data access and storage. As the name suggests, read-only memory (ROM) circuits only provide the recovery of previously recorded data; they do not permit the alteration of the stored information contents while the circuit is operating normally. ROMs are non-volatile memories, meaning that even when the power supply voltage is cut off, the data store capacity remains intact. ROMs are classified as mask-programmed ROMs, programmable ROMs (PROM), erasable PROMs (EPROM), & electrically erasable PROMs (EEPROM) depending on the kind of data storage (data write) technology.

On the other hand, data bits stored in the memory array must be able to be modified (written) and retrieved (read) as needed in read-write (R/W) memory circuits. This necessitates a volatile data storage function, meaning that saved data is lost in the event that the power supply voltage is cut. For primarily historical reasons, the read-write memory circuit is generally referred to as Random Access Memory (RAM). The R/W memory array allows for virtually equal access times for all cells, in contrast to sequential-access memories like magnetic tapes. RAMs are divided into two primary groups based on the way that individual data storage cells function: Static RAMs (SRAM) and Dynamic RAMs (DRAM).

Figure 1.2 displays the typical layout of a memory array. Individual memory cells are arranged in an array of horizontal rows and vertical columns to create the data storage structure, or core. Each cell can hold one binary bit of information. Furthermore, each memory cell has two connections: one with the cells in the same row and another with the cells in the same column. This structure is made up of two rows (word lines) and two million columns (bit lines). This means that there are $2^N \times 2^N$ memory cells in total in this array.

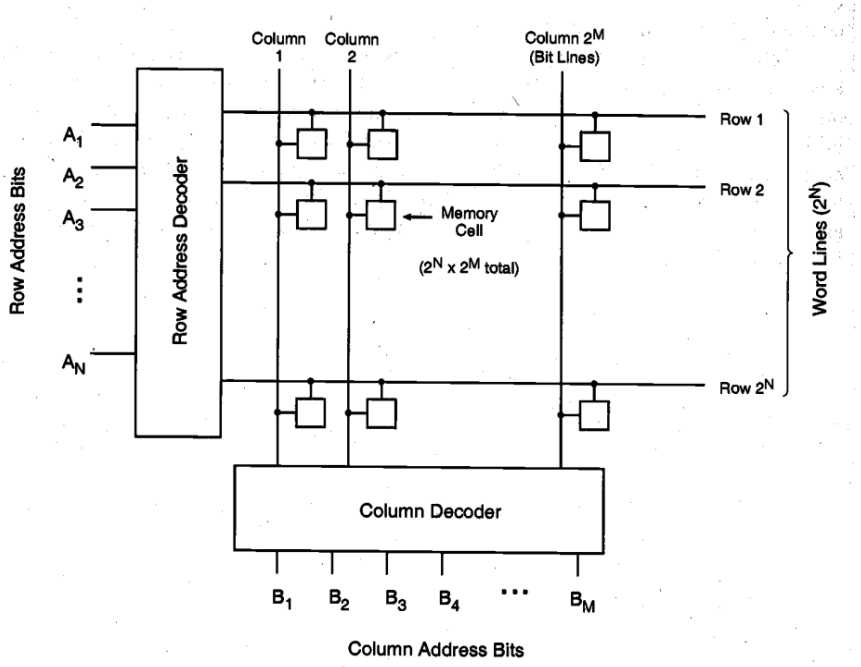


Figure 1.2. Typical RAM array organisation.

A particular memory cell, or a specific data bit in this array, may only be accessed by activating (selecting) the matching bit line and word line. Row and column decoders, respectively, carry out the row and column selection procedures. Whereas the column decoder circuit chooses one out of two million bit lines based on an M-bit column address, the row decoder circuit chooses one out of two hundred word lines based on an N-bit row address. After selecting a memory cell or group of memory cells in this way, a single bit or several bits on a certain row may be the subject of a data read and/or write operation. The column decoder circuit performs the dual functions of choosing the specific columns and sending the associated row's data content to the output.

This brief explanation demonstrates how individual memory cells, regardless of where they are physically located within the memory array, can be accessed for data write and/or read operations in any sequence. Consequently, the array structure under investigation is referred to as a Random Access Memory (RAM) structure. It should be noted that this arrangement may be utilised for read-only and read-write memory arrays. However, because RAM is the well recognised acronym for read-write memories, we shall use it exclusively for these types of memory arrays in the parts that follow.

1.2 Random Access Memory (RAM)

RAM is a sort of memory for computers that temporarily holds data and instructions for use by the CPU (Central Processing Unit) while tasks are being executed. RAM is a volatile memory, which implies that it requires a constant power supply to maintain the recorded data. When the computer or laptop's power supply is turned off, all RAM-stored data is lost.

1.2.1 Types of RAM

RAM comes in two major types:

(i) Static RAM

(ii) Dynamic RAM

Static RAM

SRAM is a type of random-access memory that can hold data bits lasting as long as power is provided. SRAM, unlike dynamic RAM (DRAM), does not require regular updating.

Figure 1.3. Static RAM

Characteristics of Static RAM

- ➢ SRAM is significantly quicker than DRAM.
- ➢ SRAM has more storage than DRAM.
- ➢ SRAM requires less electricity to operate.

Advantages of Static RAM

- ➢ SRAM is minimal in power consumption.
- ➢ SRAM provides quicker access rates than DRAM.
- ➢ SRAM aids in the creation of a speed-sensitive cache.

Disadvantages of Static RAM

- ➢ SRAM has a lower memory capacity.
- ➢ SRAM has greater production costs than DRAM.
- ➢ SRAM has a more sophisticated design.

Dynamic RAM

DRAM is a type of random access memory that allows you to store individual data bits in independent capacitors within an integrated circuit. Many modern desktop PCs come with dynamic RAM like standard memory.

Figure 1.3. Dynamic RAM

Characteristics of Dynamic RAM

- ➢ DRAM is slower than SRAM.
- ➢ DRAM is cheaper than SRAM.
- ➢ DRAM has a high electrical consumption.

Advantages of Dynamic RAM

- ➢ DRAM offers lower production costs than SRAM.
- ➢ DRAM provides higher memory capacity.

Disadvantages of Dynamic RAM

- ➢ DRAM has sluggish access speeds.
- ➢ DRAM has a significant power consumption.
- ➢ Power outages might result in the loss of DRAM data.

1.3 Memory and Logic Area Trend

Today, the most common and extensively used approach to machine programming is based on a collection of instructions or programmes. These instructions allow the execution of a variety of operations, including:

- ➢ Data transfer is the movement of data between various areas of a computer or memory.

- ➢ Directing the flow of execution by changing the order in which instructions are performed.
- ➢ Arithmetic computations involve mathematical operations like add, subtraction, multiplication, and division.
- ➢ Performing logical operations like AND, OR, NOT, and XOR.
- ➢ These instructions may optionally have data operands, which are the values or variables on which the instructions act.

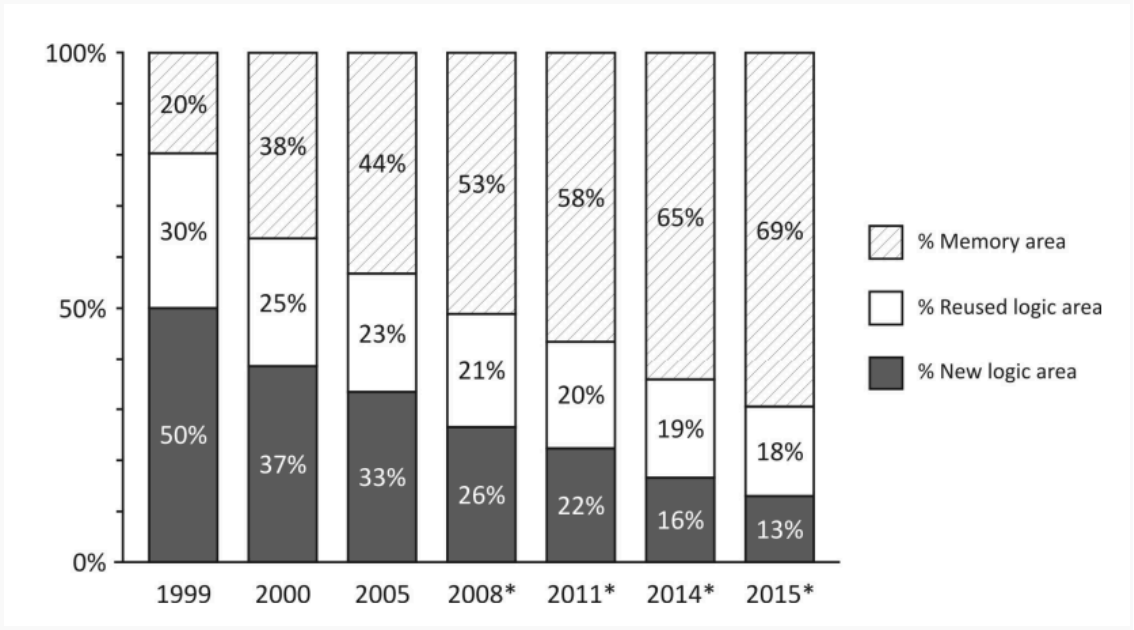


Figure 2.1. Memory and logic area trends

There are essentially two methods for speeding up code execution. The first option involves increasing the processor's operational frequency. However, as previously noted, this is difficult because of the enormous power consumption required. The second way takes advantage of the program's available Instruction-Level Parallelism (ILP). This involves attempting to execute two or more instructions at the same time. The interdependence of data and control systems presents the most significant obstacle to this method. For example, if the output of one instruction is required as input for another, the two instructions cannot be performed concurrently. Modern microprocessor designs have substantial limits since they have practically exhausted all available ILP.

CHAPTER 02 LITERATURE REVIEW

2.1 Introduction

A literature review is a thorough synthesis and critical examination of previous research and publications on a given topic. It performs many significant functions in academic and professional research.

A survey of existing knowledge gives a complete summary of what is already known about a topic, summarising major results from numerous research and sources. It identifies areas where research is missing, as well as discrepancies or conflicts in current literature. This can assist highlight areas that need more examination. It situates new research within the current body of knowledge, indicating how a new study contributes to or challenges what is previously known. It helps to provide a theoretical framework for future research, frequently synthesising hypotheses that have been used to explain the phenomena under study. It gives information on the procedures that have been employed in past studies, which can help the design of future research. By synthesising current research, a new study's research questions or hypotheses can be better justified.

2.2 Literature Review

Snehith, N., Kumar, E. S., and Rao, K. S.'s (2023) study, "Design and Analysis of 8×8 SRAM Memory Array using 45 nm Technology at 100 MHz," presented at the 2023 IEEE Devices for Integrated Circuit (DevIC) conference, contributes significantly to the ongoing development of SRAM technology. This literature review contextualises their findings in the larger research environment, concentrating on important aspects such as CMOS technology scalability, SRAM cell design, power efficiency, and operational stability. [1].

Arumugam N, Shakthi Priya M, and Suntrakanesh Subramanian's (2021) study, "Design and analysis of SAPON approach: A new technique for Low Power VLSI Design using Cadence tools with Generic 250 nm transistors," presented at the 2021 International Conference on Applied Electromagnetics, Signal Processing, and Communication (AESPC), introduces a novel approach to reducing power consumption in VLSI design. This literature review places their findings into the larger research

landscape, concentrating on key topics such as low power methodologies, the importance of technology scaling, and use of simulation tools in design verification [2].

R. Lorenzo et al. [3], propose a LCNT technique which leads to reduction in the leakage power dissipation which is the major issue in nanoscale CMOS integrated circuits. The various existing techniques for minimising leakage have been reviewed, revealing their strengths and weaknesses. This paper describes the Leakage Control NMOS Transistor (LCNT) technology, which involves adding two N-type transistors to typical CMOS circuits to control leakage. This technique significantly reduces leakage power compared to the existing technique.

C. Kumar et al. [4], proposes The stack ONOFIC approach reduces leakage power in CMOS logic devices. The technique's efficacy is illustrated with a variety of CMOS logic circuits, including NAND, inverter, and NOR. It is compared to classic LECTOR and LCNT reduction methods. In comparison to earlier techniques, the suggested stack ONOFIC methodology reduces power dissipation.

S.H. Choudhari et al. [5], presents the comparison between different SRAM cell topologies focused on the low power and leakage power reduction. Leakage power reduction in memory is crucial, and techniques like Gated Vdd, Source Biasing, Sleep Stack, and MT-CMOS are effective. This study focuses on 6T SRAM cells using 90 nm technology in Cadence Virtuoso, comparing the performance of 6T, 7T, 8T, 9T, and 10T SRAM cells. The analysis covers leakage currents, power, and read behaviour, focusing on parameters like read/write delay and power consumption.

Deepak Mittal and V.K. Tomar suggested a study that compared the 6T SRAM cell to the 7T, 8T, and 9T SRAM cells in terms of read and write delays, read and write powers, & Read and Write Static Noise Margin (RSNM) along with Write Static Noise Margin (WSNM). The Cadence Spectre test system was utilised to generate the findings [8].

Ms. Isma Rizvi, Nidhi, Dr. Rajesh Mishra, and Dr. M. S. Hashmi introduced a paper that demonstrated subjective knowledge of a 6T Static Random-Access Memory (SRAM) cell when it was influenced by noise in the power supply and inverter latch. The Write Margin, Write Time, and Static Noise Margin on Noise Induction have been investigated in 180nm CMOS innovation [9].

The primary goal of a work suggested by Premalatha, K. Sarika, and P. Mahesh Kannan was to control the power dispersal that occurs often in the SRAM cell also known as static random-access memory during write and read operations. Applying

dual limit voltage to the 6T, 7T, 8T, and 9T SRAM cells cured the problem. This study identifies and evaluates the power distribution and delay of all of these cells. This is accomplished using the Spectre test system included in the 90nm Generic Process Design Kit, as well as the Cadence Virtuoso tools.

2.3 Motivation

This Project is a highly technical project involving the development of an 8x8 SRAM memory array in 45nm Technology. Here are some motivations and points of interest related to this project:

Innovation through Proposed Technique: Highlight how the Proposed technique offers a novel approach by efficiently increasing the resistance between ground and Vdd. This addresses the issue of short circuit leakage current during transitions, which is crucial in reducing power consumption and enhancing the efficiency of the memory array.

Technology Advancement: Emphasise the significance of utilising 45nm CMOS technology. Highlight how this specific technology and the proposed technique represent advancements in semiconductor design, contributing to more efficient and powerful memory arrays.

Performance Improvement: Focus on the primary goal of achieving high performance with low power consumption. Discuss how the 3-to-8 decoder efficiently accesses the SRAM array using a 3-bit address, enabling operations at 100 MHz read/write cycles while minimising power consumption.

Simulation and Validation: Discuss the use of Cadence Virtuoso's Analog-Design Environment (ADE) for software simulations. Explain how these simulations were crucial in measuring power usage, latency of READ and WRITE operations, and validating the effectiveness of the LPLCT technique.

Comparative Analysis: Highlight the significance of the results obtained from the project. Specifically, mention the reduction in power consumption achieved by the recommended Proposed technique compared to the standard approach. This emphasises the practical significance and potential commercial implications of the project's findings.

Reliability and Noise Margins: Discuss how the project ensures a suitable margin for static noise while maintaining reliability in memory operations. This is important in real-world applications where stability and robustness are crucial factors.

Future Implications: Discuss potential future applications or developments that can stem from this project. Consider how this innovative technique and its positive results might influence the design and development of future memory arrays or related semiconductor technologies.

The continuous demand for faster, more efficient, and reliable memory solutions in modern electronic devices drives the need for innovative SRAM (Static Random-Access Memory) designs. As technology scales down to nanometer dimensions, the challenges associated with power consumption, leakage currents, and stability become more pronounced. The 45nm technology node presents an opportunity to explore advanced SRAM configurations that address these issues. This project proposes a novel 8T SRAM cell design, aimed at reducing short-circuit leakage currents by increasing the path resistance from Vdd to GND. By implementing an 8-row by 8-column SRAM array, we can evaluate the practical benefits of this design in a real-world application. The integration of a 3-to-8 decoder using 3-bit address lines facilitates efficient access to the memory array, ensuring quick and reliable read-write operations at a frequency of 100 MHz. The motivation for this project is rooted in the need to enhance the power efficiency and stability of SRAM cells without compromising performance. Previous research indicates that traditional 6T SRAM cells, while effective, exhibit significant leakage currents and limited noise margins at lower technology nodes. Our proposed 8T SRAM cell not only improves the Static Noise Margin (SNM) but also significantly reduces dynamic leakage power during both read and write operations. Software simulations with the Cadence Virtuoso Analogue Design Environment (ADE) tool show that the proposed 8T configuration improves the Hold Static Noise Margin (HSNM) by 12.42% and the Write Static Noise Margin (WSNM) by 18.13% over the 6T configuration. The suggested design also achieves a 24.06% reduction in total read power, a small drop of 1.06% in total write power, a 30.20% reduction for write dynamic leakage power, and a 40.43% reduction for read dynamic leakage power. The compelling improvements in power consumption and noise margins underscore the potential of the proposed 8T SRAM cell to deliver better efficiency during dynamic operations. This project's findings could lead to more robust and energy-efficient memory solutions, meeting the stringent requirements of modern electronic applications. Therefore, the motivation behind this research is to push the

boundaries of SRAM design, achieving a balance between power efficiency, stability, and performance in advanced semiconductor technologies.

In essence, the motivation behind this project lies in developing a novel technique to optimise SRAM memory arrays, reducing power consumption while maintaining high performance and reliability. The project's findings hold promise for more efficient and advanced memory array designs in semiconductor technology.

CHAPTER 03 PERFORMANCE PARAMETER

There are four most important performance parameters to be measured for an SRAM cell.

TABLE I

OPERATIONAL PARAMETER VALUES

Control Line	Hold	Read 1	Read 0	Write 0	Write 1
WL (Word line)	0	1	1	1	1
BL (Bit Line)	x	1	1	0	1
BLB (Bit Line Bar)	x	1	1	1	0

3.1 Write Delay

Bit line bar (BLB) and Q are the measurement points for the write delay. When word-line (WL) is enabled then access transistors are turned on so there is a path from BL to Q and BLB to Q_bar created. Inside an SRAM cell, "Write Delay" refers to the time necessary to complete 50% of the BL input waveform to reach 50 % to the Q output waveform. This requires a high word line. Data is written into a cell using this method. For instance refer Table I, when WL=1, to write 1 in Q then BL=1, BLB=0 and for write 0, BL=0 and BLB=1. Word Line Activation The delay is the amount of time it takes for the word line signal to spread and activate the access transistors [5]. It is dependent upon the word line's capacitance and WL driver strength. Bit Line Transition Delay is the time it takes to move bit lines from their precharged condition to the appropriate logic levels. It involves dealing with the bit line capacitance and driving strength of the write driver. Cell Write Time regulates when the access control transistors are switched on and the bit lines are driven, allowing the data to flip the state of the SRAM cell. This includes either discharging or recharging the SRAM cell's inner nodes. The cell write time is determined by the sizes of the access transistors, cell the transistors, and parasitic capacitors.

The total of the separate parts represents the overall write delay:

$$t_{write} = t_{WL} + t_{BL\ transition} + t_{cell\ write} \quad (1)$$

3.2 Read Delay

The time it takes to read a piece of data stored in a SRAM cell is known as the read delay. Due to its effect on the total speed of data access, this delay is critical to the memory's performance. This is the amount of time needed for the WL signal to spread and activate the pass-gate transistors, or access transistors. It is dependent upon the word line's capacitance and word line driver strength [5][6]. After the word line triggers the access transistors, the bit line starts to drain (or charge, according to the bit that is stored). A known voltage (Vdd/2) is pre-charged to the bit line. Here, the bit line's RC time constant and the transistors' driving intensity decide the delay. This is an approximation of the bit line delay:

$$t_{BL} = R_{access}.C_{BL} \tag{2}$$

where R_{access} is the resistance of the access transistor and C_{BL} is the capacitance of the bit line.

A small voltage difference must be detected by the sense amplifier and amplified to the full logic level. Sensing delay may be described in terms of input differential voltage and sense amplifier design.

The total of the separate parts represents the overall read delay:

$$t_{Read} = t_{BL} + t_{WL} + t_{sense} \tag{3}$$

3.3 Static Noise Margin (SNM)

The SNM idea is crucial in the design of SRAM cells. This parameter serves as a measure of data stability under varying operational conditions such as temperature fluctuations and manufacturing discrepancies [7]. Specifically, SNM measures a memory cell's resistance to noise-induced state transitions, such as going from 0 to 1, or the other way around. A greater SNM indicates improved SRAM cell stability. Specifically, RSNM concentrates on evaluating cell stability during read operations to guarantee precise and trustworthy data recovery[6]. This curve illustrates the performance of the SRAM cell during read operations, highlighting the crucial part RSNM plays in ensuring accurate data retrieval.

3.4 Average Power Dissipation

Static and dynamic power consumption stand as pivotal factors influencing the overall energy utilisation within an S-RAM (Static Random-Access Memory) cell.

Static power, commonly termed as leakage power, delineates the energy consumed by the S-RAM cell even in its idle state, devoid of active read or write operations [5]. In contrast, dynamic power includes the energy consumed during the dynamic processes of loading and unloading a node while read/write operations. The static current consumption, called P_{Static}, is mainly due to transistor leakage currents. The encapsulation equation for static power is formulated as follows:

$$P_{Static} = N.\ I_{peak}\ .\ V_{dd} \tag{4}$$

When reading and writing are being done in an S-RAM cell, internal node loading and unloading is correlated with dynamic power consumption $P_{Dynamic}$. This type of current usage is directly correlated with multiple SRAM cell characteristic variables, such as switching activity (AA), capacitance (CC), supply voltage (Vdd), and frequency (ff). The dynamic power is represented by the following equation:

$$P_{Dynamic} = \frac{1}{2} C.\ V_{dd}^{2}.\ f.\ A \tag{5}$$

CHAPTER 04 PROPOSED CIRCUIT

3.1 Static Random Access Memory (SRAM)

3.1.1 Circuit

The 6T SRAM cell, seen in Fig. 1, To preserve the stored data, this circuit mainly uses two back-to-back inverters. The reading and writing to the inverters is done by transistors M6 and M5. Once the WL activates M6 and M5, then the stored data is stored in Q and Q_bar nodes from the BL node and Bit-Line-Bar (BLB) node, respectively during the write operation and vice versa for read operation. M5 and M6 provide high and low signals to the BL and BLB, changing the values of Q and Q-bar.

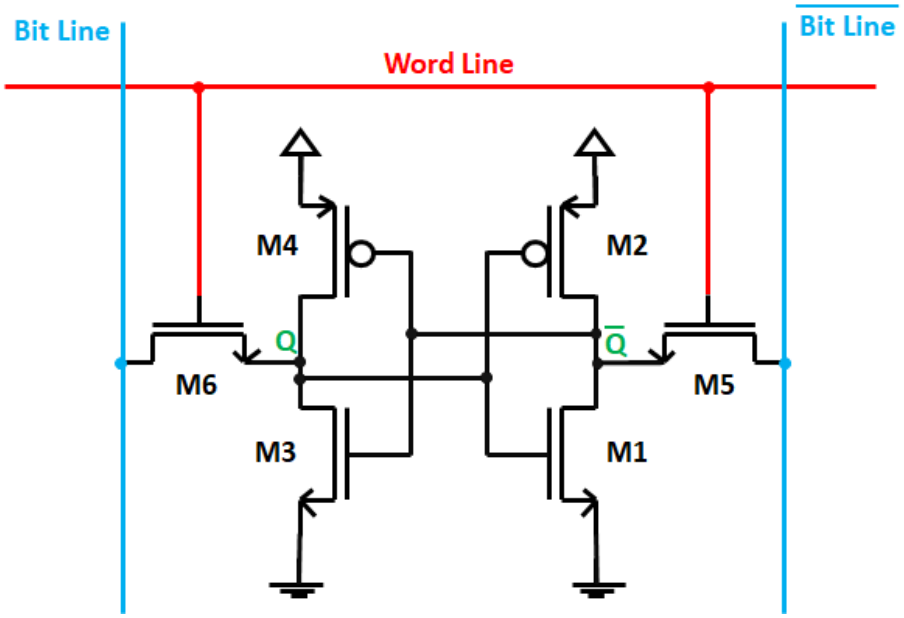
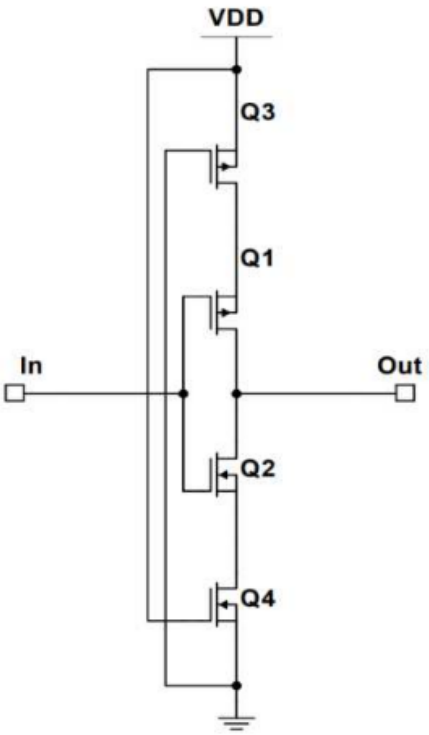
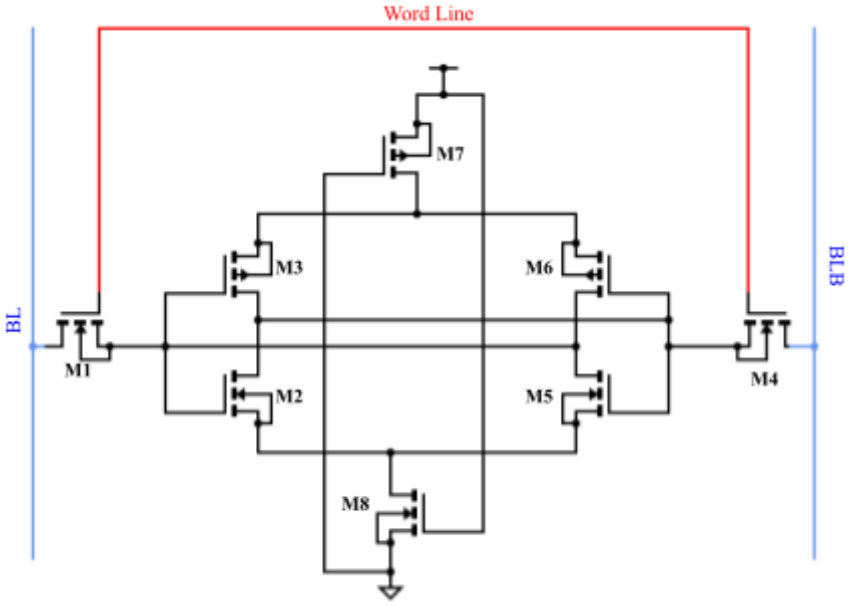


Fig. 4.1. Simple 6T SRAM Cell.

Similarly, The Proposed 8T SRAM cell, seen in Fig. 2, is the fundamental building unit of the suggested SRAM array. Additional leakage-control transistors are integrated to enhance the resistance between Vdd and GND. This helps to reduce leakage of short-circuit current during the changeover period [2].



(A)



(B)

Fig. 4.2. LCT inverter(a) Proposed 8T SRAM(b) Cell.

It uses two leakage-control transistors (Q7 & Q8) that are linked in series between VDD and ground due to the sub-threshold leakage reduction in levelling phase[2]. Ground and Vdd are linked to the gate terminals of leakage-control Transistors (PMOS and NMOS), respectively. As seen in Fig. 2, leakage-control PMOS

(Q7) is positioned above the pull-up network and leakage-control NMOS (Q8) is positioned below the pull-down network. Due to their requirement to function in an active zone, these two leakage-control transistors are active during all phases. As a result, it maintains minimal power consumption across circuits to provide desired output.

When a logic 0 is used as an input, transistors Q7 and Q8 stay active. In this situation, the NMOS is on in the pull-down network and the PMOS is on in the pull-up network, resulting in a 1 output. For logic 1 input, the output is set to zero.

TABLE 4.1

OPERATION OF LCT INVERTER

INPUT	PMOS	NMOS	LCT inverter	OUTPUT
0	ON	OFF	ON	1
1	ON	OFF	ON	0

To ensure the confidentiality of the data throughout the read operation and to provide sufficient power for pass-NMOS transistors to transmit an adequate bit line voltage through the Bit-Line along with Bit-Line-Bar during the writing process, transistor dimensions are carefully chosen according to the cell ratio as well as pull-up ratio.

3.1.2 Static Noise Margin (SNM)

The static noise margin (SNM) measures how stable the SRAM is when subjected to noise interference[2-4]. Before Calculating the SNM for Circuit we have to do Sizing of the Transistor so that we can get proper SNM from the circuit. For that purpose we have to do Parametric Analysis on width of all the SRAM cell mosfet of the circuit. So that we can select an appropriate sizing for the circuit for all our operations and the circuit gives better stability and high noise margin. In our case we choose the sizing as referred to in Table II for the 6T SRAM and TABLE III for 8T SRAM Cell.

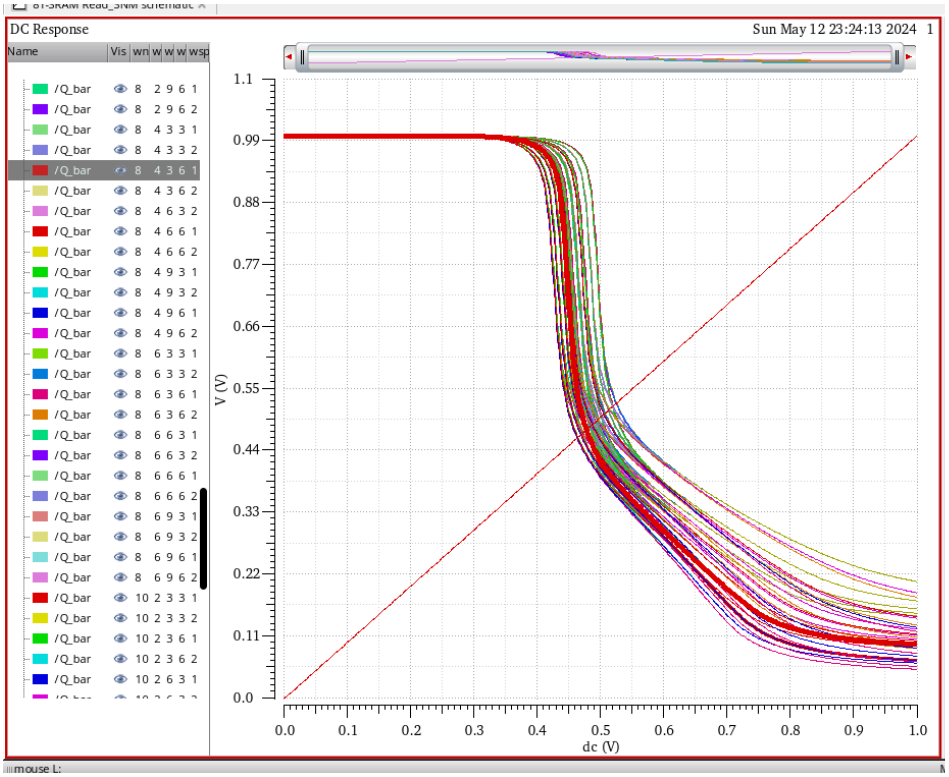


Fig. 4.3. Parametric Analysis on 8T SRAM

After doing Parametric Analysis we got the result like figure 3 in which we got different curves for the Width of the transistors. As a result, we decided to take sizing like given below Tables (*we can change also according to our analysis*):

TABLE 4.2

SIZING OF 6T-SRAM

6T-SRAM					
M1	M2	M3	M4	M5	M6
w	6w	w	6w	3w	3w

TABLE 4.3

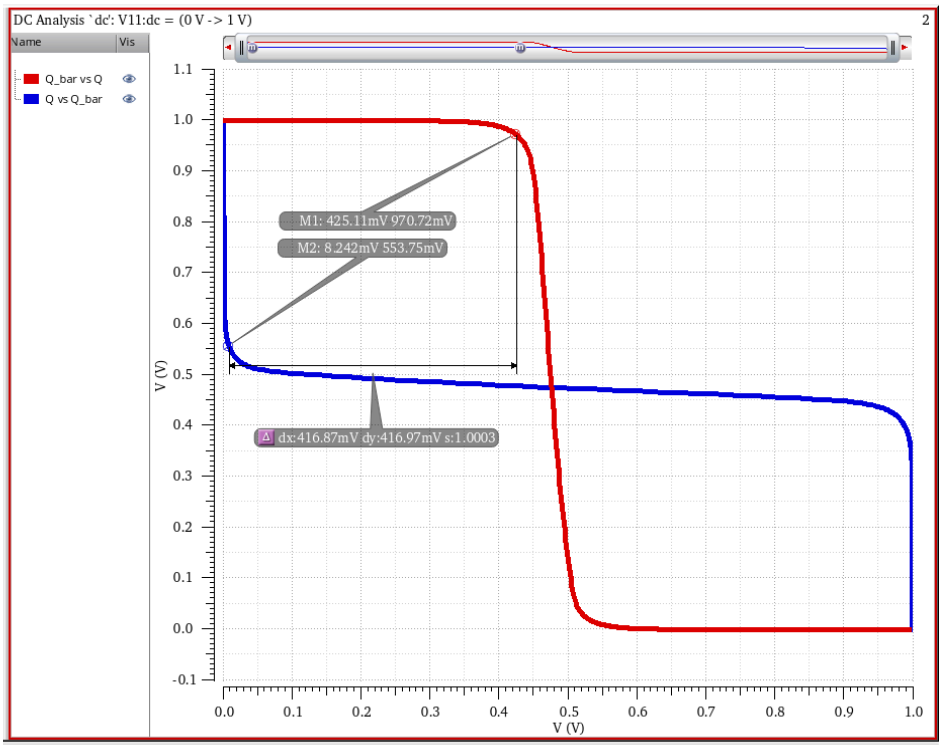
SIZING OF 8T-SRAM

8T-SRAM							
M1	**M2**	**M3**	**M4**	**M5**	**M6**	**M7**	**M8**
3w	w	6w	3w	w	6w	w	w

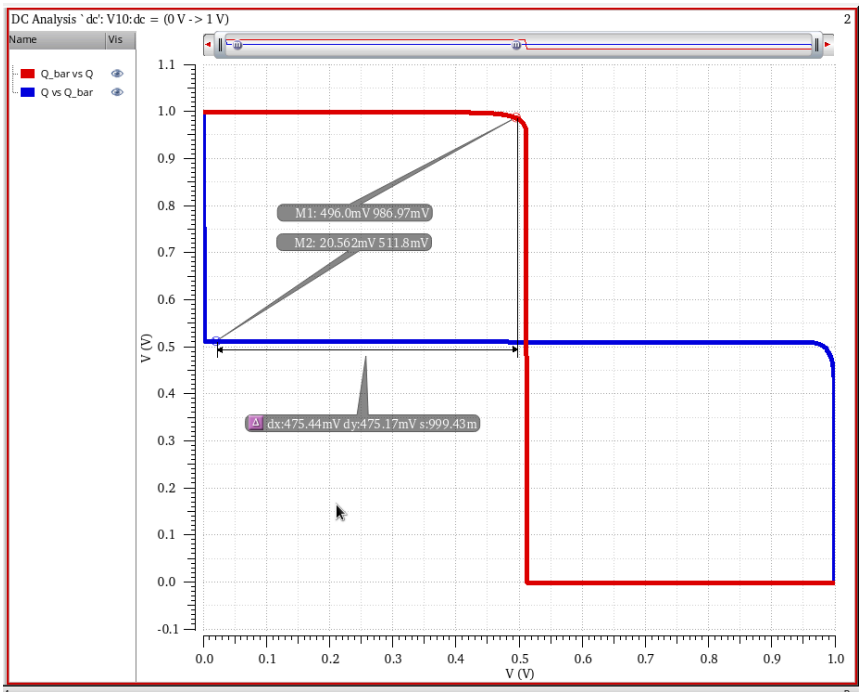
To calculate the Static Noise Margin (SNM) value, find the most significant square that falls between the two typical butterfly shapes of a static CMOS memory cell. Begin by displaying the voltage transfer characteristics (VTC) for both inverters.

The graphs depict the connection across the voltages at the input and output of each inverter. Locate the spots where the two VTC curves intersect. These intersection points are critical because they establish the bounds within which the square can fit. The key to establishing the SNM is to find the longest diagonal that fits completely between the two curves. This diagonal reflects the maximum disturbance voltage that the cell can withstand without changing state. Create a square with the length of this diagonal. This value is important since it measures the memory cell's resistance against noise.

When the cell is in a hold state. HSNM examines the stability of the SRAM cell which means no read or write operations are taking place and the cell is simply storing data. A high HSNM makes certain that the data kept within the SRAM cell is stable and is not susceptible to noise. Figures 4 (A) and (B), Refer Table V, depict HSNM Curves for 6T and 8T SRAM Cells. The HSNM increases by 12.42% when switching from a 6T to an 8T configuration. This indicates that the 8T SRAM cell has higher hold stability than the 6T cell, making it more resistant to noise when in the hold state.



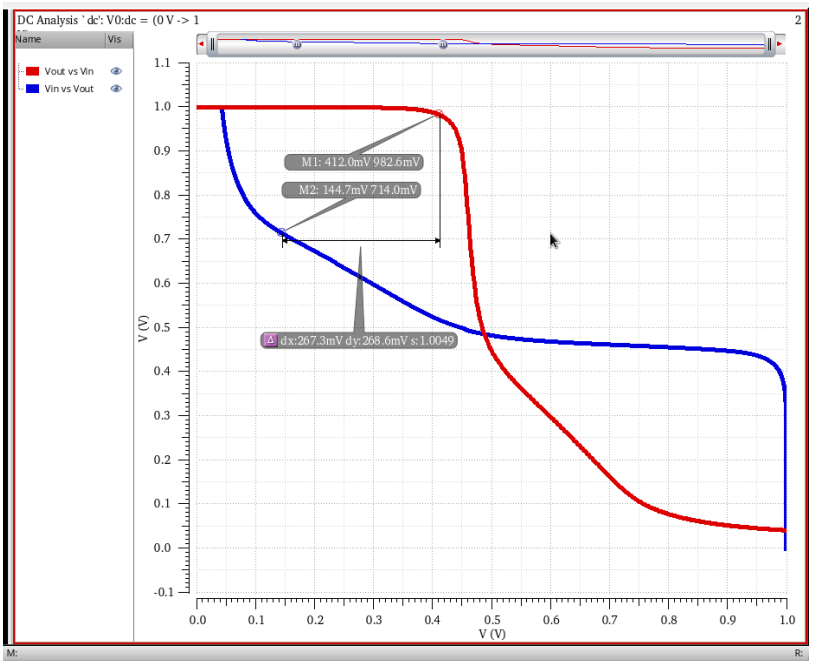
(A)



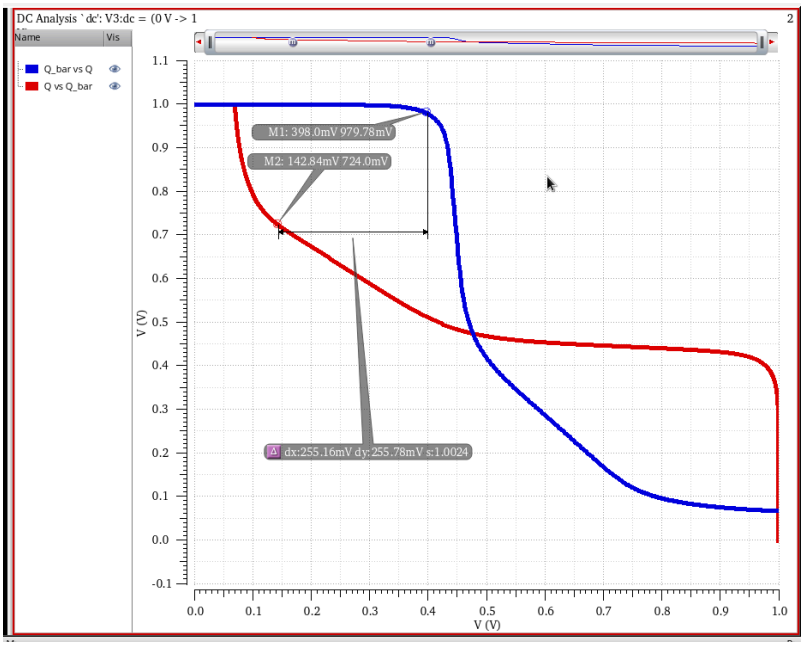
(B)

Fig. 4.4. HSNM Curve for 6T and 8T

RSNM determines how stable it is of an SRAM cell throughout the reading process. It indicates how well the cell retains its stored value when being read. High RSNM ensures that data can be read without affecting the stored value, which is critical for dependable operation.



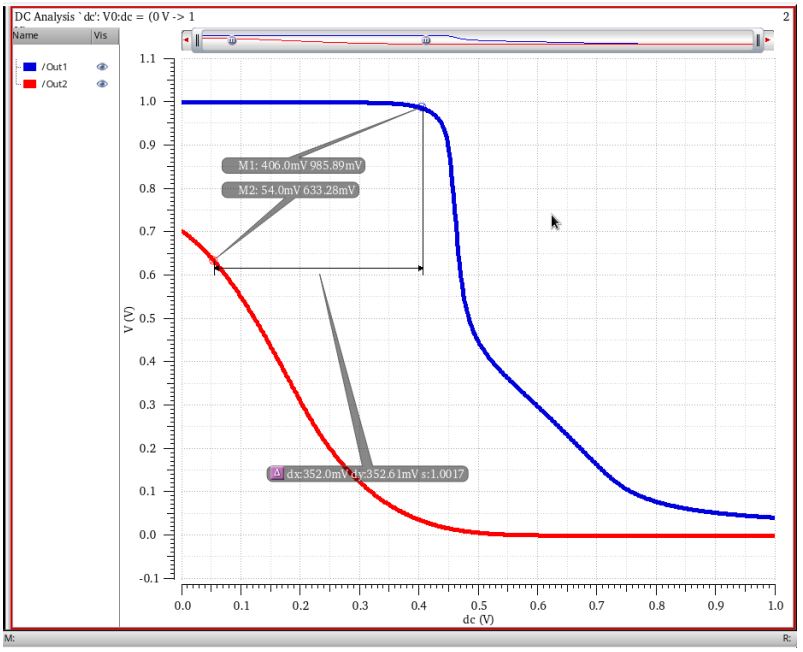
(A)



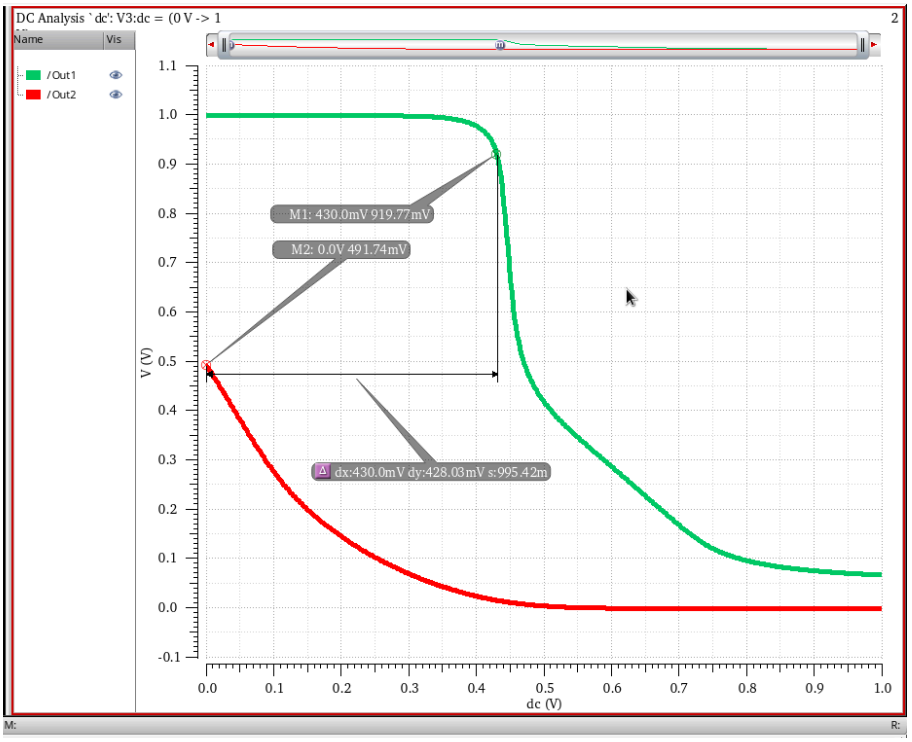
(B)

Fig. 4.5. RSNM Curve for 6T and 8T

Figures 5 (A) and (B), Refer Table V, depict HSNM Curves for 6T and 8T SRAM Cells. The RSNM decreases by 4.70% when switching from a 6T to an 8T configuration. This slight decrease implies that read stability is slightly compromised in the 8T cell compared to the 6T cell. It implies that the 8T cell is slightly more prone to errors during read operations.



(A)



(B)

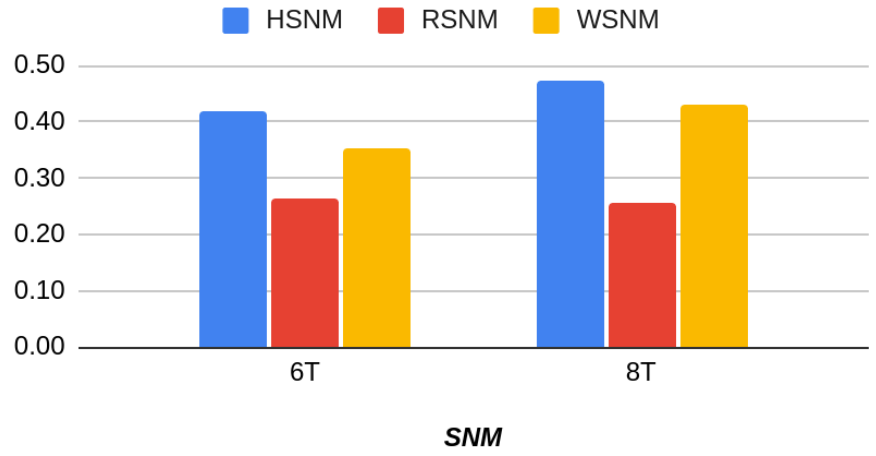
Fig. 4.6. WSNM Curve for 6T and 8T

WSNM determines the stability of a memory cell with SRAM during the writing process. It shows the ease with which new data can be entered into the cell. High WSNM ensures that the cell can be consistently overwritten with new data, which is required for proper operation. Figures 6 (A) and (B), Refer Table V, depict HSNM Curves for 6T and 8T SRAM Cells. The WSNM increases by 18.13% in the 8T configuration over the 6T configuration. This significant increase indicates that the 8T SRAM cell has much better write stability, making it easier to add new data to the cell.

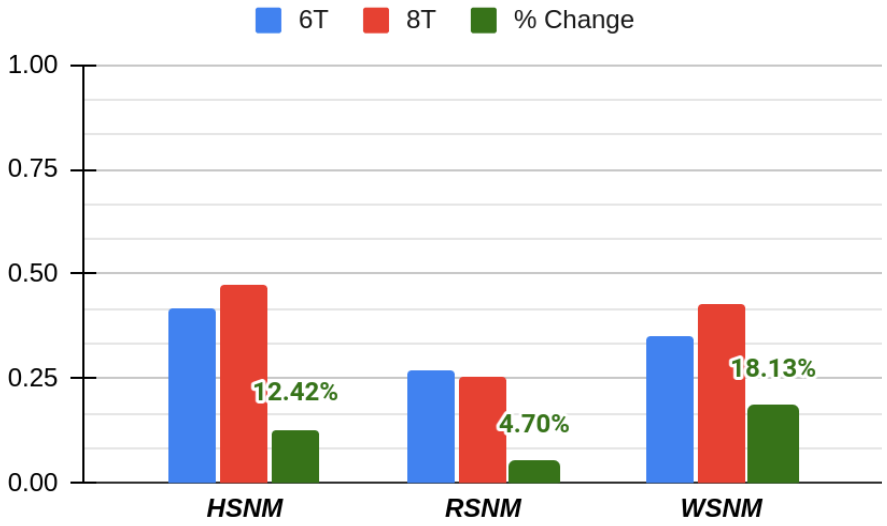
TABLE 4.4

SNM FOR 6T AND 8T

SNM	6T	8T	% Change
HSNM	0.416	0.475	12.42%
RSNM	0.267	0.255	-4.70%
WSNM	0.352	0.43	18.13%



(A)



(B)

Fig. 4.7. Comparison Column chart of SNM 6T/8T

These changes indicate that, while the 8T configuration provides significant benefits in hold and write operations, the trade-off is a slight reduction in read stability. Design choices between 6T and 8T configurations would thus be determined by the SRAM application's specific requirements and priorities.

3.1.3 Transient Analysis

Figure 8 displays the configuration used to test an individual SRAM cell. In this setup, a big capacitor is connected to BL as well as BLB to denote the transistors. This capacitor simulates the load and parasitic capacitance of the transistors in the SRAM cell. During the write procedure, imposing voltage sources are linked to the bit lines,

driving the voltages required to write data in SRAM cell. These sources of voltage guarantee that the proper levels of voltage are delivered while storing the intended bit inside the SRAM cell [1].

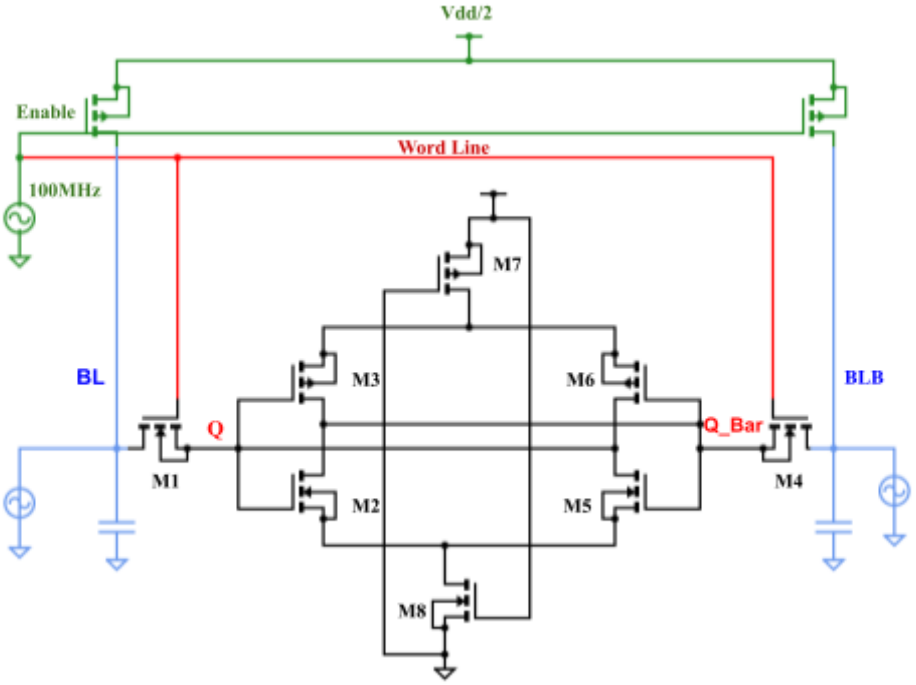


Fig. 4.8. Proposed 8T SRAM Testbench for transient analysis

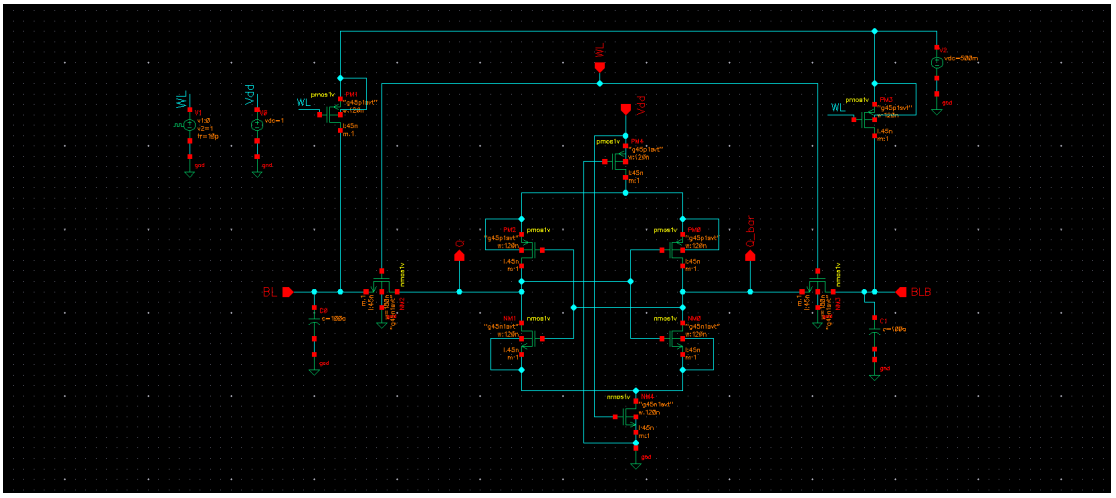


Fig. 4.9. Schematic for transient analysis

A 100 MHz supply powers both the updating PMOS transistors as well as the word line (WL). Once the WL is high, it enables the pass NMOS transistors, which connect the bit lines with the SRAM cell either read or write operations. Throughout the second part of the period, while the WL is low, the SRAM cell is separated from the bit lines. For this phase of operation, the bit lines get pre charged to fifty percent of the

source voltage (VDD). Precharging the bit lines with this intermediate voltage setting improves the efficiency of the writing and reading processes by minimising the voltage fluctuation required for both operations, resulting in faster transitions and lower power usage.

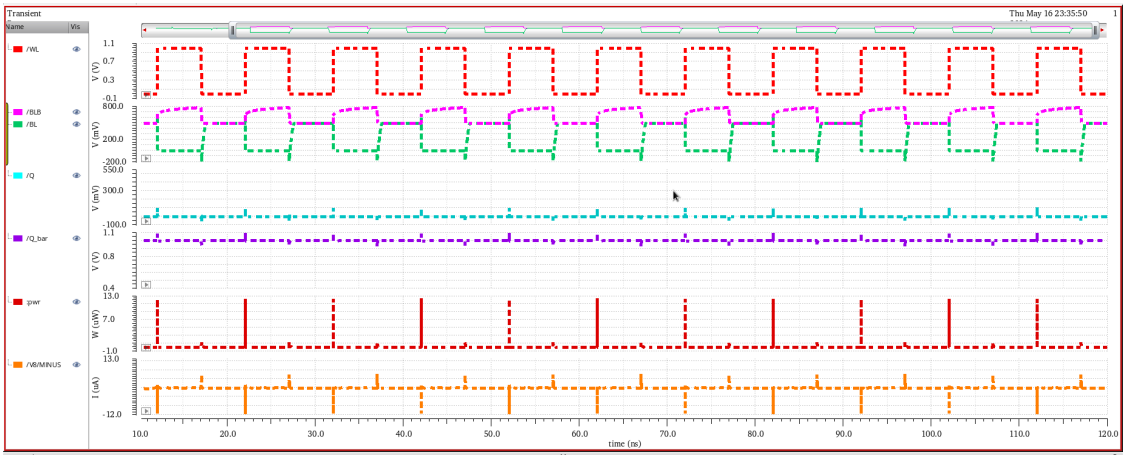


Fig. 4.10. Waveform for Read Operation

The waveforms in Figures 10 and 11 show that the values change only if the word line (WL) signal is high. This phenomenon arises because the WL signal regulates the passing transistors (usually NMOS) that connect the SRAM cell to the bit lines.

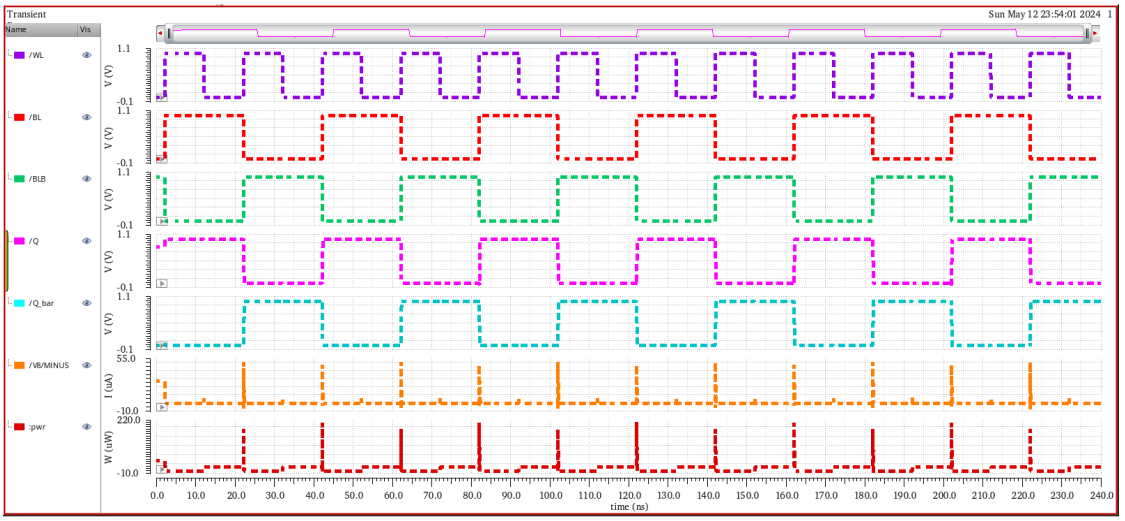


Fig. 4.11. Waveform for Write Operation

When the WL signal is low, the transistors turn off, isolating the cell away from bit lines and inhibiting data flow. When the WL signal is high, it activates the pass transistors, allowing the SRAM cell to interface with the bit lines for read and write operations. Therefore, changes in the data values across the bit lines are noticed only when the WL signal is strong. Because the pass transistor operates as an NMOS device transmitting a weak 1, the BL, which ascends throughout the read operation, only

reaches roughly 0.7 V rather than Vdd. The stored 1 falls short of Vdd during the write operation because of the back-to-back inverters' weak pull-up PMOS transistor.

For write operations, the WL is set to a high value, and data is sent to BL and BLB in opposite directions to ensure proper writing. When BL = 1, the access transistor will begin charging Node Q. Once the charge reaches the inverter switching threshold, it will attempt to maintain 1V at the Q node and 0V at the Q_bar node. Figure 10 shows that the Read Delay for the 8T configuration is 48.01 psec, which is significantly higher than the 16.3 psec for the 6T configuration. The significant increase in read delay for the 8T configuration implies that adding transistors to the SRAM cell to improve noise margins and stability introduces extra capacitance and resistance. These parasitic elements slow down the read operation, resulting in a much longer read time. As a result, while the 8T configuration increases noise margins, it reduces read speed. The write 1 delay in fig. 11 for the 8T configuration is 43.8psec, which is greater than the 32.6 psec for the 6T configuration. The write 0 delay for the 8T configuration is 26.3psec, which is slightly less than the 26.8psec for the 6T configuration. The 34.36% increase in write 1 delay in the 8T configuration is due to the additional circuitry required to improve write stability. The 1.87% decrease in write 0 delay for the 8T configuration indicates that the additional transistors have a minimal impact on the time required to write a '0'.

The 8T configuration improves noise margins and stability, which is especially useful in noisy environments or applications that require reliable data retention. However, these advantages come at the expense of longer read and write delays, necessitating careful consideration of the application's performance requirements.

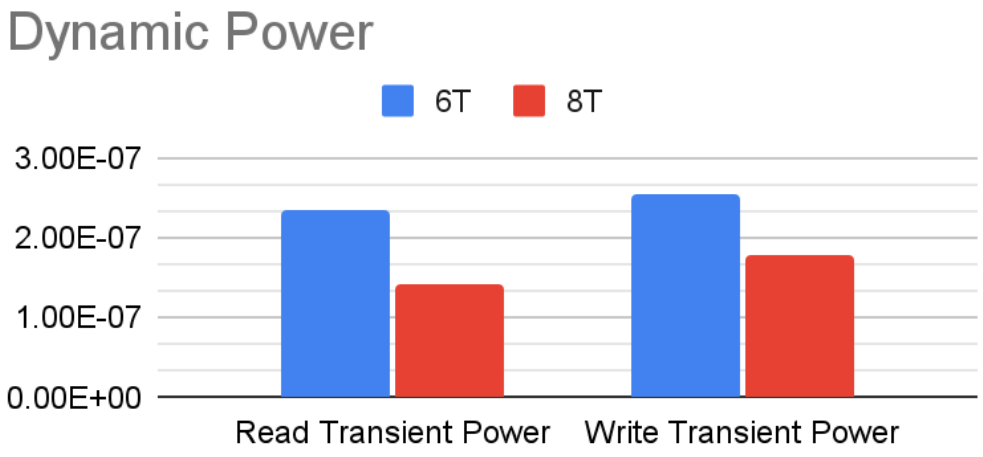


Fig. 4.12. Column Chart for Read/Write Transient Power

Figure 12, Refer Table VI, The 40.43% reduction in read transient power for the 8T configuration indicates a significant increase in dynamic power efficiency during read operations. This efficiency is most likely due to reduced switching activity and lower capacitive load per read operation caused by the additional transistors, which stabilise the cell and reduce power spikes.

Figure 12, Refer Table VI, The 30.20% decrease in write transient power suggests that the dynamic power consumed during write operations is significantly lower in the 8T configuration. This reduction could be attributed to more efficient charge distribution and faster stabilisation of cell voltages during write cycles, as the additional transistors provide better control and reduce power-intensive glitches.

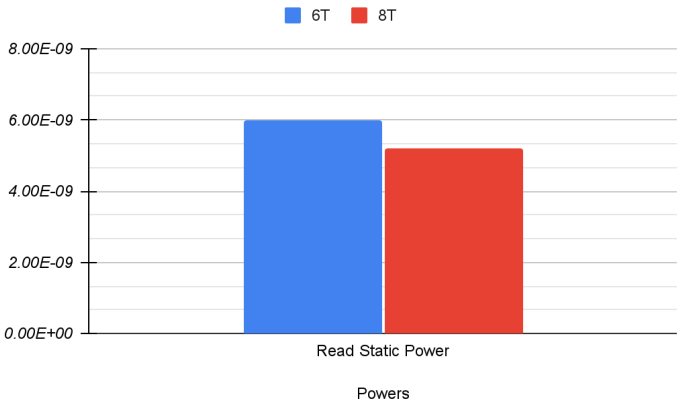


Fig. 4.13. Column Chart for Read Static Power

Figure 13, Refer Table VI, The 8T SRAM arrangement consumes roughly 13.17% less read static power than the 6T configuration. This suggests that the 8T architecture is more power efficient during idle times when the SRAM is in read mode.

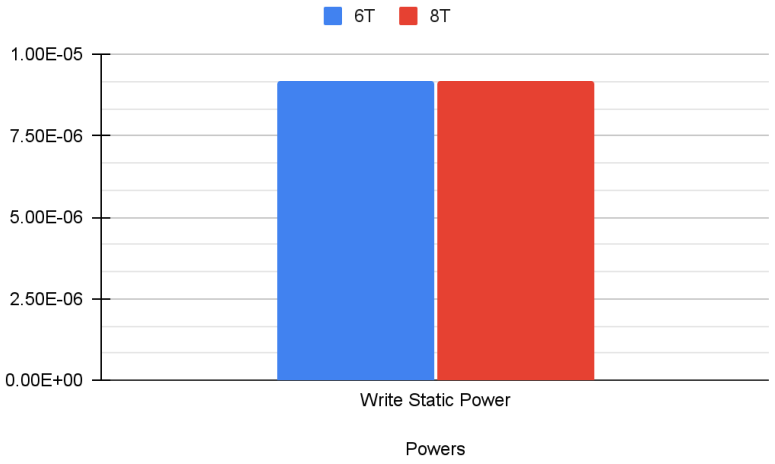


Fig. 4.14. Column Chart for Write Static Power

Figure 14, Refer Table VI, The write static power consumption is quite comparable for both setups, with the 8T option having a somewhat higher consumption of about 0.11%. This minor variation shows that, in terms of write static power, both configurations perform almost identically.

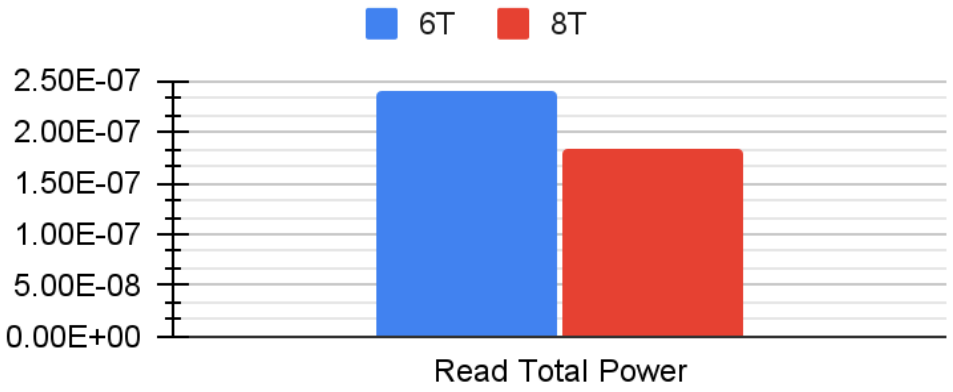


Fig. 4.15. Column Chart for Total Read Power

Figure 15, Refer Table VI, The 24.06% reduction in read total power for the 8T arrangement indicates that, despite the more transistors, the overall energy required for read operations is less. This reduction can be attributed to more efficient read operation due to improved noise margins, resulting in fewer erroneous reads and retries, and therefore conserving power.

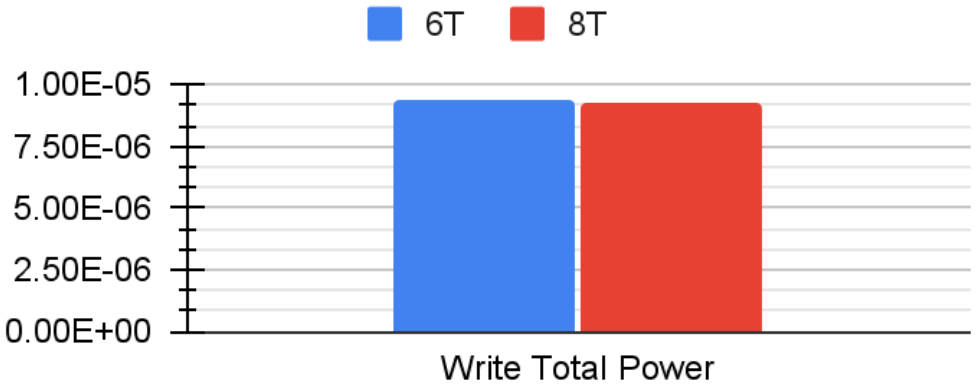


Fig. 4.16. Column Chart for Total Write Power

Figure 16, Refer Table VI, The minor decrease of 1.06% in write total power suggests that the additional transistors in the 8T arrangement do not considerably increase power consumption during write operations. The optimisation of the write path

or lower leakage current in the 8T configuration may contribute to this marginal reduction.

TABLE 4.5

POWER CONSUME IN READ/WRITE

Powers Consume	**6T**	**8T**
Read Transient Power	2.35E-07	1.40E-07
Write Transient Power	2.55E-07	1.78E-07
Read Total Power	2.41E-07	1.83E-07
Write Total Power	9.41E-06	9.31E-06
Read Static Power	6.00E-09	5.21E-09
Write Static Power	9.16E-06	9.17E-06

Overall, the 8T SRAM architecture has a significant benefit in terms of power consumption, making it an excellent choice for power-sensitive applications, as long as the trade-offs in read and write delay are acceptable in the context of the application.

CHAPTER 05 PARAMETRIC ANALYSIS

5.1 Parametric Analysis

Here we analyse the delay and powers for the different Vdd voltages.

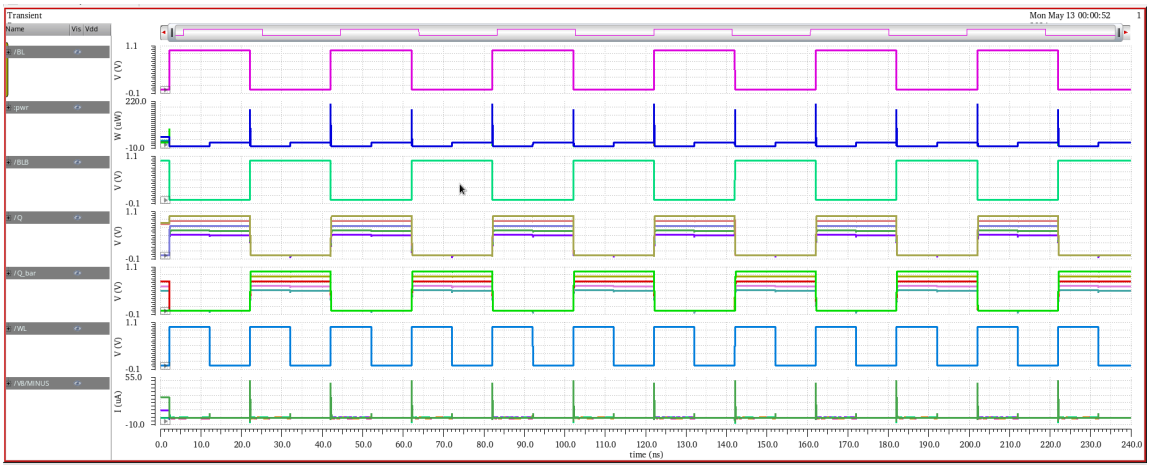


Fig. 5.1. Vdd Parametric Analysis Waveforms

5.1.1 Read Delay vs Vdd

Understanding how SRAM cells' read delay varies with supply voltage (Vdd) is critical for improving memory performance under a variety of operating conditions.

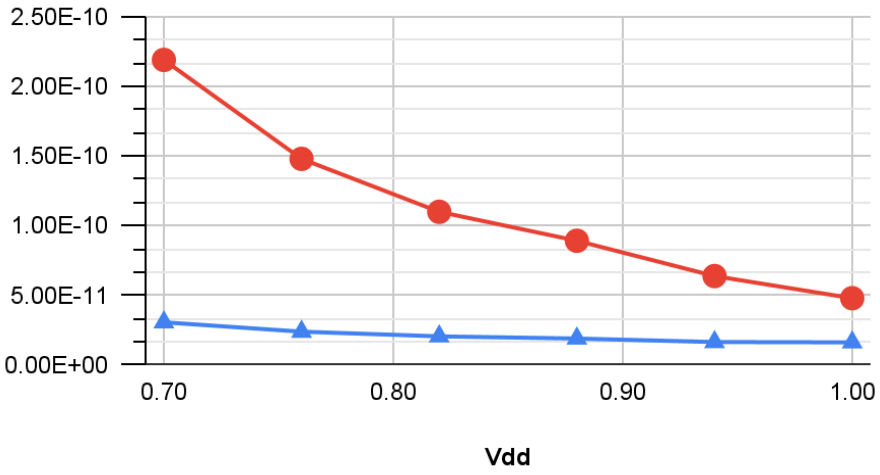


Fig. 5.2 Line Chart for Read Delay of 6T and 8T SRAM

Figure 18, The read latency in both 6T and 8T systems diminishes as the supply voltage (Vdd) increases. The 8T setup consistently has greater read latency than the 6T configuration at each Vdd level.Both 6T and 8T SRAM setups show decreasing read

latency as Vdd increases. This trend is due to increased supply voltage, which improves transistor driving strength and reduces the time necessary to read data from the cell. The 8T arrangement consistently exhibits a larger read delay than the 6T variant at all voltage settings. This is most likely due to the additional transistors in the 8T design, which provide more capacitance and resistance, slowing down the read process.

5.1.2. Write Delay vs Vdd

Figure 19, Both 6T and 8T SRAM configurations show a general trend of reducing write 1 latency as Vdd increases. A higher supply voltage increases the driving strength of the transistors, which speeds up the write operation. The percentage increase in write one delay from 6T to 8T reduces as Vdd grows. At Vdd = 0.70V, the write 1 latency for the 8T design is approximately 61.00% greater than that of the 6T configuration, while at Vdd = 1.00V, it is roughly 34.36% greater. The 8T configuration consistently has greater write 1 delays than the 6T version at all voltage levels. This is most likely due to the extra capacitance and resistance of the additional transistors in the 8T design, which slows down the write operation.

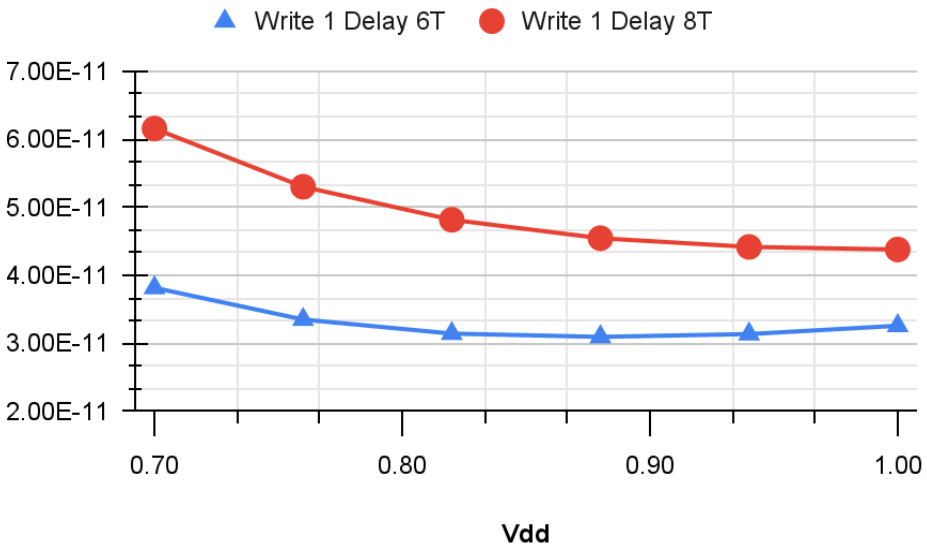


Fig. 5.3. Line Chart for Write 1 Delay vs Vdd

In figure 20, Both 6T and 8T SRAM designs exhibit an increasing trend in write 0 delay as Vdd rises. This could be due to the higher voltage creating more resistance in the write path. At lower voltages, the 8T arrangement has a significantly longer write 0 delay than the 6T version; however, at higher voltages, the delays are almost identical or even slightly lower for the 8T. The percentage increase in write 0 latency from 6T to 8T

is modest at lower Vdd values, showing comparable performance. At Vdd = 1.00V, the write 0 latency for the 8T configuration is somewhat lower than that of the 6T configuration, indicating a point of crossover where the 8T design's performance can equal or exceed that of the 6T configuration at higher voltages.

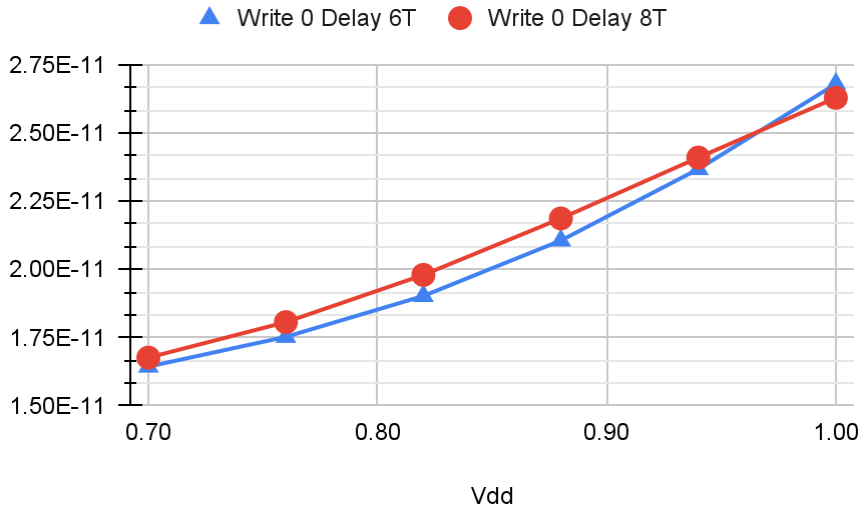


Fig. 5.4. Line Chart for Write 0 Delay vs Vdd

5.1.3 Read Power vs Vdd

Figure 21, Both setups (6T and 8T) show an increase in transient read power as Vdd increases, demonstrating that higher supply voltages result in larger power consumption. The 8T arrangement provides higher transient read power at lower voltages (up to about 0.82V), but this trend flips at higher voltages, when the 6T configuration consumes more power.

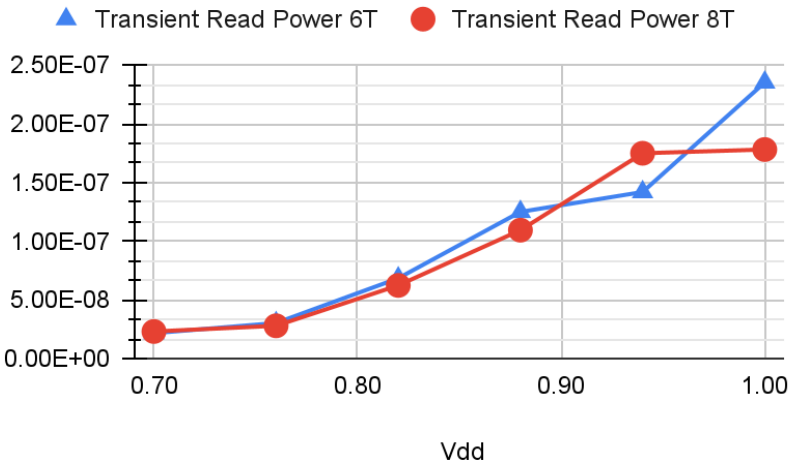


Fig. 5.5. Line Chart for Transient Read Power vs Vdd

At lower Vdd levels (0.70V to 0.82V), the 8T arrangement produces more transient read power than the 6T variant. However, as Vdd rises above this threshold, the 6T design's power consumption exceeds that of the 8T configuration. The reversal point occurs around Vdd = 0.88V, when the power consumption of both topologies begins to differ, with 6T consuming much more power at higher voltages.

In figure 22, At lower Vdd levels (0.70V and 0.76V), the 8T arrangement has a lower static read power than the 6T configuration, showing improved power efficiency. At Vdd levels of 0.82V, 0.88V, and 0.94V, both configurations have negative static read power values that are non-physical. This might be the result of measurement mistakes, simulation flaws, or improper data capture. This oddity requires more examination. At a nominal Vdd of 1.00V, the 8T arrangement has a 13.17% lower static read power than the 6T configuration, indicating higher power efficiency.

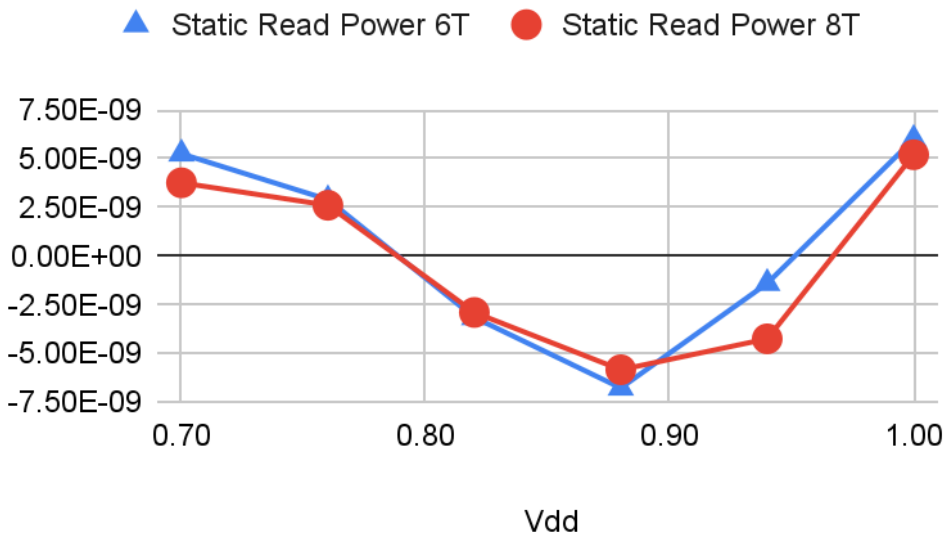


Fig. 5.6. Line Chart for Static Read Power vs Vdd

Figure 5.7 shows that both systems (6T and 8T) increase total read power when Vdd increases, suggesting that higher supply voltages result in increased power consumption. The 6T arrangement has somewhat more overall read power at lower voltages, but as Vdd grows, the 8T configuration outperforms the 6T at certain points. At lower Vdd levels (0.70V to 0.88V), the 6T arrangement often uses more total read power than the 8T setup.

Fig. 5.7. Line Chart for Total Read Power vs Vdd

However, this tendency flips when Vdd = 0.94V, when the 8T arrangement begins to consume more power. The crossover point represents a voltage level at which the 8T setup's efficiency is reduced when compared to the 6T configuration.

5.1.4 Write Power vs Vdd

Figure 24, shows that both 6T and 8T SRAM architectures have an increase in transient write power as Vdd increases, indicating increased power consumption at higher supply voltage levels. Across all voltage levels, the 6T arrangement consistently produces more transient write power than the 8T configuration does. At each Vdd level, the 8T arrangement produces less transient write power than the 6T configuration. The 8T arrangement has a significant drop in transient write power when compared to the 6T configuration, especially at higher Vdd levels, showing superior power efficiency during write operations. The percentage reduction in transient write power for the 8T arrangement compared to the 6T configuration spans between 2.60% and 45.10%, with bigger reductions found at higher Vdd levels.

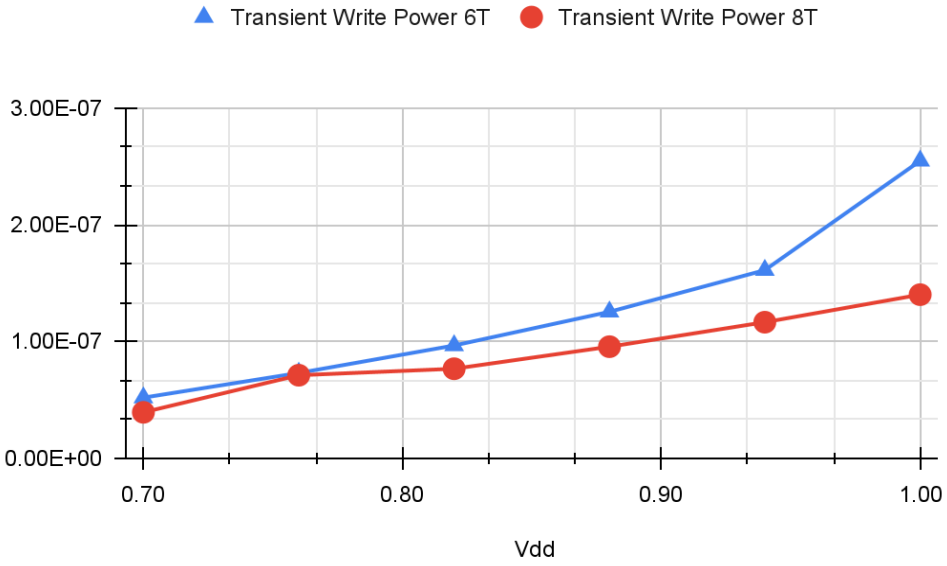


Fig. 5.8. Line Chart for Transient Write Power vs Vdd

Figure 25, The static write power consumption for both 6T and 8T SRAM configurations is very close across all tested Vdd levels, with the 8T configuration consistently consuming slightly more power by approximately 0.11%.

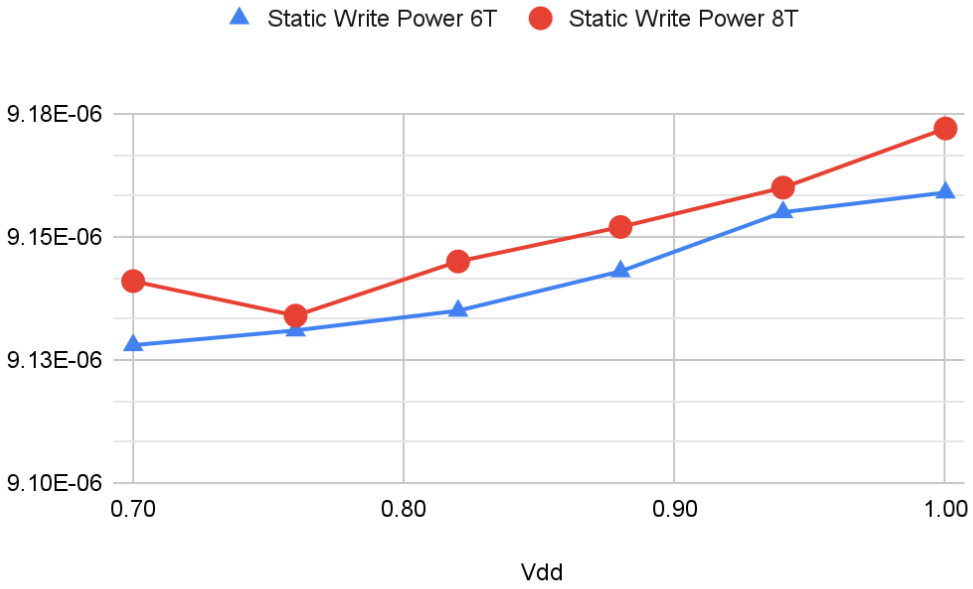


Fig. 5.9. Line Chart for Static Write Power vs Vdd

In Figure 26, both the 6T and 8T SRAM setups show a modest rise in total write power as Vdd increases, demonstrating a general trend of increased power consumption with higher supply voltages. The changes in total write power between the 6T and 8T

systems are modest, however the 8T design consumes somewhat less power at higher Vdd levels. At each Vdd level, the 8T arrangement equals or slightly underperforms the 6T configuration in terms of overall write power consumption.

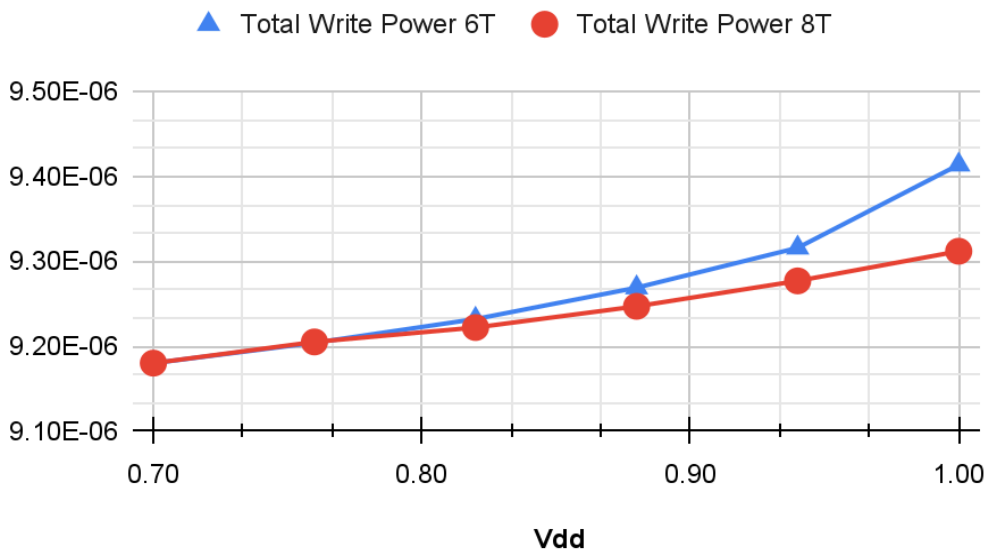


Fig. 5.10. Line Chart for Total Write Power vs Vdd

The percentage changes in total write power between the setups are minor, demonstrating comparable performance with slight efficiency advantages for the 8T arrangement at higher Vdd values.

In conclusion, the 8T SRAM design exhibits improved power efficiency during write operations across the studied voltage range, making it a better choice for applications where decreasing power consumption is a top priority. The 6T version, while having higher transient write power, may nevertheless be considered in cases where other performance aspects take precedence over power efficiency. The overall write power consumption of the 6T and 8T SRAM layouts is similar across the measured voltage range, with the 8T configuration providing small efficiency increases at higher voltages. This similarity makes both configurations Suitable for a variety of applications, with the decision potentially influenced by additional performance considerations or unique power efficiency requirements.

CHAPTER 06 SYSTEM OVERVIEW

6.1 System Overview

There are eight rows in the SRAM array, and each row has eight 8T-SRAM cells. One bit read-only or write-only bit of data is represented by one SRAM cell. Two bit lines that complement one another are used to access each bit, or single SRAM cell.

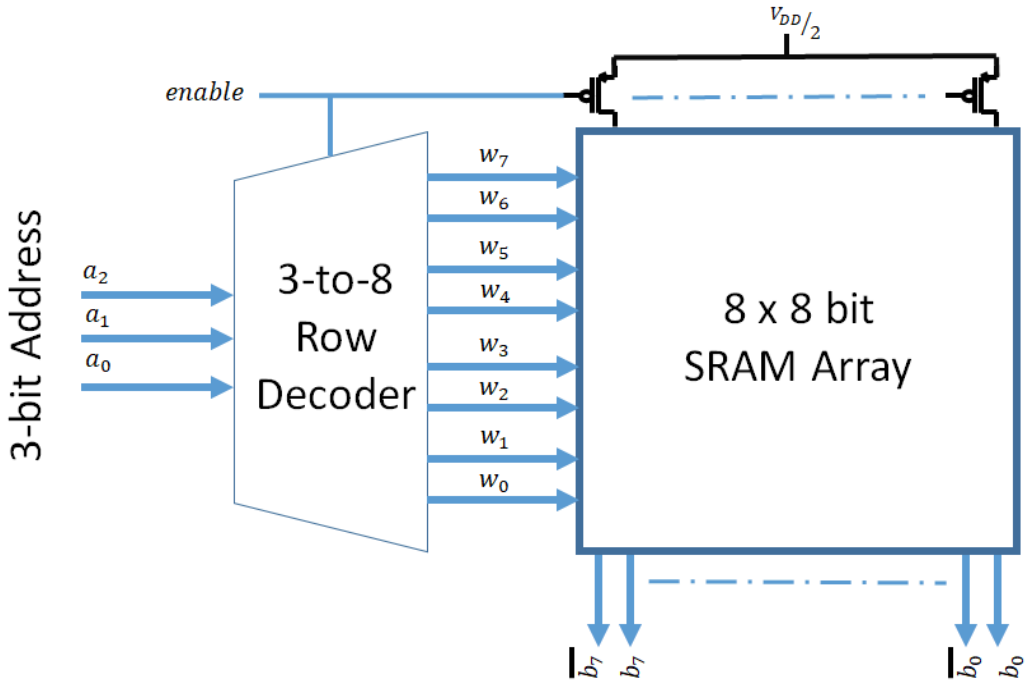


Fig. 6.1. SRAM Array & Decoder block diagram

A 3-to-8 CMOS decoder is used to activate a word line that accesses the SRAM rows [1-9]. The decoder accepts an enable signal and a 3-bit address indicating which word line should be active as inputs. The system runs at 100 MHz, with a refresh operation taking place in the second part of the cycle after the read or write information is acquired.

6.2 Row Decoder

The data stored in the SRAM array is accessible via word lines. Each WL represents the output of a 3-to-8 decoder[1]. This decoder accepts a three-bit location as input and selects which word line will activate. In addition, an enabling signal controls the decoder by turning it on during 1/2 of a 100 MHz cycle[1][2]. When the enable signal becomes active in the initial half of a period, the decoder picks the proper word

line depending on the 3-bit address, enabling read or write activities to be carried out on the relevant SRAM cells.

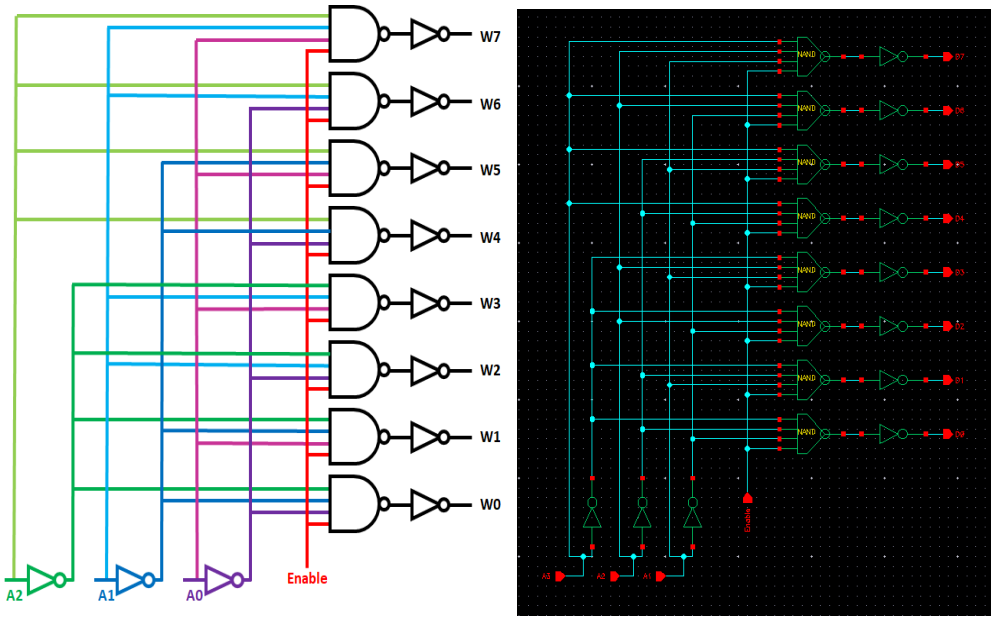


Fig. 6.2. 3-to-8 Decoder with enable circuit

The enable signal remains dormant during the second phase of the cycle, causing the decoder to switch off and essentially terminate the word lines. During this period, the BL are refreshed by precharging them to half of the supply voltage (Vdd/2), ready for the following cycle's operations. Figure 28 depicts the whole decoder circuit, including how the 3-bit address and enable signal interact to regulate access to SRAM cells via the word lines. Its architecture is based entirely on four-input NAND gates and static CMOS inverters. Four-input NAND gates are used since the address has three inputs and the enable signal has one.

The SRAM cell's inverter transistors are designed to produce balanced rise and fall timings. This indicates that the time it takes for the inverter's output to change from low to high (rise time) is roughly equal to the time it takes to change from high to low (fall time). This balance is critical for maintaining consistent performance and timing across the circuit. The NAND gate's transistors are sized differently. The aim is to guarantee that the NAND gate's worst-case latency equals that of the inverter. The worst-case delay for a NAND gate is often caused by numerous inputs switching at the same time, resulting in a greater propagation delay than simpler transitions. By carefully designing the transistors in the NAND gate, designers may guarantee that the delay does not surpass the inverter's delay. This matching of delays is critical for ensuring

synchronous operation and timing integrity inside the SRAM cell and the larger circuit in which it is embedded.

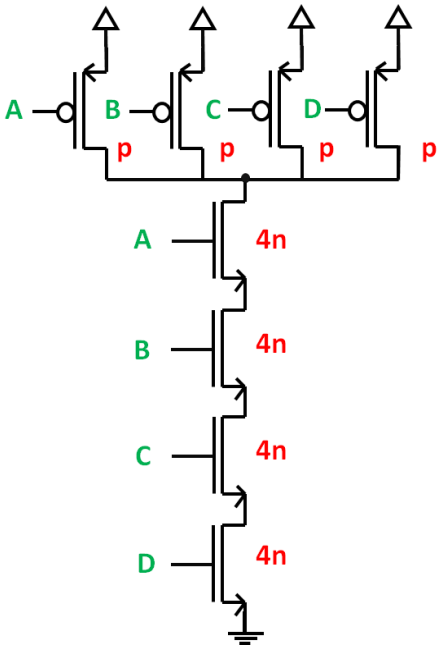


Fig. 6.3. Input static CMOS NAND gate

6.3. Transient Simulations

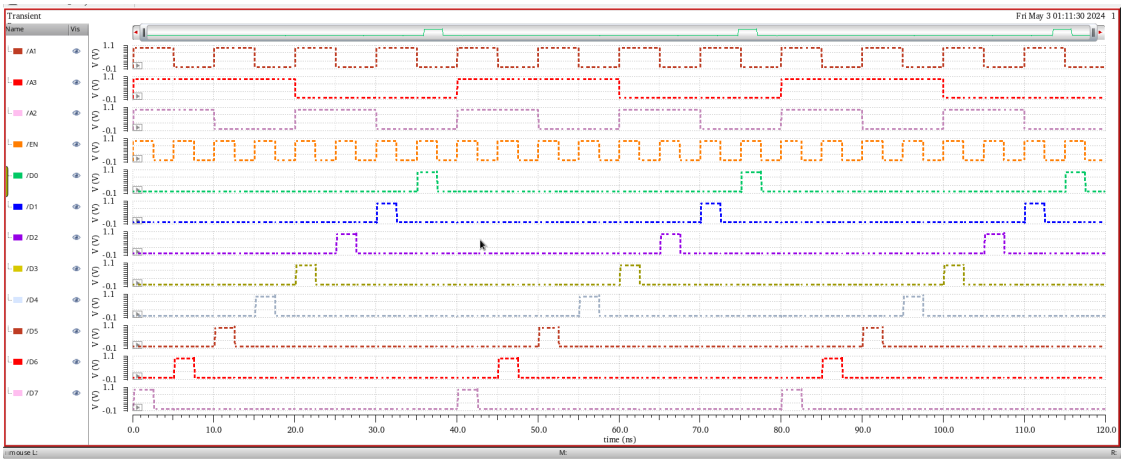


Fig. 6.4. Transient waveforms of the Decoder

Figure 30 shows the transient analysis of the decoder circuit over time. Each unique address combination supplied as input to the decoder has a corresponding single output that becomes high (logical 1) when the signal that enables it is strong. This signifies that the decoder properly converts the 3-bit address into one of the eight available word lines and activates just the chosen word line. The study additionally

accounts for the loading effects caused by the SRAM array's word lines. These loading effects might affect the timing and performance of the decoder output. The simulation incorporates these effects to offer a more accurate portrayal of the decoder's performance in a real-world setting in which the word lines contribute capacitance and resistance. This thorough analysis assures that the decoder can consistently choose the right word line and maintain accurate timing, even when linked to the actual SRAM array.

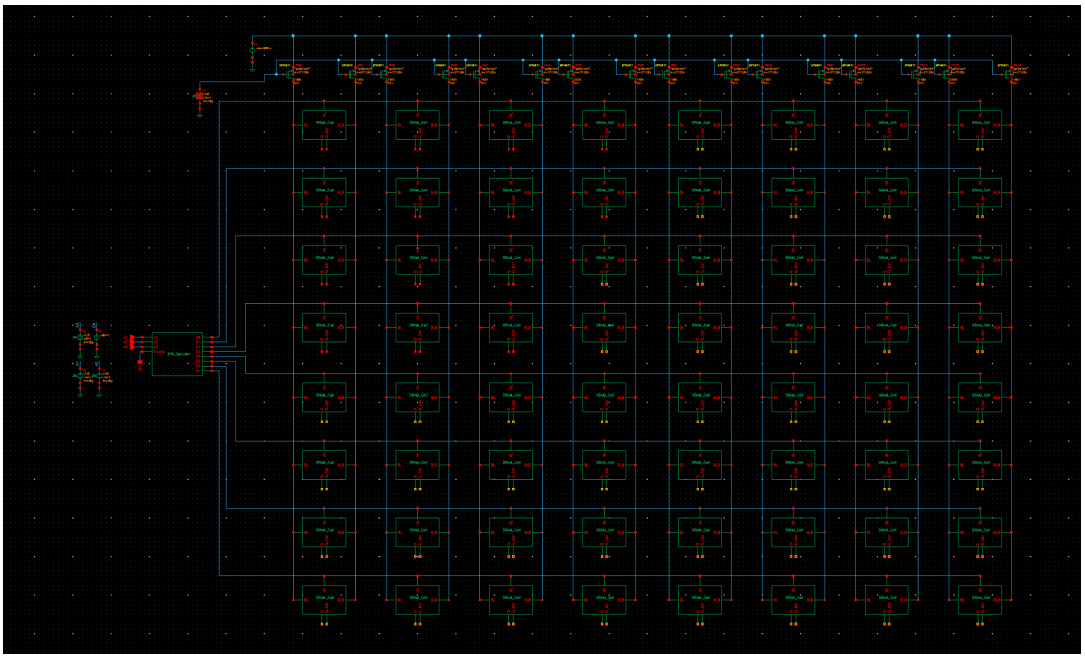


Fig. 6.5. 8x8 SRAM Array and Decoder Schematic

In Figure 31, we examine the entire system by conducting a read operation from the SRAM array. To begin the read operation, we set the enable signal (EN) to 1, activating the read process.

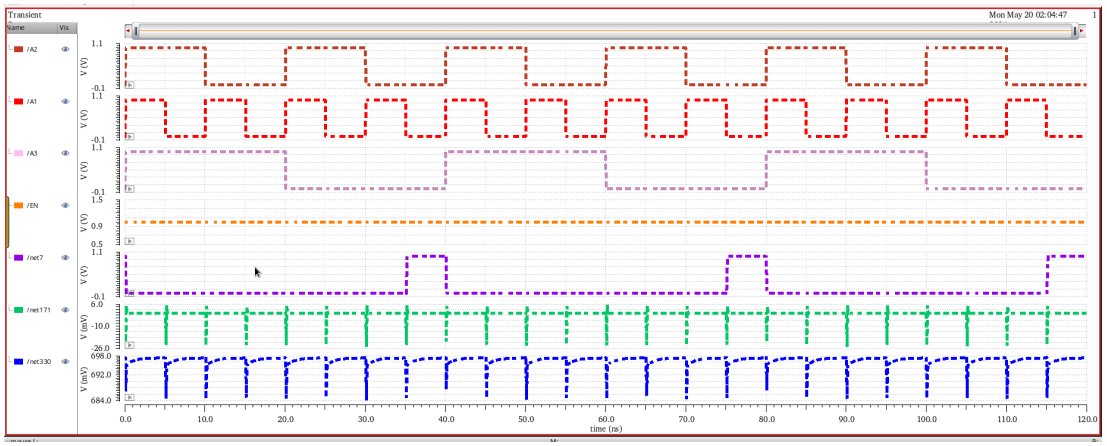


Fig. 6.6. 8x8 SRAM Operation Waveform

The data is read from the SRAM cell via the bit lines (BL and BLB). To ensure that the read operation works properly, we attach a 1V signal to Q_Bar in the SRAM cell. This arrangement simulates a known condition within the cell, with Q_Bar at a high voltage level (1V). During the read process, the bit lines are intended to accurately reflect the stored data. The results in Figure 32 demonstrate that BLB reads 1 (corresponding to the high voltage at Q_Bar) while BL reads 0. This implies that the read process is working well, since the bit lines precisely reflect the stored data. The research indicates that the system can successfully read data from the SRAM array under the specified conditions.

CHAPTER 07 LAYOUT

7.1 Layout

There is a hierarchical approach to the layout design process. Before the entire system is integrated, the layout of each block is created separately. Fig. 33 displays the configuration of a single 8T SRAM cell.

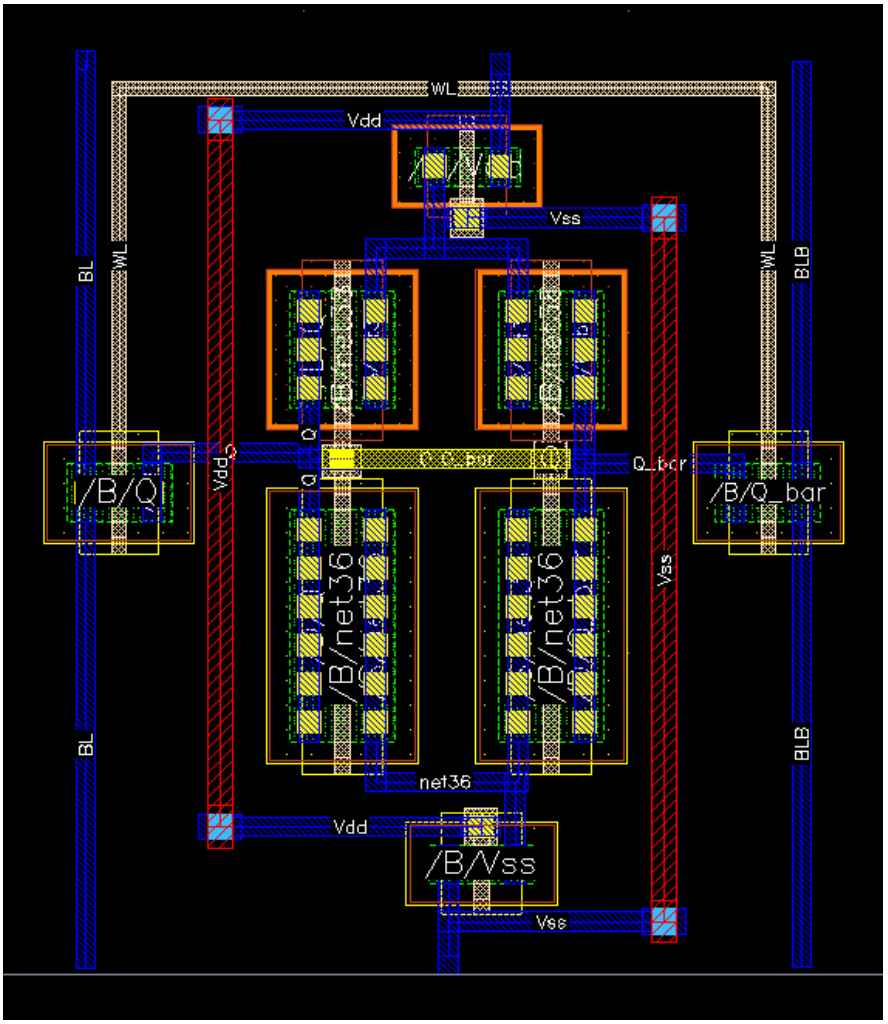


Fig. 7.1. Proposed SRAM Layout

The word lines (WL) and metal-1 lines are placed around the borders of the SRAM block to indicate the location of the bit lines. These bit lines transport data to and from SRAM cells during read/write operations. The power rails, which supply the voltages required by the SRAM cells, are positioned at both the top and bottom of each cell [1]. This precise positioning allows for quick and efficient connections with adjacent cells, ensuring that the entire array is well-powered and runs smoothly.

Polysilicon (PolySi) is used to link the gate terminals of the transistors in an SRAM cell. The material was chosen for its strong electrical characteristics and capacity to make dependable connections, both of which are required for the gates in transistors to work properly. By employing polysilicon for these connections, the design guarantees that the gate terminals are properly connected, allowing the SRAM cell to operate correctly.

To begin building the decoder, the inverter and NAND architectures are created (Figs. 34(a) and 34(b)). Figure 32 shows the finished decoder, which was built with great regard for space and power distribution. The power rails are located at the top and bottom of the gates, influencing the configuration of each row in the decoder.

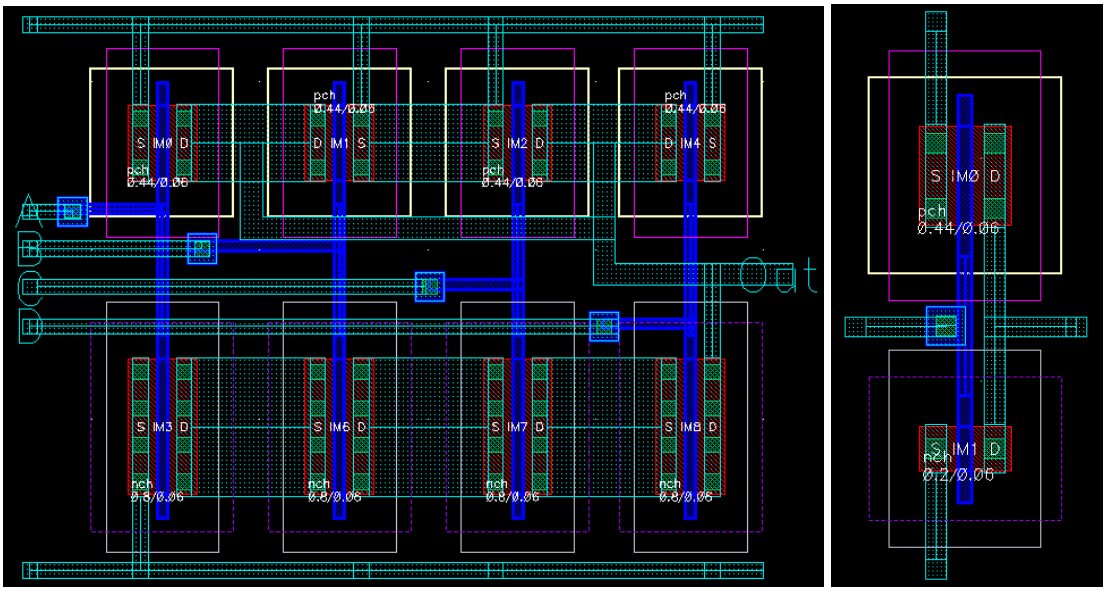


Fig. 7.2. Layout of the static CMOS NAND and Inverter

Each row in the decoder consists of two gates: a NAND gate and an inverter. To improve arrangement and save space, these rows are alternatively reversed vertically relative to the rows above and below them. This implies that if one row has the NAND gate on top and the inverter below, the following row will have the inverter on top and the NAND gate below. This alternating vertical flip makes effective use of common ground rails and VDD (supply voltage) rails. By sharing these power rails, the design decreases the amount of space required for extra wiring and hence the total footprint of the decoder [1]. This layout method keeps the decoder small and effectively organised, making it easier to incorporate into bigger circuits or systems.

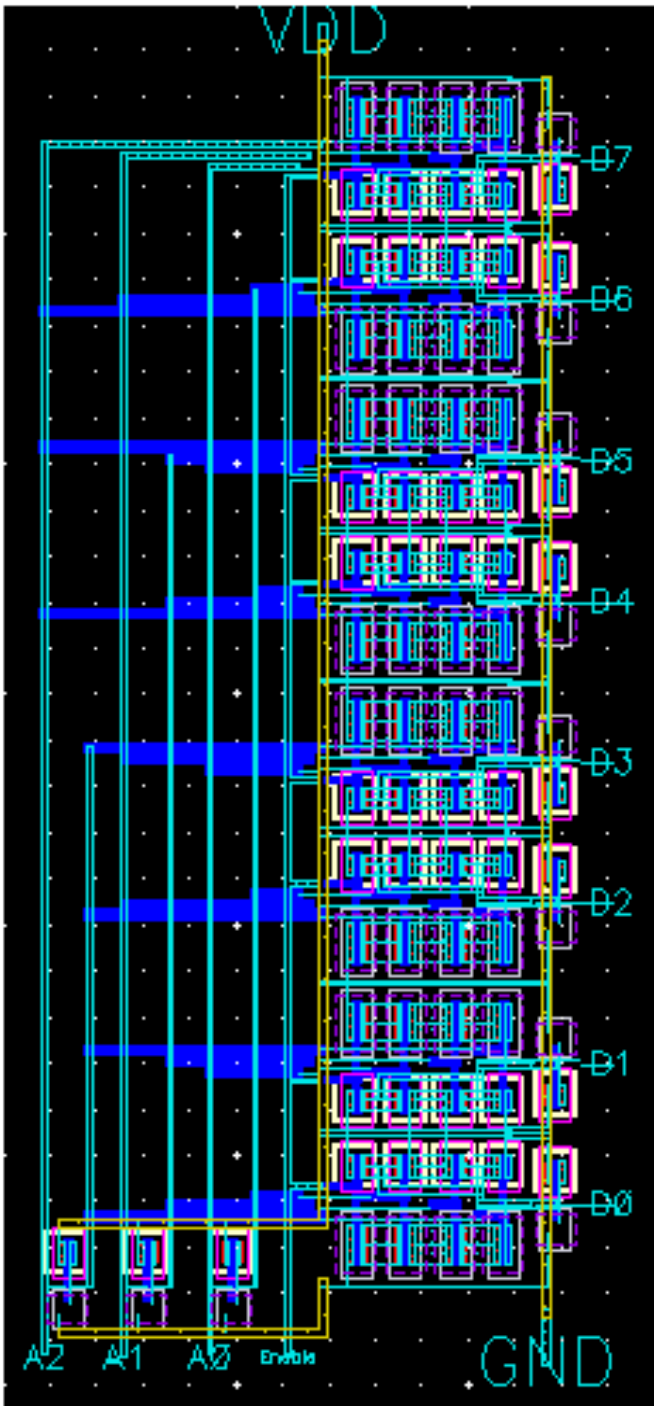


Fig. 7.3. Decoder Layout

Figure 36 depicts the complete layout of the SRAM array system. Similarly to the decoder configuration, each SRAM row rotates vertically to share a ground rail or Vdd rail with adjacent rows above and below. Metal-1 connects the system's bit lines; metal-2 operates each row's WL and metal-3 joins the power rails.

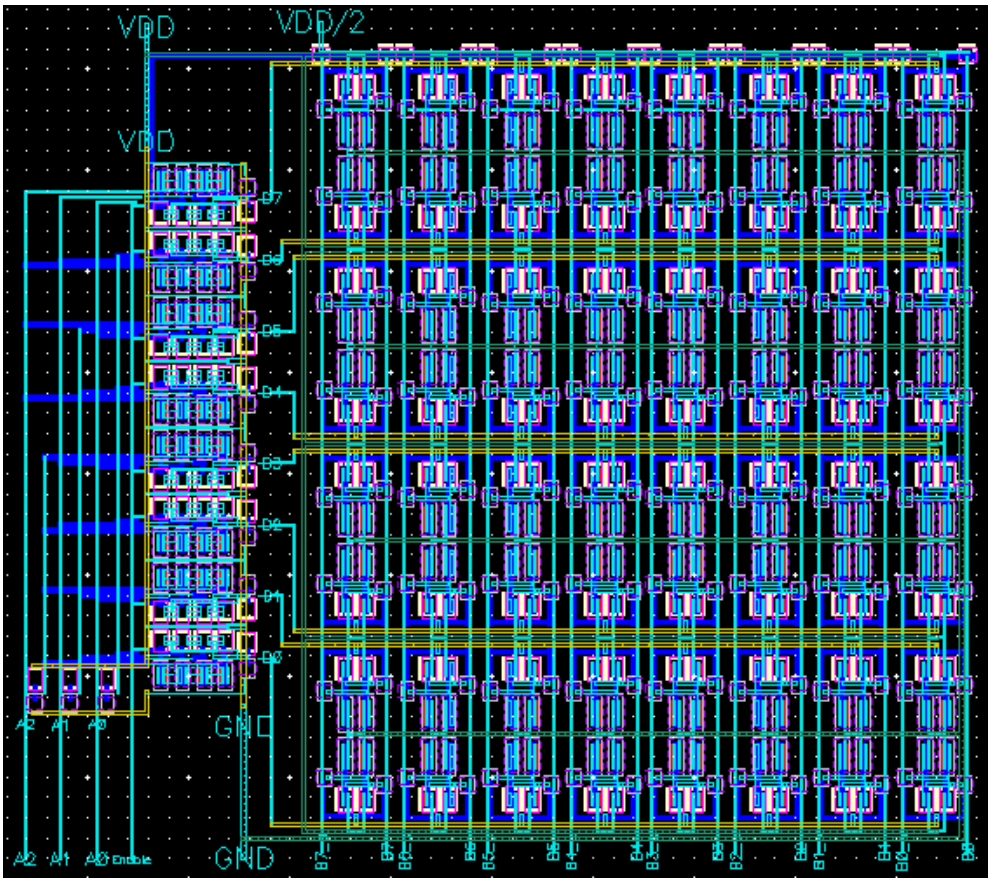


Fig. 7.4. Whole System Layout

CHAPTER 07 CONCLUSION & RESULT

7.1 Final Result and Conclusion

The SRAM array system is built with TSMC 45nm CMOS chip technology and runs on a 1 V supply of power [1]. Table V shows the most significant system parameters that resulted from this design technique. Both operations of reading and writing are performed at a frequency of 100 MHz. The 8T SRAM cell architecture in this design performs exceptionally well during write operations, especially at high Vdd levels. This characteristic makes it ideal for applications that prioritise power consumption.

TABLE 7.1

SYSTEM PARAMETERS FOR 6T AND 8T

Final System Parameter		**6T SRAM**	**8T SRAM**
Technology Node		45nm	45nm
Voltage (Vdd)		1V	1V
Frequency (f)		100MHz	100MHz
Read Power	Total	241n Watt	183n Watt
	Dynamic	235n Watt	178n Watt
	Static	6n Watt	5.21n Watt
Write Power	Total	9.41u Watt	9.31u Watt
	Dynamic	255n Watt	140n Watt
	Static	9.16u watt	9.17u Watt
Delay	Read	16.3p Sec	48p Sec
	Write 0	26.8p Sec	26.3p Sec
	Write 1	32.6p Sec	43.8p
Static Noise Margin	HSNM	0.416 V	0.475 V
	RSNM	0.267 V	0.255 V
	WSNM	0.352 V	0.430 V

REFERENCES

[1] Snehith, N., Kumar, E. S., & Rao, K. S. (2023, April). Design and Analysis of 8× 8 SRAM Memory Array using 45 nm Technology at 100 MHz. In 2023 IEEE Devices for Integrated Circuit (DevIC) (pp. 501-506). IEEE.

[2] Arumugam N, Shakthi priya M, Suntrakanesh Subramanian. Design and analysis of SAPON approach: A new technique for Low Power VLSI Design using cadence tools with Generic 250 nm transistors. 2021 International Conference on Applied Electromagnetics, Signal Processing and Communication (AESPC).

[3] Rohit, & Saini, G. (2015). A stable and power efficient SRAM cell. 2015 International Conference on Computer, Communication and Control (IC4).

[4] K. Anami, M. Yoshimoto, H. Shinohara, Y. Hirata and T. Nakano, "Design considerations of a static memory cell", IEEE J. Solid-State Circuits, vol. SC-18, no. 4, pp. 414-418, Aug. 1983.

[5] Kutila, M., Paasio, A., & Lehtonen, T. (2014). Comparison of 130 nm technology 6T and 8T SRAM cell designs for NearThreshold operation. 2014 IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS).

[6] J.Ashwani; K.Deepa; K.Charan Kumar; Mr.B.Karthick; “Performance Analysis of Different SRAM Cells and Proposed 9T SRAM Cell” 2023 8th IEEE International Conference on Communication and Electronics Systems (ICCES 2023) IEEE Xplore Part Number: CFP23AWO-ART; ISBN: 979-8-3503-9663-8.

[7] Siddik, A., Pujari, S., Mallidu, J., Chandaragi, P., Huded, A., & Lakkundi, N. (2024, March). Performance Analysis of CMOS SRAM 6T, 7T and 9T Cells using Cadence at 180nm Technology. In *2024 3rd International Conference for Innovation in Technology (INOCON)* (pp. 1-5). IEEE.

[8] D. Mittal and V. K. Tomar, "Performance Evaluation of 6T, 7T, 8T, and 9T SRAM cell Topologies at 90 nm Technology Node," 2020 11th International Conference on Computing, Communication and Networking Technologies (ICCCNT), 2020, pp. 1-4, doi: 10.1109/ICCCNT49239.2020.9225554..

[9] C. Premalatha, K. Sarika and P. M. Kannan, "A comparative analysis of 6T, 7T, 8T and 9T SRAM cells in 90nm technology," 2015 IEEE International

Conference on Electrical, Computer and Communication Technologies (ICECCT), 2015, pp. 1-5, doi: 10.1109/ICECCT.2015.7226147

[10] CA Ajoy, A Kumar, CA Anjo, V Raja. Design and analysis of low power SRAM using cadence tools in 180nm technology. IJCST, 5(1), 2014.

[11] X Wang, Y Zhang, C Lu, Z Mao. Power efficient SRAM design with integrated bit line charge pump. AEU International journal of electronics and communications, 70(10), 2016.

[12] VS Baghel, S Akashe. Low power Memristor Based 7T SRAM Using MTCMOS Technique. Fifth International Conference on Advanced Computing & Communication Technologies, 2015

[13] R. Baker, "CMOS Circuit Design, Layout, and Simulation", 2nd Ed., Wiley & Sons Inc., 2007.

[14] R. Ruchi, and Sudeb Dasgupta, "Compact Analytical Model to extract Write Static Noise Margin (WSNM) for SRAM Cell at 45nm & 65nm nodes", IEEE Transactions on Semiconductor Manufacturing, Vol. PP, Issue 99, November 2017.

[15] V. Enumula, S. Gupta, R. Manchukonda, and N. Upadhyay, "Design and implementation of 16X8 SRAM in 0.25uM CMOS technology", https://pdfs.semanticscholar.org/24c8/5982c98c177e6393aef35b8891f44564e8ec.pdf

[16] V. Saxena, "SRAM Static Characterization", Boise State University,

[17] https://www.researchgate.net/file.PostFileLoader.html?id=54be4ae2d2fd64fb0d8b45cf&assetKey=AS%3A273675910090788%401442260829994

[18] J. Rabaey, A. Chandrakasan, and B. Nikolic, "Digital Integrated Circuits – A Design Perspective", 2nd Ed., Prentice Hall, 2009.