A LOW POWER AND LEAKAGE REDUCTION TECHNIQUE FOR CMOS USING CASCADE LEAKAGE TRANSISTOR

A DISSERTATION REPORT

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SUBMITTED BY

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CANDIDATE'S DECLARATION

I, **Kunal Rupraj Jagtap (2K22/VLS/06)**, a student of MTech (**VLSI Design and Embedded Systems**), hereby declare that, in partial fulfilment of the requirements for the award of a Master of Technology degree, we have submitted a Project report on **A Low Power And Leakage Reduction Technique For CMOS Using Cascade Leakage Transistor** To the Department of Electronics and Communication Engineering at Delhi Technological University. This material is original and not something that was copied from any source without appropriate citation. There has never been a degree, certificate, associateship, fellowship, or other title or honour that is comparable to this one awarded for the work done here.

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CERTIFICATE

I hereby attest that the project report on the topic **A Low Power and Leakage Reduction Technique For CMOS Using Cascade Leakage Transistor,** submitted by **Kunal Rupraj Jagtap (2K22/VLS/06)** of the Electronics and Communication Department at Delhi Technological University, Delhi, partially fulfils the requirements needed to be awarded a Master of Technology degree. The report is a record of the project work that the student completed under my supervision. To the best of my knowledge, neither this university nor any other has accepted this work in whole or in part for a degree or diploma.

PLACE: Delhi **Dr. Ajai Kumar Gautam**

DATE: 31/05/2024 **SUPERVISOR**

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M.TECH: VLSI Design & Embedded System

(2022-24)

ABSTRACT

In the realm of nanometer-scale CMOS technology, minimizing power consumption and leakage currents is essential for enhancing the energy efficiency of modern electronic devices. This dissertation presents a novel approach to reducing power and leakage through the development of the cascade leakage transistor (CLT) technique. The CLT method integrates advanced low-leakage strategies with the cmos technique, specifically applied to CMOS inverter design and other universal gates at the 45 nm in cadence software. The CLT technique involves utilizing two cascade leakage transistors to control the on and off states of the P-type pull-up and N-type pull-down transistors in a CMOS inverter and other universal gates. This innovative configuration effectively reduces static leakage power dissipation while preserving the integrity of the output signal waveform. Due to the cascade arrangement Despite an increase in propagation delay compared to conventional CMOS inverters, the trade-off results in a substantial leakage power reduction of approximately 59% and total power dissipation reduced by 24% overall for not gate compared to other technique.

Keywords: - Leakage power, low power technique, LECTOR, MTCMOS, CLT

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CHAPTER 1
INTRODUCTION

Managing Power usage is a paramount concern inside Very Large-Scale Integration (VLSI) circuit design, with Complementary Metal Oxide Semiconductor (CMOS) technology reigning supreme [3]. The contemporary emphasis on minimizing power usage isn't solely attributable to the surge in mobile applications; it's a longstanding issue predating the mobile era. Researchers have tirelessly explored myriad solutions, spanning from the micro-level of device engineering to macro-level architectural innovations. Yet, there's no one-size-fits-all solution to circumvent the inevitable trade-offs among power, latency, and chip real estate. Designers must judiciously select techniques that align with specific function requirements [5].

Power consumption in CMOS circuits comprises dynamic and static components. Dynamic power is incurred during transistor switching, while static power persists irrespective of transistor activity. Historically, particularly at 0.18μ technology and beyond, dynamic power hogged the limelight, accounting for over 90% of total chip power. Consequently, numerous strategies, including voltage and frequency scaling, were crafted to slash dynamic power [3].

However, with shrinking feature sizes below 65nm, static power emerged as a formidable adversary for contemporary and prospective technologies. In [8] According to the ITRS asserts that subthreshold leakage power dissipation could surpass total dynamic dissipation of power at the 90 nm technology node.

The primary cause of the increase in leakage in mosfets is the rise of leakage power. The voltage supply and threshold voltage decrease with the size of a technological feature. Then, when the threshold voltage decreases, subthreshold leakage power experiences an exponential increase. Furthermore, the threshold voltage is further lowered by the short-channel devices arrangement. Due to current tunnelling through the gate-oxide insulator, gate-oxide leakage power, in insertion to subthreshold leakage, increases total static power power [7].

If uncontrolled, gate-oxide leakage power might potentially challenge subthreshold leakage power in nanoscale technology due to the decrease in gate-oxide thickness that accompanies technological downsizing. On the other hand, different approaches are expected to reduce gate-oxide leakage. One proposed method to decrease gate leakage, for example, is to use high-k dielectric gate insulators. Thus, this thesis focuses on reducing power consumption from subthreshold leakage, assuming that gate-oxide leakage will be handled by other methods.

The "cascade leakage transistor"(CLT), a revolutionary circuit construction that this dissertation presents, provides designers with a new approach to solving static power issues. This revolutionary architecture combines the best features of two well-known methods: the force stack transistor method and the new leakage transistor method. We realize an over two orders of magnitude reduction in leakage power over traditional circuits by combining the force stack technique with the suggested leakage transistor. It's important to remember, too, that this method adds area overheads and more time. Though it comes with certain area and delay penalties, the suggested leakage transistor approach offers new points for designers looking for ultra-low leakage power consumption despite the associated overheads. This thesis explores the complexities of the cascade leakage transistor's fundamental architecture. We also examine a number of circuits designed to minimize leakage and power consumption, including memory systems and general logic circuits. We thoroughly assess the benefits and limitations of the suggested method during our investigation and offer solutions to reduce the related delay overheads.

This dissertation proposes an architectural-level power reduction strategy in addition to the suggested technique structure. Lowering the supply voltage for CMOS transistors is a very good technique because the transistors power consumption increases quadratically with supply voltage. On the other hand, lowering the supply voltage will always cause transistor switching delays to increase.

As a result, CMOS circuit design frequently entails balancing power consumption and performance, which are quantified in terms of delay. Even with these CMOS circuit trade-offs, It is likely to deliberately reduce the voltage supply at design level without sacrificing functionality [1]. In order to do this, A source of voltage for circuitry in noncritical pathways is decreased while it is maintained for design in the crucial channel

or paths, removing excess slack in the former. This novel low-power cascade leakage method, dubbed "Low-Power Operation," depends on forced stack rather than lowering the supply voltage.

1.1 Problem Statement

This project aims to develop novel low-power techniques for Very Large-Scale Integration (VLSI) logic. An increasingly important factor in the design of VLSI systems is power dissipation. Static power, which was before thought to be insignificant, is now receiving more attention due to technology's smaller feature sizes, while dynamic power has historically received more attention. Leakage power consumption must be minimised due to the acute, even exponential, increase in static power in nanoscale silicon VLSI technology [9]. It is imperative to reduce power consumption and leakage in CMOS circuits, especially in light of the ongoing reduction of technological nodes. Various methods have been developed to tackle these issues, each with its own set of obstacles and limitations. For example, Multi-Threshold CMOS (MTCMOS) balances power and execution by using transistors with varying threshold voltages. However, this method requires more chip area for power gating circuitry, increases design complexity and verification work, and may result in performance issues in timing-critical circuits [13].

By altering frequency and voltage in accordance with workload requirements, a technique known as DVFS helps to conserve power. Although efficient, DVFS has limitations, including reaction latency, complex control logic, and a limited voltage range that reduces possible power savings.In [12] However, leakage power is efficiently reduced by power gating, a technique that turns off the power to inactive circuit blocks. However, it increases the process of retaining state during power gating transitions, adds wake-up delay that might impair system performance, and requires design overhead for power switches and state retention logic. Another method for controlling leakage is body biassing, which modifies the threshold voltage dynamically. However, it involves intricate circuitry, is vulnerable to dependability problems like noise and ageing effects, and its effectiveness diminishes notably at lower technology nodes.

Clock gating lowers dynamic power and avoids unnecessary switching by halting the clock signal to vacant circuit blocks. But improper implementation might cause hiccups and timing errors, increasing the difficulty of design and verification. Moreover, it just focuses on dynamic power reduction; leakage power is not impacted. As an alternative, to reduce leakage, sleep transistors (header or footer) can be incorporated to disconnect the supply or ground during standby mode. However, this method comes with a large space overhead, possible performance loss because of more resistance in the power supply network, and more control logic complexity. which offers an additional way to reduce gate leakage and improve performance. However, there are obstacles to its implementation, including increased cost and complexity of production, problems with material compatibility, and the difficulty of maintaining benefits while addressing new leakage mechanisms as technology develops [6]. Essentially, optimising power efficiency within state-of-the-art semiconductor devices requires finding a compromise between power efficiency, design complexity, performance, area, and reliability.

We provide new VLSI techniques that aim to maintain Logical condition after obtaining incredibly less leakage power consumption, making them appropriate for systems with long idle times and modest response time needs. A crucial element that effectively reduces leakage current and maintains full input-output response with low leakage current is the force stack.

1.2 Thesis Organization

seven chapters comprise the structure of the thesis:

Chapter 1: Introduction: The topics surrounding power consumption in VLSI design are introduced It also describes the general structure of the thesis and summarises its contributions.

Chapter 2: Motivation: The reason for this research is covered in this chapter, with a focus on how crucial it is to solve power consumption and leakage currents in contemporary VLSI technology.

Chapter 3: Notation And Background: To ensure that the reader understands the vocabulary and underlying principles utilised throughout the dissertation, this chapter offers an explanation of the significant notation and background concepts.

Chapter 4: Literature Survey: This chapter outlines earlier research on leakage reduction and highlights the leading distinctions linking our approach and that earlier work.

Chapter 5: Proposed Circuit: This chapter explains about the novel circuit that we proposed to reduce static leakage and power with suitable simulation.

Chapter 6: Implementation: This chapter describes the implementation of NAND2 gate with the help of CLT technique.

Chapter 7: Result: This chapter gives the simulation result of all the circuits.

Chapter 8: Conclusion: This chapter concludes the overall thesis result and simulation.

CHAPTER 02

MOTIVATION

In the 1980s, CMOS technology replaced NMOS and bipolar technologies as the industry standard for VLSI design because it consumes a lot less power. While CMOS continues to provide this benefit, power dissipation has been a cause for concern. For a long while, the main indicator of overall power consumption in technologies with 0.18μ and higher was dynamic power, which justified for extra 90% (and often even extra 99%) of total chip power [9]. However, as technology moves towards tens of subthreshold regimes, static power is now just as significant as dynamic power. Many approaches to solving the leaking power problem have been put out in response to this change. One such strategy is the sleep transistor approach, which entails switching off transistors from power rails. This approach, however, causes a loss of state during periods of inactivity, resulting in longer wake-up times, which might not be appropriate for systems that need quick reaction times [8].

The rapid progress of semiconductor technology has led to significant enhancements in functionality and performance, making way for the development of progressively intricate and potent integrated circuits (ICs). Maximum Power efficiency has become a key concern in modern electronic devices, ranging from laptops and smartphones to massive data centres and Internet of Things (IoT) devices Excessive power consumption not only shortens the battery life of portable devices but also increases the requirement for cooling and operational expenses in large-scale systems. Moreover, problems with thermal management brought on by increased power density may jeopardise the dependability and durability of integrated circuits [7].

Even in the idle state of circuits, leakage currents significantly contribute to overall power dissipation as transistor dimensions continue to decrease. Because leaking power might account for the majority of the power budget in always-on applications and standby modes, this problem is very troublesome. For this reason, developing efficient methods for reducing power and leakage is not only an optimisation objective but also a requirement for guaranteeing the long-term viability and expandability of electronic systems in the future.

Innovative solutions that strike a balance between power savings and performance, area efficiency, and dependability are required to meet these problems. The purpose of this thesis is to investigate and develop novel approaches to lower power consumption and leakage currents in CMOS circuits. In doing so, it advances the creation of electronic systems that are energy-efficient, which is essential for the advancement of technology in the future.

Examine the scenario of a cell phone's static (leakage) power consumption to illustrate the potential consequences of this thesis. Presume that the cell phone is always on and running all day. The real usage duration is short, though. The mobile phone is only actively used 1.15% of the total on-time consumption, or 500 minutes / (30 days × 24 hours × 60 minutes), and overall usage of 500 minutes each month. This suggests that the cell phone is inactive for 98.85% of the time. However, because of static power consumption, the phone uses energy even when it is in standby mode, which shortens the battery life. With cutting-edge technologies, such those that employ 0.07μ processes, the effect of the impact of leakage power becomes substantial. This situation emphasises how important it is to have efficient leakage reduction methods. These gadgets' battery lives can be greatly increased by reducing static power consumption, which improves both the general usability and energy efficiency of electronic devices. By creating novel approaches to lower power consumption and leakage currents in CMOS circuits, this thesis seeks to address these issues and promote the development of electronic systems that are more energy-efficient.

CHAPTER 3

NOTATION AND BACKGROUND

We cover through key explanations and the dissertation uses a VLSI basis in this chapter.

In the beginning, we present our main research emphasis, which is subthreshold leakage power consumption. Next, we describe the backdrop of a specific leakage power model that takes into consideration the stack effect, which plays a significant role in our study's leakage reduction. Next, we discuss the body-bias effect and how it relates to what we do. We also discuss the power consumption of subthreshold leakage in ordinary CMOS transistors. Lastly, we go over the trade-offs that CMOS circuits have between switching power and delay.

3.1 Leakage Power

This section explains the background information and notation related to leaking power consumption.

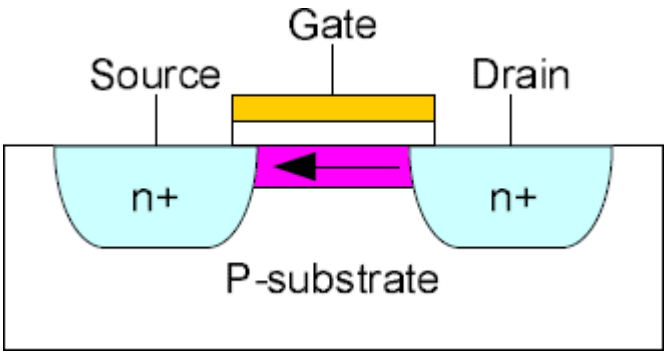

Figure 3.1: Subthreshold leakage of a mosfet

For advancements at 0.13μ or lower. leakage, that is static power consumption takes centre stage, whereas dynamic power continues to be the key component for technologies at 0.18μ and higher. One among the primary reasons for static power consumption in CMOS is subthreshold leakage current[3], which is the drain to source current flow when the gate voltage is less than the transistor threshold voltage. Figure3.1 illustrates this phenomenon. Because subthreshold current increases

exponentially with threshold voltage, nanoscale technologies with lower threshold voltages will have substantial subthreshold leakage power consumption.

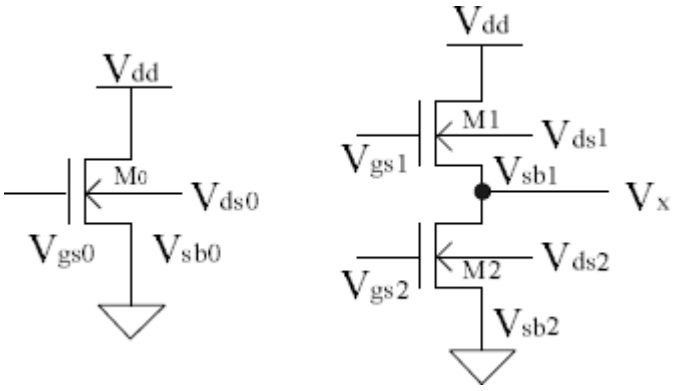

Figure 3.2: (a) A MOS transistor (b) stacked transistors

By stacking transistors, or by utilising the so-called "stack effect," subthreshold leakage can be decreased [4]. When two stacked transistors are turned off simultaneously, the stack characteristic property results in reduced leakage power consumption. Allow us to explain a key model for stack impact leakage mitigation. The leakage models in (1) and serve as the foundation for the approach we describe here. Leakage current (Isub0) for the MOS transistor in Figure 3.2(a) that is switched off can be written as follows:

$$I_{sub0} = Ae^{\frac{1}{\eta V_\theta}(-V_{th0}+\eta V_{dd})} \quad (1)$$

where V is the thermal voltage and n is the subthreshold swing coefficient. The voltages that correspond to the gate-to-source, zero-bias threshold, base-to-source, drain-to-source, and drain-to-source.

Γ the body-bias effect coefficient, is the representation of the Drain Induced Barrier Lowering coefficient. The zero-bias mobility is denoted by μ, the gate-oxide capacitance is represented by Cox, and the effective channel length is Leff. (Note that we will be assuming μn = 2μp throughout this thesis, This means that a nMOS carrier has double the mobility of a pMOS carrier. Additionally, take note of the fact that we characterise the circuit models utilised in this thesis utilising a W/L ratio determined by the real transistor's size.

A CMOS transistor's threshold voltage can be adjusted with body bias. Generally, we apply Gnd to a body of nMOS and Vdd to the body of pMOS. Zero-Body Bias (ZBB) is the state in which a transistor's body voltage and source voltage are equal. ZBB threshold voltage is the voltage at which ZBB occurs. Reverse-Body Bias (RBB) is the state in which the body voltage is less than the source voltage due to biasing a negative voltage to the body.

On the other hand, a situation known as forward-body bias occurs when the body's positive bias (FBB) causes the voltage to exceed the source voltage. A transistor's threshold voltage rises when RBB is applied and decreases when FBB is applied. The body-bias effect is a phenomenon that is widely employed to dynamically alter threshold voltage.

In Section 3.1, it was discussed how the stack effect, body-bias effects, and subthreshold leakage power consumption might alter each other. In the next section, we go into CMOS inverter leakage current.

3.2 CMOS Inverter Leakage Paths

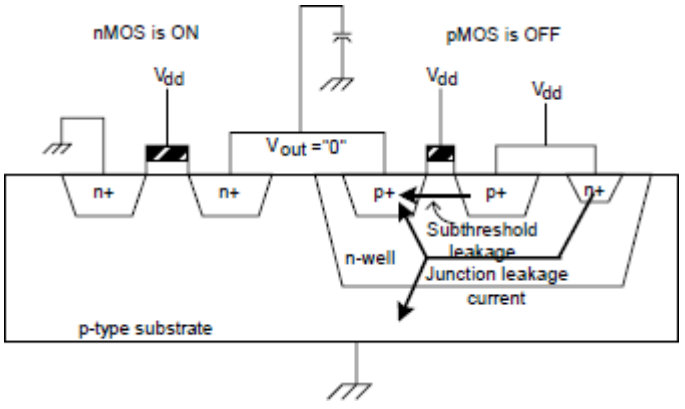

Figure 3.3: CMOS inverter leakage paths

If the gate-source voltage (Vgs) in the MOSFET transistor is lower to the threshold voltage (Vth), subthreshold leakage, also known as subthreshold conduction or subthreshold drain current takes place. The transistor may be in the "off" state, but a very minor quantity of current still goes from the drain to the source. Leakage current

can significantly influence the power consumption of CMOS circuits, particularly in contemporary low-power applications.

3.3 Mechanism of Subthreshold Leakage

When a MOSFET channel's gate voltage is high enough to slightly cause current to flow through it but not high enough to totally flip the surface, subthreshold leakage occurs as a result of the weak inversion condition. The primary source of this current is the diffusion of minority carriers electrons in p-channel MOSFETs or holes in n-channel MOSFETs across the channel.

3.4 Trade-offs between Switching Power and Delay

This section covers the trade-offs between switching power and delay.

The two components that comprise CMOS power consumption are leakage power and dynamic power, which include both switching power and short-circuit power. Short-circuit power occurs when transistors are turned on and off If a pull-up and pull-down systems are turned active simultaneously for a short period of time. A gate charges its output load capacitance, switching power is used. For channel lengths greater than 180nm, leakage power is insignificant in relation to dynamic power. Additionally, for a typical CMOS design, Less than 10% of dynamic power is used for short circuit power, and this is based upon a consistent supply voltage to threshold voltage ratio, There is no change in the link between dynamic power and short-circuit power. The switching power (Pswitching) equation for 0.18µ and Given that switching power is significantly bigger than short circuit and leakage power, higher may be used to indicate the CMOS power consumption of a specific CMOS gate under investigation.

$$P_{\text{switching}} = \alpha\, C_L\, V_{DD}^2 f \tag{2}$$

The load capacitance, supply voltage, and clock frequency of the CMOS gate are shown by the symbols CL, Vdd, and f, correspondingly [5]. The notation "pt" indicates how many times a gate's output transitions from Ground to Vdc every second. It is crucial to remember that switching power is not utilized when output capacitance discharges from Vdd to Gnd because power from Vdd is not used (i.e., discharging to Gnd does not consume battery power). Since the switching ratio varies with the input vectors and

benchmark programmes, it is possible to use the average result of each benchmark as a substitute for the switching ratio.

Equation 2 shows that CMOS switching power consumption is reduced quadratically when Vdd decreases. Regrettably, as the calculated equation below shows, this power decrease results in an increase in the gate latency in a CMOS device.

$$T_d \propto \frac{V_{dd}}{(V_{dd} - V_{th})^{\alpha}} \tag{3}$$

The terms Td, Vth, and denote the gate delay in a CMOS circuit, the transistor's velocity saturation index, and its threshold voltage, respectively. Values below 0.1μ close to 1 are well-known CMOS technology may employ a constant value instead of scaling it down with the technological feature size to prevent the hot carrier issue [7]. Changing Vth could result in a constant value because It depends on the voltage at the gate-source [8]. Equation (3) switching power decreases and Equation 3rd gate delay increases as Vdd is decreased. Equations show how the CMOS circuit speed may be changed with switching power usage. When numerous requirements must be traded off, such as power and delay, one design may outperform another in certain areas. A Pareto point in design space is one that does not have any inferior objectives.

In this thesis, to calculate the amount of leakage power used, We measure leakage power when transistors are not switching. Furthermore, we measure the power consumed by transistors during their switching process to quantify the active power consumption. This includes both dynamic and leaky power consumption.

This chapter provides an explanation of the significant nomenclature and VLSI background used in this thesis. Here will talk about earlier low-power research that is pertinent to our work in the next section.

CHAPTER 4
LITERATURE SURVEY

We examine significant earlier research that is directly relevant to our findings in this chapter. In addition, our research is contrasted with the earlier studies. We first review the literature on leakage power reduction. We conclude by reviewing earlier approaches that are pertinent to minimal power consumption and low static power.

4.1 Reducing Static Power VLSI Research

This part covers earlier low-power methods that mainly aim to lower CMOS circuit leakage power consumption. There are two categories into which techniques for leakage power reduction can be placed: Techniques categorized as (i) state-saving, in which the circuit condition (present value) is maintained, and (ii) state-destructive, in which the circuit's current Boolean output value may be lost [8]. Compared to state-destructive techniques, state-saving techniques have the benefit that the circuitry doesn't need state regeneration in order to resume operating instantly again. We use this criterion to describe all low-leakage techniques. First, we look at low-leakage circuit design techniques for general logic, then we focus on low-leakage inverter and NAND design independently.

4.1.1 Forced stack

One way to reduce leakage power even further is to stack the transistors. Figure 2.3 An inverter with forced stack. When two or more transistors are turned down simultaneously, the impact of stacking the transistor reduces sub-threshold leakage current. Also it has width half so area is same and resistance will increase.

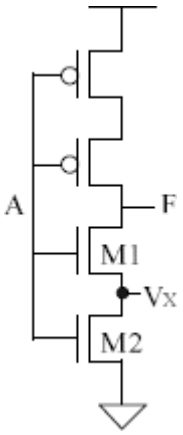

Figure 4.1: Forced stack technique

The forced stack inverter seen in figure 4.1 provides insight into the stacking effect [3]. A mere two transistors are present in the typical inverter. However, in this forced stack inverter scenario, two pull-up and two pull-down transistors are used. In a forced stack circuit, each input shares the same input. If the input is "0," transistors M1 and M2 are both off. In this instance, the intermediate node voltage is Vx. The internal resistance of transistor M2 is present. Because of this resistance, Vx is greater than the ground potential. The M1 transistor experiences a negative source-base voltage (Vsb) and a negative gate-source voltage (Vgs) as a result of this positive Vx. In this case, the drain-induced barrier lowering (DIBL) is lessened because M1 also has a lower drain-source voltage (Vds). Every transistor has the same input. This forced stack method preserves state as a result. Put otherwise, when the circuit is in the off-mode, it preserves its current state[3]. This forced stack inverter's primary flaw is that it is unable to utilize high Vth transistors. Because there is a significant increase in latency when using a high Vth transistor. Five times as much delay has increased as in a regular CMOS.

4.1.2 Sleep transistor

Sleep transistors are used in state-destructive techniques to cut off transistor networks (pull-up, pull-down, or both) from supply voltage or ground [5]. These methods are also known as gated-Vdd and gated-Gnd (keep in mind that dynamic power reduction typically uses a gated clock). Low-voltage transistors are used in logic circuits. to

maintain rapid logic switching speeds; however, Motoh et al. propose a technique they call multi-threshold-Voltage CMOS (MTCMOS). As seen in Figure 4.2, this method High-Vth sleep transistors are used between pull-up and Vdd networks, as well as between pull-down and ground [8].

The sleep transistors are turned off when the logic circuits are not in use. By isolating the logic networks, the sleep transistor technique dramatically reduces leakage power during sleep mode. On the other hand, area and latency are increased by the extra sleep transistors. Furthermore, because of floating values, the pull-up and pull-down networks will become unresponsive during sleep mode. Because of the need to recharge transistors that lost their states while you slept, these floating values have a major impact on the wake-up time and sleep approach's energy usage.

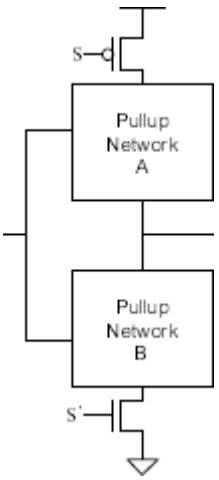

Figure 4.2: Sleep transistor technique

4.1.3 LEAKAGE CONTROL TRANSISTOR (LECTOR) Technique

The LECTOR (Low LEakage Convergent Threshold Optimization) technique is designed in order to lower digital circuit leakage power by leveraging the concept of transistor stacking. It operates on the premise that the Multiple transistors switched off along the circuit from the source voltage to ground can effectively mitigate leakage current compared with a setup where the path only has one transistor that is off [6].

In digital circuits, A transistor still conducts a tiny amount of current even when it is in the off state because of leakage. Through the clever placement of many transistors in

series with the supply voltage and ground, the LECTOR technique aims to exploit the "stack effect" to minimize leakage power. Essentially, when several transistors are turned off in succession along the path, With the astute arrangement of several transistors in series with the ground and supply voltage

This technique is particularly useful in standby or idle states of digital circuits, where reducing leakage power is crucial for prolonging battery life and improving overall energy efficiency. By optimizing the configuration of transistors in the circuit to maximize the stack effect, the LECTOR technique offers a promising approach to mitigating leakage power and enhancing the power efficiency of digital systems.

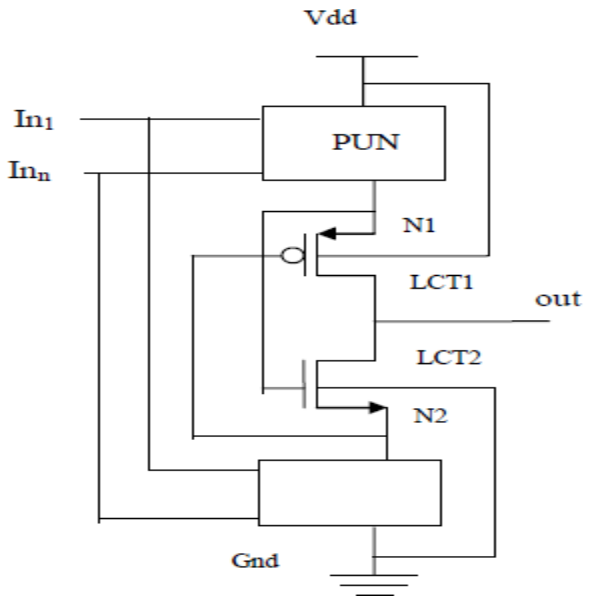

Figure 4.3: LECTOR Technique

4.1.4 ONOFIC approach

The ONOFIC (Optimized NOde Forward Inverter Chain) approach is a circuit-level strategy aimed at reducing leakage current and delays in logic circuits. This approach involves inserting an additional logic circuit, known as the ONOFIC block, to reduce leakage current between the pull-up and pull-down networks. One NMOS (n-typemetal-oxide-semiconductor) and one PMOS (p-type metal-oxide-semiconductor) transistor make up the ONOFIC block [6], configured as shown in Figure 4.4. The term "ONOFIC" is derived from the requirement that this logic block must be in either an "ON" or "OFF" condition for any output logic level.

In the ONOFIC block, the NMOS transistor's gate is connected to the PMOS transistor's drain, and the PMOS transistor's gate is connected to the circuit's output. The NMOS transistor's source is connected to the drain terminal of the pull-down network, while the PMOS transistor's source is connected to the circuit's power supply. The drain terminal of the NMOS transistor is linked to the circuit's output. Furthermore, the body terminal of the NMOS transistor is grounded, and the body terminal of the PMOS transistor is linked to the power supply level.

By strategically configuring the ONOFIC block in this manner, Leakage current and delays in the logic circuit can be minimized, thereby improving overall circuit performance and energy efficiency.

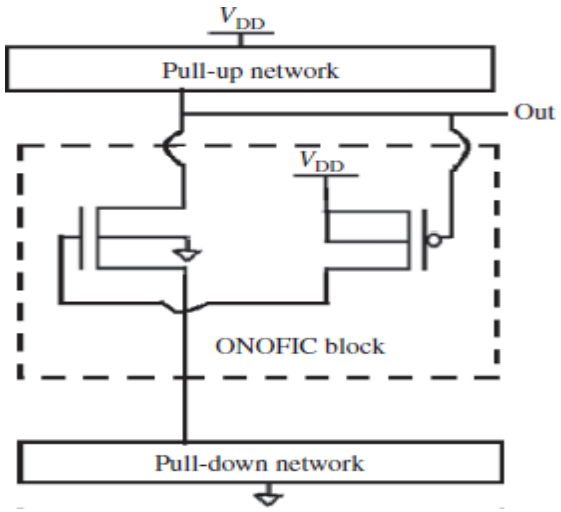

Figure 4.4: ONOFIC transistors technique

The key advantage of the ONOFIC technique lies in its improved on/off behavior. When the ONOFIC block is in the "OFF" state, both ONOFIC transistors work in the linear area, ensuring an accurate logic level at the output. When the ONOFIC block is turned "OFF," both transistors are in cutoff mode, which efficiently reduces leakage current in both active and standby modes.

In "ON" state, the ONOFIC block offers a low-resistance conducting path, facilitating efficient signal transmission. On the other hand, in the "OFF" state, the logic block has exceptionally high resistance, allowing for fine control over leakage current. This

characteristic ensures that leakage current is minimized when the circuit is not actively processing signals, this improves power efficiency and extends battery life in portable devices.

4.2 Summary

In conclusion, several advanced techniques have been developed to tackle the challenge of power consumption in CMOS circuits, each with its unique strengths and trade-offs. The forced stack technique effectively reduces static power by increasing the threshold voltage through series transistor stacking, though it introduces some delay. The sleep transistor technique, or power gating, minimizes leakage power during idle periods by disconnecting the power supply with high-threshold transistors, requiring careful management of wake-up times and performance impact. The LECTOR technique employs additional transistors to dynamically control leakage currents, offering significant reductions in both subthreshold and gate-oxide leakage without major design changes, albeit with some delay and area overhead. The ONOFIC approach focuses on optimizing the ratio between on-state and off-state currents to balance performance and leakage, utilizing adjustments in threshold voltage and advanced materials. By integrating these techniques, designers can achieve substantial power savings and improved energy efficiency in CMOS circuits, addressing the critical demands of modern low-power VLSI design.

CHAPTER 5
PROPOSED WORK

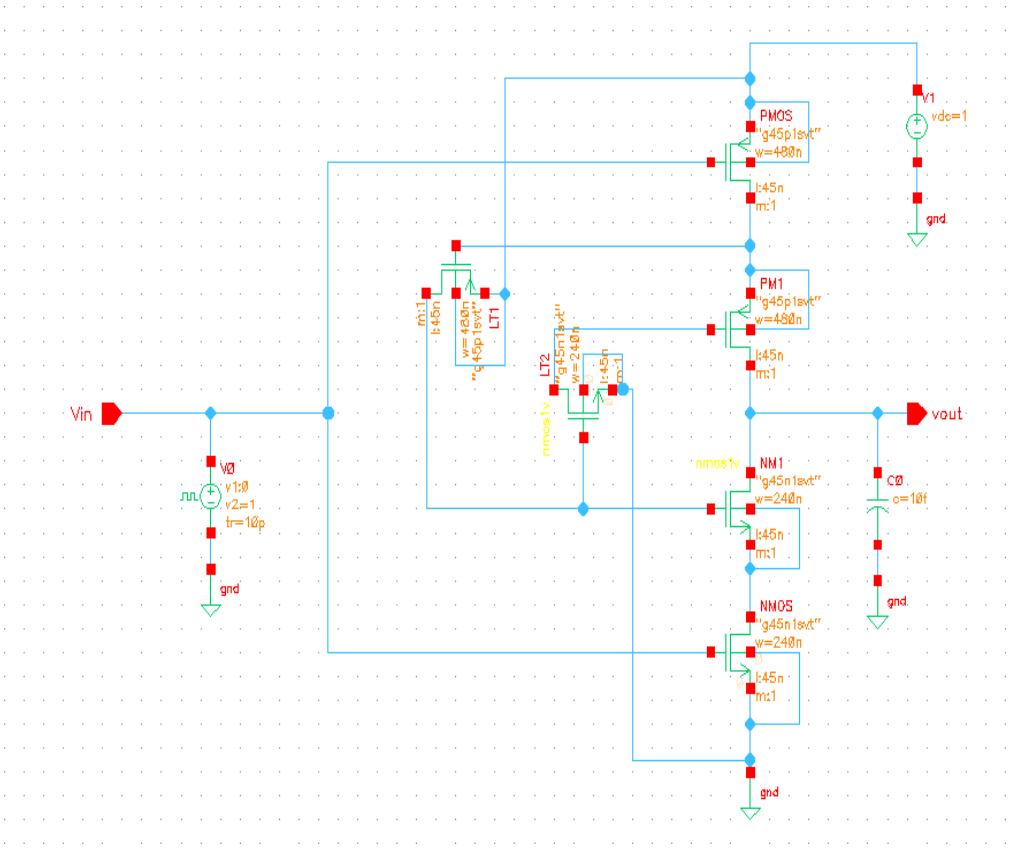

Figure 5.1: Proposed design of CLT using inverter

This method uses the stacking effect, several transistors linked in series are switched off to decrease power dissipation. The drain terminal of LT1 regulates LT2, NM1. The pull-up network's logic function determines LT1's input signal. When the input to LT1 isset to the logic value '0', LT1 allows the supply voltage to pass from source to drain terminal., activating LT2, nm1. As a result, the output logic is determined by the pull-down network's logic function and the principal inputs.

An inverter circuit based on the CLT method was constructed to illustrate its basic operation and exact input-output response. Figure 5.1 depicts a schematic representation for this inverter circuit.

When a logic 1 is applied to the input Vin, the NMOS transistor goes on and the PMOS transistor switches off, resulting in a logic 0 at the source of the PMOS, which activates LT1. This causes LT2, NM1 to turn on with a logic 1, while a logic 0 is passed to the stack consisting of PM1. Consequently, all transistors are on except the PMOS, connecting the output Vout to logic 0.

Conversely, when a logic 0 is applied to the input Vin, the PMOS transistor turns on, producing a logic 1 at its drain, which deactivates LT1. This results in the drain passing a logic 0, turning off LT2 and the stack of NM1. The drain of LT2 then activates the stack of PM1, connecting Vdd to Vout as logic 1. This is how it will work as inverter

This method minimizes leakage power without the need for additional sleep or bias transistors. It employs a fixed configuration for leakage reduction. The transistors LT1 and LT2 are responsible for minimizing leakage power, while stack combinations of PMOS and NMOS ensure the propagation delay of the logic circuits is maintained. stack combinations are crucial for achieving accurate output levels.

TABLE 5.1 Operating Status Of Transistor

Input level	PMOS	NMOS	LT1	LT2	PM1	NM1
Logic 0	ON	OFF	OFF	OFF	ON	OFF
Logic 1	OFF	ON	ON	ON	ON	ON

5.2 Simulation Setup

In the simulation setup, I utilized the Cadence tool to perform simulations, incorporating both static and transient analysis with ADL L, as well as dynamic analysis at the 45nm technology node at 27 ^{0}C Temperature. A supply voltage (Vdc) of 1 volt was used for all simulations, ensuring consistency in the respective parameters. The period for the simulations was set to 10ns, with rise and fall times of 10ps and a pulse width of 5ns. This setup was maintained across all simulations to ensure uniformity in the analysis and results.

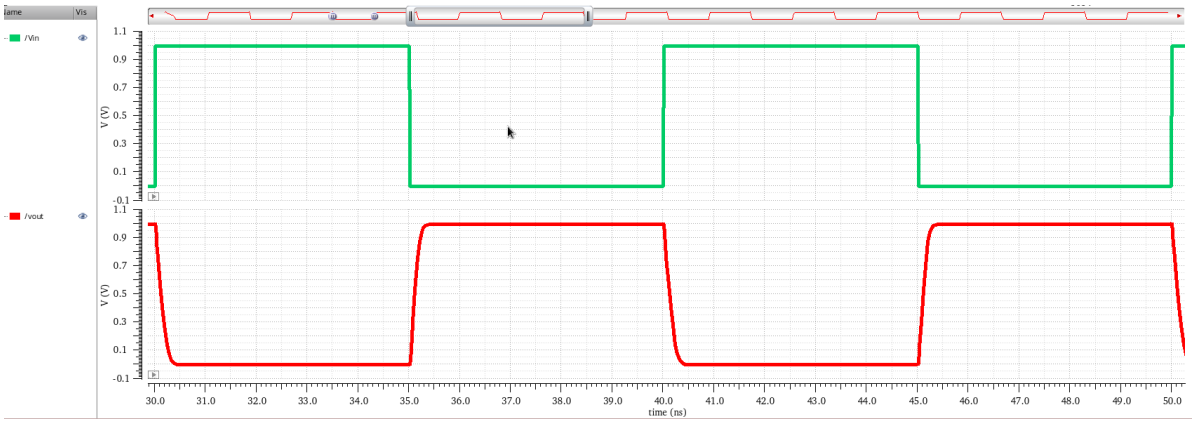

Figure 5.3: Transient analysis of inverter output using CLT approach.

Figure5.3 illustrates The input/output behavior of an inverter CMOS circuit employing the suggested leakage cascade transistor approach at the 45nm technology node.

5.3 Propagation Delay

One performance parameter used to assess a logic circuit's speed is propagation latency. If the circuit has fewer transistors, we can obtain a quick reaction from it.22 Every leakage reduction method includes extra transistors that are placed and could result in significant delays.The delay is calculated using the span of time interval between the input and output signals' 50% transitions. Equation (3) displays the propagation delay on average.

$$p = \frac{p_{hl} + p_{lh}}{2} \tag{3}$$

The average propagation delay is denoted by p. Time gap phl accounts for 50% of growing input and decreasing output, whereas plh accounts for 50% of declining input

and increasing output.Table 7.1 exhibits delays in propagation for various logic circuits using leakage mitigation methodologies at 45 nm technology nodes.

Propagation delay is coming out to be 112.5 ps for below output

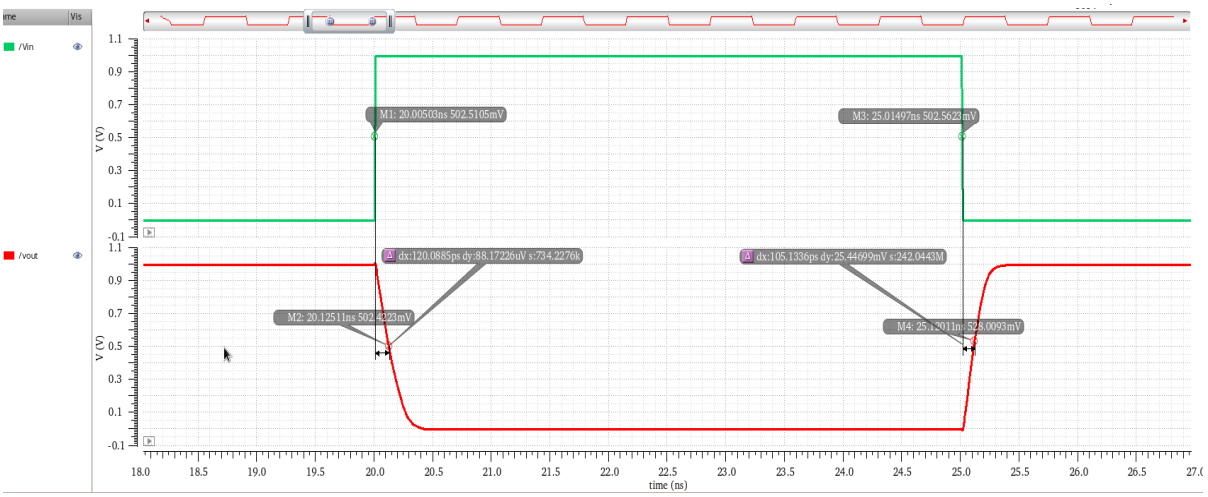

Figure 5.4: Delay of inverter output

5.4 Leakage Power

Subthreshold leakage, also known as subthreshold conduction or subthreshold drain current, happens in a MOSFET when the voltage from the gate to the source (VGS) is smaller to the threshold voltage (Vth).Transistor is technically in the "off" state, but a very minimal amount of current is still flowing from the drain to the source. This leakage current may significantly affect the power consumption of CMOS circuits, especially in modern low-power applications.

Compared to a traditional CMOS inverter, our CLT suggested design's leakage power for Vin 0 is 27.47 pA and for Vin 1 is 4.1584 pA.

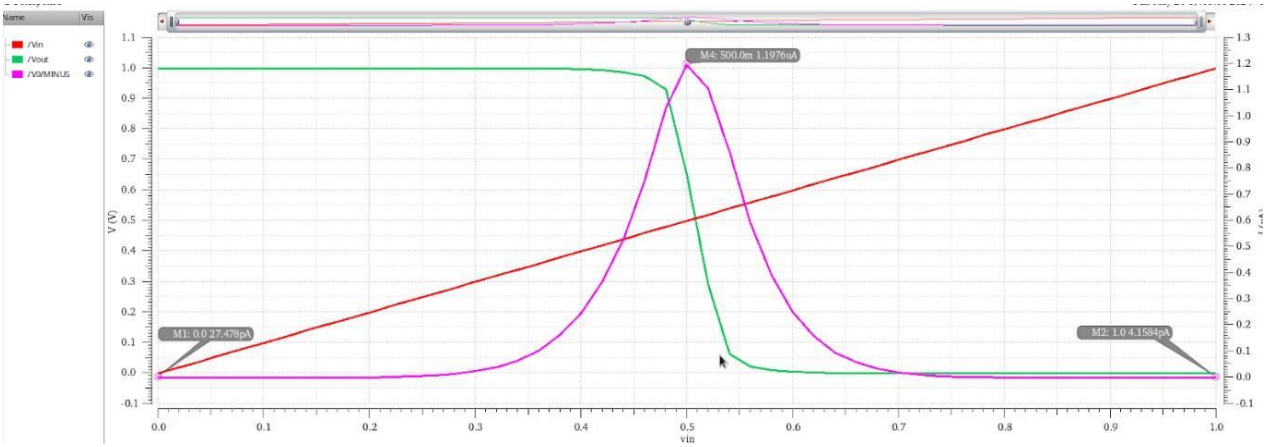

Figure 5.5: Leakage power

5.5 Dynamic Power

The main cause of dynamic power consumption in CMOS circuits is the charging and discharging of loading the capacitances during switching operations. Each time a transistor switches states, the capacitive loads associated with the circuit nodes are either charged or discharged, resulting in a flow of current from the power supply. This dynamic power usage can be calculated using the equation:

$$P_{\text{dynamic}} = \alpha C_L V_{DD}^2 f \quad (4)$$

where α is the activity factor denoting the fraction of the clock cycle that switching happens, CL is the total load capacitance, VDD2 is the supply voltage, and f is the operating frequency. This connection shows that dynamic power usage is proportional to the square of supply voltage, the load capacitance, the activity factor, and the operating frequency, highlighting the significance of the parameters to design energy-efficient CMOS circuits

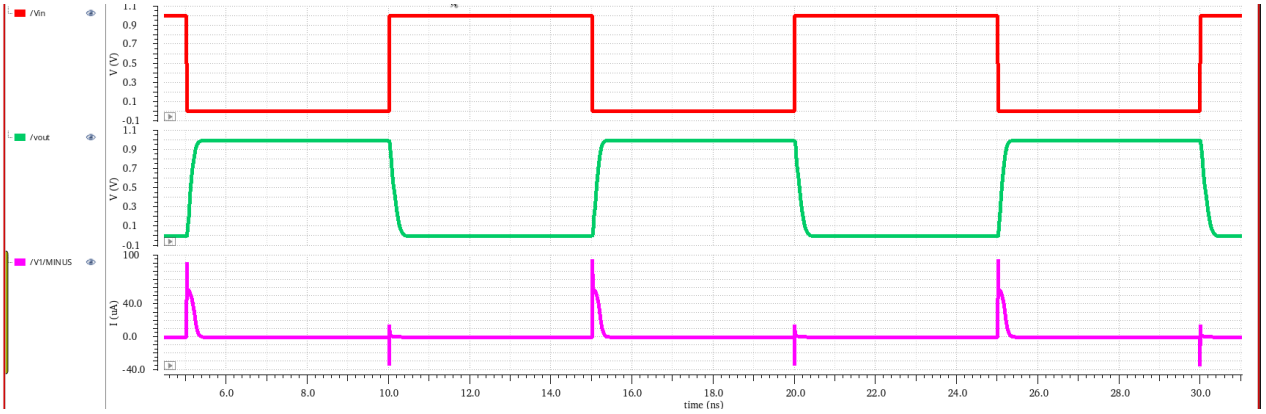

Figure 5.6: Dynamic Power

5.6 Total Power

In CMOS circuits, total power utilization includes dynamic power, static power, and short-circuit power. The charging and draining of load capacitances during switching operations generates dynamic power. Leakage currents going through transistors even when they are not actively switching provide static power, also known as leakage power. These currents are mostly caused by subthreshold leakage, gate oxide leakage, and junction leakage. When both pull-up and pull-down transistors are partially governed when switching, A direct current path is created between the source voltage and the ground. resulting in short-circuit power for limited periods of time. These components work together to manage the overall power consumption of CMOS circuits, highlighting the significance of power optimisation and management in developing energy-efficient designs, especially in high-performance and battery-operated systems.

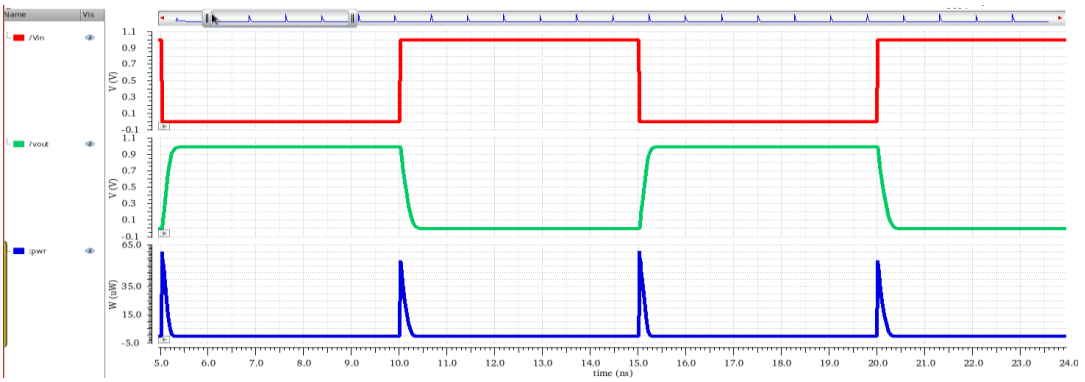

Figure 5.7: Total Power

CHAPTER 06

IMPLEMENTATION

6.1 NAND2 Design Approach using CLT

The application of the proposed cascade leakage transistor (CLT) approach extends to the design of all circuits, as exemplified in the construction of a 2-input NAND (NAND2) gate for comparative analysis. The schematic representation of the NAND2 circuit utilizing the CLT approach is delineated in Figure 4.1. Within the PDN of the NAND2 circuit, two n-channel CMOS devices are strategically incorporated to facilitate the NAND operation. The evaluation phase orchestrates the NAND operation at the output, showcasing the adaptability and effectiveness of the CLT approach in the context of digital circuit design.

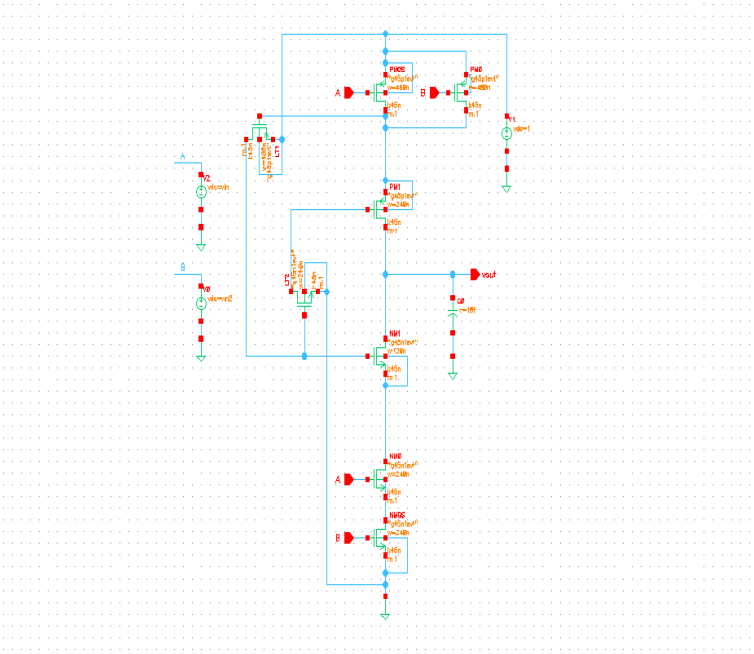

Figure 6.1: NAND2 Design Circuit Using CLT

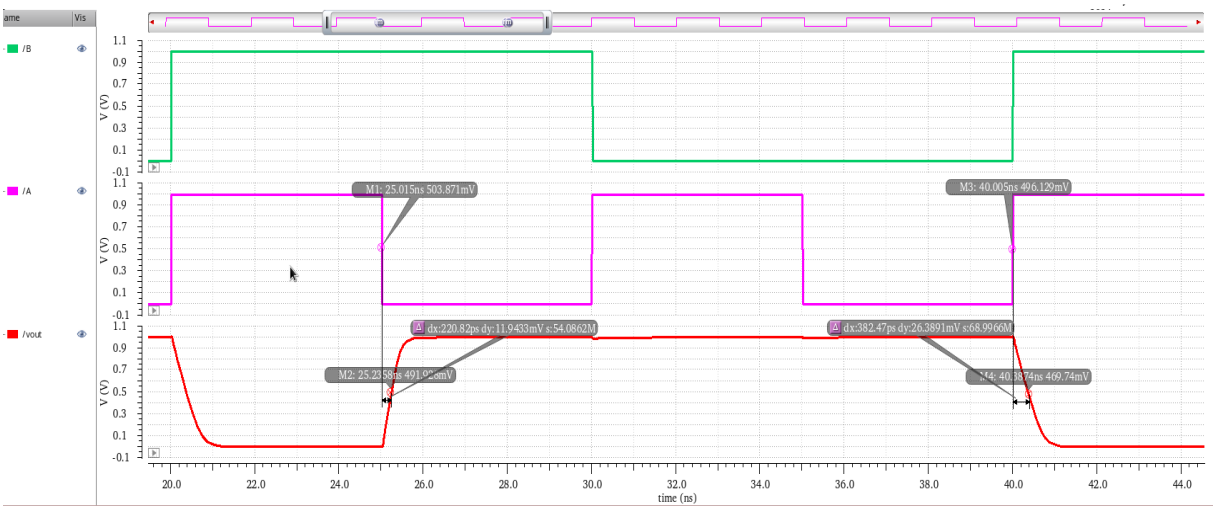

Figure 6.2: NAND2 Design Circuit Output using CLT

6.2 NOR2 Design Circuit Using CLT

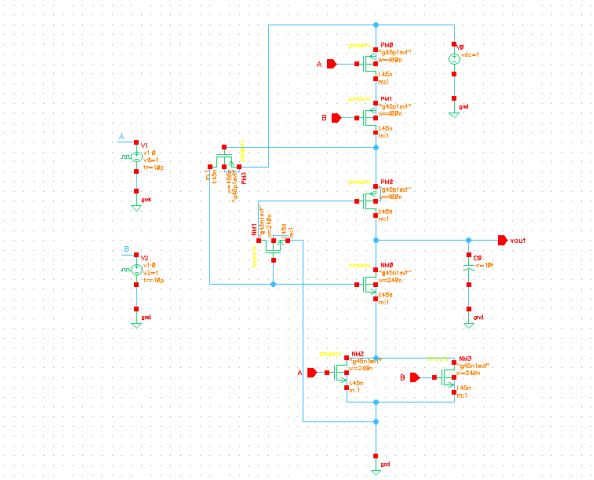

Figure 6.3: NOR2 Design Circuit Using CLT

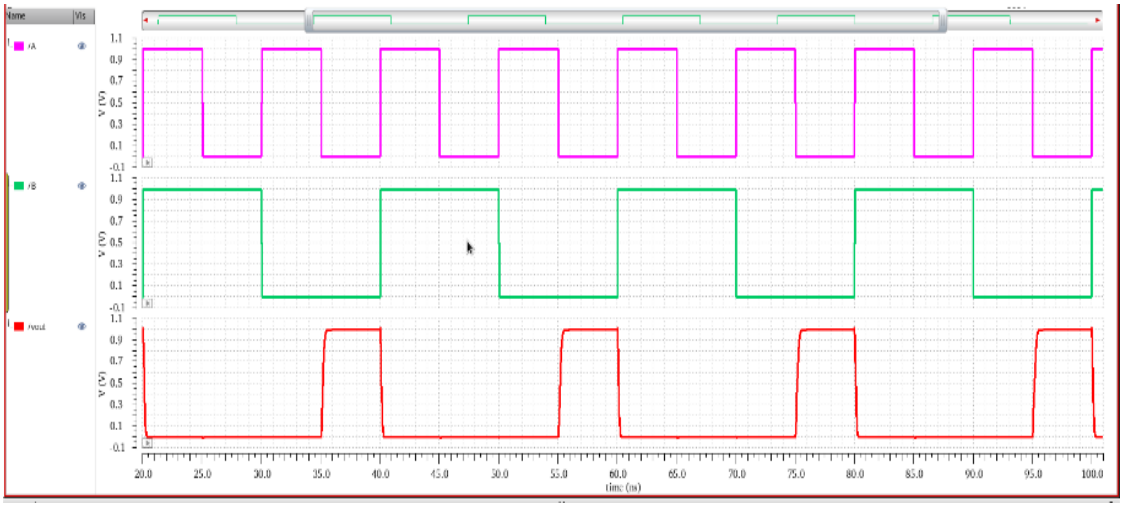

Figure 6.4: NOR2 Design Circuit Output using CLT

6.3 HALF ADDER Design Using CLT

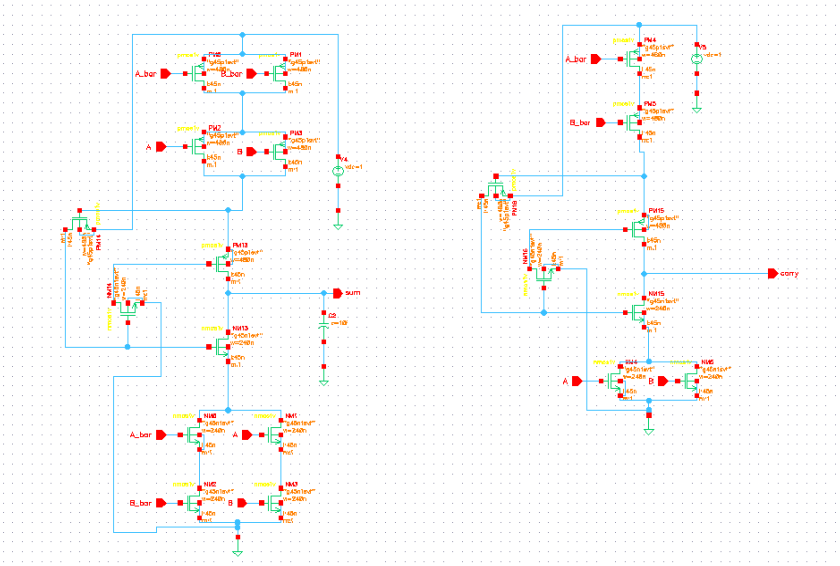

Figure 6.5: Half adder Design Circuit Using CLT

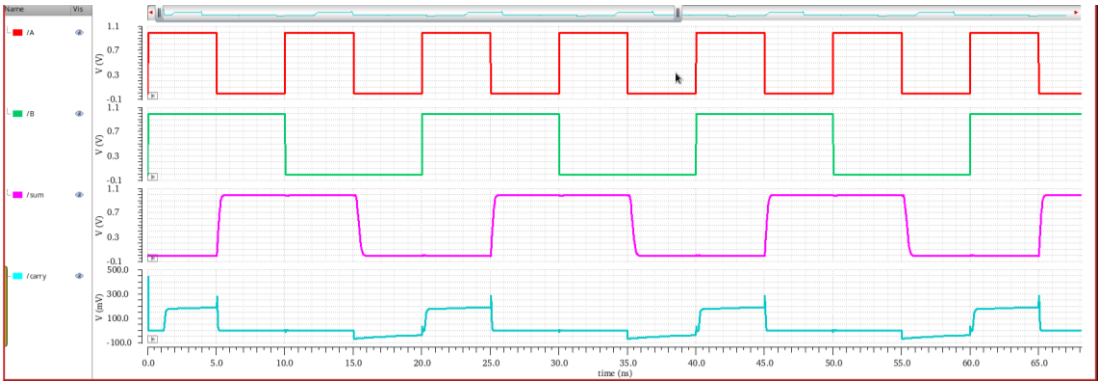

Figure 6.6: Half adder Design Circuit Output using CLT

CHAPTER 07

RESULTS

Along with static power dissipation, the propagation delay and power consumption of common CMOS architectures are tabulated below. Here, cadence tools are used to model the fundamental CMOS designs at 45nm. We have included a table that compares logic gates using our proposed CLT approach, sleep transistor logic gates, and conventional circuits employing various low power techniques. In the table, we also displayed the power consumption and delay graphs for NAND2, NOR2 and HALF ADDER architectures 6.1,6.3 and 6.5 and the figure depicts simultaneous INVERTER designs figure 5.1

Table 7.1 Simulation Results of a inverter Circuit

Inverter Technique	**Static Power(pw)**		Power dissipation (w)	Delay (ps)	PDP (aJ)
	0	**1**			
Base Case	46.73	32.01	8.089E-6	59.28	4.79E-16
Lector	41.21	29.01	10.42E-6	63.29	6.56E-16
MTCMOS	43.41	30.24	6.47E-6	70.57	4.56E-16
Transistor Stacking	28.29	25.37	7.22E-6	90.3	6.51E-16
ONOFF Approach	22.47	23.29	4.63E-6	94.36	4.36E-16
Sleepy Keeper	20.78	19.07	3.52E-6	100.21	3.52E-16
Dual Sleep	18.78	19.68	3.21E-6	112.25	3.60E-16
Proposed CLT	27.47	4.15	1.086E-6	112.5	1.22E-16

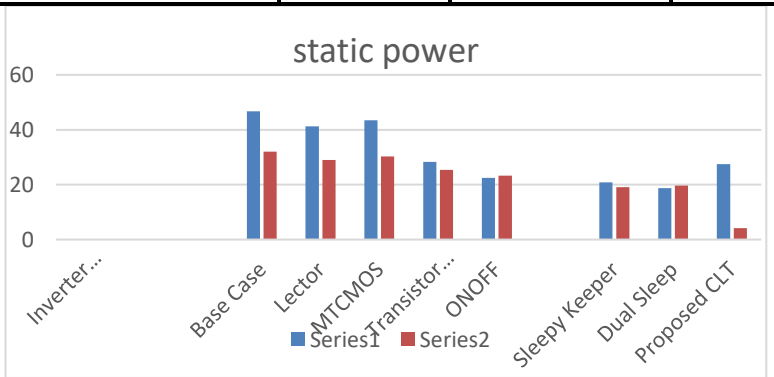

Figure 7.1: Static Power comparison of inverter circuits

Table 7.2 Simulation Results of a different logic Circuits

	Maximum power dissipation(w)	Delay(ps)	PDP(aJ)
Cmos NAND2	6.126E-3	210.32	1.28E-12
MTCMOS NAND2	4.65E-3	298.30	1.38E-12
ONOFF NAND2	4.84E-3	281.1	1.36E-12
CLT NAND2	4.114E-3	301.64	1.32E-12
Cmos NOR2	6.01E-3	160.25	1.23E-12
CLT NOR2	4.81E-3	194.23	1.16E-12
HALF ADDER CMOS(12T)	321.87E-3	219.97	7.68E-12
HALF ADDER CLT	240.7E-3	317.26	7.03E-12

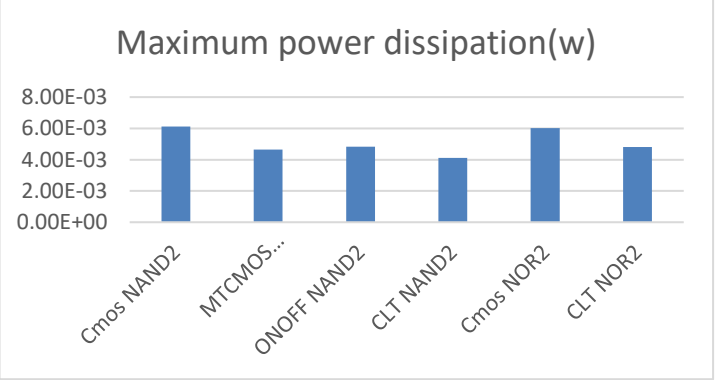

Figure 7.2: power dissipation comparison in universal gates

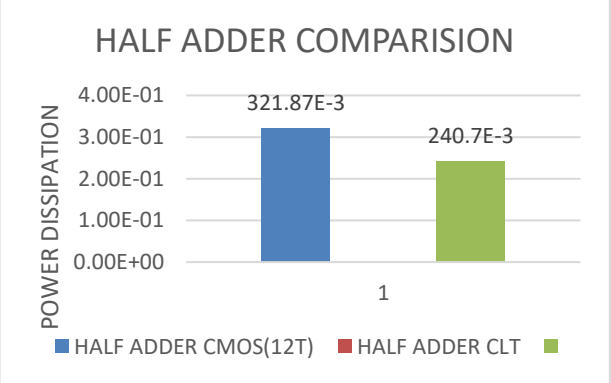

Figure 7.3: power dissipation comparison in half adder

CHAPTER 5

CONCLUSION

In nanometre-scale CMOS technology, subthreshold leakage power has become nearly as significant as dynamic power consumption. This presents a considerable challenge in power management, as reducing leakage power is critical for achieving energy efficiency in modern electronic devices. To address this issue, we introduce a novel circuit structure technique cascade leakage transistor (CLT) in this dissertation. This technique integrates advanced low-leakage methods with the lector technique, specifically targeting the CMOS inverter design implemented at the 45 nm technology node using Cadence software.

The CLT technique involves using two cascade leakage transistors to control the transistor on and off state of P type pull up and N type pull down of the CMOS inverter. This configuration not only helps manage leakage currents but also ensures the correct peak-to-peak waveform due to farced stack transistors of the input and output signals. The forced stack technique is instrumental in this design, significantly reducing static leakage power dissipation. While the propagation delay in the proposed design is higher than that of conventional CMOS inverters, this trade-off is necessary. It allows us to achieve a substantial reduction in leakage power, which is diminished by approximately 59.84% and total power reduced to 24%.

Figures, specifically Figure 5.1 and Figure 5.3, illustrate the proposed CLT circuit design and the corresponding output waveforms. In our implementation, the total power consumption, including these components, is detailed in Chapter 7 Table 7.1. We extended our proposed CLT approach to a NAND2 circuit and found it to consume significantly less static power and total power compared to a conventional NAND2 circuit also for universal gates and half adder table 7.3. This demonstrates the versatility and effectiveness of the CLT technique in various CMOS circuit designs, providing a comprehensive solution for reducing power consumption in advanced nanometer-scale technologies.

Power Dissipation of CLT NAND2 has 32.83% lower power dissipation compared to CMOS NAND2. Delay of CLT NAND2 has 43.42% higher delay compared to CMOS NAND2. Power-Delay Product (PDP) of CLT NAND2 has a 3.12% higher PDP compared to CMOS NAND2 .

Power Dissipation of The HALF ADDER CLT has 25.21% lower power dissipation compared to HALF ADDER CMOS (12T). also, Delay of The HALF ADDER CLT has 44.22% higher delay compared to HALF ADDER CMOS (12T). Power-Delay Product (PDP) is The HALF ADDER CLT has 8.46% lower PDP compared to HALF ADDER CMOS (12T).

By adopting the CLT approach at 45nm, designers can achieve a substantial reduction in leakage power while maintaining acceptable performance levels minimum 20 %. This balance is vital for the design of energy-efficient integrated circuits, especially in situations Where power usage is a key problem. The ideas and methodologies presented in this dissertation contribute to current efforts to improve power efficiency in CMOS technology, paving the path for more environmentally friendly and high-performing electronic gadgets.

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