

Comparative analysis of FD-FVF and DTMOS- Based Low Voltage High-Performance VDTAs Using 28nm FDSOI and 180nm Bulk MOS Technologies

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In Partial Fulfilment Of the Requirements For The
Degree of

MASTER OF TECHNOLOGY

in

VLSI Design and Embedded Systems

by

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(2K22/VLS/01)

Under The Supervision Of

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MAY, 2024

UNDERTAKING

I declare that the work presented in this project titled “**Comparative analysis of FD-FVF and DTMOS-Based Low Voltage High-Performance VDTAs Using 28nm FDSOI and 180nm Bulk MOS Technologies**” submitted to the **Department of Electronics & Communication Engineering, Delhi Technological University, Delhi** for the award of the **Master of Technology** degree in **VLSI Design and Embedded Systems** is my original work. I have not plagiarized or submitted the same work for the award of any other degree. In case this undertaking is found incorrect, I accept that our degree may be unconditionally withdrawn.

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CERTIFICATE

This is to certify that the work contained in the project titled “**Comparative analysis of FD-FVF and DTMOS-Based Low Voltage High-Performance VDTAs Using 28nm FDSOI and 180nm Bulk MOS Technologies**” submitted by **Ankit Raj** in the partial fulfilment of the requirement for the award of Master of Technology in Signal Processing and Digital Design to the Electronics & Communication Engineering Department, Delhi Technological University, Delhi, is a bonafide work of the student carried out under my supervision.

Date:

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Abstract

This paper introduces comparative analysis two innovative low voltage, high performance Voltage Differencing Transconductance Amplifiers (VDTAs) implemented using FDSOI technology and Bulk mos. The first VDTA incorporates a Fully Differential Flip Voltage Follower, which enables output currents exceeding the biasing current, leading to enhanced transconductances and gain. The second VDTA builds on the first by employing a DTMOS structure, leveraging body effects to further boost performance while operating at lower supply voltages and consuming less power. The designs utilize Fully Depleted Silicon on Insulator (FDSOI) devices and are implemented using Cadence Virtuoso with 28 nm MOS technology. Simulation results demonstrate that at a biasing current of 10 μA , the first VDTA ($\pm 0.7\text{ V}$) achieves a transconductance of 559.803 μS , a gain of 15.1 DB, and power dissipation of 116.1 μW , whereas the second VDTA ($\pm 0.7\text{ V}$) achieves a transconductance of 649.065 μS , a gain of 18.85 DB, and power dissipation of 98.90 μW , which shows a drastic improvement over Bulk Mos.

ACKNOWLEDGEMENT

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List of Abbreviations used

BP – Band Pass

CM – Current Mode

CC-Current Conveyor

FDSOI-Fully depleted silicon on insulator

CDTA-Current differencing transconductance amplifier

MISO-Multiple Input single input.

SoC-System on Chip

FD-FVF- Fully Differential Flip voltage follower

HP – High Pass

LP – Low Pass

BR – BAND REJECT

BS – BAND STOP

OTA - Operational Transconductance Amplifiers

VDTA – Voltage Differencing Transconductance Amplifier

VM – Voltage Mode

CHAPTER 1

INTRODUCTION

1.1 Study Overview

Integrated circuits have become smaller because of CMOS device downscaling that is ongoing. The call for active components in analogue signal processing with low supply voltage and occasional power intake has appreciably increased because of this improvement. Numerous active elements have been proposed, which include Operational amplifier, Operational Trans conductance Amplifier , Current supply generator, Current Differencing Trans conductance Amplifier , and Voltage Differencing Trans conductance Amplifier .Because VDTA incorporates wonderful trans conductance g_1 and g_2 that can be independently managed with the aid of outside biasing currents, it has a bonus over the opposite energetic factors. A unmarried VDTA may be used to recognize quite a few circuits, which includes oscillators, filters, Freq. Dep. Negative Resistors, and so forth. It also can be utilised to enforce programs for the trans-admittance and trans-conductance modes. The Flip Voltage Follower (FVF), which has a sincere structure, team spirit gain, and splendid precision, is now broadly utilised as a essential aspect in low voltage-electricity oscillators, amplifiers, filters and so on. By adopting the Dynamic Threshold MOS (DTMOS) technology, this frame effect can be substantially corrected and used to enhance the circuit's capability. It now not only complements circuit capability but also lowers the circuit's need for deliver voltage. This document makes use of a low voltage vdtA primarily based on a Fully Differential-Flip Voltage Follower that operates at low deliver voltage and gives excessive present day, trans conductance and bandwidth. Further enhancing the performance of the Structure-1 vdtA through raising its trans conductance and lowering deliver voltages is the DTMOS based FD-FVF Structure-2 VDTA. Utilising the two VDTAs, MIXED-MODE QUADRATURE OSCILLATOR may be created similarly.

1.2 Importance of VDTA

The Voltage Differencing Transconductance Amplifier (VDTA) holds significant importance in analog signal processing and integrated circuit design. Here are some reasons why VDTAs are considered important:-

- ✧ Versatility: VDTAs offer a wide range of functionality and can be used in various analog circuit applications. They can be utilized as voltage amplifiers, current amplifiers, active filters, oscillators, and more. This versatility allows for flexible circuit design and the implementation of complex analog signal processing systems.
- ✧ High linearity: VDTAs exhibit excellent linearity, which is crucial for accurate signal reproduction and maintaining the integrity of the original input signal. This makes them suitable for applications that require high fidelity, such as audio amplification and communication systems.
- ✧ Low power consumption: VDTAs typically consume low power, which is advantageous in applications where energy efficiency is critical, such as portable devices and battery-powered systems. Low power consumption also helps reduce heat dissipation and extends the battery life of portable devices.
- ✧ Compatibility with low voltage supply: VDTAs can operate with low supply voltages, making them suitable for low-voltage integrated circuits. This is particularly important in modern electronics, where power supply voltages continue to decrease due to advancements in semiconductor technology.
- ✧ Circuit simplicity: VDTAs can be implemented with relatively simple circuit topologies, requiring fewer components compared to other amplifier configurations. This simplifies the overall system design, reduces the complexity of the circuitry, and can lead to cost savings in terms of manufacturing and production.
- ✧ Integration with complementary metal-oxide-semiconductor (CMOS) technology:

VDTAs can be easily integrated into CMOS technology, which is widely used in modern integrated circuits. This compatibility facilitates their integration into complex systems-on-chip (SoCs) and allows for efficient use of chip area.

Overall, the importance of VDTAs lies in their ability to provide versatile, high-performance analog signal processing capabilities while offering advantages such as low power consumption, and compatibility with modern integrated circuit technologies.

CHAPTER 2

DESIGN OVERVIEW

Elements of VDTA

2.1 Differential Flipped Voltage Follower

The Flipped Voltage Follower is a unity gain voltage follower with shunt feedback. As previously mentioned, various differential structures can be created using the FVF, enabling outputs in either current or voltage form. These structures exhibit class-AB behavior since their output currents can be adjusted through a biasing current source (I_B), which is significantly lower than the maximum output current. This characteristic makes FVF-based circuits highly appealing for low-power applications. Figure 2.1 illustrates the FD-FVF structure. In this circuit, assuming the body effect is negligible, the output drain currents (I_{DM5} and I_{DM6}) are proportional to the differential input voltage ($V_P - V_N$) applied to the gate terminals of MOSFETs M_1 and M_2 . The FD-FVF offers fully differential operation, a high common mode rejection ratio (CMRR), and output currents (I_{DM5} and I_{DM6}) that can be equal to or exceed I_B . If a common mode signal is applied ($V_P = V_N$) and MOSFETs M_1 , M_2 , M_5 , and M_6 are matched, then I_{DM5} and I_{DM6} will both equal I_B . Variations in $V_P - V_N$ lead to corresponding changes in the output currents I_{DM5} and I_{DM6} .

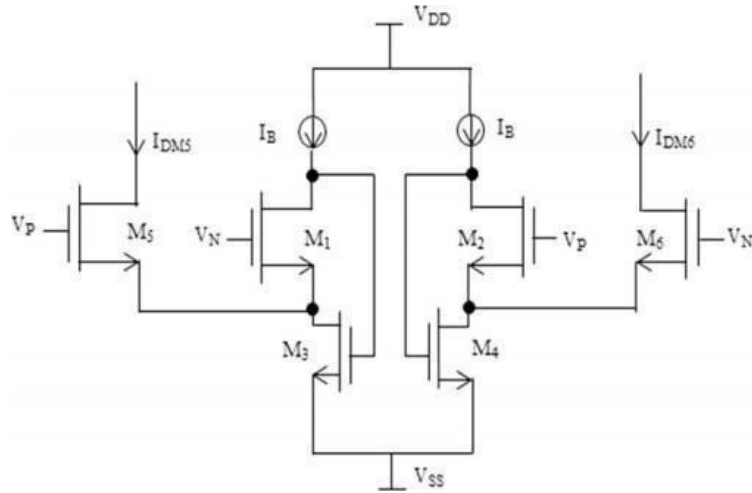


Fig 2.1:- Differential Flip Vol. Follower [10]

2.2. Voltage Differencing Transconductance Amplifier

The Voltage Differencing Transconductance Amplifier (VDTA) is an electronic amplifier that integrates the functions of a voltage amplifier and a transconductance amplifier, making it widely utilized in analog signal processing.

A VDTA features a differential input stage that amplifies the voltage difference between its two inputs, coupled with a transconductance stage that converts this voltage difference into a proportional current. Typically, the transconductance stage uses active components like transistors for this conversion.

The VDTA offers numerous benefits, including high linearity, low power consumption, and the capability to operate at low supply voltages. It is employed in various analog circuits such as filters, oscillators, mixers, and instrumentation amplifiers.

The circuit configuration and design specifics of a VDTA can vary based on the application and the desired performance characteristics.

2.3 Dynamic Threshold MOSFET (DTMOS)

The primary benefit of DTMOS technology is its capability to adjust the threshold voltage to enhance circuit performance, reduce power consumption, or achieve other desired characteristics. Fully Depleted Silicon On Insulator (FD-SOI) is a type of DTMOS transistor that demonstrates high threshold characteristics when off, minimizing leakage, while acting as a low-threshold device for high current drivability under low voltage conditions. This dual behavior makes it highly suitable for modern ultra-low-voltage analog circuits. As illustrated in Fig. 2.2, the gate and body terminals of a PMOS transistor are connected without requiring additional processing steps, enabling production using standard CMOS technology. Fig. 2.2 shows the DTMOS transistor and its commonly used circuit symbol. Although this configuration has been documented in earlier works, they provide a detailed explanation of the device's operation. The concept involves connecting the gate and body of the transistor to dynamically alter the threshold voltage, leveraging their relationship.

$$V_t = V_{t0} - \gamma(\sqrt{2|\phi_F|} - \sqrt{2|\phi_F| - V_{BS}})$$

where V_{t0} is the threshold voltage at zero body bias and is given as

$$V_{t0} = 2|\phi_F| + V_{FB} + \sqrt{2qN_a\epsilon_s 2|\phi_F|/C_{ox}}$$

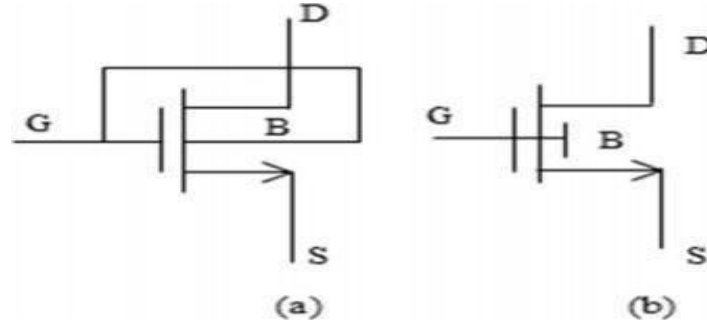


Fig 2.2:- Dynamic Threshold Mosfet transistor and symbol. [1]

2.4 Fully Depleted Silicon On Insulator

Fully depleted silicon on insulator (FD-SOI) is an advanced semiconductor technology designed to increase transistor performance and efficiency. It features a very thin layer of buried oxide under a very thin layer of silicon, which forms the transistor channel. This design reduces various small-path effects and parasitic capacitances found in conventional bulk CMOS transistors. FD-SOI transistors provide faster switching speeds due to their shorter effective channel length and steeper subthreshold gradient. Low voltage is also provided to improve the efficiency of power supply. The buried oxide provides excellent source and drain protection, reduces corrosion and increases overall device efficiency, making FD-SOI ideal for today's low-power and high-performance applications. Structure shown in Fig. : 2.3

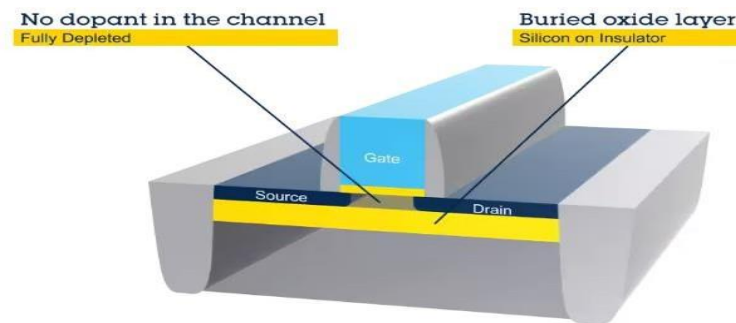


Fig 2.3:-FDSOI device. [11]

FD-SOI transistors address several short-channel effects common in bulk CMOS architectures. In bulk CMOS transistors, parasitics between the drain, source, and substrate cause problems such as gate-induced drain leakage current, drain-induced barrier lowering, and threshold voltage variability. The buried oxide layer in FD-SOI transistors acts as a shield for the source and drain, reducing these parasitic capacitances. FD-SOI transistors have a shorter effective channel length compared to bulk silicon CMOS at the same technology node. This shorter channel reduces the electron transit time from the source to the drain, resulting in faster transistor operation. Additionally, FD-SOI transistors exhibit a steeper subthreshold slope (SS), enabling quicker turn-on and lower threshold voltage. As a result, they can achieve the same performance at a lower supply voltage than conventional transistors. In contrast, bulk CMOS transistors face significant subthreshold leakage current at lower technology nodes, leading to leakage even in standby mode.

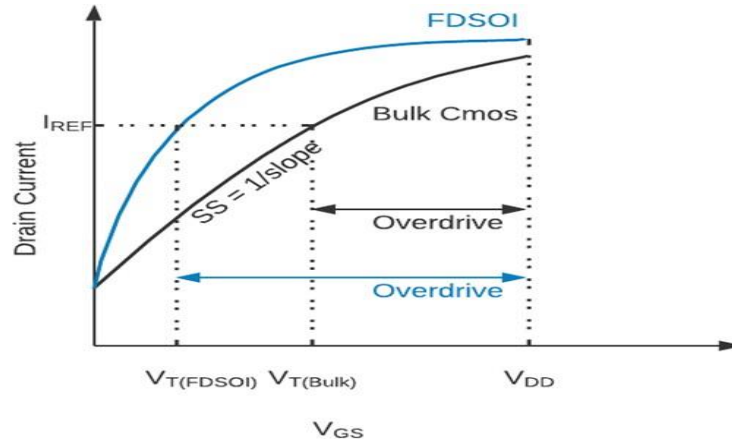


Fig. 2.4: Subthreshold slope in FDSOI[11]

In bulk CMOS, applying voltage to the substrate can improve transistor performance. Forward body biasing lowers the threshold voltage (V_{th}), aiding in the formation of the channel between the source and drain, and thereby speeding up transistor switching. Conversely, reverse body biasing raises the effective V_{th} , which reduces leakage power consumption. However, in bulk technology, the effectiveness of body biasing is constrained by parasitic current leakage and short-channel effects.

2.4.1 Bulk CMOS vs FDSOI

FD-SOI inherently provides superior transistor electrostatic properties compared to conventional bulk technology. The buried oxide reduces the parasitic capacitance between source and conduit, effectively limiting electron flow from the source to the conduit, and significantly reduces performance-degrading leakage

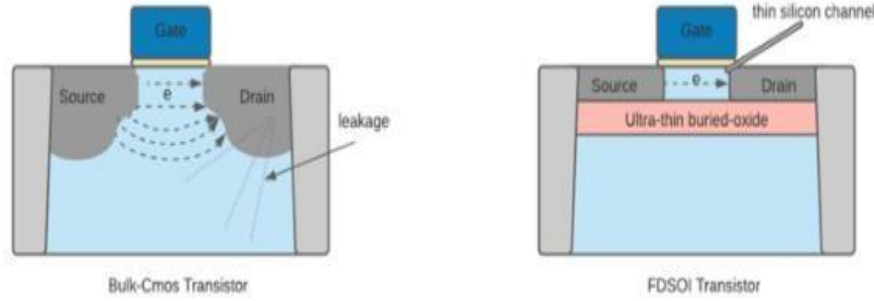


Fig. 2.5: Bulk-CMOS vs FDSOI device[11]

2.5 Biasing Circuit

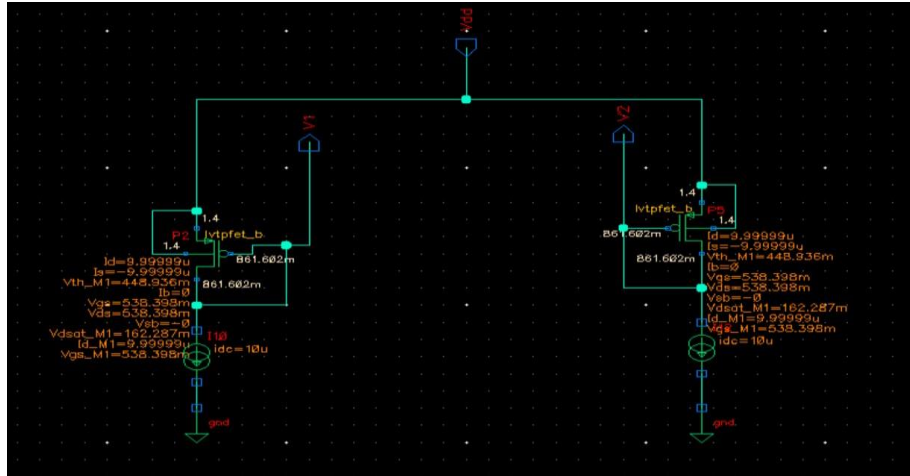


Fig. 2.6 : Biasing current mirror circuit generating 10µA current

To generate a continuous current of 10 μ A, two modernday replicate circuits were employed. These circuits have been meticulously designed with suitable width and length to make sure that the preferred biasing voltage changed into executed, thereby facilitating the generation of the specified 10 μ A current.

The output nodes, categorized V1 and V2, served as biasing enter voltages for the VDTA I and II structures. This configuration changed into essential in allowing the VDTA structures to preserve a regular 10 μ A current, way to the ideal sizing of the additives.

CHAPTER 3

VOLTAGE DIFFERENTIATING TRANSCONDUCTANCE AMPLIFIER

3.1 Introduction

The Voltage Differential Transconductance Amplifier (VDTA) is a specialized type of operational amplifier that offers unique advantages and features compared to conventional operational amplifiers. It has been gaining significant attention in recent years due to its exceptional performance characteristics and its suitability for various applications in analog signal processing, instrumentation, communication systems, and biomedical devices. This introduction provides an overview of VDTA, highlighting its significance, working principles, and potential applications.

3.2 Background

Operational amplifiers (op-amps) are crucial building blocks in analog circuits [2], widely used to amplify and process analog signals. Traditional op-amps are voltage amplifiers, where the output voltage is directly proportional to the input voltage. While they have been highly successful in numerous applications, there is a need for specialized amplifiers that can address specific challenges, such as wide high linearity, dynamic range, low power consumption, and compact size.

3.3 Need for VDTA

The VDTA emerged as a specialized amplifier to overcome limitations associated with conventional op-amps. It offers an alternative approach by providing transconductance amplification, where the output current is linearly related to the voltage difference between its two input terminals. This unique characteristic makes VDTA well-suited for applications requiring voltage-to-current conversion, such as analog signal processing and current-mode circuits.

3.4 Working Principles

The VDTA consists of multiple transistors and passive components carefully arranged to achieve voltage-to-current conversion. It typically includes a differential input stage, a transconductance stage, and an output stage. The transconductance stage converts this voltage difference into a proportional transconductance, which is the ratio of the output current to the voltage difference. Finally, the output stage buffers and delivers the converted current to the load.

3.5 Circuit Description

The symbol for the Voltage Differencing Transconductance Amplifier (VDTA) circuit is illustrated in Figure 3.2. The input signals to the VDTA are denoted as V_P and V_N , while its output is composed of four terminals: Z_+ , Z_- , X_+ , and X_- , all exhibiting high impedance. In an ideal scenario, the interconnection between these terminals can be represented using conventional notation as shown in Fig. 3.1.

$$\begin{bmatrix} I_{Z+} \\ I_{Z-} \\ I_{X+} \\ I_{X-} \end{bmatrix} = \begin{bmatrix} g_{v1} & -g_{v1} & 0 \\ -g_{v1} & g_{v1} & 0 \\ 0 & 0 & g_{v2} \\ 0 & 0 & -g_{v2} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \end{bmatrix}$$

Figure 3.1 Conventional notation of VDTA[10]

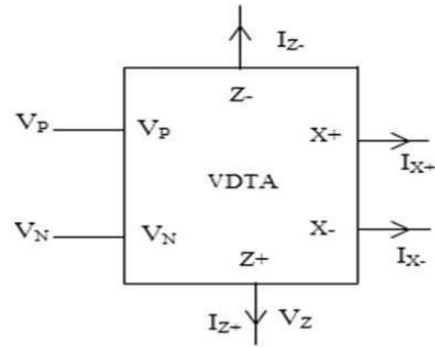


Figure 3.2 Symbol of VDTA[10]

3.6 Operation

The operation of a Voltage Differential Transconductance Amplifier involves the conversion of a voltage difference between its input terminals into proportional output current:

Differential Input Stage: The VDTA typically consists of a differential input stage that amplifies voltage differences between its input terminals. This stage comprises transistors configured in a differential configuration. The input voltage is applied to the bases or gates of these transistors, and their outputs are connected to subsequent stages.

Transconductance Stage: The amplified voltage difference from the input circuit is then fed into a transconductance stage. This stage converts the voltage difference into a proportional transconductance, which represents ratio to output current and input voltage difference. The transconductance stage may utilize active components, such as transistors operating in the linear region, to achieve desired transconductance characteristic.

Out Stage: The transconductance stage drives the output stage, which buffers and delivers the converted current to the load. The output stage may include additional transistors or current mirrors to provide sufficient current drive capability. It ensures that the output current accurately represents the input voltage difference, taking into account the transconductance gain of the VDTA.

During operation, the VDTA amplifies the voltage difference applied to its inputs, converts it into a proportional transconductance, and delivers the converted current to the output. The transconductance gain establishes the connection between input voltage difference and the output current, and maintaining linearity is a critical attribute for precise voltage-to-current conversion. It's important to note that specific implementation, characteristics of VDTAs may change depending on the design, technology, and intended applications. Therefore, detailed analysis and understanding of

the circuit topology, component selection, and biasing requirements are necessary for the successful operation of VDTAs in specific applications.

3.7 Design and implementation

The FD-FVF based VDTA is shown in Figure 4. Two dual output Operational transconductance amplifier [3] are used for this structure. In Figure 3.3, MOSFETs M1-M10, M21 and M22 are two primary output OTAs and M11-M20, M23 and M24 are two secondary OTAs. trans conductance (g_{v1} and g_{v2}) a in the Structure-1 VDTA structure is equal to the trans conductance of individual OTAs g_{v1} for the Structure-1 VDTA To obtain (1st dual output equal to the cross conductor of the OTA) .

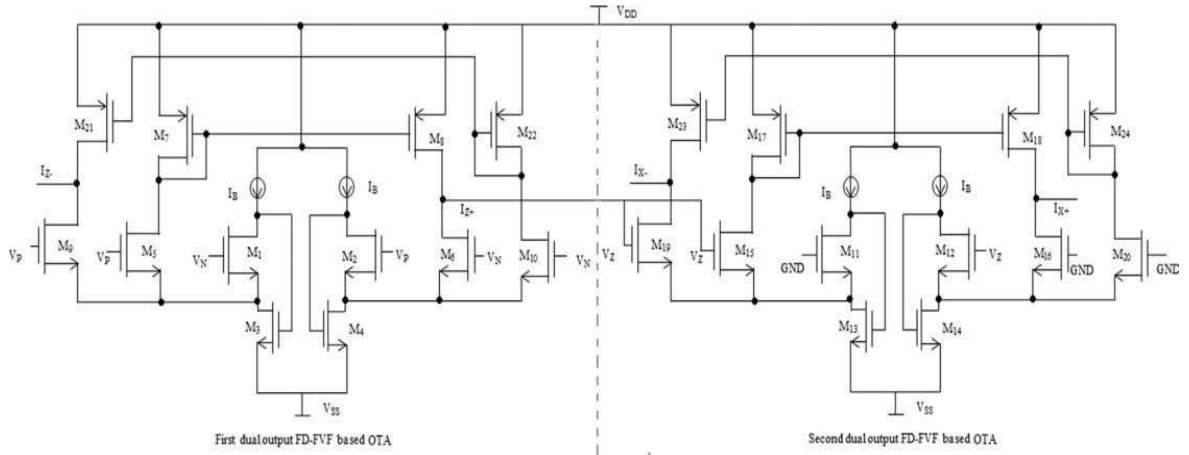


Fig 3.3:- FD-FVF based VDTA Structure-1 [10]

In the Structure-1 VDTA (Figure 3.3), the physical effects of the MOSFETs have been neglected. Considering these physical effects, non-zero V_{BS} values for MOSFET M1, M2, M5, M6, M9, M10, M11, M12, M15, M16, M19 and M20 will slightly degrade circuit performance in Figure 3.4 DT MOS a based FD-FVF VDTA (Schedule-2). is shown. This circuit has utilized the body effect of the proposed-I circuit in such a way that the circuit is more efficient. Furthermore, the energy consumption also decreases. The proposed VDTA-II consists of MOSFETs M1, M2, M5, M6, M9, M10, M11, M12, M15, M16, M19 and M20 DT MOS transistors. DT MOS transistors have higher cross-conductivity than conventional MOSFETs.

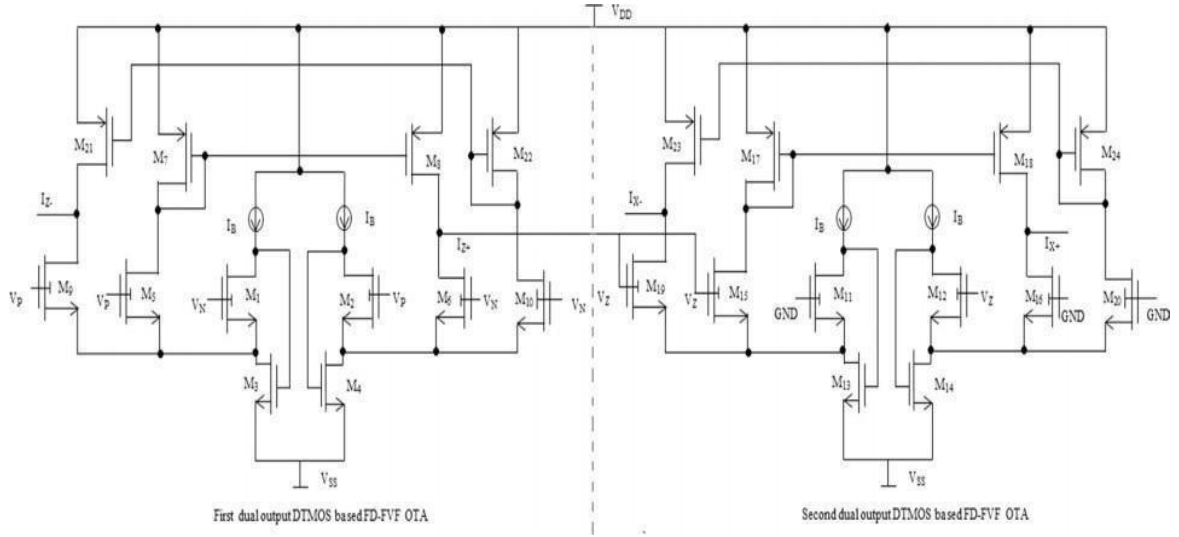


Fig 3.4:- DT-MOS based FD-FVF based VDTA [10]

3.8 Advantages of VDTA

Voltage-to-Current Conversion: The primary advantage of VDTAs is their ability to convert voltage signals in current signals. This char. is handy in various applications where voltage-to-current conversion is required, such as current-mode circuits and sensor interfaces.

High Linearity: VDTAs offer high linearity in voltage-to-current conversion, ensuring accurate and faithful reproduction of the input voltage difference. This characteristic is essential for maintaining signal integrity and minimizing distortion in analog signal processing applications.

Wide Bandwidth: VDTAs typically provide a wide bandwidth, enabling the amplification and processing of high-frequency signals. This makes them suitable for applications involving high-speed data transmission, RF circuits, and communication systems.

Compatibility with Current-Mode Circuits: VDTAs are well-suited for current-mode signal processing circuits. They can seamlessly integrate into current-mode circuits, offering advantages such as higher speed, reduced signal-to-noise ratio, and improved linearity compared to voltage- mode circuits.

Low Power Consumption: VDTAs can be designed with low power consumption, making them suitable for energy-efficient designs and portable devices. Their low power requirements contribute to extended battery life and reduced energy consumption in battery-powered applications.

3.9 Limitations of VDTA

Limited Voltage Gain: VDTAs typically have limited voltage gain compared to voltage amplifiers or operational amplifiers. They are primarily designed for voltage-to-current conversion rather than voltage amplification. Additional stages or circuitry may be required to achieve higher voltage gains if needed in a particular application.

Sensitivity to Component Variations: VDTAs can be sensitive to component variations, such as variations in transistor parameters or resistor values. This sensitivity can impact their performance and may require careful component selection or compensation techniques to ensure consistent and reliable operation.

Temperature Dependence: The performance of VDTAs may be affected by temperature variations. Changes in temperature can impact the operating characteristics, linearity, and gain of the amplifier. Temperature compensation techniques or proper thermal management may be necessary in temperature-sensitive applications.

Noise Considerations: Like any electronic amplifier, VDTAs can introduce noise into the system. The noise performance of VDTAs, including input-referred noise and noise figure, should be considered in applications where signal-to-noise ratio is critical. Careful design and optimization are required to minimize noise contributions.

CHAPTER 4

APPLICATIONS BASED ON VDTA

4.1 Filter based on VDTA structure.

A MISO (Multiple Input, Single Output) filter processes multiple input signals into a single output signal. They are used in applications such as wireless communication and signal processing to improve signal quality, reduce noise, and extract specific information. MISO filters can be linear or nonlinear, and can use adaptive algorithms to adjust parameters in real time. Although they improve the quality of the signals and provide greater flexibility, their design and implementation can be complex and resource intensive. Circuit analysis yields voltage-mode biquadratic transfer function given as [11]:

$$V_{out}(s) = \frac{\frac{g_{v1}g_{v2}}{C_1C_2}V_{in1}(s) - \frac{s g_{v2}}{C_1}V_{in2}(s) + s^2 V_{in3}(s)}{s^2 + \frac{s}{RC_1} + \frac{g_{v1}g_{v2}}{C_1C_2}} \quad [5]$$

Eq. shows that miso filter can be designed in different basic filters which we use in our daily life shown below.

$$\begin{aligned} \text{LPF : } & V_{in1} = V_{in} \text{ and } V_{in2} = V_{in3} = 0; \\ \text{BPF : } & V_{in2} = V_{in} \text{ and } V_{in1} = V_{in3} = 0; \end{aligned} \quad [1]$$

$$\begin{aligned} \text{HPF : } & V_{in3} = V_{in} \text{ and } V_{in1} = V_{in2} = 0; \\ \text{BRF : } & V_{in1} = V_{in3} = V_{in} \text{ and } V_{in2} = 0; \end{aligned}$$

$$\text{APF : } V_{in1} = V_{in3} = V_{in} \text{ and } V_{in2} = V_{in}. \quad [1]$$

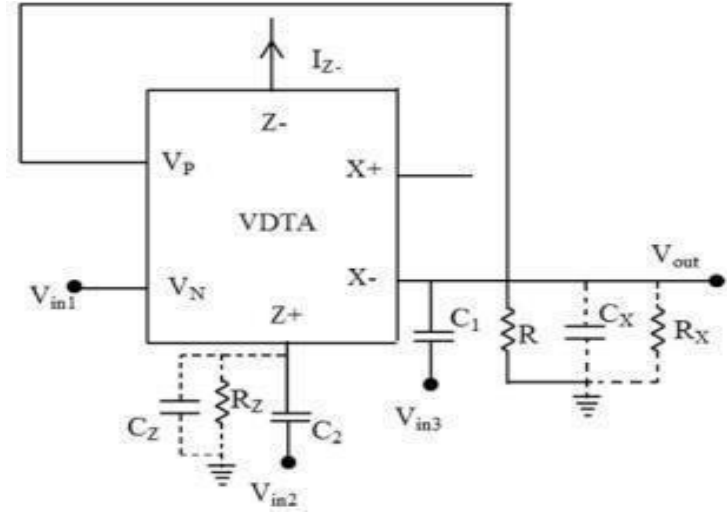


Fig. 4.1. MISO filter based on proposed VDTAs. [6]

4.2 Mixed Mode Quadrature Oscillator

A mixed-mode quadrature oscillator generates two sinusoidal outputs with a 90-degree phase difference in both voltage and current forms. It is used in communication systems, modulation and demodulation processes, and measurement systems. These oscillators typically utilize operational amplifiers or transconductance amplifiers in their design to achieve the required phase shift and signal generation.

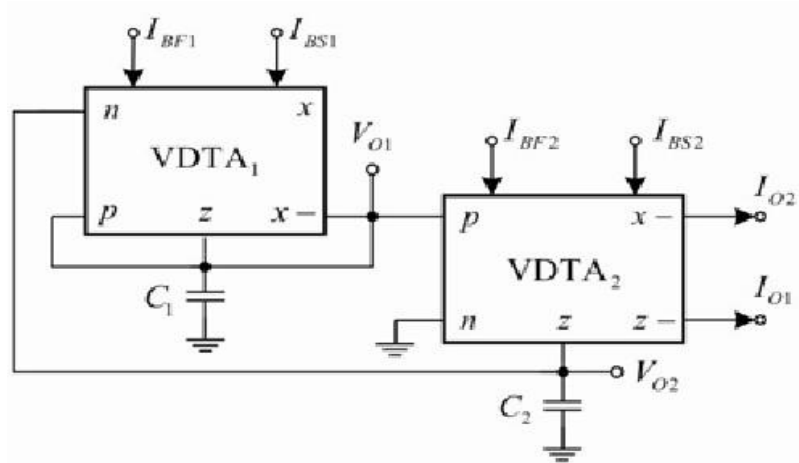


Fig. 4.2. Mixed mode quadrature oscillator [12]

CHAPTER 5 SIMULATIONS & RESULTS

STRUCTURE VDTA 1 AND VDTA 2 [15]

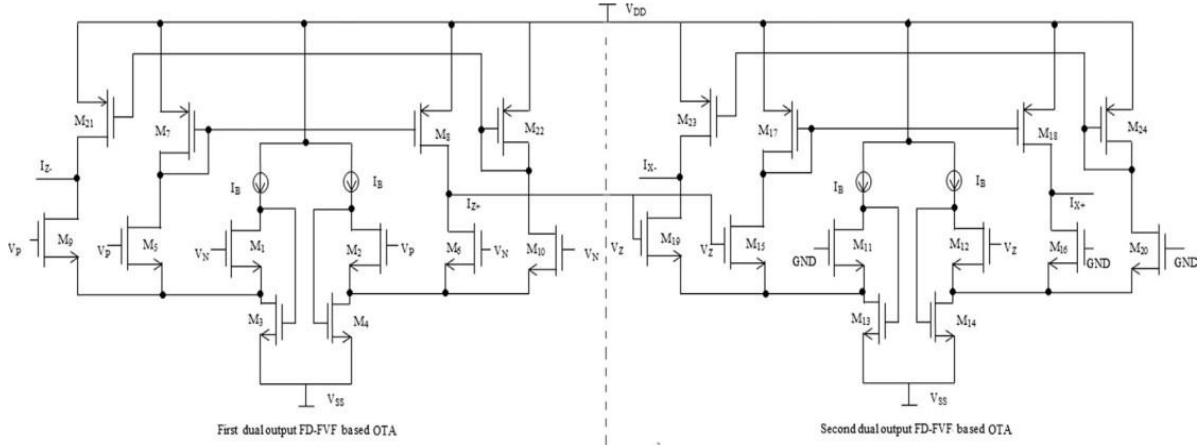


Fig. 5.1. VDTA I STRUCTURE[10]

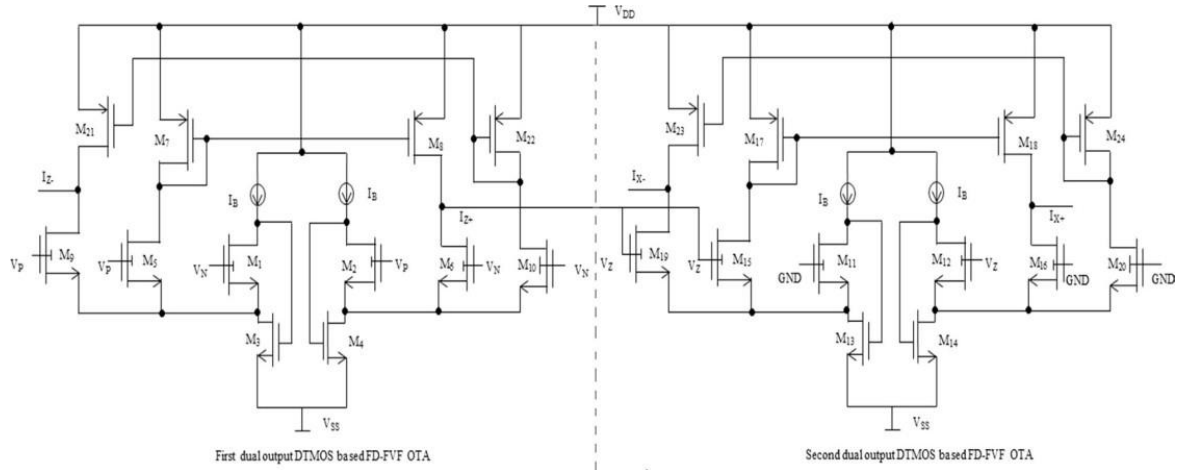


Fig. 5.2. VDTA II DTMOS STRUCTURE[10]

5.1 COMPARATIVE ANALYSIS BULK VS FDSOI

STRUCTURE (Bulk MOS) 180nm Node	Supply Voltage	Maximum Current	gm	Gain (Db)	Average Power Consumption
VDTA I	± 0.7 V	60 μ A	415.62 μ S	11	145.43 μ W
VDTA II (DTMOS)	± 0.7 V	80 μ A	422.89 μ S	13	102.14 μ W

Table I:- Bulk Mos Results [10]

STRUCTURE (FDSOI Mos) 28nm Node	Supply Voltage	Maximum Current	gm	Gain (Db)	Average Power Consumption
VDTA I	± 0.7 V	115 μ A	559.80 μ S	15	116.1 μ W
VDTA II (DTMOS)	± 0.7 V	105 μ A	649.06 μ S	18.85	98.90 μ W

Table II :- FDSOI Mos Results

We can clearly see the improvement in performance after we used FDSOI Mos. There is improvement in transconductance, gain, Avg. power consumption. The supply voltage was kept same under the simulation and proper sizing was done to get the best results.

Design Parameters Comparison

Component name (Bulk MOS)[10]	VDTA I[10]	VDTA II[10]
vdd	+0.7 V	+0.7 V
vss	-0.7 V	-0.7 V
Ib	10 μ A	10 μ A
Mos 1-Mos 6, Mos 11-Mos 16, Mos 19, Mos 20	7.2 μ m / 0.36 μ m	7.2 μ m / 0.36 μ m
Mos 7, Mos 8, Mos 17, Mos 18, Mos 21- Mos 24	14.4 μ m / 0.36 μ m	14.4 μ m / 0.36 μ m

Component name (FDSOI MOS)[11]	VDTA I[10]	VDTA II[10]
vdd	+0.7 V	+0.7 V
vss	-0.7 V	-0.7 V
Ib	10 μ A	10 μ A
Mos 1-Mos 5, Mos 7,Mos 22,Mos 10,Mos 11- Mos 15,Mos 20,Mos 24,Mos17	1 μ m / 0.2 μ m	1 μ m / 0.2 μ m
Mos 9,Mos 6,Mos 19,Mos 16	3 μ m / 0.2 μ m	3 μ m / 0.2 μ m
Mos 21,Mos 8,Mos 23,Mos 18	10 μ m / 0.2 μ m	10 μ m / 0.2 μ m

5.2 FDSOI SIMULATION RESULTS

STRUCTURE I VDTA

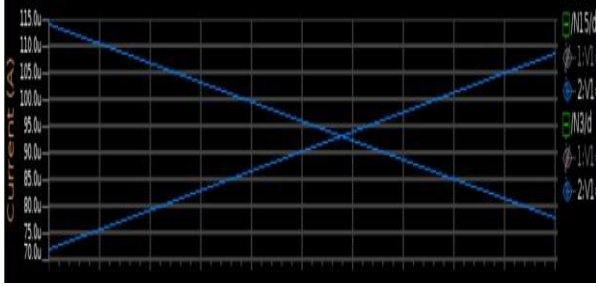


Fig. 5.3 : Current Response

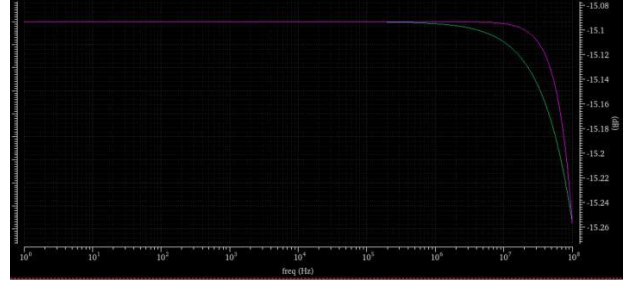


Fig. 5.4 : Gain VS Frequency

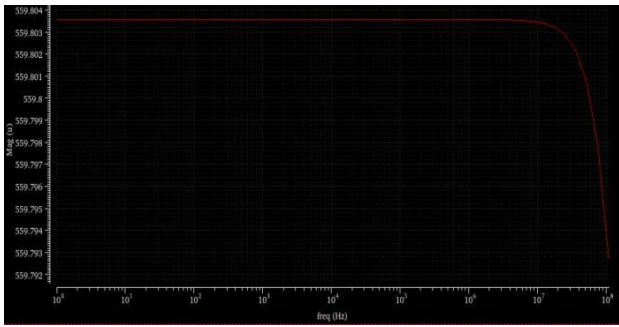


Fig. 5.5 : Transconductance vs frequency

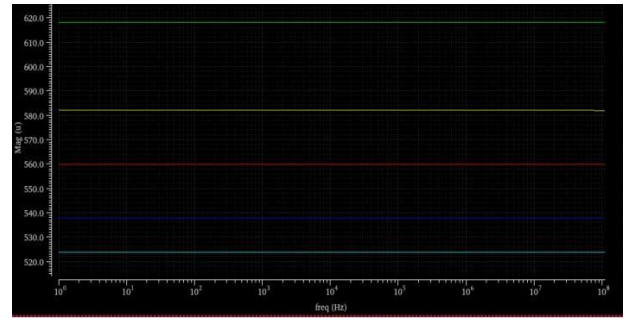


Fig. 5.6 : gm response on different corners

STRUCTURE II VDTA

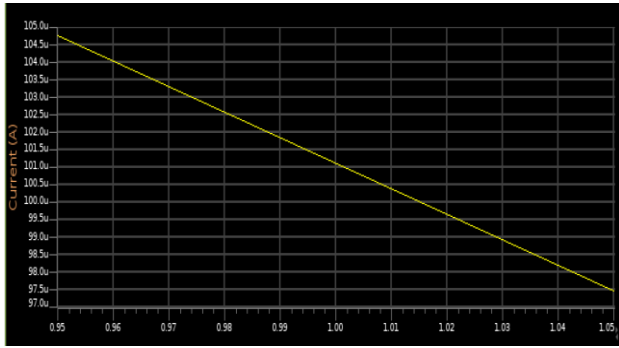


Fig. 5.7 : Current Response

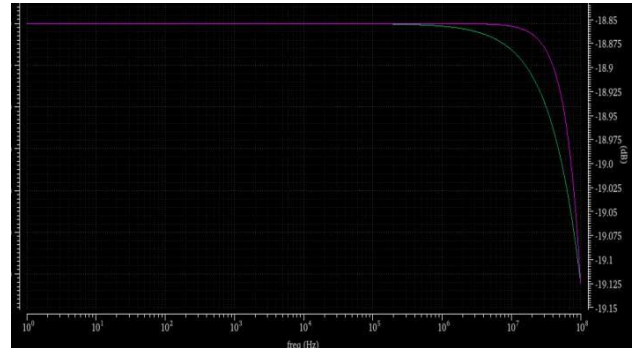


Fig. 5.8 : Gain VS Frequency

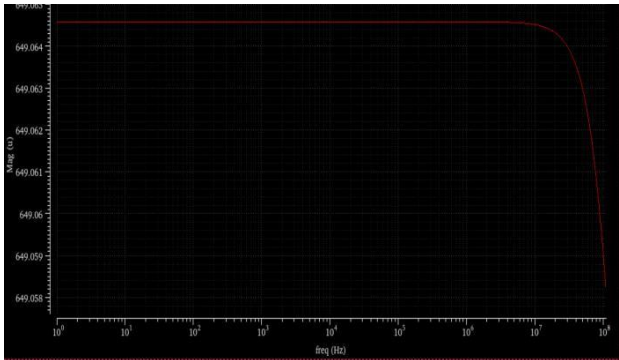


Fig. 5.9 : Transconductance vs frequency

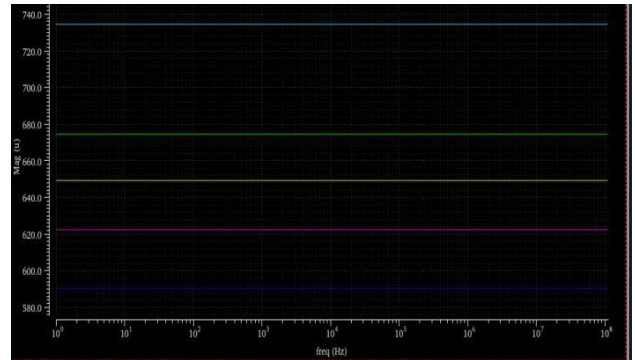


Fig. 5.10 : gm response on different corners

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

Two low-power VDTA structures were implemented using FDSOI devices at a 28nm technology node. Compared to bulk technology, FDSOI provides significantly higher current, higher gain, and higher transconductance. We can see the design parameter comparison width was kept very small in FDSOI MOS compared to Bulk MOS, still better performance in FDSOI MOS was observed compared to Bulk MOS. In the bulk technology implementation [15], the design used the same supply voltage but with a 180nm technology node. Transitioning to FDSOI at a 28nm node resulted in a drastic improvement in performance. Additionally, power consumption was reduced, with FDSOI devices delivering high current and gain while consuming less power. Filters and oscillators can be designed using VDTA, and the use of FDSOI devices ensures lower power consumption .

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