CNTFET BASED DYNAMIC GDI COMBINATIONAL LOGIC CIRCUITS

A DISSERTATION REPORT

SUBMITTED IN PARTIAL FULFILMENT OF THE
REQUIREMENTS FOR THE AWARD OF THE DEGREE

OF

MASTER OF TECHNOLOGY

IN

VLSI DESIGN AND EMBEDDED SYSTEMS

SUBMITTED BY

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CANDIDATE'S DECLARATION

I, **Bhargav Singh (2K22/VLS/02)** students of MTech **(VLSI Design and Embedded Systems)**, hereby declare that In partial fulfilment of the requirements for the award of a Master of Technology degree, we have submitted a Project report on **CNTFET Based Dynamic GDI Combinational Logic Circuits** to the Department of Electronics and Communication Engineering at Delhi Technological University. This report is original and has not been copied from any source without proper citation. There has never before been a degree, diploma, associateship, fellowship, or other title or honour that is comparable to this one awarded for the work done here.

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CERTIFICATE

I hereby attest that the project report on the topic **CNTFET Based Dynamic GDI Combinational Logic Circuits** , submitted by **Bhargav Singh (2K22/VLS/02)** of the Electronics and Communication Department at Delhi Technological University, Delhi, partially fulfils the requirements needed to be awarded a Master of Technology degree. The report is a record of the project work that the student completed under my supervision. To the best of my knowledge, neither this university nor any other has accepted this work in whole or in part for a degree or diploma.

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M.TECH: VLSI Design & Embedded System

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ABSTRACT

In this project, a Combinational circuits based on the proper combination of dynamic logic style and Gate Diffusion Input (GDI) low-power technique is proposed in Carbon Nanotube Field Effect Transistor (CNFET) technology. This goal of this thesis Carbon Nano tube Field Effect Transistors (CNTFETs) based design using Dynamic Gate Diffusion Input(D-GDI) ,Using the proposed approach, the combinational logic circuits such as XOR , XNOR gates and MUX are implemented which results in a full-swing, Proposed full-adder cell in the CNFET technology. The proposed circuits For the designing and simulation of circuit purpose we have used Stanford CNTEFT model Verilog A with 32nm technology parameters.The design tool used for the simulation is Cadence Virtuoso Finally, the simulation results justify a good improvement in the major circuit performances such as power consumption, delay and power-delay product (PDP) parameters for the proposed full-adder, half subtractor , encoder circuit. The recommended Dynamic GDI technique appears to consume 28% less power than the standard approach, based on the data.

keywords — Cadence virtuoso, CMOS, VLSI, P-CNT, N-CNT, CNTFET,GDI ,DGDI

SWCNT, MWCNT, ALU.

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Chapter 01 INTRODUCTION

1.1 Overview

The design of low-power and high-speed digital integrated circuits has drawn the attention of designers more than any other in recent years due to the rapid advancements in the development of portable electronic devices, such as laptops, smart phones, and communication systems. In the past, electronics have demonstrated a consistent evolutionary trend: they have integrated more features and sophisticated functions into ever-smaller packages. Wave after wave of cutting-edge electronics made their way to customers as this trend developed, from those that sat on a desk to those that fit on a lap to those that fit in a pocket.

Mobile applications are starting to show up as a new market driver for the scaling of integrated circuits, thanks to the recent introduction of smartphones, mobile internet devices, and other portable consumer electronics. These applications require not only a tiny form factor and excellent performance, but also power efficiency to provide a wide range of functionality that enhances the user experience.

Future demands for quicker, smaller, and more power-efficient integrated circuits should be expected as ultra-mobile electronics and smaller sensor and communication electronics become more commonplace and integrated into our daily lives. Therefore, it is more crucial than ever to provide the technology necessary to allow power-efficient integrated circuits to scale for a very long time to come. Unfortunately, the International Technology Roadmap for Semiconductors (ITRS) [1] predicts that significant challenges will impede the continuous scaling of silicon-CMOS technologies in the relatively near future. Enforcing power-efficiency requirements makes the issue worse. As a result, a number of novel materials are being explored as silicon's replacement or complement.

Therefore, high performance digital integrated circuits are a result of Moore's Law and have compact chip sizes in addition to low power consumption and low propagation delays. However, because of significant physical constraints like high leakage currents, the consequences of small transistor channel lengths, and so on. Higher integration levels in CMOS technologies may encounter new challenges in sub-micron CMOS technologies. Some new technologies, like Quantum Cellular Automata (QCA), Single Electron Transistor (SET), and Carbon Nano-Tube Field Effect Transistor (CNFET), are introduced to address the aforementioned shortcomings.

Nonetheless, CNFETs are seen as a suitable substitute for CMOS technology in the design and implementation of high-speed, low-power digital integrated circuits within the tiny chip size range, among the previously mentioned developing technologies. Furthermore, they exhibit remarkably similar circuit behavior to that of CMOS technology. However, compared to traditional CMOS technology, CNFET technology exhibits a higher power-delay efficiency and benefits from a reduced power usage.

In the realm of nanoelectronics, carbon nanotube field-effect transistors, or CNTFETs, are a new technology that has several benefits over conventional silicon-based transistors. Carbon nanotubes (CNTs) are used as the channel material in CNTFETs because of its exceptional electrical qualities, which include strong mechanical strength, high carrier mobility, and outstanding thermal conductivity. Due to these features, CNTFETs may be able to function more quickly, more power efficiently, and more compactly than traditional metal-oxide-semiconductor field-effect transistors (MOSFETs).

Instead of a silicon layer, a single or many carbon nanotubes constitute the channel in a CNTFET. By adjusting the conductivity of the CNT channel, the gate electrode regulates the current flow between the source and drain.

➢ CNTFETs are promising for several reasons:

1. High Performance: CNTs have higher electron mobility than silicon, which can lead to faster transistor switching speeds and higher frequency operation.

2. Low Power Consumption: Due to their excellent electrical properties, CNTFETs can operate at lower voltages, reducing power consumption and heat generation.

3.Scalability: CNTFETs can be scaled down to smaller dimensions than silicon transistors, potentially extending Moore's Law beyond the limits of silicon technology.

4. Flexibility: Carbon nanotubes are flexible and can be used in flexible and wearable electronics.

However, challenges remain in the mass production and integration of CNTFETs, such as the precise placement and alignment of CNTs, the control of CNT chirality, and the development of reliable fabrication processes. Research is ongoing to address these issues and realize the full potential of CNTFETs in future electronic devices

➢ Applications of CNTFETs

1. High-Performance Computing Because of their low power consumption and high electron mobility, CNTFETs are ideal for high-performance computing applications. They can

potentially replace silicon transistors in CPUs and GPUs, leading to faster and more energy-efficient processors.

2. Flexible Electronics: Carbon nanotubes' mechanical flexibility makes CNTFETs suitable for flexible and wearable electronics. Applications include flexible displays, smart textile.

3. Nanoelectronic:high-frequency response of CNTFETs makes them suitable for analog and radio-frequency (RF) applications, such as in amplifiers, mixers, and oscillators used in communication systems.

5. Sensors: CNTFETs are highly sensitive to changes in their environment, which can be harnessed for various sensing applications. They can be used in chemical and biological sensors for detecting gases, biomolecules, and other substances at very low concentrations.

CNTFETs can be used in nanoscale electronic devices where traditional silicon transistors are reaching their physical limits. Their small size and high performance make them ideal for integrating into densely packed circuits.

4. Analog and RF Electronics: The

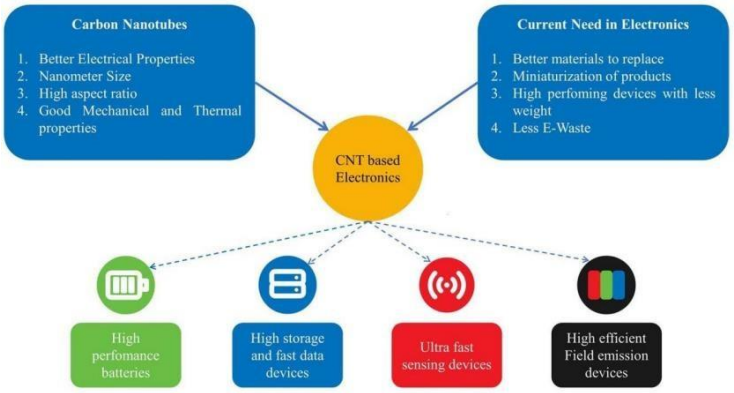

Figure 1.1. Applications of CNTFETs

➢ Future Perspectives of CNTFETs

1. Overcoming Manufacturing Challenges: One of the major hurdles in the widespread adoption of CNTFETs is the precise and large-scale manufacturing of carbon nanotubes. Advances in fabrication techniques, such as improved chemical vapor deposition (CVD) processes and better methods for sorting and aligning CNTs, are crucial for commercial viability.

2.Integration with Existing Technologies: For CNTFETs to be adopted in the semiconductor industry, they need to be compatible with existing silicon-based technologies. Hybrid approaches, where CNTFETs are integrated with traditional silicon circuits, could be a stepping stone towards full-scale adoption.

3. Improved Material Quality: The electrical properties of CNTs can vary based on their chirality and the presence of defects. Developing methods to produce high-purity, chirality-specific, and defect-free CNTs will enhance the performance and reliability of CNTFETs.

4. Economic Viability: The cost of producing CNTFETs must be competitive with silicon-based transistors. Economies of scale and advancements in production techniques will be necessary to reduce costs and make CNTFETs a commercially viable alternative.

5. New Device Architectures: As research progresses, new architectures leveraging the unique properties of CNTs are likely to emerge. This includes three-dimensional (3D) integrated circuits and novel designs that exploit the mechanical flexibility of CNTs for new types of electronic devices.

6. Environmental Impact: The environmental benefits of CNTFETs, such as lower power consumption and potentially less material waste compared to silicon manufacturing, could make them an attractive option for sustainable technology development.

Moreover, full-adders are regarded as one of the most crucial components in the design of computational logic circuits, including memory units and caches, test and address production, and arithmetic logic units (ALU).

Stated differently, distinct logic design styles derive advantages from their unique design attributes, including layout area, transistor count, and power-delay efficiency. The low transistor count and circuit complexity of the GDI design technique make it a successful low-power technique. Unfortunately, the traditional digital integrated circuits based on GDI are not capable of full swing. Furthermore, because the dynamic logic style incorporates pre-charge operation for the circuit's internal and output nodes, it successfully lowers power consumption while enhancing the circuit's full-swing capabilities. Thus, the primary contribution of this thesis is to develop new low-power CNFET logic circuits by combining the low-power GDI technique with the dynamic logic style, in order to accomplish both low power and full swing performance.

Therefore, Combinational logic circuits order to maximize overall processing efficiency, it needs to be built to achieve low levels of power consumption, latency, PDP, and transistor count. Considering the aforementioned information, selecting One essential initial step in building a high-performance computing system is selecting the right design style for digital VLSI circuits.

CNTFETs represent a promising advancement in transistor technology, offering enhanced performance and efficiency for future electronic applications. Their development could lead to significant improvements in the aera, speed and scalability in electronic devices , paving for next-generation nano electronic devices. CNTFETs hold great promise for revolutionizing various fields of electronics by offering superior performance, efficiency, and flexibility compared to traditional silicon transistors. While significant challenges remain, ongoing

research and technological advancements in future.

1.2 Carbon Nanotube Field-Effect Transistors

The acronym for Carbon Nano Tube Field Effect Transistor is CNTFETs. A FET with a carbon nanotube channel is called a CNTFET. Owing to its many advantages over conventional CMOS technology, including its tiny feature size, low power consumption, high speed, and MOSFET-like device behavior, CNFET technology is regarded as one of the strongest contenders to replace it. Figure depicts the CNFET's physical layout. Single-walled carbon nanotube transistors (SWCNT) and multi-walled carbon nanotube transistors (MWCNT) are the two main types of carbon nanotubes (CNTs), which are made of carbon molecules.

The arrangement of atoms in a single-wall carbon nanotube (CNT) allows it to function as a semi-conductor or conductor. It is governed by the Chirality vector (n, m). The CNT structure would function as a conductor if n = m and n-m = 3i (where i is an integer); if not, it would be regarded as a semi-conductor device.

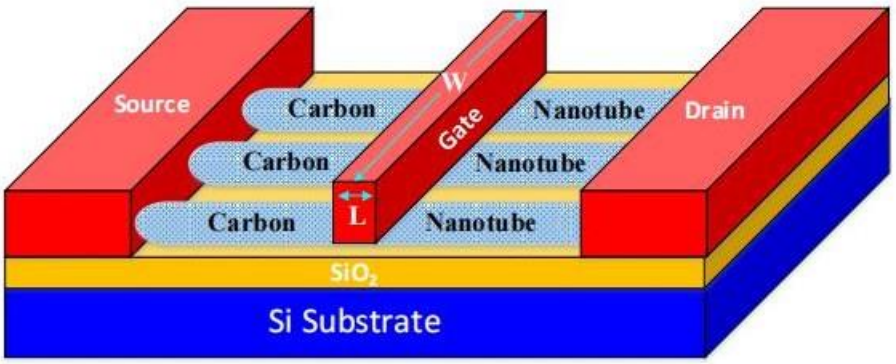

Figure 1.2. Schematic of a carbon Nanotubes field effect Transistor (CNTFET).

CNFETs, one of the most promising new technologies, get beyond most of the basic drawbacks of conventional silicon devices. Because there are no dangling bonds and all of the carbon atoms in CNTs are connected to one another via sp2 hybridization, CNTs are ideal for use in high-k dielectric materials in nano electronics applications including interconnects and nanoscale devices. Due to their great current carrying capacity as well as their semiconductor and metallic characteristics. Integrated circuits with high speed performance, low power consumption, and smaller dimensions are in high demand as new technologies advance. According to Moore's law, transistor size has decreased; however, there are certain drawbacks, such as a shorter channel effect that causes direct tunneling and a rise in gate leakage current. These drawbacks are overcome by CNTFET.

Integrated circuits with high speed performance, low power consumption, and smaller dimensions are in high demand as new technologies advance.One can roll either a single-walled or multi-walled graphene sheet to create carbon nanotubes. The carbon atoms are organized in two-dimensional honeycomb lattices in graphene.

Two categories exist.

1) Single-walled, with a diameter of 1 nm;

2) Multi-walled, with a diameter of 100 nm and numerous interconnected layers

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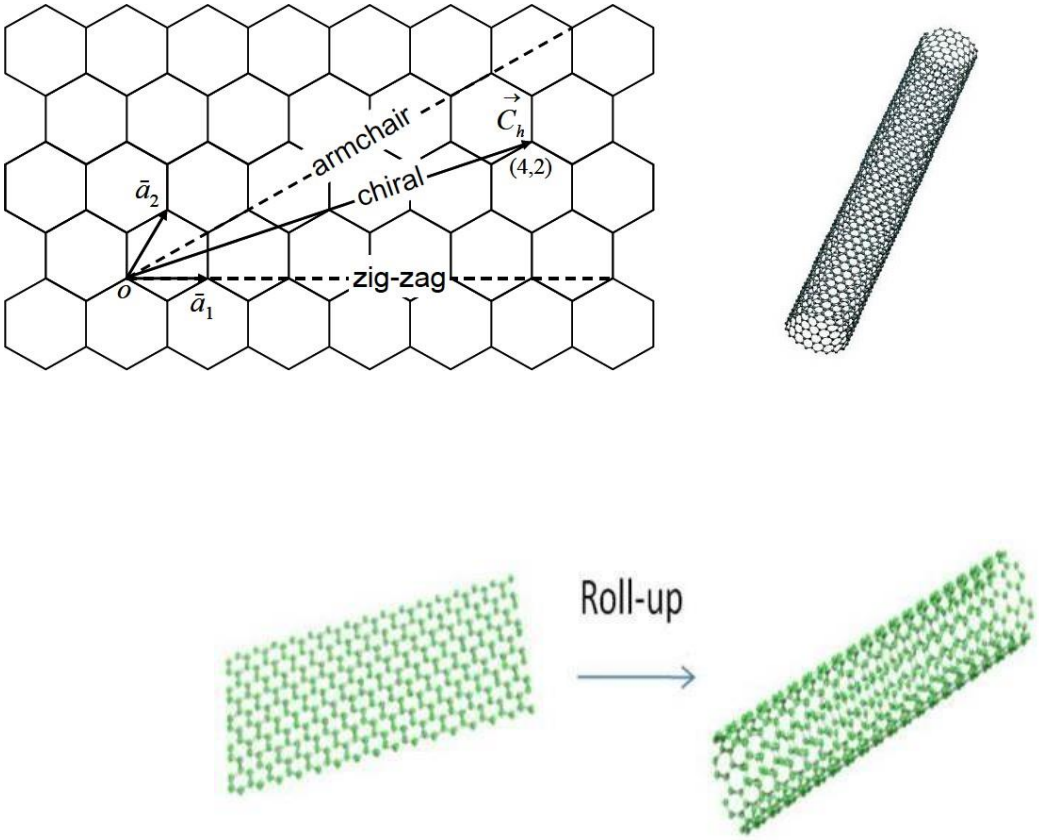

Fig 1.3. Graphite sheet and the rolled Carbon Nanotubes structure .

A graphite sheet that has been rolled up and joined together along a wrapping vector Ch = n1¯a1 + n2¯a2 can be used to visualize a single-walled carbon nanotube (SWCNT). The lattice unit vectors [¯a1, ¯a2] are represented by Fig. 1.2, and the positive integer indices (n1, n2) indicate the tube's chirality [9]. Hence, Ch's length equals the CNT's circumference, which can be found using the formula Ch = a √ n 2 1 + n 2 2 + n1n2.

Nonetheless, the diameter of the nanotube can be computed using the expression .

$DCNT = \sqrt{3}a\sqrt{n2 + m2 + nm}/\pi$ where, a0 = 0.142 nm, is the inter-atomic distance between the centers of two adjacent Carbon atoms.

Depending on the chiral number (n1, n2), single-walled CNTs are categorized into one of three groups (Figure 1): (1) armchair (n1 = n2), (2) zigzag (n1 = 0 or n2 = 0), and (3) chiral (all other indices). The diameter of the CNT is given by the formula DCNT = Ch/π. The atomic plane of graphene contains the condensed electrons found in CNT. The electrons' mobility within the nanotubes is tightly constrained because of the quasi-one-dimensional structure of CNT. Only in the direction of the tube's axis can electrons travel freely.

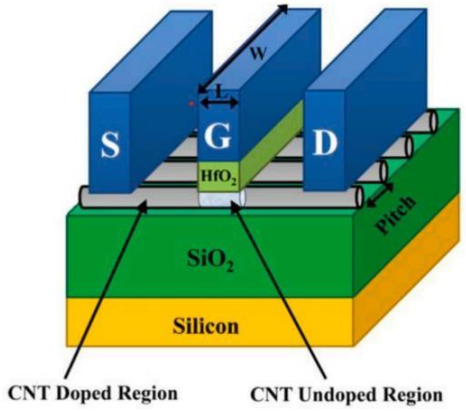

Fig. 1.4. CNFET physical structure

The tight bonding model's threshold voltage, Vth, is determined by the carbon to carbon atom distance, a = 2.49A◦, and the carbon π-π bond energy, Vπ = 3.033 eV. Furthermore, D is a nanotube's diameter and e is an electron's charge.

The CNFET parameters definitions and values.

Device parameter	Description	Value
Lch	Physical channel Length	32 nm
Lss	The length of doped CNT source-side extension region	32 nm
Ldd	The length of doped CNT source-side extension region	32 nm
Lgeff	The mean free path in the intrinsic CNT channel	100 nm
Pitch	The distance between the centers of two adjacent CNTs within the same device	20 nm
Tox	The thickness of high-k top gate dielectric material	4 nm
Csub	The coupling capacitance between the channel region and the substrate	40 aF/ um
Efi	The fermi level of the doped S/D tube	6 eV

Table I CNFETs parameters and value.

1.3 Thesis Organization

The thesis is arranged in seven chapters describing the context, aims, objectives of the research, motivation, literature review, methods and techniques employed and the research contributions The low power and high speed circuit design problems for CNFET technology are the main emphasis of this thesis.

Chapter 1, CNFET transistors and carbon nanotube technology are presented. Introduction briefly describes the importance of low power circuits and their applications to wearable, implantable and portable electronic systems. Scaling limitations of conventional CMOS devices and the importance of CNFETs. are explained in the context of the proposed research
Recently, a lot of work has gone into modeling and simulating CNT-based devices like a CNT interconnect and CNFET. Nevertheless, the majority ofThe device level has been the focus of these initiatives. But a circuit made up of multiple components performs dynamically.
Chapter 2: Litertature Survey This chapter highlights development of techniques and technologies for the low power circuits. The literature review of GDI technique and slove problem using dynamic logic design. A development based on Carbon Nanotube, CNFETs Stanford model for CNFETs is also described. Limitations, shortcomings of existing techniques are presented and some Motivation about this thesis .
Chapter 3: Low-power GDI approaches discusses how the GDI approach can be used to quickly and efficiently build circuits with fewer transistors. and high performance circuit for various logic combinational circuits using Cntfet .
Chapter 4 : We slove the issue of full swing output with Gdi combinational logic circuits and compare it with the output utilizing the dynamic GDI approach.
Chapter 5: Moreover using Dynamic-GDI we design new D-GDI full adder and Half substractor using D-GDI based on CNFETs technology is circuit are presented .
Chapter 6, The circuit's simulation results are showen.
Chapter-7 Conclusion : This chapter offers an overview of the studies, inferences made from the findings, and recommendations for additional research.

Chapter 02 LITERATURE SURVEY

2.1 Introduction

A review of the literature on dynamic GDI combinational logic circuits based on CNTFETs identifies numerous important topics for further study and advancement. Because they outperform conventional CMOS technology in terms of performance and scalability, carbon nanotube field effect transistors, or CNTFETs, are used. CNTFETs and the Gate Diffusion Input (GDI) method work together to provide low-power, high-speed logic circuit construction. According to research, CNTFET-based circuits outperform conventional designs in terms of space efficiency, transistor count, and power usage.

The effectiveness of For the purpose of building fast, low-power digital circuits, dynamic Gate Diffusion Input (GDI) combinational logic circuit design is demonstrated by a review of the literature. In comparison to conventional CMOS designs, GDI designs minimize size, transistor count, and power consumption. It enhances performance and reduces energy consumption by achieving complicated logic functions with fewer transistors.Dynamic GDI circuits, which incorporate clocking elements, enhance these benefits by further reducing leakage currents and improving switching speeds. This is particularly useful for energy-efficient computing applications.

Dynamic GDI techniques further enhance these advantages by simplifying the circuit design and reducing leakage currents, which is critical for energy-efficient computing. Dynamic Gate Diffusion Input (GDI) combinational logic circuits are an advanced technique for designing digital circuits that emphasize low power consumption, reduced transistor count, and high speed. The GDI method allows for the implementation of complex logic functions with simpler circuitry compared to traditional CMOS designs. By incorporating dynamic elements, these circuits further optimize performance by minimizing leakage currents and enhancing switching speeds. Dynamic GDI is particularly effective in energy-efficient applications, providing significant improvements in power efficiency, area reduction, and operational speed, making it ideal for modern digital systems.Studies have focused on implementing various combinational logic circuits, including adders, multiplexers, and decoders, showcasing significant improvements in performance and energy efficiency.

Key applications include various Combinational logic functions, including logic gates, multiplexers, and adders, show notable gains in power, delay, and power and delay product (PDP) performance.

Overall, dynamic GDI technique the integration of CNTFETs with dynamic GDI in combinational Logic circuits are essential for the development of sophisticated, energy-efficient digital systems and offer a promising route for the creation of next-generation, high-performance, low-power digital systems.

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2.2 Literature Review

In a research paper that and Ali Ghorbani and Mehdi Dolatshahi and S. proposed novel Dynamic-GDI complete adder with low power consumption that uses CNTFET technology in terms of power, delay, and power delay product (PDP). The Cadence Spectre test System was used to produce the results [1].

A work that presented a subjective knowledge of a Low power techniques in this work on Gate Diffusion Input (GDI) basic cell using GDI we implemented basic combinational circuits, GDI approach, which effectively lowers power consumption and layout time in digital integrated circuit design.

Gate Diffusion Input technique was introduced by Adam Morgenshtein, Avinoam Fish, and Israel A. Wagner in 2002. This Compared to conventional CMOS technology, a technique was presented to streamline the design and implementation of digital circuits, enabling lower power consumption, a lower transistor count, and better performance. These advantages are realized by the GDI method, which makes it possible to construct sophisticated logic functions with fewer components. This makes it a useful technique for low-power and fast digital circuit design.[2].

The primary goal of a work suggested by Mohammadali Zanjani and Behrang Barekatain was to using GDI, or dynamic gate diffusion input, is a sophisticated method for creating digital circuits. that emphasize low power consumption, reduced transistor count, and high speed. By incorporating dynamic elements, these circuits further optimize performance by minimizing leakage currents and enhancing switching speeds. Dynamic GDI is particularly effective in energy-efficient applications, providing significant improvements in power efficiency, area reduction, and operational speed and power consumption. Applying the dynamic logic design we resolved the one of major problem with GDI that is full output voltage swing This study calculates and examines the combinational circuits' power consumption and delay. Cadence Virtuoso tools are used for this [3].

2.3 Motivation

In recent years, carbon nanotube (CNT) technology has drawn a lot of attention as a prospective extension to silicon-CMOS technology. It provides a viable avenue for the continuous

development of integrated circuits. Among other things, carbon nanotubes are made of carbon organized in a tube-like shape and have exceptional electrical conduction capabilities. These materials are specifically one-dimensional and have the potential for ballistic transport with greatly decreased dispersion. Because of their superior current conduction and reduced capacitance, carbon nanotube field-effect transistors (CNFETs), which are transistors built from single-walled carbon nanotubes as shown in Figure, exhibit great intrinsic delay. In digital logic applications, the superior inherent delay results in reduced power consumption and increased performance (speed). According to simulation studies, CNFETs outperform silicon-CMOS in terms of performance.

Here are some motivations and points of interest related to this project:

Innovation through Technique: Dynamic gate diffusion input technique offers a differnet method by effectively cutting down on the time lag between input and output.Reducing power consumption and improving combinational circuit efficiency and speed are critical.

Technology Advancement: Emphasise the significance of utilising 32nm technology. Highlight how this specific technology and the proposed DGDI technique represent advancements in semiconductor design, contributing to more efficient and high performance devices.

Performance Improvement: Concentrate on reaching the main objectives of low power consumption, power delay product, and excellent performance with delay.

Simulation and Validation: Discuss the use of Cadence Virtuoso's Analog-Design Environment (ADE) for software simulations. Explain how these simulations were crucial in measuring power usage, latency , and validating the effectiveness of the DGDI technique.

Comparative Analysis: Highlight the significance of the results obtained from the project. Specifically, mention the 28% reduction in power consumption achieved by the recommended technique compared This emphasises the practical significance and potential commercial implications.

Future Implications: Discuss potential future applications or developments that can stem from this thesis. Consider how this innovative technique and its positive results might influence the design and development of future semiconductor technologies.

With the help of the aforementioned contributions, this thesis seeks to further the field of carbon nanotube technology in the direction of large-scale integrated circuits made of high-density carbon nanotubes.

Chapter 03 GDI TECHNIQUE

3.1 Introduction

A low power design method for digital logic circuits called Gate Diffusion Input (GDI) seeks to minimize power consumption, latency, and transistor count in different logic gate configurations. Developed by Shmuel Kvatinsky, Amir Fish, Itamar Wagner, and Alexander Kolodny in the early 2000s, GDI presents an efficient alternative for traditional combinationl logic , particularly for low-power applications.

- **Key Features of GDI :-**

1. Reduced Power Consumption: GDI circuits consume less power compared to conventional CMOS circuits because they typically use fewer transistors. This reduction in components directly correlates with lower dynamic power consumption, making GDI suitable for battery-powered and portable devices.
2. Fewer Transistors: By leveraging a unique arrangement of inputs directly to GDI lowers the number of transistors required to implement sophisticated logic functions by connecting the source and drain terminals of transistors.This reduction simplifies the design and can lead to smaller chip area.
3. Improved Speed: Fewer transistors and shorter signal paths contribute to faster switching speeds. GDI circuits can achieve lower propagation delays, which is beneficial for high-speed computing applications.
4. Design Flexibility: With just a few adjustments, GDI enables the construction of a vast array of logic gates and intricate functions. to the basic cell structure. This flexibility makes it a versatile tool in digital circuit design.

- **Advantages of GDI**

1. Low Power: The reduction in the number of transistors and the associated capacitances lead to lower power consumption.
2. Area Efficiency: Fewer transistors translate to a smaller chip area, which can reduce manufacturing costs and improve yield.
3. High Performance: The reduction in capacitive loading results in faster operation speeds.
4. Design Simplicity: The ability to implement complex functions with fewer components simplifies the design process

- **Applications**

GDI is particularly well-suited for applications where power efficiency and speed are critical, such as:

Portable and battery-operated devices

Low-power digital signal processing

High-speed communication circuits

Embedded systems

3.2 Basic Gate Diffusion Input

Like a CMOS inverter, a basic GDI cell is made up of two transistors: an NMOS and a PMOS. The source/drain and gate terminals in GDI, however, are set up differently:

1. The source/drain terminals of the NMOS and PMOS transistors, respectively, are connected to the inputs N (N-well or P-substrate) and P (P-well or N-substrate).
2. G is the transistors' shared gate input.
3. D is the output obtained from the transistors' drain terminals.

A CMOS inverter's construction is quite similar to that of the GDI circuit.The PCNT source of a CMOS inverter is connected to VDD, while the NCNT source is grounded. A GDI cell takes three inputs into account:G-common inputs to PCNT and NCNT's gate N-input to the NCNT source or drain P-input to the PCNT source or drain One significant distinction between GDI and CMOS is that, depending on the circuit to be designed, GDI (N,P&G) terminals can be provided with an input signal, grounded, or supplied with a supply VDD, hence reducing the number of transistors required.

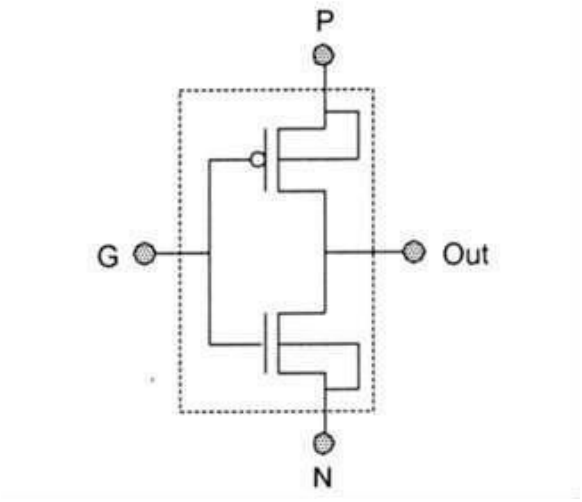

Figure 3.1 Basic GDI circuit

It has three inputs (G, P, N) where G node is the common gate input of NMOS and PMOS, P node is the Drain or Source of PMOS input and N node is the Drain or Source of NMOS input .

Logic gates including AND, OR, NOR, and MUX have been designed employing the Gate Diffusion Input (GDI) approach, which reduces the circuit's transistor count and hence lowers area and power demands.To create distinct logic functions, this cell is utilized to apply various inputs to G, P, and N.

This configuration allows the basic GDI cell to implement multiple functions such as AND, OR, MUX, XOR, and more by varying the input combinations.

N	P	G	Out	Function
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT

Table II : GDI implementation of boolean functions

CMOS implementation of same function required large number of transistors which require larger chip area and increases complexity. GDI based gates require less chip area, as we have to only change the input to get the required functionality. The GDI method is helpful for building quick and low-power circuits. using less number of transistaors and high performance circuit.

In summary, The design process known as Gate Diffusion Input (GDI) is a potent tool that provides noteworthy advantages for speed, power efficiency, and transistor count.It has some challenges, its advantages make it an attractive option for modern digital circuit design, especially in power-sensitive applications.

3.3 Simulations Based on Gate Diffusion Input Technique.

3.3.1 Inverter

An inverter is a simple digital logic gate that reverses or inverts the input signal. It is also referred to as a NOT gate. To put it another way, a logical low (0) will be the output and vice versa if the input is a logical high (1).

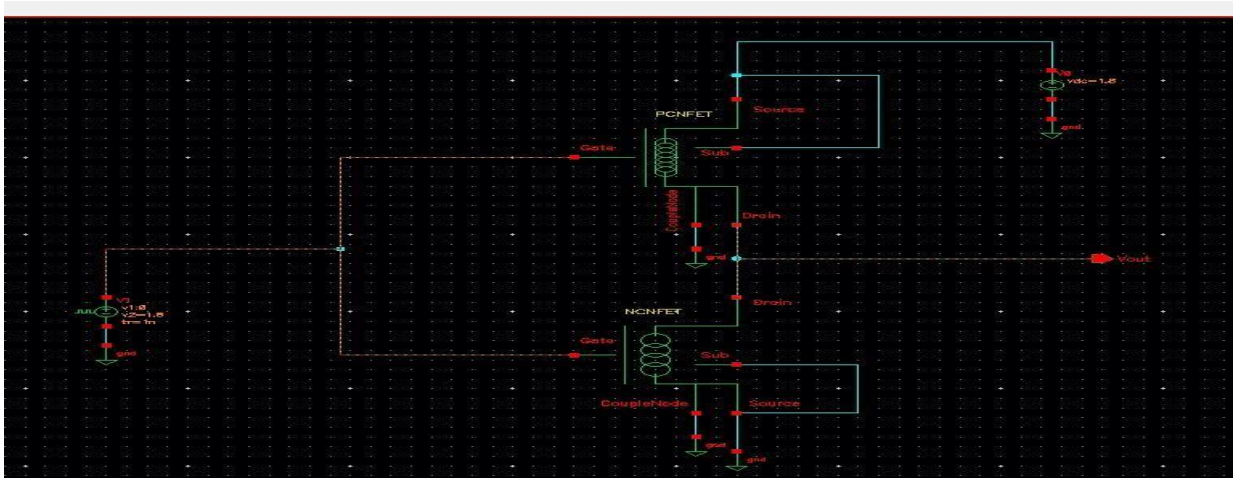

Figure 3.2. Circuit Schematic of inverter using GDI .

Figure 3.3. Output Waveform of inverter
DC and Transient Analaysis.

3.3.2 XOR Gate.

A digital logic gate known as an XOR (exclusive-OR) gate outputs true or high (1) only in the event that the number of true inputs is odd. It operates in an exclusive OR fashion, which means that if one and only one of its inputs is 1, it will output 1.

The following is the term Y's logical expression: Y = A'B + AB'

XOR gates are frequently employed in digital systems, particularly arithmetic circuits, for purposes such as inequality detection and error detection and correction systems. like adders, parity generators and checkers, and data comparison circuits

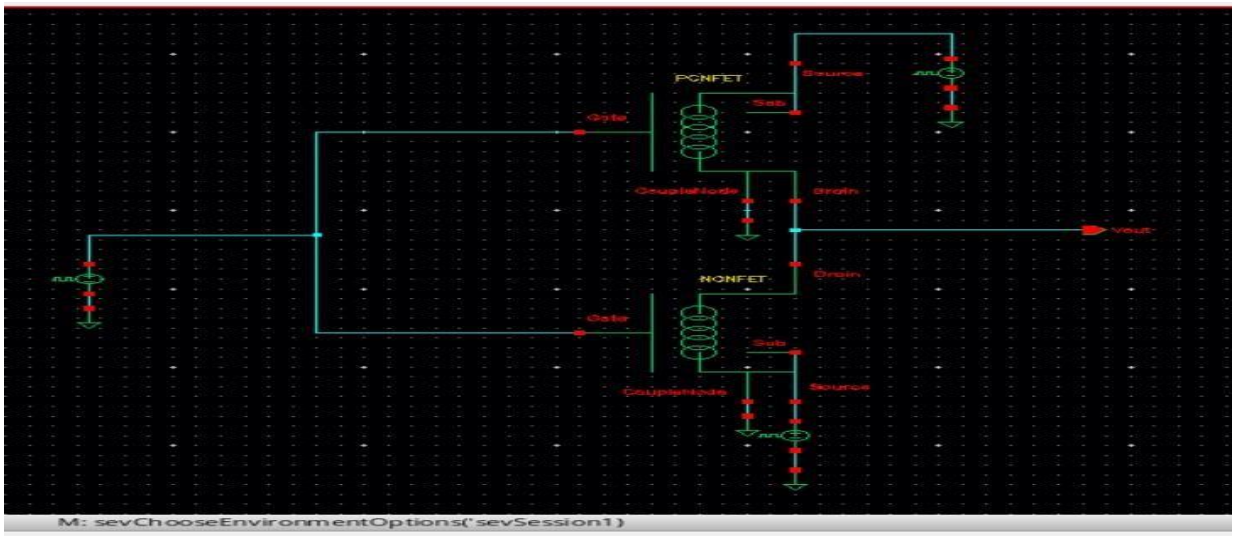

Figure 3.4. Circuit Diagram for Xor gate GDI .

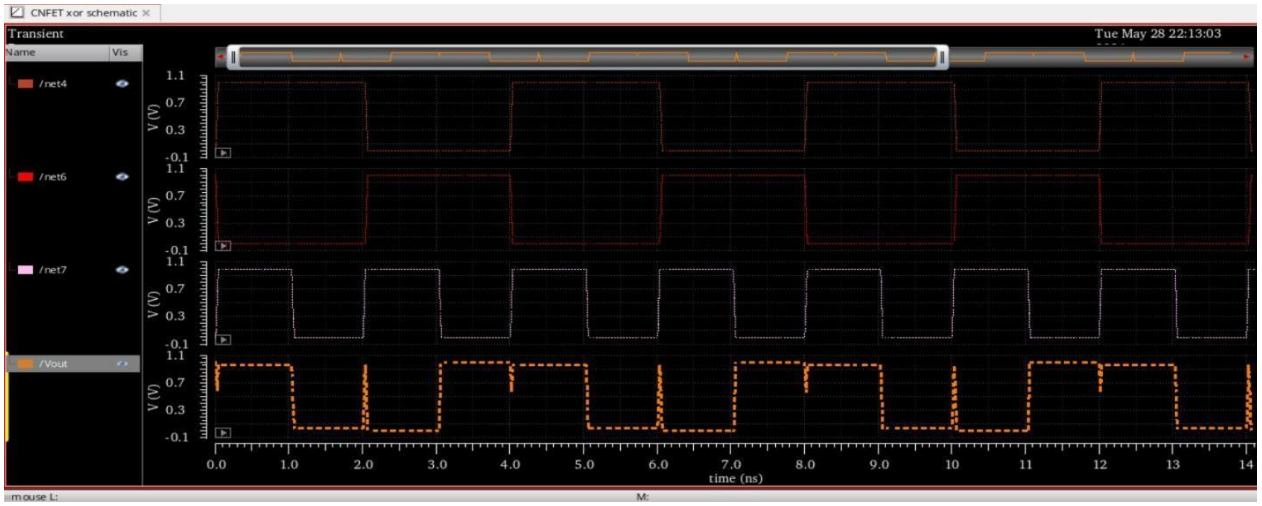

Figure 3.5. Output Waveform Xor gate GDI

3.3.3 Multiplexer

A multiplexer is a combinational circuit comprising twon input lines and one output line. A multiplexer is, in essence, a combinational circuit having several inputs and one output. Binary data is received from the input lines and transmitted to the output line. Depending on the selection lines' values, one of these data inputs will be linked to the output. Rather than an encoder and a decoder, there are n selection lines and 2n input lines. Consequently, there are 2N

potential combinations of inputs in total. Another term for a multiplexer is Mux.The multiplexer comes in different varieties, which include the following: 2x1 Multiplexer:

A 2x1 multiplexer has merely one selection line (S0), one output (Y), and two inputs (A0 and A1). Depending on the combination of inputs at selection line S0, one of these two inputs will be connected to the output. The block diagram for the 2x1 multiplexer is shown below.

The following is the term Y's logical expression: Y = S'A0 + SA1

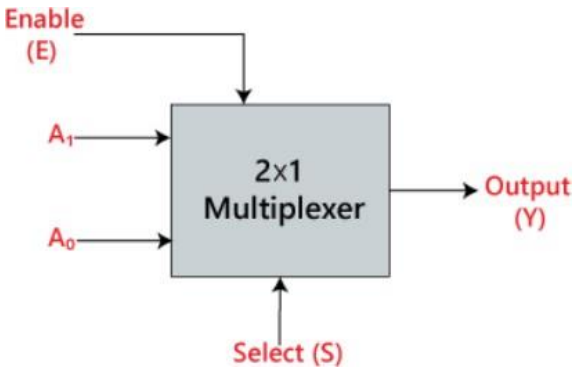

Figure 3.6. Block diagram of the 2×1 multiplexer

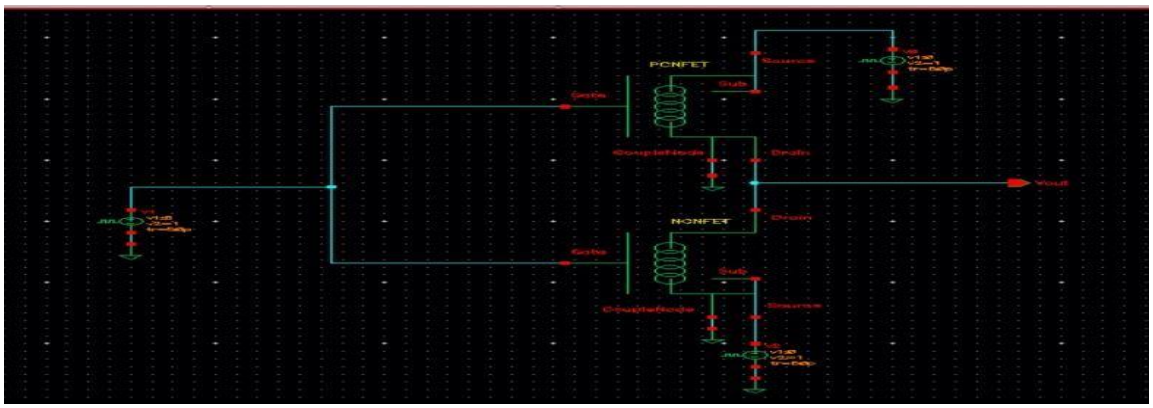

Figure 3.7. Circuit Schematic of Multiplexer using GDI

Figure 3.8. Output Waveform of Multiplexer using GDI

3.4 Simulations Table

PARAMETERS	GDI XOR	GDI MULTIPLIXER
DELAY	13.6 ps	15.2 ps
POWER	0.145 uW	0.136 uW
POWER DELAY PRODUCT (PDP)	1.97 aj	2.067 aj

3.5 Summarry

One of the best logic circuit techniques for effectively reducing the layout area and The Gate Diffusion Input (GDI) technique is used to create digital integrated circuits with low power consumption. The GDI core circuit can be seen of as a simple gate in general, with the N and P type transistors' sources connected to the inputs marked "P" and "N" instead of the supply voltage VDD or ground (GND). Consequently, the GDI approach can be used to implement many binary functions. A rudimentary GDI core cell implemented using a CNFET is shown in Fig. 3.1. The truth tables for the various logic functions are compiled in Table based on the GDI inputs (G, N, and P). Using the GDI approach in circuit design,

Despite its advantages, GDI faces some challenges:

1. Fabrication Compatibility: The GDI technique may require specific fabrication processes that are not always compatible with standard CMOS manufacturing lines.
2. Noise Margins: The reduced number of transistors can lead to lower noise margins, potentially affecting the reliability of the circuits.
3. Voltage Swing: In some GDI configurations, the output voltage swing might be less than full rail-to-rail, which can limit its use in certain applications.

In summary, Gate Diffusion Input (GDI) is a powerful design methodology that offers significant benefits in terms of power efficiency, speed, and transistor count. it has some challenges, its advantages make it an attractive option for modern digital circuit design.

Chapter 04 DYNAMIC LOGIC DESIGN

4.1 Introduction

Dynamic logic design is best technique used in digital circuit to accomplish faster processing times and lower power usage when compared to static logic devices. Unlike static logic, which uses a steady-state input to control the output, dynamic logic relies on the of clock signals and capacitive nodes for the temporary storage of data to control the timing of logic operations.

- **Key Characteristics of Dynamic Logic**

1. Clock Dependent: Dynamic combinational logic circuits required clock signals to control the precharge and evaluation phases. The operation of these circuits is synchronized with the clock, which governs the timing of logic transitions.
2. Precharge and Evaluation Phases: During this phase, the circuit's internal nodes are precharged to a known state, typically using a PMOS transistor connected to the clock.
3. High-Speed Operation: Dynamic logic circuits can achieve faster switching speeds compared to static logic because they eliminate the need for pull-up and pull-down networks found in traditional logic gates. This leads to reduced capacitive loading and faster transitions.
4. Reduced Transistor Count: By leveraging the precharge and evaluation mechanism, dynamic logic often requires fewer transistors to implement complex functions, leading.

- **Advantages of Dynamic Logic Design**

1. High Performance: Compared to staticlogic circuits, dynamic logic circuits may function at higher frequencies because of their quicker switching speeds and lower capacitive loading..
2. Compact Design: The reduced number of transistors needed for dynamic logic gates results in smaller chip area and potentially lower manufacturing costs.
3. Lower Power : Despite the fact that dynamic logic circuits' timed operation can result in higher power consumption, the overall power efficiency can be higher in applications where speed and area efficiency are crucial.

Applications

Dynamic logic is particularly well-suited for high-speed and high-performance applications, such as:

1. Microprocessors and central processing units (CPUs)
2. High-speed communication systems
3. Digital signal processors (DSPs)

4.2 Dynamic Logic Design

In digital circuits, dynamic logic design is an approach that allows for higher speeds and lower power consumption than static logic. The fundamental concept of dynamic logic is to use temporary storage of logic states and clock signals to control the evaluation of logic functions. Here's a basic overview of how dynamic logic works, along with a simple schematic

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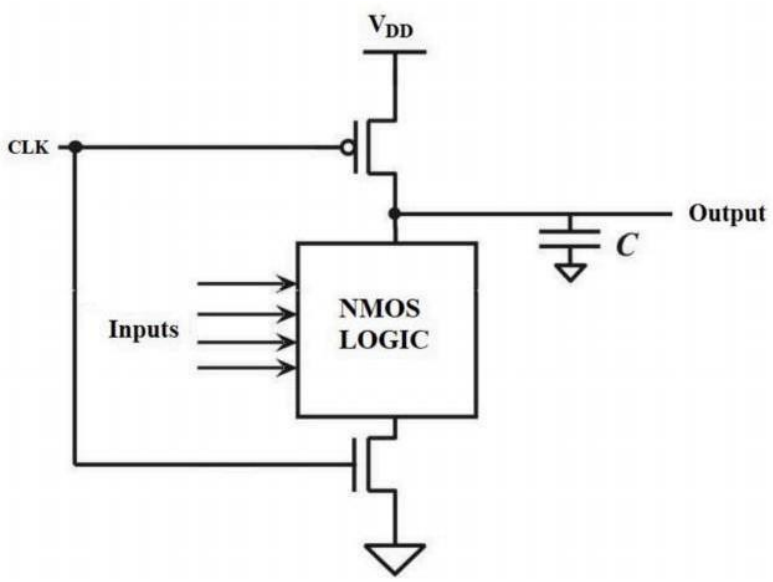

Fig 4.1. Basic Schematic of Dynamic Logic Design

When designing and implementing low-power digital circuits, dynamic logic types play a crucial role in achieving the primary goal of minimizing both chip area and power consumption .Dynamic logic gates operate on the basis of the transient storage of electric charges at the nodes attached to the internal parasitic capacitances. However, as Fig. 4 shows, digital circuits developed in the dynamic logic paradigm require clock signals in order to update the voltages of internal nodes.

This problem makes it possible to create basic sequential circuits, which have the well-known advantages of using less space and power as compared to other static or traditional CMOS logic types.

Dynamic logic design is a specialized field within digital circuit design that requires a deep understanding of both the advantages and potential pitfalls of dynamic logic techniques. Proper design and implementation can lead to significant performance improvements in various combinational circuit.

4.3 Comparsion Dynamic GDI (D-GDI) Xor gate .

The fundamental component of compresor circuits is thought to be the XOR gate. Consequently, the whole circuit's efficiency would increase with a design that uses the right circuit characteristics. Fig. 4.2 displays the general schematic of both the Dynamic GDI (D-GDI) XOR gate circuit and a traditional GDI XOR circuit.

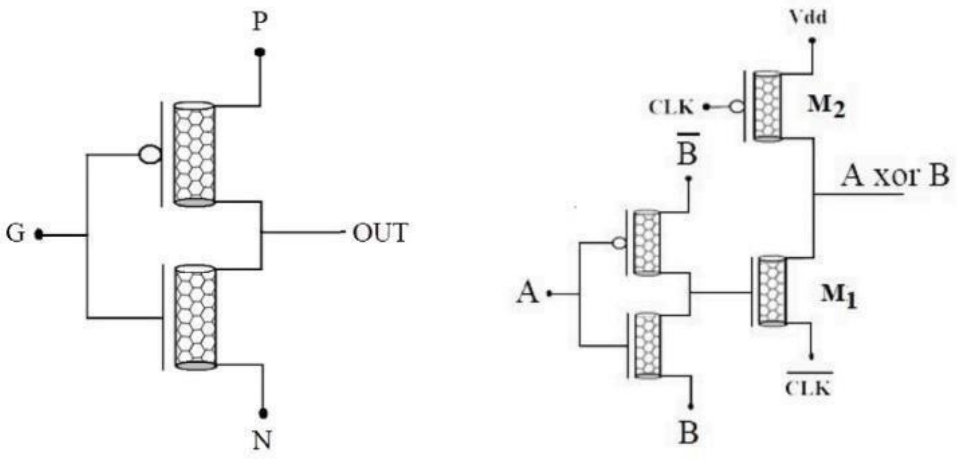

Figure 4.2. (a) Basic GDI Xor gate (b) Dynamic GDI Xor gate

The DGDI and GDI logic architectures' operational properties for various input combinations.

Operational characteristics of GDI XOR cell.

A	B	Out
0	0	$\|V_{thp}\|$
0	1	V_{DD}
1	0	V_{DD}-V_{thn}
1	1	0

Operational characteristics of the proposed DGDI XOR cell.

CLK	A	B	Out
0	x	x	V_{DD}
1	0	0	0
1	0	1	V_{DD}
1	1	0	V_{DD}
1	1	1	0

Above table, When both the inputs are equals to "0," the GDI XOR circuit's output is not able to fully swing, resulting in an output of |Vthp|. When A = 1 and B = 0, this scenario is true, and the result is VDD-Vthn. This problem is increasingly common, especially with circuits with three inputs. Conversely, the suggested D-GDI XOR gate enhances the output full swing.

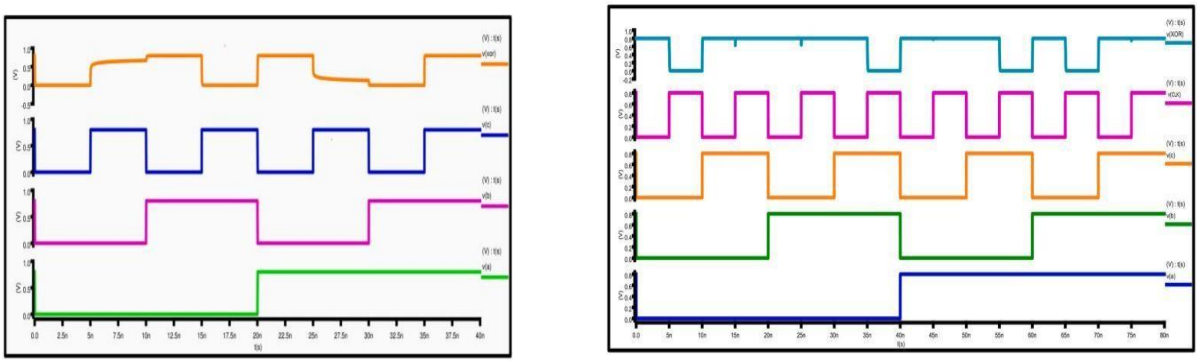

Figure 4.3. (a) Output wave form GDI Xor gate (b) The Dynamic GDI Xor gate

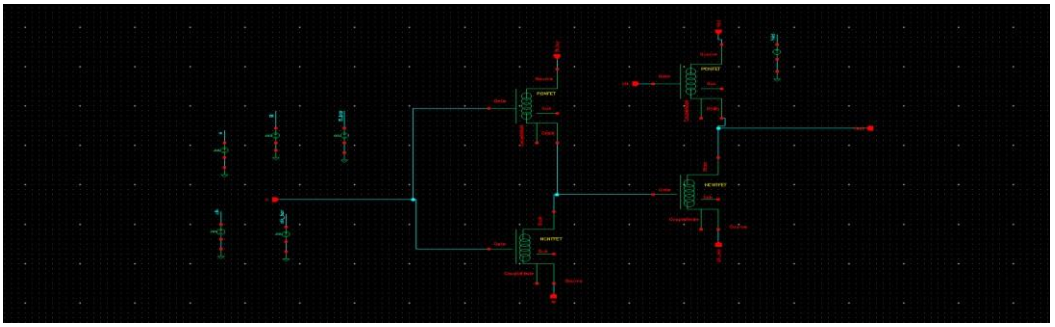

Figure 4.4 Circuit Schematic of D-GDI Xor Gate.

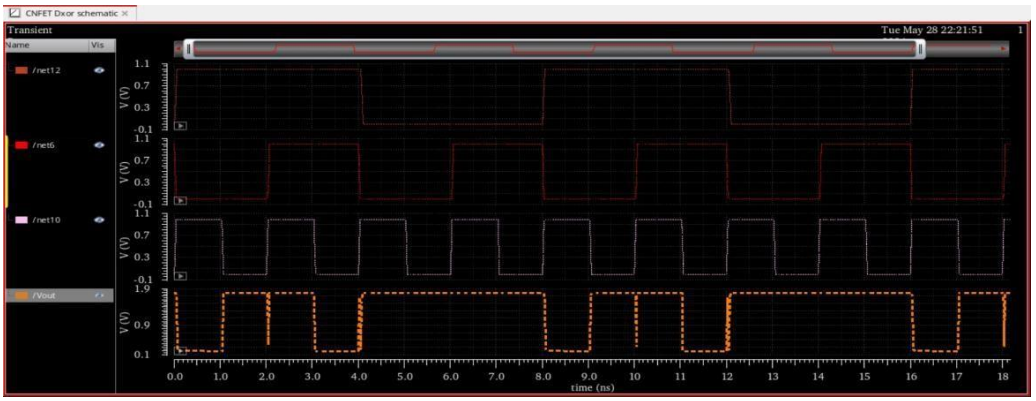

Figure 4.5 Output Waveform of D-GDI Xor Gate

Figure 4.6 Waveform for delay calculation of D-GDI Xor Gate.

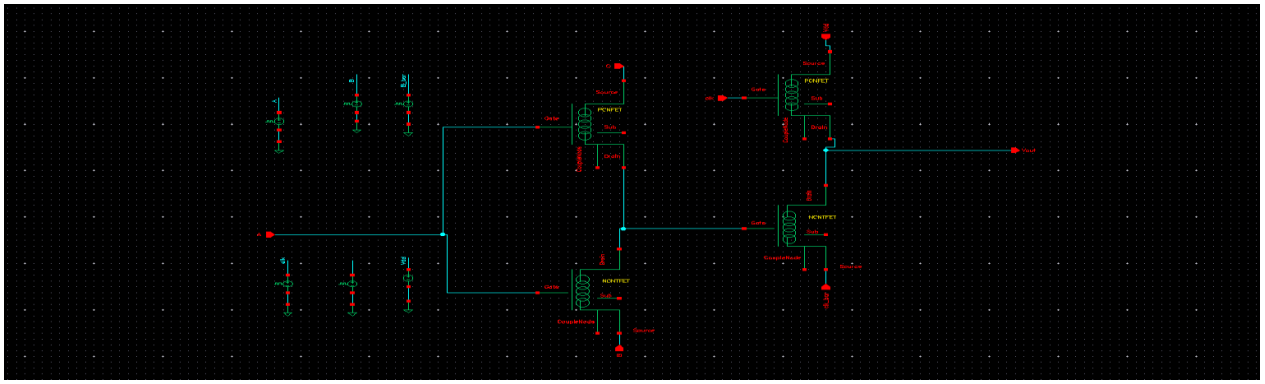

Figure 4.7. Circuit Schmatic of Multiplexer.

Figure 4.8 Output Waveform of Multiplexer.

Figure 4.9. Waveform for delay calculation of DGDI Multiplexer.

4.3 Simulations Table .

PARAMETERS	D-GDI XOR	MULTIPLIXER
DELAY	12.6 ps	15.2 ps
POWER	0.116 uW	0.118 uW
POWER DELAY PRODUCT (PDP)	1.46 aj	1.793 aj

4.4 Summary

In summary, dynamic logic design offers significant benefits in terms of transistor efficiency and speed, rendering it a useful method for high-performance digital circuits. However, its implementation requires careful consideration of noise sensitivity, timing synchronization, and power management to ensure reliable operation. Also solve one of the major problem is the output voltage swing.

Chapter 05 COMBINATIONAL CIRCUITS

D-GDI LOGIC DESIGN

5.1 Introduction

When designing and implementing low-power digital circuits, dynamic logic types play a crucial role in achieving the primary goal of minimizing both chip area and power consumption. The temporary storage of electric charges at the nodes connected to the internal parasitic capacitances is the foundation for the functioning of dynamic logic gates. Nevertheless, as Fig. 5 illustrates, clock signals are needed by the dynamic logic style digital circuits in order to update the internal nodes' voltages. In contrast to other static or standard CMOS logic types, This issue makes it possible to create simple sequential circuits, which have the well-known benefits of requiring less power and taking up less space.

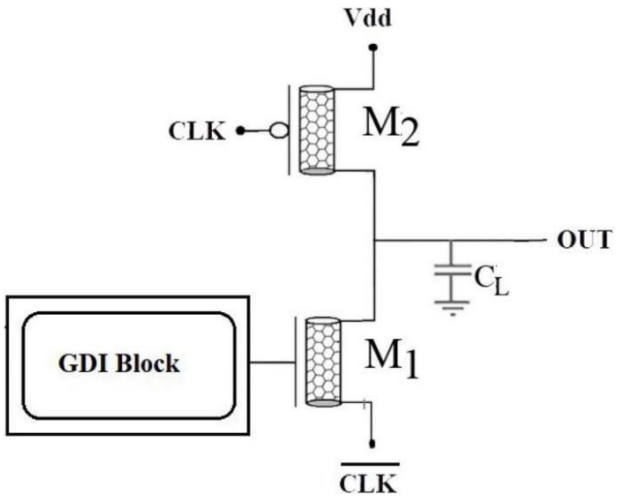

Fig-5.1. Dynamic GDI logic core.

By employing a dynamic circuit structure, the Dynamic GDI XOR circuit enhances the output swing, allowing the design to attain a rail-to-rail swing when compared to a traditional GDI XOR circuit.

Furthermore, the power consumption of the GDI circuit is further reduced by applying the CLK signal in a dynamic circuit layout. Given the aforementioned details, the DGDI circuit functions as follows: The M2 transistor charges the load capacitor to the VDD level when the CLK signal is "0." However, because transistor M1 uses the CLK signal, it cuts off when the CLK signal is "1" and the logic levels of the A and B inputs differ. At that point, the output signal is equal to the pre-charged state (VDD), or the voltage that had previously been stored in the load capacitor. Because of this problem, the suggested circuit has lower latency and dynamic power consumption values.

5.2 Dynamic GDI Full adder .

A digital circuit known as a complete adder may add three binary bits, usually two at a time. significant bit and a carry-in bit. It generate a sum and a carry-out bit, which can be used for cascading multiple adders together to handle binary numbers of arbitrary length.

A full adder is a combination device which compresses Three partial products into two partial products.Compressors, parity checkers, comparators, and other circuits involving arithmetic operations all require multipliers as vital components.Fig. 5.1 (a) displays the whole adder's block diagram. It takes in three inputs, A, B, and Cin, and outputs two: Carry and Sum. Various logic topologies can implement a complete adder cell. Generally speaking, though, it consists of three primary modules. To generate either the XOR or the XNOR function, or both, the first module is necessary. The last module produces carry output, while the second module generates total.

Figure 5(a) depicts the traditional construction of a complete adder, which has two XOR gates in the critical path. The multiplexer (MUX) produces the carry output, while the second XOR generates the sum output. Moreover, full-adders are regarded as one of the most crucial components in the design of computational logic circuits, including memory units and caches, test and address production, and arithmetic logic units (ALU). Consequently, in order to maximize overall computing efficiency, complete adders must be built to achieve low values for power consumption, latency, PDP, and transistor count.

The conventional build of a full adder, with two XOR gates on the critical path, is shown in Figure 5(a). The second XOR generates the sum output, while the multiplexer (MUX) produces the carry output. Moreover, full-adders are regarded as one of the key components in the design of memory units and caches, computational logic circuits, test and address production, and arithmetic logic units (ALU). To enhance total processing efficiency, complete adders must be built to achieve low values for power consumption, latency, PDP, and transistor count.

The M2, M4, and M6 transistors are "ON" while the M1, M3, and M5 transistors are "OFF" when the CLK signal is "0," as shown in Figs. 5.5. This permits the CL capacitor to be charged up to the VDD level (pre-charge phase). The load capacitor CL discharges to ground if the GDI block output exceeds the threshold voltage of the M1, M3, and M5 transistors; otherwise, it maintains its original logic level. On the other hand, when the CLK signal is "1″, the M2, M4, and M6 transistors turn "OFF." Therefore, the suggested combination of GDI and dynamic circuit approaches is realized by using the CLK input signal at the source terminal of the M1, M3, and M5 transistors.

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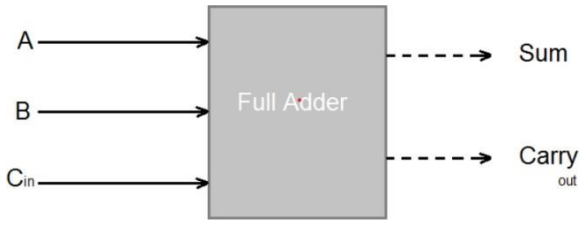


Inputs			Outputs	
A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig-5.2 (a) Basic Block Diagram **Fig-5.2 (b) Truth Table of Full adder**

A complete adder takes three one-bit inputs, adds them together, and outputs a single two-bit number. This can be thought of as a 3:2 compressor.

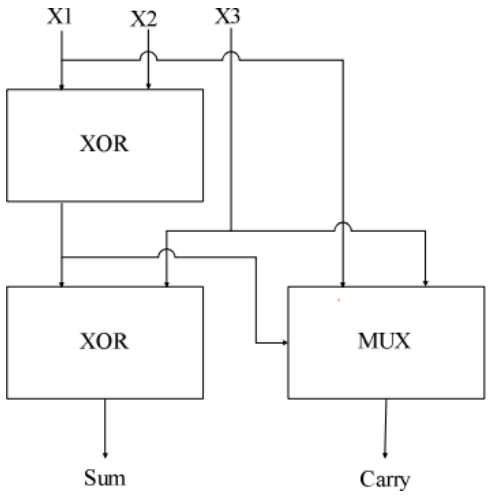


Figure 5.3. Architecture of Full adder

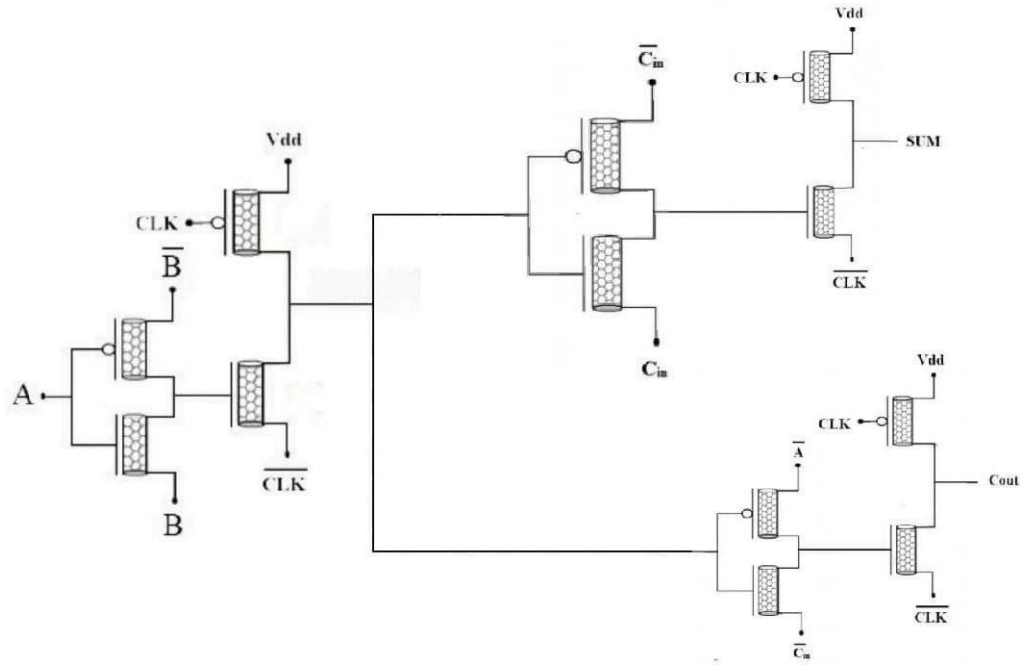


Figure 5.4 Dynamic GDI Full adder

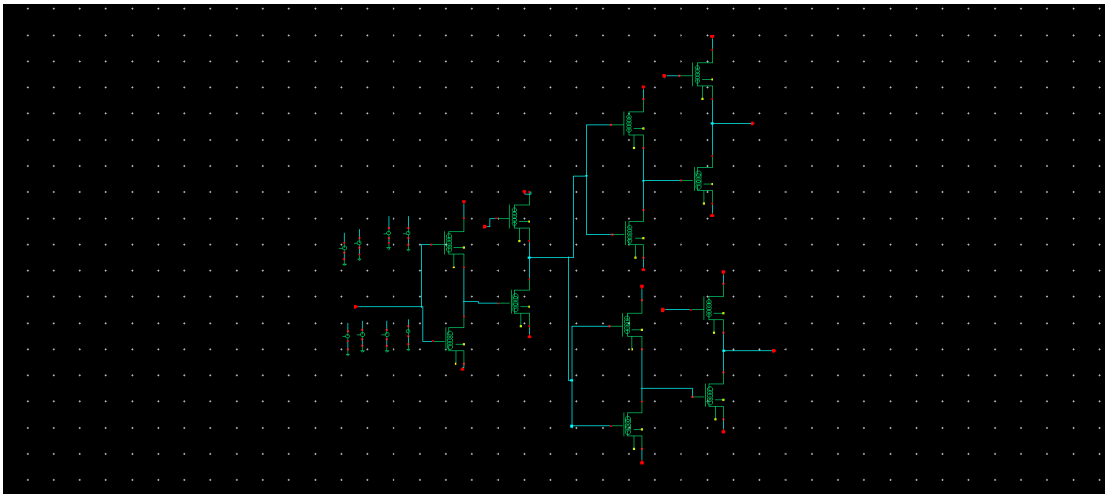


Figure 5.5 Circuit Schematic of Dynamic GDI Full adder .

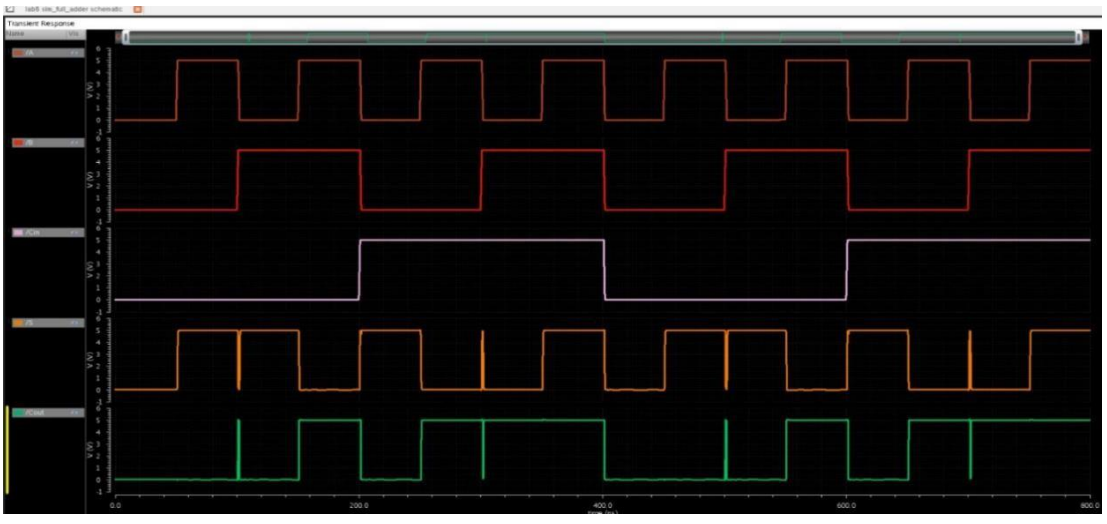


Figure 5.6 Output Waveform of Dynamic GDI Full adder.

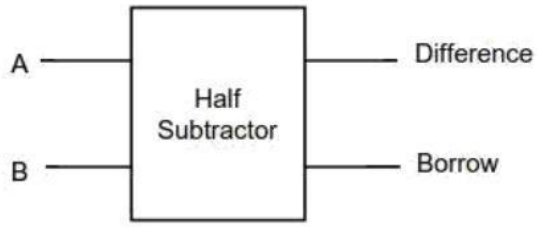
5.3 Dynamic GDI Half - Subtractor .

In digital electronics, a half subtractor is a combinational logic circuit that used to subtract two binary numbers. The difference and the borrow are the two outputs that are generated from two input bits. Larger binary integers can be added by cascading many full adders, which makes the An integral part of computer arithmetic is the complete adder.

We can locate the boolean expression in a truth table.

Borrow = A' B

Difference = A ⊕B



Inputs		Outputs	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Figure 5.7.(a) Block Diagram of Half -Subtractor **Figure 5.7. (b) Truth Table for Half Subtractor**

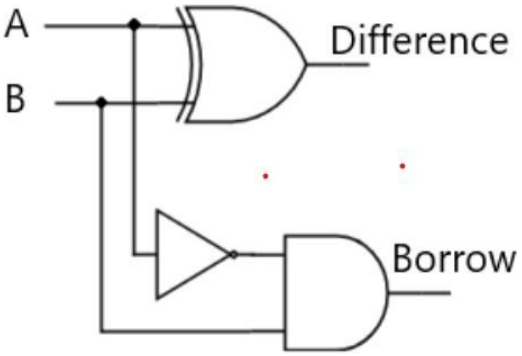


Figure 5.7. (c) Circuit Diagram of Half -Subtractor

Half subtractor is a fundamental component in digital systems, used for basic binary subtraction without considering previous borrow (unlike a full subtractor, which does). Understanding half subtractors is crucial for learning more complex arithmetic operations in digital electronics.

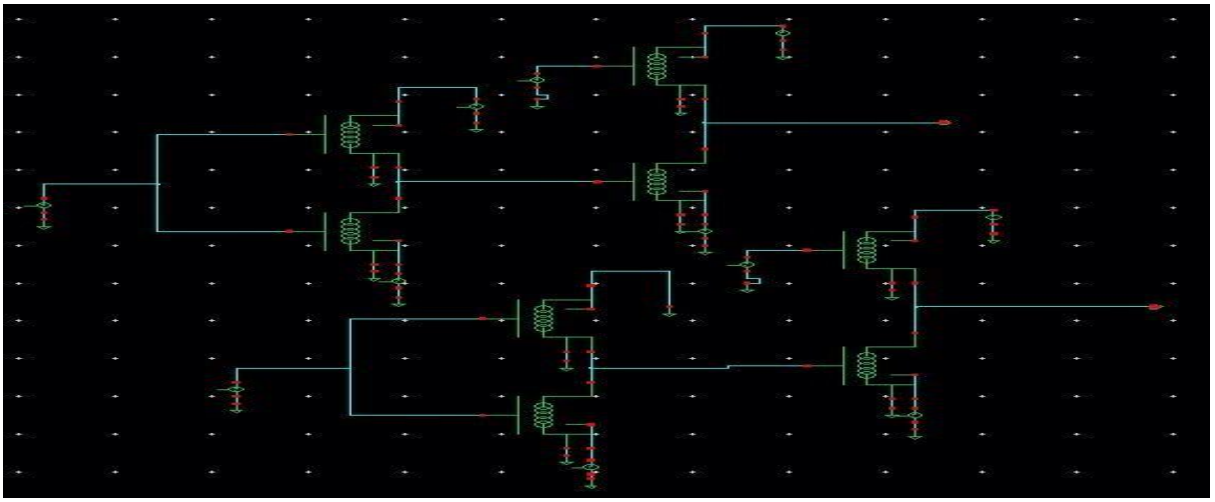


Figure 5.8. Circuit Schematic of Dynamic GDI Half subtractor .

Figure 5.9. Output Waveform of Dynamic GDI Half subtractor.

5.4 Dynamic GDI Encoder

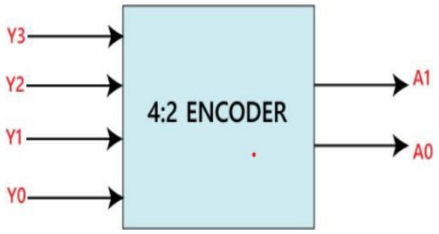
Known as encoders, these combinational circuits convert binary data into N output lines. Two N input lines are used to transmit the binary data. The binary information's N-bit coding is defined in the output lines. To put it simply, the Encoder reverses the actions of the Decoder. For simplicity, only one input line is active at a time. The binary data is equivalent to the generated N-bit output code.

4 to 2 Encoder :

These combinational circuits, also referred to as encoders, translate binary data into N output lines. The binary data is transmitted across two N input lines. The output lines define the N-bit coding for the binary data. In short, the Decoder's activities are reversed by the Encoder. There is only one active input line at a time for simplicity. The resulting N-bit output code is equal to the binary data.

$A_1=Y_3+Y_2$

$A_0=Y_3+Y_1$



INPUTS				OUTPUTS	
Y_3	Y_2	Y_1	Y_0	A_1	A_0
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

Figure 5.10. (a) Block Diagram of Encoder **Figure 5.10 (b) Truth Table for Encoder**

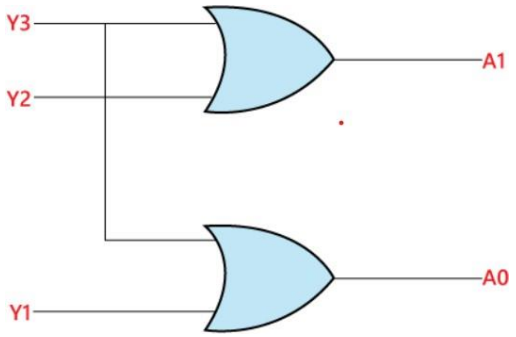


Figure 5.10 (c) Circuit Diagram of Encoder

Comprehending encoders is essential for creating effective digital systems since they reduce the amount of wires needed and make circuit complexity simpler.

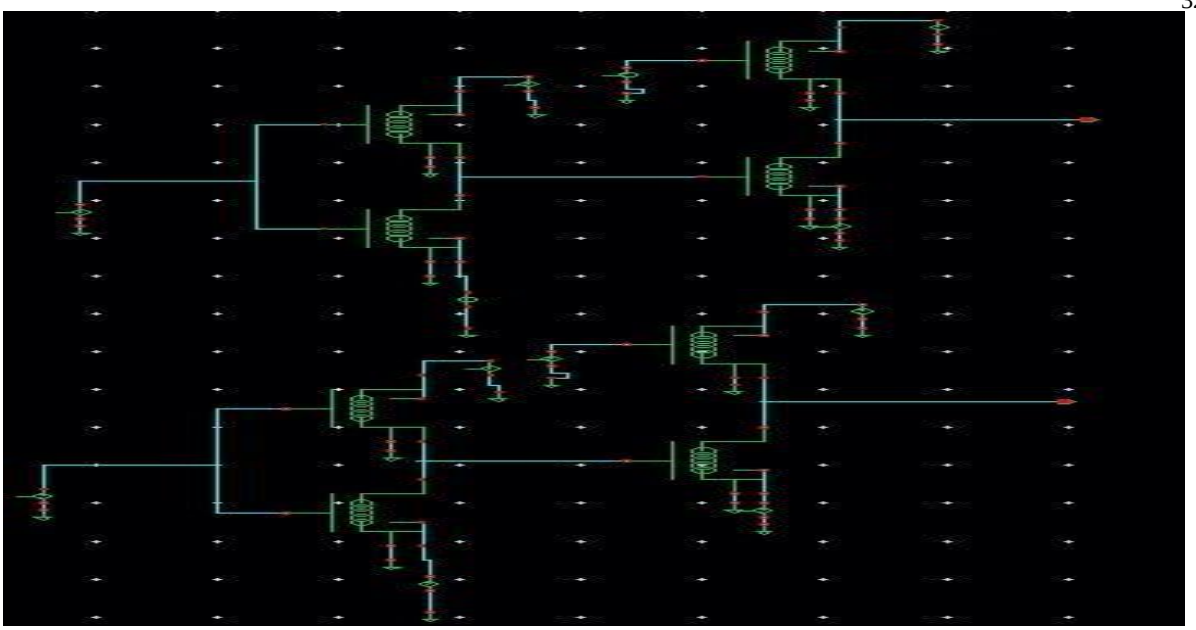


Figure 5.11. Circuit Schematic of Dynamic GDI Encoder

Figure 5.12. Output Waveform of Dynamic GDI Encoder.

Chapter 06 FINAL RESULT

6.1 Simulation Results

PARAMETERS	Full Adder	Half Subtractor	Encoder
DELAY (ps)	35.4	17.6	18.2
POWER (uW)	0.125	0.187	0.125
POWER DELAY PRODUCT (PDP) (aj)	4.5	2.17	2.275

Chapter 07 CONCLUSION

7.1 Conclusion

In the summary, of Major project a dynamic GDI approach, a low-power full adder circuit based on Cntfet technology, is based on the appropriate fusion of dynamic logic style with the GDI low-power technique. has been implemented. As demonstrated in the project, the logic design can be thought of as an energy-efficient circuit in which the circuit's speed is increased and power consumption is greatly decreased, resulting in the lowest PDP. (Power Delay Product) and also get Full swing , The logic design, as shown in the project, canbe viewed as an energy-efficient circuit that has the lowest PDP due to its enhanced speed and much reduced power consumption.

For the design purpose we have used Stanford CNTEFT modelVerilog A with 32nm technology parameters.The design tool used for the simulation is **Cadence Virtuoso.** Furthermore, the Monte-Carlo analysis is carried out to look into the non-idealities impacts that result from the undesired process and manufacturing fluctuations on the overall performance of the circuit.

Dynamic GDI logic full adder design has been implemented for better efficiency and reduced power consumption.The existing design based on Compressor when compared with the our design of D-GDI we can conclude that; our design reduces the chip area as the number of transistor requirements are less. Finally, the circuit simulation results confirm that we have reduce to 28% ,and we reduce power 20% And overall Power Delay Product reduce apporximately 28%. Our full adder has good low-power performance of the circuit.

7.2 Future Work

There remains massive scope to further optimize the performance of Dynamic -GDI circuits and develop and implement . Some of the future direction includes:

- Fabrication of proposed D-GDI circuits on IC chips.
- To work on noise analysis and leakage current .
- To develop system architecture for D-GDI circuits.
- Simulations and further realization of circuits at sub 10nm level

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