DESIGN AND IMPLEMENTATION OF A 10T SRAM CELL UTILIZING LOW POWER TECHNIQUE

Thesis Submitted
In Partial Fulfillment of the Requirements for the Degree of

MASTER OF TECHNOLOGY

in

VLSI DESIGN AND EMBEDDED SYSTEM

by

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CANDIDATE'S DECLARATION

I, **Shubham Gupta**, Roll No. **2K22/VLS/18** student of M. Tech (**VLSI Design and Embedded System**), hereby announce that the project Dissertation titled "**Design and Implementation of a 10T SRAM Cell Utilizing Low Power Technique**" which I have submitted to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology is original and has not been copied. This work has never before been used to provide a degree, certificate, associateship, fellowship, or other comparable title or honor.

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CERTIFICATE

I hereby attest that the project report on the topic **Design and Implementation of a 10T SRAM Cell Utilizing Low Power Technique**, submitted by **Shubham Gupta (2K22/VLS/18)** of the Electronics and Communication Department at Delhi Technological University, Delhi, partially fulfills the requirements needed to be awarded a Master of Technology degree. This report details the project work carried out by the student under my supervision. To the best of my knowledge, this work has not been submitted, in whole or in part, for any degree or diploma at this university or any school.

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ACKNOWLEDGEMENT

I would like to convey my sincere thanks and debt of gratitude to my very recognised and valued mentors, **Dr Harikesh and Dr Manjeet Kumar**, for helping me on this research and granting me all autonomy and adaptability in my work. Their encouragement has been tremendously inspiring and encouraging, and it has always gotten stronger over time. I could not have attempted this Report without their unwavering support and direction.

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M.TECH: VLSI Design & Embedded System

(2022-24)

ABSTRACT

***Abstract* — As technology advances, several improvements are being demanded from cache memories and in turn from the SRAM cell with regards to certain aspects such as stability, access speed, power consumption, etc. A 10T SRAM cell architecture is proposed, which is enhanced with respect to the aspects mentioned above. According to the simulation findings, it is established that the proposed model has lower power consumption (i.e., 51.7nw) compared to the 10T SRAM cell (i.e., 65.14nw). The analysis associated depicts that the read latency of the proposed model is 110.9ps, which is lower than the 10T SRAM cell(i.e., 165.6ps). All the simulations were performed using Cadence Virtuoso software, operating at 1 volt, with 45 nm CMOS process technology. The proposed 10T SRAM cell has better performance and low power consumption than the compared design.**

Keywords— 10T SRAM, low power, Delay, Butterfly curve, ONOFIC Technique, SNM (Static Noise Margin).

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CHAPTER 01

INTRODUCTION

1.1 INTRODUCTION

Static Random Access Memory (SRAM) cell is a type of semiconductor memory that is widely used in a variety of electronic devices, from microprocessors and microcontrollers to cell phones and cache memory in computers. SRAM is a fundamental building block of computer memory systems. Low power consumption and high speed operation are well-known characteristics of the SRAM cell, making it an essential component in various electronic devices, such as microprocessors, cache memories, and graphics cards. In contrast to Dynamic RAM (DRAM), which needs regular refreshing to preserve data, Static RAM (SRAM) maintains data continuously as long as power is available, offering greater speed and reliability for specific uses. SRAM is commonly used in cache memory because it can be accessed more quickly than DRAM, providing faster data retrieval for the processor. This speed is crucial for maintaining high performance in computing systems. Additionally, SRAM's ability to operate at lower power levels makes it ideal for battery-powered devices where energy efficiency is paramount. As the demand for faster and more efficient computing continues to rise in the future, SRAM cells are expected to play a crucial role in meeting these requirements. With the increasing adoption of artificial intelligence, Internet of Things, and edge computing applications, the demand for SRAM cells is expected to grow even further, driven by the need for high-speed data processing, low-latency access, and power efficiency. Additionally, emerging technologies such as self-driving cars, smart cities, and advanced robotics will also contribute to the increased demand for SRAM cells in the future, making them a vital component in the evolving landscape of computing and information technology.

Throughout history, semiconductor memories have been a crucial component of computer storage systems. Development in this subject has been fueled by the constant need for more storage space with less power and space, particularly in random-access

memories (RAMs), which provide faster read and write rates than other memory types. SRAM and DRAM are two of the most popular varieties of RAM. SRAMs are far quicker than DRAMs, compatible in CMOS based technology, and don't require refreshing circuits to retain their data when the power supply is on, despite the fact that they often require a greater space and cost more.

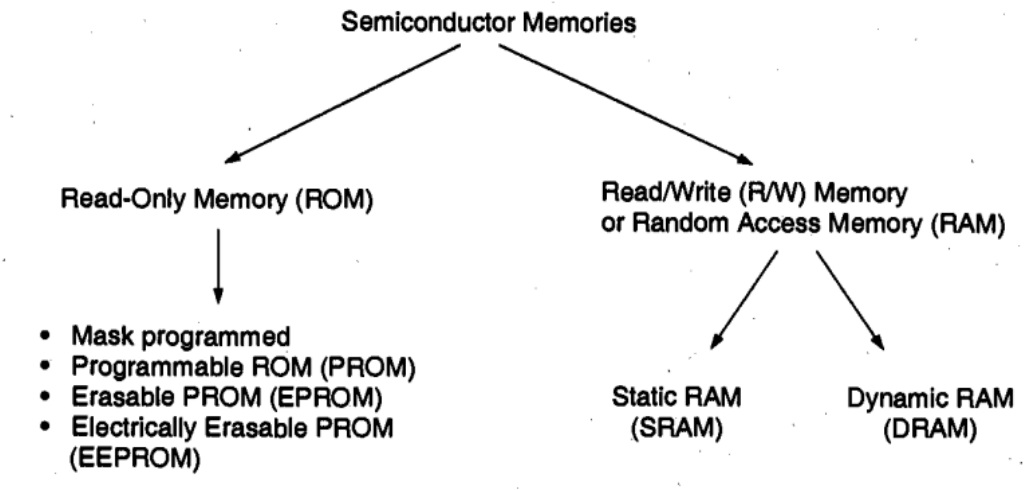


Figure 1.1. Overview of semiconductor memory types

Access time of memory is the amount of time needed to save and/or retrieve a specific data bit from the memory, and is one of the crucial factors for memory speed. Lastly, given the growing significance of low-power applications, the power consumption by memory is an important design consideration.

In the sections that follow, we will examine various memory types. Memory circuits are often categorized based on the kind of data access and storage. As the name suggests, read-only memory (ROM) circuits only provide the recovery of previously recorded data, they do not permit the alteration of the stored information contents while the circuit is operating normally. ROMs are non-volatile memories, meaning.

For primarily historical reasons, the read-write memory circuit is generally referred to as Random Access Memory (RAM). RAMs are divided into two primary groups based on the way that individual data storage cells function: SRAM and DRAM. An overview of the many forms of memory is presented in Figure 1.1.

1.2 RANDOM ACCESS MEMORY (RAM)

Random Access Memory, or RAM, is a form of computer memory than temporarily stores information and commands that are utilised by the Central Processing Unit (CPU) during task completion. RAM is a volatile memory, which implies that it requires a constant power supply to maintain the recorded data. When the computer or laptop power supply is turned off, all RAM-stored data is lost.

1.2.1 Types of RAM

Generally RAM divided in two major types:

(i) Static RAM

(ii) Dynamic RAM

Static RAM

Static RAM (SRAM) is a type of random-access memory which retains data bits for so long as power is provided. SRAM, unlike dynamic RAM (DRAM), doesn't need regular updating.

Figure 1.2. Static RAM

Characteristics of Static RAM

➢ SRAM is significantly quicker than DRAM.

➢ SRAM has more storage than DRAM.

➢ SRAM requires less electricity to operate.

Advantages of Static RAM

➢ SRAM is minimal in power consumption.

➢ SRAM provides quicker access rates than DRAM.

➢ SRAM aids in the creation of a speed-sensitive cache.

Disadvantages of Static RAM

➢ SRAM has a lower memory capacity.

➢ SRAM has greater production costs than DRAM.

➢ SRAM has a more sophisticated design.

Dynamic RAM

The acronym DRAM stands for Dynamic Random Access Memory. It is a type of random access memory that allows you to store individual data bits in independent capacitors within an integrated circuit. Many modern desktop PCs come with dynamic RAM is like standard memory.

Figure 1.3. Dynamic RAM

Characteristics of Dynamic RAM

➢ DRAM is weaker than SRAM.

➢ DRAM is lesser expensive than the SRAM.

➢ DRAM has a high electrical consumption.

Advantages of Dynamic RAM

➢ DRAM offers lower production costs than SRAM.

➢ DRAM provides higher memory capacity.

Disadvantages of Dynamic RAM

➢ DRAM has sluggish access speeds.

➢ DRAM has a significant power consumption.

➢ Power outages might result in the loss of DRAM data.

1.3 MOTIVATION

The motivation for research into 10T SRAM cells is driven by the growing demand for high-performance, low-power memory solutions in modern computing. As advancements in technology continue, and with the rise of data driven applications like artificial intelligence, virtual reality, and big data analytics, conventional 6T SRAM cells face challenges concerning their stability, leakage current, and energy usage. The 10T SRAM cell architecture, with its additional transistors, offers enhanced stability, reduced leakage, and improved read and write capabilities. Studying 10T SRAM cells allows us to explore their potential benefits and limitations, leading to more efficient and reliable memory designs for future computing systems.

The relentless demand for extended battery life in portable electronics and energy-efficient computing systems fuels the continuous evolution of low-power memory design. SRAM, a cornerstone of modern processors, contributes significantly to overall system power consumption. Conventional 6T SRAM cells, while ubiquitous, face limitations in power efficiency, particularly at smaller technology nodes. Leakage currents, even during standby mode, become a major concern. Furthermore, reducing the supply voltage (Vdd) for lower power can compromise stability and performance. 10T SRAM cells offer a compelling path to overcome these challenges. Their additional transistors enable the implementation of innovative low-power techniques. These techniques, such as sleep transistors and assist circuits, can significantly reduce leakage currents and improve write margin at lower Vdd, enabling lower power operation without sacrificing functionality. By addressing the critical need for energy-efficient memory solutions, this research paves the way for a future of sustainable and efficient computing, empowering the ever-growing world of portable and battery-powered electronics.

1.4 OBJECTIVE

The objective of this research is to investigate and analyze the performance characteristics of SRAM cells. SRAM cells are integral components of modern digital systems, playing a crucial role in memory storage and data retrieval. With the increasing demand for high speed and low-power memory solutions, it is essential to explore and understand the behavior of advanced cell designs. By focusing specifically on 10T cells, this research aims to explore their advantages, limitations, and potential

applications. Through rigorous experimentation and analysis, the objective is to provide valuable insights and contribute to the advancement of SRAM technology for future computing systems. The design and implement a 10T SRAM cell incorporating advanced low power techniques, aiming to reduce power consumption while maintaining high performance and stability. This involves developing a schematic for the 10T SRAM cell and implementing strategies to lower power usage during read and write operations. Additionally, the stability and reliability of the SRAM cell will be enhanced, ensuring it can effectively store and retrieve data despite variations and noise. Ultimately, this research aims to contribute to the development of more energy-efficient memory solutions, particularly in portable and battery powered devices, addressing the pressing need for sustainable technology solutions in modern electronics.

CHAPTER 02

LITERATURE REVIEW

In every discipline, inspecting the previous research is always crucial. A literature review seeks to offer a comprehensive understanding of the topic through examination of previous studies. This keeps work from being copied and recognises the efforts of other investigators. A review of the published research can also be used to discover new possibilities, inconsistencies, gaps in the research and unsolved concerns from earlier studies. The literature review of the earlier research is addressed in this chapter.

2.1 PREVIOUS REPORTED WORK:

R. Lorenzo et al. [1], propose a LCNT technique which results in reduction of the leakage power dissipation which is the major issue in nanoscale CMOS integrated circuits. The various existing techniques for minimising leakage have been reviewed, revealing their strengths and weaknesses. This study introduces the Leakage Control NMOS Transistors (LCNT) technique, which adds two NMOS transistors to standard CMOS circuits to control leakage. This technique significantly reduces leakage power compared to the existing technique.

C. Kumar et al. [2], proposes the stack ONOFIC approach reduces leakage power in CMOS logic devices. The technique's efficacy is illustrated utilizing a variety of CMOS logic circuits such as the NAND gate, inverter, and NOR. It is compared to classic LECTOR and LCNT reduction methods. Compared to earlier techniques, the suggested stack ONOFIC technology produces results for reducing power dissipation.

S.H. Choudhari et al. [3], presents the comparison between different SRAM cell topologies focused on the low power and leakage power reduction. Leakage power reduction in memory is crucial, and techniques like Gated Vdd, Source Biasing, Sleep Stack, and MT-CMOS are effective. This research examines 6T SRAM cells utilizing 90 nm technology within Cadence Virtuoso, evaluating the performance of various SRAM cells, including 6T, 7T, 8T, 9T, and 10T configurations. The analysis considers leakage currents, power consumption, and read behavior, with a particular emphasis on

parameters such as power usage and read/write delay. The findings indicate that the proposed 10T SRAM cell outperforms the others in terms of leakage power and delay.

E. Abbasian and M. Gholipour [5], introduced a transmission gate-based 10T SRAM cell designed for IoT applications. This cell was evaluated against 6T, TG-8T, and fully differential 8T cells under extreme PVT variations. The proposed 10T SRAM cell uses a differential method to increase the sensing margin and two transmission gates (TGs) rather than two NMOS access transistors to improve readability. Furthermore, it includes two additional buffer transistors to improve read stability. With a larger number of PMOS devices, the TG10T cell efficiently minimises leakage power dissipation. Overall, this cell delivers superior performance compared to other SRAM configurations, making it well-suited for IoT applications.

R. Krishna et al. [6], Presents A 10T SRAM cell featuring a source-biased inverter for deep submicron applications. This source-biased inverter features two extra transistors to reduce leakage power without increasing dynamic power. The additional transistors raise the source voltage, lowering the drain-to-source voltage and effectively reducing leakage power usage. Additionally, support techniques are used to improve stability.

P. V. Kiran et al. [7], presents the design and comparison of various SRAM cells, including the conventional 6T, as well as 7T, 8T, 9T, and 10T topologies. The study focuses on the leakage currents, leakage power, and read behaviour of each SRAM cell type. The 10T SRAM cell reduces leakage power and current while improving read stability compared to other architectures. The purpose of this research is to maintain low read and write access times and power consumption while reducing leakage power and current and boosting read performance across varied SRAM cell designs.

V. K. Joshi et al. [8], provides comparisons of the performance of 6T, 7T, 8T, 9T, and 10T SRAM cells. This article compares power, performance, and stability. According to the study, 10T cells are more stable than 6T cells. Similarly, other SRAM cells were compared to the 6T SRAM cell. The tool was used to create SRAM cells and layouts. Post-layout simulation results aligned well with pre-layout simulations.

S.Shaik et al. [9], investigates the design and performance of various standard SRAM topologies, including 6T, 7T, 8T, 9T, and 10T cells, across different technologies (45, 90, and 180 nm). These SRAM cells were analyzed for delay and power dissipation under different supply voltages. Additionally, the layouts of these cells were designed, and their areas were tabulated, providing a comprehensive analysis of their merits and demerits in terms of power consumption, area and delay.

V. Aswini et al. [10], proposes A transmission gate-based SRAM cell architecture optimised for biomedical applications, eliminating the requirement for peripheral circuitry during read operations. In comparison to the standard structure, this novel topology provides a smaller area, less latency, lower power consumption, and enhanced data stability during reads. Delay is optimized when the peripheral circuitry for reading is replaced with the transmission gate and compared with conventional structure.

N. Gupta et al. [11], examines an 8T single-ended static random access memory (SRAM) and compares two methods for lowering sub-threshold leakage current and power consumption. The first technique involves a dynamic variable voltage level (VVL) method to adjust effective supply and ground node voltages, while the second technique focuses on scaling down the power supply. When these strategies are coupled, the 8T SRAM cell with one word line, two bitlines, and a transmission gate performs significantly better. The study shows decrease in both leakage and dynamic power compared to the standard 8T single-ended SRAM cell, while maintaining correct read and write operations.

C. Premalatha et al. [12], Presents the comparative analysis of different SRAM architecture at a particular technology node. It addresses power dissipation in conventional SRAM cell structures during read and write operations by applying a dual-threshold voltage technique. The power dissipation and delay of these cells have been estimated and compared. The analysis concludes that there is always a tradeoff between power, delay, and area. Designers must select strategies that address specific application requirements, with the dual-threshold voltage technique efficiently decreasing power dissipation and delay due to cell structure.

CHAPTER 03

10T SRAM CELL

3.1 ARCHITECTURE & WORKING OF 10T SRAM CELL

The architecture of the 10T SRAM cell incorporates transmission gates to enhance its performance, stability, and power efficiency. Transmission gates, consisting of parallel nMOS and pMOS transistors, provide improved control over signal flow, resulting in better read and write operations and reduced leakage currents. Through the transmission gate, the read operations will be performed.

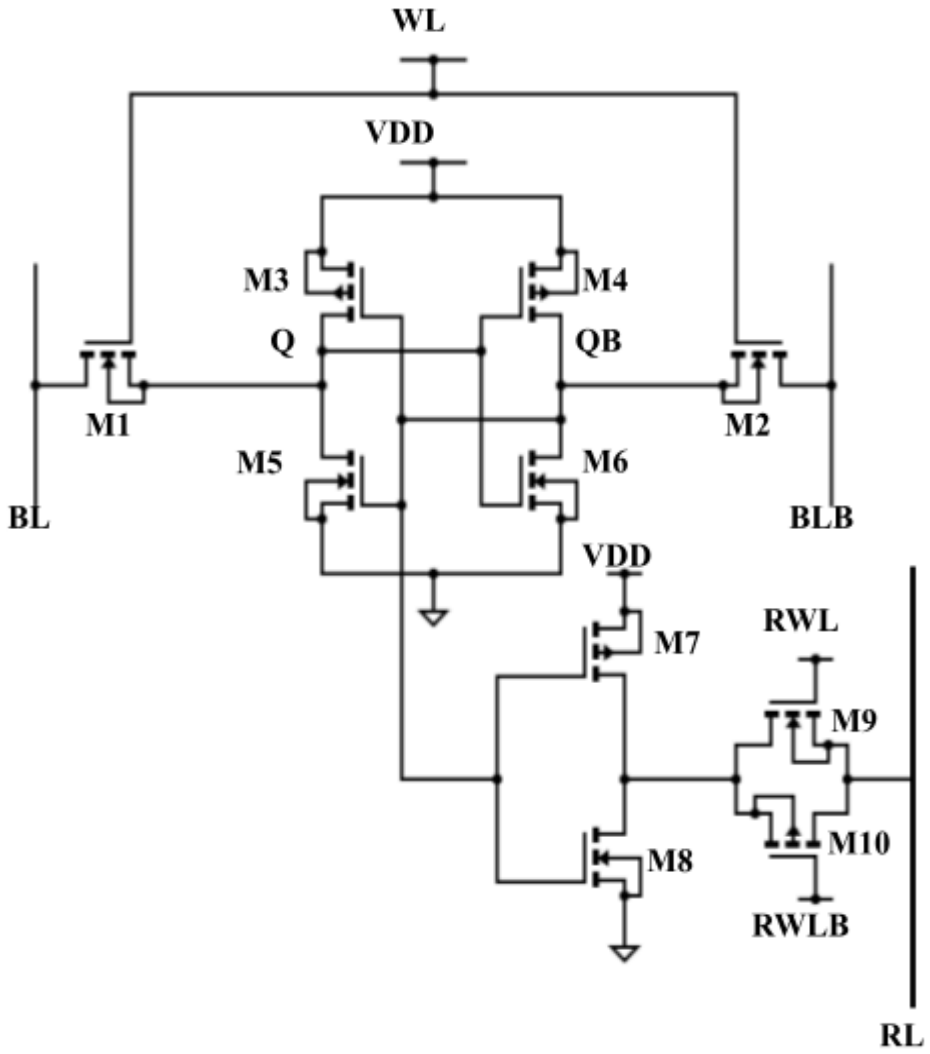


Figure 3.1. 10T SRAM CELL

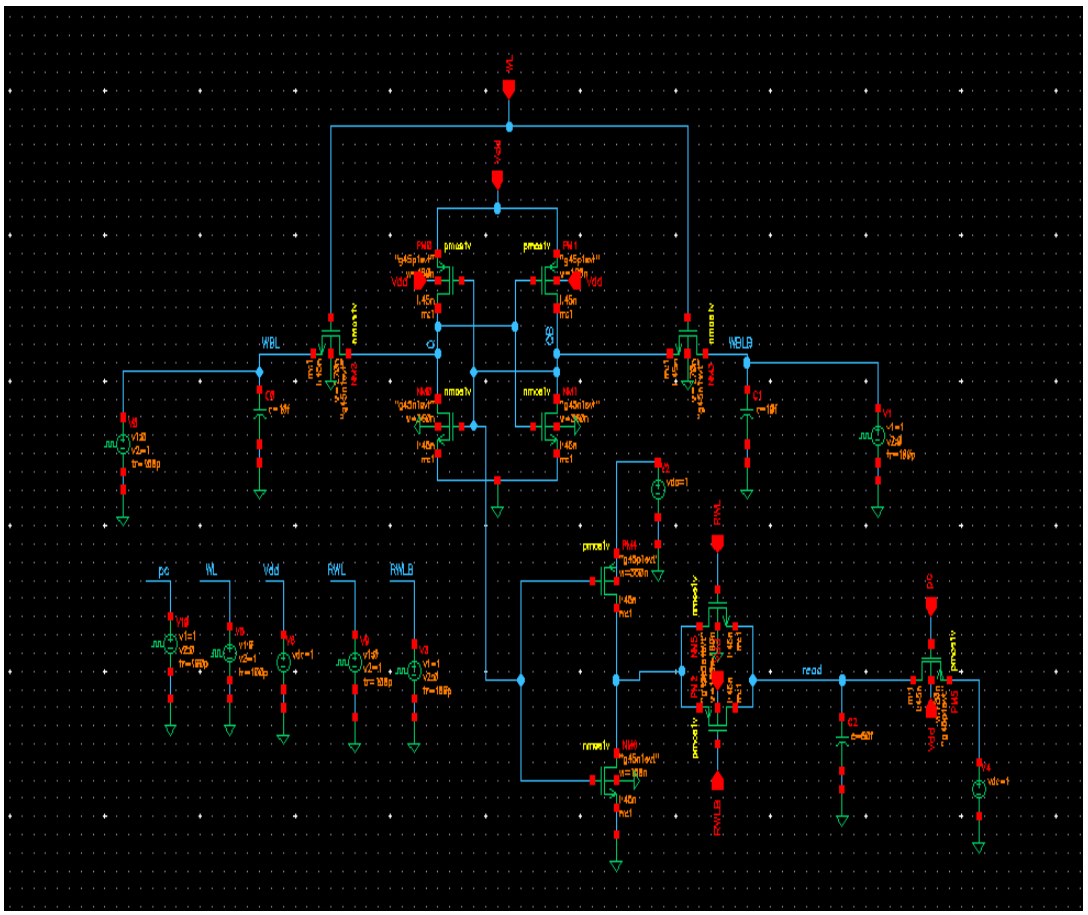


Figure 3.2. SCHEMATIC OF 10T SRAM CELL

Two cross-coupled inverters, similar to those in a 6T SRAM cell, form the storage nodes Q and QB. Two access transistors manage the connection between the bitlines (i.e, BL, BLB), word lines (WL) and storage nodes (i.e., Q, QB) for write operations. Transmission gates control the read pathways, enhancing operational stability and efficiency. The structure incorporates decoupled read and write operations.

Data is stored using a back to back connected CMOS inverter. Then it has two bitlines called Bitline (BL) and Bitline_bar (BLB) that are used to transfer data onto the cell via the access transistor M1 & M2. It is a dual port SRAM cell because it has a separate port for each of read/write operations. Fig. 3.1, the circuit of the 10T SRAM cell [3]. The read operations will be carried out by means of transmission gate. The input through NMOS (M9) of the transmission gate is the Read word line (RWL) and the input through PMOS (M10) of the transmission gate is the reverse of RWL [7] [11]. While both the NMOS and PMOS assert, this takes the transmission gate to an active state which is connected to QB via an inverter. As a result, the value which Q holds can

be read through an inverter. Here the write operation is dependent on WL, BL, and BLB. When WL is 1, NMOS transistors M1 and M2 turn ON and so the value of QB and Q can be obtained. For the read operation to be performed, RWL=1 and RWLB=0. Here the value of Q will be read.

In SRAM architectures, the dimensions of transistors has crucial role in determining the cell's performance, energy and area efficiency. Typically, the dimensions of transistors in SRAM cells are optimized based on the particular requirements of the application and the targeted technology node.

TABLE 3.1

SIZING OF 10T-SRAM

	Access Transistor (i.e., M1, M2)	PU Transistor (i.e., M3,M4)	PD Transistor (i.e., M5, M6)
length	45n	45n	45n
width	270n	180n	360n

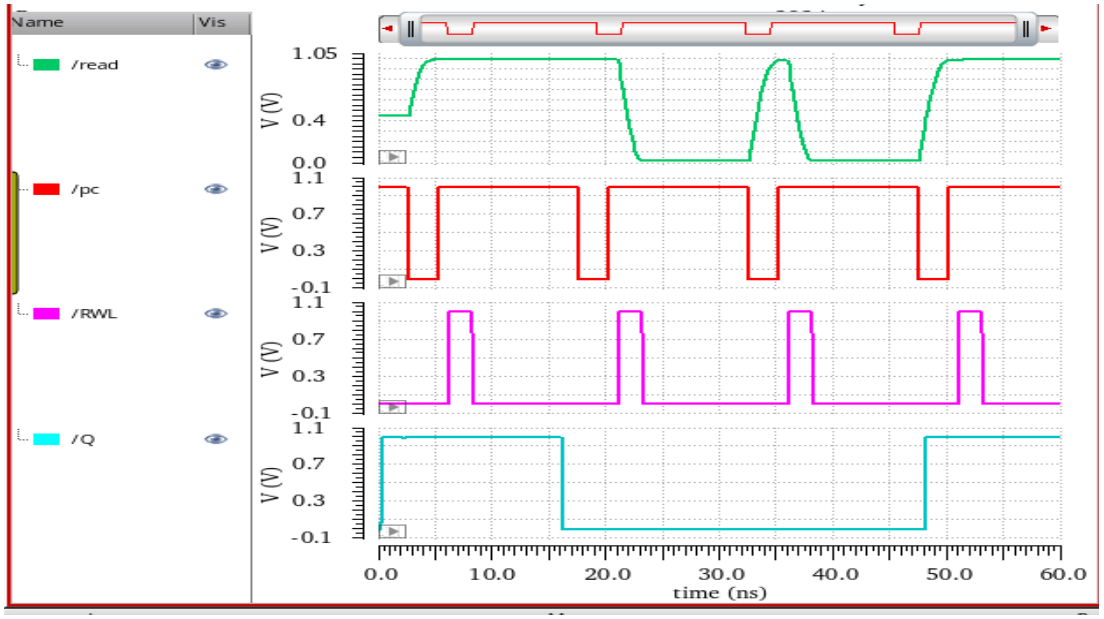
.

Access transistors control the access to storage nodes in SRAM cells during write operations. Their sizing influences the speed of access and the power consumed during these operations. Larger channel widths (W) can enhance access speed but may increase area overhead and power consumption.

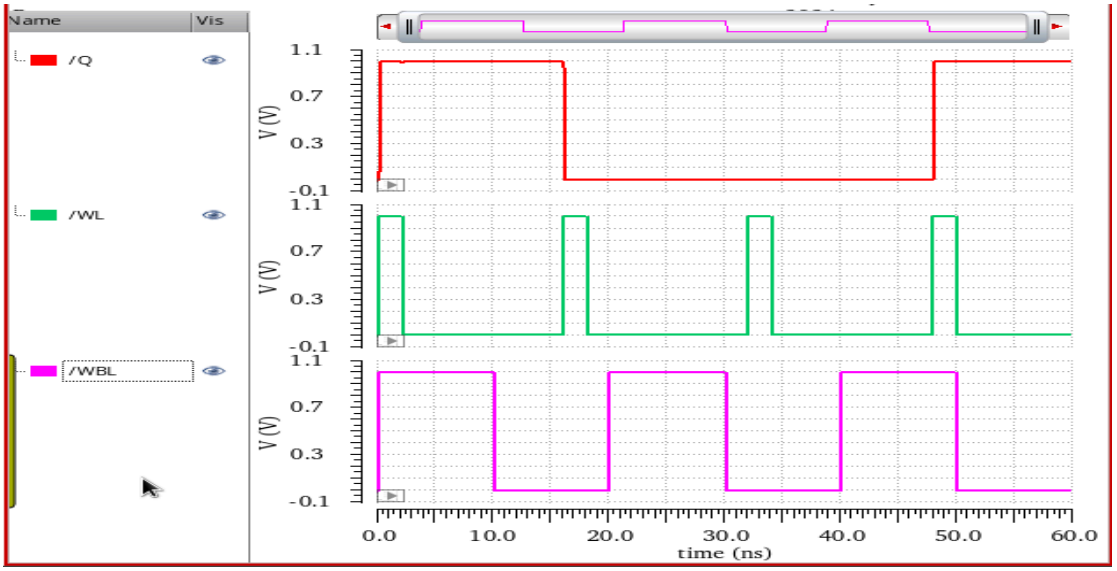
The storage node transistors, forming the cross-coupled inverters, are critical for data storage and stability. Their sizing is optimized to ensure sufficient drive strength for stable storage while minimizing leakage currents. Proper sizing of these transistors is essential to maintain data integrity during read and write operations. Overall, transistor sizing in SRAM architecture involves careful optimization to achieve the desired balance between speed, power and area efficiency.

3.2 SIMULATION RESULTS

In this section, simulation for read and write operation are performed on the 10T SRAM Structure. It involves examining the cell's behavior during dynamic operations such as reading, writing, and transitioning between states. This analysis is essential for understanding the timing characteristics, stability, and performance of the SRAM cell.



(a)



(b)

Fig.3.3. Simulation Results of 10T SRAM cell (a) Read (b) Write

Transient analysis was done on the model to make sure that the read and write operations functioned properly. The results of the simulation for read and write operations are demonstrated in Fig. 3.3 for the 10T SRAM cell.

3.3 ACCESS DELAY

Access delay in SRAM refers to the time taken to access the data that is stored in the memory cell, either during a read or write operation. This delay is a crucial performance metric, affecting the overall speed and efficiency of the SRAM. It is the time interval between the initiation of a read or write operation and the completion of that operation. It is a critical performance metric, impacting the overall speed and efficiency of the memory.

In SRAM access delay is a key performance parameter, crucial for high-speed memory applications. It is usually measured between the time the input signal reaches half of its final value and the time the resulting signal achieves half of its final value. By understanding and optimizing the factors influencing read and write delays, designers can enhance the speed and efficiency of SRAM cells. Consideration of transistor sizing, supply voltage, load capacitance, temperature effects, and technology scaling is essential for minimizing access delay and achieving optimal memory performance.

3.3.1 Write Delay

In a write operation, the write accessing delay is the time between when the word line (WL) signal reaches half of its final value and when the storage node (Q) receives half of its final amount.

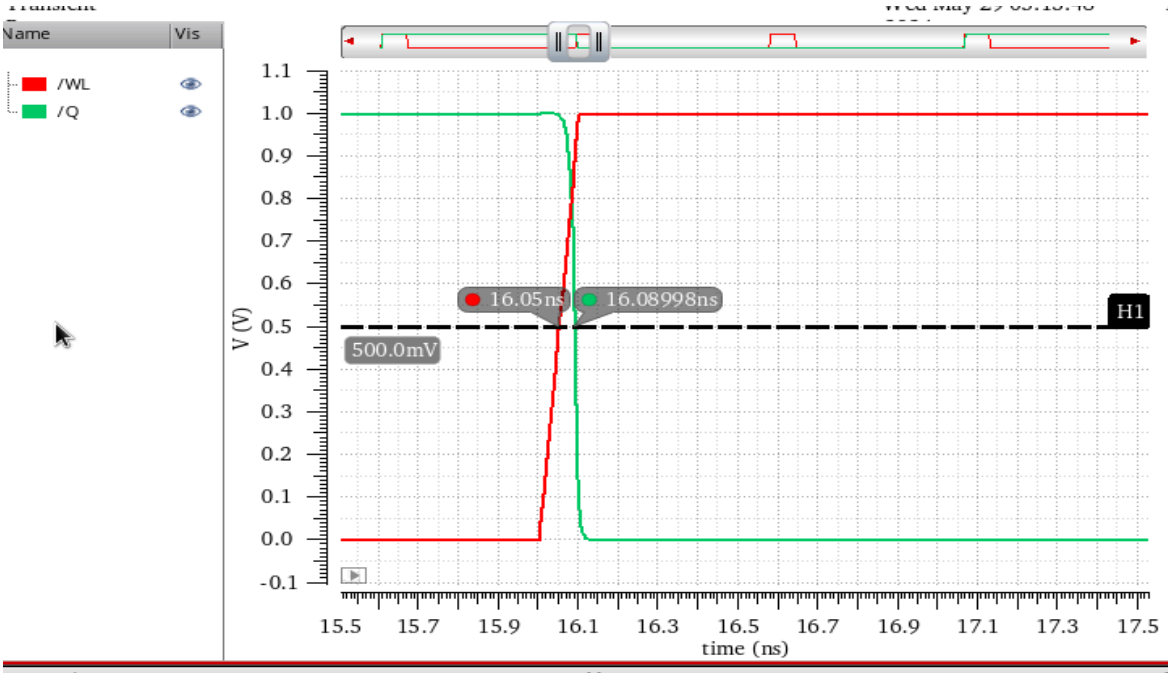


Fig. 3.4. Simulation result for write delay

According to the simulation results shown in Figure 3.4, the write delay for the 10T SRAM cell is 39.98 ps.

3.3.2 Read Delay

For a read operation, the read access delay is the time from when the Read word line (RWL) reaches half of its final value to when the read bitline (RBL) or read output reaches half of its final value.

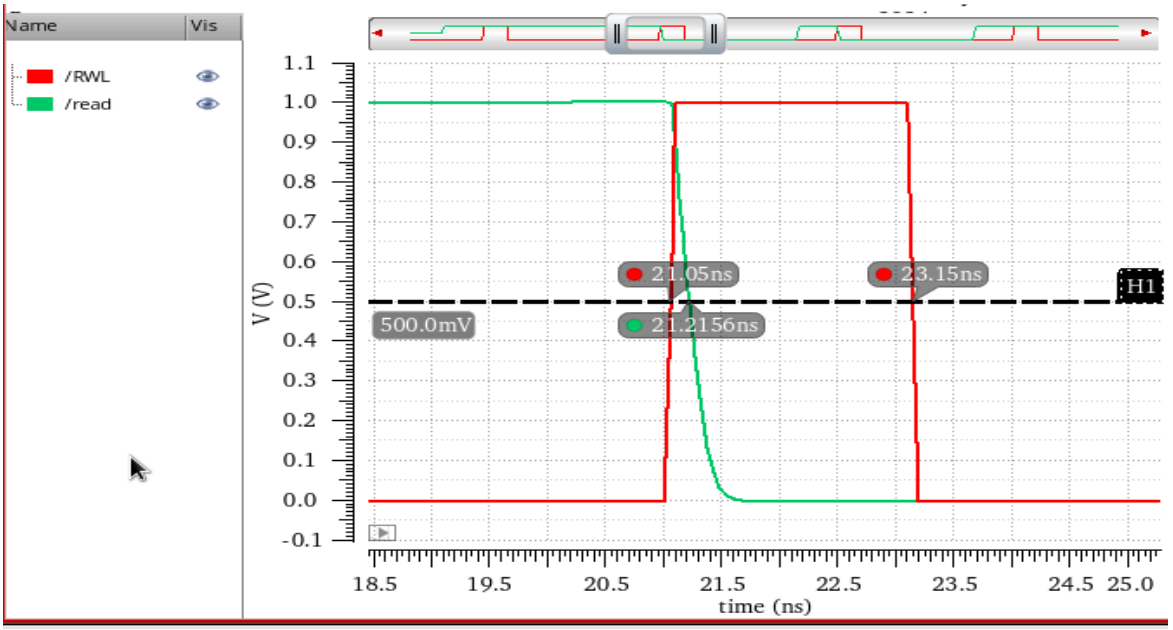


Fig. 3.5. Simulation result for read delay

According to the simulation results shown in Figure 3.5, the read delay for the 10T SRAM cell is 165.6 ps.

3.4 STATIC NOISE MARGIN

The static noise margin (SNM) measures how stable the SRAM is when subjected to noise interference. To calculate the Static Noise Margin (SNM) value, find the most significant square that falls between the two typical butterfly shapes of a static CMOS memory cell. Begin by displaying the voltage transfer characteristics (VTC) for both inverters. The graphs depict the connection across the voltages at the input and output of each inverter. Locate the spots where the two VTC curves intersect. These intersection points are critical because they establish the bounds within which the square can fit. The key to establishing the SNM is to find the longest diagonal that fits completely between the two curves. This diagonal reflects the maximum disturbance voltage that the cell can withstand without changing state. Create a square with the length of this diagonal. This value is important since it measures the memory cell's resistance against noise.

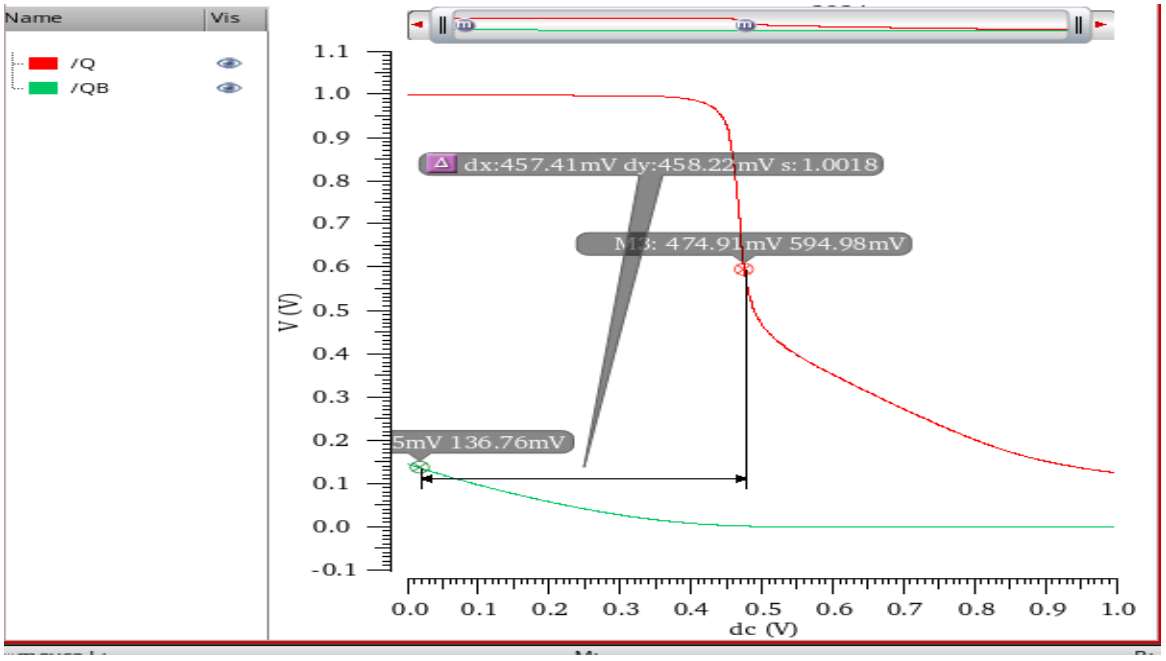


Fig 3.6. WSNM Curve for 10T

Write Static Noise Margin (WSNM) determines the stability of a memory cell with SRAM during the writing process. It shows the ease with which new data can be entered into the cell. High WSNM ensures that the cell can be consistently overwritten with new data, which is required for proper operation. According to the simulation results shown in Figure 3.6, the write SNM for the 10T SRAM cell is 457 mv.

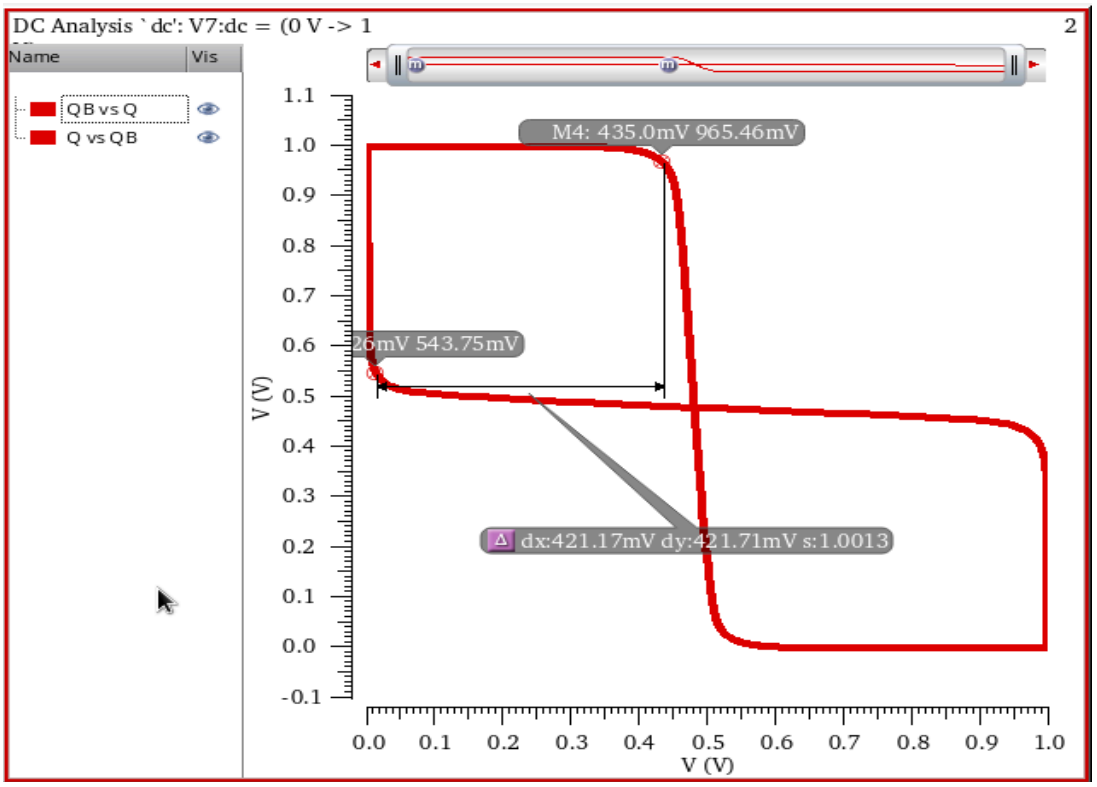


Fig 3.7. RSNM Curve for 10T

Read SNM indicates the maximum noise voltage that an SRAM cell can tolerate during a read operation without altering its stored state. High Read SNM is crucial for ensuring data integrity, especially in high-performance and low-power applications where noise susceptibility is higher due to reduced voltage margins and increased density of cells. According to the simulation results shown in Figure 3.7, the read SNM for the 10T SRAM cell is 421 mv.

CHAPTER 04

10T SRAM CELL WITH LOW POWER TECHNIQUE

The growing demand for portable electronics with extended battery life necessitates continuous advancements in low-power integrated circuit (IC) design. SRAM is a vital component in these appliances, but its leakage power consumption becomes a significant concern at smaller technology nodes [1]. This chapter includes a 10-transistor (10T) SRAM cell design that leverages the ONOFIC technique in a 45nm CMOS process to achieve substantial power reduction compared to 10T SRAM cells.

4.1 ONOFIC TECHNIQUE

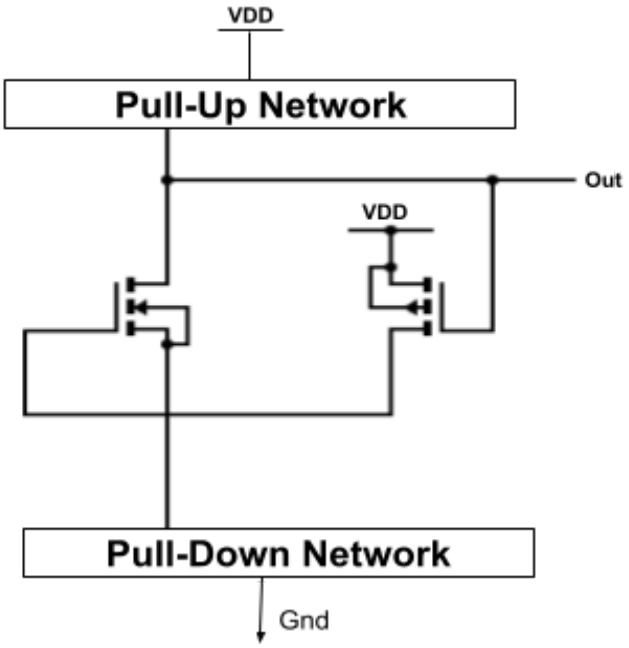


Fig 4.1. ONOFIC

The ONOFIC technique shown in Fig.4.1, offers a promising approach for reducing leakage current in SRAM cells by essentially forcing the logic block into a definitive 'ON' or 'OFF' state during standby mode, thereby minimizing leakage current paths.

The ONOFIC technique incorporates leakage control transistors (LCT) within the logic block, NMOS transistor. An additional PMOS transistor is strategically placed with its

drain connected to the gate of the N-type LCT. The gate terminal of the PMOS transistor connects to the output of the logic block. This configuration ensures that when the output is high, the PMOS transistor turns off, effectively shutting off the N-type LCT, the OFF NMOS transistor is offering highest resistance and minimizing leakage current paths. Conversely, when the output is low, the PMOS transistor turns on, allowing the N-type LCT to operate with least resistance. The ONOFIC technique utilizes a uniform threshold voltage throughout the entire block for design simplicity and ease of control [1][2].

4.2 ARCHITECTURE AND WORKING OF PROPOSED STRUCTURE

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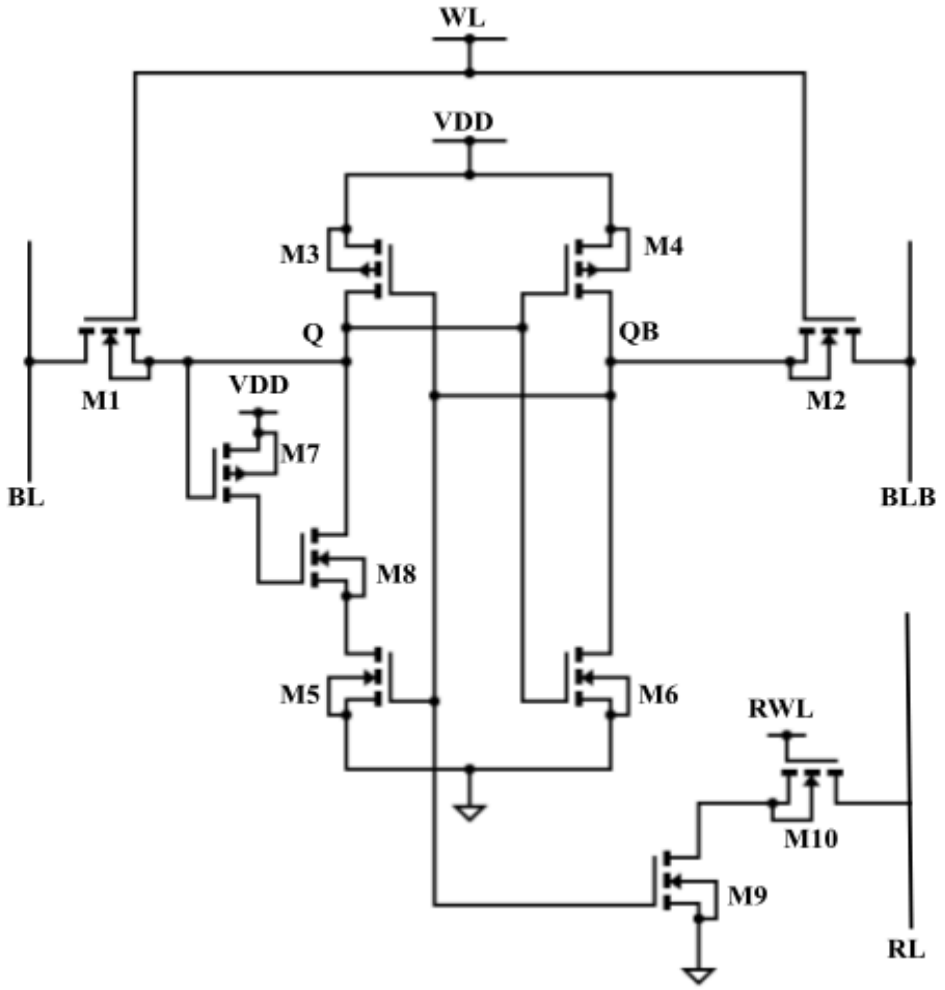


Figure 4.2. PROPOSED 10T SRAM CELL

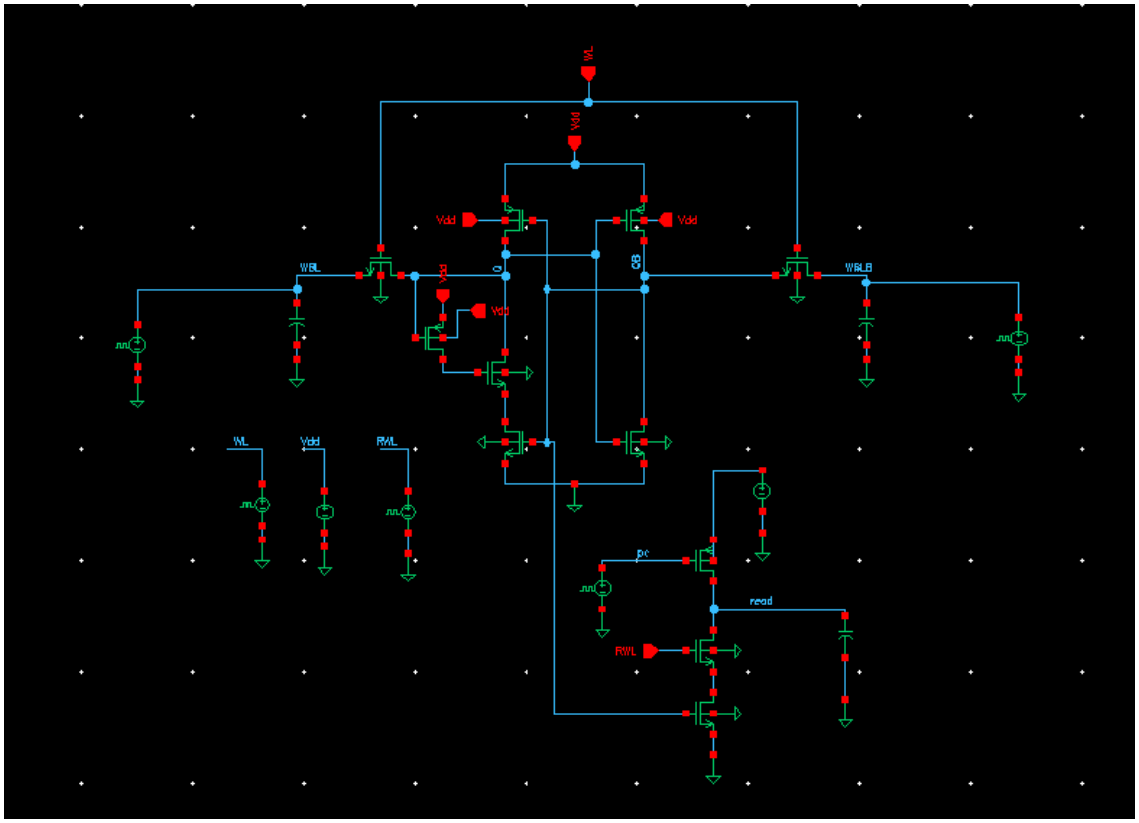


Figure 4.3. SCHEMATIC FOR PROPOSED 10T SRAM CELL

The architecture shown in Fig. 4.1 consists of 10 transistors. It is a dual port SRAM cell because it has a separate port for each of read and write operations. This design incorporates a low-power technique called ONOFIC to minimize the Power consumption. To save power, this design uses M8 as a LCT. The P-type MOS transistor (M7) is strategically placed with its drain connected to the gate of the N-type LCT (M8). The gate terminal of the P-type MOS transistor connects to the output of the logic block. This configuration ensures that when the output is high, the P-type MOS transistor (M7) turns off, effectively shutting off the N-type LCT (M8) which offers highest resistance and minimizing leakage current paths. When the output is low, the P-type MOS transistor (M7) turns on, effectively switching on the N-type LCT (M8) which offers least resistance from output node to ground. Here the write operation is dependent on WL, BL, and BLB. When WL is 1, NMOS transistors M1 and M2 turn ON and so the value of QB and Q can be obtained. For the read operation to be performed, RWL=1. The value of Q will be read at the read line (RL).

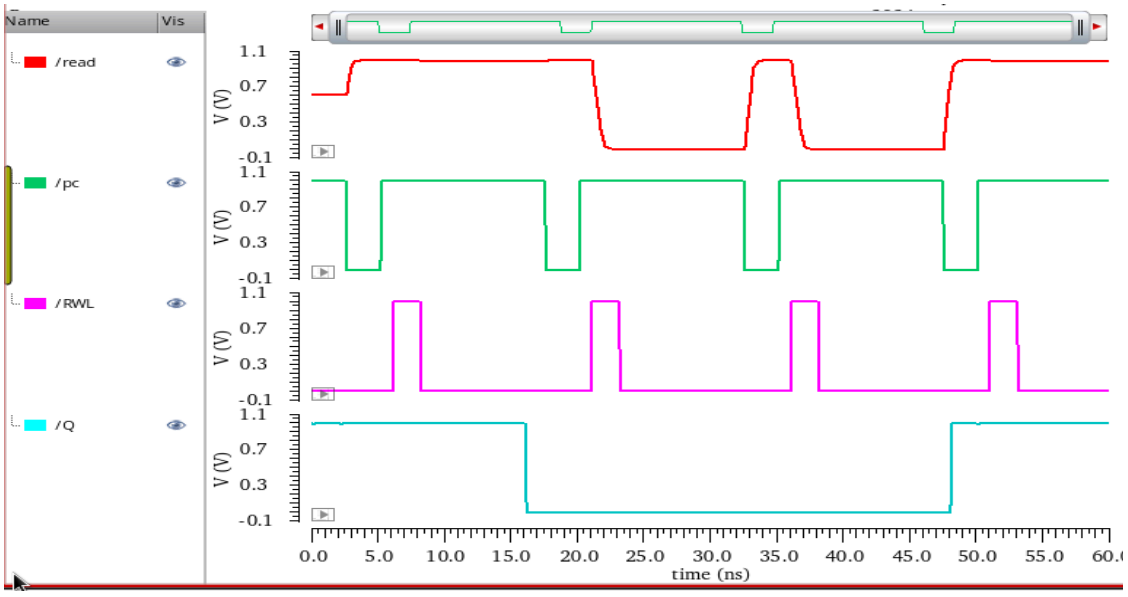
In SRAM architectures, the dimensions of transistors has a crucial role in determining the cell's performance, power and area efficiency. Typically, the dimensions of transistors in SRAM cells are optimized based on the particular requirements of the application and the targeted technology node.

TABLE 4.1
SIZING OF PROPOSED 10T SRAM

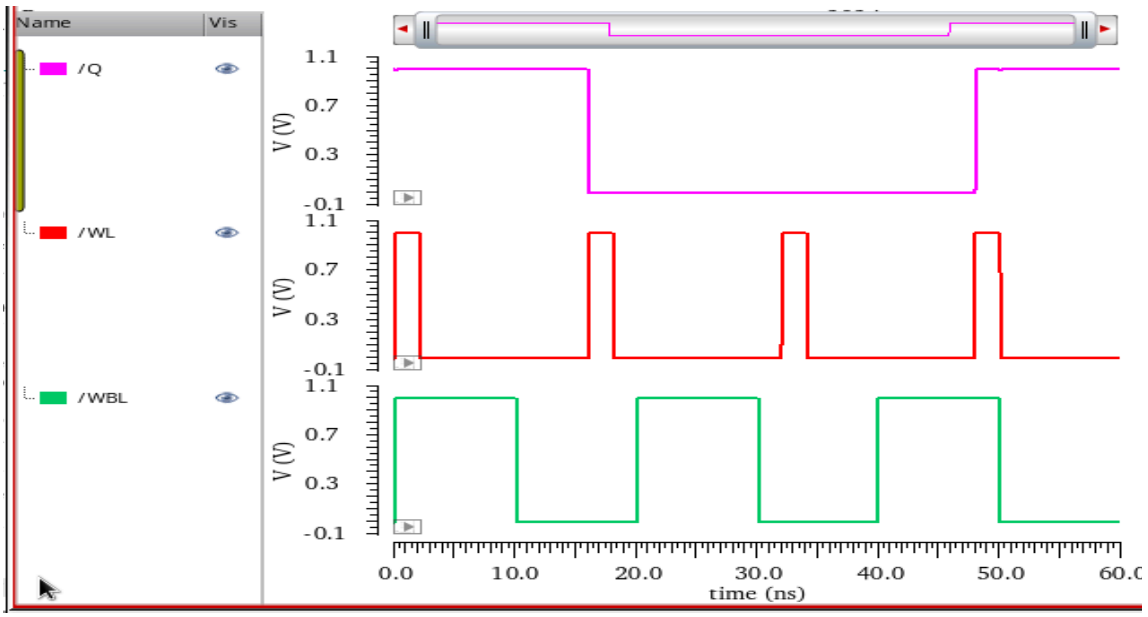
	Access Transistor (i.e., M1, M2)	PU Transistor (i.e., M3,M4)	PD Transistor (i.e., M5, M6)
length	45n	45n	45n
width	270n	180n	360n

4.3 SIMULATION RESULTS

In this section, simulation for read and write operation are performed on the Proposed 10T SRAM Structure. It involves examining the cell's behavior during dynamic operations such as reading, writing, and transitioning between states. This analysis is essential for understanding the timing characteristics, stability, and performance of the SRAM cell.



(a)



(b)

Fig.4.4. Simulation Results of Proposed 10T SRAM cell (a) Read (b) Write

Transient analysis was done on the model to make sure that the read and write operations functioned properly. The results of the simulation for read and write operations are demonstrated in Fig. 4.4 for the Proposed 10T SRAM cell.

4.4 ACCESS DELAY

Access delay in SRAM refers to the time it takes to access the data that is stored in the memory cell, either during a read or write operation. In SRAM access delay is a key performance parameter, crucial for high-speed memory applications. By understanding and optimizing the factors influencing read and write delays, designers can enhance the speed and efficiency of SRAM cells. Consideration of transistor sizing, supply voltage, load capacitance, temperature effects, and technology scaling is essential for minimizing access delay and achieving optimal memory performance.

4.4.1 Write Delay

The write access delay is defined as the time from when the word line (WL) signal reaches half of its final value to when the storage node (Q) reaches half of its final value during write operation.

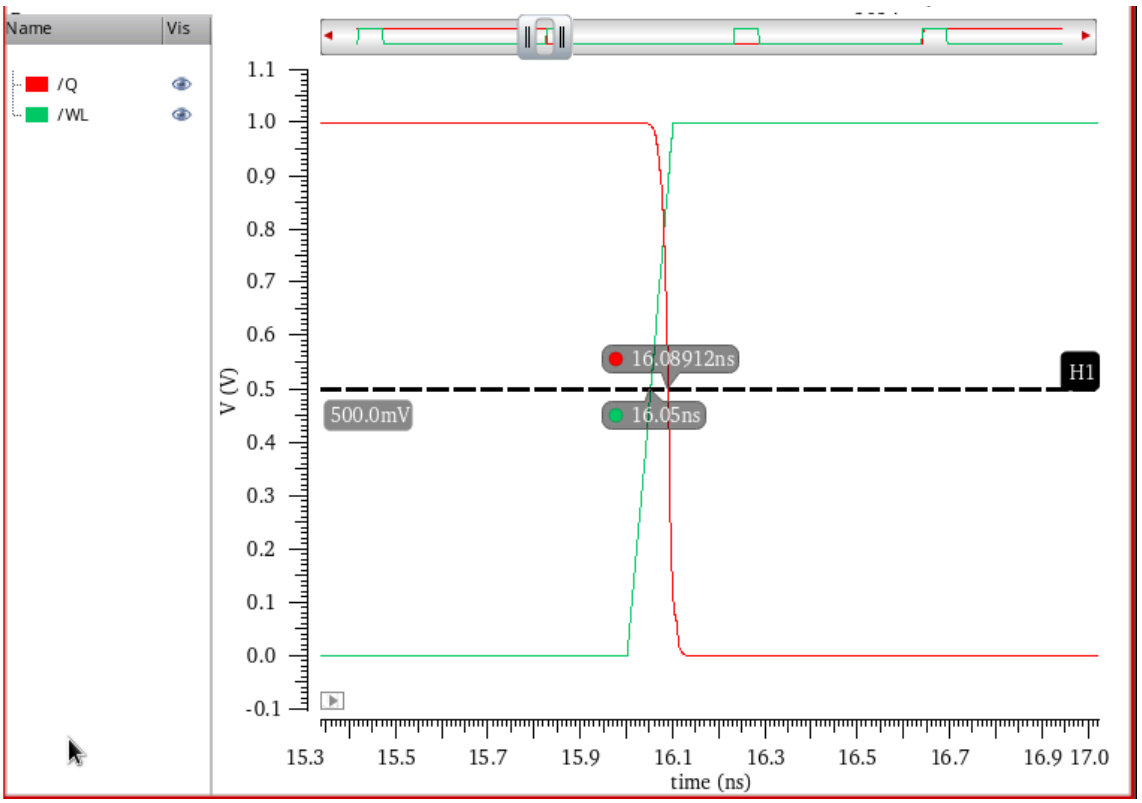


Fig. 4.5. Simulation result for write delay

According to the simulation results shown in Figure 4.5, the write delay for the Proposed 10T SRAM cell is 39.12 ps.

4.4.2 Read Delay

The interval between the read word line (RWL) reaching half of its final value and the read bitline (RBL) or read output reaching half of its final value is known as the read access delay for a read operation.

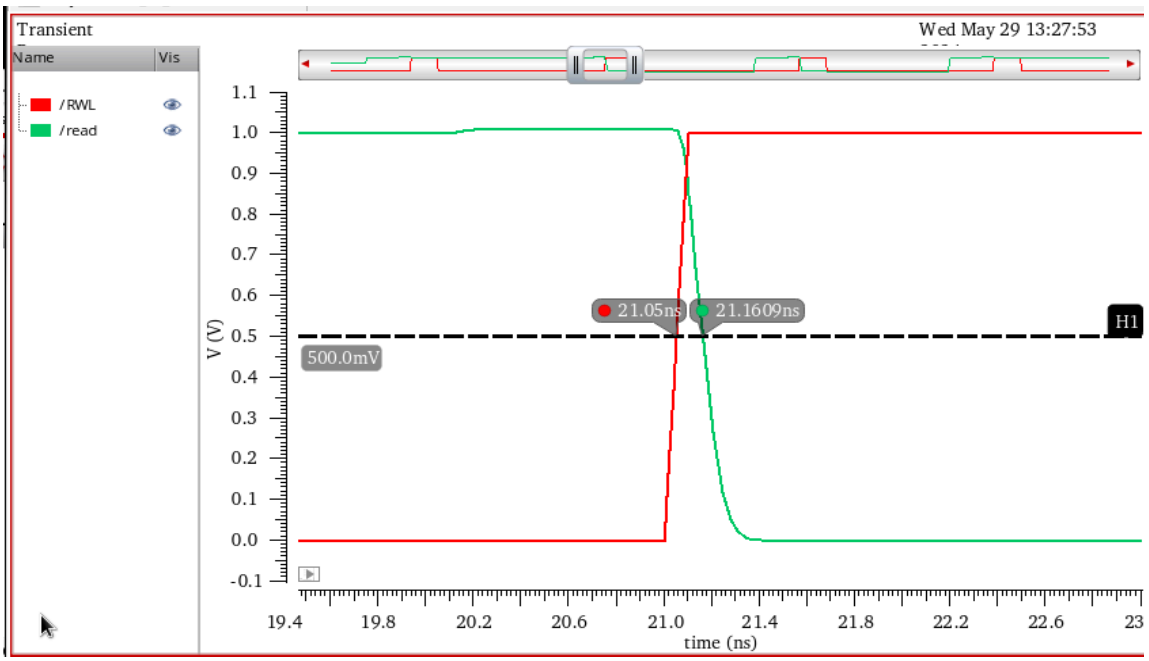


Fig. 4.6. Simulation result for read delay

According to the simulation results shown in Figure 4.6, the read delay for the Proposed 10T SRAM cell is 110.9 ps.

4.5 STATIC NOISE MARGIN

As discussed in Chapter 3, the Static Noise Margin (SNM) measures SRAM stability under noise. To find the SNM, plot the voltage transfer characteristics (VTC) for both inverters and locate their intersection points. The SNM is the length of the diagonal of the largest square that fits between the curves, representing the maximum noise the cell can withstand without changing state.

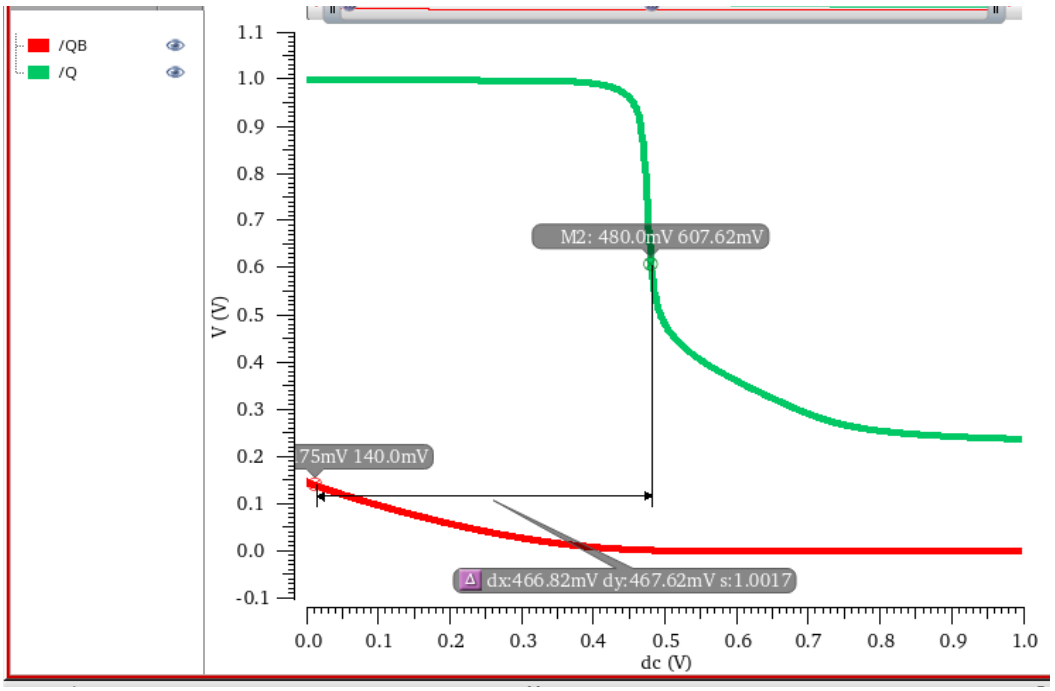


Fig 4.7. WSNM Curve for Proposed 10T

A memory cell with SRAM's stability when writing is assessed using the Write Static Noise Margin (WSNM). It shows the ease with which new data can be entered into the cell. High WSNM ensures that the cell can be consistently overwritten with new data, which is required for proper operation. According to the simulation results shown in Figure 4.7, the WSNM for the 10T SRAM is 466 mv.

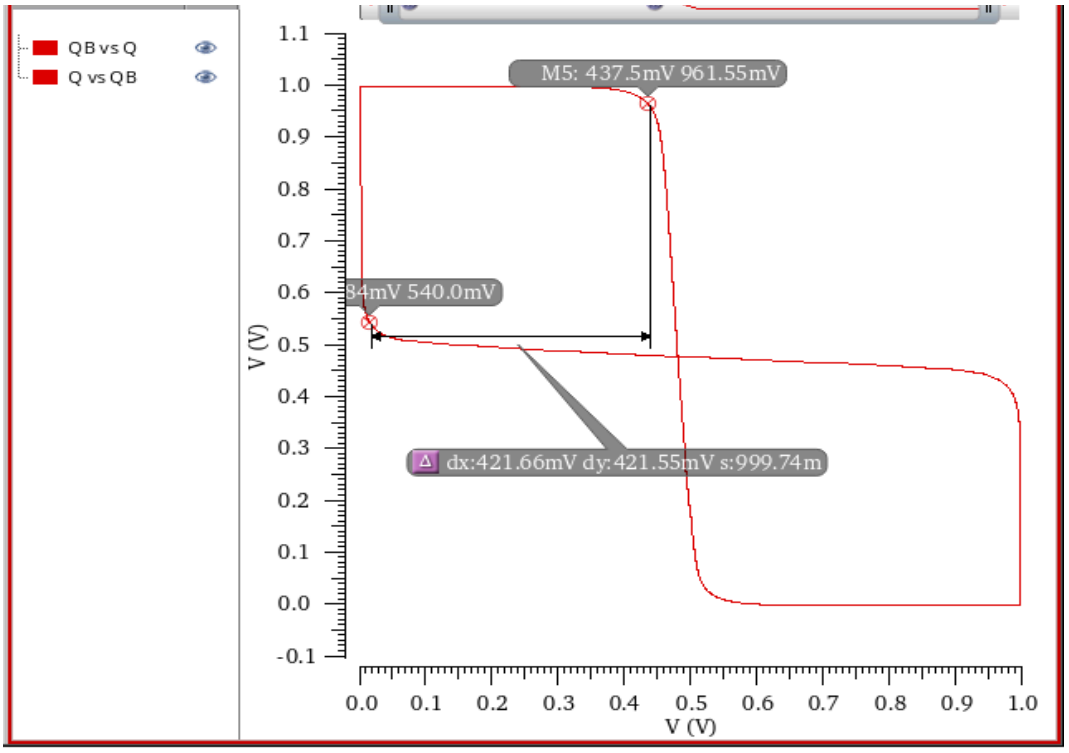


Fig 4.8. RSNM Curve for Proposed 10T

The read SNM value is the highest noise voltage that an SRAM cell can withstand without causing any changes to its recorded state during a read operation. High Read SNM is crucial for ensuring data integrity, especially in high-performance and low-power applications where noise susceptibility is higher due to reduced voltage margins and increased density of cells. According to the simulation results shown in Figure 4.8, the RSNM for the 10T SRAM is 421 mv.

CHAPTER 05

PERFORMANCE COMPARISON

This chapter focuses on the comparison between a 10T SRAM cell and a proposed 10T SRAM cell. The performance metrics such as power, access time, and static noise margin (SNM) will be analyzed to provide a comprehensive evaluation of both SRAM cell architectures. The findings from this comparison will contribute to a deeper understanding of how low power strategies can enhance the efficiency of SRAM cells, ultimately guiding future developments in low power memory design.

5.1 POWER CONSUMPTION

The integration of the ONOFIC technique into the 10T SRAM cell significantly enhances power efficiency compared to the traditional 10T SRAM design.

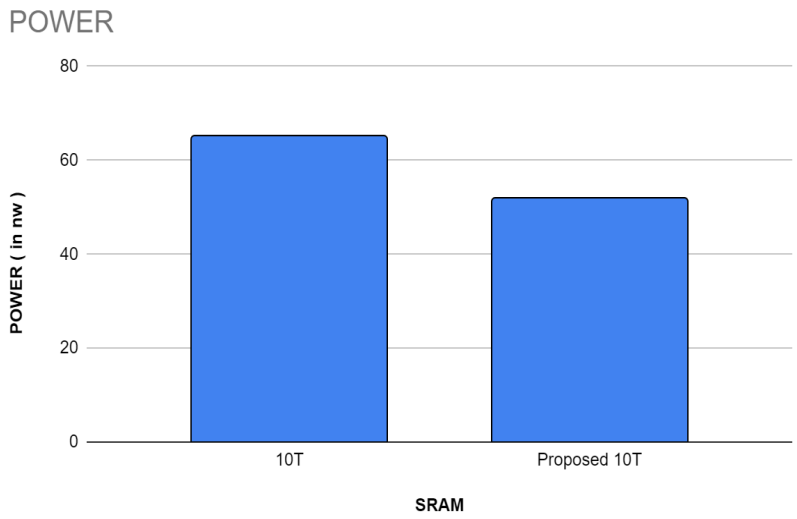


Fig 5.1. Comparison of Power

An analysis is conducted on the power consumption of both the architectures. The graphical comparison of power for both the structures are shown in Fig. 5.1. The analysis indicates that the power consumption is higher in the 10T SRAM Cell(i.e., 65.14nw) compared to the Proposed 10T SRAM Cell(i.e., 51.7nw), due to the integration of low power technique in the proposed 10T SRAM cell structure.

5.2 ACCESS DELAY

The data stored in storage nodes of a SRAM are accessed during read and write operation. Read Access Delay is by the amount of time required for the data stored at the storage nodes to be reflected in read line (RL) during a read operation. As the graph in Fig. 5.2 indicates, the read access delay of the proposed 10T SRAM cell(i.e., 110.9 ps) is less than the 10T SRAM cell(i.e., 165.6 ps).

Write Access Delay quantifies the time taken to transfer data onto the storage nodes. From the graph in Fig. 5.2, the write delay of the proposed structure (i.e., 39.12 ps) is less than the 10T SRAM cell (i.e., 39.98 ps).

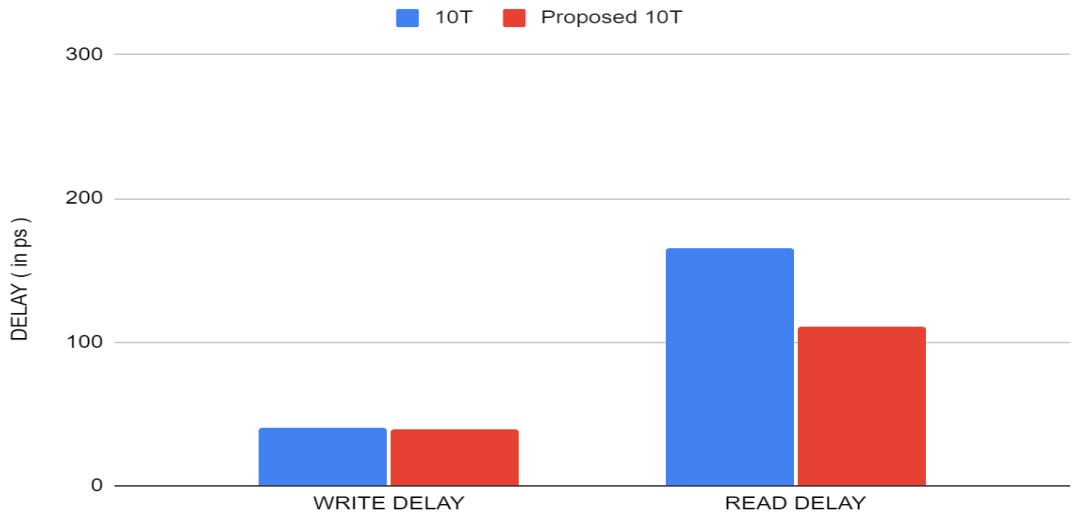


Fig 5.2. Comparison of Delay

5.3 STABILITY

Since it exemplifies the reliability inherent in every design, the stability of the cell is crucial in SRAMs. Butterfly curves are utilised to calculate the values of RSNM and WSNM.

Fig 5.3. Comparison of SNM

As indicated in the comparison in Fig. 5.3, the proposed 10T SRAM cells has better write SNM (i.e., 466mv) as compared to 10T SRAM cell (i.e., 457mv) and similar read SNM (i.e., 421mv).

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1. CONCLUSION

In this project, we explored the design and implementation of a 10T SRAM cell with an emphasis on reducing power consumption while maintaining performance. The integration of the ONOFIC technique into the 10T SRAM cell architecture demonstrated significant advancements in power efficiency compared to traditional 10T SRAM designs. The ONOFIC technique, which employs leakage control transistors, effectively increases resistance between the power supply (Vdd) and ground, thereby minimizing power consumption during idle states without impacting the dynamic performance of the cell.

Through detailed simulation and analysis, we evaluated several key performance metrics, including power consumption, read/write access delay, and static noise margin. The proposed 10T SRAM cell exhibited a lower total power consumption, with results indicating a substantial reduction compared to conventional designs. Specifically, the power consumption was measured at 51.7 nW for the proposed design versus 65.14 nW for the 10T SRAM cell, highlighting the efficiency of the ONOFIC technique.

Moreover, the proposed design also showed improvements in read and write access delays. The read access delay was reduced to 110.9 ps compared to 165.6 ps in the conventional 10T design. Similarly, the write access delay decreased from 39.98 ps to 39.12 ps, reflecting the enhanced speed performance of the proposed architecture. The static noise margin (SNM), an essential indicator of stability, showed favorable results with the proposed cell achieving better write SNM (466 mV) compared to the traditional 10T SRAM cell (457 mV), while maintaining a comparable read SNM (421 mV).

The implementation of the ONOFIC technique within the 10T SRAM cell architecture offers a promising approach for achieving low-power, high-performance memory cells. This research contributes to the field of low-power memory design by demonstrating

that power efficiency can be significantly enhanced without compromising other critical performance metrics.

6.2. FUTURE SCOPE

The future scope of this research includes several promising directions to further enhance the performance and applicability of the proposed 10T SRAM cell design. One potential area of exploration is the adaptation of this design to more advanced technology nodes, where leakage power issues become increasingly significant. Additionally, integrating the 10T SRAM cell with other low-power techniques, such as multi-threshold CMOS (MTCMOS) and dynamic voltage scaling (DVS), could yield further improvements in power efficiency. Investigating the application of the 10T SRAM cell in different types of memory architectures, including multi-port SRAMs and embedded DRAMs, would assess its versatility and performance benefits in various contexts. Another avenue for future research is the practical implementation and testing of the 10T SRAM cell in real-world applications to validate its theoretical and simulated advantages, ensuring it meets the demands of modern low-power electronic devices and systems. Finally, exploring new materials and fabrication techniques could lead to further advancements in the performance and efficiency of 10T SRAM cells, contributing to the development of next-generation memory technologies.

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