PERFORMANCE ANALYSIS OF MULTI-GATE FERROELECTRIC FET

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I, **Sagar Gosai (2K22/VLS/14)** students of MTech **(VLSI Design and Embedded Systems)**, hereby declare that the Major-1 Project report for Topic **MULTI-GATE FERROELECTRIC FET** which is submitted by us to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associate ship, Fellowship or other similar title or recognition.

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CERTIFICATE

I hereby certify that the Seminar Report for topic **MULTI-GATE FERROELECTRIC FET** which is submitted by SAGAR GOSAI (2K22/VLS/14) of Electronics and Communication Department, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ABSTRACT

This report presents an extensive analysis of Multi gate Ferroelectric Field-Effect Transistors (FETs) and their applications in high-frequency electronic devices. The report delves into the fundamental characteristics, working principles, design considerations, challenges, and potential future directions of high frequency ferroelectric FETs. It also discusses various aspects such as material selection, fabrication techniques, integration, and provides an in-depth overview of their applications in high-frequency communication systems, radar technology, and data transmission. Using simulations using the TCAD Silvaco ATLAS simulator and the ferro model, fermi, Lombardi CVT model, Shockley-Read-Hall (SRH) recombination models, a Dual Gate Accumulation Mode Without Junction It has been suggested to use a ferroelectric Field Effect Transistor (JAM-DG-FE-FET). and evaluated for RF/analog specifications. When comparing the JAM-DG-FE-FET configuration to the Junctionless Accumulation Mode Ferroelectric Field Effect Transistor (JAM-FE-FET) setup, key analog metrics such as g_m, A_v, g_d, and early voltage (V_{EA}) are obtained. Subsequently, the suggested apparatus undergoes frequency examination, and several crucial radiofrequency characteristics, such as f_T is noted about the Dual Gate Junctionless Accumulation Mode Ferroelectric Field Effect Transistor (JAM-DG-FE-FET). Therefore, when compared to Junctionless Accumulation Mode ferroelectric FETs (JAM-FE-FET), Dual Gate Junctionless Accumulation Mode ferroelectric FETs (JAM-DG-FE-FET) have been discovered to have improved analogue and RF performance. Therefore, it can be said that the JAM-DG-FE-FET device that is being shown here is a strong candidate for use in high-frequency systems.

Keywords: Junctionless accumulation mode (JAM), RF parameters, Ferroelectric, HfO_2

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PLACE: Delhi **Sagar Gosai**

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CHAPTER 01 Introduction

Ferroelectric FET (Field-Effect Transistor) is a type of transistor that utilizes ferroelectric materials for controlling the flow of electric current. It combines the principles of traditional FETs with the unique properties of ferroelectric materials, resulting in improved performance and novel functionality. Ferroelectric FETs have the potential to revolutionize electronics by enabling low-power, non-volatile memory, and advanced logic devices.

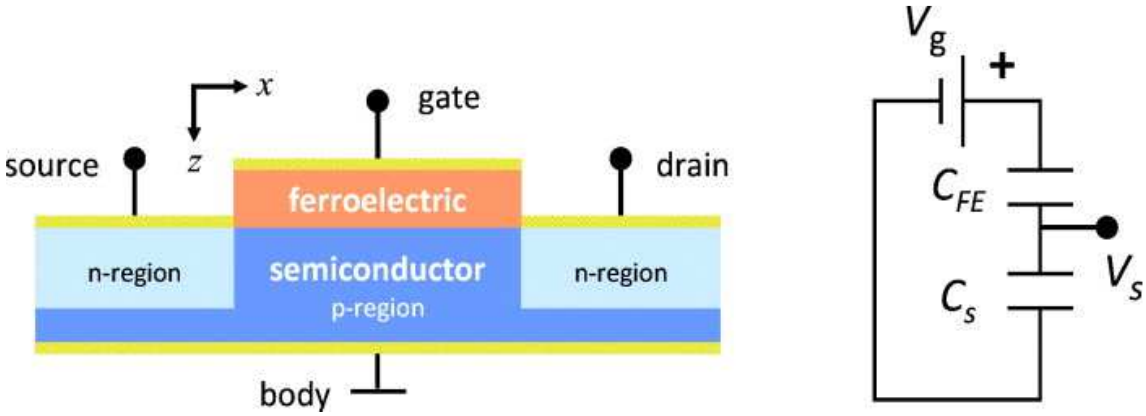

Fig 1 : Ferroelectric FET

To understand Ferroelectric FETs, let's break down the key components and concepts involved:

- **Ferroelectric Materials**: It possess spontaneous electric polarization that get reversed by application of electric field applied externally. This property is known as ferroelectricity and is crucial for the functioning of Ferroelectric FETs. Examples of ferroelectric materials include lead zirconate titanate (PZT), bismuth ferrite (BiFeO3), and others.
- **Transistor Basics**: Field-Effect Transistors (FETs) are fundamental electronic devices that controls the current flow inside semiconductor channel using electric field. Traditional FETs include Metal-Oxide-Semiconductor FETs (MOSFETs), where the channel conductivity is modulated by the gate voltage.
- **Ferroelectric FET Structure**: A Ferroelectric FET typically consists of three key components: the ferroelectric gate insulator, the semiconductor channel, and the drain-source electrodes. A ferroelectric material is sandwiched between gate electrode and the channel, allowing the polarization of the ferroelectric material to influence the channel conductivity.
- **Operation Modes**: Ferroelectric FETs can operate in different modes, utilizing the unique properties of ferroelectric materials. The most common modes are:

    - Memory Mode: In this mode, the Ferroelectric FET acts as a non-volatile memory device. Polarized state of the ferroelectric gate insulator represents the stored data, and the channel current is controlled based on this polarization state.
    - Transistor Mode: In this mode, the Ferroelectric FET functions as a traditional transistor. The gate voltage regulate the conductivity of the channel, and the device behaves as a switch or an amplifier.
- **Advantages and Applications**: Ferroelectric FETs offer several advantages over traditional FETs, including:
    - Non-Volatile Memory: The ability to retain data even when the power supply is disconnected makes Ferroelectric FETs ideal for non-volatile memory applications, such as storage in computers, mobile devices, and embedded systems.
    - Low Power Consumption: Ferroelectric FETs can operate at lower voltages, resulting in lower power consumption compared to usual memory technologies.
    - High Speed: The polarization switching speed of ferroelectric materials is typically faster than traditional memory technologies, enabling high-speed read and write operations.
    - Integration Potential: Ferroelectric FETs is integrable with existing CMOS technology, facilitating their adoption in large-scale integrated circuits (ICs).

Potential applications of Ferroelectric FETs include memory devices, neuromorphic computing, low-power logic circuits, and radio-frequency (RF) communication systems. In summary, Ferroelectric FETs leverage the unique properties of ferroelectric materials to create high-performance, low-power, and non-volatile electronic devices. With ongoing research and development, Ferroelectric FETs hold promise for advancing various fields of electronics and shaping the future of computing technology.

CHAPTER 02 Review of Literature

Over the past few decades, a variety of MOSFET structures have been realized, and their scaling down to the nanoscale has been extremely effective, leading to a significant boost in performance. Nevertheless, as these transistors get smaller, the connections get closer, which makes it challenging to achieve the significant doping concentration gradients needed. J. E. Lilienfeld developed the idea of junctionless transistors in the 1920s to address this issue [2]. Numerous analytical studies have also been conducted on the surface potential of junctionless transistors. Additionally, we know that microwave frequency applications can benefit from the superior switching performance of cylindrical surrounding gate MOSFETs [3-4]. However, there are several drawbacks to the junctionless transistor, including reduced mobilities brought on by high doping levels. Moreover, the greater gate work function for a fully depleted channel area, which ensures the device turns, is one of the significant barriers in the device. The JAM FET, a newly modified structure with highly doped Source/Drain regions and less doping in channel that leads to less mobility degradation [5]. Heavy power consumption and dissipation of heat, which both slow down data processing rate, are another significant problem brought on by reducing and increasing the density of transistors on a device. By overcoming "Boltzmann's Tyranny," a lower working voltage constraint, this may be improved, and the transistor operating voltage can be lowered, resulting in a reduction in power consumption. Ferroelectric field effect transistors (FE-FETs) are one such promising gadget. However, hysteretic behaviour in memory applications was the focus of most research. Due to its CMOS compatibility, the ferroelectric characteristics of hafnium oxide (HfO_2) that were discovered in 2011 have attracted a lot of interest [6-7]. Large coercive field and higher residual polarization at low thickness, as well as better performance characteristics, have been shown in ferroelectric HfO_2 [8]. Zirconium-doped HfO_2 (HZO) has emerged as a promising material because of its adjustable ferroelectric characteristics and decreased annealing temperature. Ferroelectric hafnium oxide is only a material system that, in addition to realizing memory, may be used to realise the 2008-proposed Negative Capacitance Field Effect Transistor (NCFET), a novel type of steep slope device [9]. Because it can generate a subthreshold swing of 60 mV/decade, negative capacitance FET has been researched empirically and theoretically for digital applications. The documented literature contains a few examples and analyses of NCFET's digital and DC behaviour, but its

high frequency (RF) capabilities have not yet been thoroughly investigated. Such a study is essential for future RF applications of NCFET. A little improvement in f_T was seen in the experiment and worthwhile circuit-level features were found in the simulations [1]. On the other hand, information about JAM-FE-FET's RF performance has been released [1]. The relationship between ferroelectric thickness (t_{FE}) and channel thickness (t_{ch}) and quantum confinement is also explored. This research incorporates the benefits of JAM-DG-FE-FET over JAM-FE-FET. The device simulation techniques are covered in detail in the section that follows the introduction. Section 3 looks at the performance metrics of the recommended device. The final portion includes conclusions.

CHAPTER 03 Ferroelectric Materials and their Properties

3.1 Introduction to Ferroelectric Materials

Ferroelectric materials are a unique materials that exhibit a spontaneous electric polarization that can be reversed by an external electric field. This property sets them apart from other dielectric materials, which do not possess such reversibility. The term "ferroelectric" is derived from the Latin word "ferrum" (iron) and "electric," emphasizing their similarities to ferromagnetic materials and their ability to exhibit electric polarization.

Ferroelectric materials have a crystal structure that allows for the existence of spontaneous dipoles. The displacement of positive and negative charges within the material creates dipoles, leading to the generation of a macroscopic electric polarization. Unlike ordinary dielectrics, which have randomly oriented dipoles, ferroelectric materials exhibit a preferred orientation of their dipoles known as spontaneous polarization.

3.2 Ferroelectric Properties

- **Spontaneous Polarization**: Ferroelectric materials electric polarization is permanent, even if external electric field is absent polarization remains. This polarization arises due to the alignment of electric dipoles within the crystal lattice.
- **Reversibility**: One of the most distinctive features of ferroelectric materials is the ability to switch their polarization direction according to an applied electric field. This property makes them valuable for various technological applications.
- **Hysteresis Behavior**: Ferroelectric materials exhibit a hysteresis loop in their electric polarization-electric field characteristics. The hysteresis loop shows the dependence of the polarization on the magnitude and direction of the applied electric field.
- **Piezoelectric Effect**: These materials possess the piezoelectric effect, meaning that they convert mechanical stress or strain into an electric voltage and vice versa. This property finds applications in sensors, actuators, and energy harvesting devices.
- **Curie Temperature**: Ferroelectricity is temperature-dependent, and each ferroelectric material has a specific Curie temperature (Tc) above which its

ferroelectric properties disappear. Below the Curie temperature, the material exhibits ferroelectric behavior.

- **Dielectric Constant**: Ferroelectric materials typically have high dielectric constants, making them useful for energy storage applications such as capacitors.

3.3 Ferroelectric materials for high frequency FET'S

Ferroelectric materials plays a crucial role in the development of High Frequency Ferroelectric Field-Effect Transistors (FETs). The choice of ferroelectric material significantly impacts the performance and operational characteristics of these devices. This section will discuss some commonly used ferroelectric materials for high-frequency FETs and their properties.

- Lead Zirconate Titanate (PZT): Lead Zirconate Titanate, commonly known as PZT, is one of the most used and widely studied ferroelectric materials for high-frequency FETs. It is a solid solution of lead titanate (PbTiO3) and lead zirconate (PbZrO3). PZT offers high piezoelectric coefficients, excellent ferroelectric properties, and a Curie temperature in the range of 200-400°C, depending on its composition. PZT-based FETs have demonstrated good high-frequency performance and have been employed in various applications, including wireless communication systems and radar technology.
- Barium Strontium Titanate (BST): Another popular ferroelectric material used for high-frequency FETs. It is a perovskite oxide with the general formula Ba1-xSrxTiO3. BST exhibits a tunable dielectric constant, allowing for the adjustment of its electrical properties. This tunability makes it suitable for frequency-agile devices and enables the realization of low-loss microwave components. BST-based FETs have shown promising results for high-frequency applications due to their wide tunability and low loss characteristics.
- Lithium Niobate (LiNbO3): Lithium Niobate, denoted as LiNbO3, is a ferroelectric material with excellent electro-optic and piezoelectric properties. While LiNbO3 is primarily known for its use in the field of optics, it has also found applications in high-frequency FETs. LiNbO3-based FETs exhibit high speed, low power consumption, and good linearity, making them suitable for microwave and millimeter-wave frequency applications. Additionally, the

electro-optic properties of LiNbO3 enable the integration of optical functionalities with high-frequency electronic devices.

- Bismuth Ferrite (BiFeO3): Bismuth Ferrite, represented by the chemical formula BiFeO3, is a multiferroic material that exhibits both ferroelectric and antiferromagnetic properties. BiFeO3 offers several advantages, such as high Curie temperature (~830°C), good piezoelectric response, and low leakage currents. These properties make it an attractive candidate for high-frequency FETs. BiFeO3-based FETs have shown potential for applications requiring high-frequency switching and memory functionalities.
- Lead Magnesium Niobate-Lead Titanate (PMN-PT): It is a relaxor ferroelectric material. It possesses a high dielectric constant, large electromechanical coupling coefficient, and excellent piezoelectric properties. PMN-PT-based FETs have been investigated for their potential use in high-frequency devices, such as filters and resonators, due to their wide bandwidth and low insertion loss characteristics.

These are just a few examples of ferroelectric materials utilized in high-frequency FETs. The selection of the appropriate ferroelectric material depends on specific application requirements, including frequency range, desired performance, temperature stability, and integration compatibility. Ongoing research and development efforts aim to explore new ferroelectric materials and optimize their properties to enhance the performance of high-frequency FET

CHAPTER 04 Field-Effect Transistors: A Brief Overview

4.1 Basic Principles of Field-Effect Transistors

Field-Effect Transistors (FETs) are electronic devices that controls flow of charge carriers through a semiconductor channel using an electric field generated by a gate electrode. FETs have three terminals: source, drain, and gate. The semiconductor channel is formed between the source and drain, and gate is insulated from the channel by a dielectric layer. MOSFETs are the most widely used and are further categorized into n-channel (NMOS) and p-channel (PMOS) types.

The operation of FETs relies on the gate-source voltage (VGS) applied across the gate and source terminals. By applying a voltage at gate, an electric field is introduced in the channel, influencing the flow of charge carriers. In NMOS FETs, which have an n-type channel, a positive VGS attracts electrons from the source, forming a path between source and drain. Conversely, in PMOS FETs with a p-type channel, a negative VGS attracts holes, creating a conductive path.

FETs operate in different modes based on the relationship between VGS and the drain-source voltage (VDS). In the cut-off mode, with VGS below the threshold voltage (VTH), no significant current flows through the channel. In the triode (or linear) mode, VGS exceeds VTH, and the FET operates as an amplifier, with the drain current (ID) proportional to VDS. In the saturation mode, VGS is sufficiently high, resulting in a constant ID despite variations in VDS, making the FET suitable for switching applications.

The threshold voltage (VTH) is the minimum gate voltage (VGS) required to initiate significant current flow. It determines the turn-on behavior of the FET. Transconductance (gm) quantifies the relationship between the change in ID and the change in VGS, representing the FET's amplification capability.

Biasing is crucial for proper FET operation as an amplifier, involving the application of appropriate voltages to establish the desired operating point. FETs possess high input impedance, low output impedance, low power consumption, and wide frequency response, making them versatile for various applications like digital logic circuits, amplifiers, oscillators, and voltage-controlled switches.

In conclusion, Field-Effect Transistors utilize the control of an electric field through gate terminal to control the flow of charge carriers through a channel. Understanding

the principles of FET operation is fundamental to harnessing their amplification and switching capabilities in electronic circuits and systems.

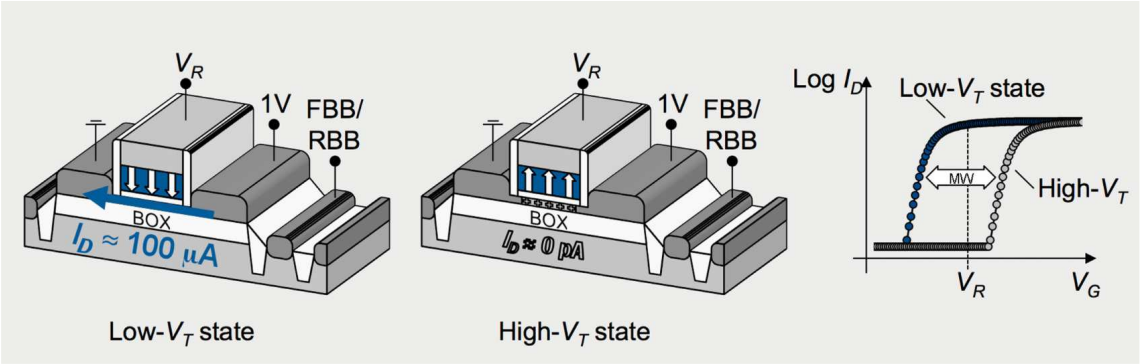

Fig 2 : Ferroelectric Fet at low and high threshold

4.2 Traditional FETs vs. Ferroelectric FETs

Table01: Comparison of FET and Ferroelectric FET

	Traditional FETs	**Ferroelectric FETs (FeFETs)**
Operation Principle	Control of current via voltage	Control of current via polarization
Gate Insulator	Oxide (typically SiO2)	Ferroelectric material
Switching Behavior	Controlled by voltage	Controlled by polarization
Non-Volatility	Volatile	Non-volatile
Memory Operation	Not applicable	Suitable for memory devices
Hysteresis	No hysteresis behavior	Hysteresis behavior
Read/Write Speed	Fast	Generally slower
Endurance	No endurance limitations	Limited endurance

Power Consumption	Low	Generally higher
Integration	Compatible with CMOS	Compatibility being explored
Applications	Logic circuits, amplifiers,	Non-volatile memories,
	switches, processors	neuromorphic computing, etc.

CHAPTER 05 Working Principles of High Frequency feFET

5.1 Polarization Switching and Channel Conductivity Control

The working principle of high-frequency Ferroelectric Field-Effect Transistors (FETs) involves the polarization switching of the stacked ferroelectric gate and its influence on the conductivity of the semiconductor channel. In Ferroelectric materials there is spontaneous polarization, which can be electrically switched between two stable states. This switching can be achieved by applying an electric field externally or by using the inherent properties of the material.

In a Ferroelectric FET, the ferroelectric gate insulator is between the gate electrode and the channel. The polarization of the stacked ferroelectric material can be controlled by applying a voltage to the gate electrode. When the ferroelectric material is polarized in one direction, it induces a specific charge distribution at the interface with the semiconductor channel, affecting the conductivity of the channel. By switching the polarization, the charge distribution at the interface changes, leading to a modification of the channel conductivity.

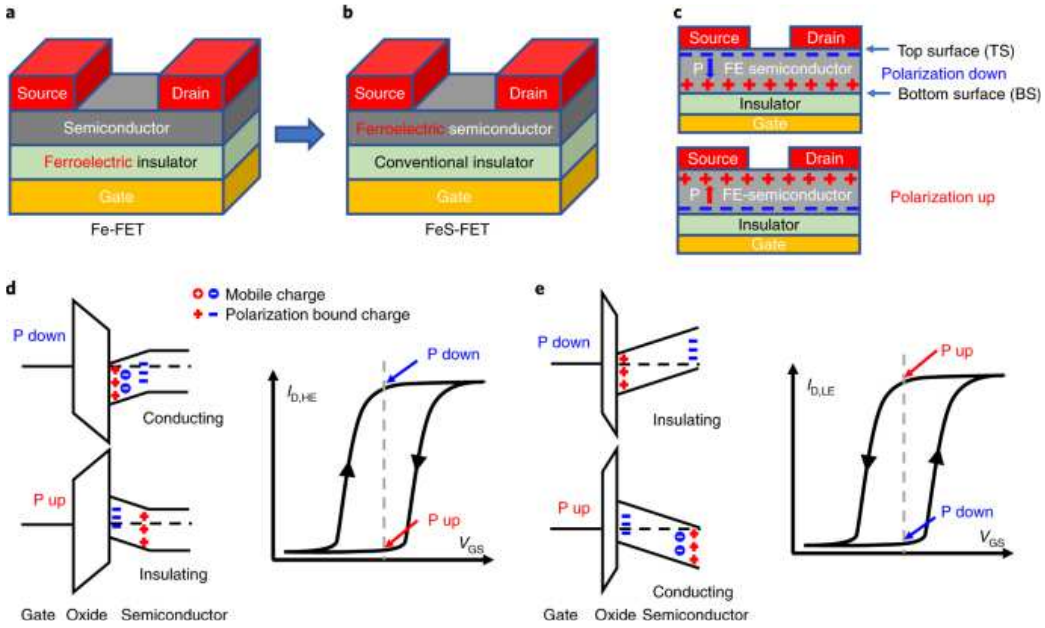

Fig 3 : Working of Ferroelectric FET

The polarization switching in the ferroelectric gate insulator is typically achieved by applying a voltage above a specific switching threshold. This voltage can be either a negative or positive bias, depending on material and device design. The switching can

be reversible or irreversible, depending on the ferroelectric material and operating conditions.

By controlling the polarization state of the ferroelectric gate insulator, the conductivity of the semiconductor channel can be modulated. This allows for the control of current flow through the channel, enabling the operation of the FET as a switch or an amplifier. The high-speed switching capability of ferroelectric materials makes them suitable for high-frequency applications.

5.2 Gate Voltage and Ferroelectric Gate Insulator

In a high-frequency Ferroelectric FET, the gate voltage plays a crucial role in determining the state of the stacked ferroelectric gate insulator and, consequently, the conductivity of the semiconductor channel. The gate voltage is applied on gate electrode, which is in contact with the ferroelectric material.

When a positive gate voltage is applied, it can induce a specific polarization state in the ferroelectric material, resulting in a particular charge distribution at the interface with the semiconductor channel. This charge distribution influences the conductivity of the channel. Similarly, a negative gate voltage can induce an opposite polarization state and a different charge distribution, leading to a different conductivity state of the channel.

The gate voltage magnitude required to switch the polarization of the ferroelectric material and control the conductivity of the channel depends on the specific characteristics of the ferroelectric material used, such as coercive field and remnant polarization. Device design parameters, including the thickness of the ferroelectric layer and the electrode configuration, also impact the required gate voltage.

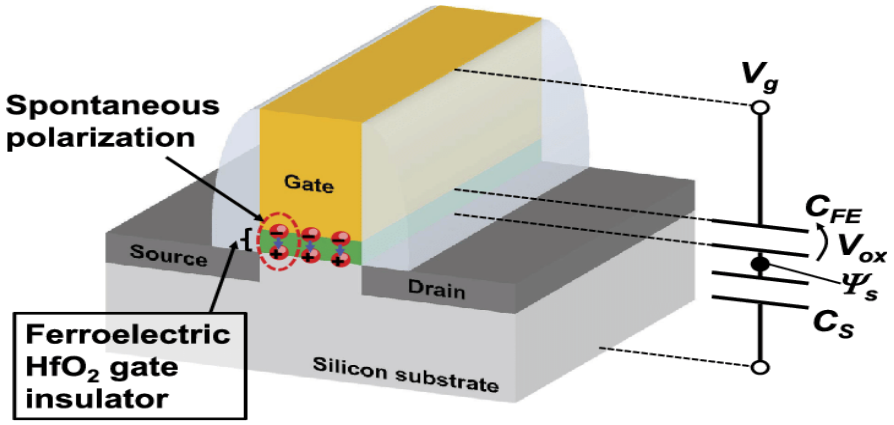

Fig4 : Gate Voltage and Ferroelectric Gate Insulator

5.3 Semiconductor Channel Operation

The semiconductor channel in a high-frequency Ferroelectric FET acts as current-carrying path between the source and the drain. The conductivity of the channel can be changed by the polarization state of the ferroelectric gate insulator, which depends on gate voltage applied.

When the ferroelectric gate insulator is polarized in a specific direction, it induces a charge distribution at the interface with the channel. This charge distribution alters the concentration and mobility of carriers (electrons or holes) inside the channel, affecting its conductivity. The channel can transition between high and low conductivity states based on the state of polarization of ferroelectric gate insulator.

Conductivity modulation of semiconductor channel enables the high-frequency operation of Ferroelectric FETs. The rapid switching of the ferroelectric gate insulator allows for fast control of the channel conductivity, enabling high-speed switching and amplification of electrical signals.

Overall, the working principles of high-frequency Ferroelectric FETs involve the control of polarization switching in the ferroelectric.

CHAPTER 06 Advantages, Limitations and Applications

6.1 Advantages of High-Frequency Ferroelectric FETs

1. High-Speed Operation: Ferroelectric FETs offer rapid switching capabilities due to the fast polarization switching of the ferroelectric gate insulator. This makes them suitable for high-frequency applications where quick response times are crucial.
2. Non-Volatility: Ferroelectric materials can retain their polarization state even when the power supply is removed. This non-volatile characteristic enables the development of non-volatile memory devices based on Ferroelectric FETs, offering persistent data storage even in the absence of power.
3. Low Power Consumption: Ferroelectric FETs can operate at lower power levels compared to traditional CMOS-based technologies. The non-volatile nature of ferroelectric materials eliminates the need for continuous power supply to maintain the device state, resulting in energy-efficient operation.
4. High On/Off Ratio: Ferroelectric FETs can achieve a high on/off ratio, meaning they can effectively switch between conducting and non-conducting states. This leads to improved signal integrity and reduced leakage current when the device is in the off state.
5. Compatibility with CMOS Technology: Ferroelectric FETs are integrable with existing complementary metal-oxide-semiconductor (CMOS) processes, allowing compatibility with conventional fabrication techniques and enabling the incorporation of ferroelectric FETs into existing semiconductor technologies.

6.2 Limitations of High-Frequency Ferroelectric FETs

1. Limited Endurance: Ferroelectric materials can experience degradation over time due to repeated polarization switching, leading to a limited endurance compared to traditional FETs. The number of reliable switching cycles is a critical factor that needs to be addressed for long-term device reliability.
2. Hysteresis: Ferroelectric FETs exhibit hysteresis behavior in their electrical characteristics, which can introduce non-linearities in device operation. This hysteresis can affect device performance and may require additional circuit design considerations to compensate for its effects.

3. Lower Mobility: Some ferroelectric materials may have lower charge carrier mobility compared to traditional semiconductors, which can impact the overall speed and performance of Ferroelectric FETs. Improving the mobility of ferroelectric materials is an ongoing research challenge.

6.3Applications of High-Frequency Ferroelectric FETs

1. Non-Volatile Memory: The non-volatile nature of Ferroelectric FETs makes it suitable for memory applications. FeFETs can be used in non-volatile memory devices such as FeRAM (Ferroelectric Random Access Memory), which offers high-speed read/write operations and non-volatility.
2. Neuromorphic Computing: Ferroelectric FETs have shown potential in neuromorphic computing applications, where they can mimic the synaptic behavior of biological neurons. The non-volatile memory capability of FeFETs is particularly advantageous for implementing artificial neural networks.
3. Radio Frequency (RF) Applications: Ferroelectric FETs can be utilized in high-frequency RF switches and amplifiers due to their fast switching speeds. They offer improved linearity and lower power consumption compared to traditional RF devices.
4. High-Speed Digital Logic: Ferroelectric FETs can be employed in high-speed digital logic circuits, such as clock generators and frequency dividers, to take advantage of their rapid switching capabilities.
5. Sensor Interfaces: The non-volatile nature and low-power operation of FeFETs make them suitable for sensor interfaces, where persistent data storage, low power consumption, and fast response times are desirable.

CHAPTER 7 Structure, Graphs and Discussions

7.1 Structure of JAM-FE-FET

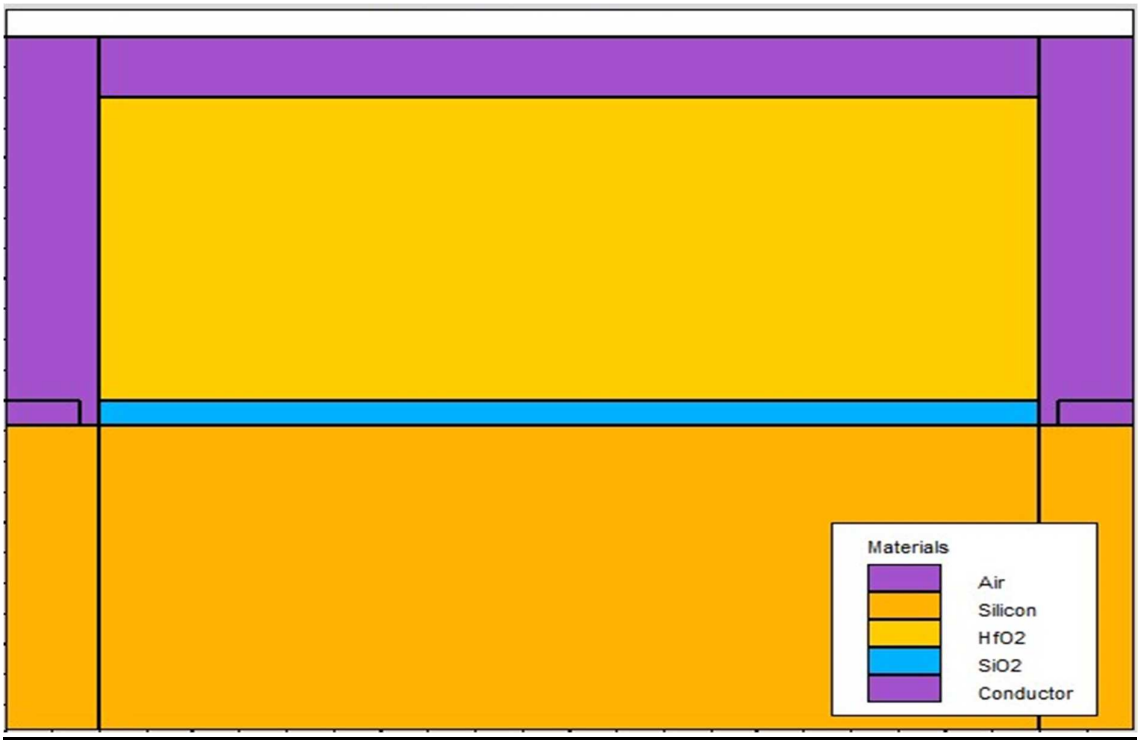

Fig5 : Structure of JAM-FE-FET after simulation

7.2 Structure of JAM-DG-FE-FET

In the simulations, the suggested structure with a stacking of gate $TiN/HfO_2/SiO_2$ is used. The channel length (L) is between 10 and 110 nm. In the gate stack, a insulator layer thickness of 0.8 nm. In JAM-DG-FE-FET, the drain and source regions have substantial doping of 1e19 cm^{-3} n-type dopants, while the channel made of silicon has 1e17 cm^{-3} of n-type dopants doped in it. It is believed that the doping level is consistent throughout the simulation. As a gate material, titanium nitride (TiN) with a work function (φ_m) of 4.85 eV is utilized. Afterwards, numerical methods like Newton and Gummel have been considered to enhance convergence.

Fig6 : Structure of JAM-DG-FE-FET

7.3 Drain current vs Gate voltage

To achieve the transfer characteristics, the gate to source voltage (V_{gs}) was changed from 0 to 1 V, and the drain to source voltage (V_{ds}) was set at 50 mV as depicted in *Fig.7.* The I_d-V_{gs} curves of both JAM-DG-FE-FET and JAM-FE-FET is depicted in *Fig. 7.* We can clearly see the JAM-DG-FE-FET has better drain current than JAM-FE-FET at constant drain voltage of 50 mV, due to gate control on channel from both top and bottom.

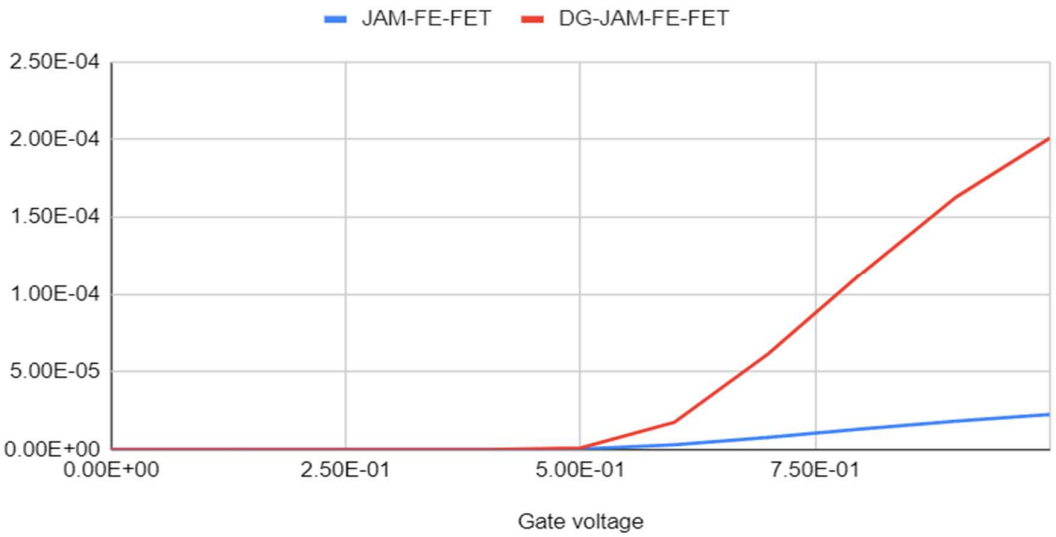

Fig. 7: Drain current vs Gate voltage

7.4 g_m vs Gate voltage

The link between variation of drain current and V_{gs} at constant V_{ds} is measured as g_m. The I_d-V_{gs} curve derivative is used to determine g_m at constant drain voltage of 50mV, as shown in *Fig. 8*. When compared to JAM-FE-FET, JAM-DG-FE-FET has the higher g_m value because control over the channel of gate is improved.

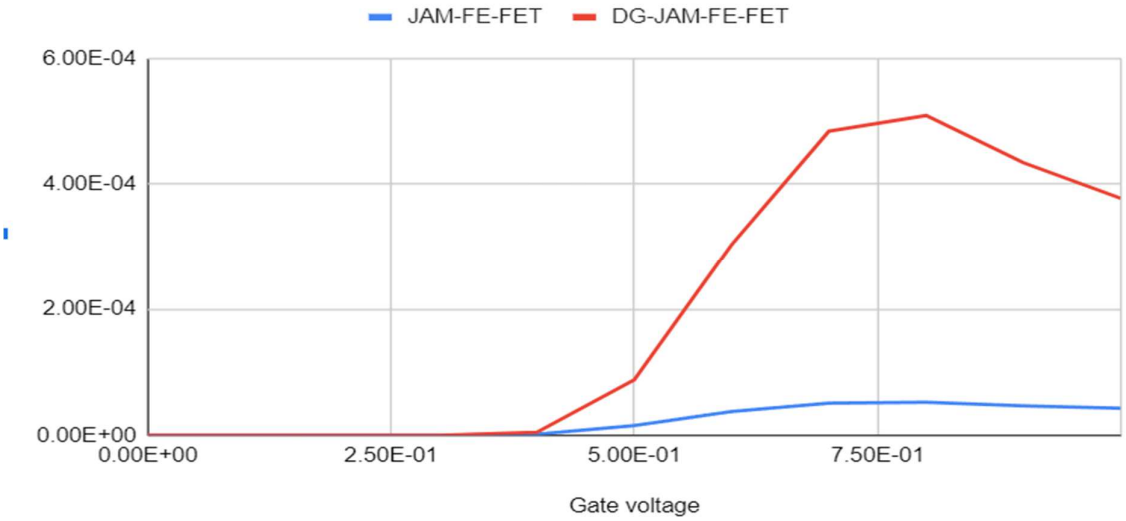

Fig. 8: g_m *vs Gate current*

7.5 Drain current vs Drain voltage

Fig. 9 shows the drain current of fluctuation with drain voltage for V_{gs}=1 V, JAM-DG-FE-FET is higher than JAM-FE-FET. This is because the two gates allow for better control over channel. The dual-gate structure provides enhanced control over the channel reducing short channel effects and improving subthreshold slope, threshold voltage control and over scalability.

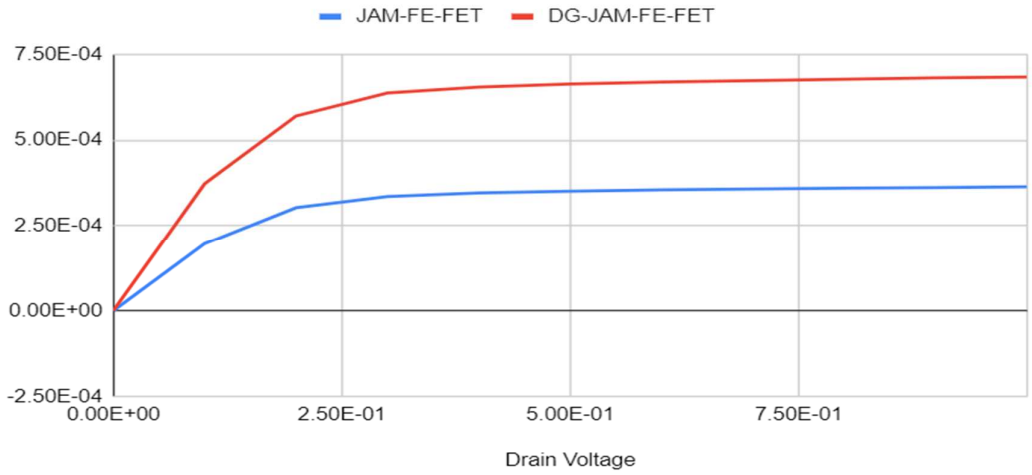

Fig. 9: Drain current vs Drain voltage

7.6 g_d vs Drain voltage

The g_d variation for the device structures under comparison is shown in *Fig. 10* By adjusting the drain current in relation to the drain to source voltage while keeping the gate to source voltage constant at 1V, the g_d can be computed.

It is represented by the formula below:

$$g_d = \frac{\partial I_d}{\partial V_{ds}} \tag{1}$$

It is evident from graphic that output transconductance g_d is more in linear zone and stays constant in saturation region. As a result, suggested gadget has a higher driving capability than the one being compared. The g_d rises because of the greater gate controllability and suppressed short channel effects.

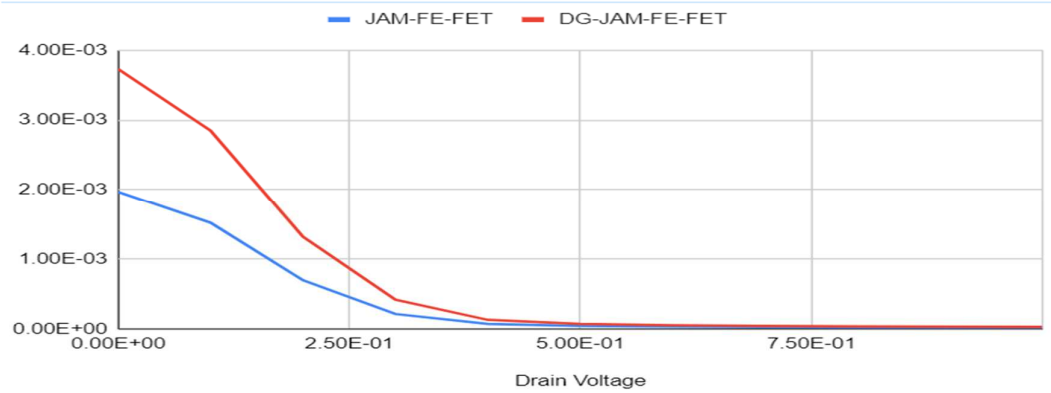

Fig. 10: g_d *vs Drain voltage*

7.7 V_{EA} vs Gate voltage

Compared to JAM-FE-FET, the JAM-DG-FE-FET has a larger Early voltage (V_{EA}) due to the rise in drain current (I_d), being greater than the drop in g_m as shown in *Fig. 11*.

$$V_{EA} = \frac{I_d}{g_d} \tag{2}$$

A higher gain and potential use in amplifiers are indicated by a bigger V_{EA}.

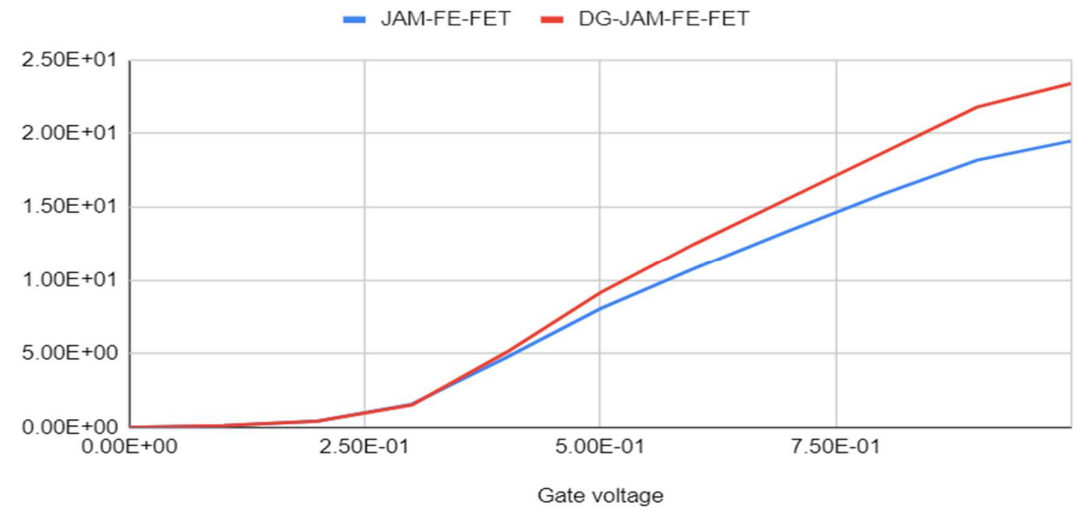

Fig.11: V_{EA} vs Gate voltage

7.8 A_V vs Gate voltage

The intrinsic DC gain, or g_m/g_d, is the next figure *Fig. 12* of merit and is defined as the ratio of g_m to g_d.

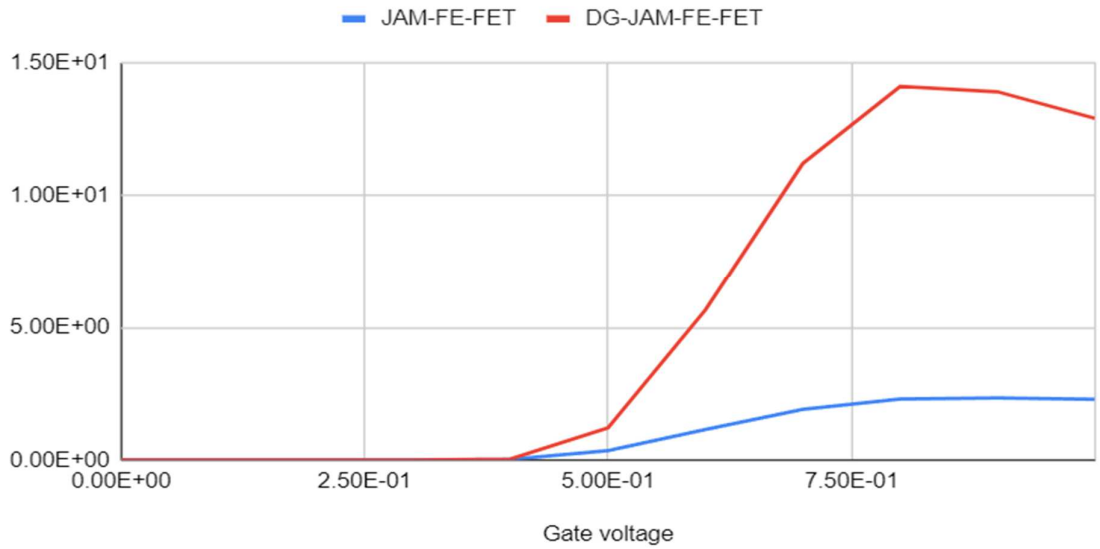

Fig. 12: A_v *vs gate voltage*

7.9 Total Capacitance vs Gate voltage

The functioning of a gadget at high frequency is governed by capacitive behaviour of the device. The relationship between total gate capacitance (C_{gg}) and gate bias (V_{gs}) in JAM-DG-FE-FET and JAM-FE-FET is depicted in the *Fig. 13*.

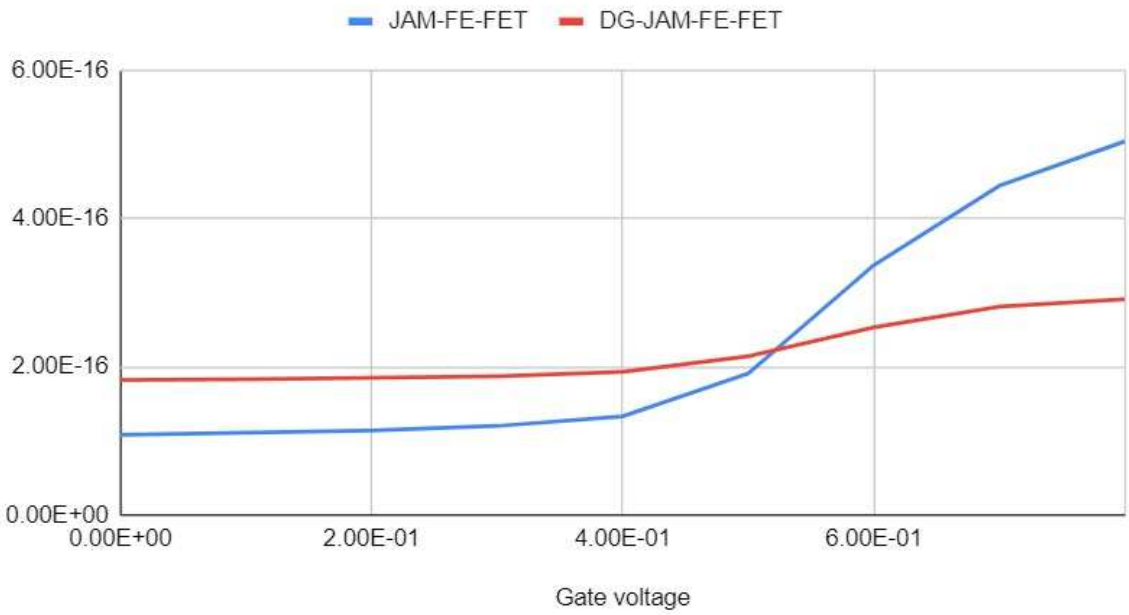

Fig. 13: Total gate capacitance (C_{gg}) vs Gate voltage

7.10 f_T vs Gate voltage

The cut of frequency (f_T), a property which is intrinsic of a device, is a benefit for device operating at high frequency . It is expressed below:

$$f_T = g_m/2\pi C_{gg} \quad (3)$$

From *Fig. 14* we see, the cut of frequency of JAM-DG-FE-FET is much higher than JAM-FE-FET.

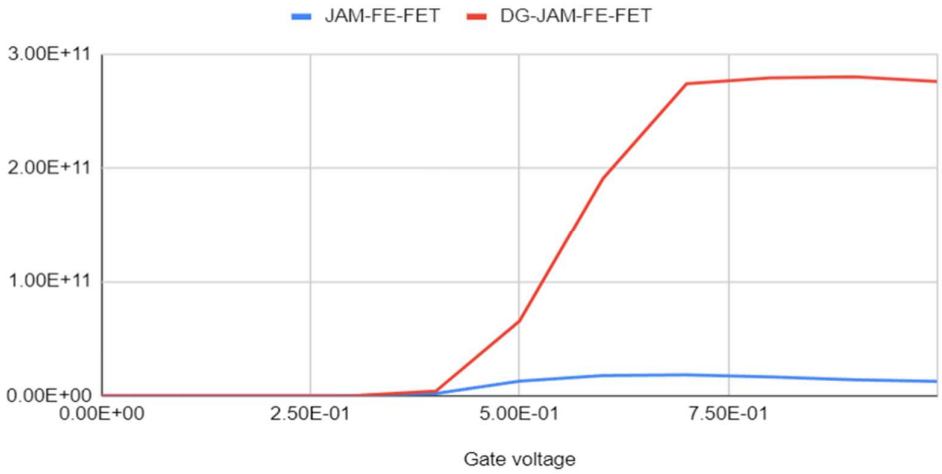

Fig. 14: Cut-off frequency(f_T) vs Gate voltage

CHAPTER 8 Conclusion

The study conducted a simulation-based evaluation to compare the performance of Junctionless Accumulation-Mode Field-Effect Transistor (JAM-FE-FET) with a newly proposed variant, the Junctionless Accumulation-Mode Double-Gate Field-Effect Transistor (JAM-DG-FE-FET). The analysis utilized the SILVACO ATLAS 3D simulator to assess the radiofrequency and analog characteristics of these devices.

The findings indicate that the JAM-DG-FE-FET outperforms the JAM-FE-FET in several key performance metrics. One of the most significant advantages of the proposed JAM-DG-FE-FET is its superior transconductance (gm). This higher gm is directly correlated with an increased cut-off frequency (fT), which is crucial for applications in the radiofrequency domain. The enhanced gm leads to better amplification capabilities and faster switching times, making the JAM-DG-FE-FET a more efficient option for high-frequency operations.

Radiofrequency characteristics, such as the unity-gain cut-off frequency, are markedly improved in the JAM-DG-FE-FET compared to the JAM-FE-FET. These improvements are indicative of the potential for the proposed device to achieve higher performance in high-frequency systems. The JAM-DG-FE-FET's design allows for more effective gate control, which is instrumental in achieving the observed performance gains.

In conclusion, the JAM-DG-FE-FET demonstrates a clear advantage over the JAM-FE-FET in terms of radiofrequency and analog performance. The simulation results strongly suggest that the proposed JAM-DG-FE-FET is a viable and superior alternative for high-frequency applications. Its enhanced transconductance and improved radiofrequency characteristics position it as a promising candidate for future electronic systems that demand high-speed and high-frequency capabilities.

References

1. Yadav S, Rewari S, Pandey R, Silicon (2022) 14:7245–7255 Junctionless Accumulation Mode Ferroelectric FET (JAM-FE-FET) for High Frequency Digital and Analog Applications. Available: https://doi.org/10.1007/s12633-021-01537-y
2. Lilienfeld JE (1926) Method and apparatus for controlling elec- tric currents. Patent
3. Gupta N, Kumar P, "Elicitation of scattering parameters of dual- halo dual-dielectric triple-material surrounding gate (DH-DD- TM-SG) MOSFET for microwave frequency applications," *Adv. Electr. Electron. Eng.*, vol. 19, no. 1, pp. 66–73, 2021, doi: https://doi.org/10.15598/aeee.v19i1.3788
4. Kumar P, Vashisht M, Gupta N, Gupta R (2021) Subthreshold current modeling of stacked dielectric triple material cylindri- cal gate all around (SD-TM-CGAA) Junctionless MOSFET for low power applications. Silicon. https://doi.org/10.1007/ s12633-021-01399-4
5. Borkar S (1999) Design challenges of technology scaling. IEEE Micro 19(4):23–29
6. Yurchuk E et al (2016) A 28nm HKMG super low power embed- ded NVM technology based on ferroelectric FETs. IEEE Trans. Electron Devices 63(9):3501–3507. https://doi.org/10.1109/TED. 2016.2588439
7. Mikolajick T *et al.*, "Next Generation Ferroelectric Memories enabled by Hafnium Oxide," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, vol. 2019-Decem, pp. 354–357, 2019, doi: https://doi.org/10.1109/IEDM19573.2019.8993447
8. Kim JY, Choi MJ, Jang HW (2021) Ferroelectric field effect tran- sistors: Progress and perspective. *APL Mater* 9(2). https://doi.org/10.1063/5.0035515
9. Appleby DJR *et al.*, "Experimental Observation of Negative Capacitance in Ferroelectrics at Room Temperature," *Nano Lett.*, vol. 14, no. 7, 2014, doi: https://doi.org/10.1021/nl5017255

Appendix 1

7.1 Code for JAM-FE-FET

```
go atlas
mesh space.mult=1.0
x.mesh loc=0.000 spac=0.001
x.mesh loc=0.008 spac=0.001
x.mesh loc=0.010 spac=0.001
x.mesh loc=0.012 spac=0.0001
#x.mesh loc=0.050 spac=0.0001
x.mesh loc=0.108 spac=0.0001
x.mesh loc=0.110 spac=0.001
x.mesh loc=0.112 spac=0.001
x.mesh loc=0.120 spac=0.001

y.mesh loc=0.000 spac=0.001
y.mesh loc=0.002 spac=0.001
y.mesh loc=0.012 spac=0.001
y.mesh loc=0.0128 spac=0.001
y.mesh loc=0.0228 spac=0.001

region number=1 x.min=0.0 x.max=0.120 y.min=0.00 y.max=0.0356 material=Air
region number=2 x.min=0.0 x.max=0.010 y.min=0.0128 y.max=0.0228
material=Silicon
region number=3 x.min=0.010 x.max=0.110 y.min=0.0128 y.max=0.0228
material=Silicon
region number=4 x.min=0.110 x.max=0.120 y.min=0.0128 y.max=0.0228
material=Silicon
region number=5 x.min=0.010 x.max=0.110 y.min=0.002 y.max=0.012
material=HfO2
region number=6 x.min=0.010 x.max=0.110 y.min=0.012 y.max=0.0128
material=oxide

Electrode name=source number=1 x.min=0.0 x.max=0.008 y.min=0.012
y.max=0.0128
Electrode name=drain number=2 x.min=0.112 x.max=0.120 y.min=0.012
y.max=0.0128
Electrode name=gate number=3 x.min=0.010 x.max=0.110 y.min=0.00 y.max=0.002

doping uniform concentration=1e19 n.type x.min=0 x.max=0.010 y.min=0.0128
y.max=0.0228
doping uniform concentration=1e19 n.type x.min=0.110 x.max=0.120 y.min=0.0128
y.max=0.0228
```

```
doping uniform concentration=1e17 n.type x.min=0.010 x.max=0.110 y.min=0.0128
y.max=0.0228

interf qf=3e10

contact name=drain neutral
contact name=source neutral
contact name=gate workfunction=4.86

models srh cvt fermi print temperature=300
output val.band con.band qfn qfp e.field j.electron j.hole j.conduction j.total ex.field
ey.field flowline e.mobility h.mobility qss e.temp h.temp j.disp
mobility mun=100

# ferroelectric material defining
models region=5 ferro
material region=5 ferro.ec=1e6 ferro.pr=1e-6 ferro.ps=20e-6 ferro.epsf=31
#models region=8 ferro
#material region=8 ferro.ec=1e6 ferro.pr=1e-6 ferro.ps=20e-6 ferro.epsf=31
#material mun=100.0

save outf=ferro1_10nm.str
tonyplot ferro1_10nm.str

method gummel newton itlim=50 trap maxtrap=10
solve init
solve prev
#solve vdrain=0.05
#log outfile=ferro1_idvg_s_1.log master
#solve vgate4=0.0 vstep=0.05 vfinal=1.0 name=gate
#tonyplot ferro1_idvg_silicon1.log

Solve VDRAIN=0.01
#LOG OUTFILE=jnt_30nmidvg_sgmos_nmos.log
LOG OUTFILE=jnt_30nm_ac(1.0)_sgmos_nmos.log  master gains s.params
inport=gate outport=drain width=0.04
Solve NAME= GATE VGATE=0 VFINAL=1 VSTEP=0.1 ac freq=10E6
#extract name="vt1"x.val from curve(abs(v."gate"),abs(i."drain")) where \
        y.val=1e-7

###################transconductance###############
#extract name="gm" deriv(v."gate",i."drain")outfile="jnt_30nmgm_sgmos_nmos.dat"
#Solve VGATE=1.0
#LOG OUTFILE=jnt_30nmidvd_sgmos_nmos.log
```

```
#Solve NAME= DRAIN VDRAIN=0 VFINAL=1.0 VSTEP=0.1

##################outputconductance############
#extract name="gd" deriv(v."drain",i."drain") outfile="jnt_30nmgd_sgmos_nmos.dat"

quit
```

Appendix 2

7.2 Code for JAM-DG-FE-FET

```
go atlas
mesh space.mult=1.0
x.mesh loc=0.000 spac=0.001
#x.mesh loc=0.008 spac=0.001
x.mesh loc=0.010 spac=0.001
#x.mesh loc=0.012 spac=0.0001
#x.mesh loc=0.060 spac=0.0001
#x.mesh loc=0.108 spac=0.0001
x.mesh loc=0.110 spac=0.001
#x.mesh loc=0.112 spac=0.001
x.mesh loc=0.120 spac=0.001

y.mesh loc=0.000 spac=0.001
y.mesh loc=0.002 spac=0.001
y.mesh loc=0.012 spac=0.001
y.mesh loc=0.0128 spac=0.001
#y.mesh loc=0.016 spac=0.001
#y.mesh loc=0.018 spac=0.001
y.mesh loc=0.0228 spac=0.001
y.mesh loc=0.0236 spac=0.001
y.mesh loc=0.0336 spac=0.001
y.mesh loc=0.0356 spac=0.001
region number=1 x.min=0.0 x.max=0.120 y.min=0.00 y.max=0.0356 material=Air
region number=2 x.min=0.0 x.max=0.010 y.min=0.0128 y.max=0.0228 material=Silicon
region number=3 x.min=0.010 x.max=0.110 y.min=0.0128 y.max=0.0228 material=Silicon
region number=4 x.min=0.110 x.max=0.120 y.min=0.0128 y.max=0.0228 material=Silicon
region number=5 x.min=0.010 x.max=0.110 y.min=0.002 y.max=0.0120 material=HfO2
region number=7 x.min=0.010 x.max=0.110 y.min=0.0236 y.max=0.0336 material=HfO2
```

```
region number=6 x.min=0.010 x.max=0.110 y.min=0.0120 y.max=0.0128 material=oxide
region number=8 x.min=0.010 x.max=0.110 y.min=0.0228 y.max=0.0236 material=oxide
#region number=9 x.min=0 x.max=0.120 y.min=0.0246 y.max=0.0248 material=GaN

Electrode name=source number=1 x.min=0.0 x.max=0.010 y.min=0.012 y.max=0.0128
Electrode name=drain number=2 x.min=0.110 x.max=0.120 y.min=0.012 y.max=0.0128
Electrode name=gate number=3 x.min=0.010 x.max=0.110 y.min=0.00 y.max=0.002
Electrode name=gate1 number=4 x.min=0.010 x.max=0.110 y.min=0.0336 y.max=0.0356

doping uniform concentration=1e19 n.type x.min=0 x.max=0.010 y.min=0.0128 y.max=0.0228
doping uniform concentration=1e19 n.type x.min=0.110 x.max=0.120 y.min=0.0128 y.max=0.0228
doping uniform concentration=1e17 n.type x.min=0.010 x.max=0.110 y.min=0.0128 y.max=0.0228
#doping uniform concentration=1e17 p.type x.min=0 x.max=0.120 y.min=0.018 y.max=0.0228

interf qf=3e10

contact name=drain neutral
contact name=source neutral
contact name=gate workfunction=4.85
contact name=gate1 workfunction=4.85  common= gate

models srh cvt fermi print temperature=300
output val.band con.band qfn qfp e.field j.electron j.hole j.conduction j.total ex.field ey.field flowline e.mobility h.mobility qss e.temp h.temp j.disp
mobility mun=100


# ferroelectric material defining
models region=5 ferro
material region=5 ferro.ec=1e6 ferro.pr=1e-6 ferro.ps=20e-6 ferro.epsf=31
models region=7 ferro
material region=7 ferro.ec=1e6 ferro.pr=1e-6 ferro.ps=20e-6 ferro.epsf=31
material mun=100.0


save outf=ferro1_10nm.str
```

```
tonyplot ferro1_10nm.str

method gummel newton itlim=50 trap maxtrap=10
solve init
solve prev
#solve vdrain=0.01
#log outfile=ferro1_idvg_stack.log master
#solve vgate4=0.0 vstep=0.1 vfinal=1.0 name=gate
#tonyplot ferro1_idvg_dgmos.log


####################transconductance###############
#extract name="gm" deriv(v."gate",i."drain")outfile="jnt_30nmgm_dgmos.dat"

#Solve VGATE=1.0
#LOG OUTFILE=jnt_30nmidvd_dgmos_nmos.log
#Solve NAME= DRAIN VDRAIN=0 VFINAL=1.0 VSTEP=0.1


###################outputconductance############
#extract name="gd" deriv(v."drain",i."drain") outfile="jnt_30nmgd_dgmos_nmos.dat"
Solve VDRAIN=0.05
LOG OUTFILE=jnt_30nmidvg_dgmos1_nmos.log
#LOG OUTFILE=jnt_30nm_ac(1.0)_dgmos_nmos.log master gains s.param
inport=gate outport=drain width=0.4

Solve NAME= GATE VGATE=0 VFINAL=1 VSTEP=0.1
#ac freq=1E06
#extract name="vt1"x.val from curve(abs(v."gate"),abs(i."drain")) where \
        y.val=1e-7

####################transconductance###############
extract name="gm" deriv(v."gate",i."drain")outfile="jnt_30nmgm_dgmos1_nmos.dat"

quit
```