MEMRISTOR SPICE MODEL COMPARISON FOR NEUROMORPHIC COMPUTING

A DISSERTATION REPORT

SUBMITTED IN PARTIAL FULFILMENT OF THE
REQUIREMENTS FOR THE AWARD OF THE DEGREE

OF

MASTER OF TECHNOLOGY
IN
VLSI DESIGN AND EMBEDDED SYSTEMS

SUBMITTED BY

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I, Suraj Gupta, Roll No. 2K22/VLS/20, student of M.Tech (VLSI Design & Embedded System), hereby declare that the Project Dissertation titled **"Memristor Spice Model Comparison For Neuromorphic Computing"** which is submitted by me to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology is original and not derived from any source without appropriate citation. This work has not previously formed the basis for the award of any Degree, Diploma Associate-ship, Fellowship, or other similar title or recognition.

Place: Delhi

Date: 31 May, 2024

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CERTIFICATE

I hereby certify that the Project Dissertation titled **"Memristor Spice Model Comparison For Neuromorphic Computing"** which is submitted by Suraj Gupta Roll No. 2K22/VLS/20 Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge, this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ABSTRACT

Memristors, also known as memory resistors, are a novel kind of electrical component that set them apart from more conventional passive circuit components. This abstract provides a concise overview of memristor technology, covering their fundamental properties, diverse applications, and the promising future they hold in the realm of electronics.

Memristors exhibit non-volatile memory behavior, retaining resistance states even when power is turned off. Their V-I (voltage-current) characteristics display non-linear, hysteresis-driven responses, allowing for precise control and manipulation of resistance. Because of this, memristors are appropriate for a variety of uses, including neuromorphic computing and non-volatile memory storage. The essential properties of memristors, including as their resistance-switching ability, bistability, and dual-mode operation. They are use in developing fields like brain-inspired computing and non-volatile memory. Because memristors provide faster, more energy-efficient solutions, they have the potential to completely transform memory technologies.

Memristor device modeling is required for memristor-based circuit and system design. This study reviews the state-of-the-art memristor modeling methods and offers simulations that compare a number of models with memristor characterization data that has been published. The simulations have been completed in LTspice, to compare the output of the various models to the relationships between current and voltage in real devices. Throughout the simulations, sine and triangle pulse inputs were used to assess each model's capabilities.

Keywords: Memristors, neuromorphic computing, von neumann architecture, non-volatile memory, LTspice simulation, Integrated circuit, Semiconductor, window function, SPICE model.

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CHAPTER 1
INTRODUCTION

1.1 Overview

A memristor, or memory plus resistor, was the missing circuit element that Leon Chua introduced in 1971 [1]. He revealed that there are proven correlations for five of the six conceivable variations on the 4 primary electronic circuit (i, v, q, and Φ). The trio of circuit components, resistor (R = dv/dt), inductor (L = dΦ/di), and capacitor (C = dq/dv), provide the remaining information. Utilizing the concept of symmetry, he asserted the existence of A fourth essential component known as a memristor, characterized as A link between between magnetic flux and charge (M = dΦ/dq). A memristor is a two-terminal electrical device where magnetic flux and electric charge are coupled in a nonlinear way.

A memristor, as opposed to a linear or nonlinear resistor, displays a vital connection between voltage and current and remembers previous voltages or currents. Chua provided a mathematical generality to the dynamic memory resistors that other scientists had developed, such as Bernard Window's memistor. While he demonstrated the practical realization of a memristor in laboratory settings through active circuits, it wasn't until May 2008 that the physical manifestation of a memristor as a distinct device was first uncovered.

Characteristics and derivation:

The memristor was initially described as a the nonlinear functional interaction between the quantity of electric charge that has flown q(t), and the magnetic flux linkage Φm(t):

$$F(\Phi m(t), q(t)) = 0 \quad \text{(i)}$$

The inductor's circuit characteristic serves as a generalization for the magnetic flux linkage, or Φm. Here, it does not symbolize a magnetic field. One could think of the symbol Φm as the voltage integral over time.

$$M(q) = \frac{d\phi}{dq} \quad \text{(ii)}$$

The following more practical forms result from substituting charge for the period integral of current and flux for the time integral of voltage:

$$M(q) = \frac{(\frac{d\phi}{dt})}{\frac{dq}{dt}} = \frac{V(t)}{I(t)} \quad \text{(iii)}$$

Table 1: Differential equation of fundamental elements

Device	Characteristic (units)	Differential equation
Memristor (*M*)	Memristance (Wb / C, or ohm)	$M = \mathrm{d}\Phi_\mathrm{m} / \mathrm{d}q$
Inductor (*L*)	Inductance (Wb / A, or henry)	$L = \mathrm{d}\Phi_\mathrm{m} / \mathrm{d}I$
Capacitor (*C*)	Capacitance (C / V, or farad)	$C = \mathrm{d}q / \mathrm{d}V$
Resistor (*R*)	Resistance (V / A, or ohm, Ω)	$R = \mathrm{d}V / \mathrm{d}I$

This suggests that the resistance of memristance is dependent on charge. Ohm's law, R(t) = V(t)/I(t), is obtained if M(q(t)) is a constant. But since q(t) and M(q(t)) are subject to change over time, the equation is not equivalent if M(q(t)) is nontrivial.

$$V(t) = M(q(t) \times I(t) \quad \text{(iv)}$$

If the memristance (M) remains constant with charge, This mathematical expression illustrates that memory establishes a straightaway connection between current and voltage. Nonzero current indicates changing charge over time. However, alternating current can highlight direct dependency during circuit functioning by generating a quantifiable voltage with no inducing transfers of total charges throughout the time as the greatest variation in charge (q) doesn't significantly affect M.

1.2 HP Laboratories' Established Memristor Model

The memristor was first proposed by Dr. Leon Chua in 1971 [1], and the technology was first created in 2008 at HP Labs by a research group under the direction of Dr. Stanley Williams [2]. AtHP Labs, a light coat TiO2 memristor was manufactured. The

device consisted of two platinum electrodes encased in a stoichiometric (TiO2) and an oxygen-deficient (TiO2−x) layer.

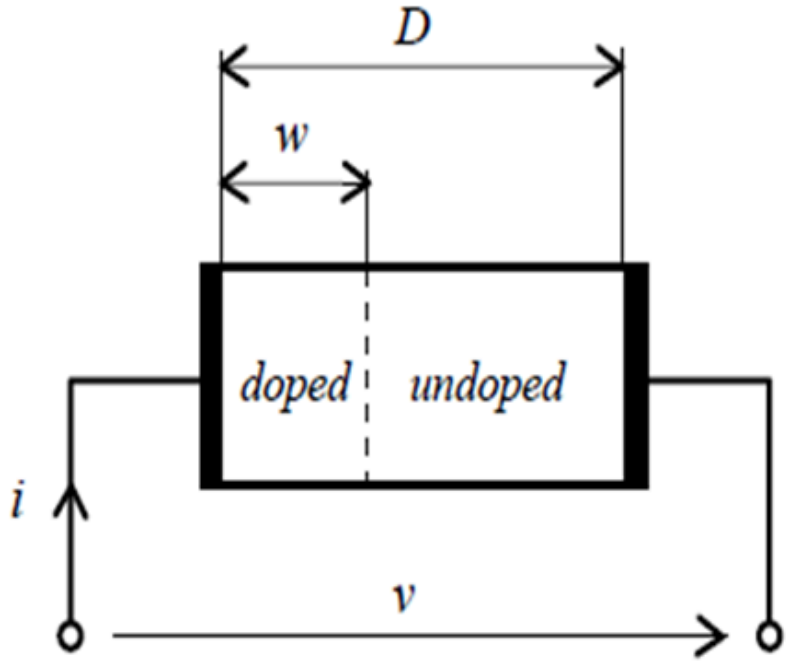


Fig.1.1: Memristor model proposed by HP Laboratories' Dr. Stanley Williams [4].

When a voltage is applied over a memristor, The TiO2-x layer's oxygen shortages propagate, resulting in a modification of the layer's thickness. Similarly, this modifies the memristor device's resistance. Oxygen vacant positions move very slowly and choose to remain in one location once the voltage input is withdrawn. This event demonstrates how a memristor is utilized as a nonvolatile storage device. A memristor stores information through its resistance.

The two-layer TiO2 thin film (size D = 10 nm) that is inserted among platinum contacts makes up the anatomical form of the memristor. Because one of the surfaces has oxygen vacancies doped in it, it functions like a semiconductor. The undoped portion in the second place is insulating. A complex series of material reactions results in an electric charge that flows through the memristor, influencing the width (w) of the doped zone. The separation across the two zones moves in identical directions as the electric current flowing through it.

The relationship between the device thickness D and the quantity inside the dynamical state parameter w(t) determines true resistance of the device. The oxygen-deficient titanium dioxide layer (TiO2−x) has a thickness symbolized by w(t), the state variable. The total device resistance decreases as w(t) grows since ROFF > RON.

$$V(t) = [R_{on} \times \frac{w(t)}{D} + R_{off} \times (1 - \frac{w(t)}{D})] \times I(t) \quad (1)$$

Equation (2) can determine the changing value of the state variable over time, with dw/dt representing the drift velocity of oxygen deficiencies (vD) within the device.

$$vD = \frac{dw}{dt} = [\mu_D \times \frac{Ron}{D}] \times i(t) \quad (2)$$

Integrating Eq. (2) yields the value for w(t), and the result is shown in Eq. (3). Integration reveals how the equation of W (t) is directly related to the charg(q) of device. This explains why memristors have a non-volatile effect: when no current flows across the device, the resistance stays constant since the amount of charge is the integration of the current.

$$w(t) = [\mu_D \times \frac{Ron}{D}] \times q(t) \quad (3)$$

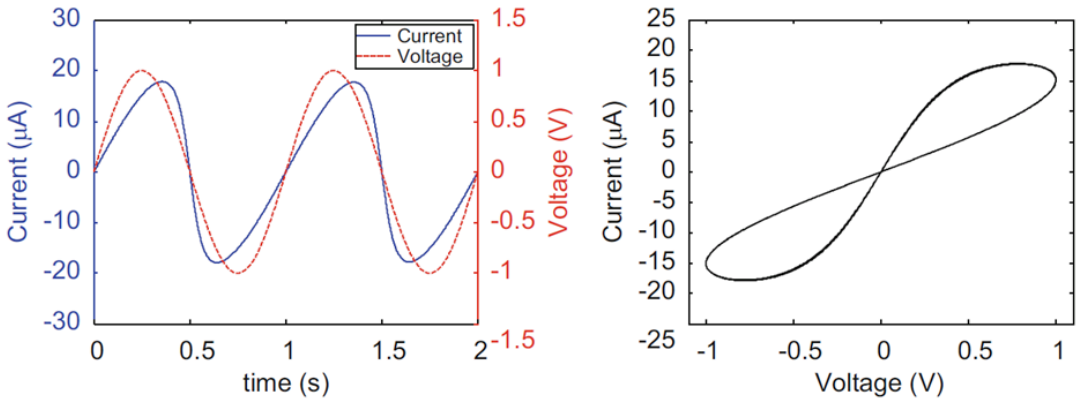


Fig.1.2: Simulation outcomes for a sinusoidally input memristor from HP Laboratories [13].

A constricted hysteresis looping process, which is characteristic of memristors, is shown in the I-V curve. Since multiple current values can be connected to a single voltage, the hysteresis demonstrates the fact that the conductance of a memristor is associated with the earlier value of the state parameter w(t).

CHAPTER 2

LITERATURE REVIEW

Reviewing current literature is critical. The goal of a literature review is to develop a basic understanding of the topic, identify areas of past expertise to prevent repetition and credit other researchers, and find discrepancies, research gaps, major disputes, and unsolved difficulties in earlier studies.

2.1 PREVIOUS REPORTED WORK:

Chua, L.O. (1971) [1] invented a novel two-terminal structure element called the memristor, defined by a connection across charge and flux linkage. This element is suggested as the 4th elementary circuit element. The study interprets this relationship using the quasi-static expansion of Maxwell's equations.

R. Stanley Williams (2008) [2] explains the invention and development of the memristor. The article describes the path of the HP Labs research team, lead by Williams, who discovered and built the first practical memristor. The paper summarizes the theoretical basis supplied by Dr. Leon Chua's previous work and discusses how the HP Labs team was able to transfer these theoretical principles into a practical device. The finding is noteworthy because it verifies the presence of the fourth essential passive circuit element, which completes the quartet together with the resistor, capacitor, and inductor.

Joglekar YN, Wolf SJ (2009) [3] The authors examine the theoretical characteristics and applications of memristors in fundamental electrical circuits. The study gives a complete examination of memristors, which are classified as the fourth essential passive circuit element after resistors, capacitors, and inductors.

Biolek Z, Biolek D, Biolková V (2009) [4] the authors develop and present a SPICE model for simulating memristors that incorporates nonlinear dopant drift. This work

addresses the need for a more accurate and practical way to model memristor behavior in electronic circuit simulations.

Pino, R. E., Bohl, J. W (2010) [5] The study describes a compact and efficient approach for modeling and simulating ion conductor chalcogenide-based memristors. The proposed model is validated using experimental data, confirming its correctness and usefulness for approximating memristor behavior in a variety of application settings. The model's modest size makes it a useful tool for designers working on circuits and systems that use memristors.

Abdalla and Pickett's (2011) [6] study describes the creation and validation of SPICE models for memristors, which can then be simulated using normal circuit design tools. The models accurately represent the distinct properties of memristors and are confirmed using experimental data. The study also explores the models' possible uses in various circuit design scenarios, as well as thorough implementation directions for incorporating them into SPICE simulations.

The research by Laiho et al.(2010) [7] examines the current state and future possibilities of memristive synapses in neuromorphic systems. It examines the biological inspiration, current advances, applications, problems, and experimental results for memristive synapses, emphasizing their ability to mimic biological synaptic function and contribute to the evolution of neuromorphic engineering.

Laiho et al. (2011) [8] examine the current state and future possibilities for memristive synapses in neuromorphic devices. It examines the biological inspiration, current advances, applications, problems, and experimental results for memristive synapses, emphasizing their potential to mimic biological synaptic function and promote neuromorphic engineering.

Yakopcic et al.'s (2013) [12] study gives a thorough SPICE model for memristors with nanosecond switching speeds and shows how to use it to simulate memristor crossbar arrays. The study emphasizes the need of proper modeling for creating high-performance memristor-based circuits and investigates the possibilities of these devices for upcoming computing technologies.

Zheng et al.'s(2015) [14] work discusses the design, implementation, and applications of memristor-based synapses and neurons in neuromorphic computing. The study advances the field of cognitive computing by using the distinct capabilities of memristive devices to create brain-inspired computer systems.

CHAPTER 3

INITIAL MEMRISTOR SPICE MODELING

3.1 Overview

Because the capacity to recreate the memristor in SPICE simulators is particularly useful for circuit designers, SPICE subcircuits for memristors were created using Eqs. (1) and (2). These original equations were changed in order to develop a reliable method based on these basic equations for memristor simulation. First, it should be mentioned that the variable substitution x(t)=w(t)/D was used to update the state variable equations. Now, The scaled state variable is numbered in the range of 0 and 1. The least conductive state of the memristor device is at x(t)=0, and the state that conducts foremost is at x(t)=1. Ever since memristor devices were suggested with a variety of material structures [7–12], the change in titanium oxide layer thickness is not always the cause of the resistance switching mechanism. By changing the state variable, the model is made more general, in order for it to serve as a representation device other than titanium oxide ones.

The bounds of the state variables were then established. The state variable bounds, x(t) between 0 to 1, are not taken into consideration by the computational equations in chapter 1. The magnitude of x(t) will increase to more than 1 if the memristor receives enough charge, which will cause the model's output to become unstable and erroneous. Two distinct windowing functions were used to restrict the state variable's movement, and SPICE versions were created using these altered equations as a basis.

3.2 Joglekar Modifications

Yogesh N. Joglekar and Stephen J. Wolf altered the original equations created by HP Labs [2] in a journal [3]. The parameter η was created to model memristors in which the state variable could change in relation to the input voltage in any direction. If a memristor receives a positive voltage signal that raises the state variable's value, the memristor component should be represented with η is equal to 1. For a memristor, η =

-1 should be used when a positive voltage signal is given and the state variable decreases.

Furthermore, The state variable motion equation was extended to include the windowing function found in Eq. (4). By doing this, it is guaranteed that the state variable will always lie between x(t)=0 and x(t)=1. As illustrated in the left plot of Fig. 12.3, the Joglekar window function creates boundaries by guaranteeing that the state variable motion is zero at x(t)=0 or x(t)=1. Depending on the value of p, the function can give a more balanced non-linearity in the state variable motion with p = 1 or a more prominent boundary effect with p = 100 p=100. Equation (5) displays The equation for state variables in its adjusted form. It should be noted that the substitution x(t)=w(t)/D has resulted in a squared parameter D.

$$F(x(t)) = 1 - (2(x(t) - 1)^{2p} \tag{4}$$

$$\frac{dx}{dt} = [\eta \times \mu_D \times \frac{Ron}{D^2}] \times I(t) \times F(x(t)) \tag{5}$$

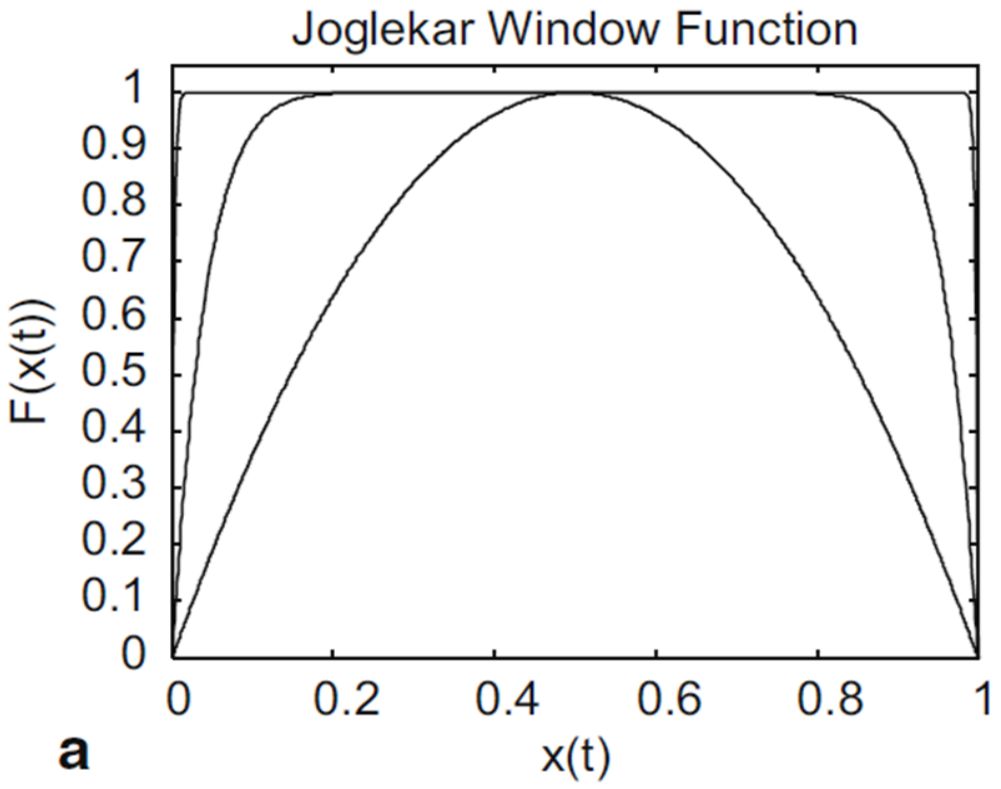


Fig.3.1: Joglekar window functions for p at 1, p at 6, and p at 100 [13].

It is evident that setting p to a high value in every windowing function can provide the desired tight restriction effect at the borders.

3.3 The Results of Simulation with Joglekar Window

The Joglekar window function code for the memristor subcircuit was taken from [3].

Simulation Result:

Input signal: sinusoidal wave

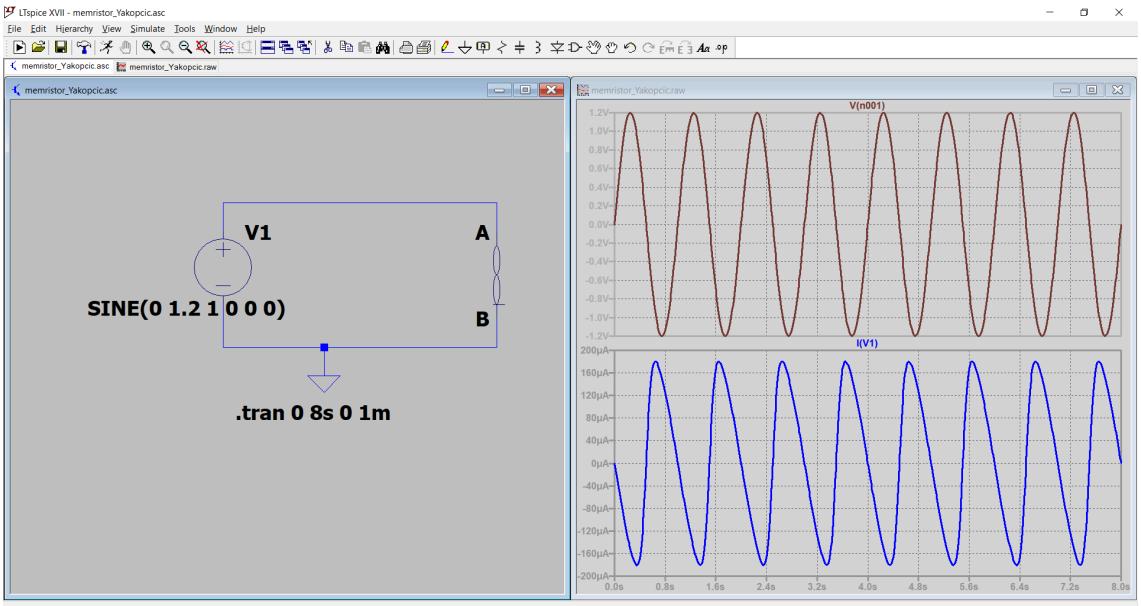


Fig.3.2: Input voltage and current waveform.

I-V characteristics:

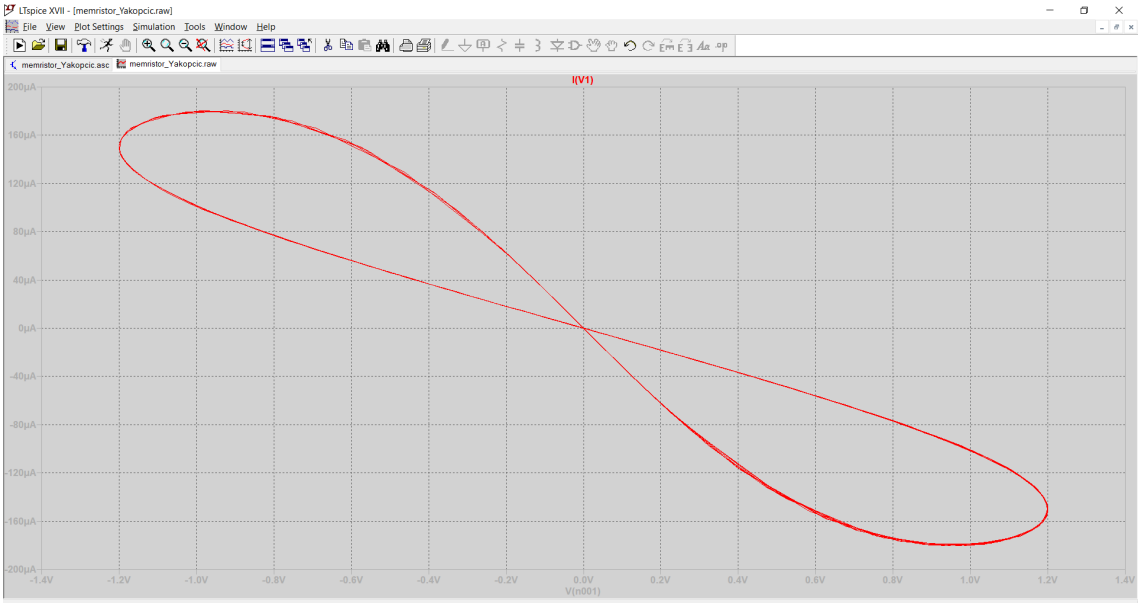


Fig.3.3:Results of the LTspice simulation for the sinusoidally input memristor model.

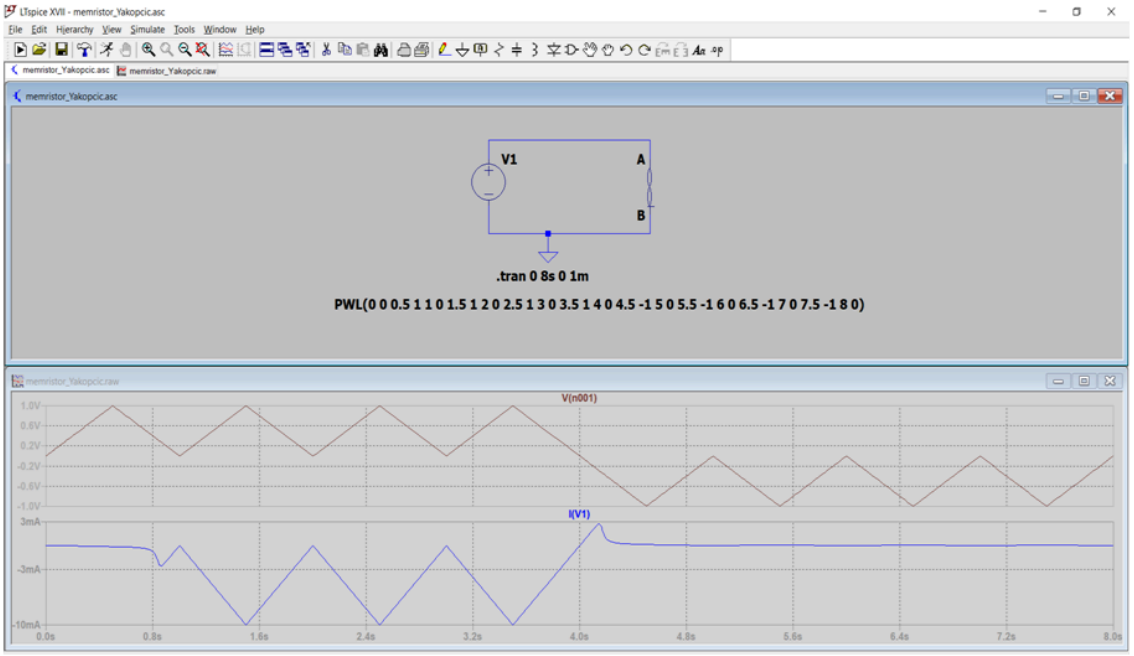


Fig.3.4: Input voltage and current waveform.

I-V characteristics:

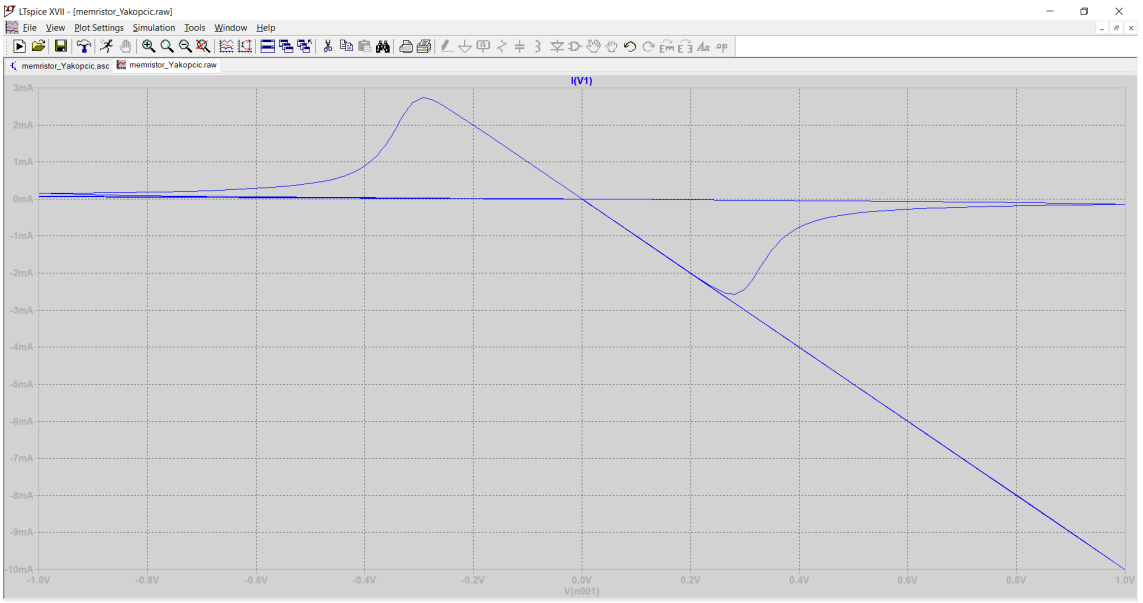


Fig.3.5: Results of the LTspice simulation for a triangular pulsed input memristor model. Triangle pulses have a growth and decline period of 0.5 s, a amplitude of 1 V, and a puls duration of 1 s.

3.4 Biolek Modifications

Zdenek Biolek proposed an alternate window function in a publication [4]. Biolek's window function precisely minimizes the velocity only when the state variable is traveling toward the boundary, in contrast to Joglekar's suggested windowing function [3], which inhibits the state variable's movement in proximity to the border regardless if it is near or advancing away. This adaptation appears to be a more accurate inference, supported by data from HP Labs. The mathematical expressions for the Biolek window function are provided in Eqs. (6) and (7).

$$F(x(t)) = 1 - (x(t) - stp(-I(t)))^{2p} \quad (6)$$

$$stp(I(t)) = \begin{cases} 1, & \text{if } I(t) > 0 \\ 0, & \text{if } I(t) < 0 \end{cases} \quad (7)$$

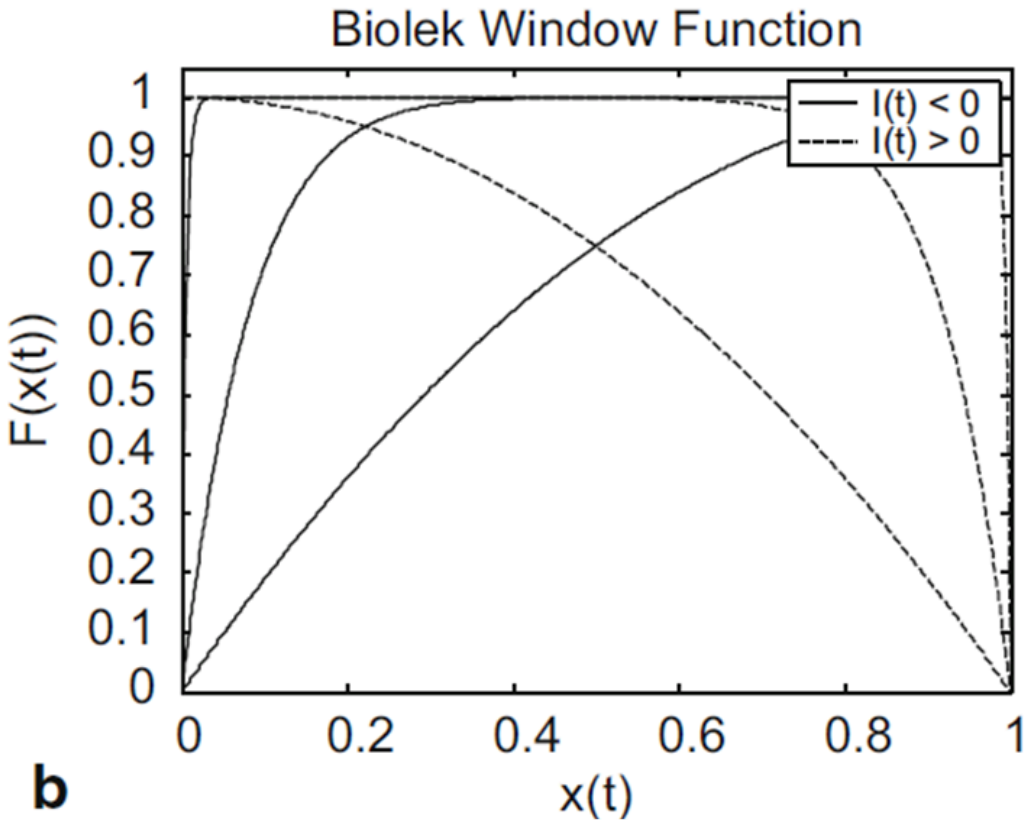


Fig.3.6: Functions of the biolek window at p=1, p=6, and p=100 [13].

The cumulative effect of the resistances in the doped and undoped areas of the memristor, or RMEM, is the total resistance,

$$R_{mem}(x) = R_{on}(x) + R_{off}(1 - x) \quad (8)$$

where x= w/D $\in$ (0,1) (9)

For w is equals to 0 and w is equal to D, the memristor resistance's limit values are denoted by ROFF and RON. The standard notation for the ratio of each of the resistances is 102 - 103.

The link that exists with the memristor's voltage and current of the memristor is applicable through Ohm's law:

$$V(t) = R_{mem}(w) \times i(t) \quad (10)$$

The state equation states that the resistance of the doped location, the current flowing through, and other parameters affect the speed of boundary migration that occurs between doped and undoped regions:

$$\frac{dx}{dt} = k \times i(t) \times f(x) \quad (11)$$

small voltages in nanoscale devices can produce massive electric fields, which can subsequently lead to significant ionic transport nonlinearities. The nonlinearities in question are especially noticeable at the thin film borders, where the velocity of the separation between the regions that are doped and undoped progressively approaches zero. Nonlinear dopant drift is a phenomenon that can be represented by the window function f(x).

3.5 Outcomes of the Biolek Window Simulation

Reference [4] Specifies a script for memristor circuit that makes use of the Biolek Window function.

Result:

Input signal: sinusoidal wave

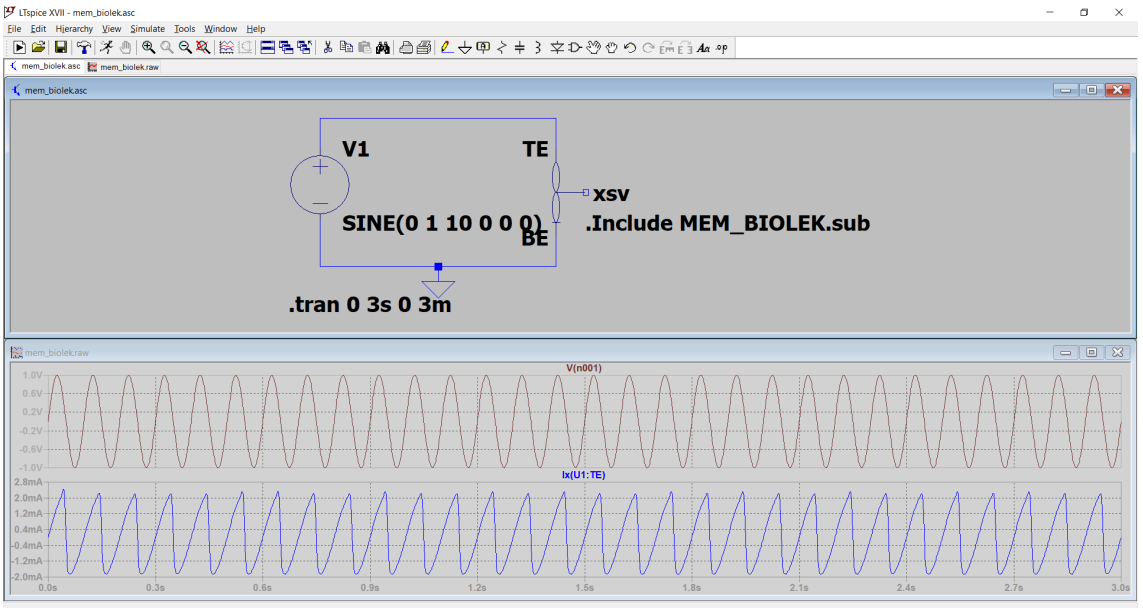


Fig.3.7: Input voltage and current waveform.

I-V characteristics:

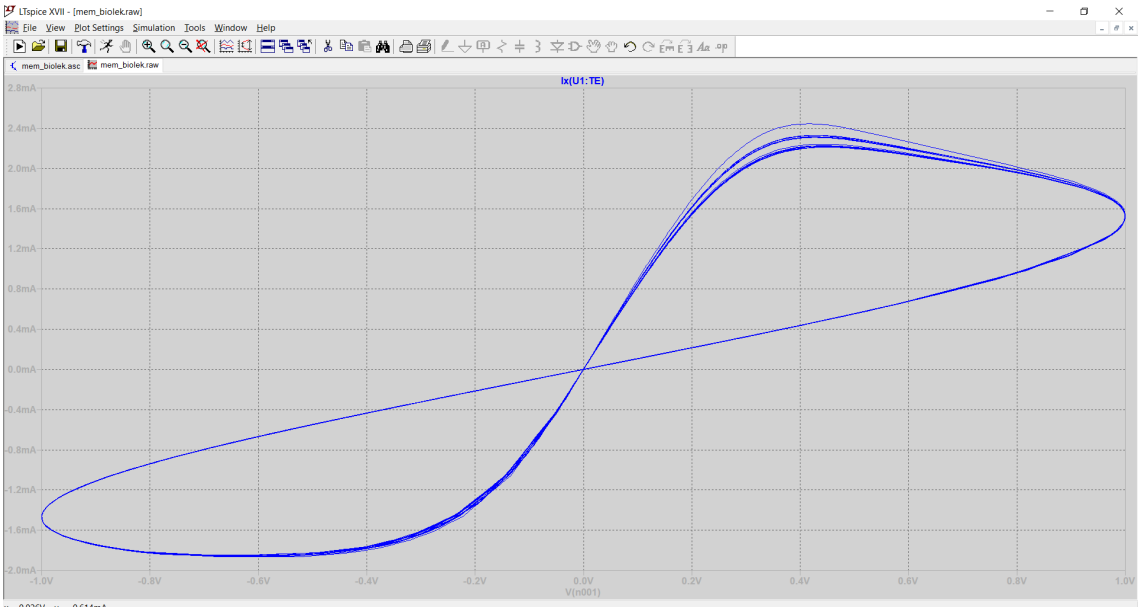


Fig.3.8: Results of the Biolek memristor model simulation with a sinusoidal input, performed with LTspice.

Input signal: triangular waveform

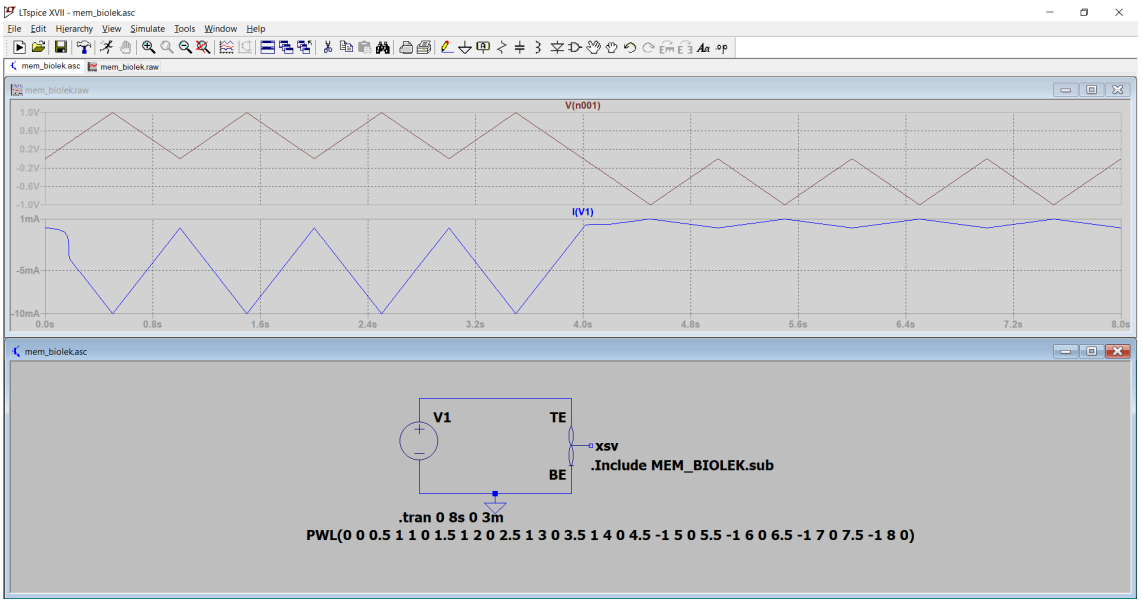


Fig.3.9a: Input voltage and current waveform.

I-V characteristics:

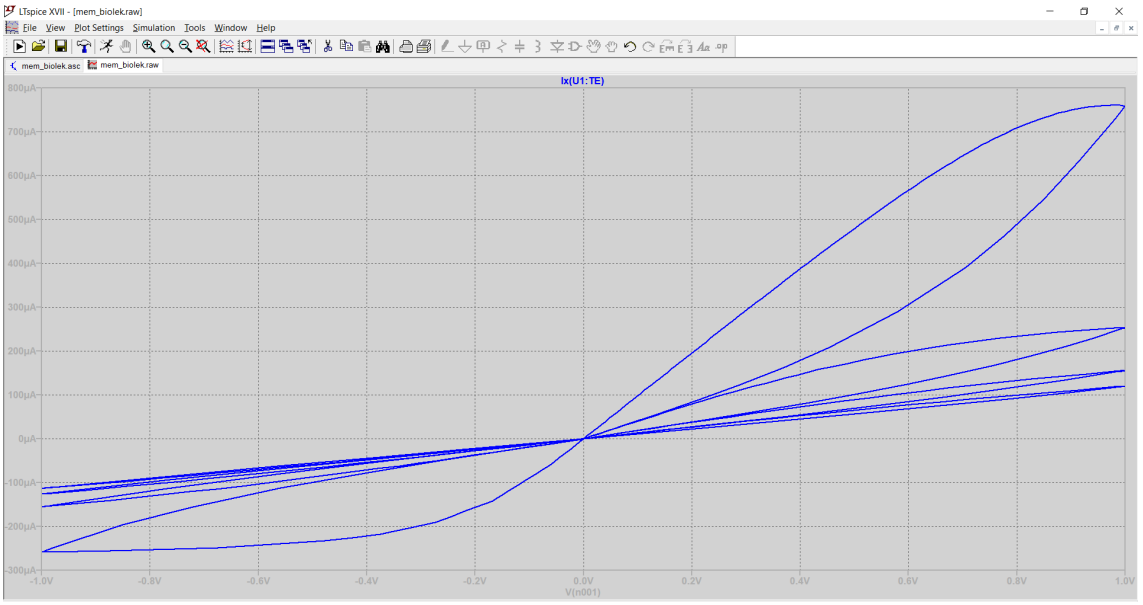


Fig.3.9b: Results of an LTspice simulation using a triangular pulsed input for the Biolek memristor model. Triangle pulses have a 1 V magnitude, a 1 s pulse width, and a 0.5 s rise and fall period.

Chapter 4

Hardware Correlated Models

4.1 Introduction

When comparing existing physical characterization data with the outcomes of the Joglekar [3] and Biolek [4] models, there are a number of differences. These models demonstrate that when a pulsed wave is applied, the diameter of the loops that cause hysteresis in the positive sector increases with conductivity. On the other hand, the tendency in the published characterisation data is the opposite. Furthermore, there is a threshold voltage at which no hysteresis is seen in physical memristor devices. These versions lack this threshold voltage.

Other models of memristors have been suggested, aligning more nearly with physical characterization data. This portion explores two distinct approaches to memristor modeling employing sinusoidal input voltage instead of a continuous pulse supply. Both models demonstrate a close alignment with specific memristor devices in terms of their outcomes.

4.2 Air Force Research Lab Model

The initial HW-correlated framework to mimic the current-voltage characteristics of a device was created by Dr. Robinson E. Pino and his colleagues at the Air Force Research Lab (AFRL) [5]. By connecting the slope to a piecewise function and voltage amplitude that is specifically designed to correspond with the physical device's characterization, this model successfully aligns with the I–V characteristic. Compared to using a state variable to indicate the change of resistance with time, this model uses Eqs. (12) and (13) directly. More specifically, Eq. (12) is employed to ascertain how the memristor device's resistance as the voltage exceeds Th (threshold). In contrast, the change in device resistance is found using Eq. (13) when the voltage drops below Tl (threshold low). Interestingly, resistance does not change the moment the memristor's voltage is between Tlv(t) ≤ Th.

$$\frac{dR}{dt} = \begin{cases} -Kh1 \times e^{kh_2(V(t)) - Th)} & R(t) > RON \end{cases}$$

$$0, \qquad R(t) \leq RON$$
$$\} \qquad (12)$$

$$\frac{dR}{dt} = \{$$
$$k_{l1} \times e^{k_{l2}(v(t)) - Tl)} \qquad R(t) < ROFF$$
$$0, \qquad R(t) \geq ROFF$$
$$\} \qquad (13)$$

Three terminals make up the model: Two terminals are used for the top and bottom electrodes, while a 3rd terminal is used to represent the integral of the rate equation. Since resistance is only declared state variable, The connector RSV displays the variation in resistance. One can calculate the current flowing through the memristor by dividing the two voltages. While V (rsv) is shown in the simulation as a voltage, It accurately portrays the memristor's resistance.

4.3 AFRL Model's Simulation Results

Reference [5] Provides a script for memristor subcircuit that makes use of the AFRL Model created by Dr. Robinson E. Pino.

Simulation Result:

Input signal: sinusoidal waveform

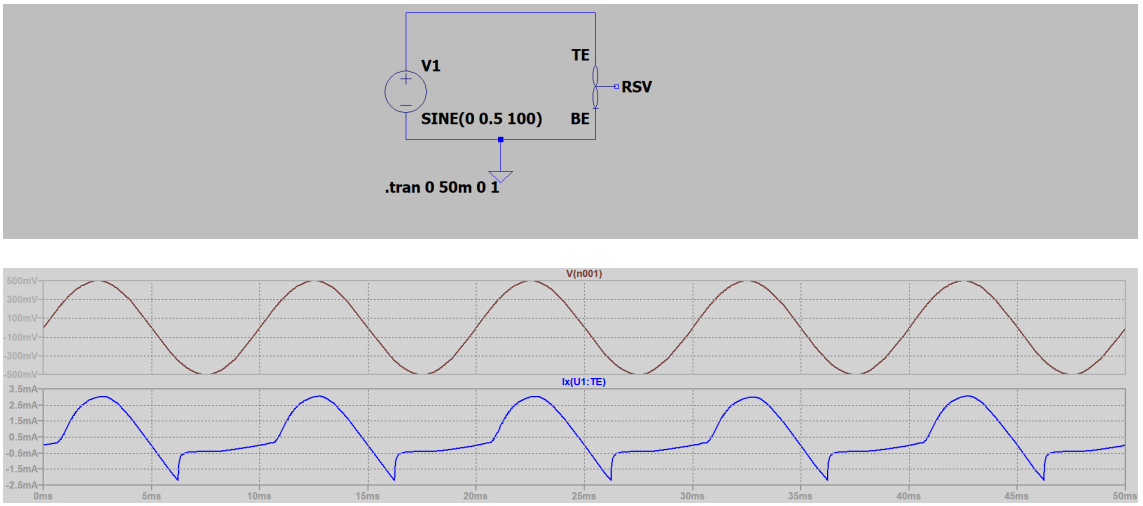


Fig.4.1: Waves for the source voltage and current

I-V characteristics:

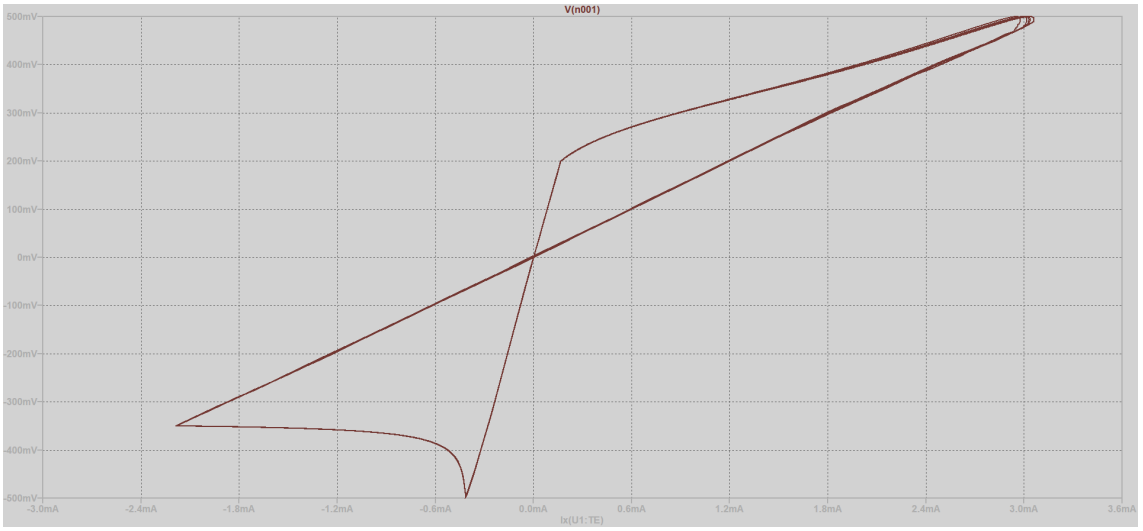


Fig.4.2: Results of the LTspice simulation using a sinusoidal input for the PINO HP Labs MIM Model.

4.4 MIM Model from HP Labs

At HP Labs, Drs. Hisham Abdalla and Matthew D. Pickett presented a more intricate model [6]. This model is grounded in the (MIM) tunnel barrier function for memristor

[6]. The memristor's structure includes a TiO2 layer acting as a barrier and a TiO2−x layer functioning having a low resistance metal covering. Notably, the tunnel barrier's width is observed to increase with applied voltage, modulating because of the locations of oxygen vacancies within the apparatus. This particular model demonstrates a notable alignment with the characterization data, and its validity is reinforced by a close connection to the internal mechanical components of the device.

One can examine the model equations in (14) through (18). The variable of dynamic state in these equations is designated as w(t). However, the TiO2 layer thickness in this model is represented by w(t), rather than the TiO2−x layer. Equations (14) and (15) control the state variable's dynamics.

$$\frac{dw}{dt} = f_{off} \times sinh(\frac{|i(t)|}{i_{off}}) \times e^{[\frac{-exp(w(t)-a_{off})}{wc} - \frac{|I(t)|}{b}]} - \frac{w(t)}{wc} \quad (14)$$

$$\frac{dw}{dt} = -f_{off} \times sinh\frac{|i(t)|}{i_{on}} e^{[-exp(a_{on} - \frac{w(t)}{wc} - \frac{|i(t)|}{b}) - \frac{w(t)}{wc}]} \quad (15)$$

Eq. (14) describes the state variable motion when I(t) > 0, whereas Eq. (15) describes the state variable motion in all other cases. f_off at 3.5 μs, ioff at 115 μA, aoff is 1.2 nm, f_on at 40 μs, ion is 8.9 μA, aon is 1.8 nm, b is 500 μA, and wc is 107 pm were the model's fitting parameters.

To take into consideration a variable barrier width, formulas (16) through (18) were created through altering Initial publication of the MIM tunnel barrier formulations may be found in reference [26]. φ0 = 0.95 V, w1 = 0.1261 nm, B = 10.24634_w, _ = 0.0998/w(t), and _w = w2 − w1 are the values of these equations. The voltage through the memristor's TiO2 layer is shown by the variable vg. The total of vg plus vr, with vr being the voltage within the TiO2−x layer, represents the entire voltage across the device.

$$I(t) = \frac{0.0617}{\Delta w^2}\{\phi_I \times e^{-B\sqrt{\phi_I}} - (\phi_I + |Vg|)e^{-B\sqrt{\phi_I + |Vg|}}\} \quad (16)$$

$$\phi_I = \phi_0 - |vg| \times \frac{(w1+w2)}{(w(t))} - (\frac{0.1148}{w})ln(w2\,(w(t) - w1) \div (w1 \times (wt - w2)) \quad (17)$$

$$w2 = w1 + w(t)(1 - \frac{9.2\lambda}{2.85 + 4\lambda - 2|vg|}) \quad (18)$$

The circuit used to evaluate this memristor model is shown in Fig. 3.3. A 2.4 kΩ resistor was provided to mimic the resistance of the electrodes used to characterize the memristor device.

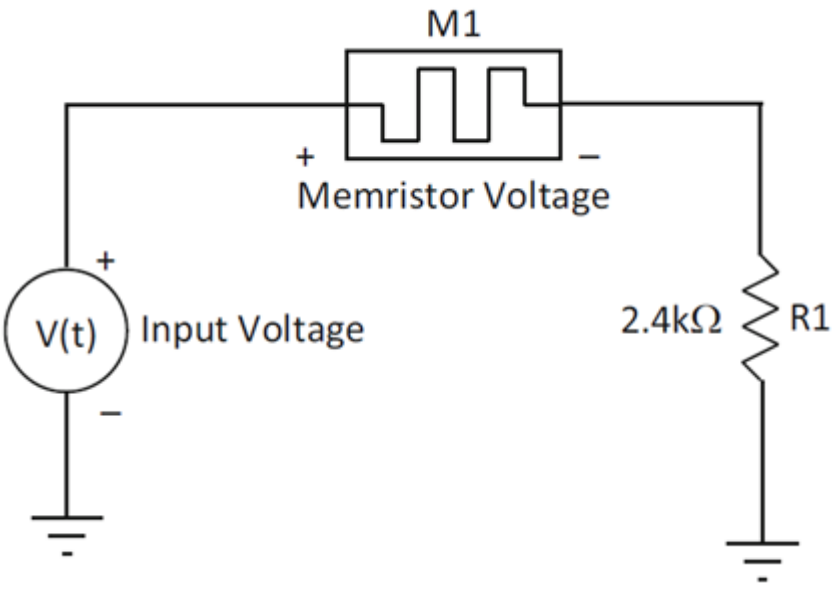


Fig. 4.3: Schematic fortesting the MIM memristor model [13]

4.5 MIM Model's simulation Results

The memristor subcircuit code, which makes use of the MIM Models is obtained from [6].

Simulation Result:

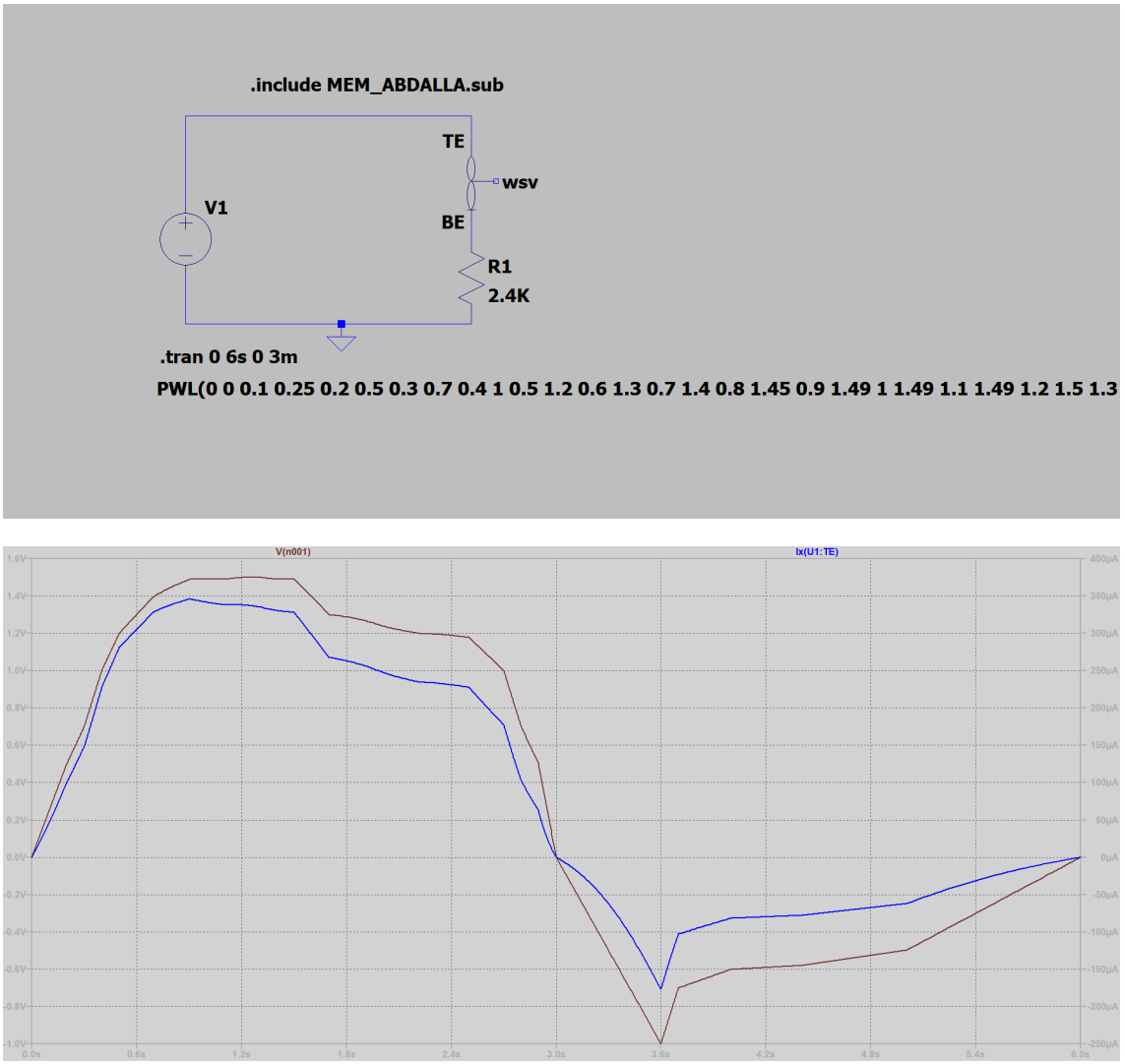


Fig.4.4: Applied waveforms of the input voltage and current

I-V characteristics:

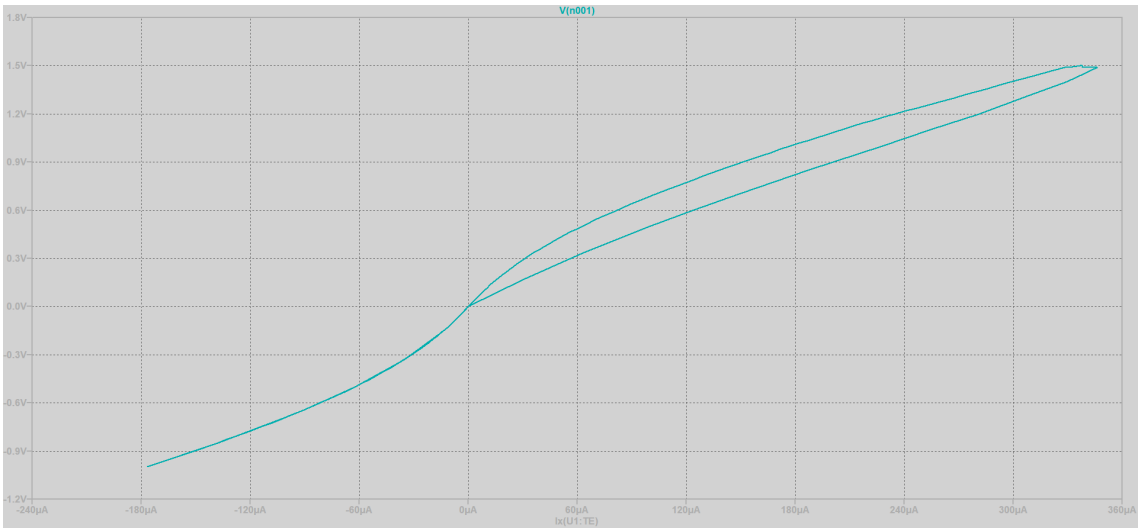


Fig.4.5: Results of simulations utilizing the HP Labs MIM model.

Chapter 5

Hyperbolic Sine Models

5.1 Introduction

Because of its adaptability, For numerous memristor models, the hyperbolic sinusoid geometry has been selected. The reason for this decision is because the I–V connection of a Metal–Insulator–Metal (MIM) junction may be accurately approximated by the hyperbolic sinusoid function [6]. It makes sense to model a thin-film memristor as a metal-insulator membrane (MIM) device as these devices are usually formed by encasing two metal electrodes with an oxide substance in between. Results seem to be much better when a An hyperbolic sine distribution is used in the voltage-current characteristic, especially when a repeating voltage pulse input is employed.

5.2 General Hyperbolic Sine Model

Dr. Mika Laiho and associates [7] provided a thorough hyperbolic sinusoid model, which is explained in Eqs. (19) and (20). The state variable x(t) modulates a hyperbolic sinusoid in the model, which represents the current-voltage connection.Some of the parameters that affect the model's I-V response are a1, a2, b1, and b2. Equation (19) illustrates how a hyperbolic sine curve is used to describe the state variable. According to a number of memristor characterizations, the condition of the device doesn't change until the voltage that is being supplied exceeds some particular threshold [7–12]. This behavior can be modeled using a hyperbolic sinusoid-based state variable. The way the state variable's dynamics threshold and intensity are influenced by the constants c1, c2, d1, and d2.

I (t) = {

$$a_1 \times x(t) \times sinh(b_1 \times V(t)), \qquad V(t) \geq 0$$

$$a_2 \times x(t) \times sinh(b_2 \times V(t)), \qquad V(t) < 0$$

} (19)

dx/dt = {

$$c_1 \times sinh(d_1 \times V(t)), \qquad V(t) \geq 0$$

$$c_2 \times sinh(d_2 \times V(t)), \qquad V(t) < 0$$

} (20)

The device boundaries were defined by integrating the Biolek window function [4] into the updated model. Equation (21), where F {x(t)} is the Biolek window function, shows the updated equation of state variable.

dx/dt = {

$$c_1 \times sinh(d_1 \times V(t)) \times F(x(t)), \qquad V(t) \geq 0$$

$$c_2 \times sinh(d_2 \times V(t)) \times F(x(t)), \qquad V(t) < 0$$

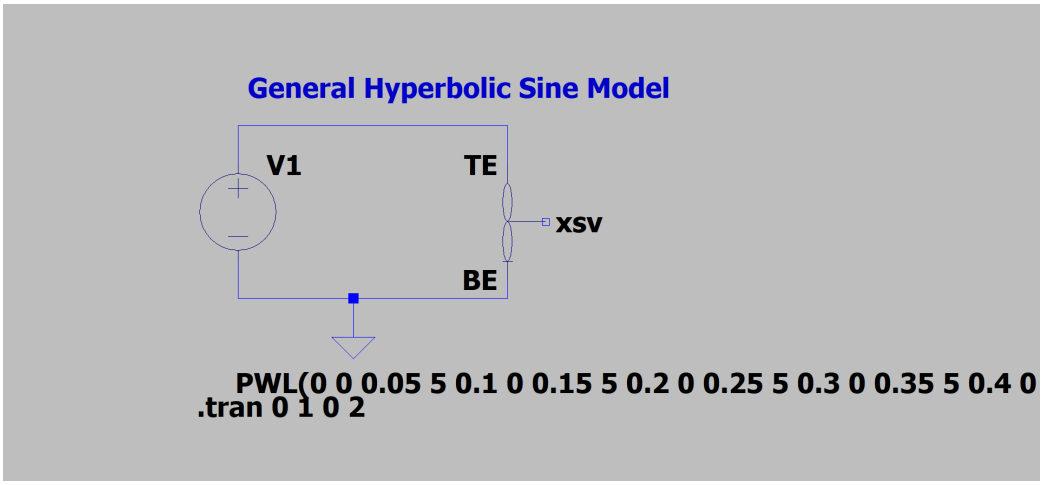
} (21)

5.3 Outcomes of the General Hyperbolic Sine Model Simulation

Reference of the Code for the memristor subcircuit for General Hyperbolic Sine Model is in [7].

Simulation Result:

Input signal: triangular waveform



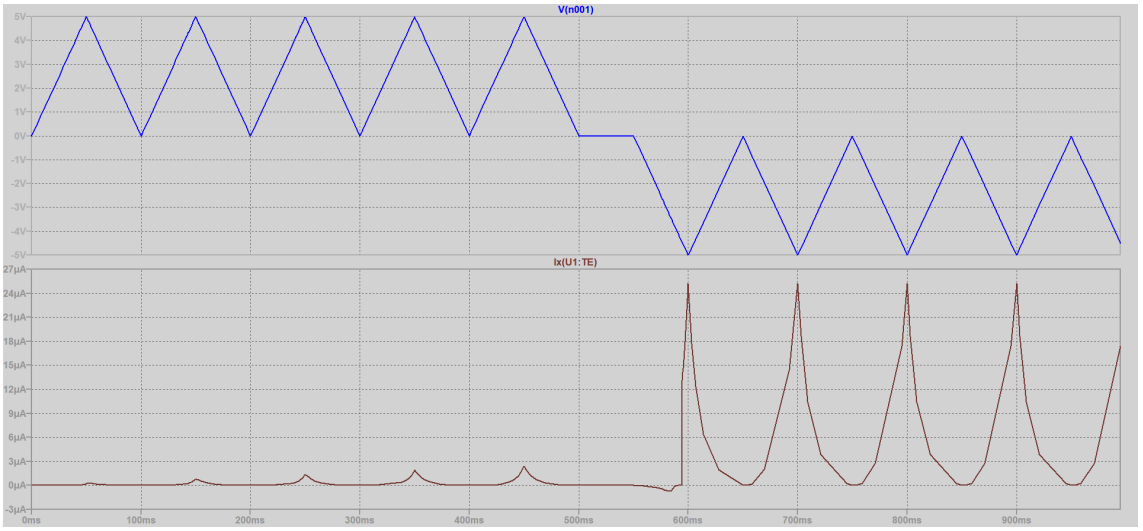


Fig.5.1: Input voltage and current waveform

I-V characteristics:

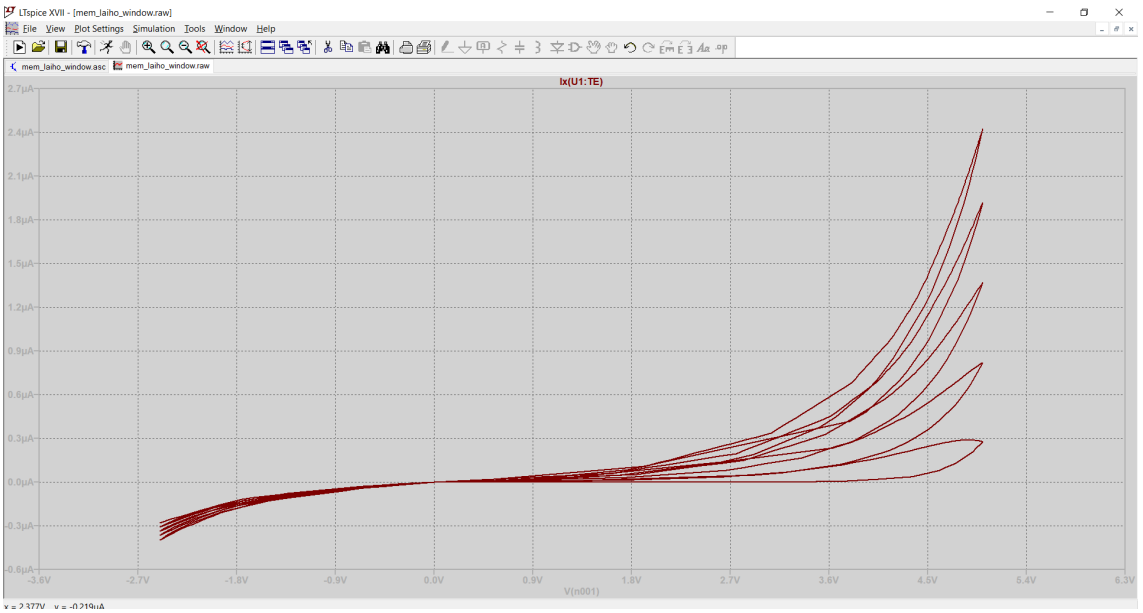


Fig.5.2: Simulation result: I-V characteristics

Until the maximum boundary of the state-variable motion is reached, it is evident that the current flowing grows after every voltage pulse passing through the gadget. At this moment, until the input voltage's polarity is switched, every current pulse has a consistent peak.

5.4 Model of University of Michigan

Ting Chang et al. presented a unique model in [8] that was based on the hyperbolic sine I-V connection. The correlation in between V-I, or I–V, is represented by two terms in

equation (22). Although the second phrase is the consequence of tunneling through the (MIM) junction, Ion migrations that impact With a range of 0 to 1, the state variable x(t) represents the conductive property of the device. Eq. (23), which describes the state variable's dynamics, is quite similar to Eq. (20). The parameters η1, η2, and λ in Eq. (23) are utilized to shape the behavior of the state variable. For each simulation in Figs. 4.4 through 4.6, The following definitions applied to the constants in the equations: α = 5(10^−7), β = 0.5, γ = 4(10^−6), δ = 2, φ = 4.5, η1 = 0.004, η2 = 4, and τ = 10.

$$I(t) = (1 - x(t) \times \alpha \times (1 - e^{\beta \times v(t)}) + x(t) \times \gamma \times sinh(\delta \times v(t))) \quad (22)$$

$$\frac{dx}{dt} = \phi \times [\eta 1 \times sinh(\eta 2 \times V(t))] \quad (23)$$

To account for many colliding loops of hysteresis that occurred during the device's testing with a repeating pulse input. It was stated that ion diffusion inside the device produced the hysteresis overlap. Equation (24) displays the diffusion-component augmented state variable equation.

$$\frac{dx}{dt} = \lambda \times [\eta 1 \times sinh(\eta 2 \times V(t)) - \frac{x(t)}{\tau}] \quad (24)$$

5.5 Simulation Results for University of Michigan Model

The memristor subcircuit code for the University of Michigan Model is detailed in [8].

Simulation Result:

Input signal: triangular wave

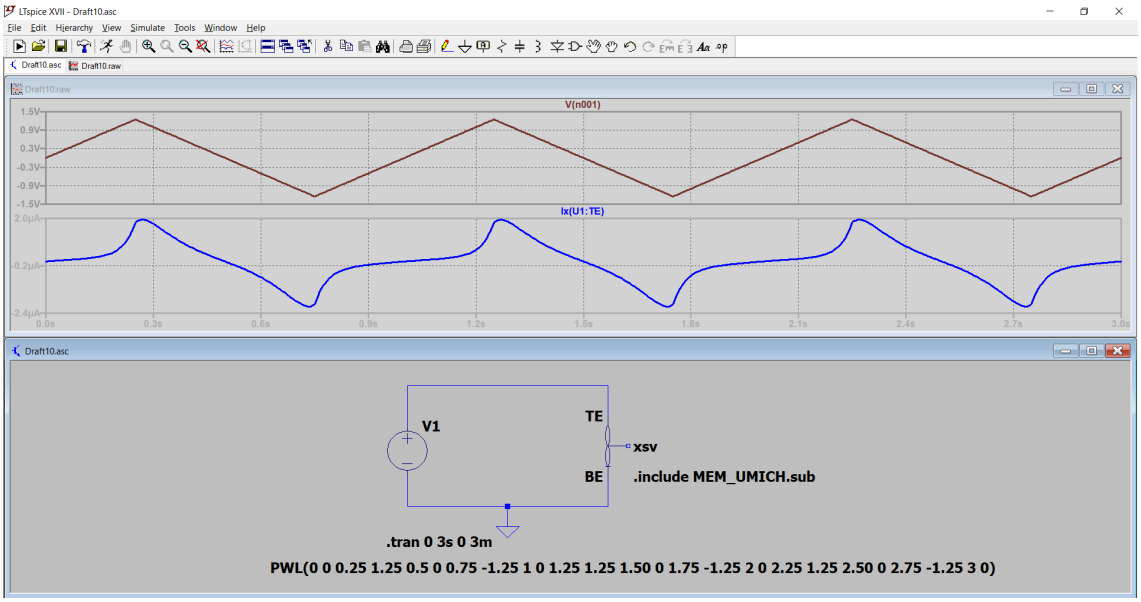


Fig.5.3: Input voltage and current waveform.

I-V characteristics:

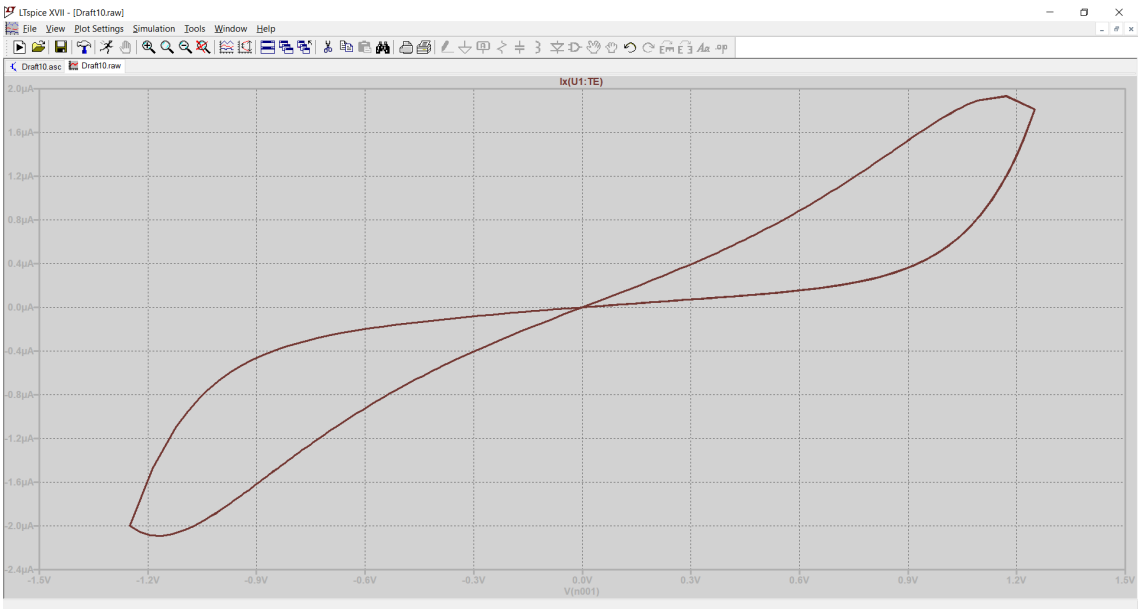


Fig.5.4: Results of simulations using the Chang et al. memristor SPICE model without using the state parameter equation's ion diffusion term.

Input signal: The triangle pulses have rise/fall duration of 0.25 s, a puls duration of 0.5 s, and a magnitude of 1.25 V.

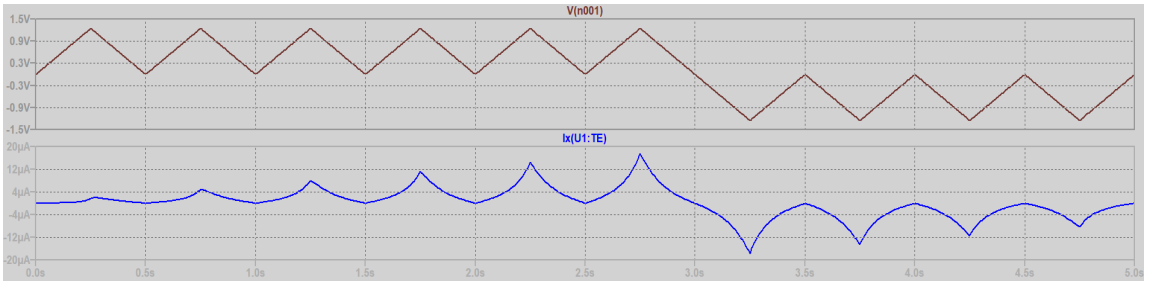


Fig.5.5: Input voltage and current waveform.

I-V characteristics:

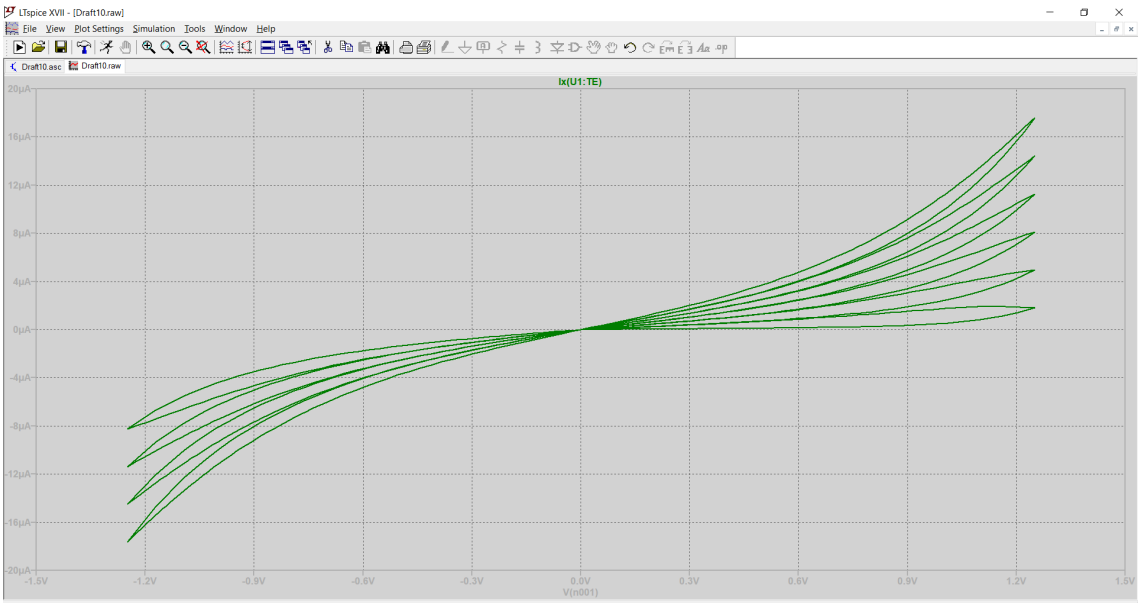


Fig.5.6: Results of simulations using the Chang et al. memristor SPICE model.

When the memristor gadget receives a potential signal with no overall charg(q), the model produces the results shown in Fig. 4.4. This simulation's result is similar to earlier ones using a sinusoidal input, but this time, the hyperbolic sine component in the I-V connection is responsible for a discernible curvature. The model results are shown in Figure 4.6 following the addition of the ion diffusion component to the state variable equation. When negative pulses are applied, a greater gap is seen between the hysteresis loops even though they crossover in the region that is positively biased. A logical explanation for this occurrence is ion diffusion.

Chapter 6

Generalized Model for Many Devices

In [9], a memristor circuit design was created that could faithfully replicate the I-V characteristics found in a number of memristor devices that had been described. The equations were created using a broader knowledge of memristor dynamics, and the results were compared to data from physical characterization by use of fitting parameters.

6.1 Equations for the Generalized Memristor Model

The universal I–V interconnection for this memristor architecture is shown in Eq. (25). It was discovered during the construction of this model so a solitary factor b might be employed independently of voltage polarity. Above a specific voltage level, the MIM structure causes the hyperbolic sinusoid shape, which increases the device's conductivity. For different memristor device topologies, Eq. (25) is modified using parameters a1, a2, and b. The orientation of the input voltage determines a different magnitude value is required because the memristor characterisation data currently available indicates better conductivity in the positive zone. The threshold function's intensity, It links the amount of the input voltage to conductance, is controlled by the fitting parameter b. As an example, the apparatus presented in [10] having higher cutoff (b=3) as compare to the apparatus presented in [11] (b=0.7). The current-voltage relationship is additionally influenced by the state variable x(t), which represents resistance variations according to the physical dynamics of each device. This variable, which has a range of 0 to 1, directly influences the conductivity of the device.

I (t) = {

$$a1 \times x(t) \times sinh(b \times V(t)), \qquad V(t) > 0$$
$$a2 \times x(t) \times sinh(b \times V(t)), \qquad V(t) > 0$$

} (25)

Changes to the state variable are determined by two distinct identities: f(x(t)) and g(V(t)). The function g(V(t)) enforces the logic cutoff of the memristor model. This threshold denotes the least amount of energy required to change the the device's structural composition, including the migration of dopants, low mobility ions, or the state transition in a within a semiconductor device. We used equation (26) to include the programming threshold.In contrast to the hyperbolic sinusoid scripting cutoff [15], the method given in Eq. (26) allows for the inclusion of several thresholds based on the input voltage's orientation. It's critical to take into consideration the different threshold values of these devices, which, to better fit the characterization data, differs depending about if the voltage being supplied is positive or negative, the characterization data can be more accurately fitted. It is possible to change the magnitudes of the exponentials (Ap and An) The limits for positive and negative values. The rate at which the state changes once the threshold is reached is determined by the exponential's magnitude. As can be observed in Sect. IV, the chalcogenide device needs to be significantly modified once the threshold is crossed. On the other hand, a substantially smaller amplitude coefficient is needed for the device that tracks the movement of silver dopants [10], suggesting a slower phenomenon.

g(V(t)) = {

$$\begin{cases} A_p(e^{V(t)} - e^{Vp}) & V(t) > V_p \\ -A_n(e^{-V(t)} - e^{Vn}) & V(t) < -V_n \\ 0, & -Vn < V(t) < Vp \end{cases} \quad (26)$$

Equations (27) and (28) show the second function that was utilized to model the state variable f(x(t)).Based on the idea that when the state variable becomes closer to the boundaries, it gets difficult to modify the state of the devices, this function was implemented. Theorized in [3, 4], this concept was experimentally proven in [6]. Additionally, this function offers the option to model the state variable's mobility in several ways based on the input voltage's polarity. The fact that there is no comparison between the state variable mobility in either direction has been empirically confirmed, making this addition required [6].

Switching state variables, in which the motion varies according to the polarity of the current flowing through the device, are also used in the memristor device model that

was published in [6]. This could be explained by the fact that when ions have been displaced, it becomes more difficult to return them to their former positions. Equation (27) describes the state variable motion when ηV(t) > 0, and Equation (28) describes the motion in the other case. The axis of movement of the state variable in relation to the voltage polarity was indicated by the introduction of the character η. When η is equals to 1, a positive voltage (over the threshold) will increase the value of the state variable. while a positive voltage will cause the state variable value to decrease when η=−1. The function f (x(t)) was created assuming that the state variable motion was unchanged through the value of xp or xn, the function f (x(t)) was constructed. The current mobility of the state variable was restricted by an exponential function that decays. Since the state variable's motion seems to vary depending on the kinds of devices examined, this feature fitting parameters were applied to account for the variation. The equation's constants indicate the point (xp and xn) at which the state variable motion becomes constrained, and the rate of decay (αn and αp) of the exponential. These variations could be brought about by the reality that a chalcogenide device's state change motion is substantially different compared to ion or dopant mobility.

$$f(x(t)) = \begin{cases} e^{-\alpha_p \times (x(t) - xp)} \times w_p(x(t), xp) & x(t) \geq xp \\ 1, & x(t) < xp \end{cases} \quad (27)$$

$$f(x(t)) = \begin{cases} e^{-\alpha_n \times (x(t) + xn - 1)} \times w_n(x(t), xp) & x(t) \leq 1 - x_n \\ 1, & x(t) > 1 - x_n \end{cases} \quad (28)$$

A windowing function called wp(x, xp) in Eq. (29), makes sure that f (x) tends to diminish when x(t) = 1. In Eq. (30), once the direction of movement is changed, wn(x, xn) prevents x(t) from falling below 0.

$$w_p(x, x_p) = \left[\frac{x_p - x}{(1 - x_p)}\right] + 1 \quad (29)$$

$$w_n(x, x_n) = \frac{x}{1-x_n} \tag{30}$$

The dynamic state variable's direction of motion is also determined by the amount η.

$$\frac{dx}{dt} = \eta \times g(v(t)) \times f(x(t)) \tag{31}$$

6.2 Generalized Memristor Model Results

[9] Shows the sub circuit code for the Generalized memristor subcircuit

Simulation Result:

Input signal: sinusoidal waveform

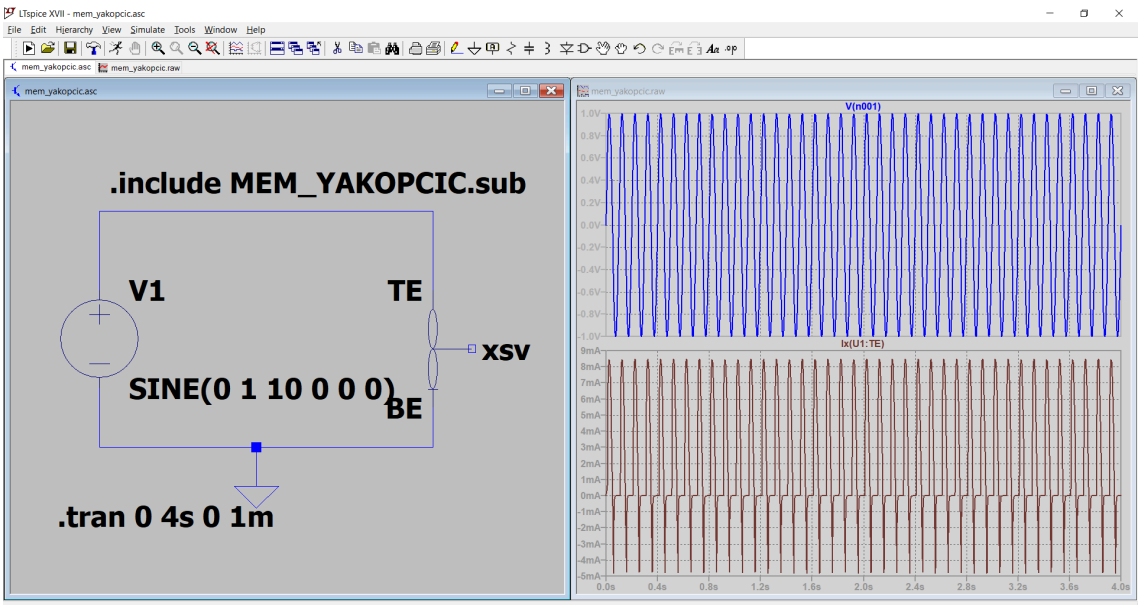


Fig.6.1: Input voltage and current waveform

I-V characteristics:

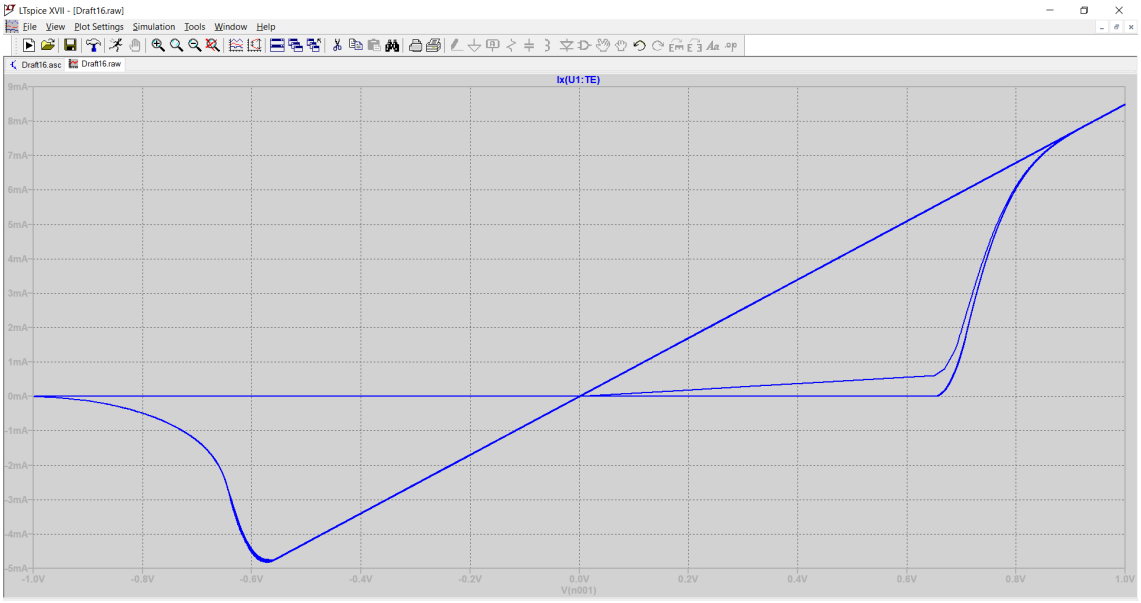


Fig.6.2: Results of an LTspice simulation using a sine-wave input in the YAKOPCIC memristor design

Input signal: triangular waveform

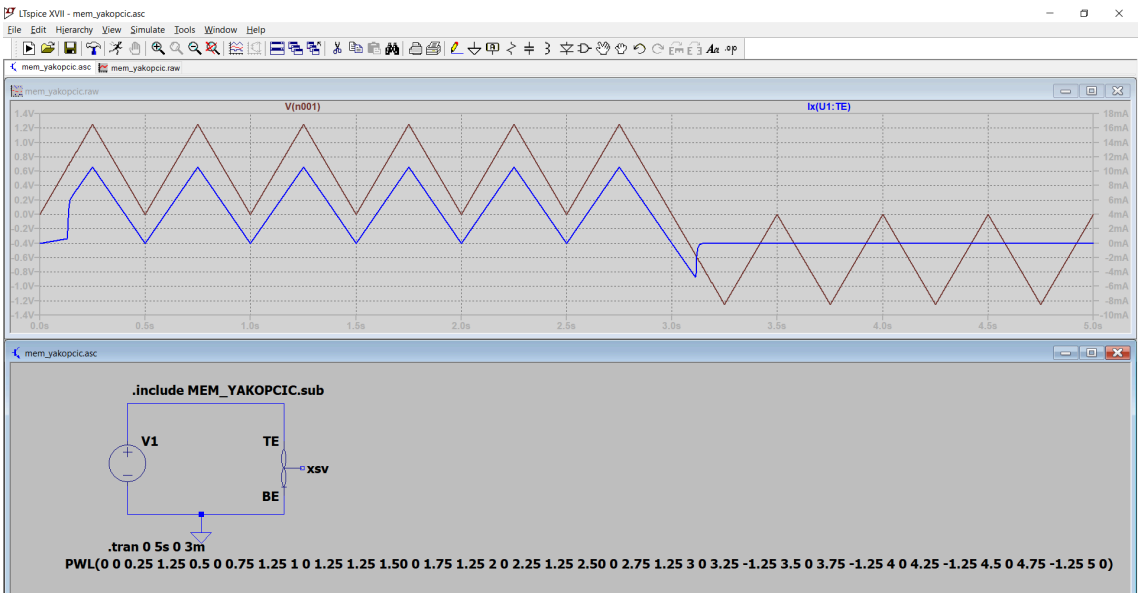


Fig.6.3: Input voltage and current waveform

I-V characteristics:

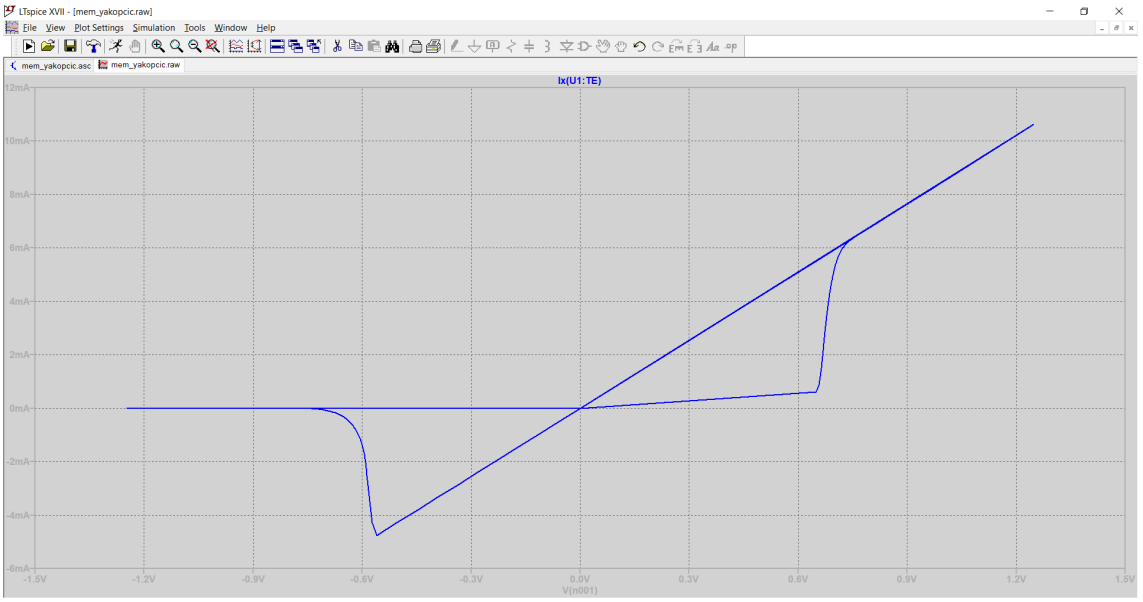


Fig.6.4: Results of the LTspice simulation using a triangle pulse as the input for the YAKOPCIC memristor model.

Chapter 7

Neuronal Spike Generator Using Memristors

7.1 Architecture for Neuromorphic Computing

Neural networks found in biology have an enormous amount of connections. Our study begins with a simple m × n net that has neurons and synapses based on memristors. A m × n number of synapses connects M pre-synaptic nerve cells and n post-synaptic nerve cells, as shown in Fig. 6.1.

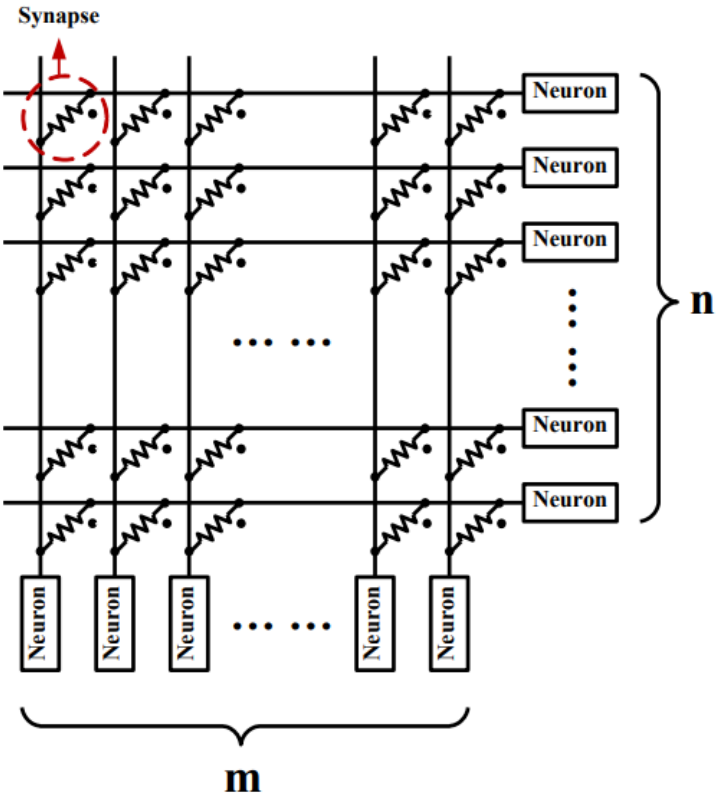


Fig.7.1: The memristor-based neural network's topology [14].

Every neuron is programmed to produce regular spikes that occur at a specific frequency and time once it is triggered. When neural spikes transmit the information to be processed, the differential signal across the synapse constantly modifies the synapse

weight, allowing analog computation at the synapses. Memristors are non-volatile, therefore the results of these calculations are stored at the synapses by nature. With the tiny feature size of typical memristors (~10 nm), this architecture is able to implemented successfully with a memristor crossbar, enabling neural networks with a significant integration density

7.2 Synpases based on Memristors

Ionic flux within a biological structure can accurately control the amount of weight of synapses that connect two neurons. It is thought that this kind of self-adaptation is crucial for memory and learning processes. It has been noted that memristors and transistors have very comparable characteristics in that The electrical energy is temporally integrated across the device directly controls the conductance [3-5].

The lowest and highest conductance of a memristor-based synapse are represented by the HRS and LRS values of the memristor. The behavior of the entire neural network is influenced by the synapse's sensitivity of an external signal, which is controlled by the memristor's switching speed. According to current experimental findings, spike-timing dependent plasticity (STDP), a crucial learning process validated by biological tests, is exhibited by nanoscale memristor-based synapses [9]. The timing of both pre- and post-synaptic pulses corresponds to the modification of synaptic weight. The duration between these pulses determines the extent of synaptic weight adjustment, with shorter intervals resulting in more significant changes.

7.3 Memristor-based Production of Neuronal Spikes

Neurons produce action potentials, or neural spikes, in order to communicate. A well-known model explaining spike formation by means of the effects of sodium and potassium channels on membrane potential was created by Hodgkin and Huxley. Both the potassium and sodium channels could be viewed as voltage-controlled memristive one-ports, which is consistent with Chua and Kang's classification of a membrane potential's function as a memristive mechanism. Taking reference from [14], which describe a neural spike generator using a memristor as shown in fig. 6.1.

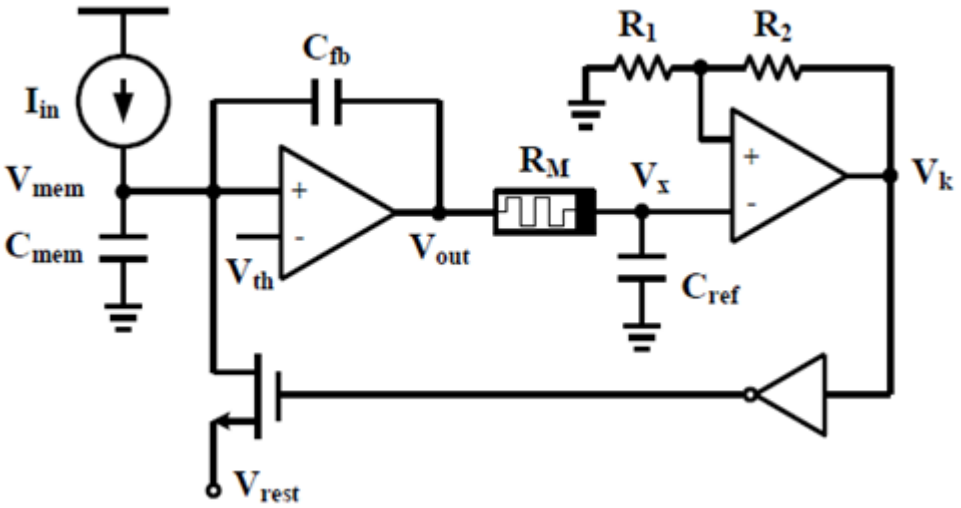


Fig.7.2: Diagram of the neural spike generator based on a memristor [14].

Upon activation of the generator, the membrane voltage Vmem displays transient voltage waveforms resembling spikes. The dynamics of the potassium and sodium channels are modeled by distinct time constants given by RM and Cref As soon as the memristor RM flips in between HRS and LRS. Depending on the notion that refractory as well as integration durations control the complete cycle of the spike event, Iin and Cref typically modify the spike rate.

7.4 Simulation Result

7.4.1 Circuit diagram of carver Mead Neuron

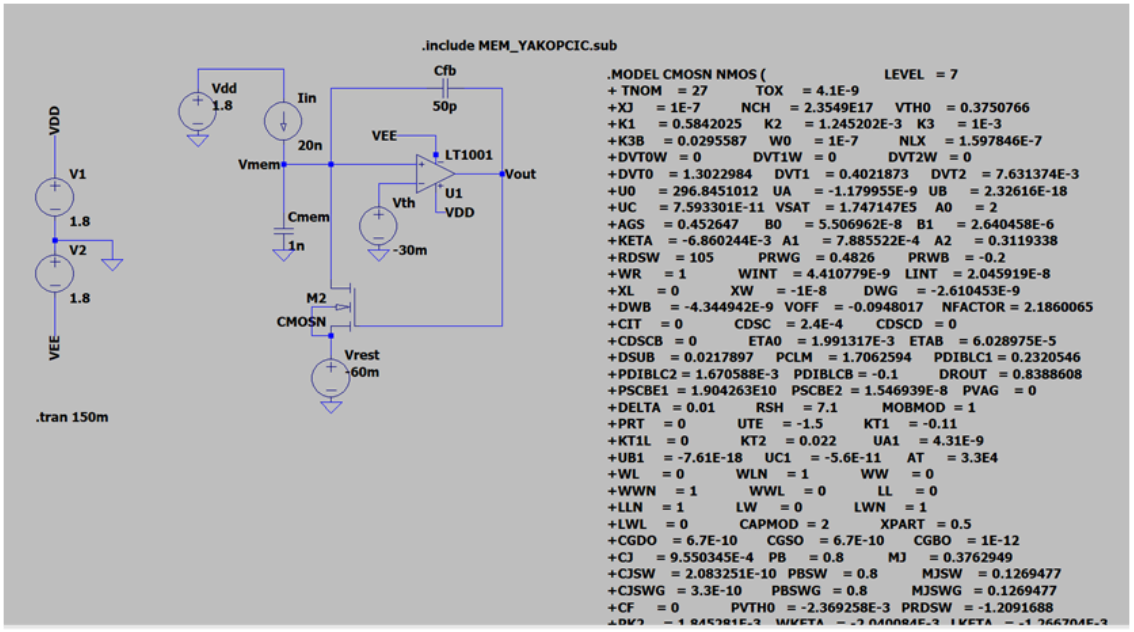


Fig.7.3: circuit diagram for simulating carver Mead Neuron

Output waveform:

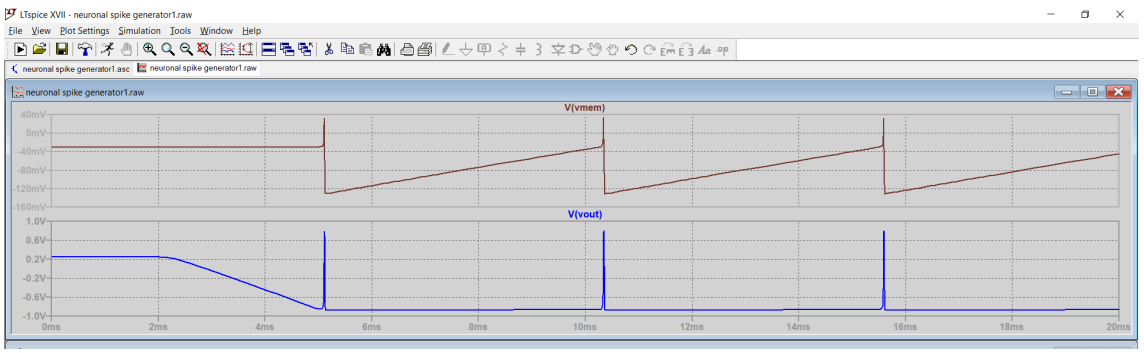


Fig.7.4: simulation result of carver Mead Neuron

7.4.2 Diagram of the neural spike generator with a memristor.

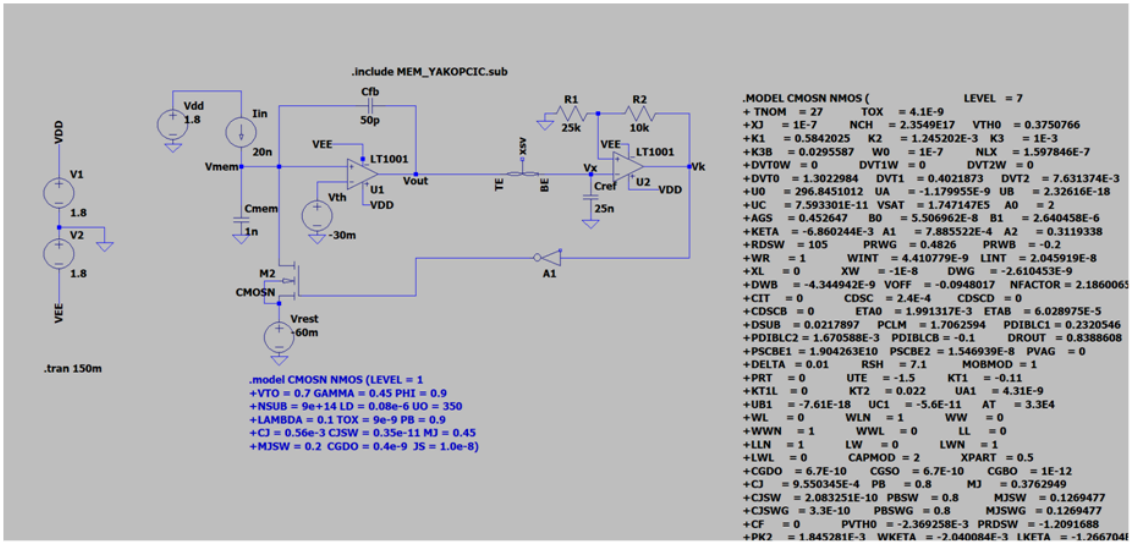


Fig.7.5: circuit of neural spike generator with a memristor.

Output waveform:

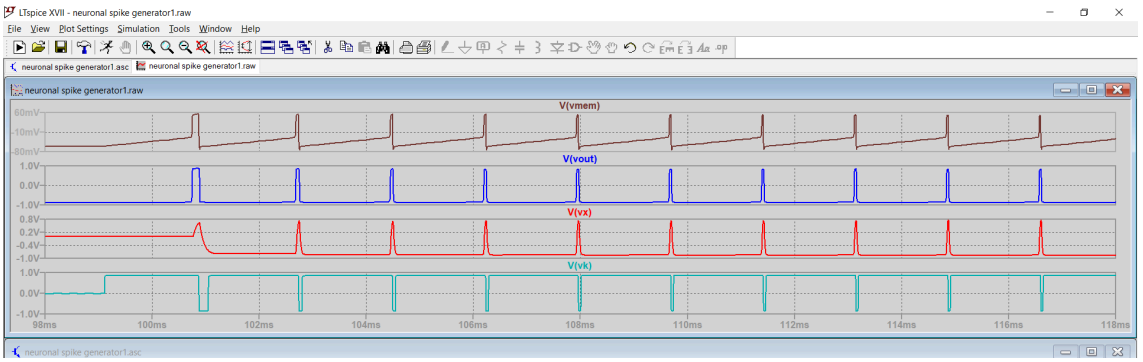


Fig.7.6: simulation result of Neuron spike generator module.

Chapter 8

Conclusion

It is clear from looking over every model that many methods have been suggested to model memristor devices. Every technique was validated either by accurately describing behaviors observed in memristor devices or by agreeing with published characterisation data.

The models presented in chapter 1 are based on a direct correlation between the total device resistance and the ionic drift in the oxide layer. These models offer a straightforward description of memristor activity that is directly related to the hypothesis that was first put forth by Dr. Chua. However, limited information is available regarding their performance with alternative device structures and varied voltage inputs.

A specific memristor device's characterisation data exhibits a very strong correlation with the models in Chapter 2;The usefulness of such models with different device topologies and applied inputs remains uncertain.

The models presented in chapter 3 illustrate a straightforward and effective approach to use Hyperbolic sine curve in the current-voltage connection to simulate the Metal-Insulator-Metal (MIM) junction. These models align with observed memristor behavior, particularly demonstrating effectiveness when subjected to repeated pulsed inputs. However, it's noteworthy that these models have yet to be numerically linked to any fabrication data.

Chapter 4 describes a further generalized SPICE version that can match the current-voltage characteristics of numerous devices. Compared to the University of Michigan or HP Labs MIM models, this model's The mathematical correlation with the actual systems driving the device is lower. The results suggest that the model discussed in chapter 6 provides the most precise description of memristor current-voltage data that has been released. It has demonstrated versatility across various materials and device structures, making it adaptable to the evolving landscape of memristor device fabrication. Given that this model has been shown to properly match characterizations across a variety of memristors, its fitting parameters may be modified to accommodate future fabrication approaches.

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