MODELLING, ANALYSIS AND CONTROL OF TRISTATE DC-DC CONVERTERS FOR LOW POWER CIRCUITS

A PROJECT REPORT

SUBMITTED IN PARTIAL FULFILLMENT OF THE
REQUIREMENTS FOR AWARD OF THE DEGREE OF

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Power Electronics and Systems

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DECLARATION

I, Raunak Karan, Roll No. 2K22/PES/12 student of M. Tech. (Power Electronics and Systems), hereby declare that the project dissertation titled " **MODELLING, ANALYSIS AND CONTROL OF TRISTATE DC-DC CONVERTERS FOR LOW POWER CIRCUITS** " which is submitted by me to the Department of Electrical Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Masters of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

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CERTIFICATE

I hereby certify that the Project Dissertation titled " **MODELLING, ANALYSIS AND CONTROL OF TRISTATE DC-DC CONVERTERS FOR LOW POWER CIRCUITS** " which is submitted by Raunak Karan, Roll No. 2K22/PES/12, Department of Electrical Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Masters of Technology, is a record of the project work carried out by the students under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ABSTRACT

In the realm of DC-DC converters, boost and buck-boost converters serve a significant role. These converters are extensively utilized in various applications due to their proficiency in modulating and transforming voltage levels. Boost converters are commonly employed in photovoltaic systems, electric vehicles, and portable electronic devices to elevate low input voltages to higher levels, ensuring an adequate power supply. Buck-boost converters are essential in battery-powered systems, including laptops and mobile devices, providing both step-up and step-down voltage regulation. Both varieties are crucial for augmenting the efficacy and reliability of power management systems. A significant issue with both boost and buck-boost converters are the presence of the right-hand plane zero, which impacts their stability. The advent of the Tristate converter in boost and buck-boost configurations has mitigated this problem by eradicating the right-hand plane zero, thereby enhancing the stability of both converters. Consequently, the Tristate converter is used to modulate the voltage of the DC grid. This project investigates the performance of the Tristate boost converter with two different types of controllers: PI controllers and Type II compensators. An analogous analysis is conducted using a boost converter. Additionally, the development of the Dual Output Tristate Boost Converter is investigated. This converter features an incorporated output: the main output exhibits the characteristics of a Tristate boost converter, while the auxiliary port produces a buck characteristic. The secondary port is controlled through a buck-boost converter affixed to the auxiliary port's output. A comparative analysis between the buck-boost converter and the Tristate buck-boost converter is presented, concentrating on steady-state output voltage gain and stability conditions illustrated through bode plots and root locus. This comparison emphasizes the superiority of the Tristate buck-boost converter over the standard buck-boost converter. The only disadvantage of the Tristate converter is its steady-state output gain, which is addressed by the high-gain Tristate converter. The chapter on the high-gain Tristate converter details its derivation in buck-boost and boost configurations and portrays its steady-state performance. The report concludes with a segment on future scope, delineating potential advancements for the Tristate converter.

TABLE OF CONTENTS

LIST OF ABBEVIATION

PWM: Pulse width modulation

PID: Proportional Integral Derivation

T3C: Type II compensator

PFM: Pulse Frequency Modulator

PI: Proportional Integral

HVG: High Voltage Gain

ZVS: Zero Voltage Switching

THD: Total Harmonic Distortion

NPC: Neutral point clamping

SPWM: Sinusoidal pulse width modulation

RHP: Right hand pole

TSB: Tristate Boost Converter

TSBB: Tristate Buck Boost Converter

T2C: Type 2 compensator

BBODC: Buck Boost DC Dc converter

BUDC: Buck DC DC converter

IDO: Integrated dual output

SC: Switch Capacitor

DOTSB: Dual Tristate Boost

HGTSB: High gain Tristate Boost

HGT: High Gain Tristate

PM: Phase Margin

PB: Phase boosting

GM: geometric mean

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Chapter 1

INTRODUCTION

1.1 Introduction

DC-DC converters are indispensable in low-powered applications, serving to efficiently modulate voltage levels for optimal device performance. BODC converters play a crucial role in low-powered applications by efficiently increasing voltage levels. The TSB converter meets the requirement of sustaining a consistent voltage profile. This design eliminates the RHP zero present in a standard boost converter. The DOTSB which is provides with two outputs have been developed. Similar things are for BBODC converter and TSBB converter for removing the RHP zero. High gain DC-DC converters are crucial for applications requiring significant voltage step-up, such as renewable energy systems as well as electric vehicles, enhancing efficiency and performance in power management. The HGT converter is also developed to enhance the gain of the Tristate converter.

1.2 Objective of the Project

The objective of the project is to go through detail analysis of BODC and TSB converter. The DOTSB converter which is provides with two outputs have been developed. One of the outputs of the DOTSB gives a boost output and auxiliary port gives a buck output. The comparison of TSBB and the BBODC converter has been presented. The HGT converter is also developed to enhance the gain of the Tristate converter.

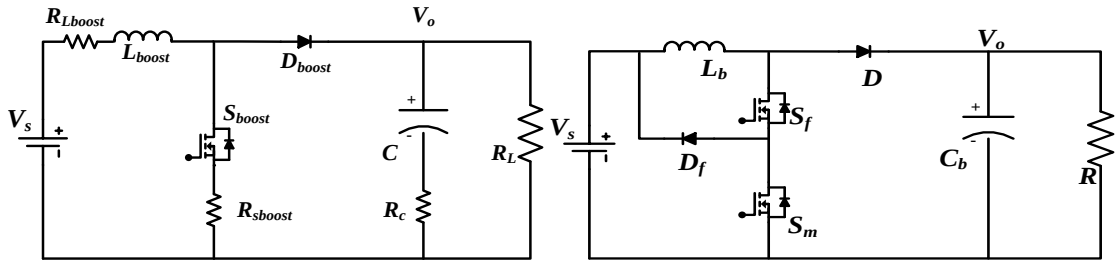


Fig.1(a) Fig.1(b)

Fig.1.1 Circuit diagram of BODC and TSB converter.

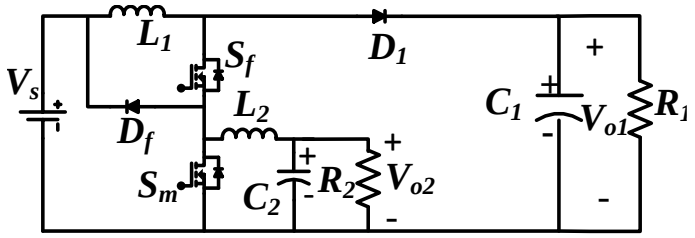


Fig.1.2 Circuit diagram of DOTSB

1.3 Analysis of Boost converter

The modelling of DC-DC converters entails the mathematical representation of their electrical characteristics, aiding analysis, design, and control across various power electronic applications. This process captures the dynamic relationships among input and output voltage, current, and other relevant parameters. Techniques such as state-space modelling, averaged modelling, and small-signal modelling are employed to accurately characterize converter behaviour. The BODC converter, designed to increase output voltage from a reduced input voltage, is widely used in renewable energy systems, electric vehicles, and portable electronics, facilitating efficient voltage enhancement.

1.4 Analysis of Tristate boost converter.

This section tackles the necessity for a stable and consistent voltage profile in practical applications. The TSB converter satisfies this requirement by preserving a constant voltage profile. This topology eliminates the RHP zero commonly encountered in standard boost converters. In the time domain, there is a presence of the RHP zero results which results in a sudden decrease in output voltage and thereby increasing the load current and the duty ratio, consequently extending the discharge time of the output capacitor. It leads to a sudden drop in the load voltage till the inductor current holds the position to recharge the capacitor.

1.5 Analysis of Dual output Tristate Boost converter.

The 48-V DC link ensures consistent voltage levels within the microgrid, which is crucial for the reliable and continuous operation of connected components and equipment. TSB converter fulfils the need for a stable voltage profile by eradicating the RHP zero characteristic prevalent in standard BODC converters. The non-isolated DC-DC Single Input Dual Output architecture was devised to provide both step-up and step-down outputs from a single DC input. Additional outputs can be generated using a low-pass filter network. Notably, the attained step-up and step-down outputs are comparable to those obtained by individual BODC and BUDC converters,

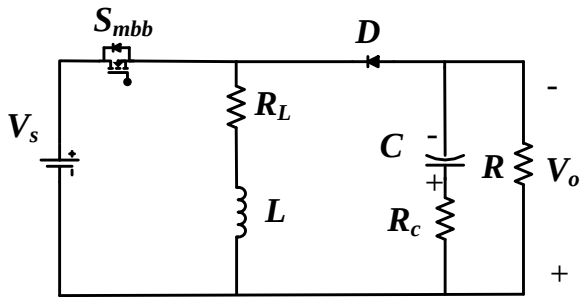


Fig. 3(a)

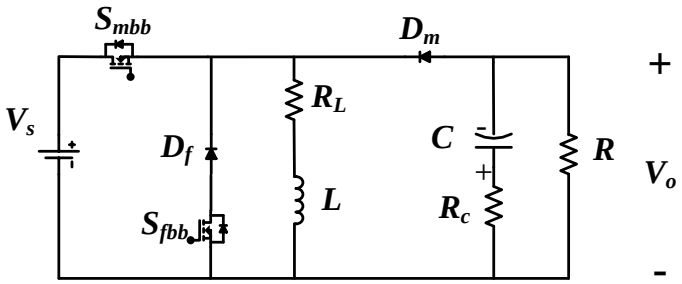


Fig. 3(b)

Fig.1.3 Circuit diagram of a) BBODC and b) TSBB converter.

1.6 Analysis of Tristate Buck Boost converter.

The conventional BBODC converter encounters a non-minimum phase anomaly deriving from the presence of a RHP zero in its control-to-output transfer function during Continuous Conduction Mode operation. This RHP zero detrimentally influences the converter's efficacy. Systems exhibiting an RHP zero can be identified by the starting of an undershoot in the output voltage response to a step input voltage. Conversely, the Tri-state converter integrates an additional mode of operation, specifically the inductor freewheeling mode in Continuous conduction mode, which eliminates the RHP zero from the control-to-output transfer function of the switching converter. Consequently, the Tri-state converter overcomes the non-minimum phase issue, thereby enhancing the closed-loop dynamic performance of the converter.

1.7 High Gain Tristate Converter

The conventional BBODC and BODC converters manifest a non-minimum phase phenomenon owing to the presence of a RHP zero during Continuous Conduction Mode operation. The influence arising from the RHP zero in these converters can be delineated as follows: an initial decrease (undershoot) in the output voltage stimulates the control system

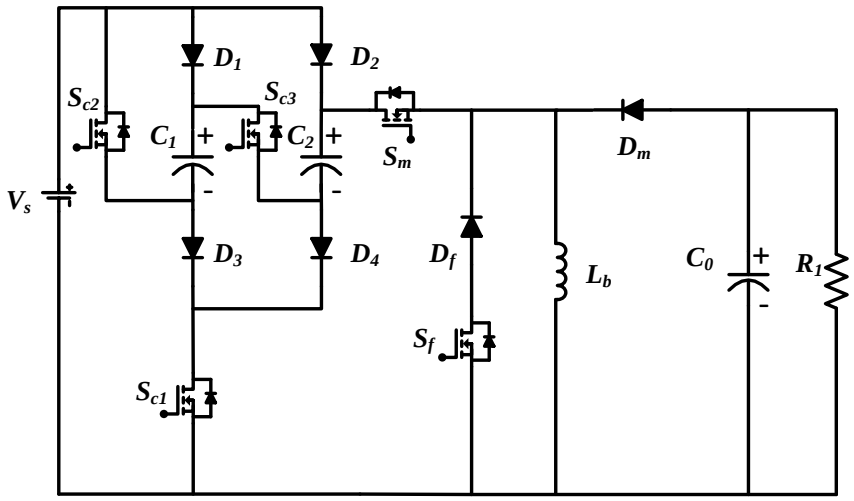


Fig. 1.4(a)

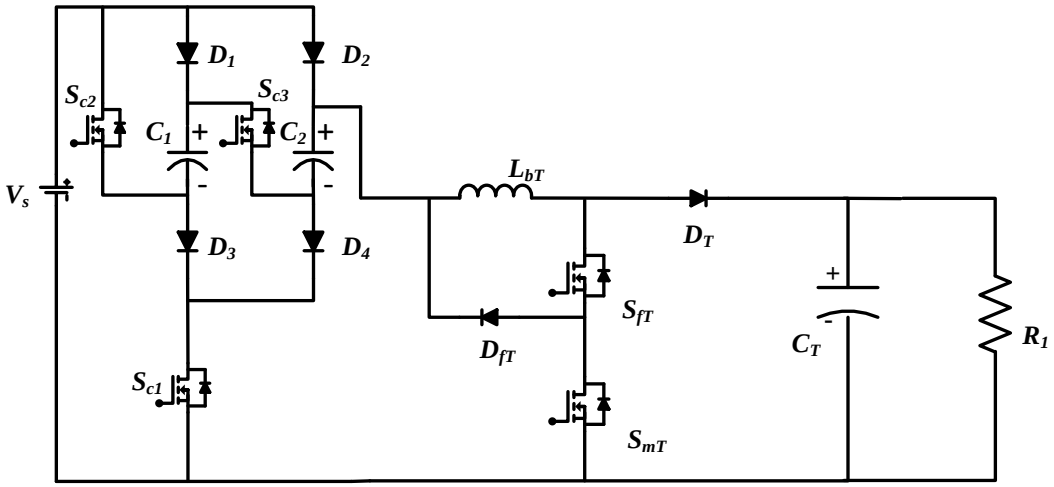


Fig. 1.4(b)

Fig.1.4 Circuit diagram of a) HGTSBB and b) HGTSB converter.

to initiate an increase in the duty cycle ratio. Employing a cascade of two BBODC or BODC converters results in a reduced aggregate efficiency, equivalent to the product of each individual converter's efficiencies. Consequently, this approach is regarded inappropriate for augmenting converter gain. This chapter advocates the incorporation of a SC circuit into both TSB and TSBB converters. While a SC converter can provide versatile voltage ratios dependent upon the number of capacitors in its configuration, its efficacy endures a significant decline when tasked with maintaining a constant output voltage.

1.8. Outline

Fig. 1.5 portrays the outline of the project. The introduction of the project introduces each and every part of the project. The chapter related to the literature review of the study materials related to basic converter and the tristate converter have been depicted in this part. The chapter related to BODC converter explains derivation of controlling of the BODC through PI controller and Type 2 compensator. The results of the BODC in this chapter

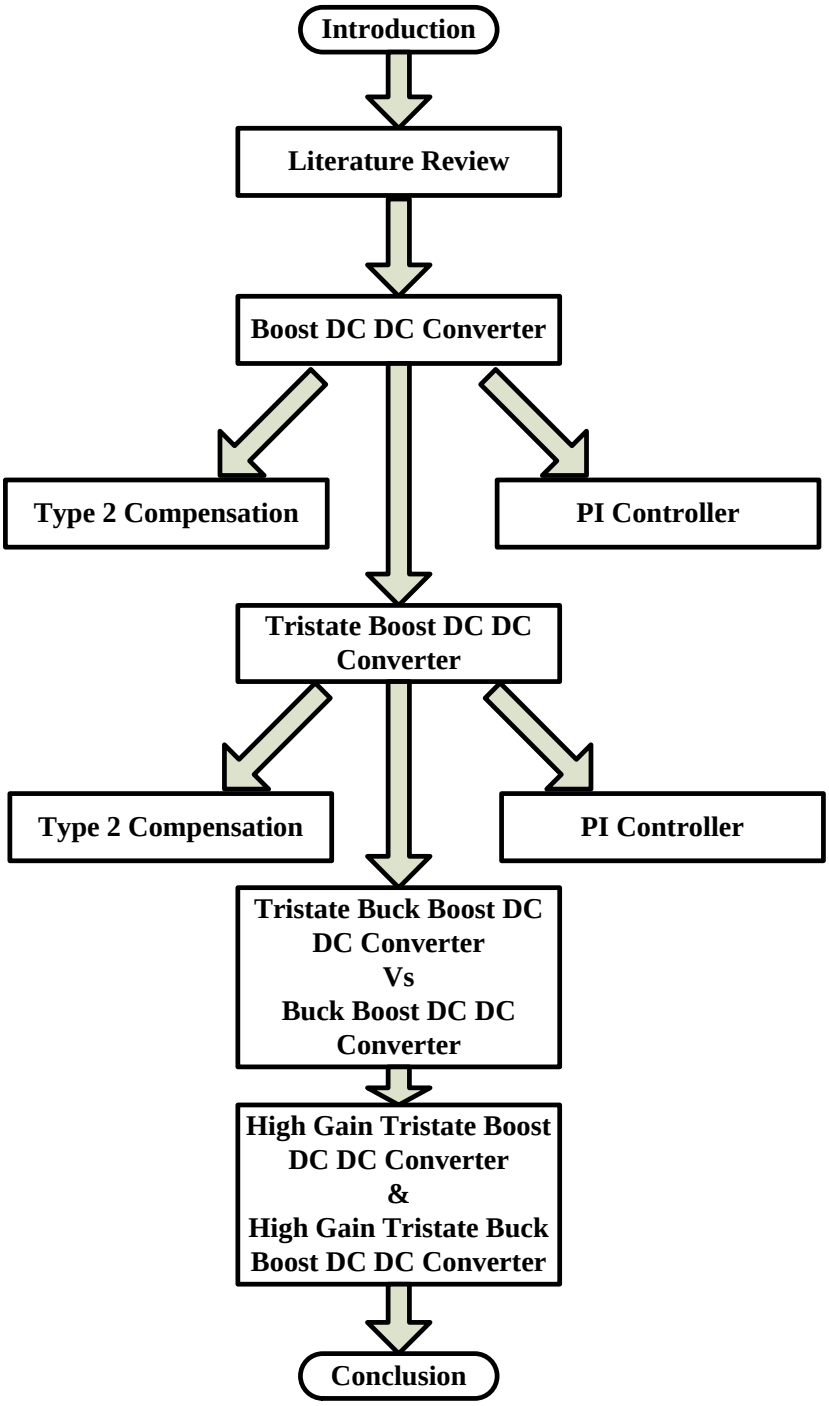


Fig.1.5. Outline of the project

proves that how good the feedback system accompanied to the BODC converter. Similar things are done with TSB converter. The dual loop concept is also accompanied with TSB converter. The chapter related to the comparison of BBUDC and TSBB converter explains every concept that the BBUDC converter is different from TSBB converter. The stability analysis of both TSBB converter and BBUDC are portrayed through this chapter. The hopes of getting a higher gain in Tristate converter is resolve through the chapter related to HGT converter.

1.9. Conclusion

This section introduces every part of the project with its application. This shows the major highlights of the chapter and how they are developed. The way Tristate converter is more effective when it comes to the basic DC DC converter available. It shows the evolution of TSB to DOTSB converter and the then to HGTSB converter.

Chapter 2

LITERATURE REVIEW

2.1 Introduction

The section sums up each and every publication which had paved the path to development of the BODC converter to TSB converter and then DOTSB converter. The comparsion between the TSBB converter with the buck boost converter is also developed which is displayed over here. The way how the high gain Tristate converter has been derived is display in this portion.

2.2 Literature of Boost converter.

The paper [1] examines conventional control techniques for hard-switched DC-DC converters, concentrating on PWM and small-signal analysis. It investigates the impact of increasing switching frequencies and advances in digital signal processing, which facilitate higher operating bandwidths and enhanced performance. The paper defines performance limits of traditional small-signal designs and examines geometric control methods and alternative state feedback implementations. It emphasizes opportunities for large-signal control tuning and compares various tuning strategies, illustrating how geometric controls

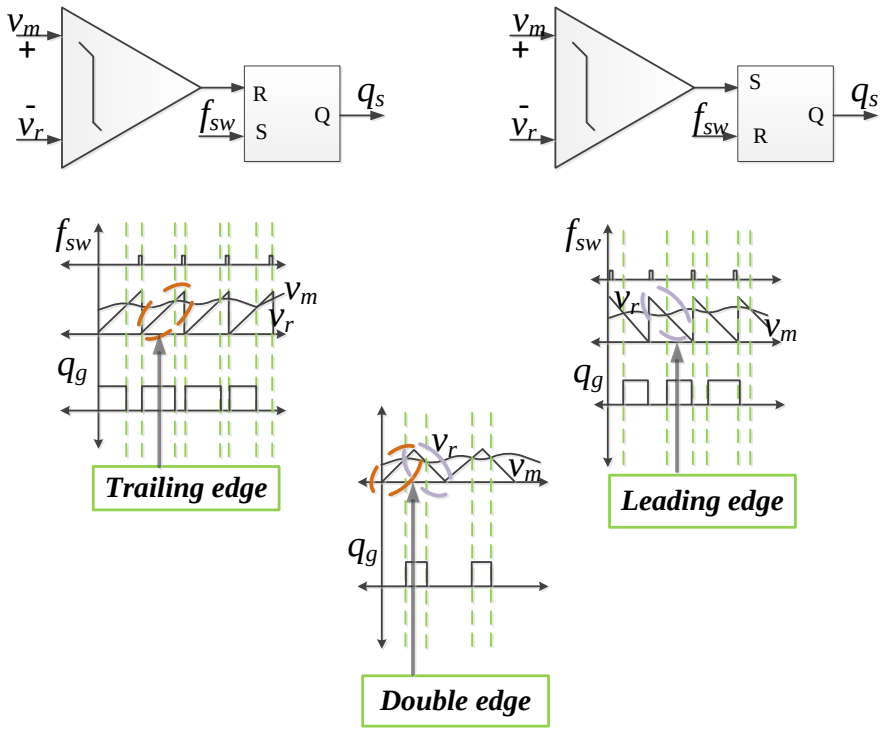


Fig.2.1 Three different types of PWM carrier

can substantially enhance dynamic performance. This has contributed to realize the converter with the use of digital control system. Fig.2.1 illustrates three different types of PWM carrier and describes the functionally of the different types of PWM techniques.

Closed-loop control is a fundamental concept in power electronics converters, essential for sustaining desirable performance metrics such as voltage regulation, current limiting, and overall system stability. In a closed-loop control system, the output is continuously monitored and transmitted back to the input through a controller that modifies the operating parameters to maintain the intended output despite variations in load and input conditions. This feedback mechanism is crucial for addressing disturbances and non-linearities inherent in power electronic systems.

The essence of closed-loop control in power converters often entails using PID controllers [2-3], which provide a robust method for obtaining precise control by modifying the duty cycle of the switching elements. Advanced control strategies, such as T3C [4], are also employed to enhance performance, particularly in systems with rapid dynamic requirements or varying operating conditions.

The implementation of closed-loop control can substantially increase the efficacy and reliability of power electronic converters. It enables precise control over transient responses, reduces steady-state error, and enhances the overall robustness of the system. Furthermore, the incorporation of digital control techniques and rapid processors has allowed for more complex algorithms and real-time adjustments, paving the way for innovations in energy management and smart grid applications.

Studies and advancements in closed-loop control methodologies continue to play a critical role in maximizing the performance of power electronic systems, ensuring they satisfy the stringent demands of modern electrical and electronic applications.

Current loop control [5] in power electronics converters is pivotal for attaining precise current regulation, enhancing dynamic response, and ensuring system stability. This control method entails an inner current loop that provides rapid response to current changes, effectively mitigating disturbances and protecting against overcurrent conditions. By applying methods such as hysteresis control or PI control, current loop control optimizes the converter's performance by maintaining appropriate current levels despite changes in load or input voltage. This approach is crucial in applications requiring stringent current control, such as motor circuits, renewable energy systems, and battery management systems.

These papers [6] analyses the output impedances of PWM DC-DC converters, which influence the dynamic interaction between converters and their load subsystems. It presents

analytical expressions for the output impedances of three fundamental PWM DC-DC converters under current mode control, supported by prototype measurements. Practical application examples, including current-mode controlled buck and boost converters with practical loads, demonstrate the utility of these results. These papers [7-9] proposes a modified small signal state-space average model to analyze pulse-width modulated converters that function in discontinuous conduction mode. Bode plots of the transfer functions have been produced using MATLAB toolboxes. To verify the proposed model, a simulation is conducted in MATLAB, and the frequency response is recorded in real-time using the linearization technique.

To extend battery life in portable devices, sustaining high efficiency in DC-DC converters over a wide discharge current range is essential. This necessitates a multi-mode controller employing PWM and PFM. Existing methods struggle with seamless transitions due to structurally distinct controllers. The paper proposes a unified digital PWM/PFM scheme utilizing a shared digital PWM block, permitting online controller configuration and automatic frequency adaptation. The scheme assures efficient operation and seamless transitions across varying conditions. A unified discrete-time framework is also introduced for analyzing and designing the controller, with successful implementation and testing on buck and boost converter prototypes using an FPGA.[10]

These papers [11-12] introduce a bidirectional buck-boost converter for connecting energy storage systems to a DC microgrid, enhancing the utilization of renewable energy sources. Efficient control of energy storage and associated converters is necessary. Two operating modes are considered: current control mode for efficient charging/discharging of storage, and voltage control mode for sustaining microgrid transit voltage. An averaged model was derived for controller design, employing a cascaded control loop with parameters selected via the root locus method. Traditional AC microgrids face challenges such as reactive power mismatch, synchronization issues, and harmonic effects, impacting reliability, power quality, and the demand-supply divide, while also introducing conversion losses. DC microgrids mitigate these issues by employing several DC-DC converters connected in parallel to a DC link or transit. This investigation analyses two high-power DC-DC boost converters connected to a 400V DC bus, operating as controlled current sources instead of traditional voltage sources used in droop control schemes.

In contrast with standard power infrastructures, DC microgrids strengthen the integration of distributed and renewable energy sources while minimizing energy consumption, so they're highly applicable in various real-life scenarios. High-gain DC-DC converters are essential for enhancing the voltages of low-voltage DC power sources, such as photovoltaic panels and small wind turbines. The paper [13] outlines the principles, voltage gain formulas, and component requirements for classical boost converters, Double-Duty-Triple-Mode converters, as well as quadratic voltage gain converters. It contrasts and analyses these parameters, examines their advantages and disadvantages, and presents conclusions based on the findings.

The paper [14] presents a novel, transformer-less DC-DC Converter meant for HVG applications. The proposed converter integrates an active switched inductor to accomplish HVG while minimizing voltage and current stress across components. With a voltage gain of (3D+1) times that of standard boost converters, the proposed topology offers fewer components and supports bidirectional operation with broad duty ratio variations. Additionally, it guarantees equal voltage stress across all switches and intermediate capacitors, thereby offering an efficient solution for HVG requirements.

The paper [15] offers a novel configuration for a high-gain, high-efficiency DC-DC converter tailored for low voltage solar PV module applications. Fig 2.2 demonstrates the system The proposed design incorporates a single switch, two intermediate capacitors, and a coupled inductor. High voltage gain is obtained by parallel charge and series discharging of the intermediate capacitors through the coupled inductor. A passive lossless clamped circuit is incorporated to recover leakage energy, reduce voltage surges, and enhance efficiency. Maximum power point monitoring is implemented to optimize performance across various irradiation levels. Similar concept has been illustrated in [16].

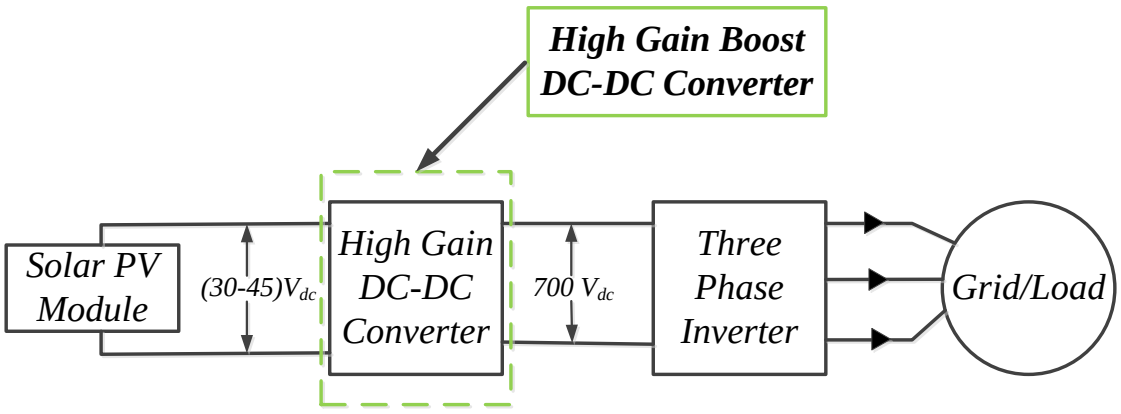


Fig 2.2. Application of High Gain DC DC Converter.

The papers [17-18] introduces a novel soft-switched high-gain coupled-inductor boost converter operating within a permissible spectrum of duty ratios. All semiconductor switches in the proposed converter transition states under soft-switched conditions, while diodes undergo soft commutation.

The paper [19] offers a ZVS technique for soft switching in boost DC-DC converters, deploying an auxiliary circuit configuration featuring an auxiliary diode, inductor, and switch. This configuration ensures ZVS conditions for the main switch, minimizing inductor current ripple and reducing switching losses. Additionally, the auxiliary circuit retains energy in the inductor, transferring it to the load through the diode. A soft-switching ZVS boost DC-DC converter is applied in vehicle-to-grid systems for enhanced operational efficiency.

The paper [20] recommends a simple lossless passive snubber cell for boost converters to mitigate switched-off power losses in the primary power MOSFET ZVS operations. The snubber circuit efficiently addresses reverse recovery issues in the boost diode, switching transients, and stressors across the main switch, offering potential for energy recovery or lossless operations. This approach enhances the efficacy of DC-DC surge power converters. Similar concept has been illustrated in [21].

The grid connected system with the concept are all portrayed through the papers [22-23].

The paper [24] emphasizes the substantial reduction of harmonics, measured by THD, across the output side of NPC five-level inverters with a single-stage LC filter. This configuration plays a crucial role in maintaining power quality in distribution systems. Flexible SPWM control is employed to operate power switches, effectively mitigating asymmetrical harmonics with lower-rated semiconductors. Performance evaluation, modelling, and analysis concentrate on minimizing switching power losses, making it applicable for medium-power applications.

2.3 Literature of Tristate Boost DC DC converter.

The papers [25-26] investigate leading-edge modulation, where the PWM signal becomes active when the error signal crosses the ramp waveform, and deactivated at the clock signal. These conditions include using leading-edge modulation, averting averaging of capacitor voltage switching ripple in feedback compensation, along with the selecting appropriate power stage’s values

The papers [27-28] address a challenging aspect of boost converter design in continuous-conduction mode: the presence of a dynamically altering RHP zero in the control-to-output transfer function. It introduces a novel TSB converter devoid of this zero, accomplished

through an additional freewheeling interval and simple control technique. Eliminating the RHP zero enhances closed-loop bandwidth, facilitating quicker response times in the control scheme.

Compensators serve a crucial role in sustaining accurate converter dynamics in DC-DC power supplies. Certain DC-DC power supplies, including BODC and BBODC converters, exhibit a RHP zero, posing a non-minimum phase challenge that complicates effective PID controller performance. To remedy this, a T2C is implemented for enhanced performance. The paper [29] outlines the design of a T2C for a DC-DC step-up power supply.

The steady-state behaviour of a converter is determined by its topology, while the controller plays a crucial role in maintaining accurate transient and dynamic performance. DC-DC power supplies, such as boost converters, exhibit a RHP negative in their small-signal control-to-output transfer function when operating in continuous conduction mode, complicating effective PID controller performance. To resolve this, a T3C is incorporated for enhanced efficacy. The tri-state boost converter integrates an additional degree of freedom through a freewheeling interval, eradicating the RHP zero and facilitating larger

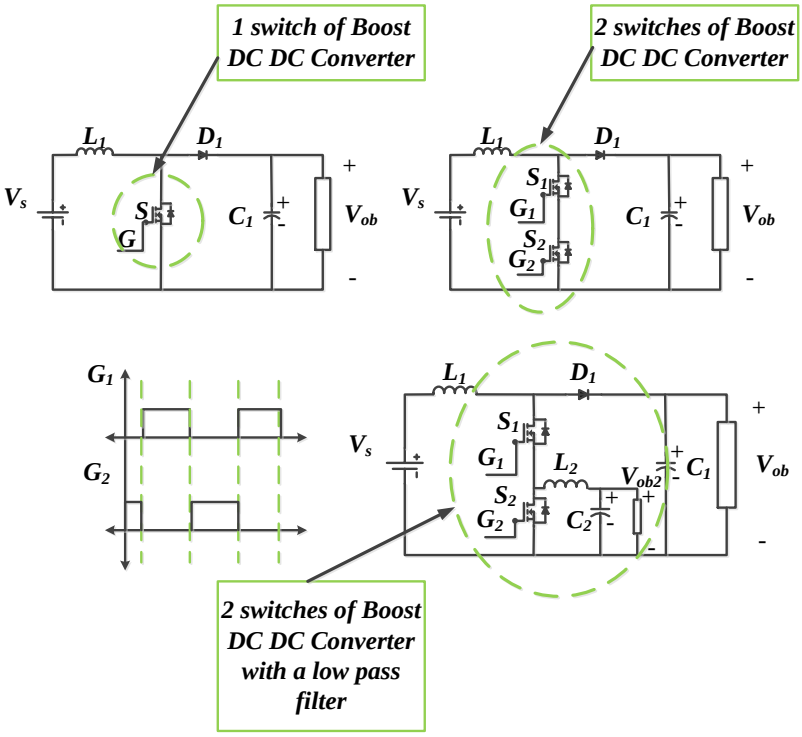


Fig. 2.3 Evolution of IDO Converter

bandwidth under closed-loop conditions, resulting in a speedier response. This offers the combination of T3C with TSB converter.[30]

The development of TSB converter with T2C have been created through these papers.

2.4 Literature of Dual output Tristate Boost converter.

The knowledge of an active load by using a voltage controlled active load is absorbed from the paper [31].

Many topologies are synthesized by substituting the control switch of a boost converter with series-connected switches, using additional switch nodes to generate step-down DC outputs. Compared to distinct converters, these topologies use fewer switches and offer implicit shoot-through protection, enhancing reliability. Analysis demonstrates these topologies exhibit similar dynamic behaviour to individual BUDC and BODC converters, permitting the same control system methodology for precise output regulation. This paper illustrates these concepts using an IDO converter with both step-up and step-down outputs.[32]

2.5 Literature of High gain Tristate converter.

The paper proposes an abrupt step-up of the line voltage by integrating a SC circuit within a boost converter. The SC circuit accomplishes any voltage ratio, significantly enhancing input voltage while remaining unregulated for high efficiency. The boost stage provides regulation along with operates at a low duty cycle, avoiding diode-reverse recovery issues. Unlike cascade interconnections, this integrated approach offers simplicity, robustness, higher voltage ratios without transformers, and enhanced overall efficiency.[33]

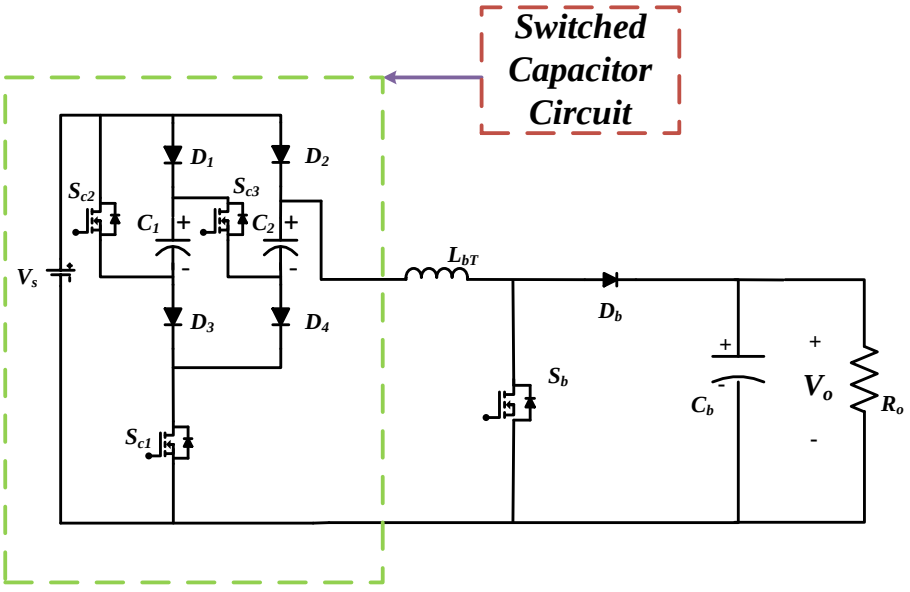


Fig. 2.4 BODC converter with SC circuit

The paper describes the design along with the evaluation of a low-profile, multistage, current-controlled SC step-down DC/DC converter. This converter retains the advantages of classical SC converters while offering enhanced regulation capability and a continuous input

current waveform, resulting in low conducted electromagnetic interference with the supply network. Energy transmission is obtained by paralleling the input and output of two step-down converter cells operating in antiphase. The voltage conversion ratio is controlled by manipulating the charging trajectories of the capacitors in each cell. [34]

The development of HGT converter have been created through these papers.

2.6 Literature of Tristate Buck Boost converter.

The paper [35-36] discusses the design and development of a TSBB converter with an optimized T3C. Standard BBODC converters exhibit a RHP zero in their control-to-output transfer function, compounding controller design for continuous conduction mode operation and deteriorating converter performance. The proposed TSBB converter eliminates the RHP zero, enhancing performance. A T3C is devised and implemented in closed-loop control to enhance transient and steady-state performance.

2.7 Conclusion.

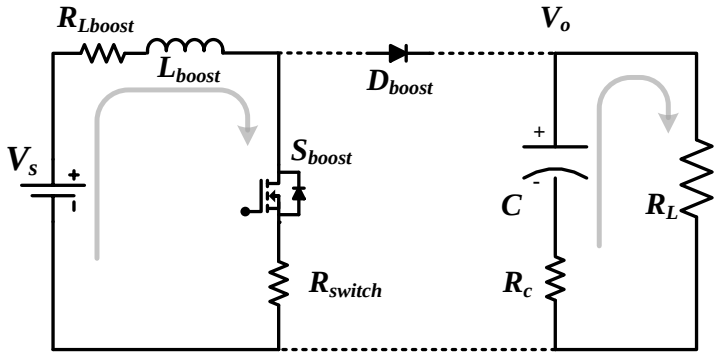
This chapter pronounces the contribution of the papers in the project. The development of the two topologies DOTSB converter and HGTSB converter are expressed in the portion of the literature survey of it are mentioned in these portions. The chapter of the comparison between TSB converter and BBODC converter have taken helped for deriving the steady state equations and the transfer function, from the literature survey.

Chapter 3

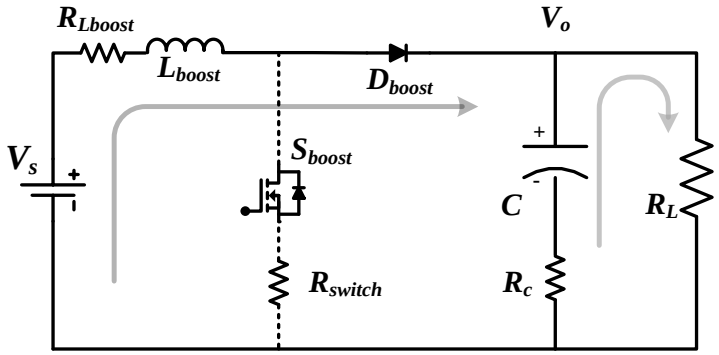
MODELLING AND ANALYSIS OF BOOST CONVERTER

3.1 Introduction

The modelling of DC-DC converters incorporates the mathematical depiction of their electrical characteristics, thereby facilitating the analysis, design, and control within a multiplicity of power electronic applications. This procedural endeavour entails encapsulating the dynamic correlations among input and output voltage, current, and other relevant parameters. Precise models play a pivotal role in forecasting converter performance, efficiency, and stability across disparate operational scenarios. Techniques such as state-space modelling, averaged modelling, and small-signal modelling are utilized to characterize converter behaviour with precision and accuracy. The BODC converter is a power electronic equipment engineered to elevate output voltage levels from a reduced input voltage. Its utility extends to renewable energy systems, electric vehicles, as well as portable electronics, aiding effective voltage enhancement.



(a)



(b)

Fig.3.1 (a)Schematic during Charging interval (b)Schematic during Discharging interval

3.2 Modelling of non ideal Boost converter

The BODC functions under two discernible steady-state circumstances. The initial state arises during the conduction mode of switch S_{boost}, wherein inductor L_{boost} actively charges, as depicted in Figure 1 (a). The subsequent state emerges during the non-conduction mode, where inductor L_{boost} discharges, as illustrated in Figure 3.1 (b).

While the switch S_{boost} is functioning in the conducting state, the inductor voltage is established as

$$V_s = i_{Lboost}(R_{switch} + R_{Lboost}) + L_{boost}\frac{di_{Lboost}}{dt} \tag{3.1}$$

where i_{Lboost} & R_{Lboost} represents the inductor current and inductor resistance respectively of BODC. V_s is input voltage.

$$L_{boost}\frac{di_{Lboost}}{dt} = V_s - i_{Lboost}(R_{switch} + R_{Lboost}) \tag{3.2}$$

where R_{switch} is internal resistance of switch.

The current which tends to pass through the capacitor is provided by

$$i_c = -i_o = -\frac{V_o}{R_L} \tag{3.3}$$

$$c\frac{dV_c}{dt} = -\frac{V_o}{R_L} \tag{3.4}$$

where R_L is load resistance.

While the switch S_{boost} is functioning under the non-conducting state, the inductor voltage is established as

$$V_s = i_{Lboost}R_{Lboost} + L_{boost}\frac{di_{Lboost}}{dt} + V_D + V_o \tag{3.5}$$

$$L_{boost}\frac{di_{Lboost}}{dt} = V_s - i_{Lboost}R_{Lboost} - V_D - V_o \tag{3.6}$$

The current which tends to pass through the capacitor is depicted as

$$i_{Lboost} = i_c + i_o \tag{3.7}$$

$$i_{Lboost} = c\frac{dV_c}{dt} + \frac{V_o}{R_L} \tag{3.8}$$

$$c\frac{dV_c}{dt} = i_{Lboost} - \frac{V_o}{R_L} \tag{3.9}$$

The steady state value of the output voltage equation is established as

$$V_s = i_{Lboost}R_{Lboost} + L_{boost}\frac{di_{Lboost}}{dt} + V_D + V_o \tag{3.10}$$

$$L_{boost}\frac{di_{Lboost}}{dt} = V_s - i_{Lboost}R_{Lboost} - V_D - V_o \tag{3.11}$$

$$\left(V_s - i_{Lboost}(R_{switch} + R_{Lboost})\right)D + \left(V_s - i_{Lboost}R_{Lboost} - V_D - V_o\right)D' = 0 \tag{3.12}$$

$$V_o = \frac{V_s - i_{Lboost}R_{Lboost} - i_{Lboost}R_{switch}D - D'V_D}{D'} \tag{3.13}$$

3.3 Small Signal Analysis of non ideal Boost converter

While the switch S_{boost} is functioning in the conducting state, the equations are as follows

$$V_s = \left(R_{switch} + R_{Lboost}\right)i_{Lboost} + L_{boost}\frac{di_{Lboost}}{dt} \tag{3.14}$$

The current which tends to pass through the capacitor is provided by

$$c\frac{dV_c}{dt} = -\frac{V_o}{R_L} = -\frac{V_c}{R_L + R_c} \tag{3.15}$$

The relationship of the output voltage (V_o) with capacitor voltage (V_c) is depicted by

$$V_o(s) = aV_c(s) \tag{3.16}$$

where, $a = \frac{R_L}{R_L + R_c}$

While the switch S_{boost} is functioning in the non-conducting state, the equations are as follows

$$L_{boost}\frac{di_{Lboost}}{dt} = V_s - V_D - V_o - R_{Lboost}i_{Lboost} \tag{3.17}$$

The current which tend to pass through the capacitor is given by

$$c\frac{dV_c}{dt} = -\frac{V_o}{R_L} + i_{Lboost} \tag{3.18}$$

$$c\frac{dV_c}{dt} = -\frac{aV_c + ai_{Lboost}R_c}{R_L} + i_{Lboost} \tag{3.19}$$

The relationship of the output voltage (V_o) with capacitor voltage (V_c) during the time when the switch S_{boost} is non conducting is given by

$$V_o(s) = aV_c(s) + aI_{Lboost}(s)R_c \tag{3.20}$$

The state equation with the substitution of output voltage (V_o) is portrayed as

$$L_{boost}\frac{di_{Lboost}}{dt} = V_s - V_D - aV_c - ai_{Lboost}R_c - R_{Lboost}i_{Lboost} \tag{3.21}$$

The averaging equations depicted as

$$L_{boost}\frac{di_{Lboost}}{dt} = V_s - R_{Lboost}i_{Lboost} - Di_{Lboost}R_{switch} - D'V_D - aD'V_c - aD'i_{Lboost}R_c \tag{3.22}$$

$$c\frac{dV_c}{dt} = -\frac{V_c}{R_{boost} + R_c} + i_{Lboost}D'\left(1 - \frac{R_c}{R_L + R_c}\right) \tag{3.23}$$

The equation formed after the introduction of the perturbations in the Eq (3.22),

$$\begin{aligned} sL_{boost}\hat{i}_{Lboost} = {} & \hat{V}_s - \hat{i}_{Lboost}R_{Lboost} - \left(D + \hat{d}\right)\left(I_{Lboost} + \hat{i}_{Lboost}\right)R_{switch} - (D' - \hat{d})V_D \\ & - a(D' - \hat{d})(V_c + \hat{v}_c) - a(D' - \hat{d})\left(I_{Lboost} + \hat{i}_{Lboost}\right)R_c \end{aligned} \tag{3.24}$$

$$\left(sL_{boost} + R_{Lboost} + DR_{switch} + aD'R_c\right)\hat{i}_{Lboost} = -\hat{d}\left(I_{Lboost}R_{switch} + aV_c + V_D + aI_{Lboost}R_c\right) - aD'\hat{v}_c \tag{3.25}$$

The equation formed after the introduction of the perturbations in the Eq (3.23),

$$c\frac{d\hat{v}_c}{dt} = -\frac{\hat{v}_c}{R_L + R_c} + (I_{Lboost} + \hat{i}_{Lboost})(D' - \hat{d})\left(1 - \frac{R_c}{R_L + R_c}\right) \tag{3.26}$$

Converting the perturbed equations into the Laplace domain and which is depicted as,

$$sc\hat{v}_c + \frac{\hat{v}_c}{R_L + R_c} = \left(sc + \frac{1}{R_L + R_c}\right)\hat{v}_c = -I_{Lboost}\hat{d}\left(1 - \frac{R_c}{R_c + R_L}\right) + \hat{i}_{Lboost}D'\left(1 - \frac{R_c}{R_c + R_L}\right) \tag{3.27}$$

Eliminating the complexity of the equation (3.27)

$$\hat{v}_c = \frac{1}{sc\left(R_L + R_c\right)+1}\left[-I_{Lboost}\hat{d}R_L + \hat{i}_{Lboost}D'R_L\right] \tag{3.28}$$

Replacement of any variable with respect to the capacitor voltage (V_c)

$$\left(s^2 L_{boost}C\left(R_L + R_c\right) + sM + N\right)\hat{i}_{Lboost} = \hat{d}P\left(sc\left(R_c + R_L\right)+1\right) + aD'I_{Lboost}R_L\hat{d} \tag{3.29}$$

where,

$$M = L_{boost} + c\left(R_L + R_c\right)\left(R_L + DR_{switch} + aD'R_c\right) \tag{3.30}$$

$$N = \left(R_{Lboost} + DR_{switch} + aD'R_c\right) + a\left(D'\right)^2\left(R_c + R\right) \tag{3.31}$$

$$P = -I_{Lboost}R_{switch} + V_D + aV_c + aI_{Lboost}R_c \tag{3.32}$$

The current loop transfer function is displayed with the help of inductor current and duty cycle as,

$$\frac{\hat{i}_{Lboost}}{\hat{d}} = \frac{P\left(sc(R_c + R_L)+1\right) + aD'I_{Lboost}R_L}{\left(s^2 L_{boost}C\left(R_c + R_L\right) + sM + N\right)} \tag{3.33}$$

Eliminating the complexity equation (3.27)

$$\left(sc + \frac{1}{R_c + R_L}\right)\hat{v}_c = -I_{Lboost}\hat{d}\left(1 - \frac{R_c}{R_c + R_L}\right) + \hat{i}_{Lboost}D'\left(1 - \frac{R_c}{R_c + R_L}\right) \tag{3.34}$$

$$\begin{aligned}&\left(sL_{boost} + R_{Lboost} + R_{switch}D + aD'R_c\right)\left[\hat{v}_c\,\frac{sc(R_L + R_c)+1}{D'R_L} + I_{Lboost}\,\frac{\hat{d}}{D'}\right] \\ &\quad = -\hat{d}\left(I_{Lboost}R_{switch} - aV_c - V_D - aI_{Lboost}R_c\right) - aD'\hat{v}_c\end{aligned} \tag{3.35}$$

The voltage loop transfer function is displayed with the help of capacitor voltage (V_c) and duty cycle and this is provided as,

$$\frac{\hat{v}_c}{\hat{d}} = \frac{R_L\left[P - \frac{I_{Lboost}}{D'}\left(sL_{boost} + R_{Lboost} + R_{switch}D + aD'R_c\right)\right]}{s^2 L_{boost}C\left(R_L + R_c\right) + sM + N} \tag{3.36}$$

The averaging output voltage equations is displayed as followed

$$V_o(s) = aV_c(s) + aD'I_{Lboost}(s)R_c \tag{3.37}$$

The equation formed after the introduction of the perturbations are expressed as,

$$\hat{v}_o(s) = a\hat{v}_c(s) + a\left(D' - \hat{d}\right)\left(I_{Lboost} + \hat{i}_{Lboost}\right)R_c \tag{3.38}$$

Eliminating the complexity equation (3.38)

$$\hat{v}_o(s) = a\hat{v}_c(s) - a\hat{d}(s)I_{Lboost}r_c + aD'\hat{i}_{Lboost}(s)R_c \tag{3.39}$$

The voltage loop transfer function is displayed with the use of output voltage (V_o) and duty cycle and is stated as,

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = a\frac{\hat{v}_c(s)}{\hat{d}(s)} - aI_{Lboost}R_c + aD'\frac{\hat{i}_{Lboost}(s)}{\hat{d}(s)}R_c \tag{3.40}$$

3.4 Control system of non ideal Boost converter

The closed-loop system in power electronics DC-DC converters functions to guarantee stability and modulate output voltage through continuous monitoring and adjustment based

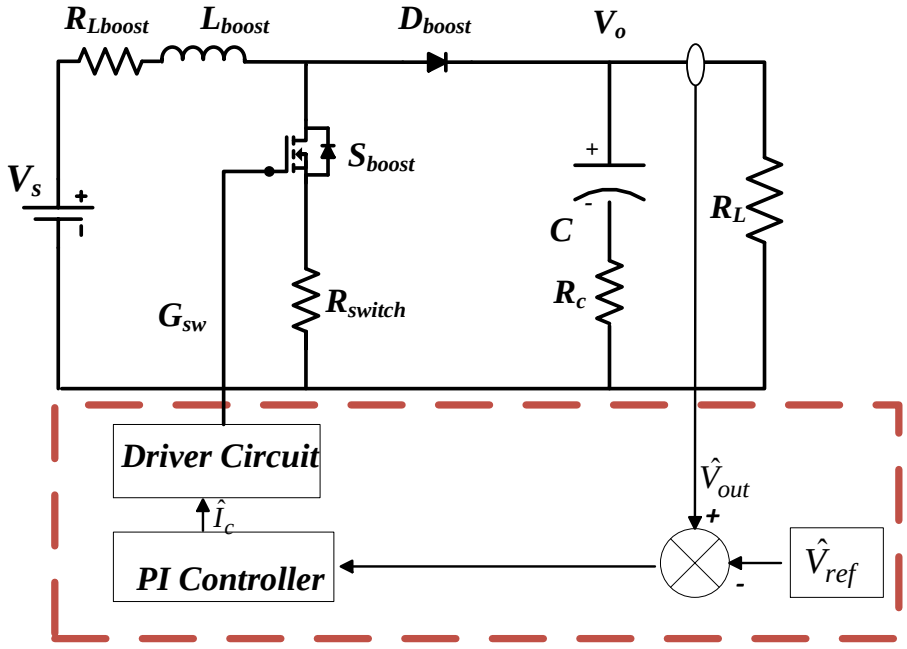


Fig. 3.2 Non ideal voltage controlled BODC with PI controller

on feedback. It facilitates real-time alterations to regulate signals by comparing actual output with the intended reference via a feedback loop. This mechanism, coupled with

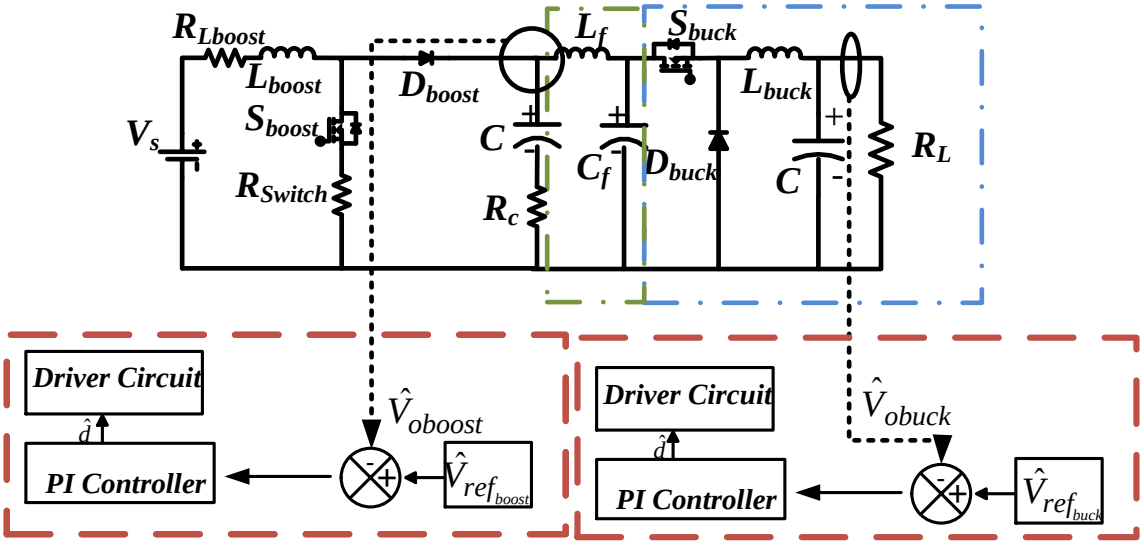


Fig. 3.3 Non ideal voltage controlled BODC with PI controller feeding a constant power load.

consideration for fluctuations and disturbances in input conditions, ensures precise and reliable voltage control.

3.4.1 Closed loop control with PI controller

The PI (Proportional-Integral) controller bears supreme significance within closed-loop systems of power electronics DC-DC converters, facilitating meticulous regulation of output voltage. Through the integration of proportional and integral actions, it modifies the control signal in response to the current error and accumulated past errors. This mechanism assures expeditious adaptation to abrupt variations and eradicates steady-state errors, thereby augmenting both stability and precision. There are two types of load encountered in this section, firstly there is resistive load and secondly there is a constant power load attached to the system as shown in Fig. 3.3. The constant power load is a voltage controlled BUDC and the BUDC is attached through a filtration system consisting of an inductor (L_f) and capacitor (C_f).

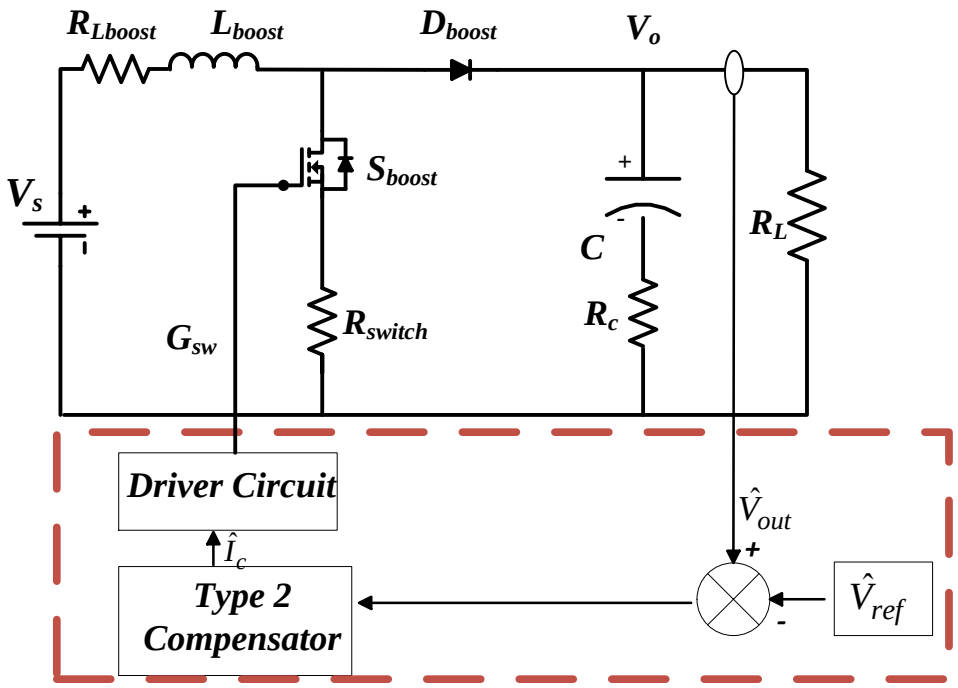


Fig. 3.4 Non ideal voltage controlled BODC with T2C

3.4.2 Closed loop control with Type 2 compensator

Closed-loop response is attained using a Type II compensator (T2C) This system employs T2C for optimal performance. minimizes output voltage error, serving as input for the PWM block. The T2C acting as the voltage controller, introduces an additional pole, providing added flexibility. This lead compensator, along with a pole at the origin, to ensure null steady-state error with this, it imparts a phase boost from 0° to 90°, enhancing system performance.

$$T_{C_V}(s) = \frac{\left(1+\frac{s}{\omega_z}\right)}{\frac{s}{\omega_{po}}\left(1+\frac{s}{\omega_p}\right)} \tag{3.41}$$

where ω_z depicted as the pole location, ω_p stands for the zero location along with ω_{po} refers the pole at a specific crossover frequency.

The magnitude offered by the T2C controller can be illustrated as,

$$\left|T_{C_V}(s)\right| = \frac{\left|1+j\frac{\omega}{\omega_z}\right|}{\left|j\frac{\omega}{\omega_{po}}\right|\left|1+j\frac{\omega}{\omega_p}\right|} = \frac{\sqrt{1+\left(\frac{\omega}{\omega_z}\right)^2}}{\frac{\omega}{\omega_{po}}\sqrt{1+\left(\frac{\omega}{\omega_p}\right)^2}} \tag{3.42}$$

The phase angle offered by the T2C is depicted as,

$$\arg T_{C_V}(jw) = \tan^{-1}\left(\frac{\omega}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega}{\omega_p}\right) - \frac{\pi}{2} \tag{3.43}$$

The frequency range demanded for the phase boosting which can be aspect from T2C is refereed as,

$$\begin{aligned}\frac{d}{df}\left(\arg T_{C_V}(j\omega)\right) &= \frac{d}{df}\left(\tan^{-1}\left(\frac{\omega}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega}{\omega_p}\right) - \frac{\pi}{2}\right) \\ &= \frac{1}{f_z\left(\frac{f^2}{f_z^2}+1\right)} - \frac{1}{f_p\left(\frac{f^2}{f_p^2}+1\right)} = 0\end{aligned} \tag{3.44}$$

As it is portrayed, the GM taken between the pole along with the zero frequencies which gives maximum phase boost is depicted as,

$$f_{max} = \sqrt{f_p f_z} \tag{3.45}$$

The PB which can be offered by the T2C is illustrated as,

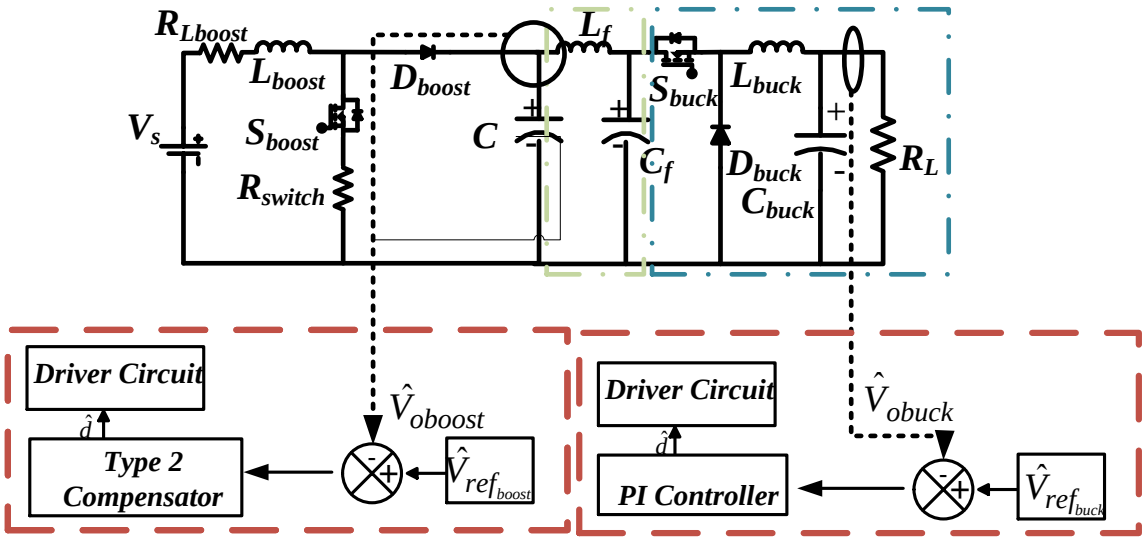


Fig. 3.5 Non ideal voltage controlled BODC with T2C feeding a CPL.

$$PB = \tan^{-1}\left(\frac{f_c}{f_z}\right) - \tan^{-1}\left(\frac{f_c}{f_P}\right) \tag{3.46}$$

If T2C controller is considered, gain crossover frequency f_c which is defined as,

$$f_c = f_{\max} = \sqrt{f_p f_z} \tag{3.47}$$

For every compensator, the optimum PM can be chosen to enhance the performance which is desired from the system. The frequency of the zero can be assumed by the values of f_p as

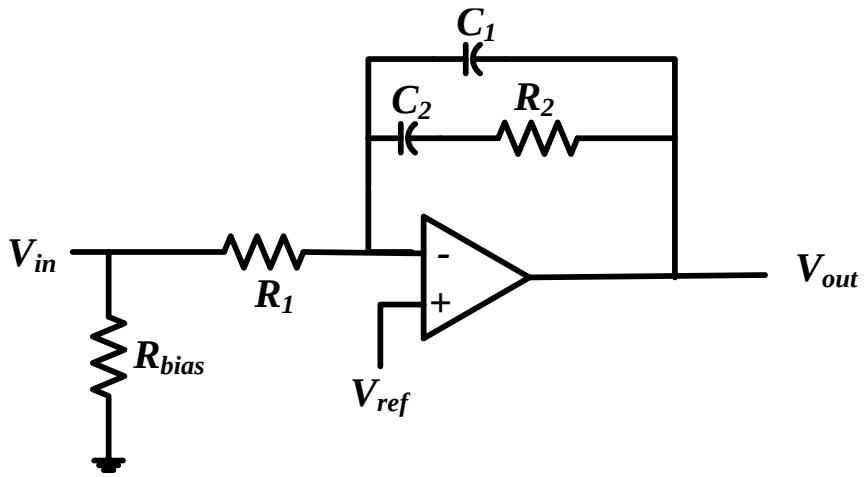


Fig. 3.6 T2C circuit diagram.

well as f_c which are known. The frequency of zero which is demanded from the system, can be formulate as,

$$f_z = \frac{{f_c}^2}{f_p} \tag{3.48}$$

Taking the consideration of T2C, the 'constant k' used in this case. So that the PB demanded in terms of k can be formulated as,

$$PB = \tan^{-1}(k) - \tan^{-1}\left(\frac{1}{k}\right) \tag{3.49}$$

where $k = \frac{f_p}{f_z}$

The expression which is used for phase boosting along with the frequencies can be summarised as,

$$k = \tan\left(\frac{PB}{2} + \frac{\pi}{4}\right) \tag{3.50}$$

The expression which can be relate to pole as well as zero frequencies considering PB can be depicted as,

$$f_p = k \times f_c = \tan\left(\frac{PB}{2} + \frac{\pi}{4}\right) \times f_c \tag{3.51}$$

$$f_z = \frac{f_c}{k} = \frac{f_c}{\tan\left(\frac{PB}{2} + \frac{\pi}{4}\right)} \tag{3.52}$$

Assuming the phase boost as 83° at the specific crossover frequency which is of 400 Hz, and recognizing that a higher phase boost corresponds to a greater PM, the pole along with zero frequencies which can be estimated as follows:,

$$f_p = \tan\left(\frac{83^\circ}{2} + 45\right) \times 400 = 6.54kHz \tag{3.53}$$

$$f_z = \frac{400}{\tan\left(\frac{83^\circ}{2} + 45\right)} = 24.5Hz \tag{3.54}$$

A pole-zero pair, which can be combined with an extra advantage of an origin pole, constitutes a T2C. In case of rewriting the numerator by factoring s/ω_Z .

$$T_{C_V}(s) = \frac{s}{\omega_z} \frac{\left(1 + \frac{\omega_z}{s}\right)}{\frac{s}{\omega_{po}}\left(1 + \frac{s}{\omega_p}\right)} = \frac{\omega_{po}}{\omega_z} \frac{\left(1 + \frac{\omega_z}{s}\right)}{\left(1 + \frac{s}{\omega_p}\right)} = G_o \frac{\left(1 + \frac{\omega_z}{s}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \tag{3.55}$$

The mid band gain is named as G_o along with its value is ω_{po}/ω_z .

After summing up, the overall transfer function of T2Cwhich is defined as,

$$T_{c_v}(s) = \frac{1271.23(s + 153.7184)}{s(s + 41091.668)} \tag{3.56}$$

A similar concept of CPL is applied over here. The CPL is attached through a filtration system. As depicted in Fig. 3.5, the system of BODC with T2C controlled feeding a CPL is depicted over here.

3.5 Results of non ideal Boost converter

This section illustrates the steady-state outcome of a 25 W BODC converter. It reveals two

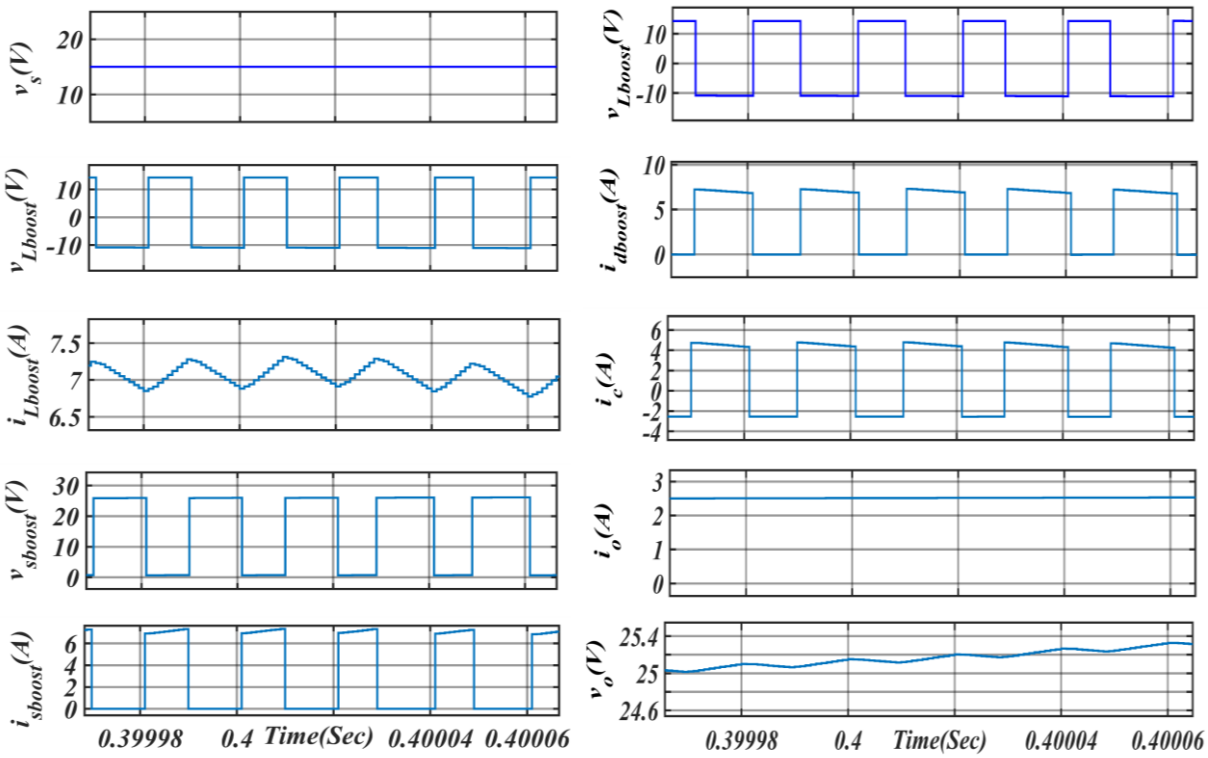


Fig. 3.7 (a) Fig. 3.7 (b)

Fig 3.7(a): Waveform of the $v_s(V)$,$v_{Lboost}(V)$,$i_{Lboost}(A)$,$vs_{boost}(V)$*and* $is_{boost}(A)$; Fig 7(b) Waveform of the $v_{Lboost}(V)$, $i_{dboost}(A)$, $i_c(A)$, $i_o(A)$ *and* $v_o(V)$.

distinct phases in the inductor current waveform: a charging stage and a discharging stage. The switch experiences a voltage stress reaching up to 25 volts. The proportional-integral controller is precisely calibrated to establish a closed-loop operation for the BODC converter and this is one of the most applied concepts in closed loop operation. In this section, the performance of BODC is validated under both resistive load and constant power load by utilizing of both PI controller along with T2C.

3.5.1 Simulation Results of non ideal Boost converter with PI controller.

A stiff supply of 15 volt is provided to the system. The waveform of inductor voltage ($v_{Lboost}(V)$) and inductor current ($i_{Lboost}(A)$) brings clarity in charging and discharging stored energy. Fig. 3.7 (a) depicts the switch voltage and switch current with their limit. The switch voltage is sustained till 25 volts which is the output voltage in this case. The switch current does not cross beyond the 7 A. The switch develops a voltage of 25 volts across it when the switch is not in conducting mode and the switch current is not present at the moment. Fig. 3.7 (b) repeats the waveform of inductor voltage to bring the connection between Fig. 3.7

(a) along with the Fig. 3.7 (b). The Fig. 3.7 (b) shows the behaviour of diode current and capacitor current. The diode current showcases two states of the BODC converter. The waveform of the output current and voltage is portrayed in the Fig. 3.7 (b) and this shows a stable behaviour of the BODC.

3.5.2 Simulation Results of non ideal Boost converter with Type 2 controller.

The T2C, serving as the voltage controller, introduces an additional pole, thereby enhancing flexibility. This lead compensator, featuring a pole at the origin, guarantees null steady-state error along with a phase boost from 0° to 90°, thereby enhancing system performance. A stable 15-volt power supply is provided to the system. The waveforms of inductor voltage ($v_{Lboost}(V)$) and inductor current ($i_{Lboost}(A)$) elucidate the charging and discharging of stored energy. In Figure 3.8 (a), the switch voltage and switch current, along with their respective limits, are depicted. The switch voltage remains constant at 25 volts, which is the output voltage in this scenario, while the switch current does not exceed 7 A. When the switch is not conducting and no switch current is present, a voltage of 25 volts is developed across the switch. Figure 3.8 (b) replicates the inductor voltage waveform to establish continuity between Figure 3.8 (a) and Figure 3.8 (b). Figure 3.8 (b) presents the waveforms of diode

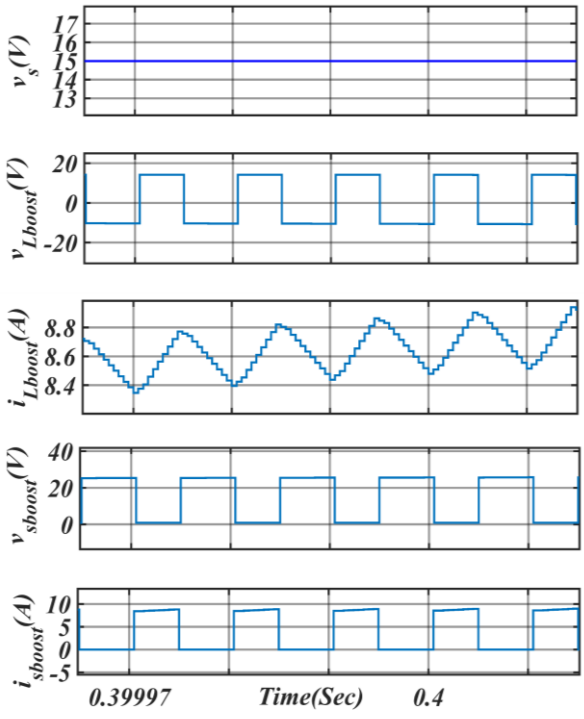


Fig. 3.8 (a)

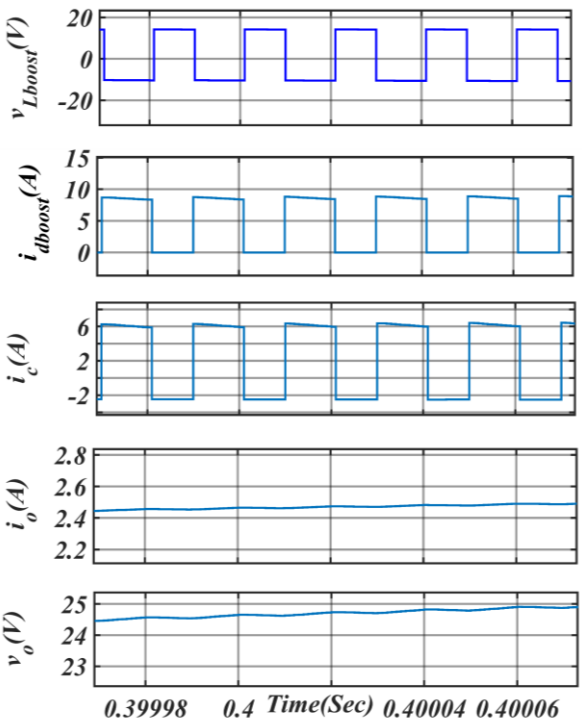


Fig. 3.8 (b)

Fig 3.8 (a): Waveform of the $v_s(V)$,$v_{Lboost}(V)$,$i_{Lboost}(A)$,$vs_{boost}(V)$*and* $is_{boost}(A)$; Fig 3.8 (b) Waveform of the $v_{Lboost}(V)$, $i_{dboost}(A)$, $i_c(A)$, $i_o(A)$ *and* $v_o(V)$.

current and capacitor current. The diode current illustrates two states of the BODC converter. The waveform of load current with the load voltage can be illustrated in Figure 3.8 (b) demonstrates a quite a stable behaviour of the BODC. The BODC converter brings a similar result as BODC using a PI controller.

most applied concept in closed loop operation.

3.5.3 Simulation Results of non ideal Boost converter with PI controller feeding a constants power load

The concept of CPL portrays equal amount of power in both the input and output of a system. A voltage controlled BUDC is attached with the BODC which is voltage controlled through a PI controller. A stiff supply of input voltage of 15 V is being attached. The BODC follows the property of discharging and charging of inductor. The voltage of the inductor reaches up to 15 volt while charging of the inductor. While the charging stage, the current is flowing through the switch and its value reaches up to 6 A and while the discharging state, there is no current through the switch (S_{boost}). Fig. 3.9 (b) shows the waveform of the diode current which is not conducting during the conducting stage of the switch (S_{boost}). It can be seen that the output voltage of the BODC is restricted with a desired limit and after passing through a filtering system, the input voltage of BUDC comes stable. The switch currents of the BUDC is illustrated in Fig. 3.9 (b) and this shows that the switch current is in a limit. Fig. 3.9 (c) portrays the standard behaviour of a conventional BUDC which is discharging and charging of inductor. It depicts the stable behaviour of the BUDC through its output voltage and output current. The effect of PI controller is illustrated through the Fig. 3.10 (d) which portrays its PM of 40º. As show in the figure, it is closed loop stable as well.

3.5.4 Simulation Results of non ideal Boost converter with the T2C controller feeding a constants power load

The concept of a CPL entails an equilibrium of power between the input and output of a system. A voltage-controlled BUDC is integrated with the BODC, governed by a PI controller. A stable 15 V input voltage is supplied. The BODC operates by charging and discharging the inductor. During the charging phase, the inductor voltage reaches 15 volts, with a current flow through the switch culminating at 7 A. In the discharging phase, there is no current flow through the switch (S_{boost}). Fig 3.10 (a) illustrates the diode current waveform, which remains inactive during the switch's conducting phase. The BODC's output voltage is constrained within desired limits, stabilized after passing through a filtering system, ensuring the stability of the BUDC's input voltage. The switch currents of the BUDC

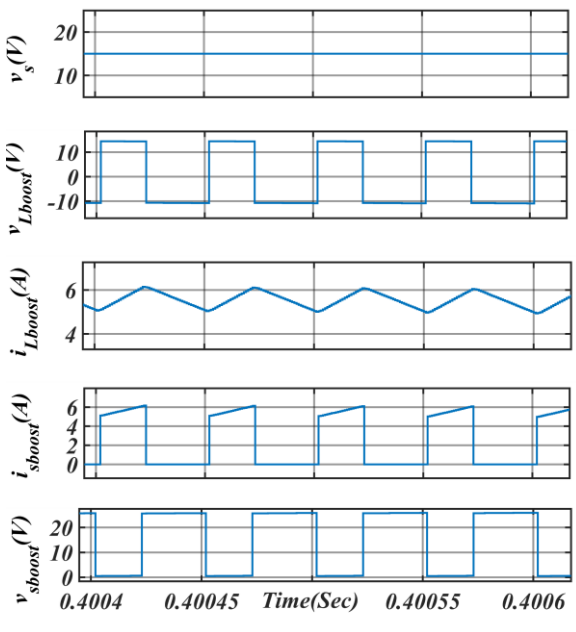


Fig. 3.9 (a)

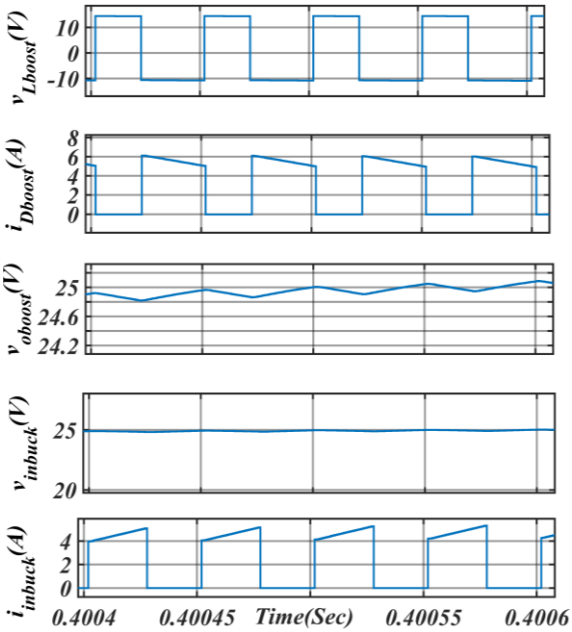


Fig. 3.9 (b)

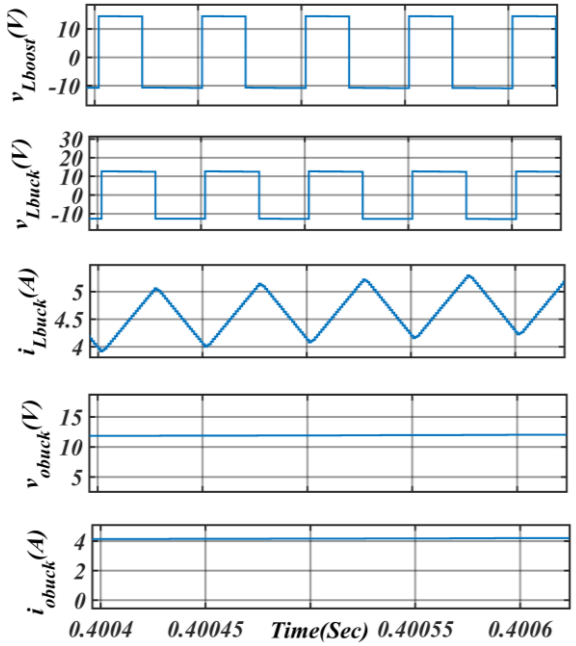


Fig.3.9(c)

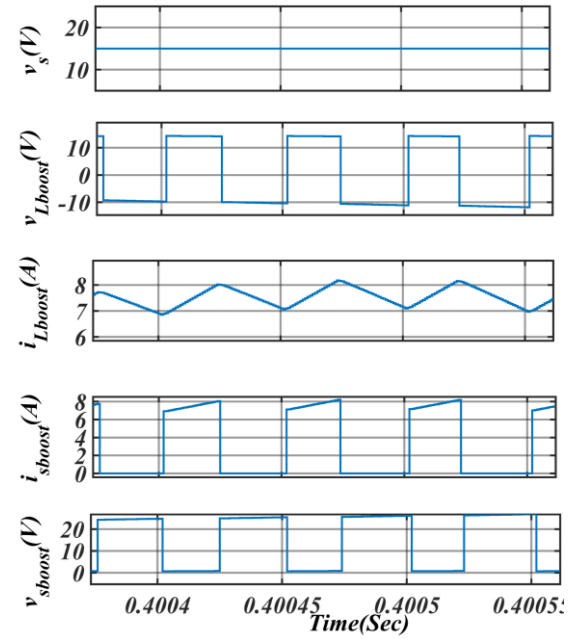


Fig.3.9(d)

Fig. 3.9 (a) Waveform of $v_s(V)$, $v_{Lboost}(V)$, $i_{Lboost}(A)$, $i_{sboost}(A)$, $v_{sboost}(V)$ in case of using PI controller Fig. 3.9 (b) Waveform of $v_{Lboost}(V)$, $i_{Dboost}(A)$, $v_{oboost}(V)$, $v_{inbuck}(V)$, $i_{inbuck}(A)$ in case of using PI controller. Fig. 3.9 (c) Waveform of $v_{Lboost}(V)$, $v_{Lbuck}(V)$, $i_{Lbuck}(A)$, v_{obuck} (V), $i_{obuck}(A)$) in case of using PI controller. Fig. 3.9 (d) Waveform of $v_s(V)$, $v_{Lboost}(V)$, $i_{Lboost}(A)$, $i_{sboost}(A)$, $v_{sboost}(V)$ in case of using T2C.

are depicted in Fig3.10 (a), indicating adherence to set limits. Fig 3.10 (b) displays the typical behaviour of a conventional BUDC, involving the charging and discharging of the inductor,

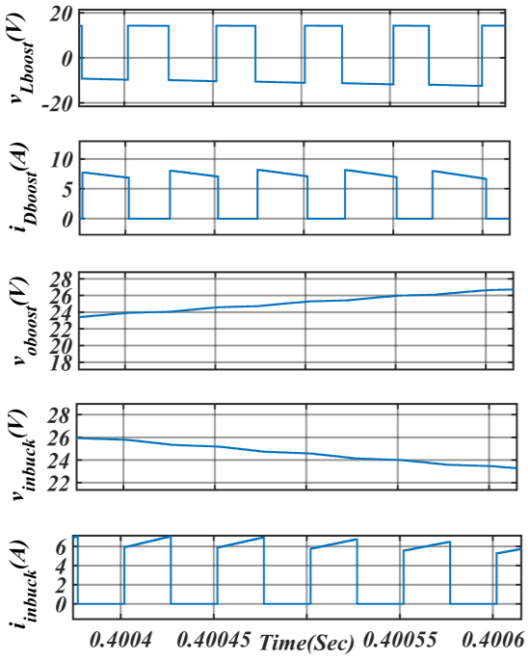


Fig. 3.10(a)

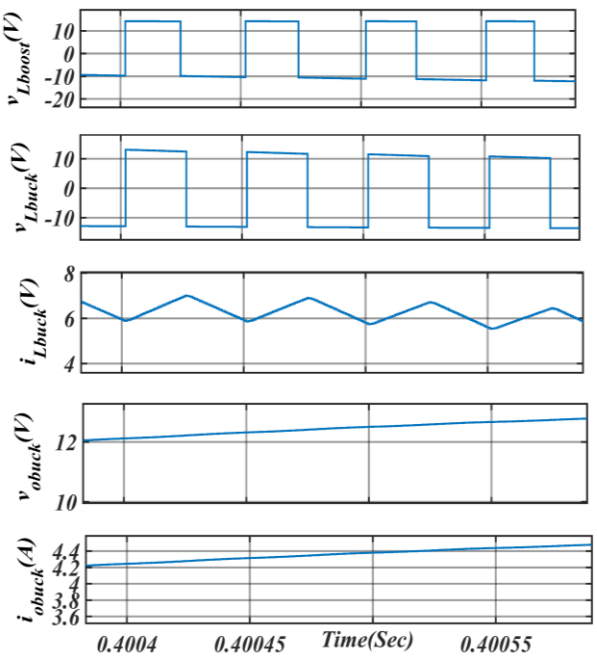


Fig. 3.10(b)

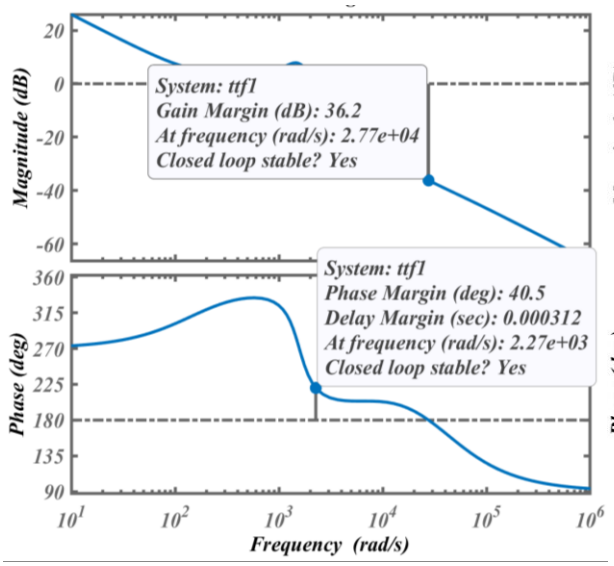


Fig. 3.10(c)

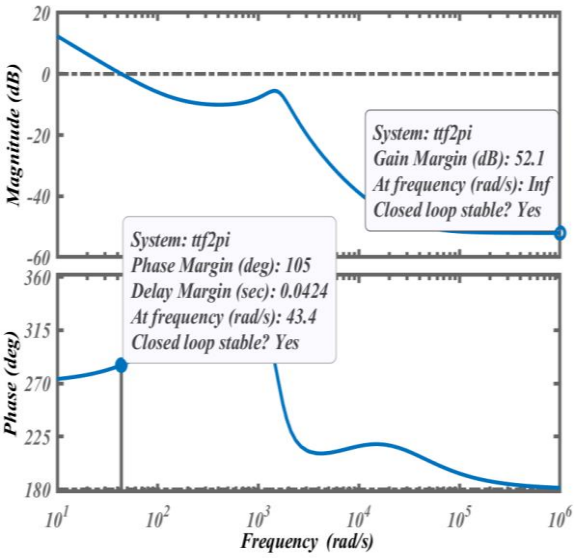


Fig. 3.10(d)

Fig. 3.10 (a) Waveform of $v_{Lboost}(V)$, $i_{Dboost}(A)$, $v_{oboost}(V)$, $v_{inbuck}(V)$, $i_{inbuck}(A)$ in case of using Type 2 controller. Fig. 3.10 (b) Waveform of $v_{Lboost}(V)$, $v_{Lbuck}(V)$, $i_{Lbuck}(A)$, $v_{obuck}(V)$, $i_{obuck}(A)$) in case of using T2C. Fig. 3.10 (c) Bode of BODC with PI compensator. Fig. 3.10 (d) Bode of BODC with T2C.

showcasing sustained output voltage and current. The effect of T2C is illustrated through the Fig. 3.10 (c) which portrays its PM of 105º.

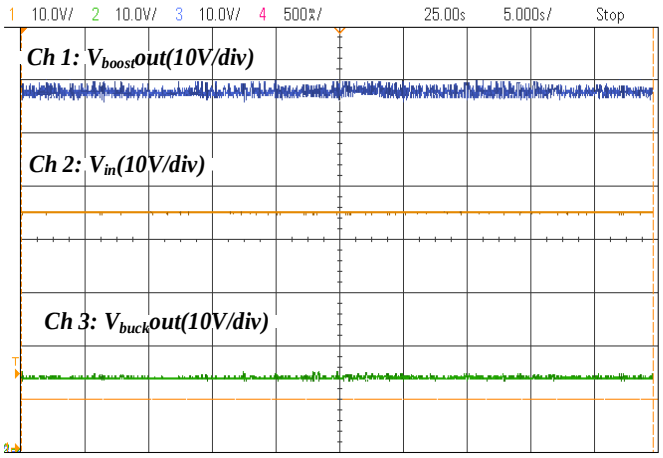


Fig. 3.11 Waveform of output voltage in the BODC and the BUDC with the variation in input voltage at Steady State.

3.5.5 Steady state results of non ideal Boost converter with PI controller feeding a constants power load through experimental setup.

In this section, a fixed input voltage of 45V is applied, as shown in Fig. 3.11. Fig 3.12 illustrates the complete experimental configuration, which includes a host PC that

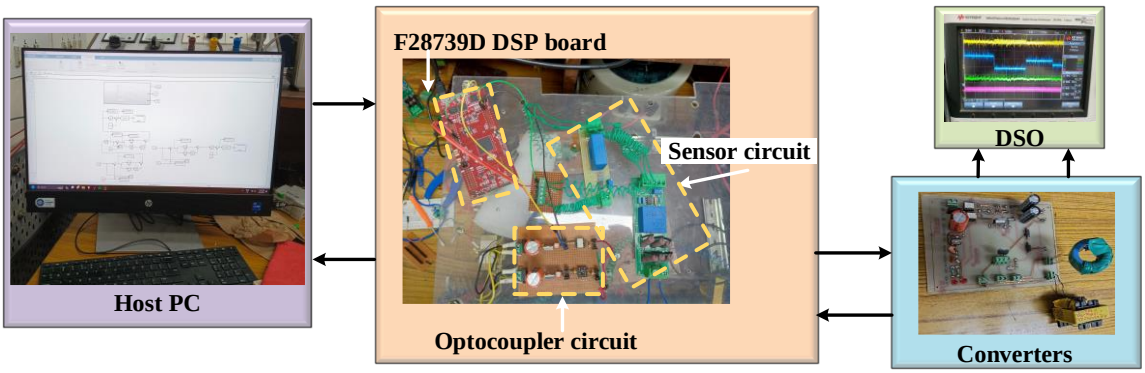


Fig. 3.12 Experimental setup

communicates with the DSP TI F28739. An optocoupler circuit initiates the converter switch, while two sensor circuits provide feedback. Various parameter waveforms are recorded using a Digital Storage Oscilloscope (DSO). The fixed input voltage, with a power rating of 36 watts, is examined through the output voltage waveforms in both the BODC and BUDC. The results indicate that the output ripple for both converters remain within acceptable limits. The BODC produces an output of 69V, while the BUDC produces an output of 13V.

3.6 Conclusion

This chapter explains the concept related to BODC converter through 4 portions. The modelling of BODC at steady state is portrayed in the second portion of this chapter and the voltage equation at the output in steady state is being depicted in this portion. The small

signal modelling which includes the effect of ESR is clarified in the portion of small signal modelling. The BODC is displayed under two types of controllers which are PI controller and T2C with both resistive and constant power is taken into consideration. The results of BODC under different types of loads and controllers are catered under this portion. The capability of BODC to cater constant power load which is a BUDC, is clarified in this portion. As the small signal analysis points out the effect of the RHZ which is eliminated to TSB converter is portrayed in upcoming chapters.

Chapter 4

MODELLING AND ANALYSIS OF TRISTATE BOOST CONVERTER

4.1 Introduction

This part addresses the need for a stable and consistent voltage profile in practical applications. The TSB converter satisfies this requirement by preserving a steady voltage profile. This topology eliminates the RHP zero prevalent in standard BODC converters. The existence of RHP zero in the time domain results in a very much a sudden decline in the load voltage of the converter, which increases the load current and the duty ratio, thereby extending the output capacitor's discharge time. This leads to a further decline in output voltage until the inductor current increases sufficiently to recharge the capacitor. This section explains the concept of TSB converter and the way it eliminates RHP zero of the standard BODC.

4.2 Modelling of Tristate Boost converter

This section sums up the modelling portion in TSB converter, encompassing all modes of operation in TSB converter. The primary circuit schematic which is illustrated the numerous operational phases, is depicted in Fig. 4.2. In Fig. 4.2 (a), the principal circuit of TSB converter is viewed, while the Fig. 4.2 (b), (c), and (d) illustrate three distinct stages.

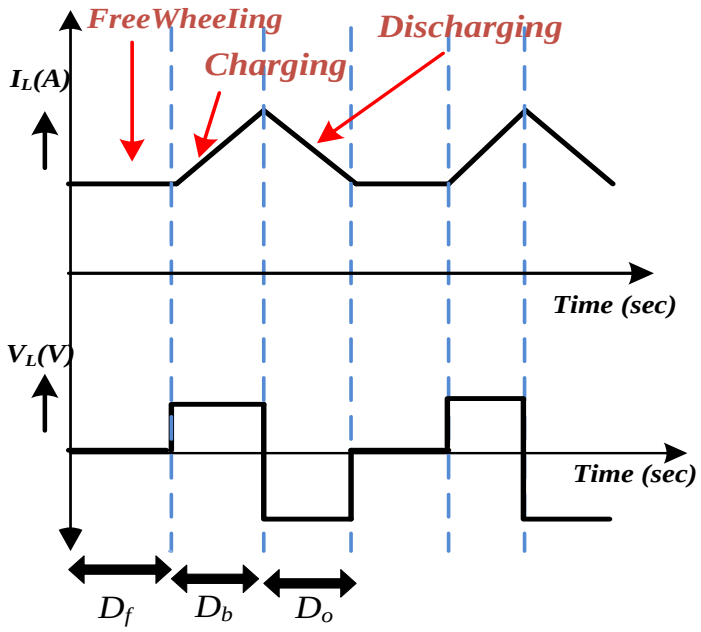


Fig. 4.1 Graph displaying Inductor Current along with the Inductor Voltage in ideal TSB converter

Mode I describes the freewheeling mode, where switch S_f remains conductive while S_m is off, rendering diode D non-conductive. During this stage, the capacitor supplies power to the load. In Mode II of the operation in TSB, both switches S_f and S_m are conductive, permitting the accumulation of inductor current. Diode D is in reverse bias, and capacitor C_b powers the load which is attached to TSB. In Mode III of the operation in TSB, the switches

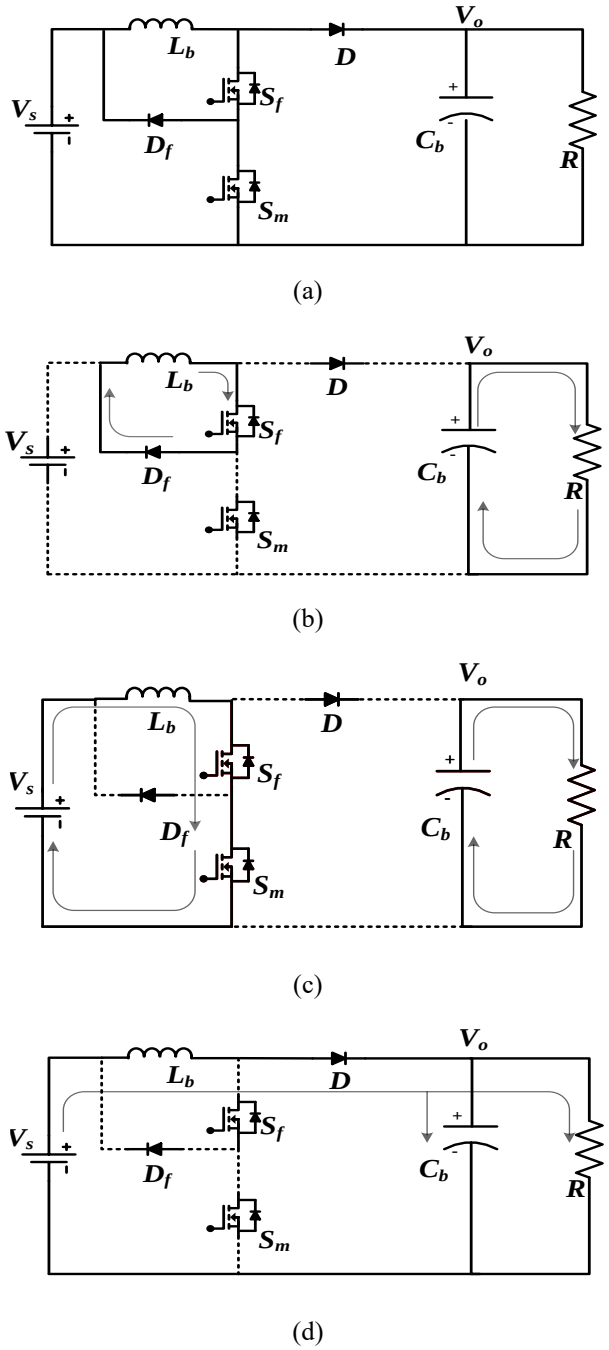


Fig. 4.2 Circuit of TSB along with the modes (a) Circuit of the TSB (b)operating in Mode-I executing in TSB (c) operating in Mode II executing in TSB (d) operation executing in Mode III operation in TSB.

S_f and S_m are both not conductive by nature, along with the diode D is conductive. The inductor current decreases as power are transferred to the load, and capacitor C_b is recharged. The modelling procedure accommodates for the various modes of operation, which is depicted in the Fig. 4.1, which illustrates all the defined profiles of the inductor current and inductor voltage for the TSB converter.

As mentioned in Fig. 4.1, there are three stages in the TSB which is having three different duty cycle taken into consideration. The first one which represents the freewheeling stage is D_f and rest of the part resembles just as standard BODC which is the charging stage (D_b) and the discharging stage (D_o). The freewheeling stage makes the inductor voltage equal to zero where the inductor is allowed to freewheeling the charge stored in the inductor.

The Steady state output voltage gain is stated as,

$$\frac{V_o}{V_s} = \frac{D_b + D_o}{D_o} \tag{4.1}$$

4.3 Small Signal Modelling of Tristate Boost converter

As it is depicted in the Fig.4.1, the indication of the inductor current (I_L) along with the inductor voltage (V_L) profile in case of TSB converter is portrayed with clarity. While the small-signal model of TSB is been derived, realistic disturbances are assumed. By assuming, control input perturbation one at a time which resulting in the state variables and these are expressed as,

$$v_c = V_c + \hat{v}_c \tag{4.2}$$

$$i_L = I_L + \hat{I}_L \tag{4.3}$$

$$d_b = D_b + \hat{D}_b \tag{4.4}$$

$$d_o = D_o + \hat{D}_o \tag{4.5}$$

where D_f , D_b and D_o pointed out to be freewheeling ratio and then the charging interval ratio as well as the term discharging ratio respectively. R_M , R_L as well as R_C sums up to be the on-state resistance of the MOSFET, inductor resistance along with ESR of capacitor respectively.

The equations which is defined for the non-ideal TSB along with the various modes can be mentioned as,

Freewheeling (D_fT) time interval:

$$\begin{pmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{pmatrix} = \begin{pmatrix} \frac{-(R_M + R_L)}{L_b} & 0 \\ 0 & \frac{-a}{RC_b} \end{pmatrix} \begin{pmatrix} i_L \\ v_C \end{pmatrix} - \begin{pmatrix} \frac{V_D}{L} \\ 0 \end{pmatrix} \tag{4.6}$$

where $a = \frac{R}{R + R_c}$

Charging (D_bT) time interval:

$$\begin{pmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{pmatrix} = \begin{pmatrix} \frac{-(2R_M + R_L)}{L_b} & 0 \\ 0 & \frac{-a}{RC_b} \end{pmatrix} \begin{pmatrix} i_L \\ v_C \end{pmatrix} - \begin{pmatrix} \frac{1}{L_b} \\ 0 \end{pmatrix} V_s \tag{4.7}$$

Discharging (D_oT) time interval:

$$\begin{pmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{pmatrix} = \begin{pmatrix} \frac{-(2R_C + R_L)}{L_b} & \frac{-a}{L_b} \\ \frac{1}{C_b} - \frac{aR_C}{RC_b} & \frac{-a}{RC_b} \end{pmatrix} \begin{pmatrix} i_L \\ v_C \end{pmatrix} - \begin{pmatrix} \frac{1}{L_b} \\ 0 \end{pmatrix} V_s - \begin{pmatrix} \frac{V_D}{L_b} \\ 0 \end{pmatrix}$$

(4.8)

The averaging of the equations from the all defined modes of operation can be illustrated as,

$$\begin{pmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{pmatrix} = \begin{pmatrix} \frac{-aR_C D_o + R_L + R_M(1 + D_b - D_o)}{L_b} & \frac{-a}{L_b} D_o \\ \left(\frac{1}{C_b} - \frac{aR_C}{RC_b}\right) D_o & \frac{-a}{RC_b} \end{pmatrix} \begin{pmatrix} i_L \\ v_C \end{pmatrix} - \begin{pmatrix} \frac{1}{L_b}(D_b + D_o) \\ 0 \end{pmatrix} V_s - \begin{pmatrix} \frac{V_D}{L_b}(D_f + D_O) \\ 0 \end{pmatrix} \tag{4.9}$$

After the negligence of DC terms along with higher non-linear terms, the equations can be formulated as,

$$\frac{d\hat{I}_L(t)}{dt} = -\frac{\left[aR_c D_o + R_L + R_M(1 + D_b - D_o)\right]}{L_b} \hat{I}_L(t) - \frac{a}{L_b} D_o \hat{V}_c(t) + \frac{V_s + V_D - R_M I_L}{L_b} \hat{D}_b(t) \tag{4.10}$$

$$\frac{d\hat{V}_C(t)}{dt} = \left(\frac{1}{C_b} - \frac{aR_c}{RC}\right) D_o \hat{I}_L(t) - \frac{a}{RC_b} \hat{V}_C(t) \tag{4.11}$$

After the conversion into the Laplace domain, all the predefined equations can be denoted as,

$$sI_L(s) = -\frac{\left[aR_C D_o + R_L + R_M\left(1 + D_b - D_o\right)\right]}{L_b} I_L(s) - \frac{a}{L_b} D_o V_C(s) + \frac{V_s + V_D - R_M I_L}{L_b} D_b(s) \tag{4.12}$$

$$sV_C(s) = \left(\frac{1}{C_b} - \frac{aR_c}{RC_b}\right) D_o I_L(s) - \frac{a}{RC_b} V_C(s) \tag{4.13}$$

The current loop transfer function can be defined with the utilization of the inductor current (I_L) with respective to the charging interval duty defined to be,

$$\frac{I_L(s)}{D_b(s)} = \frac{1}{JL_b C_b R} \frac{\left(V_s + V_D - R_M I_L\right)\left(a + sR_C C_b\right)}{\frac{1}{J}s^2 + \frac{P}{J}s + 1} \tag{4.14}$$

where, $J = \frac{1}{RL_b C_b}\left(aR_L + aR_M + \left[1 - D_o + D_b\right] + a^2 R_C D_o + a^2 D_O^2 R\right)$ (4.15)

where, $P = \frac{1}{RL_b C_b}\left(aL_b + R_L RC_b + RC_b R_M\left[1 - D_o + D_b\right] + aR_C D_O RC_b\right]$ (4.16)

After finding out the relationship between the capacitor voltage and the output voltage, the equation can be portrayed as,

$$v_o(t) = av_c(t) + aR_c D_o i_L(t) \tag{4.17}$$

After conversion into the Laplace-domain, the load voltage equation expresses as the following,

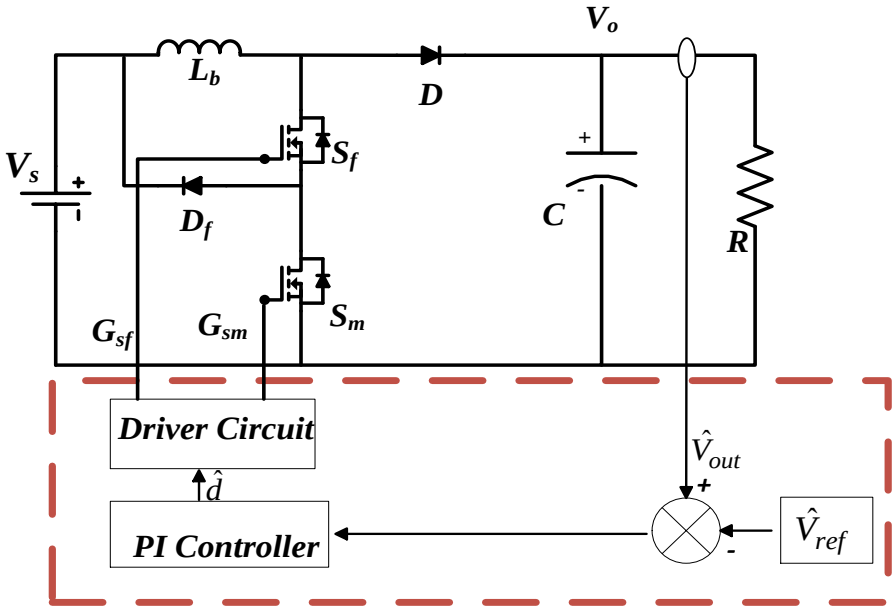


Fig. 4.3. Voltage controlled TSB converter with PI controller.

$$V_o(s) = aV(s) + aR_c D_o I_L(s) \tag{4.18}$$

The voltage loop transfer function can be derived using the output voltage (V_o) along with charging interval duty, is stated as,

$$G_{11}(s) = \frac{V_o(s)}{D_b(s)} = \frac{1}{JL_bC_b} \frac{(V_s + V_D - R_M I_L)(1 + sR_cC_b)}{\frac{1}{J}s^2 + \frac{P}{J}s + 1}$$

(4.19)

where I_L portrays a steady state parameter $I_L = \dfrac{V_s(D_b + D_o) - V_D(D_f + D_o)}{R_L + 2D_bR_M + R_MD_f + aR_CD_o + aRD_o^2}$ (4.20)

4.4 Control system of Tristate Boost converter

The closed-loop system in power electronics DC-DC converters ensures stability and governs output voltage through continuous monitoring and adjustment based on feedback. It facilitates real-time modifications to control signals by comparing the actual output with the intended reference via a feedback loop. This mechanism, combined with the ability to account for fluctuations and disturbances in input conditions, assures precise and reliable voltage control. There are three types of control strategy addressed in this section with the two different types of load which are a constant power load and the resistive.

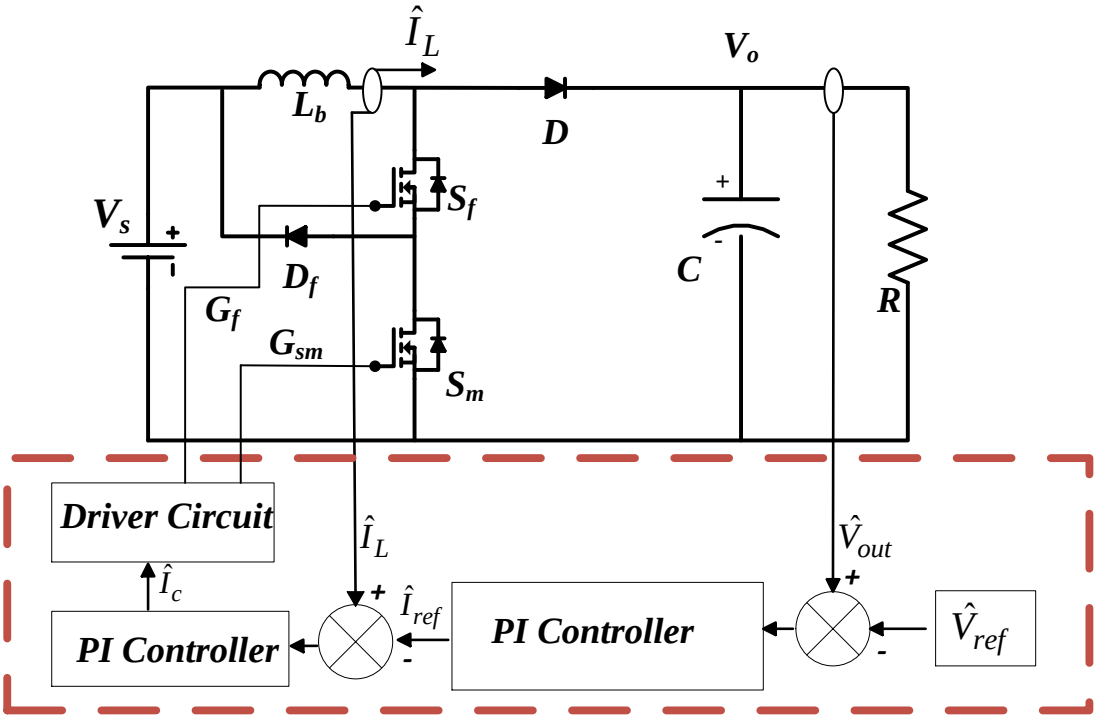


Fig. 4.4 Dual controlled TSB converter using PI controller.

4.4.1 Closed loop control with PI controller

The PI controller bears paramount significance within closed-loop systems of power electronics DC-DC converters, enabling precise regulation of output voltage. By integrating proportional and integral actions, it modifies the control signal in response to the current error and the accumulated prior errors. As expressed in the Fig. 4.3, the output voltage loop is used where the output voltage is compared with the given reference value and fed to a PI controller after that, the signal passes through the driver circuit to perform a proper switching action. The dual loop control is also portrayed in this portion with the use of two PI controllers. One is taking voltage reference at the output of the converter and through another PI controller, it completes the purpose of governing the inductor current with the normal output voltage control as shown in Fig.4.

4.4.2 Closed loop control with Type 2 controller

The T2C acting as the voltage controller, introduces an additional pole, providing added flexibility. This lead compensator, in combination of a pole in the origin, ensures null steady-state error with imparts a PB which is starting from 0° to 90°, enhancing system performance.

$$T_{C_V}(s) = \frac{\left(1+\frac{s}{\omega_z}\right)}{\frac{s}{\omega_{po}}\left(1+\frac{s}{\omega_p}\right)} \tag{4.21}$$

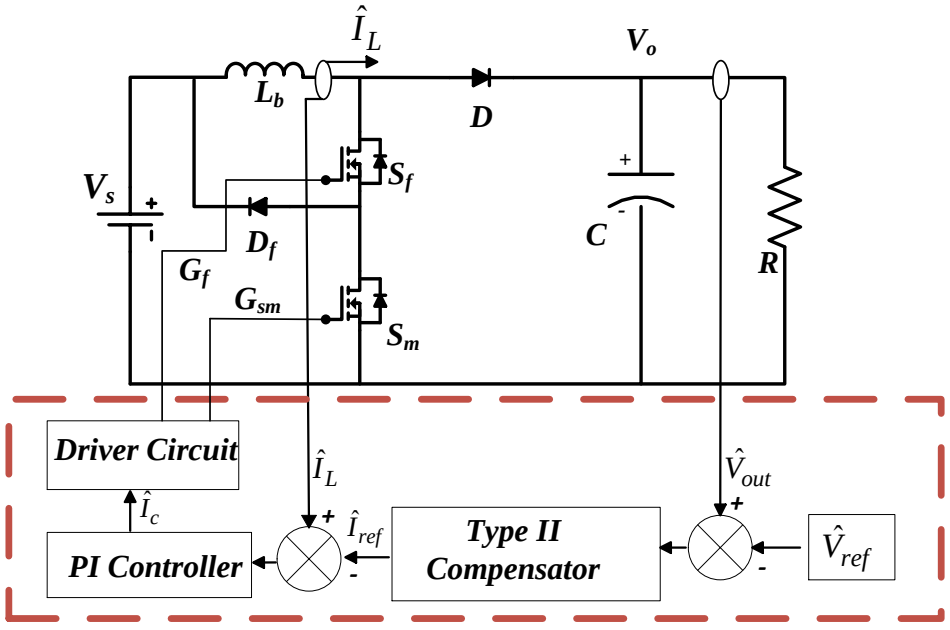


Fig. 4.5. Dual controlled TSB converter using T2C controller.

where ω_z stands for the location of the pole of T2C, ω_p stands for the location of the zero of T2C and ω_{po} stands for the pole with respect to the specified crossover frequency in case of T2C.

Assuming the phase boost to be 83° at the selected crossover frequency at 400 Hz, and recognizing that a higher phase boost corresponds to a greater PM, the pole along with the zero frequencies which can be estimated as follows:

$$f_p = \tan\left(\frac{83^\circ}{2} + 45\right) \times 400 = 6.54kHz \tag{4.22}$$

$$f_z = \frac{400}{\tan\left(\frac{83^\circ}{2} + 45\right)} = 24.5Hz \tag{4.23}$$

A pole-zero pair, with a pole at the origin, constitutes a T2C. Thereby, rewriting the numerator by factorising s/ω_Z .

$$T_{C_V}(s) = \frac{s}{\omega_z} \frac{\left(1+\frac{\omega_z}{s}\right)}{\frac{s}{\omega_{po}}\left(1+\frac{s}{\omega_p}\right)} = \frac{\omega_{po}}{\omega_z} \frac{\left(1+\frac{\omega_z}{s}\right)}{\left(1+\frac{s}{\omega_p}\right)} = G_o \frac{\left(1+\frac{\omega_z}{s}\right)}{\left(1+\frac{s}{\omega_p}\right)} \tag{4.24}$$

The mid band gain is named as G_o along with its value is ω_{po}/ω_z .

After summing up, the overall transfer function of T2C controller can be defined as

$$T_{c_V}(s) = \frac{1271.23(s+153.7184)}{s(s+41091.668)} \tag{4.25}$$

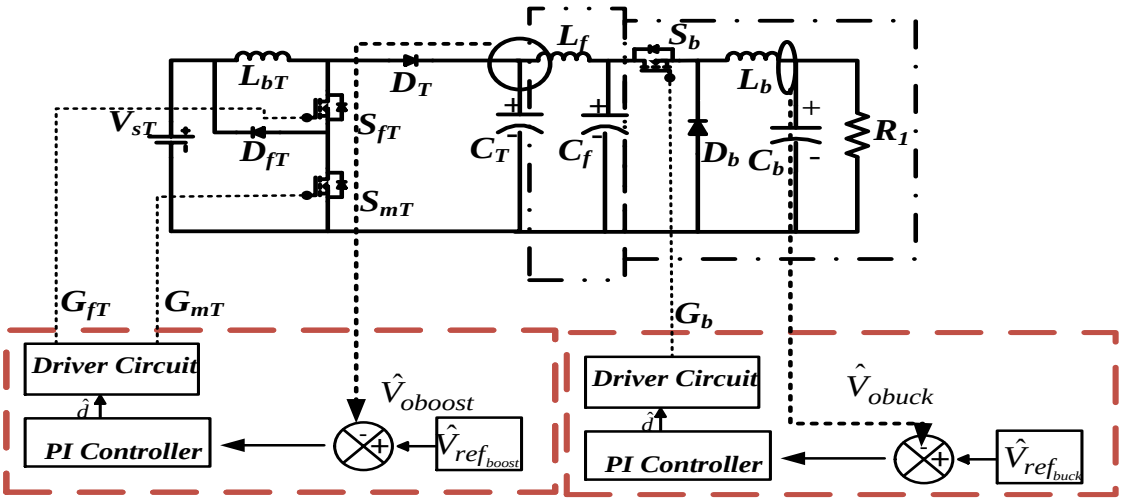


Fig. 4.6. Dual controlled TSB converter using PI controller for CPL.

As explained before, rest of the portion are similar as the portion explained in the chapter related to standard BODC. The closed-loop response is attained using a PI controller and a T2C within a Dual Loop control framework. The system employs two controllers to achieve optimal performance. The Type 2 compensator govern the output voltage error and its output is fed as the reference of the current loop which is maintain by a PI controller which can be served the total purpose of the Dual control loop.

4.4.3 Closed loop control with a constant power load.

This portion have portrayed the TSB converter with a CPL. There is a filtration system which filters out the output of the TSB converter and feeds it to the BUDC which is acting as a CPL. This BUDC is operating under a voltage controlled loop to bring out a stiff output voltage at the end of the BUDC. The CPL is controlled with the use of a PI controller and this is reflected through a driver circuit. The use of a digital circuit is utilized to generate the two different gate signals to trigger both the switch S_f and S_m as shown in the Fig. 4.6. Similar concept is applied to the BUDC converter.

4.5 Result of Tristate Boost converter.

The section shows the steady-state results of the power rating of 25 W TSB converter, emphasizing two distinct phases in the inductor current waveform: a charge stage and a discharging stage. The switch endures voltage stress up to 25 volts. The proportional-integral

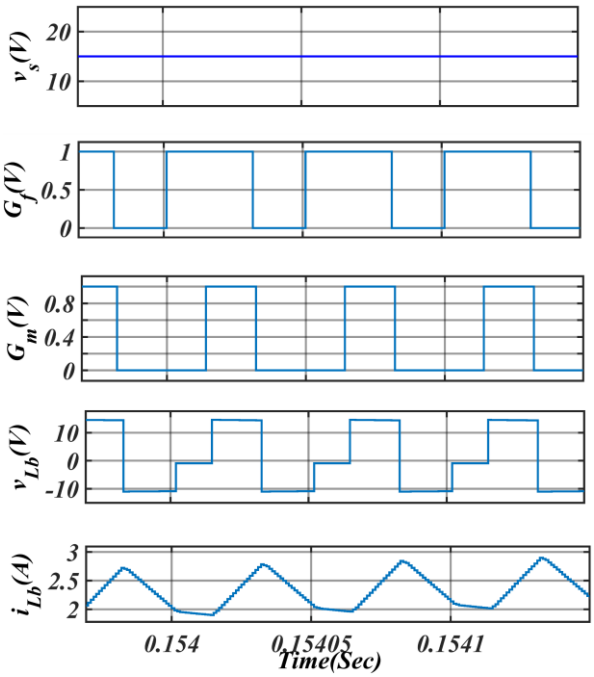


Fig. 4.7(a)

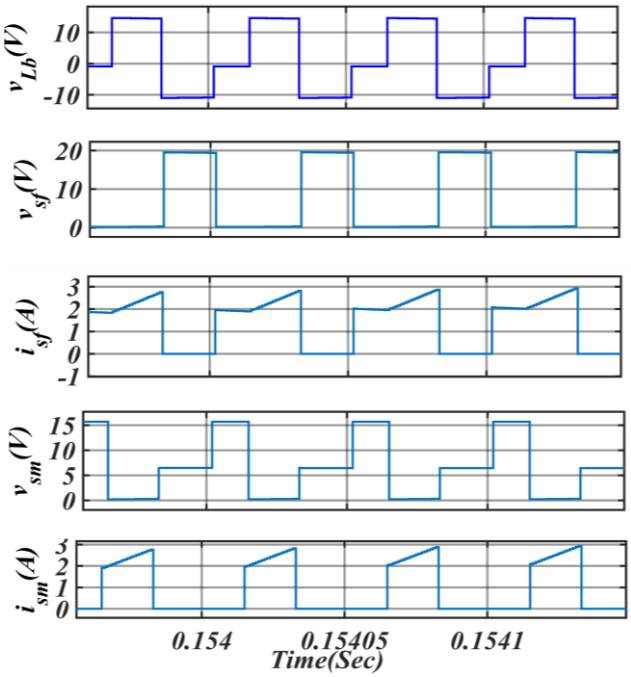


Fig. 4.7(b)

Fig. 4.7 Steady State waveform of (a) $v_s(v)$, $G_f(V)$, $G_m(V)$,$v_{Lb}(V)$, $i_{Lb}(A)$ (b) $v_{Lb}(V)$, $v_{sf}(V)$, $i_{sf}(A)$, $v_{sm}(V)$, $i_{sm}(A)$ in voltage loop controlled TSB converter.

controller is thoroughly calibrated to assure closed-loop operation of the TSB converter, an extensively utilized concept in closed-loop systems. The performance of the TSB is validated

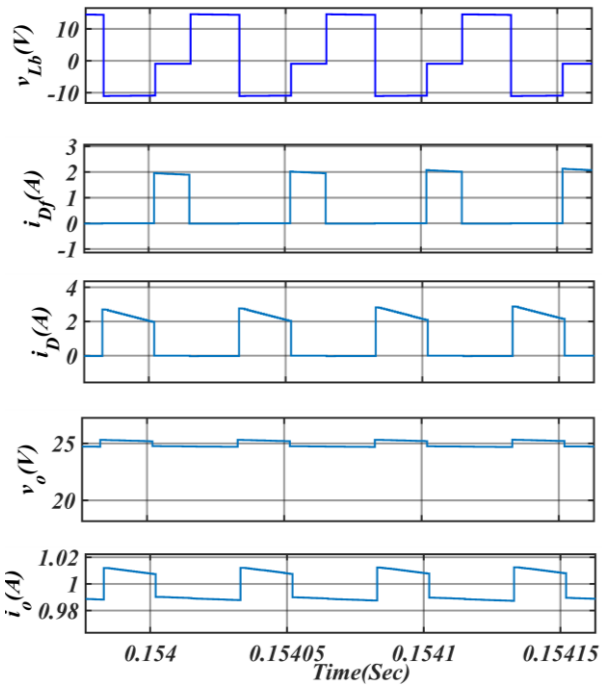


Fig. 4.8(a)

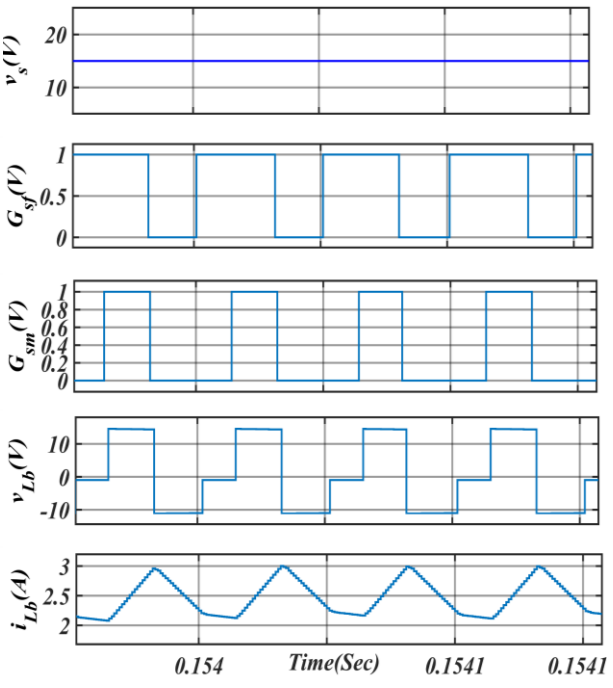


Fig. 4.8(b)

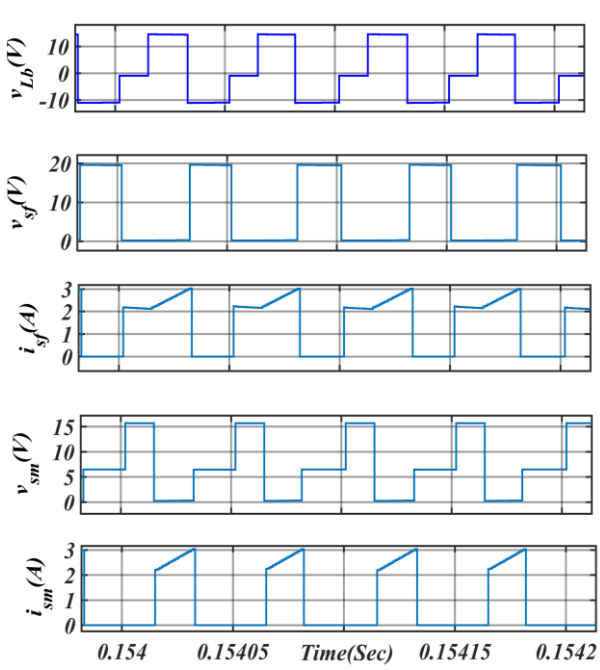


Fig.4.8(c)

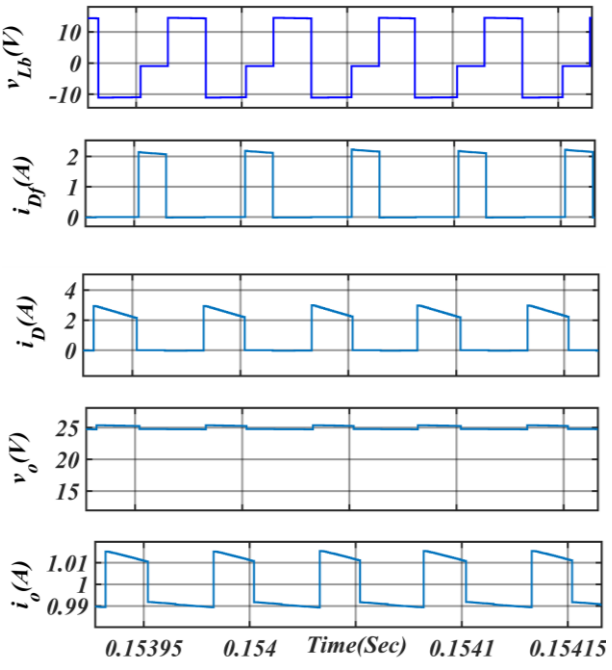


Fig.4.8(d)

Fig. 4.8(a) Steady State waveform of (a) $v_{Lb}(V)$, $i_{Df}(A)$, $i_D(A)$, $v_o(V)$, $i_o(A)$ in voltage loop controlled TSB converter. Steady State waveform of 7 (b) $v_s(v)$, $G_f(V)$, $G_m(V)$,$v_{Lb}(V)$, $i_{Lb}(A)$ (c) $v_{Lb}(V)$, $v_{sf}(V)$, $i_{sf}(A)$, $v_{sm}(V)$, $i_{sm}(A)$ (d) $v_{Lb}(V)$, $i_{Df}(A)$, $i_D(A)$, $v_o(V)$, $i_o(A)$ in dual loop controlled TSB converter.

under both resistive and constant power loads utilizing the PI controller and T2C compensator. The section also goes through the dynamic stage of the TSB converter along with its stability analysis through bode plots and root locus.

4.5.1 Simulation Results of Tristate Boost converter with the PI controller.

In this section, dual loop control which is a combination of current controlled loop and voltage-controlled loop, as well as voltage loop controlled are being portrayed. Fig. 4.7 and 4.8 (a) deals with a standard voltage-controlled TSB converter feeding a resistive load. A stiff supply of 15 volt is being applied to the system. G_f and G_m denotes gate signal given to the switch S_f and S_m respectively. The inductor voltage as well as the inductor current has been captured in the Fig. 4.7(a) and this illustrates the three stages of the charging and discharging of the inductor current. The freewheeling state has the constant inductor current flowing but still there is slight drop in the current flowing through the inductor due to the non ideal property of the inductor. In the Fig. 4.7(b), it can be observed that voltage stress of the switches is reduced. It is also within a specified limit. As shown in Fig 4.7(b), the switch S_f make the voltage stress up to 20 V and for the switch S_m, it reaches up to 15 V. The Fig. 4.8(a) depicts the waveform of the current of the both the diodes, D_f and D. The steady state waveform of the output voltage along with the output current can be portrayed in the Fig. 4.8(a). It shows that the ripple percentage of the voltage is quiet less and ideal for low powered application. The Fig 4.8(b), (c) and (d) are results of the TSB converter which is under the dual loop control concept where the feedback from the output voltage along with

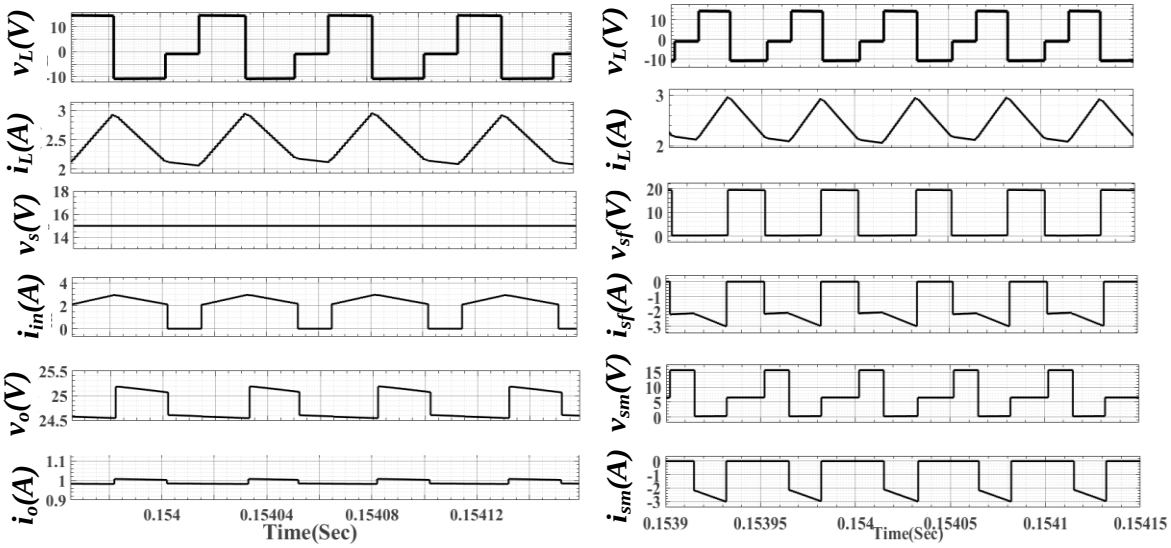


Fig. 4.9(a) Fig. 4.9(b)

Fig. 4.9 Steady State Performance parameter: a) v_L, i_L, v_s, i_{in}, v_o, i_o b) v_L, i_L, v_{sf}, i_{sf}, v_{sm}, i_{sm}.

inductor current are taken. It can be observed that the results replicate the system with a standard voltage loop control in it but the dual loop control gives an advantage of faster response over a standard voltage loop control.

4.5.2 Simulation Results of Tristate Boost converter with the Type 2 compensator.

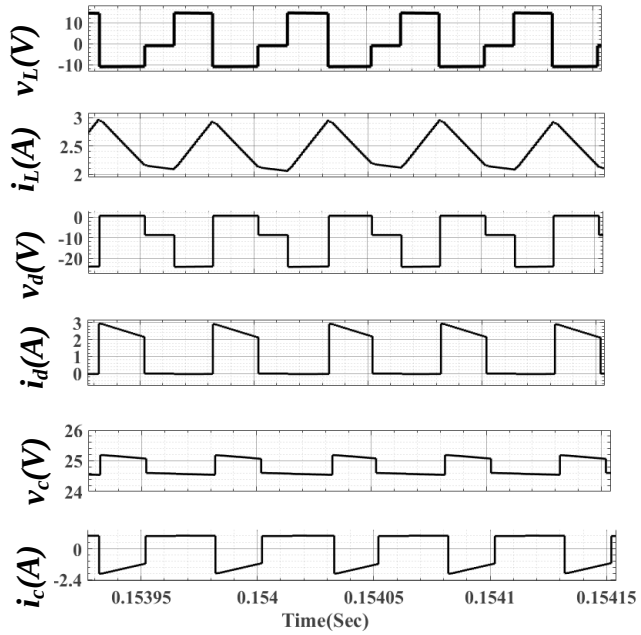


Fig 4.10: Steady Performance parameter: v_L, i_L, v_d, i_d, v_c, i_c

A system with a power rating of 25 W for the TSB converter can be portrayed and evaluated using MATLAB/Simulink. It demonstrates that the ripple percentage of the voltage is quiet less and optimal for low powered application. The period which portrays the freewheeling of the inductor current exhibits a minor decline, indicative of a non-ideal system. The output voltage dispersion can be approximated 0.7 V. Figure 4.9(b) demonstrates that the voltage stress on the switches decreases and remains within specified limits. Specifically, the voltage stress on switch S_f rises up to 20 V, while for switch S_m, it goes up to 15. All values remain within permissible limits, accurately delineating the properties of the TSB DC-DC converter. Additionally, the load current (i_o) organised within the specified bandwidth, after facing of abrupt voltage variations.

4.5.3 Simulation Results of Tristate Boost converter with PI controller for a Constant power load.

This section exhibits the results of the TSB DC-DC converter coupled with a 50 W BUDC converter system. The analysis is validated utilizing MATLAB/Simulink. The BUDC functions as a constant power supply. Figure 4.11(a) illustrates the TSB's inductor voltage (v_{L1}), inductor current (i_{L1}), input voltage (v_s), input current (i_s), output voltage (v_{oT}), and output current (i_{oT}). This illustrates the three stages of the charging and discharging of the inductor current. The freewheeling state has the constant inductor current flowing but still there is slight drop in the current flowing through the inductor due to the non ideal property of the inductor. It shows that the ripple percentage of the voltage is quiet less and ideal for low powered application. Figure 4.11(b) shows the waveforms of the BUDC converter's inductor current (i_b), output current (i_{ob}), and output voltage (v_{ob}), along with the TSB converter's diode current (i_{dft}). Figure 4.12 details the inductor voltage (v_{Lb}) of the BUDC converter, input power (P_{in}), output power of the TSB converter, and output power of the active load. The results confirm that the TSB converter is appropriate for operating with a CIL load, demonstrated here by the BUDC converter.

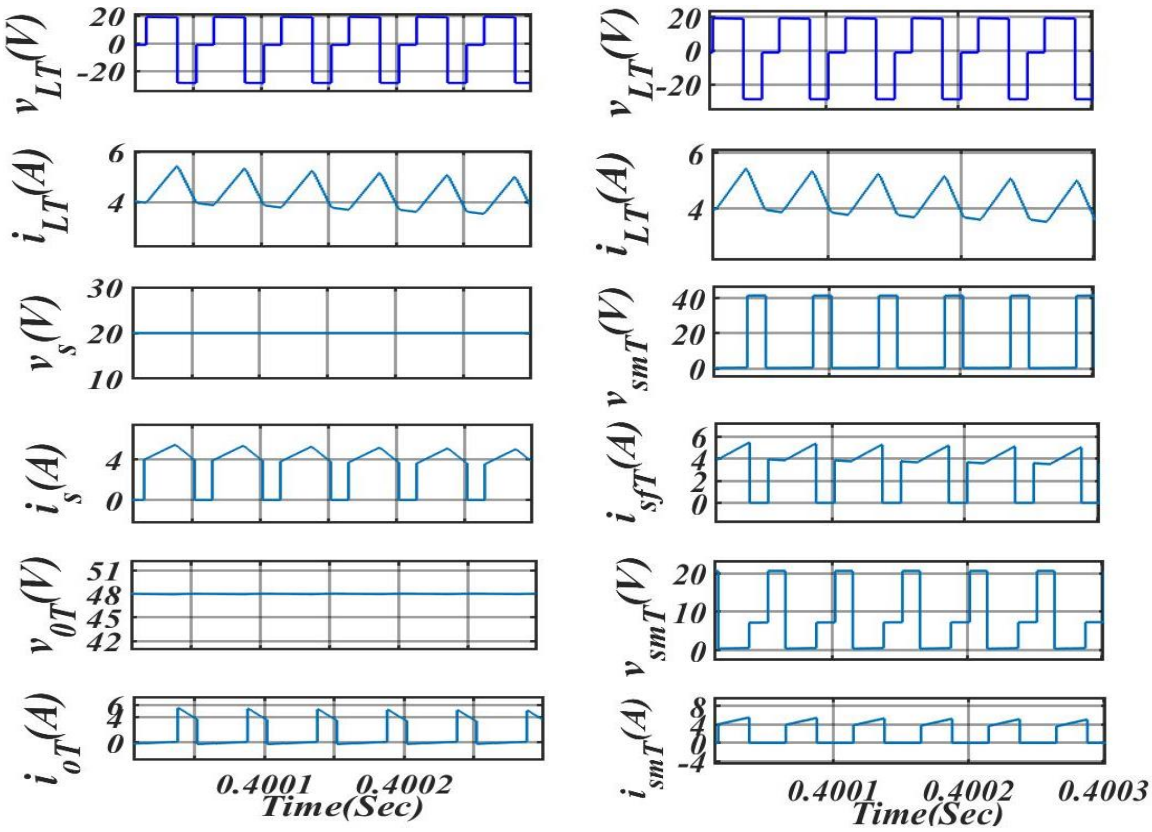


Fig. 4.11(a) Fig.4.11(b)

Fig.4.11 a) Steady State result of $v_{LT}(V)$, $i_{LT}(A)$, $v_s(V)$, $i_s,(A)$, $v_{oT}(V)$, $i_{oT}(A)$, *b)* $v_{LT}(V)$, $i_{LT}(A)$, $v_{ob}(V)$, $i_{ob}(A)$, $i_{dfT}(A)$, $i_{Lb}(A)$

4.5.4 Simulation Results of Transient analysis of Tristate Boost converter with the Type 2 compensator.

This section portrays the results of TSB converter under T2C compensator in a dynamic state change. Fig 4.13(a) depicts the sudden increase in the supply voltage by 5 volt which means it was 15 volts but now it became 20 volts. The variation in load current, input current and inductor voltage are demonstrated in the Fig. 4.13 (a) and it was also able to recover its nature quietly fast. It was also able to restricts the current and the voltage level. The output voltage was within a certain limit while maintaining its stability. A similar thing can be expressed with the Fig. 4.13 (b) where there is a sudden decrease in voltage.

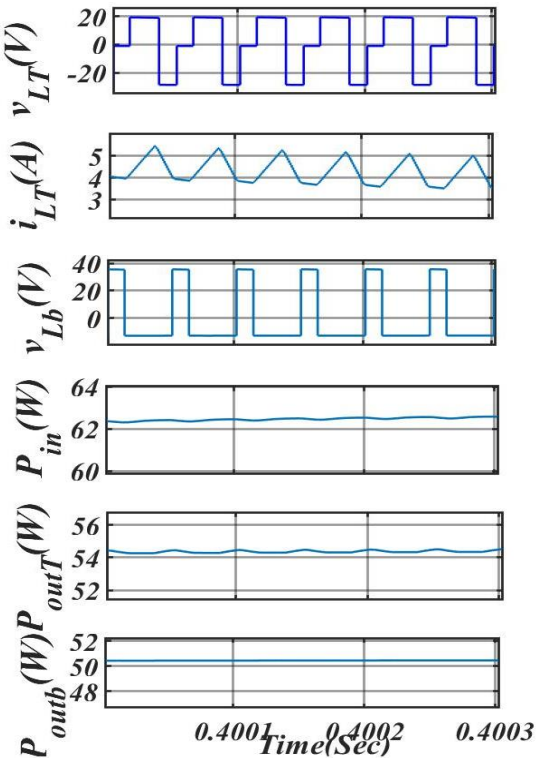


Fig.4.12 Steady State result of $v_{LT}(V)$, $i_{LT}(A)$, $v_{Lb}(V)$, $P_{in}(W)$, $P_{outT}(W)$, $P_{outb}(W)$

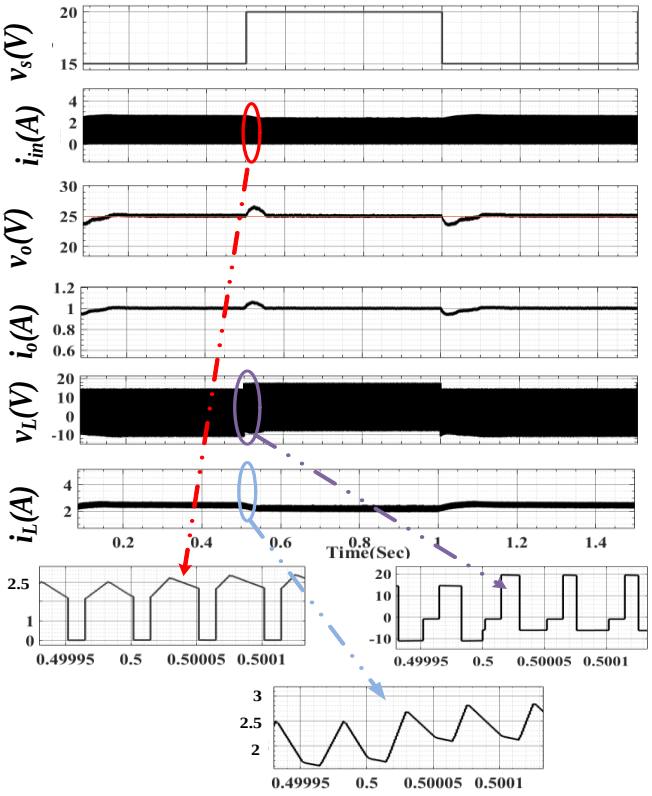


Fig. 4.13 (a)

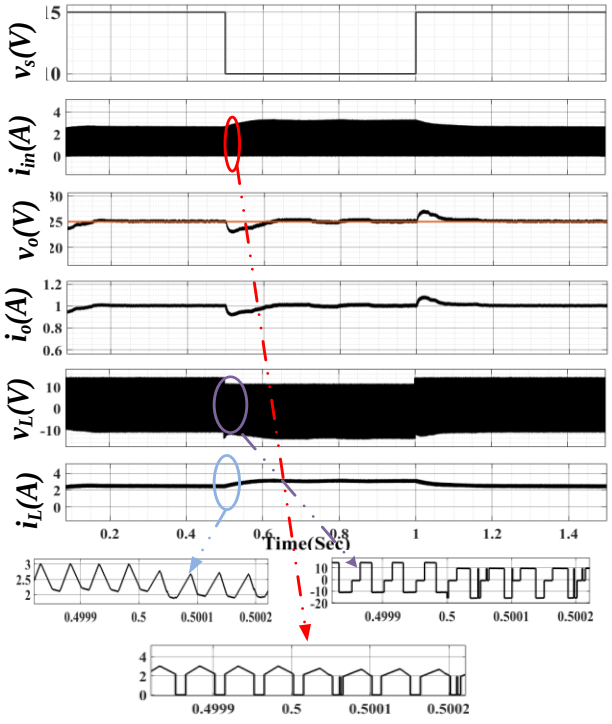


Fig. 4.13 (b)

Fig 4.13 Transients performance parameters (V_L, I_L,V_s, I_{in}, V_o, I_o) when there is a variation in supply which is considered (a) starting from 15 to 10 V and (b) starting from 15 to 20 V.

4.5.5 Stability analysis of Transient analysis of Tristate Boost converter with the Type 2 compensator.

Closed-loop analysis in power electronics, utilizing root locus and Bode plot techniques, is vital for enhancing system stability and performance. Root locus analysis provides insights into the system's pole-zero configuration along with dynamic response, steering the design

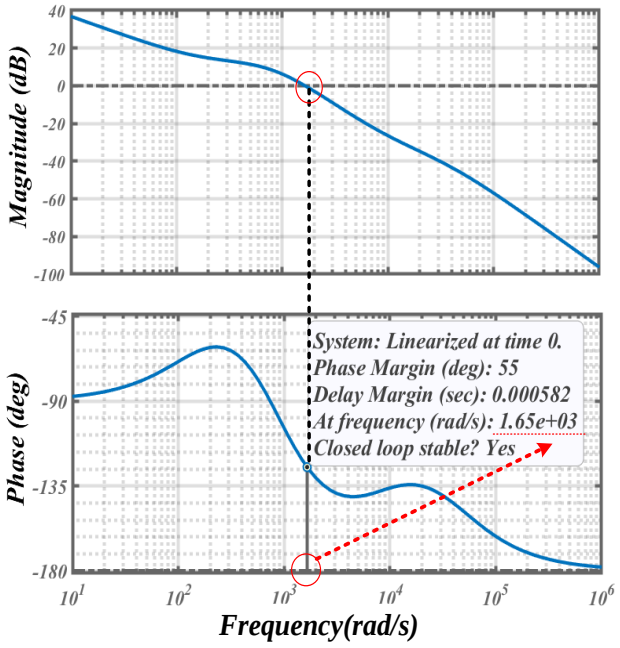


Fig. 4.14 (a)

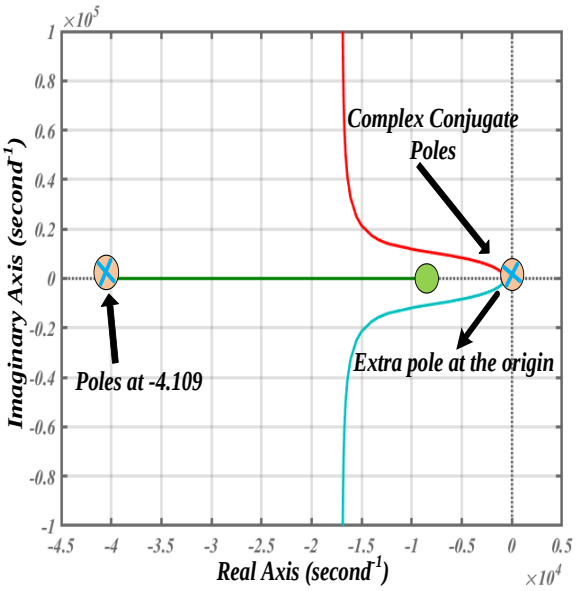


Fig. 4.14(b)

Fig 4.14. Bode plot and root locus of T2C compensated TSB Converter.

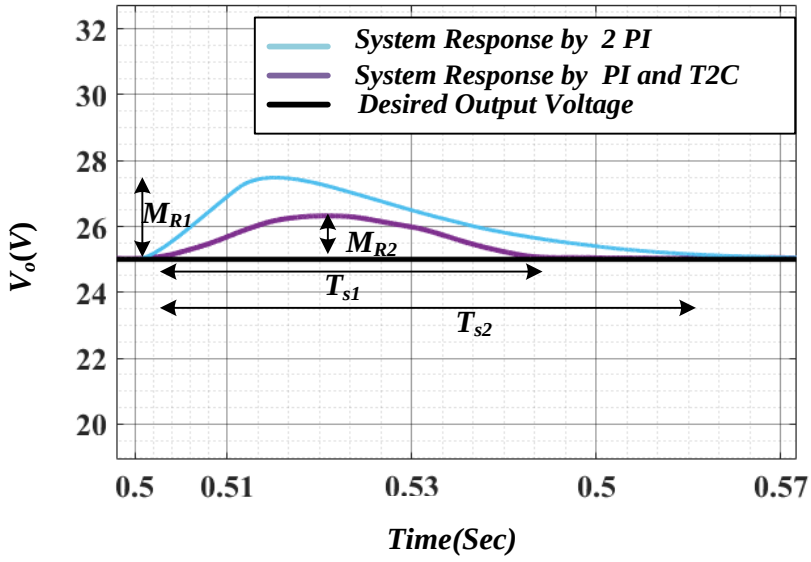


Fig. 4.15 Dynamic response of TSB converter when there is a change of 15 to 20 V

of robust controllers. Bode diagrams offer a frequency domain perspective, illustrating gain as well as phase margins, which are crucial for stability assessment and control system adjustment. In this Fig. 4.14(a), it can be bringing the clarification about the criteria of the stability of TSB converter where the bode plot is lifted up the PM of the overall system by attaching T2C compensator which has an extra pole at the origin as shown the Fig 4.14(b). The root locus of the overall system portrays the additional pole due to which it boosts up the PM of the system. The PM of the system is 55º according to the bode plot of the overall system which signifies that it is closed loop stable. The concerning matter is the speed of the system, by the application of T2C compensator, a trade off was made with the cross over and the phase boost that it is needed. The root locus also shows that all poles and the zeroes are in the right half of the S-plane and this means that it is completely stable by its nature. Another aspect has been present here through the Fig. 4.15. This figure denotes the desired output voltage, system with PI and T2C and system along with 2 PI controller placed in a dual loop concept. The observation can be how the PI and T2C is better than two PI controller in terms of the percentage overshoot denoted as M_{R1} and M_{R2} with respect to two PI controlled system and PI with T2C respectively as well as settling time which is denoted by T_{s1} and T_{s2}. T_{s1} is for a combination of PI controller and T2C compensator and T_{s2} is for two PI controlled in dual loop configuration.

4.6 Conclusion

This chapter elucidates the concepts related to the TSB converter through four sections. The second section presents the steady-state modelling of the TSB, including the output voltage equation. The small signal modelling, integrating the effects of Equivalent Series Resistance (ESR), is detailed in the corresponding section. The TSB is analyzed under two categories of controllers, the PI controller and the T2C, with both resistive and constant power loads considered. This section provides results of the TSB's efficacy under various conditions and controllers. Additionally, the chapter explains the TSB's capability to manage constant power demands, specifically within a BUDC. Through the portion related to stability analysis, it has been portraying the superiority of the TSB over a standard BODC and even with TSB converter govern by PI controller. The one thing which is triggered and does not fit the TSB converter is the steady state output voltage gain but this has been covered in the later chapter through high gain tristate converter.

Chapter 5

ANALYSIS OF DUAL OUTPUT TRISTATE BOOST CONVERTER

5.1 Introduction.

The 48-V DC link helps maintain consistent voltage levels within the microgrid, which is essential for assuring the reliable and continuous operation of connected components and apparatus. The TSB converter satisfies the requirement for a stable voltage profile by eradicating the RHP zero characteristic inherent in a standard boost converter. The prevalence of the RHP zero. The non-isolated DC-DC Single Input Dual Output architecture was developed to provide both step-up and step-down outputs from a single DC input.

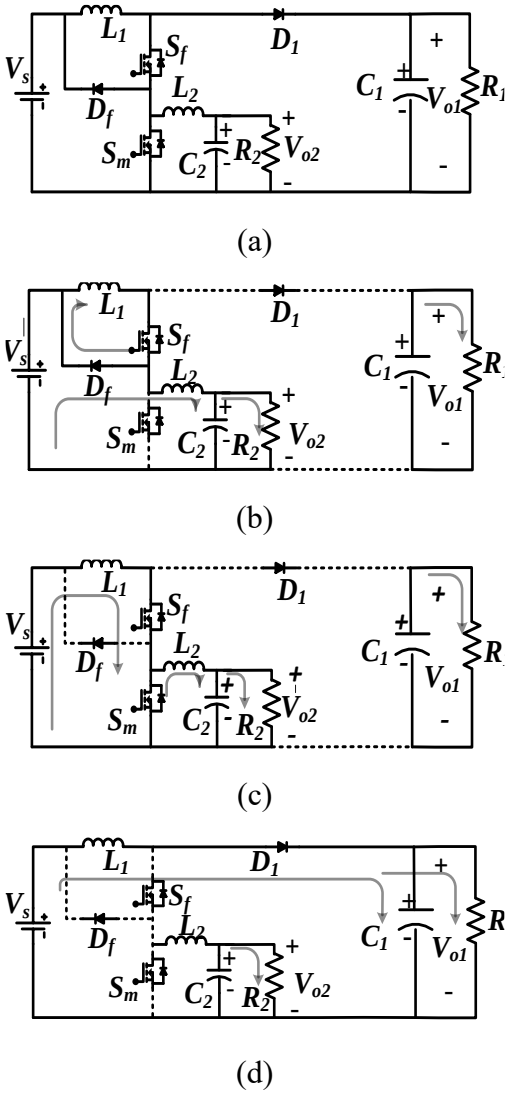


Fig. 5.1 Circuit schematic of DOTSB converter besides the modes (a) Circuit schematic of DOTSB converter (b) operation in Mode-I operation executing in DOTSB converter (c) operating in Mode II in DOTSB converter (d) operation in Mode III executing in DOTSB converter.

Additional outputs can be produced using a low-pass filter network. Notably, the attained step-up and step-down outputs are comparable to those obtained by distinct BODC and BUDC converters, respectively.

5.2 Modelling of Dual output Tristate Boost Converter

This section presents the whole modelling related to the DOTSB converter, incorporating all modes of operation. Figure 5.1(a) illustrates the fundamental circuit of the DOTSB converter, while Figures 5.1(b), 5.1(c), and 5.1(d) display its three distinct operational stages. In Mode I, the main TSB is in the freewheeling state, with inductor L_1 freewheeling through diode D_f and supply voltage V_s applied directly across switch S_m. In Mode II, inductor L_1 charges while inductor L_2 discharges across the second output port. In Mode III where the switches S_f and S_m both are not-function, along with the diode D_1 is turned on by nature. During this mode, the inductor current I_{L1} can be decreased as power conveying to the load, capacitor C_1 is replenished, and capacitor C_2 discharges through R_2. The mathematical expressions at steady state conduction for the voltage V_{L1} across inductor L_1, the current i_{C1} through capacitor C_1, the voltage V_{L2} across inductor L_2, and the current i_{C2} through capacitor C_2 can be presented as follows.

This represents the first mode of the DOTSB converter, analogous to the freewheeling (D_{fT}) interval. During this interval, switch S_f is on while switch S_m is off. The corresponding equations are provided below:

$$V_{L1} = 0 \quad [5.1]$$

$$i_{c1} = -\frac{V_{o1}}{R_{o1}} \quad [5.2]$$

$$V_{L2} = V_s - V_{o2} \quad [5.3]$$

$$i_{c2} = i_{L2} - \frac{V_{o2}}{R_{o2}} \quad [5.4]$$

This is the charging state, where both switches S_f and S_m are conducting. The corresponding equations are provided below:

$$V_{L1} = V_s \quad [5.5]$$

$$i_{c1} = -\frac{V_{o1}}{R_{o1}} \quad [5.6]$$

$$V_{L2} = -V_{o2} \quad [5.7]$$

$$i_{c2} = i_{L1} - \frac{V_{o2}}{R_{o2}} \quad [5.8]$$

This is the discharging state. The corresponding equations are provided below:

$$V_{L1} = V_s - V_{o1} \quad [5.9]$$

$$i_{c1} = i_{L1} - \frac{V_{o1}}{R_{o1}} \quad [5.10]$$

$$V_{L2} = 0 \quad [5.11]$$

$$i_{c2} = -\frac{V_{o2}}{R_{o2}} \quad [5.12]$$

Where V_{o2} is the output voltage across the resistance R_1.

Here the Voltage balance equation is being utilized:

$$\left[V_{L1_f} \times D_f\right] + \left[V_{L1_b} \times D_b\right] + \left[V_{L1_o} \times D_o\right] = 0 \quad [5.13]$$

$$\left[0 \times D_f\right] + \left[V_{in} \times D_b\right] + \left[\left(V_{in} - V_{o1}\right) \times D_o\right] = 0 \quad [5.14]$$

The boost output voltage is expressed as,

$$V_{o1} = V_{in}\left(\frac{D_b}{D_o} + 1\right) \quad [5.15]$$

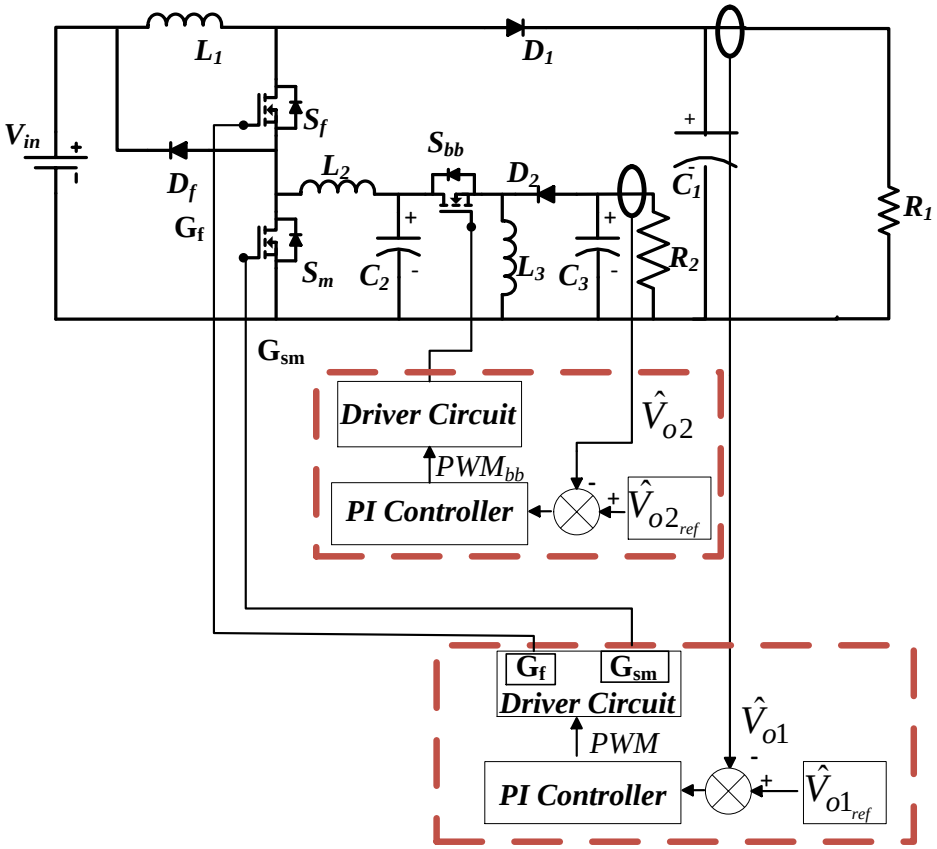


Fig. 5.2 DOTSB converter with resistive load.

$$\left[V_{L2_f} \times D_f\right] + \left[V_{L2_b} \times D_b\right] + \left[V_{L2_o} \times D_o\right] = 0 \quad [5.16]$$

$$\left[(V_{in} - V_{o2}) \times D_f\right] + \left[-V_{o2} \times D_b\right] + \left[0 \times D_o\right] = 0 \quad [5.17]$$

The buck output voltage is expressed as,

$$V_{o2} = V_{in}\left(\frac{D_f}{D_b + D_f}\right) \quad [5.18]$$

5.3 Control system of Dual output Tristate Boost Converter

Closed-loop control is critically important for achieving smooth voltage regulation and enhancing the system's dynamic response. This closed-loop response is facilitated by a PI controller. As there are two ports, the auxiliary port which delivers buck output is control using a standard BBODC converter. There are two loads tested on this converter, first one is a standard resistive load and another one is a CPL.

5.3.1 Control strategy for Dual output Tristate Boost Converter with a resistive load.

This portion deals with a standard resistive type of load. The auxiliary port which delivers buck output is control using a standard BBODC. As depicted in the Fig 5.2, both ports are governed under voltage loop control to maintain the output voltage. The output voltage of the main port sensed, compared to the reference value. This is passed to the PI controller which gives an output as duty cycle to the driver circuit which gives two gate signals for the two individual switches. Similarly, it is for the auxiliary port which gives the signal to the switch of the BBODC converter.

5.3.2 Control strategy for Dual output Tristate Boost Converter with a CPL.

The term CPL can be used for a power electronic converter with a controlled output. Here CPL is framed through a voltage controlled BUDC. Figure 5.6 exhibits the control strategy of the TSB converter, with the circuit governed by a voltage-controlled loop. State-space averaging and linearization techniques are employed to derive the control-to-output transfer

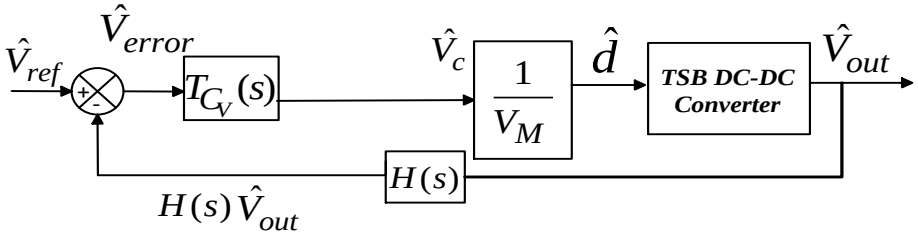


Fig. 5.3. Control Schematics of TSB Converter

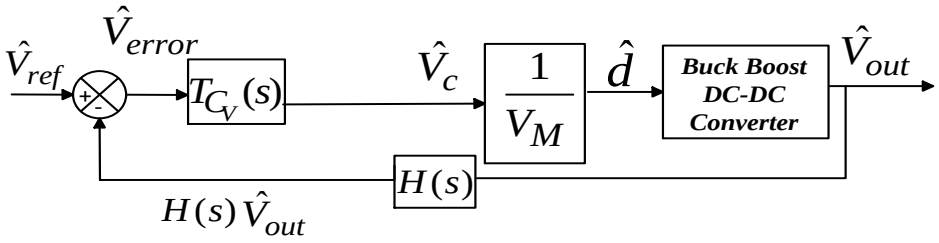


Fig. 5.4. Control Schematics of BBODC Converter

function for the TSB converter with respect to duty cycle of charging function is expressed as:

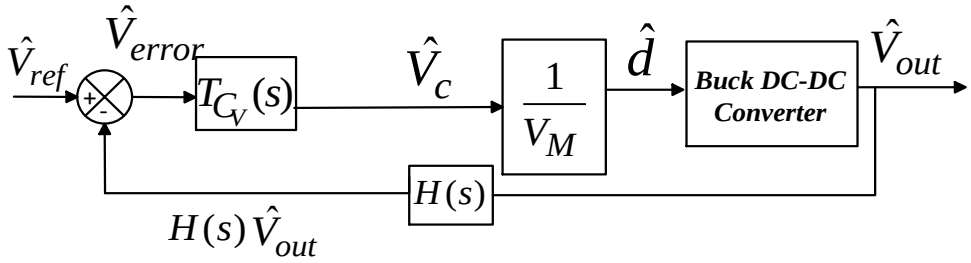


Fig. 5.5. Control Schematics of CPL load

$$\frac{V_o(s)}{D_b(s)} = \frac{V_o}{D_o} \frac{1}{s^2 \frac{LC}{D_o^2} + s\frac{L}{RD_o^2} + 1} \quad [5.19]$$

The BBODC converter is utilized to regulate the auxiliary port, capable of either boosting or bucking the voltage as needed. The transfer function is provided below:

$$\frac{V_o(s)}{d(s)} = \frac{\frac{sLV_o}{RD'} - D'(V_g - V_o)}{s^2LC + \frac{L}{R}s + (D')^2} \quad [5.20]$$

The voltage-controlled loop maintains the stability of the output voltage of the BUDC converter. The transfer function of the BUDC converter is provided below:

$$\frac{V_o(s)}{d(s)} = \frac{RV_g}{s^2LCR + Ls + R} \qquad [5.21]$$

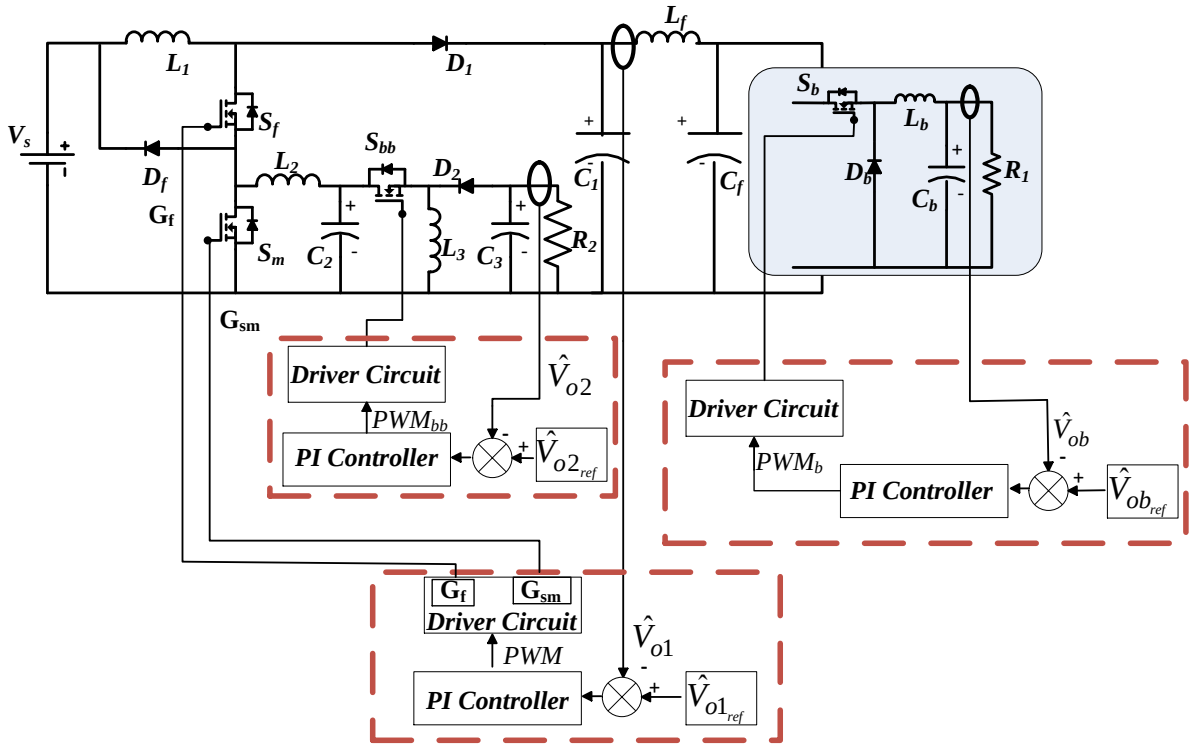


Fig. 5.6 DOTSB converter with active load.

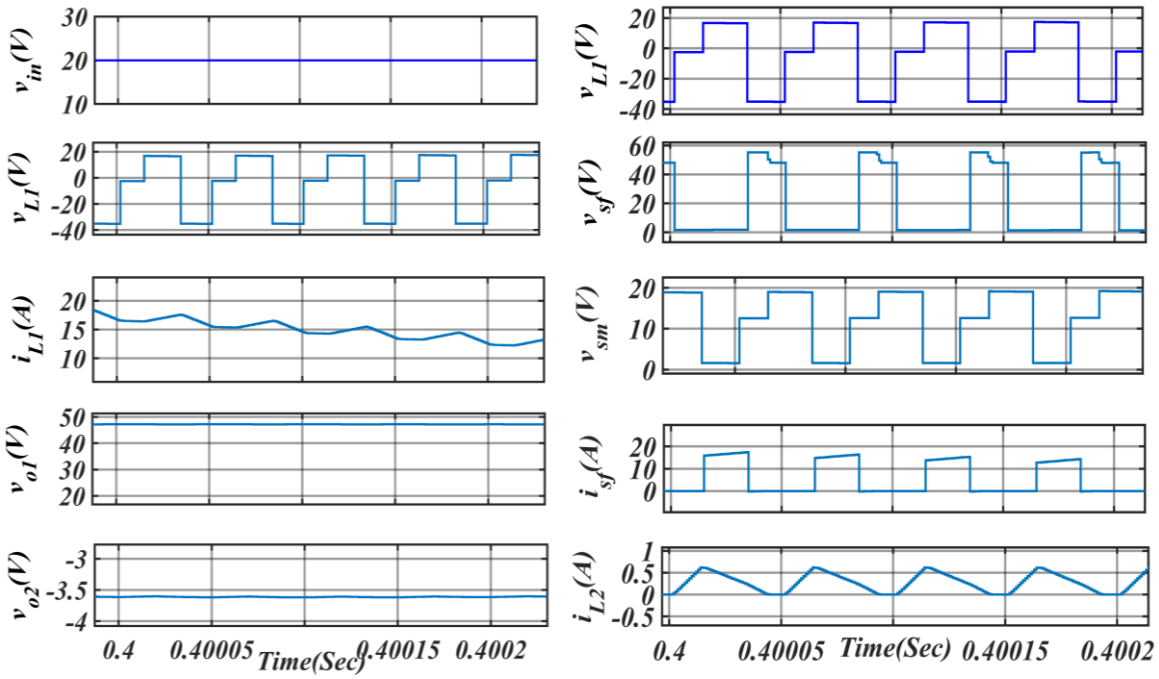


Fig. 5.7(a) Fig. 5.7(b)

Fig. 5.7 Waveform of (a) $v_{in}(V)$, $v_{L1}(V)$, $i_{L1}(A)$,$v_{o1}(V)$,$v_{o2}(V)$; (b) $v_{L1}(V)$,$v_{sf}(V)$,$v_{sm}(V)$, $i_{sf}(A)$,$i_{L2}(A)$

5.4 Result of Dual output tristate boost converter

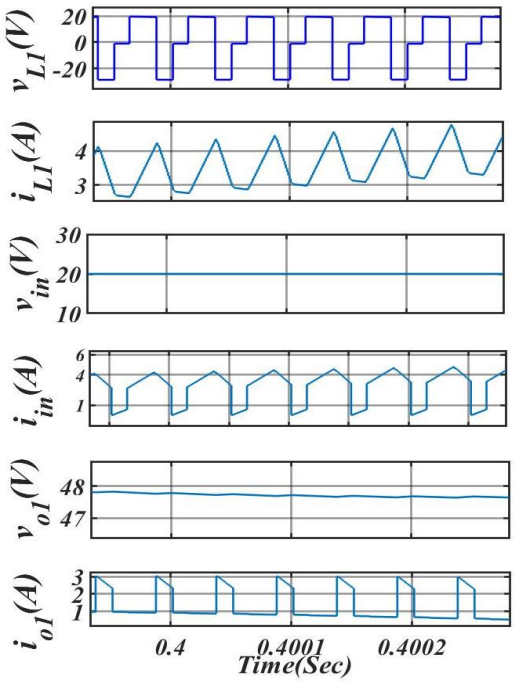


Fig. 5.8(a)

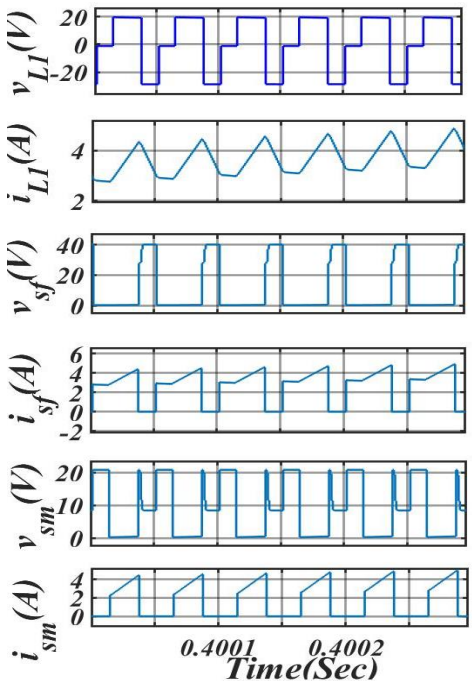


Fig. 5.8(b)

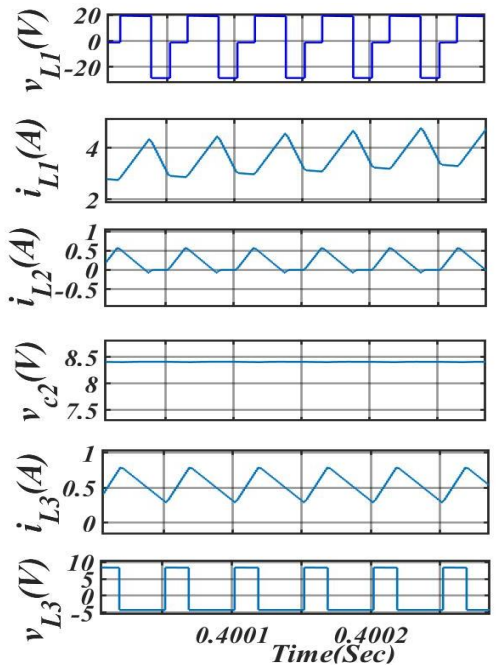


Fig.5.8(c)

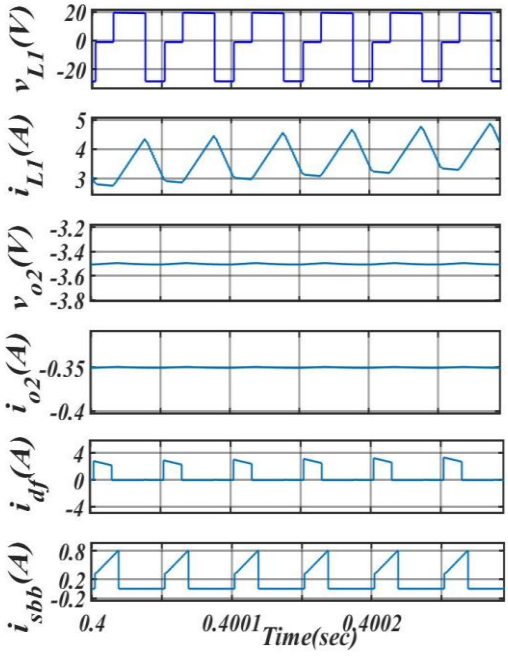


Fig.5.8(d)

Fig.5.8 Waveform of (a) $v_{L1}(V)$, $i_{L1}(A)$,$v_{in}(V)$, $i_{in}(A)$, $v_{o1}(V)$, $i_{o1}(A)$ b) $v_{L1}(V)$, $i_{L1}(A)$, v_{sf}, (V), $i_{sf}(A)$, $v_{sm}(V)$, $i_{sm}(A)$.c) $v_{L1}(V)$, $i_{L1}(A)$, $i_{L2}(A)$, $v_{c2}(V)$, $v_{L3}(V)$, $i_{L3}(A)$ d) $v_{L1}(V)$, $i_{L1}(A)$, $v_{o2}(V)$, $i_{o2}(A)$, $i_{df}(A)$, $i_{sbb}(A)$

In this section, there are two types of loads considered, first one is with a standard resistive load and the second one is with a CPL. The DOTSB converter is connected in parallel with TSB converter feeding a CPL, to show the compatibility along with other converters.

5.4.1 Simulation Result of Dual output tristate boost converter with a resistive load.

Fig. 5.7(a) and 5.7(b) denotes the performances of the DOTSB converter with a resistive load. The input voltage of 20 volts has been applied. It can be seen that the inductor L_1 exhibits the same property of a standard TSB DC DC converter. There are three stages in it, one is the freewheeling state where the inductor L_1 freewheeling its charge, charging stage and the discharging stage of the inductor L_1. A stiff output voltage at both the ports are preserved. In Fig 5.7(b), the waveform of the switches S_f and S_m are shown and the nature of the switch stays with the limits. The current which is entering the auxiliary port is also depicted in the Fig. 5.7(b).

5.4.2 Simulation Result of Dual output tristate boost converter with a Constant power load.

A simulation of the DOTSB converter is conducted with a supply voltage of 20V, resulting in an output voltage of 48V. The inductor voltage (v_{L1}) along with inductor current (i_{L1}) of the DOTSB are depicted in Fig. 5.7(a), demonstrating that the DOTSB converter adheres to the properties of a TSB converter. Figure 5.7(a) also illustrates the waveforms of the supply current (i_{in}) as well as the load current (i_{out}). Figure 5.7(b) displays the waveforms of the

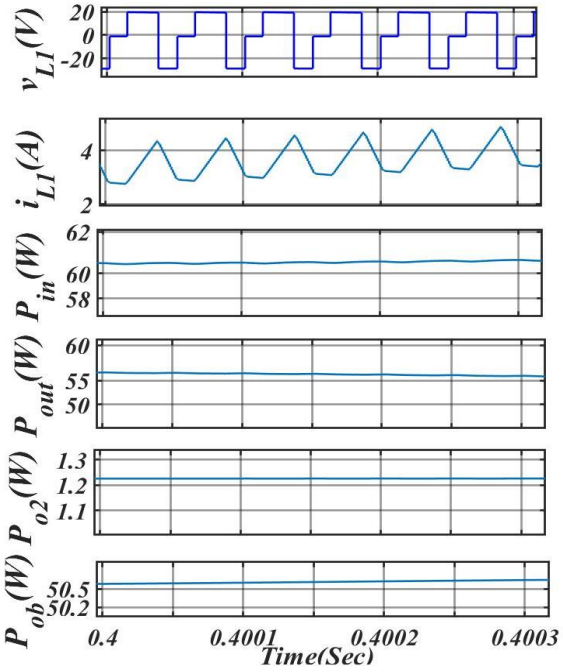


Fig. 5.9 Waveform of $v_{L1}(V)$, $i_{L1}(A)$, $P_{in}(W)$, $P_{out}(W)$, $P_{o2}(W)$, $P_{ob}(W)$.

inductor voltage (v_{L1}), inductor current (i_{L1}), switch voltage of S_f (v_{sf}), switch current of S_f

(i_{sf}), switch voltage of S_m (v_{sm}), and switch current of S_m (i_{sm}). It is observed that the switch ratings is maintained within secure limits.

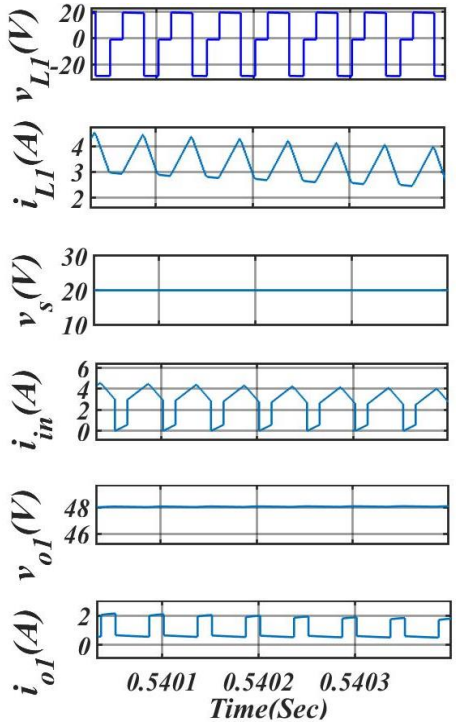


Fig. 5.10(a)

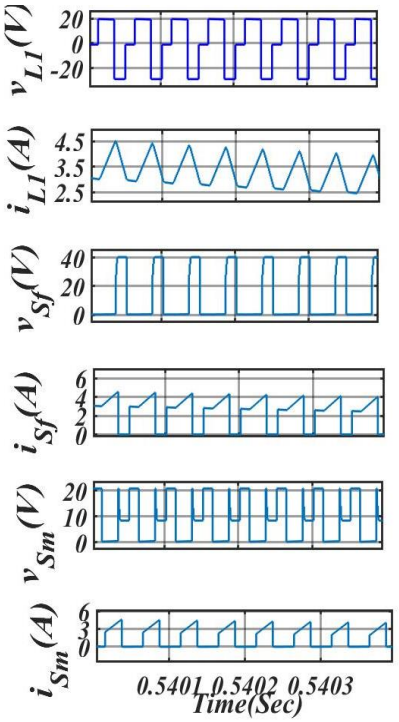


Fig. 5.10(b)

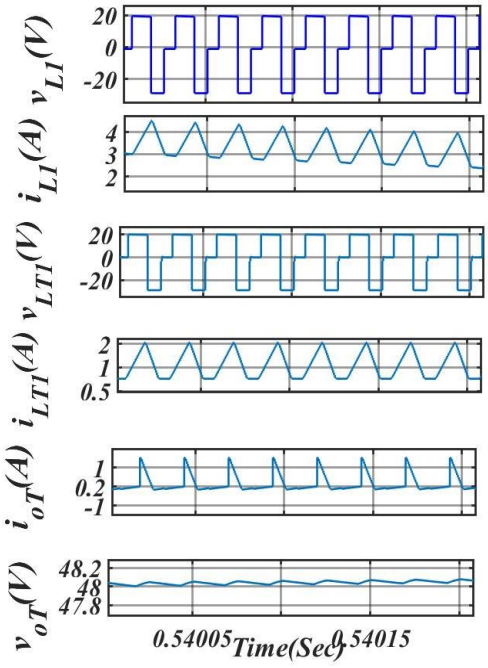


Fig.5.10(c)

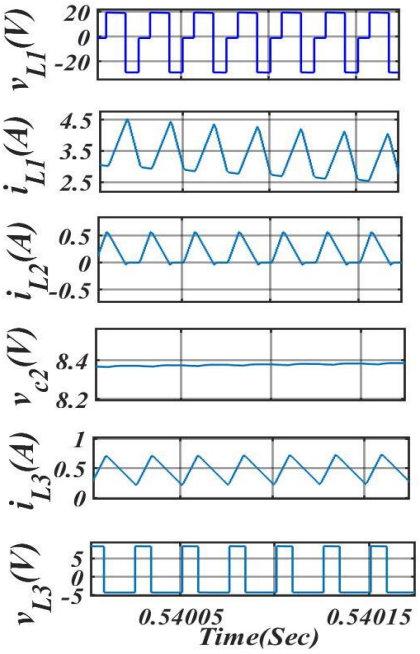


Fig.5.10(d)

Fig. 5.10. Waveform of a) $v_{L1}(V)$, $i_{L1}(A)$, $v_s(V)$, $i_{in}(A)$, $v_{o1}(V)$, $i_{o1}(A)$ b) $v_{L1}(V)$, $i_{L1}(A)$, $v_{sf}(V)$, $i_{sf}(A)$, $v_{sm}(V)$, $i_{sm}(A)$ c) $v_{L1}(V)$, $i_{L1}(A)$, $v_{LTI}(V)$, $i_{LTI}(A)$, $i_{oT}(A)$, $v_{oT}(V)$ d) $v_{L1}(V)$, $i_{L1}(A)$, $i_{L2}(A)$, $v_{c2}(V)$, i_{L3}, $v_{L3}(V)$

Figure 8(a) shows the waveforms of the inductor voltage (v_{L1}), inductor current (i_{L1}), voltage

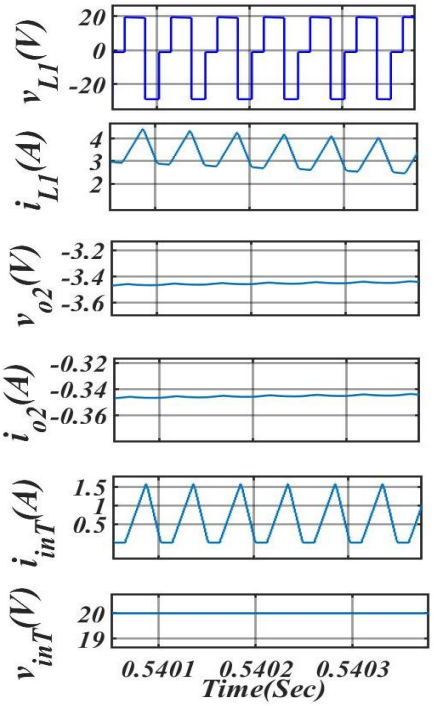


Fig.5.11(a)

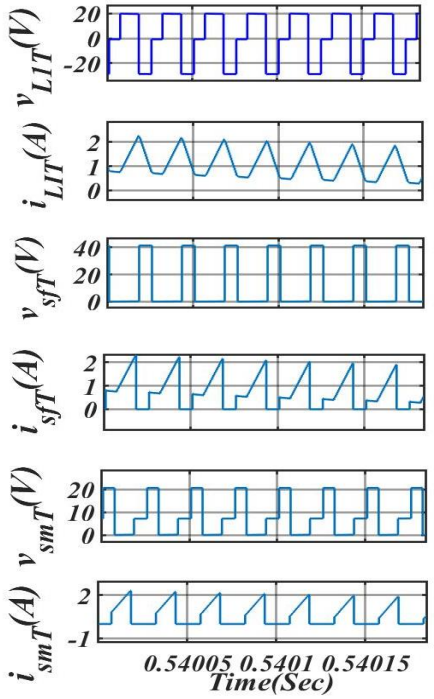


Fig.5.11(b)

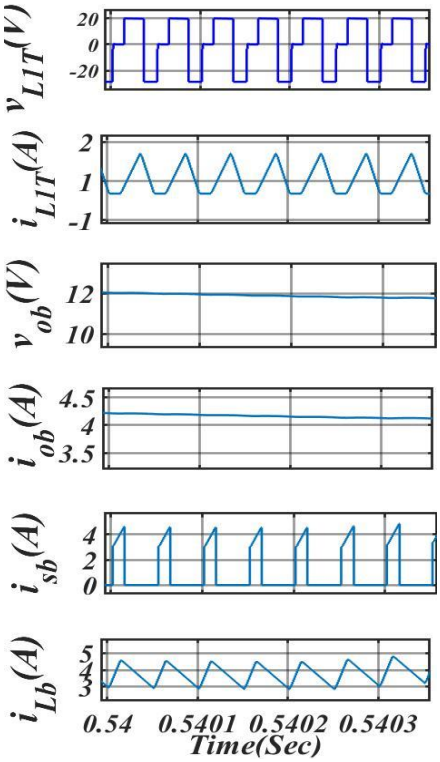


Fig.5.11(c)

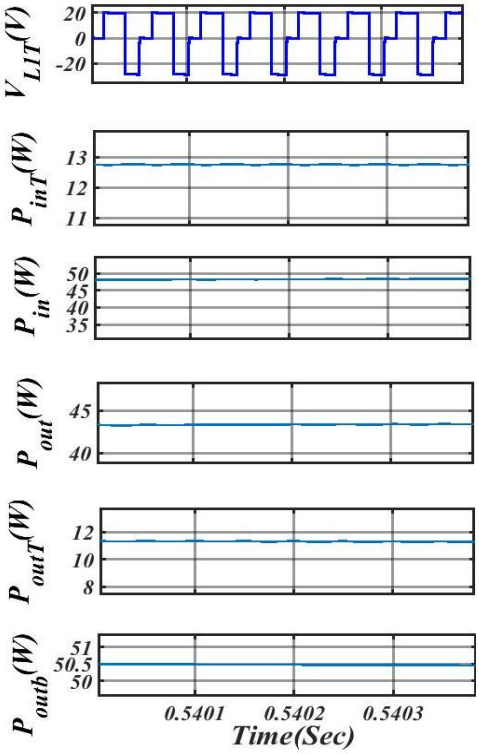


Fig.5.11(d)

Fig. 5.11) Waveform of a)$v_{L1}(V)$, i_{L1}, $v_{o2}(V)$, $i_{o2}(A)$, $v_{int}(V)$, $i_{int}(A)$ b) $v_{L1T}(V)$, $i_{L1T}(A)$, $v_{sfT}(V)$, i_{sfT}, $v_{smT}(V)$, $is_{mT}(A)$ c) $v_{L1T}(V)$, $i_{L1T}(A)$, $v_{ob}(V)$, $i_{ob}(A)$ $v_{sb}(V)$, $i_{sbb}(A)$, $i_{Lb}(A)$ d) $v_{L1T}(V)$, $P_{in}(W)$, $P_{inT}(W)$, $P_{out}(W)$, $P_{outT}(W)$, $P_{outb}(W)$

across the inductor L_2, inductor current I_{L2}, voltage across the auxiliary port capacitance C_2 (V_{c2}), and the voltage (v_{L3}) and current (i_{L3}) of the buck-boost converter governing the auxiliary port voltage. Figure 8(b) portrays the stability of the auxiliary port's output voltage (v_{o2}) and output current (i_{o2}), along with the current through the freewheeling diode (D_f) and the current through the auxiliary port switch (i_{sbb}). Figure 5.8(c) presents the waveforms of the input power (P_{in}), the output power from the DOTSB (P_{out}), the output power from the auxiliary port (P_{o2}), and the power at the output terminal of the buck converter (P_{ob}).

5.4.3 Simulation Result of Dual output tristate boost converter in parallel with Tristate Boost Converter feeding a Constant power load

. The inductor voltage (v_{L1}) as well as inductor current (i_{L1}) of the DOTSB converter are shown in Fig. 5.10(a), demonstrating that the DOTSB converter adheres to the properties of the TSB converter. Figure 5.10(a) demonstrates the waveforms of the input current (i_{in}) and output current (i_{o1}). Figure 5.10(b) presents the waveforms of the inductor voltage (v_{L1}), inductor current (i_{L1}), inductor voltage of the TSB (v_{L1T}), and inductor current of the TSB (i_{L1T}), indicating that both converters exhibit characteristics of an ideal TSB. In Fig. 5.10(c), it is evident that the converter maintains a stable output of 3.5V with a power of 1.12W.

Figure 5.10(d) shows the waveforms of the inductor voltage (v_{L1}), inductor current (i_{L1}), switch voltage of S_f (v_{sf}), switch current of S_f (i_{sf}), switch voltage of S_m (v_{sm}), and switch current of S_m (i_{sm}), confirming that the switch ratings remain inside safe limits. The waveforms of inductor current (i_{L2}), voltage across the auxiliary port capacitance (v_{c2}), voltage across inductor L_3 (v_{L3}), and inductor current (i_{L3}) are depicted in Fig. 5.10(e). Figure 10(f) displays the inductor voltage of the TSB (v_{L1T}), inductor current of the DOTSB (i_{L1T}), switch voltage of S_{fT} (v_{sfT}), switch current of S_{fT} (i_{sfT}), switch voltage of S_{mT} (v_{smT}), and switch current of S_{mT} (i_{smT}), demonstrating that v_{L3} and i_{L3} exhibit the behaviour characteristic of a BBUDC converter. Figure 11(a) displays the waveforms of the voltage across the switch of the active load (v_{sb}), the current through the switch of the active load (i_{sb}), the voltage across the inductor of the active load (v_{Lb}), and the current through the inductor of the active load (i_{Lb}). Figure 5.11(b) illustrates the power sharing between the converters, where P_{inT} embodies the input power of the DC-DC TSB converter, P_{in} reflects the input power of the

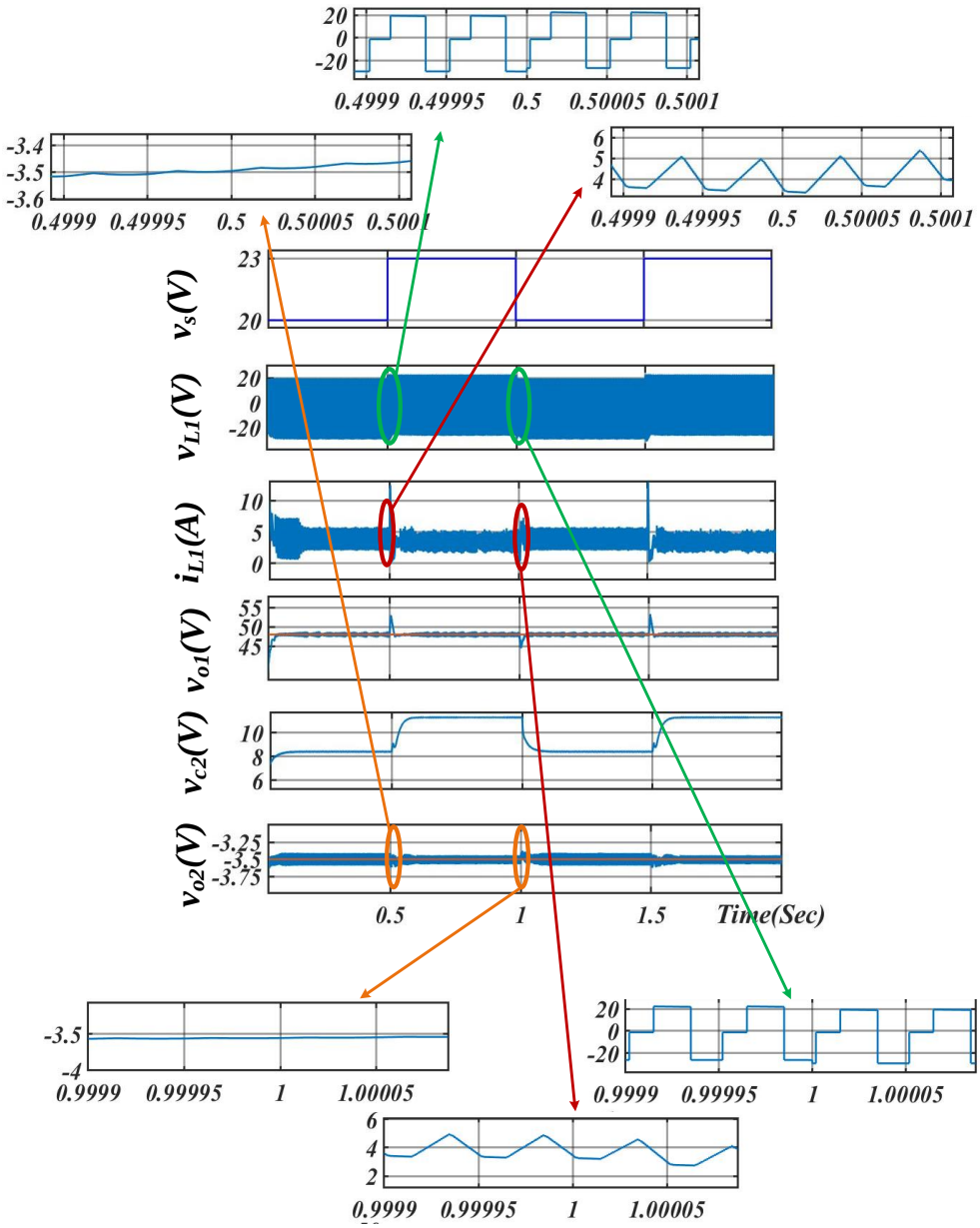


Fig. 5.12. Dynamic State performance parameters ($v_S(V)$, $v_{L1}(V)$, $i_L(A)$, $v_{o1}(V)$, $v_{C2}(V)$, $v_{o2}(V)$) when there is a variation in input starting from 20 to 23 V.

DC-DC DOTSB converter, P_{out} reflects the output power of the DC-DC DOTSB converter, P_{outT} symbolizes the output power of the DC-DC TSB converter, and P_{outb} represents the output power of the active load.

5.4.4 Simulation Result of transient state analysis of Dual Tristate Boost Converter feeding a Constant power load.

This section demonstrates the transient state results of the DOTSB converter when the input voltage goes up by 3 volts. Figure 5.12 depicts the waveforms of the supply voltage (v_S), inductor voltage of L_1 (v_{L1}), inductor current of L_1 (i_{L1}), output voltage of the DOTSB

converter (v_{o1}), voltage across the auxiliary port capacitance (v_{C2}), and output voltage of the auxiliary port (v_{o2}). Despite the variation in supply voltage, the features of the TSB converter are maintained.

5.5 Conclusion

The chapter develop an idea of the multiport concept in TSB converter. The main port contributes to boost output voltage and the auxiliary port gives a buck mode output. The main output port poses the property of TSB converter. The performance of the DOTSB is evaluated by driving a resistive or an active load. DOTSB converter has evaluated alongside TSB converter in parallel combination, to prove its resilience. The dynamic state performance by increasing the supply by 3 volts, is checked and it is bringing a satisfactory result. The simplicity of the control is a highlight of DOTSB converter. The auxiliary port is controlled through a voltage controlled BBODC converter. The voltage loop control gives a satisfactory result to maintain a constant power through the whole system. The development of the circuit can be done by including a dual loop control instead of the voltage loop control for the future aspect.

Chapter 6

MODELLING AND ANALYSIS OF TRISTATE BUCK BOOST CONVERTER.

6.1 Introduction

The standard BBODC converter encounters an instability issue which is due to the presence of a RHP zero when operating in Continuous Conduction Mode. This RHP zero negatively influences the converter's efficacy. Systems with a RHP zero can be recognized by the initial undershoot in the output voltage response to a step input voltage. The Tri-state converter, however, can be incorporated with an extra mode of operation, specifically the inductor freewheeling mode in Continuous Conduction Mode. This mode excludes the RHP zero from the control-to-output transfer function of the switching converter. Consequently, the Tri-state converter is spared from the non-minimum phase problem, consequently improving the closed-loop dynamic performance of the converter.

6.2 Modelling of Buck Boost converter and Tri-state Buck Boost converter.

This section portrays the modelling of BBODC converter and TSBB converter. The BBODC converter composes of two stages while TSBB converter composed of three stages. An extra stage in TSBB is the freewheeling state.

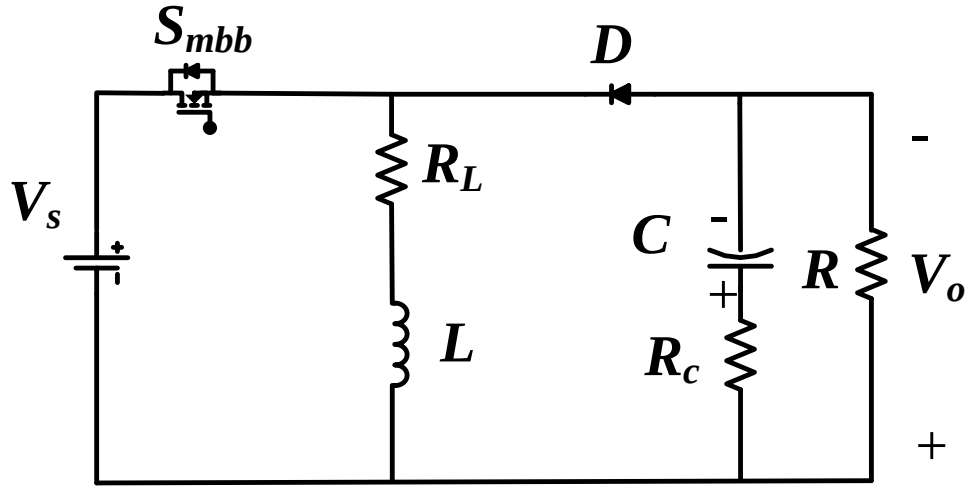


Fig. 6.1 Circuit diagram of BBUDC

6.2.1 Modelling of Buck Boost converter.

Fig. 1 is the circuit diagram of BBUDC. The MOSFET S_{mbb} is used to shuffle between two stages of BBUDC. Here output voltage polarity is reverse since diode *D* allows reverse current flowing direction unlike BODC. The polarity of the capacitor is also affected due to

this case. The first stage denotes the conducting stage of the switch $S_{mbb.}$ In this stage, the inductor gets charged through the direct connection with the supply voltage V_s. The second stage is the discharging of the inductor and contributing to the load. In this stage, the supply is cut out using the switch S_{mbb} as denoted in the Fig 6.2(a). The Fig. 6.2(b) represents the charging state of the inductor.

Considering all the parameters are ideal, the output voltage can be derived as follows,

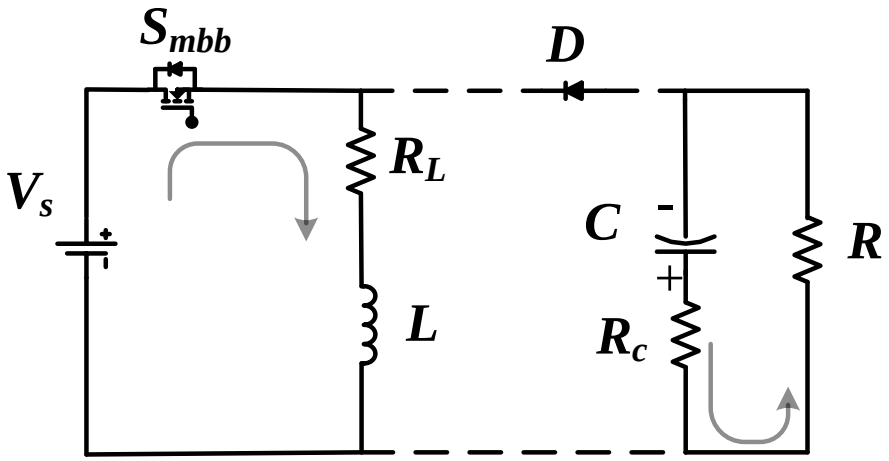


Fig. 6.2(a)

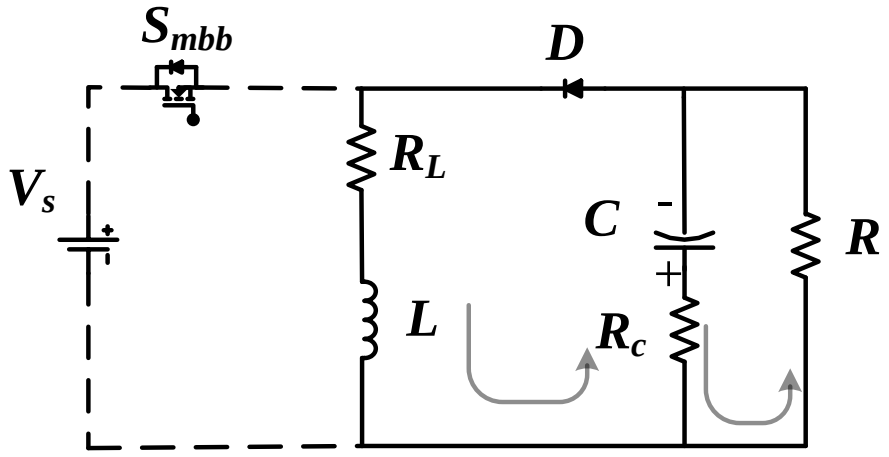


Fig. 6.2(b)

Fig. 6.2. Circuit diagram of BBODC during a) Charging state b) Discharging state.

While the switch S_{mbb} is functioning in the conducting state, the inductor voltage is established as

$$L\frac{di_L}{dt} = V_s - i_L R_L \tag{6.1}$$

The current which tends to pass through the capacitor is provided by

$$i_c = -i_o \tag{6.2}$$

$$c\frac{dV_o}{dt} = -\frac{V_o}{R} \tag{6.3}$$

While the switch S_{mbb} is functioning in the non conducting state, the inductor voltage is established as

$$L\frac{di_L}{dt} = -V_o \tag{6.4}$$

The current which tend to pass through the capacitor is provided by

$$i_L = i_c + i_o \tag{6.5}$$

$$c\frac{dV_o}{dt} = i_L - i_o = i_L - \frac{V_o}{R} \tag{6.6}$$

With the help of the concept, the Voltage second balance equation. The output voltage can be derived as follows,

$$V_s d - V_o(1-d) = 0 \tag{6.7}$$

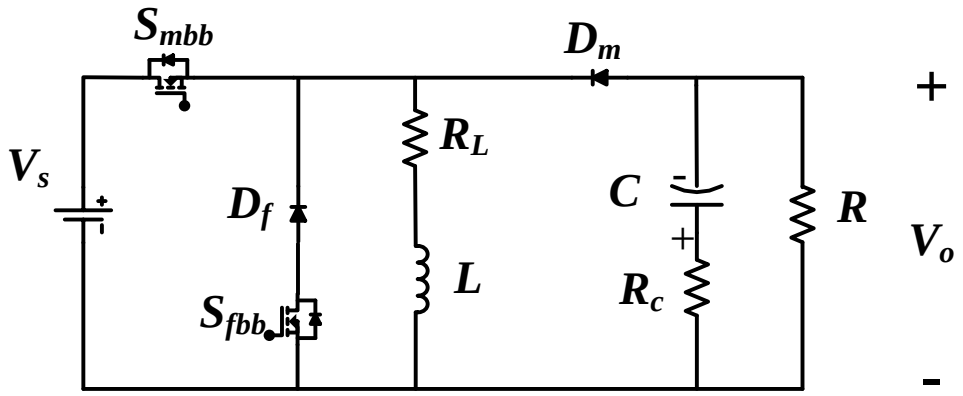


Fig. 6.3. Circuit diagram of TSBB converter.

$$V_o = \frac{V_s d}{(1-d)} \tag{6.8}$$

6.2.2 Modelling of Tristate Buck Boost converter.

Fig. 6.3 is the circuit diagram of TSBB. The MOSFET S_{mbb} is used to shuffle between two stages of TSBB converter. Here output voltage polarity is reverse since diode D allows reverse current flowing direction unlike TSB converter. The polarity of the capacitor is also affected due to this case. There are three stages. There is an extra stage known as freewheeling stage available over there, this stage helps in eliminating the RHP zero which is available in the BBDC converter. As represented in Fig. 6.5(a), it denotes the charging stage of the inductor through the switch S_{mbb} . The diode D_m seperates the load from the rest of the circuit. After this, the second stage contributes in discharging of the inductor. In this, the inductor transfers it energy to the load through the diode D_m which is conducting stage. The last stage which is the freewheeling stage, is portrayed in the Fig. 6.5(c). In this stage, the inductor is allowed to freewheel its energy through the diode D_f and the switch $S_{fbb.}$ This is the full working methodology of the TSBB.

Considering all the parameters are ideal, the output voltage can be derived as follows,

The inductor voltage established in the charging stage can be expressed as,

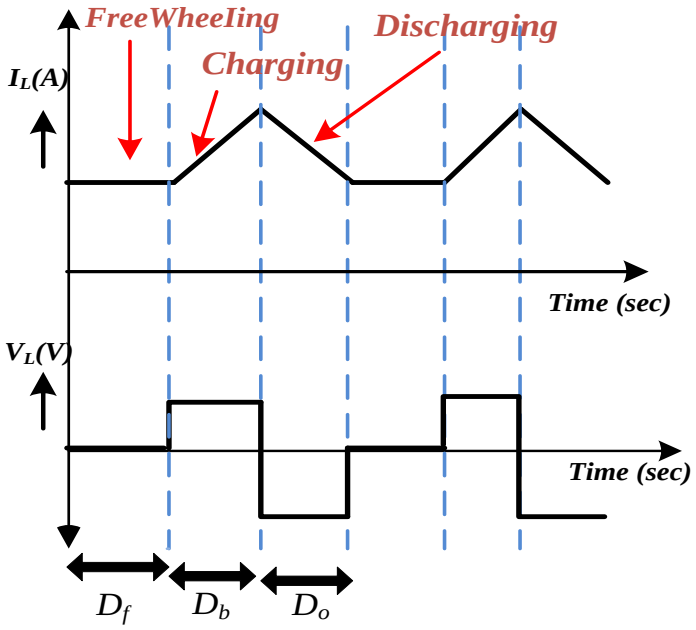


Fig. 6.4 Graph displaying the Inductor Current along with Inductor Voltage in ideal TSBB converter.

$$L\frac{di_L}{dt} = V_s \tag{6.9}$$

The current passing through the capacitor is provided by

$$i_c = -i_o \tag{6.10}$$

$$c\frac{dV_o}{dt} = -\frac{V_o}{R} \tag{6.11}$$

The inductor voltage established in the discharging stage can be expressed as,

$$L\frac{di_L}{dt} = -V_o \tag{6.12}$$

The current passing through the capacitor is provided by

$$i_L = i_c + i_o \tag{6.13}$$

$$c\frac{dV_o}{dt} = i_L - i_o = i_L - \frac{V_o}{R} \tag{6.14}$$

The inductor voltage established in the freewheeling stage can be expressed as,

$$L\frac{di_L}{dt} = -i_L r_L \tag{6.15}$$

The current passing through the capacitor is provided by

$$c\frac{dV_o}{dt} = -\frac{V_o}{R} \tag{6.16}$$

With the help of the concept, the Voltage second balance equation. The output voltage can be derived as follows,

$$V_s d_b + (-V_o) d_o - i_L r_L d_f = 0 \tag{6.17}$$

$$V_o = \frac{V_s d_b}{d_o} \tag{6.18}$$

where $d_b + d_o + d_f = 0$.

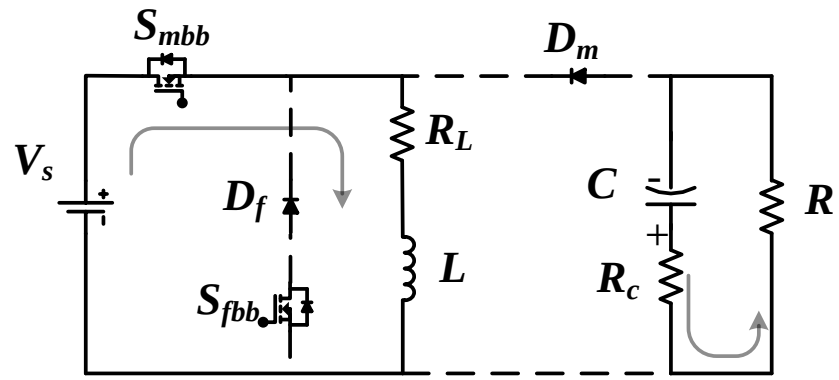


Fig. 6.5(a)

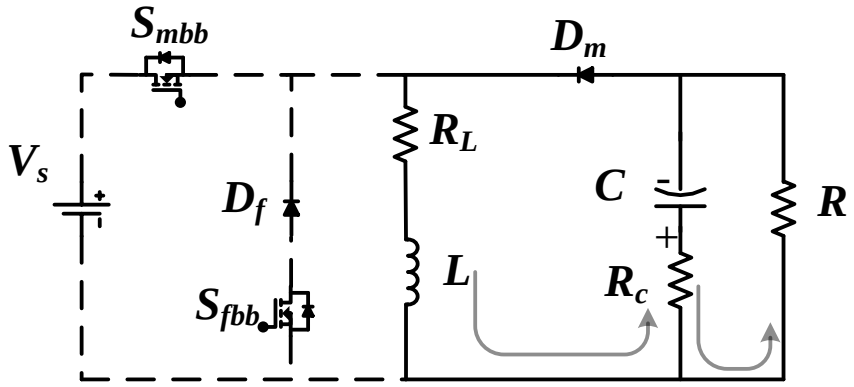


Fig.6.5(b)

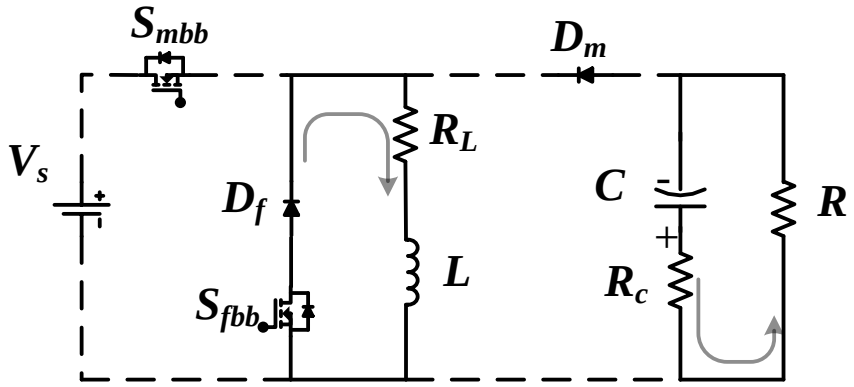


Fig.6.5(c)

Fig. 6.5. Circuit diagram of TSBB during a) Charging state b) Discharging state c) Freewheeling state.

6.3 Small signal analysis of Buck Boost converter and Tri-state Buck Boost converter.

Small signal analysis is an essential tool in the study of power electronics converters, providing information regarding their dynamic behaviour and stability. By linearizing the converter's nonlinear equations around a steady-state operating point, small signal analysis enables the derivation of transfer functions that characterize the system's response to

perturbations. This approach is crucial for designing control systems, as it helps predict how the converter will respond to changes in input voltage, load conditions, and other disturbances. Through small signal models, engineers may enhance the converter's performance, ensuring robust and stable operation under varied operating conditions. In this portion, the small signal analysis of BBODC and TSBB converter is presented.

6.3.1 Small signal analysis of Buck Boost converter

While the switch S_{mbb} is functioning in the conducting state, the inductor voltage is established as

$$L\frac{di_L}{dt} = V_s - i_L(R_m + R_L) \tag{6.19}$$

The relationship between capacitor voltage and output voltage in time domain can be stated as:

$$V_o = \frac{R}{R + R_c}V_c \tag{6.20}$$

$$V_o = aV_c \tag{6.21}$$

Where $a = \frac{R}{R + R_c}$,

The current which tends to pass through the capacitor is provided by

$$i_c = -i_o \tag{6.22}$$

$$c\frac{dv_c}{dt} = -\frac{V_o}{R} \tag{6.23}$$

While the switch S_{mbb} is functioning in the non conducting state, the inductor voltage is established as

$$L\frac{di_L}{dt} = -V_o - V_D - i_L R_L \tag{6.24}$$

The current which tends to pass through the capacitor is provided by

$$i_L = i_c + i_o \tag{6.25}$$

$$i_L = c\frac{dv_c}{dt} + i_o \tag{6.26}$$

The relationship between capacitor voltage and output voltage in time domain can be stated as:

$$V_o = i_c R_c + V_c \tag{6.27}$$

Eliminating the parameter i_c, from the relationship between capacitor voltage and output voltage in time domain can be stated as:

$$V_o = \left(i_L - \frac{V_o}{R} \right) R_c + V_c \tag{6.28}$$

$$V_o = a i_L R_c + a V_c \tag{6.29}$$

The inductor voltage after eliminating the parameter related to output voltage is expressed as,

$$L \frac{d i_L}{dt} = -\left(a i_L R_c + a V_c \right) - V_D - i_L R_L \tag{6.30}$$

The averaging equation of the inductor voltage after using available the modes are denoted as,

$$L \frac{d i_L}{dt} = \left(V_s - i_L (R_m + R_L) \right) D + \left(-\left(a i_L R_c + a V_c \right) - V_D - i_L R_L \right) D' \tag{6.31}$$

Transforming equation (6.31) into Laplace domain,

$$s L i_L = D V_s - D i_L R_m - i_L R_L - a D' i_L R_c - a D' V_c - D' V_D \tag{6.32}$$

The averaging equation of the current through the capacitor using the all the are depicted as,

$$sc V_c = -\frac{a V_c}{R} + i_L D' - \frac{a i_L R_c D'}{R} \tag{6.33}$$

After adding perturbation to the equation (33) through supply voltage, inductor current, duty cycle and capacitive voltage,

$$sc \hat{v}_c = -\frac{a \hat{v}_c}{R} + \left(I_L + \hat{i}_L \right) \left(D' - \hat{d} \right) - \frac{a \left(I_L + \hat{i}_L \right) R_c \left(D' - \hat{d} \right)}{R} \tag{6.34}$$

$$\left(sc + \frac{a}{R} \right) \hat{v}_c = \hat{i}_L \left(D' - \frac{a R_c D'}{R} \right) - \hat{d} \left(I_L - \frac{a R_c I_L}{R} \right) \tag{6.35}$$

The perturbation in capacitive voltage is expressed as,

$$\hat{v}_c = \hat{i}_L \frac{\left(RD' - aR_cD'\right)}{\left(sRc + a\right)} - \hat{d}\frac{\left(RI_L - aR_cI_L\right)}{\left(sRc + a\right)} \tag{6.36}$$

After adding perturbation to the equation (2) through supply voltage, inductor current, duty cycle and capacitive voltage,

$$sL\hat{i}_L = \left(D + \hat{d}\right)\left(V_s + \hat{v}_s\right) - \left(D + \hat{d}\right)\left(I_L + \hat{i}_L\right)R_m - \left(I_L + \hat{i}_L\right)R_L$$

$$-a\left(D' - \hat{d}\right)\left(I_L + \hat{i}_L\right)R_c - a\left(D' - \hat{d}\right)\left(V_c + \hat{v}_c\right) - \left(D' - \hat{d}\right)V_D \tag{6.37}$$

$$sL\hat{i}_L + \hat{i}_L DR_m + \hat{i}_L R_L + aD'\hat{i}_L R_c = \left(V_s - I_L R_m + aI_L R_c + aV_c + V_D\right)\hat{d} - aD'\hat{v}_c \tag{6.38}$$

Eliminating the capacitive voltage from the equation (38)

$$sL\hat{i}_L + \hat{i}_L DR_m + \hat{i}_L R_L + aD'\hat{i}_L R_c = \left(V_s - I_L R_m + aI_L R_c + aV_c + V_D\right)\hat{d} - aD'\left(\hat{i}_L \frac{\left(RD' - aR_cD'\right)}{\left(sRc + a\right)} - \hat{d}\frac{\left(RI_L - aR_cI_L\right)}{\left(sRc + a\right)}\right) \tag{6.39}$$

The current loop transfer function can be termed as,

$$\frac{\hat{i}_L}{\hat{d}} = \frac{P\left(sRc + a\right) + aD'\left(RI_L - aI_L R_c\right)}{s^2 LRc + s\left[RcM + La\right] + a\left[M + D'N\right]} \tag{6.40}$$

where ,

$$P = V_s - I_L R_m + aI_L R_c + aV_c + V_D \tag{6.41}$$

$$M = DR_m + R_L + aD'R_c \tag{6.42}$$

$$N = RD' - aR_cD' \tag{6.43}$$

The voltage loop transfer function is displayed with the help of capacitor voltage (V_c) and duty cycle and this is provided as,

$$\frac{\hat{v}_c}{\hat{d}} = \frac{PN - \left(RI_L - aR_cI_L\right)\left(sL + M\right)}{s^2 LRc + s\left[RcM + La\right] + a\left[M + D'N\right]} \tag{6.44}$$

The averaging output voltage equations is displayed as followed

$$V_o(s) = aV_c(s) + aD'I_L(s)R_c \tag{6.45}$$

The equation formed after the introduction of the perturbations are expressed as,

$$\hat{v}_o(s) = a\hat{v}_c(s) + a\left(D' - \hat{d}\right)\left(I_L + \hat{i}_L\right)R_c \tag{6.46}$$

$$\hat{v}_o(s) = a\hat{v}_c(s) - a\hat{d}(s)I_L r_c + aD'\hat{i}_L(s)R_c \tag{6.47}$$

The voltage loop transfer function is displayed with the use of output voltage (V_o) and duty cycle and is stated as,

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = a\frac{\hat{v}_c(s)}{\hat{d}(s)} - aI_L R_c + aD'\frac{\hat{i}_L(s)}{\hat{d}(s)}R_c \tag{6.48}$$

6.3.2 Small signal analysis of Tristate Buck Boost converter

As stated before, TSBB converter have 3 stages. The charging stage is denoted by the duty cycle d_b, the discharging stage is denoted by d_o and the freewheeling stage is denoted by d_f.

During the charging stage (d_b,) the inductor voltage is established as

$$L\frac{di_L}{dt} = v_s - i_L r_L \tag{6.49}$$

The current which tends to pass through the capacitor is provided by

$$i_c = -i_o$$

(6.50)

$$c\frac{dv_c}{dt} = -\frac{v_o}{R} \tag{6.51}$$

The relationship between capacitor voltage and output voltage in time domain can be stated as:

$$v_o = \frac{R}{R + r_c}v_c \tag{6.52}$$

The state equations matrix during the charging state is expressed as,

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{r_L}{L} & 0 \\ 0 & -\frac{1}{c(R + r_c)} \end{bmatrix}\begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}v_s \tag{6.53}$$

During the discharging stage (d_o) the inductor voltage is established as

$$L\frac{di_L}{dt} = -i_L r_L - v_o \tag{6.54}$$

The current which tends to pass through the capacitor is provided by

$$c\frac{dv_c}{dt} = i_L - i_o \tag{6.55}$$

The relationship between capacitor voltage and output voltage in time domain can be stated as:

$$v_o = i_c r_c + v_c \tag{6.56}$$

$$v_o = \left(i_L - \frac{v_o}{R}\right) r_c + v_c \tag{6.57}$$

$$v_o = i_L\left(\frac{Rr_c}{R+r_c}\right) + \frac{Rv_c}{R+r_c} \tag{6.58}$$

The inductor voltage after eliminating the parameter related to output voltage is expressed as,

$$L\frac{di_L}{dt} = -i_L\left(\frac{Rr_c}{R+r_c} + r_L\right) - \frac{Rv_c}{R+r_c} \tag{6.59}$$

The current through the capacitor after eliminating the parameter related to output voltage is expressed as,

$$c\frac{dv_c}{dt} = i_L\frac{R}{R+r_c} - \frac{v_c}{R+r_c} \tag{6.60}$$

The state equations matrix during the discharging state is expressed as,

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{r_L R + r_L r_c + D_o r_c R}{L(R+r_c)} & -\frac{R}{L(R+r_c)} \\ \frac{R}{c(R+r_c)} & \frac{1}{c(R+r_c)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} \tag{6.61}$$

During the freewheeling stage (d_f) the inductor voltage is established as

$$L\frac{di_L}{dt} = -i_L r_L \tag{6.62}$$

The current which tends to pass through the capacitor is provided by

$$c\frac{dv_c}{dt} = -\frac{v_c}{R + r_c} \tag{6.63}$$

The state equations matrix during the freewheeling state is expressed as,

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{r_L}{L} & 0 \\ 0 & -\frac{1}{c(R + r_c)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} \tag{6.64}$$

The averaging equation of the inductor voltage after using all the modes are denoted as,

$$sLi_L = (v_s - i_L r_L) d_b - i_L \left(\frac{Rr_c + r_L R + r_L r_c}{R + r_c} \right) d_o - \frac{Rv_c}{R + r_c} d_o - i_L r_L d_f \tag{6.65}$$

The averaging equation of the current through the capacitor using all the modes are established as,

$$scv_c = -\frac{v_c}{R + r_c} d_b + d_o i_L \frac{R}{R + r_c} - d_o \frac{v_c}{R + r_c} - d_f \frac{v_c}{R + r_c} \tag{6.66}$$

The averaging equation of the output voltage using all the modes of operation are portrayed as,

$$v_o = r_c i_c + v_c \tag{6.67}$$

After adding the perturbation, the inductor current can be expressed as,

$$\hat{i}_L = \frac{R + r_c}{D_o R} \left(sc + \frac{1}{R + r_c} \right) \hat{v}_c \tag{6.68}$$

After adding the perturbation, the inductor voltage in Laplace domain is expressed as,

$$sL\hat{i}_L = \hat{d}_b V_s - \frac{(r_L R + r_L r_c + D_o r_c R)}{R + r_c} \hat{i}_L - \frac{D_o R}{R + r_c} \hat{v}_c \tag{6.69}$$

Eliminating the inductor current from the equation (3.69) is expressed as,

$$\left[sL + \frac{(r_L R + r_L r_c + D_o r_c R)}{R + r_c} \right] \left(\frac{R + r_c}{D_o R} \left(sc + \frac{1}{R + r_c} \right) \hat{v}_c \right) = \hat{d}_b V_s - \frac{D_o R}{R + r_c} \hat{v}_c$$

(6.70)

The voltage loop transfer function is displayed with the help of capacitor voltage (V_c) along with the duty cycle is provided as,

$$\frac{\hat{v}_c}{\hat{d}_b} = \frac{V_s}{L} \times \frac{1}{s^2 \frac{c(R+r_c)}{D_o R} + s\frac{(1-Mc(R+r_c))}{RD_o} + \left(N - \frac{M}{RD_o}\right)} \tag{6.71}$$

where,

$$M = -\frac{r_L R + r_L r_c + D_o r_c R}{L(R+r_c)} \tag{6.72}$$

$$N = \frac{RD_o}{L(R+r_c)} \tag{6.73}$$

The addition of perturbation in the output voltage equation, the output voltage equation can be stated as,

$$V_o + \hat{v}_o = r_c c \frac{d}{dt}(V_c + \hat{v}_c) + (V_c + \hat{v}_c) \tag{6.74}$$

$$v_c = \frac{v_o}{(1+sr_c c)} \tag{6.75}$$

The voltage loop transfer function can be expressed with the use of load voltage (V_o) along with charging interval duty, can be stated as,

$$\frac{\hat{v}_o}{\hat{d}_b} = \frac{V_s}{L} \times \frac{(1+sr_c c)}{s^2 \frac{c(R+r_c)}{D_o R} + s\frac{(1-Mc(R+r_c))}{RD_o} + \left(N - \frac{M}{RD_o}\right)} \tag{6.76}$$

6.4 Stability analysis of Buck Boost converter and Tri-state Buck Boost converter.

Within the domain of power electronics, closed-loop analysis techniques employing root locus and Bode plots are instrumental in obtaining optimal system stability and performance. Root locus analysis unveils the critical information regarding the positioning of poles and zeros within the system, consequently influencing its dynamic response. This knowledge empowers engineers to design robust controllers that effectively regulate the converter's behaviour. Conversely, Bode diagrams offer a valuable perspective in the frequency domain, depicting the gain and phase margins of the system. These margins are paramount for assessing stability and fine-tuning the control system. By strategically employing these combined techniques, engineers gain the capability to meticulously alter control parameters to ensure optimal performance and reliability in DC-DC converters and other power

electronic circuits. This meticulous approach empowers them to effectively mitigate the impact of fluctuating or disturbed input conditions.

The presence of a RHP zero negatively impacts the performance of switching converters.

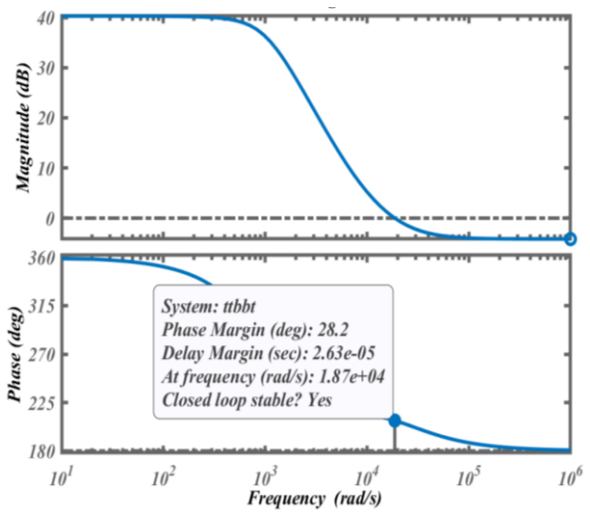


Fig. 6.6(a)

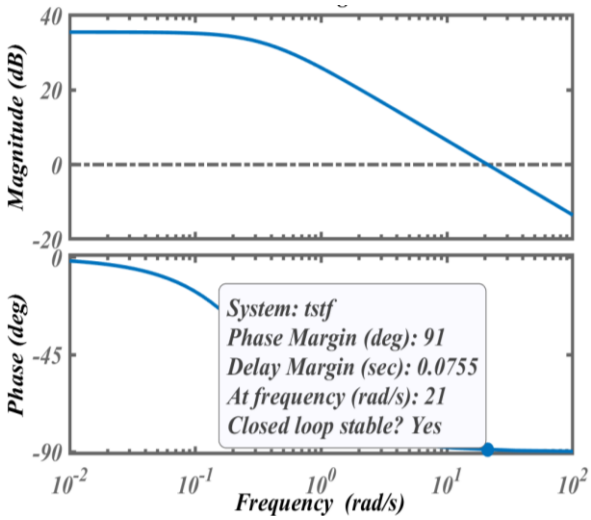


Fig. 6.6(b)

Fig 6.6. Bode plot of a) BBODC converter b) TSBB converter

This phenomenon manifests itself in systems with an open-loop RHP zero as an initial

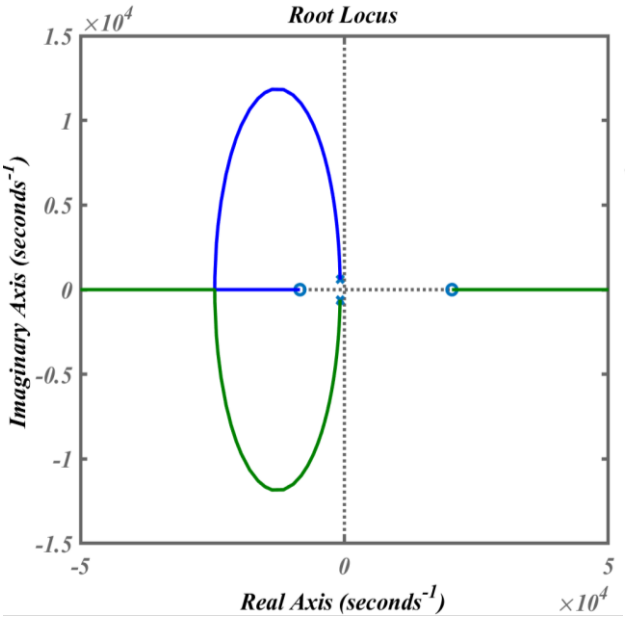


Fig.6.7(a)

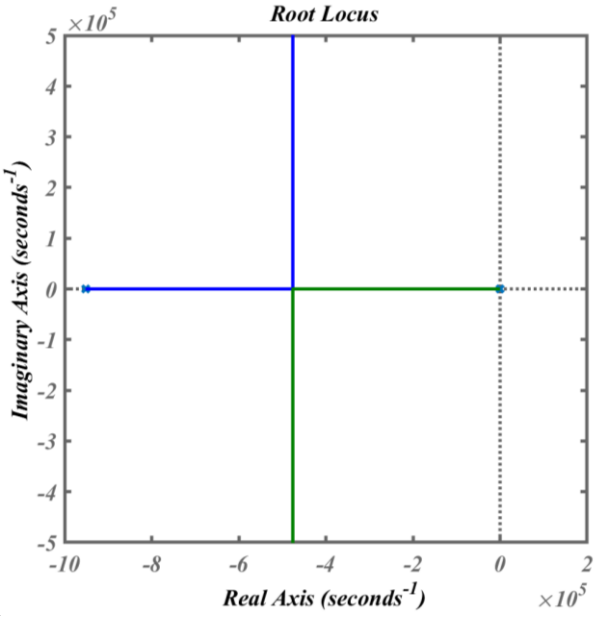


Fig. 6.7(b)

Fig 6.7. Root locus of a) BBODC converter b) TSBB converter

decrease in the output voltage when subjected to a sudden rise in input voltage (step input).

The Tri-state converter offers a solution by incorporating an additional operating mode, specifically the inductor discontinuous conduction mode within the continuous conduction mode condition. This unique mode eliminates the RHP zero from the control-to-output transfer function of the converter, improving its overall stability and transient response.

As denoted in the Fig. 6.7, the PM of BBODC converter is stated as 28.2º and the PM of TSBB converter is 91º. As PM specifies that the more is better, so this tells that TSBB is better in terms of stability. With the non-existence of the RHP zero, PM becomes much more than the one which comes with RHP zero in it like BBODC converter. Fig 6.7(a) and 6.7(b) denotes that both of the converter is closed loop stable. There is another method to tell the location of the pole as well as zero of the transfer function derived from the power electronics converter and this method is root locus. Fig. 6.7(a) denotes the root locus of the BBODC converter. The RHP zero is visible over here and as mentioned, this is the reason the PM is decreases so much by a big margin as compare to the TSBB converter. The Fig. 6.7(b) is of TSBB converter which denotes that reason of its stability since there is no pole or zero at right half of the S-plane.

6.5 Conclusion

This chapter portrays the difference between TSBB converter and BBODC converter through their steady state output voltage equation, transfer function and stability analysis of both the converter. The steady state equation has been derived in case of ideal condition for both the converter. The transfer function has been derived for the non ideal condition. The stability analysis of both converters has been portrayed with the use of bode plot and root locus. The root locus shows the right hand zero present in the standard BBODC converter. All these points sum up to the reason that why the TSBB converter than a standard BBODC converter.

Chapter 7

HIGH GAIN TRISTATE CONVERTERS.

7.1 Introduction

The conventional BODC converter and the BBODC converter encounters an instability issue owing to the existence of a RHP zero when running in Continuous Conduction Mode. The impact originating from the RHP zero in the conventional BBODC converter or BODC converter in the time domain can be elucidated as follows: a sudden initial degradation (undershoot) in the output voltage prompts the control system to initiate an augmentation in the duty cycle ratio. The concatenation of two BBODC converters or BODC converter entails a diminished overall efficiency, equating to the product of the efficiencies of each individual converter. Consequently, this approach is regarded inappropriate for enhancing the gain of the converter. This chapter proposes the incorporation of a SC circuit into a BBODC converter as well as BODC converter. While a SC converter can offer flexible voltage ratios based on the number of capacitors in its structure, its efficacy experiences an enormous drop when confronted with maintaining a constant output voltage.

7.2 Modelling of High Gain Tristate Converter.

The modelling of HGT converter is portrayed in this part. The portion shows both HGT of BBUDC and BODC. Here there are 4 stages in HGT converter. There is an additional stage for the charging of the capacitors of SC circuit.

7.2.1 Modelling of High Gain Tristate Buck-Boost Converter.

The modeling of the HGTSBB Converter is clarified in this section. Fig. 2 represents the switching diagram of the HGTSBB converter and based on it, all the switches of the HGTSBB converter are triggered. In Fig. 7.1 a, the switches S_{c1} and S_m are on. This stage charges both the capacitors C_1 and C_2. In the stage 7.1 b, the charging of the inductors L_b is taking place. In stage 7.1 c, the discharging of the inductors L_b is taking place. Stage 7.1 d is the free-wheeling stage where the inductor free-wheeling its energy. The additional stages involving the capacitors C_1 and C_2 is included to achieve the property of higher gain.

The corresponding steady state equations are stated as follows:

This is the first stage, mode 1 a where the switch S_{c1} and S_m are on.

$$C\frac{dv_c}{dt} = V_s \qquad [7.1]$$

$$L_b \frac{di_{Lb}}{dt} = V_s \quad [7.2]$$

$$C_0 \frac{dV_o}{dt} = \frac{V_o}{R_1} \quad [7.3]$$

The mode 1 b is the place where the switch S_{c2}, S_{c3} and S_m are on.

$$C \frac{dv_c}{dt} = -i_{Lb} \quad [7.4]$$

$$L_b \frac{di_{Lb}}{dt} = V_s + 2V_c \quad [7.5]$$

$$C_0 \frac{dV_o}{dt} = \frac{V_o}{R_1} \quad [7.6]$$

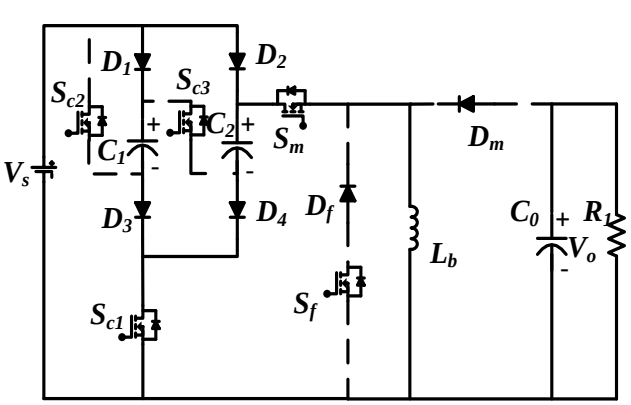


Fig.7.1(a)

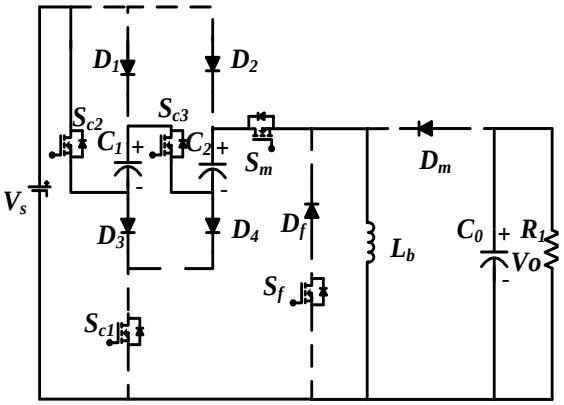


Fig.7.1(b)

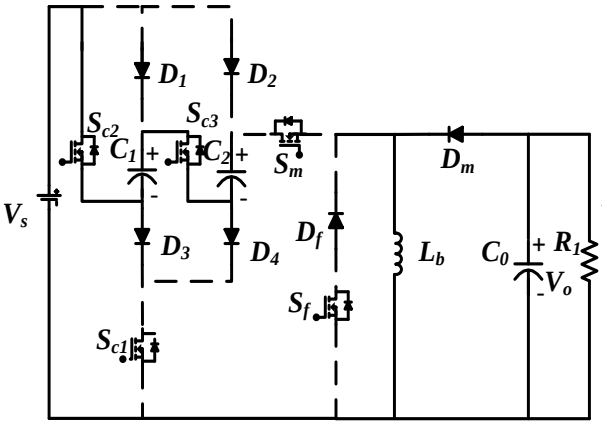


Fig.7.1(c)

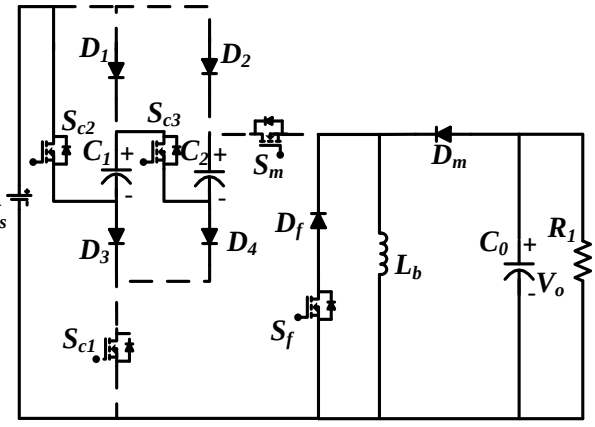


Fig.7.1(d)

Fig 7.1. Circuit schematics of modes of HGTSBB Converter.

The mode 7.1 c switches S_{c2} and S_{c3} on.

$$L_b \frac{di_{Lb}}{dt} = -V_o \quad [7.7]$$

$$C_0 \frac{dV_o}{dt} = \frac{V_o}{R_1} - i_{Lb} \quad [7.8]$$

The mode 1 d switches S_{c2}, S_{c3} and S_f are on. This is the free-wheeling mode.

$$L_b \frac{di_{Lb}}{dt} = 0 \quad [7.9]$$

$$C_0 \frac{dV_o}{dt} = \frac{V_o}{R_1} \quad [7.10]$$

In a steady state, the time integral of the inductor voltage (v_L) over one complete time period must be zero. Assuming ideal components, the DC gain of the HGTSBB converter can be represented as:

$$V_s x + [(2V_c + V_s) \times (d_b - x)] - v_0 d_b = 0 \quad [7.11]$$

$$V_s d_b + 2V_c \times (d_b - x) = v_0 d_b \quad [7.12]$$

$$V_0 = V_s \frac{d_b}{d_o} + 2V_c \times (d_b - x) \quad [7.13]$$

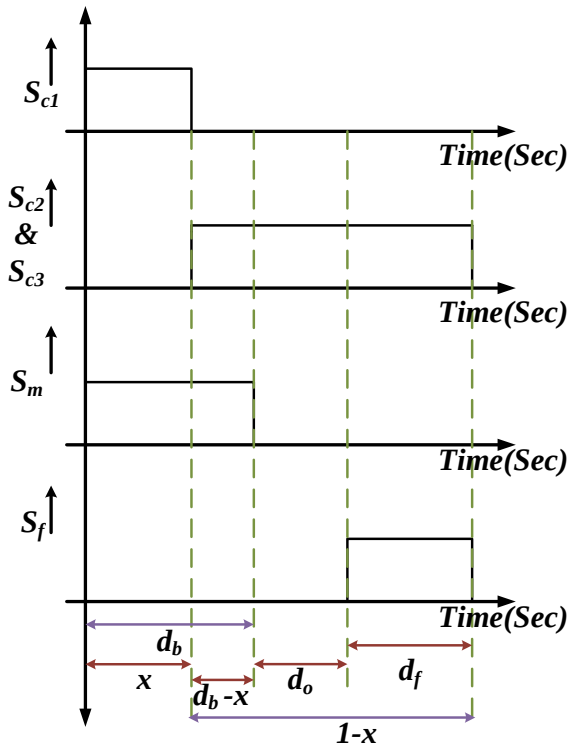


Fig 7.2. Switching characteristics of the switches S_{c2}, S_{c1}, S_{c3}, S_m and S_f.

Considering $V_c = V_s$,

$$V_0 = V_s \frac{d_b}{d_o} + 2V_s \times (d_b - x) \quad [7.15]$$

7.2.2 Modelling of High Gain Tristate Boost Converter.

The modeling of the HGTSB Converter is clarified in this section. Fig. 7.4 represents the switching diagram of the HGTSB converter and based on it; all the switches of the HGTSB converter are triggered. In Fig. 7.3 a, the switches S_{c1} and S_{ft} are on. This stage charges both the capacitors C_1 and C_2. In the stage 7.3 b and 7.3 c, the charging of the inductors L_{bT} is taking place. In stage 7.3 d, the discharging of the inductors L_{bT} is taking place. The additional stages involving the capacitors C_1 and C_2 is included to achieve the property of higher gain.

The corresponding steady state equations are stated as follows:

This is the first stage, mode 7.3 a where the switch S_{c1} and S_{ft} are on.

$$C \frac{dv_c}{dt} = V_s \quad [7.16]$$

$$L_b \frac{di_{Lb}}{dt} = 0 \quad [7.17]$$

$$C_0 \frac{dV_o}{dt} = -\frac{V_o}{R_1} \quad [7.18]$$

The mode 7.3 b is the place where the switch S_{c2}, S_{c3} and S_{mT} are on.

$$C \frac{dv_c}{dt} = V_s \quad [7.19]$$

$$L_b \frac{di_{Lb}}{dt} = V_s \quad [7.20]$$

$$C_0 \frac{dV_o}{dt} = -\frac{V_o}{R_1} \quad [7.21]$$

The mode 7.3 c switches S_{c2} , $S_{c3,}$ S_{mT} and S_{ft} are on.

$$L_b \frac{di_{Lb}}{dt} = 3V_s \quad [7.22]$$

$$C_0 \frac{dV_o}{dt} = -\frac{V_o}{R_1} \quad [7.23]$$

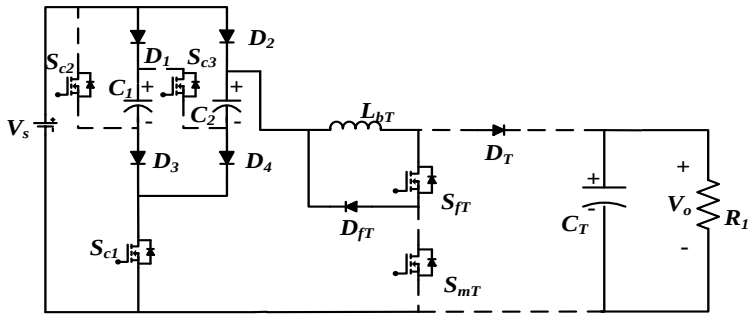


Fig. 7.3(a)

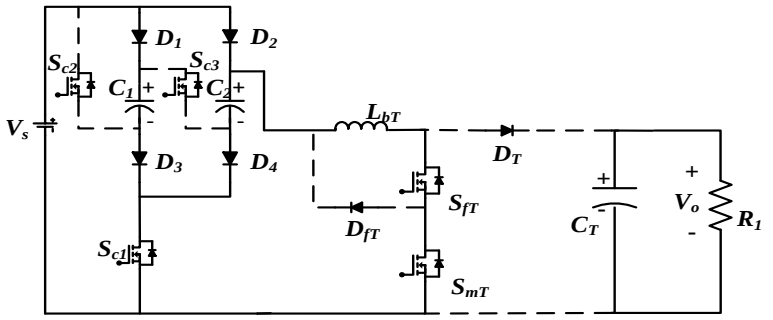


Fig. 7.3(b)

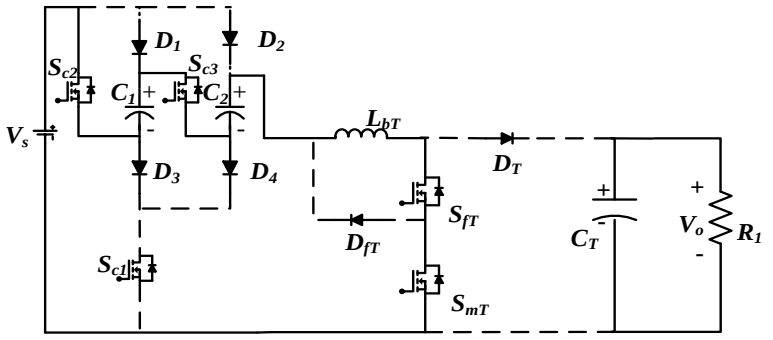


Fig. 7.3(c)

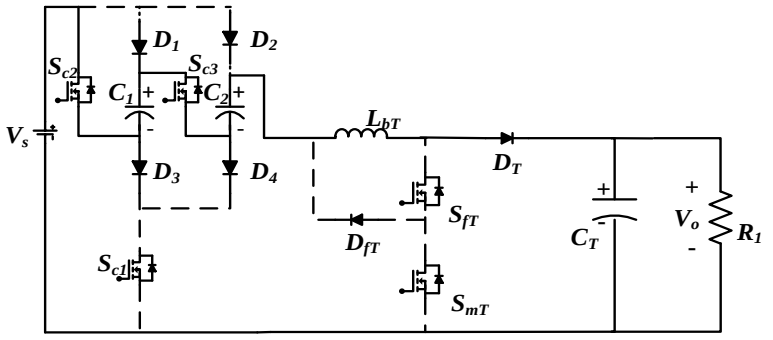


Fig. 7.3(d)

Fig 3. Circuit schematics of modes of HGTSB Converter.

The mode 2 d switches S_{c2} and S_{c3} are on.

$$L_b \frac{di_{Lb}}{dt} = 3V_s - V_o \quad [7.24]$$

$$C_0 \frac{dV_o}{dt} = i_{Lb} - \frac{V_o}{R_1} \quad [7.25]$$

In a steady state, the time integral of the inductor voltage (v_L) over one complete time period must be zero. Assuming ideal components, the DC gain of the HGTSB converter can be represented as:

$$[V_s \times (x - d_b)] + \left[\left(d_b + d_f - x\right) \times 3V_s\right] + \left[\left(3V_s - V_o\right) \times d_o\right] = 0 \quad [7.26]$$

$$V_0 = V_s \frac{\left[-2x + 3 - d_b\right]}{d_o} \quad [7.27]$$

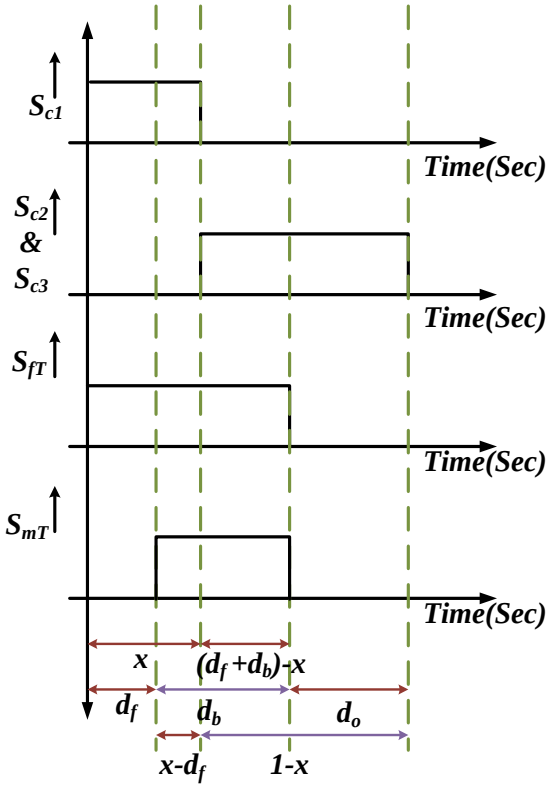


Fig 7.4. Switching characteristics of the switches S_{c2}, S_{c1}, S_{c3}, S_{mT} and S_{fT}

7.3 Result of High Gain Tristate Converter.

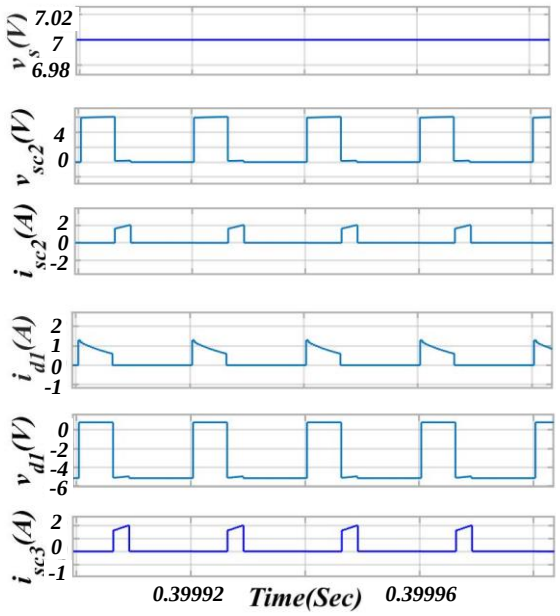


Fig.7.5 a

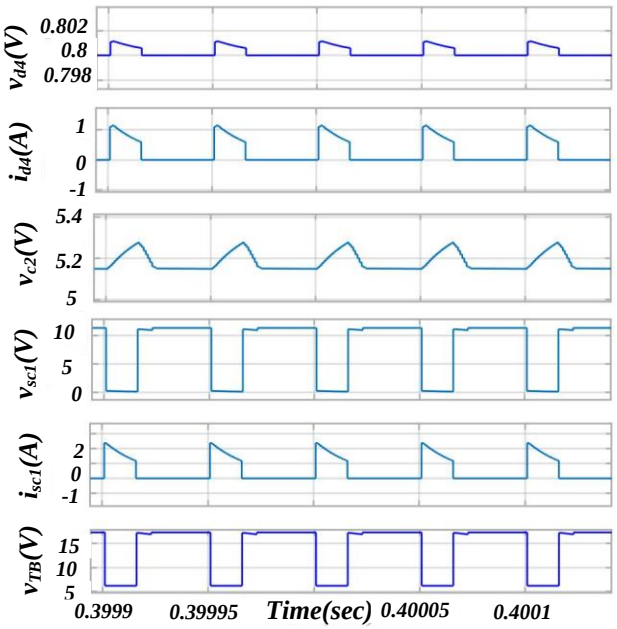


Fig. 7.5 b

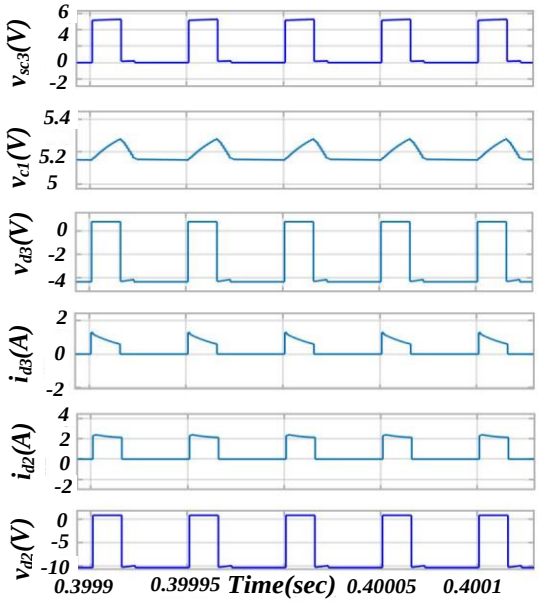


Fig..7.5(c)

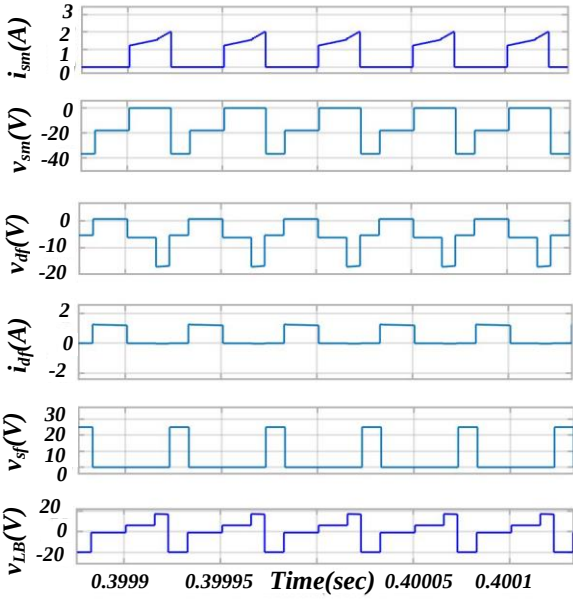


Fig.7.5(d)

Fig. 7.5 a) Steady State Simulated parameters: $v_s(V)$, $v_{sc2}(V)$, $i_{sc2}(A)$, $i_{d1}(A)$, $v_{d1}(V)$, $i_{sc3}(A)$ b) Steady State Simulated parameters: $v_{d4}(V)$, $i_{d4}(A)$, $v_{c2}(V)$, $v_{sc1}(V)$, $i_{sc1}(A)$, $v_{TB}(V)$ c) Steady State Simulated parameters: $v_{sc3}(V)$, $v_{c1}(V)$, $v_{d3}(V)$, $i_{d3}(A)$, $i_{d2}(A)$, $v_{d2}(V)$ d) Steady State Simulated parameters: $i_{sm}(A)$, $v_{sm}(V)$, $v_{df}(V)$, $i_{df}(A)$, $v_{sf}(V)$, $v_{Lb}(V)$

The portion shows the performance of both HGT of BBUDC and BODC. Here there are 4 stages in HGT converter. There is an additional stage for the charging of the capacitors of SC circuit.

7.3.1 Simulation Results of High Gain Tristate Buck-Boost Converter.

The circuit incorporates a switched capacitor circuit with the topology of the TSBB Converter. The switched capacitor topology enhances the gain of the TSBB Converter, contributing to enhanced stability compared to the conventional BBODC converter. Fig. 7.5 a depicts the steady state parameters of v_s(V), v_{sc2}(V), i_{sc2}(A), i_{d1}(A), v_{d1}(V) and i_{sc3}(A). The supply voltage is kept at 7 volts. This figure shows that the diode and switch voltages as well as the current rating are within a suitable limit. Fig. 7.5 b brings the vision of v_{d4}(V), i_{d4}(A), v_{c2}(V), v_{sc1}(V), i_{sc1}(A) and v_{TB}(V). This figure indicates that the diode and switch voltages as well as the current rating are within the appropriate limit. The voltage v_{TB}(V) shows the voltage as a supply to the TSBB converter. So here it is seen that the voltage has increased due to the presence of the switch capacitor circuit. Fig. 7.5 c depicts the steady state parameters of v_{sc3}(V), v_{c1}(V), v_{d3}(V), i_{d3}(A), i_{d2}(A) and v_{d2}(V). This figure shows that the diode and switch voltages as well as the current rating are within a suitable limit. Fig. 7.5 d enters the TSBB part. The voltage and the current rating of freewheeling diode and main switch are shown in this figure. The graph depicts the waveform of the inductor voltage which consists of four stages, as mentioned earlier. The waveform of the voltage of the

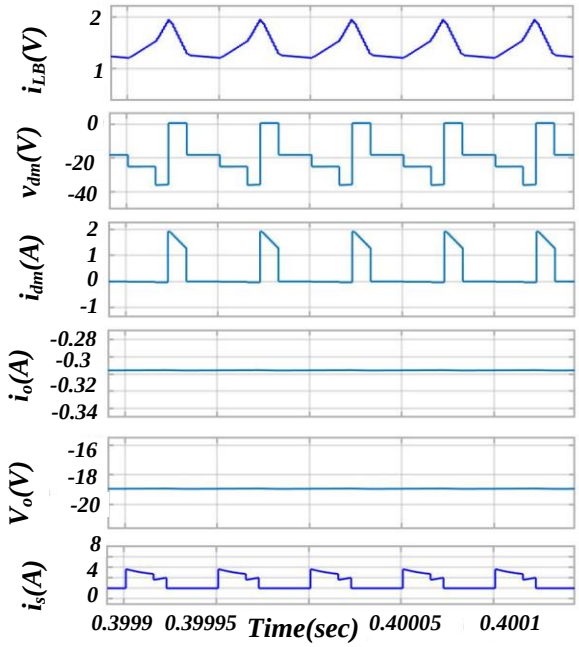


Fig. 7.6 Steady State Simulated parameters: $i_{Lb}(A)$, $v_{dm}(V)$, $i_{dm}(A)$, $i_o(A)$, $v_o(V)$, $i_s(A)$

switch S_f is also provided. Fig. 5 d depicts the steady state parameters which are i_{sm}(A), v_{sm}(V), v_{df}(V), i_{df}(A), v_{sf}(V) and v_{Lb}(V). This figure indicates that the diode and switch voltages as well as the current rating are within the appropriate limit. The Fig. 7.6 is a continuation of all the steady state results of the HGTSBB Converter. As shown in Fig. 7.5 d, Fig. 7.6 depicts the waveform of the inductor current which consists of four stages, and the extra stage provides the extra gain to the HGTSBB Converter. The waveform of the both the current and the voltage rating of the main diode are provided. The waveform of the output current and the output voltage shown. The waveform of the source current i_s is maintained within limits. Fig. 6 depicts the steady state waveform of the i_{Lb}(A), v_{dm}(V), i_{dm}(A), i_o(A), v_o(V) and i_s(A). The steady state performance of the HGTSBB Converter is stable and fulfils its purpose.

7.3.2 Simulation Results of High Gain Tristate Boost Converter.

The circuit incorporates a SC circuit with the topology of the TSB Converter. The switched capacitor topology enhances the gain of the TSB Converter, contributing to enhanced stability compared to the conventional BODC converter. The supply voltage of 7 volts have posed in the HGTSB converter, the waveform of supply current(i_s), pulses which is used to trigger the switches in SC circuits, the inductor voltage of TSB converter and the current through the capacitor in SC circuit (i_{D1}) are portrayed with the Fig.7.7(a). The switch S_{c1} is triggered through G_{sc1} and G_{sc2} as well as G_{sc3} which are the complemented form of G_{sc1}. The waveform of the current through the diode D_1 and D_2 shows the charging of capacitor of the SC circuit. Fig. 7(c) depicts the voltage of the capacitor of SC which is the part of SC circuit. The pulses that help to trigger the switches of the TSB which is attached to SC circuit are portrayed in Fig.7(b). The voltage and the current of the switches $S_{c1,}$ S_{c2} and S_{c3} are restricted within a particular limit. The voltage and current of the switches S_{mT} and S_{fT} are prevailed within a limit. The voltage and current of inductor (L_b) are v_{Lb}(V) and i_{Lb}(V) are portrayed through Fig. 7.8(a). Fig. 7.8(b) shows the waveform of the output voltage and the output current which is coming out to be within the limits. The extra stage is provided to pull up the voltage at the output. Fig. 7.7(a) depicts the steady state of the v_s(V),i_s(A),G_{sc1}(V),G_{sc2}(V), G_{sc3}(V),v_{Lb}(V). Fig. 7.7(b) depicts the steady state waveform of v_{Lb}(V), G_{smt}(V), G_{sft}(V), v_{sc2}(V), i_{sc2}(A) and i_{sc3}(A). Fig.7.7(c) portrays the steady state performance of v_{sc3}(V), v_{Lb}(V),v_{c1}(V),i_{D2}(A), i_{D3}(A) and v_{c2}(V). Fig. 7.7(d) shows that waveform of v_{Lb}(V), i_{D4}(A),v_{sc1}(V),i_{sc1},i_{inT}(A) and v_{inT}(V). Fig.7.8(a) shows the waveform

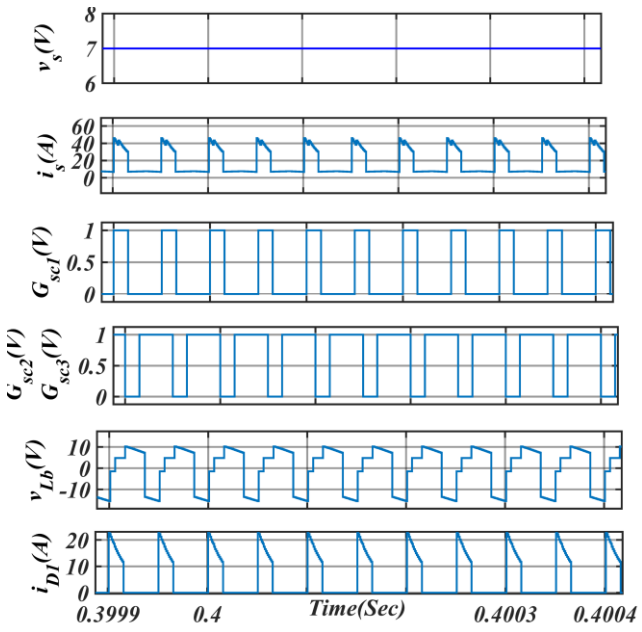


Fig.7.7(a)

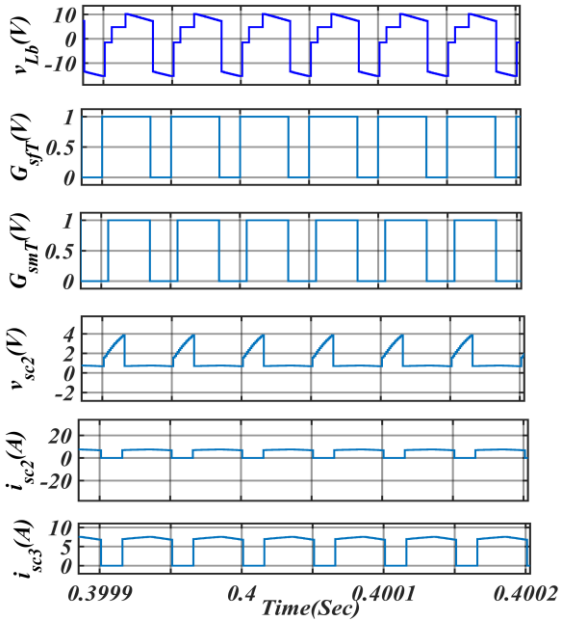


Fig.7.7(b)

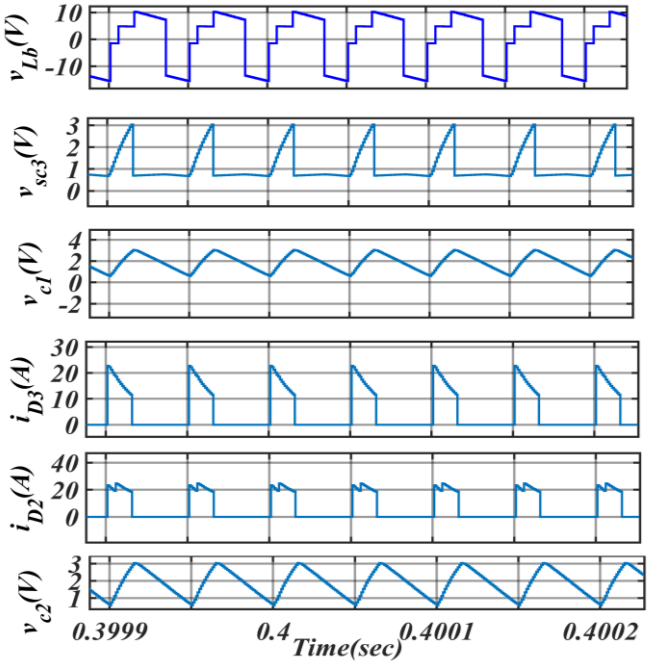


Fig.7.7(c)

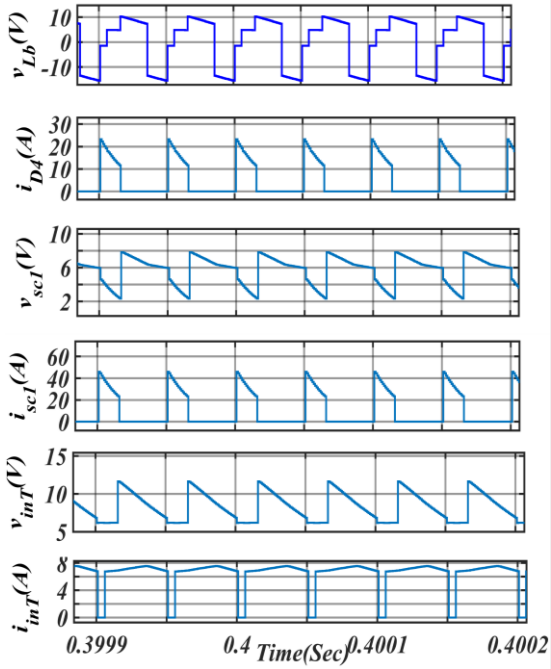


Fig.7.7(d)

Fig. 7.8 Steady state parameters a) $v_s(V), i_s(A), G_{sc1}(V), G_{sc2}(V), G_{sc3}(V), v_{Lb}(V)$ b) $v_{Lb}(V), G_{smt}(V), G_{sft}(V), v_{sc2}(V), i_{sc2}(A)\ i_{sc3}(A)$ c) $v_{sc3}(V), v_{Lb}(V), v_{c1}(V), i_{D2}(A), i_{D3}(A)\ v_{c2}(V)$ d) $v_{Lb}(V), i_{D4}(A), v_{sc1}(V), i_{sc1}(A), i_{inT}(A)\ v_{inT}(V)$

of v_{Lb}(V),i_{Lb}(A),v_{sfT}(V),i_{sfT}(A), v_{smT}(V), i_{smT}(A). Fig. 7.8(b) illustrates the steady state performance of v_{Lb}(V), i_{DfT}(A), i_{DT}(A), i_{cT}(A), i_o(A), v_o(V).

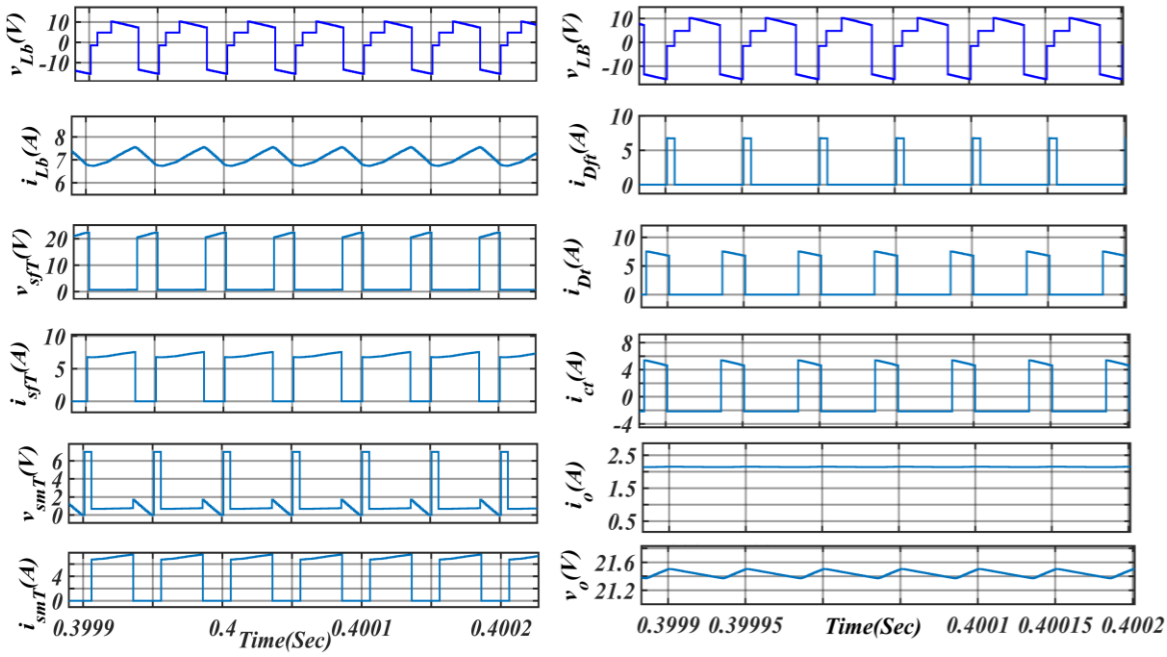


Fig.7.8(a) Fig.7.8(b)

Fig. 8 Steady state parameters a) $v_{Lb}(V)$,$i_{Lb}(A)$,$v_{sfT}(V)$,$i_{sfT}(A)$, $v_{smT}(V)$, $i_{smT}(A)$.b) $v_{Lb}(V)$, $i_{DfT}(A)$, $i_{DT}(A)$, $i_{cT}(A)$, $i_o(A)$, $v_o(V)$.

7.4 Conclusion

This chapter paved through the path of getting high gain converter through TSB and TSBB converter. The circuit schematics of the HGTSB and HGTSBB has been portrayed in this chapter. There are 4 stages in HGTSB and HGTSBB and the one extra stage help in providing the higher gain through the capacitor in SC circuit part. The steady state performance of both the converter HGTSB and HGTSBB had been portrayed in detail in this chapter. The output voltage and the output current which is coming out to be within the limits. The extra stage is provided to pull up the voltage at the output.

Chapter 8

CONCLUSION

This project focuses on the stability criteria of BODC and BBODC converter. The major problem with a standard BODC and BBODC is the presence of RHP zero and the solution of this RHP zero is the use of TSB and TSBB converter. The TSB and TSBB converter have one extra stage which is the freewheeling state in which the charge stored in the inductor is freewheeled through a diode. The transfer function of TSBB and TSB converter formed due to this freewheeling state comes out to be stable. The results of TSB converter with T2C are better than PI controller which is shown in the chapter of analysis of TSB converter. The stability analysis of TSB with T2C and PI controller is illustrated through the chapter of analysis of TSB converter, shows the superior of the combination of TSB converter with T2C over TSB with PI controller. The development of DOTSB is being inspired from IDO converter. DOTSB converter gives out to type of output. One is taken out from the main output which gives the output of the TSB converter and auxiliary one is gives out buck output. The concept of using another DC DC converter to control multiport converter is adapted over here. The comparison of the TSBB and BBODC is depicted over here and it points out the clear advantage TSBB converter over a standard BBODC. The concept of CPL and how to use attached CPL to another converter is used over here. The CPL is attached with BODC and TSBB converter to point out the capability of the converter. The CPL is also tested with DOTSB converter. The problem of the Tristate converter is limited gain of the output voltage, it receives. This problem is resolved through the development of HGT converter with both the configuration TSBB and TSB converter. The future of the project can be based on two things. The first thing is the feedback controlling of HGT converter and the second thing is the use of dual loop control in DOTSB converter where the application of voltage loop control is used.

APPENDICES

The parameters of Tristate Boost DC DC converter and Boost DC DC converter is taken to be same for the purpose of better comparison. The list of system parameters is stated below,

Table I: Simulated System Parameters

System Parameters	Values
Supply voltage	15 Volt
Inductance	275 µH
Inductive Resistance	0.22 Ω
Capacitance	540 µF
ESR	0.218 Ω
Switch Resistance	0.1 Ω
Voltage drop of the Diode	0.7 Volt
Load Resistance	25 Ω
Switching Frequency	50 kHz
Active Load Resistance	2.8544 Ω

The experimental parameters of Boost DC DC converter. The list of system parameters is stated below,

Table II: Experimental Parameters

PARAMETERS	VALUE
Supply voltage	45V
Power rating	36W
Inductance	3mH
Inductance of the active load	2.1mH
Inductive Resistance	2 Ω
Inductive Resistance of the active load	1.4Ω;
Switch Resistance	0.85 Ω;
Capacitance	100uF
ESR	100mΩ
Voltage drop of the Diode	0.8V

Switching Frequency	20kHz
$K_{Pboost1}$	0.06
$K_{Iboost1}$	0.25
$K_{Pboost2}$	0.55
$K_{Iboost2}$	0.35
K_{Pbuck}	0.45
K_{Ibuck}	0.05

Table III: Simulated System Parameters of Dual Output Tristate Boost DC DC Converter with active load

System Parameters	**Values**
Supply voltage	20 Volt
Inductance	275 µH
Capacitance	540 µF
Switch Resistance	0.1 Ω
Voltage drop of the Diode	0.7 Volt
Load Resistance (with resistive load)	25 Ω
Switching Frequency	50 kHz
Active Load Resistance	2.8544 Ω
Active Load Inductance	275 µH
Active Load Capacitance	540 µF

Table IV: Simulated System Parameters of High Gain Tristate Converter.

PARAMETERS	**VALUE**
Supply voltage	45V
Inductance	0.273mH

Inductive Resistance of the active load	1.4Ω;
Switch Resistance	0.1 Ω;
Capacitance	0.540mF
Load Resistance of High Gain Tristate Buck Boost Converter	60Ω
Voltage drop of the Diode	0.8V
Switching Frequency	20kHz
Load Resistance of High Gain Tristate Buck Boost Converter	10 Ω

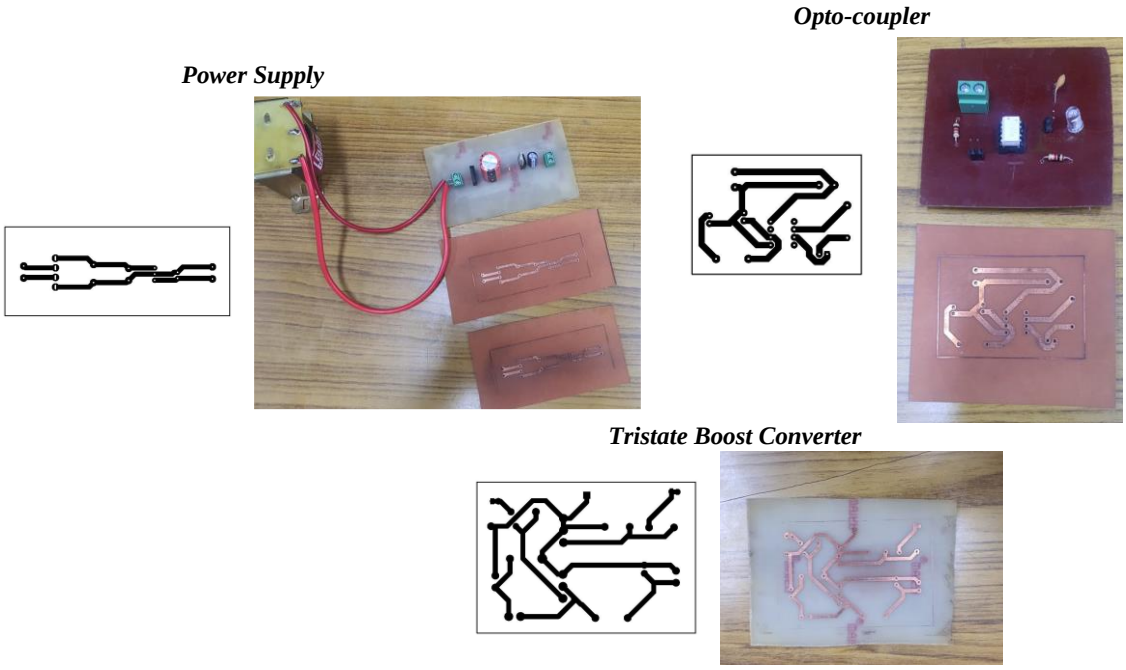


Fig. A1. PCB layout.

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LIST OF PUBLICATION

CONFERENCE PAPER I: Small Signal Analysis of Non-Ideal Tri-State Boost DC-DC Converter for Low Power Circuits

Author names (in sequence as per research paper): **Raunak Karan, Saurabh Mishra; Dr. Mayank Kumar.**

Name of Conference/Journal: **Smart Technologies for Power, Energy and Control (STPEC 2023).**

Conference Dates with venue (if applicable): **10 Dec 23, Venue: KIIT, Orissa**

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Author names (in sequence as per research paper): **Raunak Karan, Saurabh Mishra; Dr. Mayank Kumar.**

Name of Conference/Journal: **ICPC^{2}T 2024.**

Conference Dates with venue (if applicable): **18 Jan 24, Venue: NIT Raipur**

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Date of paper acceptance: **17th Dec 2023**

Website of conference: ICPC2T : International Conference on Power, Control and Computing Technologies (nitrr.ac.in)

Journal PAPER I Title of Paper: **Close Loop Modelling of Non Ideal Boost Converter for Constant Power Load**

Author names: **Mohd Adib, Raunak Karan and Saurabh Mishra**

Name of Journal: ***IETE journal of research***

Status of paper: **Communicated**

CONFERENCE PAPER III: Analysis of High gain Tristate Converter for active loads.

Author names (in sequence as per research paper): **Raunak Karan, Saurabh Mishra; Dr. Mayank Kumar.**

Name of Conference/Journal: **2024 IEEE International Conference on Power Electronics Drives and Energy Systems.**

Conference Dates with venue (if applicable): **18 Dec 24, Venue: NIT Karnataka**

Status of paper (Accepted/Published/Communicated): **Communicated**

Website of conference: Home | PEDES 2024

Declaration and Certificate

ANNEXURE - I

DECLARATION

I hereby certify that the work which is presented in the Major Project-II entitled **MODELLING, ANALYSIS AND CONTROL OF TRISTATE DC-DC CONVERTERS FOR LOW POWERED CIRCUITS** in fulfilment of the requirement for the award of the Degree of Masters of Technology in **Power Electronics and Systems** and submitted to the Department of **Electrical Engineering, Delhi Technological University**, Delhi is an authentic record of my/our own, carried out during a period from January to May 2024, under the supervision of **Mr. Saurabh Mishra**. and **Dr. Mayank Kumar.**

The matter presented in this report has not been submitted by me for the award of any other degree of this or any other Institute/University. The work has been accepted in peer reviewed Scopus indexed conference with the following details:

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Name of Conference/Journal: **Smart Technologies for Power, Energy and Control (STPEC 2023).**

Conference Dates with venue (if applicable): **10 Dec 23, Venue: KIIT, Orissa**

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Raunak Karan
(2K22/PES/12)

SUPERVISOR CERTIFICATE

To the best of my knowledge, the above work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere. I, further certify that the publication and indexing information given by the students is correct.

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(Assistant Professor, Electrical Engineering Dept.)
Delhi Technological University

Place: New Delhi
Date: 18/06/2024

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Dr. Mayank Kumar
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Delhi Technological University

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