DESIGN OF LOW LEAKAGE SRAM CELLS WITH ENHANCED STABILITY FOR NEAR THRESHOLD VOLTAGE REGIME

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Date: (**SUPERVISOR)**

Place: Delhi **MS. ANUPAMA**

Date: **(CO SUPERVISOR)**

ABSTRACT

Operating the SRAM cell at near-threshold voltages is an effective way to achieve higher energy efficiency though it reduces stability and degrades the cell's performance. This thesis presents novel SRAM cells designs characterized by high hold, read stability along with enhanced writability (HSNM/RSNM/WSNM) as well as low leakage power. The proposed devices employ additional read buffer circuitry that eliminates read disturbance issue by decoupling the read path from internal data storage nodes. The feedback-cutting and power-gating based write assist techniques respectively disrupt the internal feedback during read cycle thereby facilitating a smoother write operation. The core circuit of the SRAM cells has been augmented by Schmitt trigger and tristate inverters which enhance hold stability and reduce the leakage power dissipated. The simulation results in 90nm CMOS technology at a supply voltage of 0.5V show that the proposed devices outperform conventional 6T SRAM cell showing 41%/ 297.72%/ 27.2% and 22.62%/ 281.81%/ 12.84% increase in HSNM/RSNM/WSNM respectively. Moreover, the presented designs drastically reduce leakage power dissipation as compared to peers showing as high as 3.45x reduction.

May, 2024 Rachit Bhatia

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I wish express my gratitude to my beloved parents and friends for their understanding andsupport. Above all, thanks to Almighty for blessing and guiding me throughout my life.

Rachit Bhatia

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ACRONYMS

SRAM	Static Random Access Memory
MOS	Metal Oxide Semiconductor Field Effect Transistor
ST	Schmitt Trigger
VTC	Voltage Transfer Characteristics
Vth	Threshold Voltage
HSNM	Hold Static Noise Margin
RSNM	Read Static Noise Margin
WSNM	Write Static Noise Margin

CHAPTER 1

INTRODUCTION

1.1 MEMORIES

Memory is a fundamental component of digital systems, (especially the sequential logic-based designs where output is governed by both present input as well as the past output) where it plays a critical role of storing and receiving data necessary for computation. The efficiency, performance and reliability of memory directly influence the overall functionality of electronic devices, from simple embedded systems to advanced architectures for high power computing. As technology continues to advance, the demand for faster, more efficient and low power designs is occupying greater importance. Memory in digital systems can be classified into two types: as in fig. 1.1, volatile and non-volatile memory.

1. **Volatile memory**

a. Static Random-Access memory (SRAM): A widely used memory design in on-chip cache memories of the CPU due to its high speed and low latency. It stores data in a flip-flop configuration, requiring a continuous power to maintain the stored information.

b. Dynamic Random-Access Memory (DRAM): DRAM, fig.1.2 stores data in capacitors, which need to be periodically refreshed. It is used extensively in main

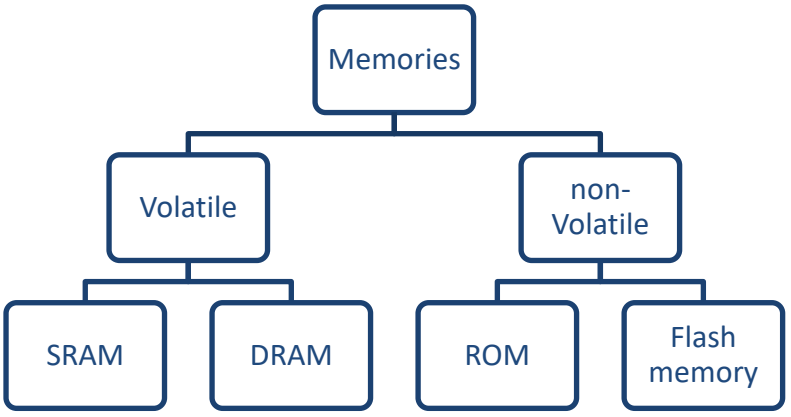


Fig 1.1 Classification of memory

memory due to its high density and relatively lower cost compared to SRAM.

2. **Non-Volatile Memory:**

a. **Read Only memory (ROM):** ROM is used to store firmware and bootstrap loaders that do not change frequently. Data in ROM is retained even when the power supply is off.

b. **Flash memory:** Flash memory is a type of electrically erasable programable read-only memory (EEPROM). Used in variety of applications like USB drives, SSDs, due to its ability to be re-written and its high storage capacity.

A structured arrangement of storage systems in a computing device are shown in fig 1.3 They are organized by varying levels of speed, cost and size. This hierarchy aims to put forward a blend of faster access time and large storage capacities to optimize overall system performance. In the memory hierarchy, SRAM occupy a central role on the cache memory, which can be described as a small high-speed memory located close to the CPU or often integrated in the CPU itself. It can range from few kilobytes (kB) to several megabytes (MB). Below are the various levels of cache:

1. L1 cache: The smallest, fastest and located within the CPU itself.
2. L2 cache: Larger and slightly slower and is sharable between different CPU cores.
3. L3 cache: Even larger and slower and is common for multiple cores.

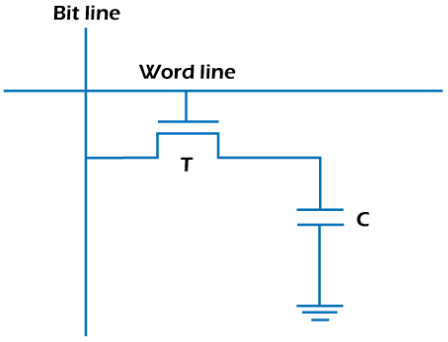


Fig 1.2 DRAM

SRAM stands out among these memory types for its speed and efficiency. Unlike DRAM, which requires periodic refreshing, SRAM retains data as long as power is supplied. However, SRAM is an expensive memory and consumes more power than DRAM. Hence it is used at places where speed is of primary concern.

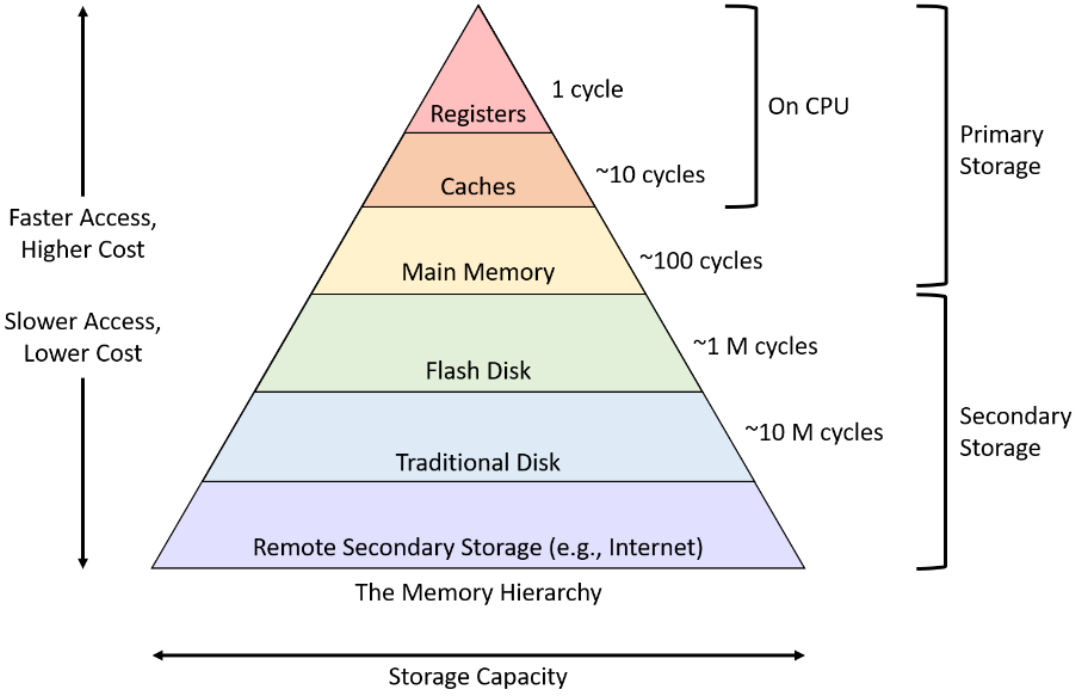


Fig 1.3 Memory Hierarchy

1.2 SUB-THRESHOLD, NEAR THRESHOLD AND SUPER THRESHOLD VOLTAGE REGIMES

Operating the SRAM cell at reduced supply voltages lowers the power requirements. However, this effort compromises on the stability and performance. This section puts light on popular operation voltage regimes thereby reducing the conclusions on which voltage regime should be used for specific applications, as table 1.1. The subthreshold region refers to operating conditions where the supply voltage is below transistors threshold voltage (V_{th}). In this regime the transistors are minimally conducting and thereby current flow is primarily due to leakage. During the sub-V_{th} region, the static power consumption is greatly reduced because the leakage currents depend exponentially on the supply voltage. This makes the subthreshold region really

popular for ultra-low power designs. However, the performance in subthreshold regions is highly compromised as a primary challenge posed is the exponential increase in delay as supply drops below V_{th}. This slow switching severely limits the operation frequency making them unsuitable for highspeed performance. Due to a reduced stability, the designed devices become highly susceptible to data corruption and read/write failures [1]. Due to its ultra-low power nature, subthreshold designs are preferred where power efficiency is critical such as implanted medical devices, sensor networks and other relatively low speed but power efficient architectures.

The near threshold region refers to conditions where the supply voltage is close but slightly above the threshold voltage. The regime is intended to balance a trade-off between power consumed and performance. Both static and dynamic powers are reduced in this regime as compared to super-threshold region of operation. The reductions in power overheads make it attractive enough to operate in the near threshold regions. The near threshold region offers better compromise between power and performance making it suitable for applications with moderate to higher operation frequency. While there are still compromises on the stability considerations but the degradations in the noise margins are less severe in case of the near V_{th} regions. With certain design modifications widely discussed in literature (refer chapter 2), susceptibility to noise and read/write failures have drastically been reduced. It is well suited for portable electronics, wearables and other battery-operated devices where moderate performance and extend battery life is aimed.

The super threshold voltage regime refers to operating the device at voltages which is significantly above the transistor's threshold voltage. The regime may be assumed to be the conventional range of application and is assumed to be applied by default. Here the device consumes high static and dynamic power, have high read and write delays but portray high stability hence eliminating the need for stability enhancement techniques. Memories so exceptional data retention as they

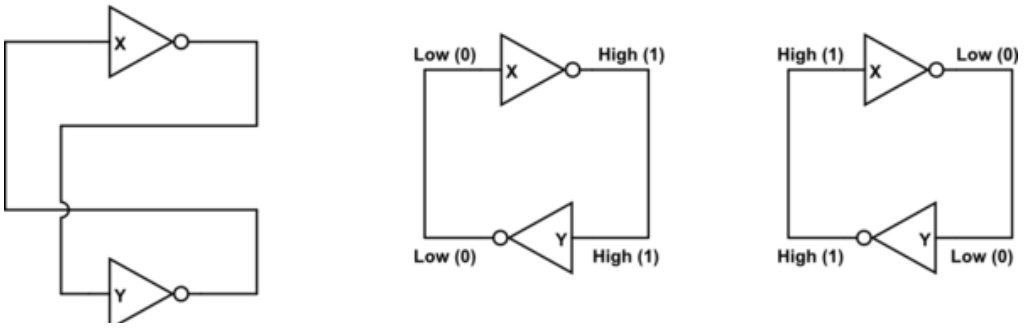
TABLE 1.1 COMPARISON OF SUBTHRESHOLD, NEAR THRESHOLD AND SUPER THRESHOLD VOLTAGE REGIME

Parameter	**Subthreshold voltage**	**Near-threshold voltage**	**Super threshold voltage**
Voltage supplied	Below the transistor's threshold voltage (Vth)	Just above the transistor's threshold voltage	Significantly above the transistor's threshold voltage
Power Consumed	Very low static and dynamic power	Reduced static and dynamic power	High static and dynamic power
Speed	Reduced speed, high delay	Moderate speed, delay	High speed, low delay
Stability	Poor stability	Improved stability	High stability
Leakage Currents	Minimal leakage currents	Low leakage currents	High leakage currents
Complexity	High, requires complex techniques for stability	Moderate, requires some stability enhancement techniques	Lower, less need for stability enhancements
Applications	Ultra-low-power, low-performance applications	Energy-efficient, moderate-performance applications	High-performance applications
Read/ write failures	High risk of read/write failures	Lower risk of read/write failures	Minimal risk of read/write failures
Sensitivity	High sensitivity to process variations	Moderate sensitivity to process variations	Lower sensitivity to process variations
Data retention	Poor data retention	Good data retention	Excellent data retention
Noise susceptibility	High	Moderate	Low
Power gating	Essential for reducing power during inactivity	Useful for additional power savings	Less critical

Suitability	Best for applications with extreme power constraints and minimal performance requirements	Suitable for a balance of power efficiency and performance	Ideal for performance-critical applications where power consumption is less of a constraint
Use cases	Sensor networks, biomedical devices	Portable electronics, IoT devices	Desktop CPUs, servers

are less susceptible to any kind of noises. But due to power thirsty operations it is not a suitable regime for portable electronics thereby making it useful for areas where stability is the most critical aspect and an availability of abundant power supply. Applications like fixed desktop CPUs on site control rooms as well as server stations are typical use cases.

1.3 AN ELEMENTARY MEMORY UNIT



(a) (b) (c)

Figure 1.4 (a) Basic Memory Unit (b) Retention of Logic ‘0’
(c) Retention of Logic ‘1’

The basic concept of an elementary memory is to design a bistable circuit or a circuit which can stay at either of two different states (logic ‘1’ or logic ‘0’) forever if not perturbed. This concept has to be realized using the building blocks of the digital electronics that are CMOS inverters as fig 1.4. The same is realized via the incorporation of minimum of two (or any greater even number) of inverters in a feedback loop fashion. The output of the first inverter is connected

as the input to the second while the output of the second inverter is connected as an input to the first. This connection is popularly known as cross-coupling of inverters.

As evident in the Fig 1.5 when the logic ‘0’ is given as an input to the

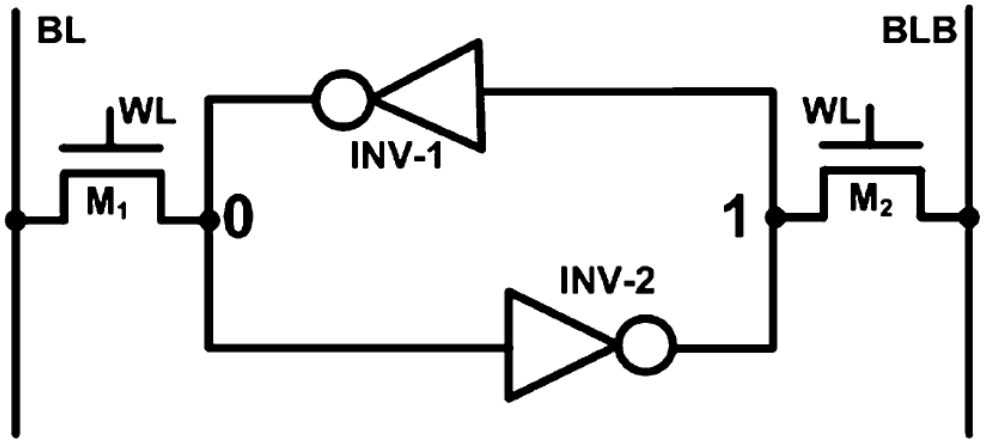


Fig 1.5 Storage of logic ‘0’ with access

inverter X, the output of it becomes logic ‘1’ which is again transfers as the input to inverter Y which outputs logic ‘0’. Similarly, when the logic ‘0’ is given as an input to the inverter X, the output of it becomes logic ‘1’ which is again transfers as the input to inverter Y which outputs logic ‘0’. Hence the circuit presented successfully qualifies as the bistable circuit thereby storing desired logic. Further in order to access the data stored in the bistable circuit i.e performing the read and write operation on the bistable unit we somehow need to provision it through an additional circuit unit is incorporated to the presented draft. Hence two additional access transistors are added to the presented circuit which are connected to the bit line and its complement that serves as two functions in different operation. Nevertheless, these additional transistors affect both speed and stability of the said memory unit greatly as the facilitate read and write operations

As the memory unit needs to hold the data as well when in the hold state, the access transistors M1 and M2 cannot be in the ON state forever so they also need to be controlled. This sense of control has arisen the need for introduction of control signal WL which remains in the state low during the hold state which

will shield the data during the standby mode or the hold mode. This signal WL, however would stay high during the read and write modes thereby facilitating the interaction of the memory unit with the bitline and its compliment.

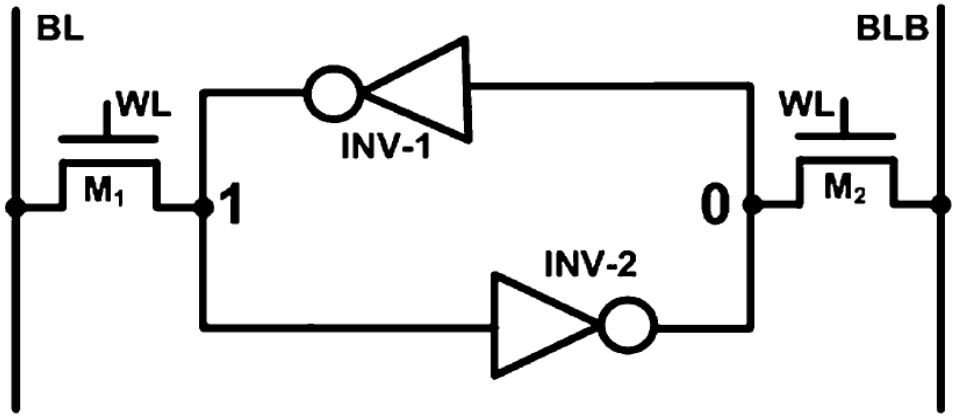


Fig 1.6 Storage of logic ‘1’ with access

1.4 6T SRAM CELL

Two exactly same CMOS inverters are cross coupled to form 6T SRAM. It forms an elementary bistable unit, a latch to create a bi-stable circuit facilitating the storage of a single bit, either logic ‘1’ or logic ‘0’. The data repository nodes (Q

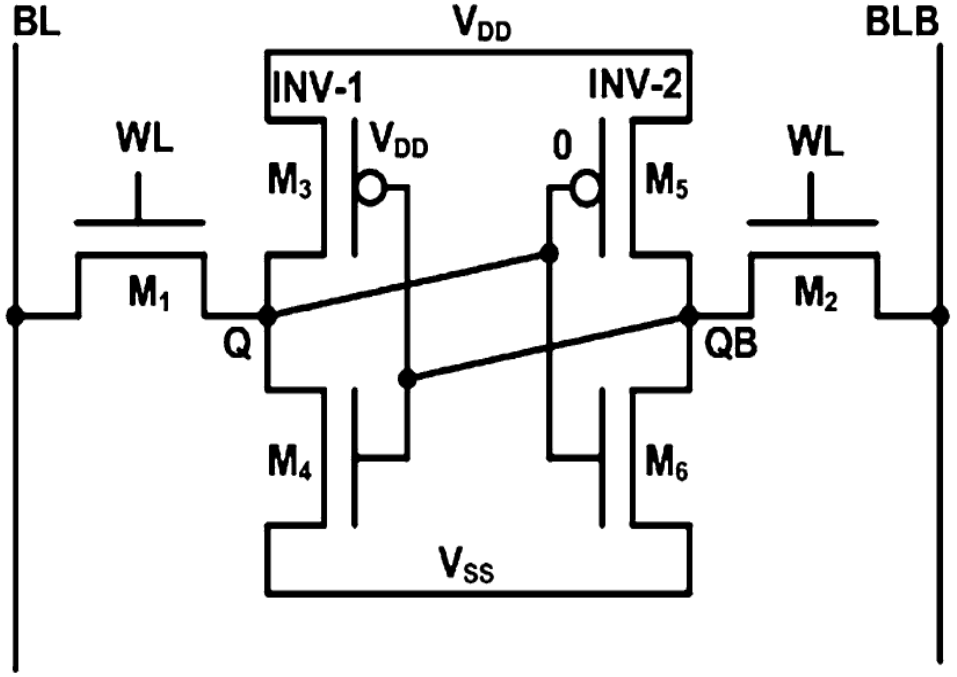


Fig 1.7 6T SRAM cell

and QB) are designed in a fashion that they consistently contain a logic and its compliment, respectively. The dual inverter configuration connected in a feedback format is built up of a pair of pull-up devices (M3 and M5) along with pull-down devices (M4 and M6). A pair of access transistors (M1 and M2), are gated by wordline (WL), realizing a switching action between the latch core and bitlines (BL, BLB) , responsible for the crucial read and write cycles. Notably, the data in SRAM cell can only be preserved till the time the supply rail is active, failure to which leads to data loss. Hence the static random access memory cell presented is classified as a volatile type memory

1.4.1 WRITE OPERATION

In write mode, the bitlines are driven to the desired values by write driver circuitry. For instance, to write '1', BL is set to VDD and BLB is set to 0 V, while BL is set 0 V and BLB set to VDD in case of write '0'. The word line is then activated, turning access transistors and allowing the values on the bitlines to be written into the SRAM cell. The strong voltage levels on the bit lines change the existing stored values on the cross coupled inverters. When WL is turned high, the data enters the bit cell. At the end of the effort, the node QB is pulled trip point if INV-1, so that the feedback loop of the cross coupled inverter begins to work and bitcell is flipped. Here primarily the success of write operation depends on the pull up ratio i.e. W/L ratio of M3 and M1 and that of M5 and M1. In the course of write cycle, a tussle exists among access transistors (M1 and M2) and pull-up network (M3 and M5) especially in the course of entering complement of the retained data into the cell. In the sake of clarity, assuming that the data held previously is '1' and logic '0' is being input in the current cycle. This would translate following status: BLB, WL are rendered VDD and BL is held at VSS . For an efficacious write cycle, QB shall be driven above the trip p of the inverter "INV1" while Q shall be rendered below the trip-point of the inverter "INV2". A tussle hence arises among M1 and M3. Since M1 tries to plunge Q conversely M3 is pulling it towards VDD. A write operation would get completed if effect of M1 dominates. After the switching of inverter, an internal propulsion is created in the circuit till the time new stable state has been achieved. So, an effective write operation is manifested lowering

PR value, realised by employing access transistors (M1 and M2) stronger than pull-up transistors (M3 and M5).

Fig 1.9 shows the set-up employed to quantify write static noise margin (WSNM). A resistive voltage divider is realised by M1 (or M3) and M5 (or M6) for falling BL (or BLB) and retaining point Q (or QB). The event of plunging Q below the trip-point of inverter 2 (INV-2), guarantees completion of write cycle. WSNM is a widely accepted metric of writability calculation. The WSNM is calculated by utilising read voltage transfer characteristics (VTC) and the write

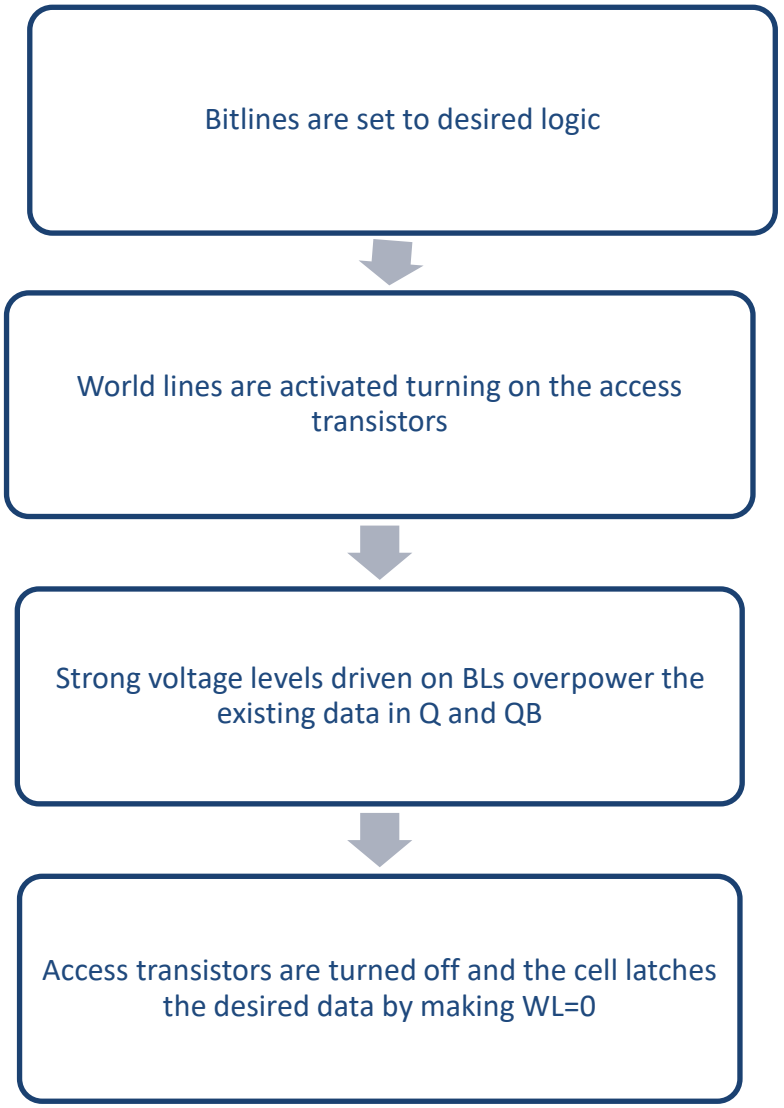


Fig 1.8 Sequence of write operation for 6T

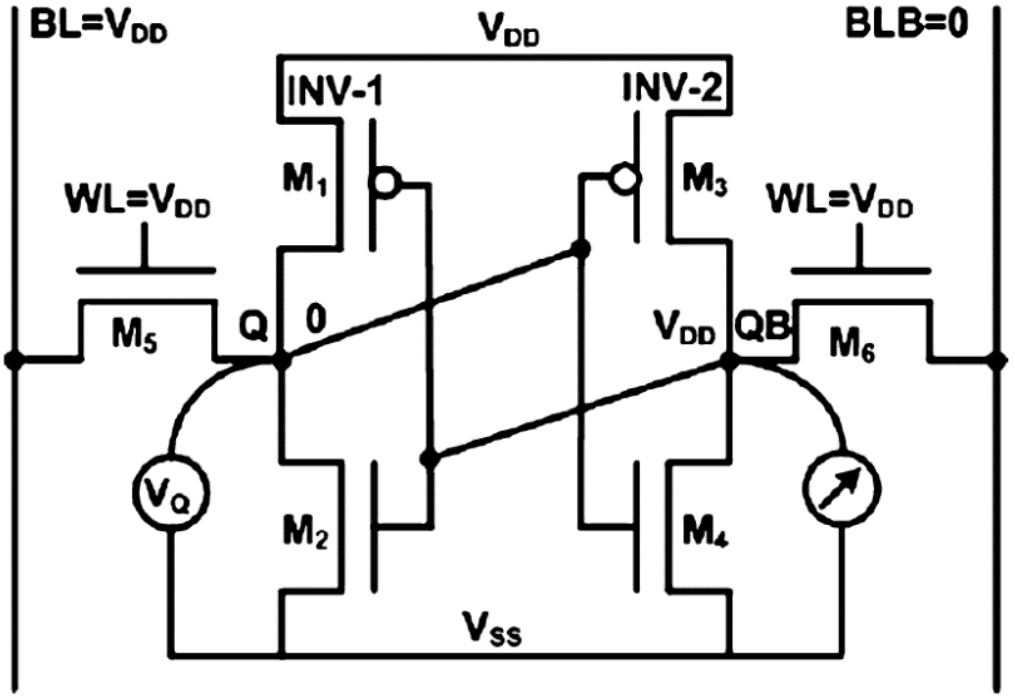


Fig 1.9 Experimental setup for WSNM calculation

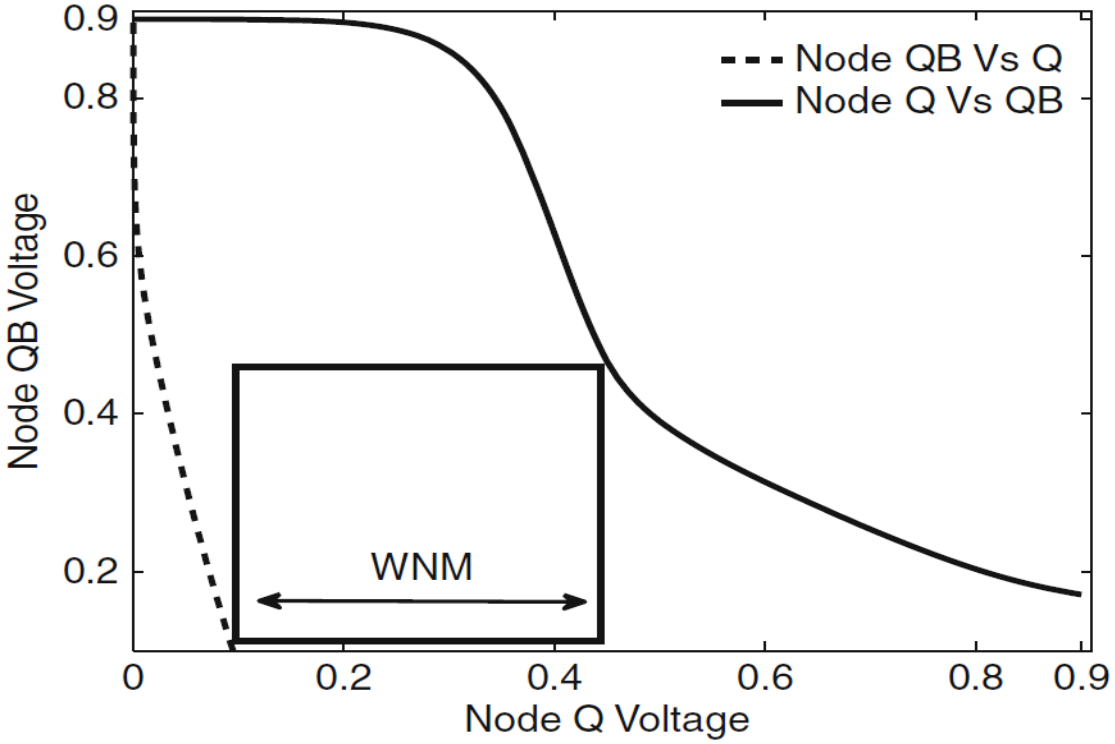


Fig 1.10 WNM Curve

VTC. Read curve is gauged by varying voltage at QB while plotting the voltage at Q, on the other hand, write characteristic is measured by varying the voltage at the Q with BL and WL clamped at VDD and BLB clamped at VSS, plotting the voltage QB. The WSNM can be realised by side of the smallest square incorporated within read and write VTCs, as shown in Fig. 1.10. Notably, in event of WSNM falling below positive values, a write failure is depicted as read and write VTC intersect.

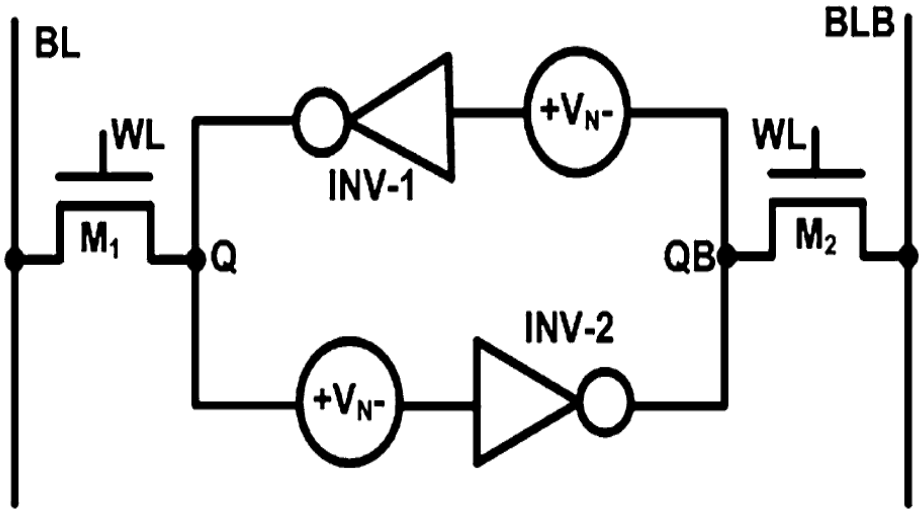


Fig 1.11 Experimental Setup for RSNM calculations

1.4.2 READ OPERATION

Let the data retaining nodes Q and QB are at ‘0’ and ‘1’, respectively, which is in parlance with Fig 1.11. Aiming to read the contents stored, we proceed with the following set of operations: the bitlines (BL and BLB) are undergo a cycle of precharging to the supply voltage (VDD). In a lot of contemporary designs, discussed in literature, power is saved by precharging to an in-between value. Next, the assertion of wordline (WL) to logic ‘1’ takes place. Due to this eventual rise the WL from ‘0’ to ‘1’, either half of the SRAM cell that retains logic ‘0’; it facilitates a gradual discharge of corresponding BL through the access transistor and pulldown network. The conventional 6T, depicted in Fig. 1.12, devices M1

and M4 discharges the capacitive BL. Consequently, the discharge of BLB indicates the storage of logic '1'. Conversely, a discharge of BL from VDD towards VSS denotes the retention of, logic '0'. Hence, the discharge of a particular bitline governs the storage of a particular logic. Specialised circuitry designed for read sensing, known as sense amplifier transforms this differential between BL and BLB to a binary logic. The wordline (WL) is rendered a value 0, signifying closure of read cycle. In the course of a read cycle, the node retaining '0' tries to plunge the corresponding bitline (BL) low through access transistor M1 and pulldown transistor M4. Care must be taken, in design itself that this node storing '0' should not show a kink higher than trip-point of the inverter being gated by it (say INV-2 if Q holds '0').

The read VTCs are utilised to gauge the read stability, manifested via RSNM. The read VTC can be measured by sweeping the voltage at the data storage node Q (or QB) with both bitlines (BL, BLB) and wordline (WL) biased at VDD Let the data retaining nodes Q and QB are at '0' and '1', respectively,

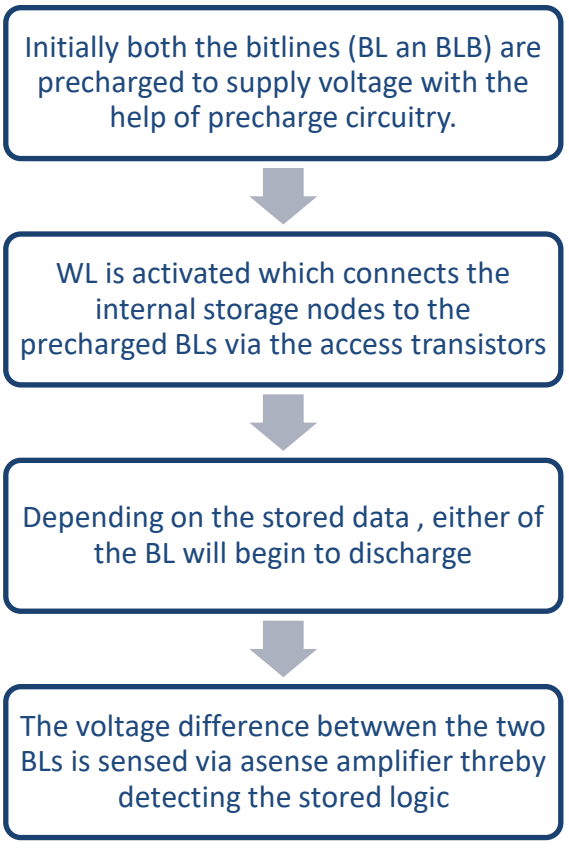
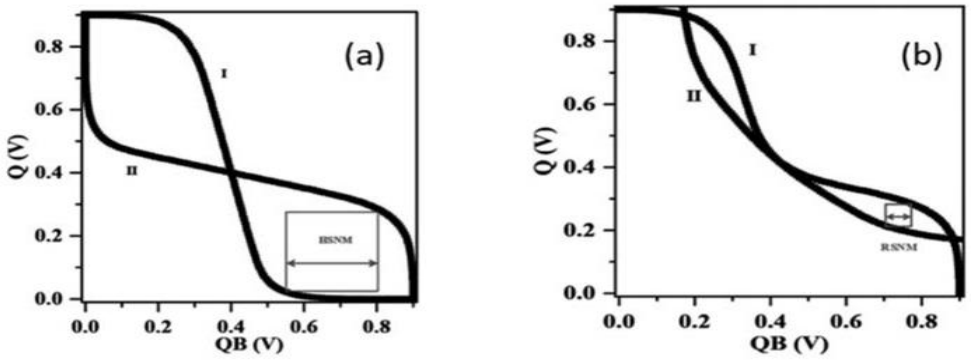


Fig 1.12 Sequence of operations for read operation

which is in parlance with Fig 1.11. Aiming to read the contents stored, we proceed with the following set of operations: the bitlines (BL and BLB) are undergo a cycle of precharging to the supply voltage (VDD). In a lot of contemporary designs, discussed in literature, power is saved by precharging to an in-between value. Next, the assertion of wordline (WL) to logic '1' takes place. Due to this eventual rise the WL from '0' to '1', either half of the SRAM cell that retains logic '0'; it facilitates a gradual discharge of corresponding BL through the access transistor and pulldown network. The conventional 6T, depicted in Fig. 1.12, devices M1 and M4 discharges the capacitive BL. Consequently, the discharge of BLB indicates the storage of logic '1'. Conversely, a discharge of BL from VDD towards VSS denotes the retention of, logic '0'. Hence, the discharge of a particular bitline governs the storage of a particular logic. Specialised circuitry designed for read sensing, known as sense amplifier transforms this differential between BL and BLB to a binary logic. The wordline (WL) is rendered a value 0, signifying closure of read cycle. In the course of a read cycle, the node retaining '0' tries to plunge the corresponding bitline (BL) low through access transistor M1 and pulldown transistor M4. Care must be taken, in design itself that this node storing '0' should not show a kink higher than trip-point of the inverter being gated by it (say INV-2 if Q holds '0').

The read VTCs are utilised to gauge the read stability, manifested via RSNM. The read VTC can be measured by sweeping the voltage at the data storage node Q (or QB) with both bitlines (BL, BLB) and wordline (WL) biased at VDD while monitoring the node voltage at QB (or Q).

Figure 1.11 shows a visual flow chart depicting sequence of events in a read cycle. Furthermore, the noise that occur in the read cycle via the bitlines can be



(a) (b)

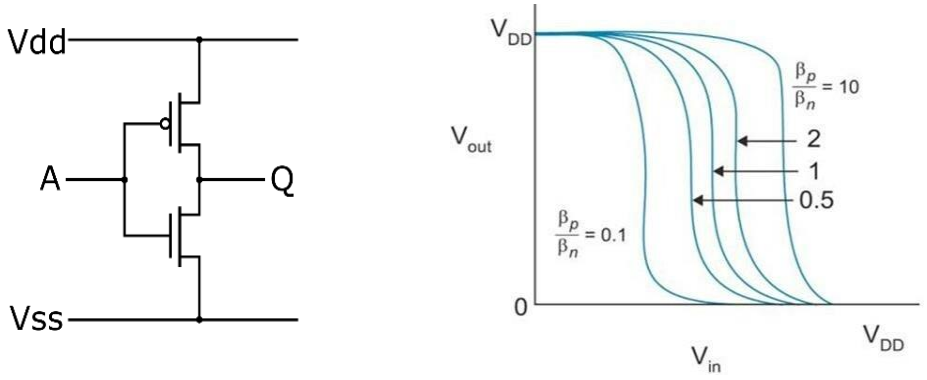
Fig 1.13 (a) Hold Margin Curve (b) Read Margin Curve

realised by adding static voltage sources at the internal storage nodes. The magnitude of these voltage sources greatly affect the stability considerations in the read cycle. To be specific, the event of read cycle commencement is marked by assertion of WL. Node retaining a value '0' gets pulled towards higher voltages by an effect induced by access transistor owing to a voltage division scenario across the pass gate transistors (M1 and M2) and pull-down transistors (M4 and M6). The consequent increase in the transient value of logic '0' stored at the node is a primary cause of degraded stability and is referred to as read disturbance issue. It is primarily determined by the ratio of the pull-down transistor to access transistor, known as bitcell ratio.

1.4.3 HOLD STATE

During the hold state of the SRAM cell the only intention is to retain the withheld data even in the presence of noise. When WL or the word line signal is deactivated, the access transistors M5 and M6 are deactivated. This activity disrupts the access of the internal storage nodes (Q and QB) with the Bls thereby helping the SRAM circuit act as a latch.

The hold static noise margin may be referred to as the capacity of the SRAM cell to effectively store the intended data even in the presence of DC noise voltages. The calculation of the hold static noise margin is done via placing both BL and BLB at a high voltage while keeping the signal WL at a value 0. The activity of keeping BL and BLB at a voltage high helps the cell be prepared for the upcoming read/ write operation thereby securing faster operations. The DC noise of voltages sweeping from 0to VDD are introduced at node Q while



(a) (b)

Fig 1.14 (a) CMOS inverter (b) Cell β variation and VTC

the characteristics of node QB are plotted. In parlance, A DC noise voltage is introduced at QB from 0 to VDD and then on the same graph the characteristic curve obtained at Q is plotted. This curve is referred to as butterfly curve in the literature. The minimum out of the maximum squares which can possibly be accommodated in the either lobe of the butterfly curve is called the hold static noise margin. A higher value of the hold static margin is desirable as it favours a higher data retention in the hold state despite of the presence of DC noise.

When we introduce a noise at the node Q, the transistors M1 and M2 are gated by the node QB due to a cross-couple connection. The presence of a complimentary logic at the node QB does not let the DC noise augment the data stored at the node Q. This phenomenon observed in the cross-coupled circuits is referred to as internal feedback.

The phenomenon of internal innate feedback, though an advantage in the hold state as well as the read operation, poses a threat to the successful write operation, as the circuit displays a degree of inertia to the incoming logic. To overcome this issue, several modifications are proposed of 6T SRAM cell (refer chapter 2).

1.5 COMMON PROBLEMS IN 6T DESIGN

The conventional 6T SRAM cell faces certain issues by design itself. These issues affect the stability and performance of the SRAM cell to a great extent. This section discusses three of the basic design issues which are in the scope of this thesis.

1.5.1 READ -WRITE CONFLICT

The basic building block of any digital circuit is the CMOS inverter as it generate strong logic ‘0’ and logic ‘1’. The CMOS inverter basically comprises two MOSFETs, one is a PMOS (referred to as a pull-up network) while other NMOS (referred to as pull down network). When the input of the CMOS inverter is swept from 0V to VDD, we obtain the characteristics as shown in Fig….

As the mobility of PMOS is less than NMOS, efforts are made equalizing the values of β_p and β_n so that the schematic of CMOS inverter are symmetric. It is observable in Fig. that if we increase the ratio ‘π’, then the schematic of

CMOS inverter moves towards right on the other hand they move towards left if reduce ‘π’.

However, in the SRAM circuit of conventional 6T, it is important that the low internal node (Q) should not rise above the trip-point (switching threshold voltage) of the inverter storing QB, to avoid a destructive read operation. A destructive read operation can be prevented by ensuring a large enough ratio AR, in other words, pull-down transistors (M4 and M6) must be stronger than the access transistors (M1 and M2). AR is defined as

$$AR=\left(\frac{w4/l4}{w1/l1}\right)=\left(\frac{w6/l6}{w2/l2}\right)\text{…….(1)}$$

$$PR=\left(\frac{w3/l3}{w1/l1}\right)=\left(\frac{w5/l5}{w2/l2}\right)\text{……..(2)}$$

In the course of write cycle, a tussle exists among access transistors (M1 and M2) and pull-up network (M3 and M5) especially in the course of entering complement of the retained data into the cell. In the sake of clarity, assuming that the data held previously is ‘1’ and logic ‘0’ is being input in the current cycle. This would translate following status: BLB, WL are rendered VDD and BL is held at VSS. For an efficacious write cycle, QB shall be driven above the trip p of the inverter “INV1” while Q shall be rendered below the trip-point of the inverter “INV2”. A tussle hence arises among M1 and M3. Since M1 tries to plunge Q conversely M3 is pulling it towards VDD. A write operation would

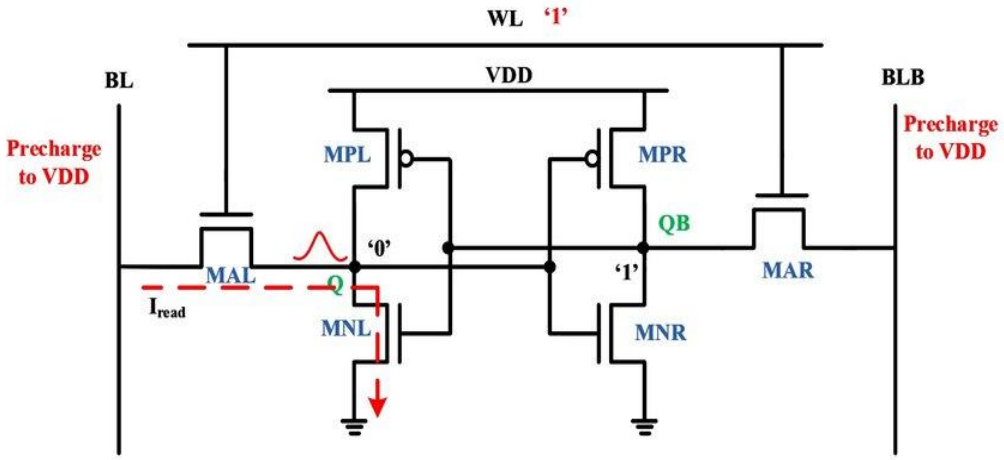


Fig 1.15 Read disturbance in 6T

get completed if effect of M1 dominates. After the switching of inverter, an internal propulsion is created in the circuit till the time new stable state has been achieved. So, an effective write operation is manifested lowering PR value, realised by employing access transistors (M1 and M2) stronger than pull-up transistors (M3 and M5).

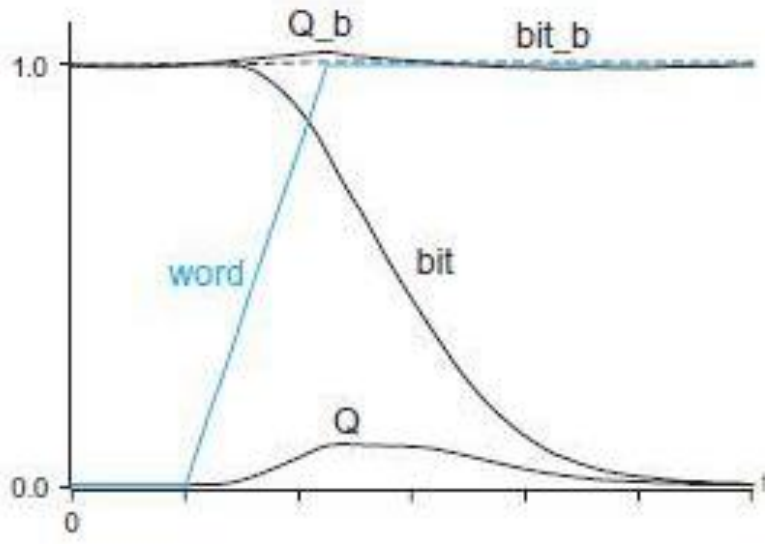


Fig 1.16 Waveform of read disturbance

Unfortunately, larger width of access transistors is an undesirable attribute for the stability of read cycle, adversely affecting the RSNM. This issue of sizing of the pass gate transistor is referred to as read-write conflict as it becomes contradictory to achieve both of them simultaneously.

An issue encountered in the course od read cycle is that both bitlines are precharged at a logical high. This activity must not unintentionally flip the retained value in the storage nodes, as fig 1.16. An intention to avoid this data corruption, demands voltage at node holding ‘0’ be ceased to rise above trip voltage, i.e. higher voltage drop among bitline and ground should occur across the access transistors (M1 and M2) than across the pull-down transistors (M4 andM6). Conversely, the strength of the access transistors should be less than the strength of the pull-down transistors for effective read cycle. In an extension, an effective write cycle, calls for a lowering the voltage at the node holding ‘1’ below the trip point of the other inverter. Therefore, access transistors (M1 and M2) must be stronger than the pull-up transistors (M3 and M5) for a successful

write operation. Keeping it all together, yields the following relation:

$$\left(\frac{w}{l}\right)\text{Pull-up} < \left(\frac{w}{l}\right)\text{Access} < \left(\frac{w}{l}\right)\text{Pulldown}\ldots..(3)$$

1.5.2 READ DISTURBANCE ISSUE

As evident in Fig…., during the read operation both the bitlines are precharged to VDD. Eventually, the word line signal is asserted and the node containing logic '0' (or node Q) starts to facilitate a current flow. In Fig…. a current flow path is shown from BL to ground via transistors MAL and MNL. During this transient phase, there is a slight increase in the voltage stored at node Q.

This transient increase is of a small voltage, say ΔV, which is connected to the input of inverter storing QB, a logic '1' in our case. Due to occurrence of any noise at this point of time, or due toa natural heightened voltage at node Q, the input to MPR and MNR become more susceptible to smaller perturbations. In an event, when ΔV increases the threshold voltage of MNR, it can turn MNR or the pull-down network at QB in ON state. This event can manifest logic '0' at node QB. This phenomenon is called read failure. During the occurrence of a read cycle, we end up flipping the data stored inside the cell, only due to transient changes occurring at the data storage nodes.

The issue of read disturbance gets more pronounced especially if operations of the cell are made at low voltage levels because the cell noise margins are directly proportional to the voltage supplied [2]. The read static noise margin being really small is affected by smaller values of read disturbances. This can partially be corrected by proper sizing of the access transistors. If the pass gate are of minimum size, then there is a marginal improvement is the read static noise margin but this phenomena compromises of the SRAM cells writability. Hence, the read disturbance problem is existing by default in the design of 6T SRAM cell and it cannot get mitigated altogether.

1.5.3 INTERNAL FEEDBACK

The data node at Q gates the inverter storing data QB. Due to a cross coupled nature of the circuit, vice versa is also true. When slight change in data occurs at a particular node due to noise, the compliment of it tries to resist it,

akin to a feedback loop, this adds on to the stability while the circuit is existing in the hold state or is in the read mode. But this inertia resists the incoming logic as well during the write mode of operation.

In a standard 6T SRAM cell, the write operation involves overwriting the data stored in the cross-coupled inverters. This process can be challenging, especially at lower supply voltages (near-threshold or sub-threshold regions), because the existing data is strongly held by the feedback loop of the inverters. Lowering the supply voltage reduces the driving strength of the transistors, making it difficult to flip the stored state. Additionally, the strong positive feedback in the cross-coupled inverters resists changes, exacerbating the difficulty of writing new data.

1.5 SCOPE OF WORK

Significant contributions of this study are:

- Read disturbance free designs are presented.
- Write assist techniques namely power-gating and feedback cutting are incorporated which manifest as higher write-ability to the circuits.
- Leakage power control mechanisms are incorporated in the novel design resulting in extremely low standby power.
- Instead of standard inverters, the core circuits have been augmented with tristate inverter, embedded transistor inverters and ST inverters

1.6 THESIS ORGANIZATION

The content of the thesis is organized into following chapters:

- Chapter I INTRODUCTION
- Chapter II LITERATURE REVIEW
- Chapter III A SINGLE ENDED NEAR THRESHOLD 10T SRAM CELL WITH ENHANCED STATIC NOISE MARGINS
- Chapter IV A LOW LEAKAGE NEAR THRESHOLD 11T SRAM CELL WITH ENHANCED STATIC NOISE MARGINS
- Chapter V SIMULATION AND RESULTS

- Chapter VI CONCLUSION AND FUTURE SCOPE

Chapter I – This chapter gives a brief introduction about memory system, classification of memory, a comparative analysis of various operation voltage regimes and an introduction to 6T SRAM cell. Further the common problems innate in the 6T SRAM design which fall within the scope of this work are also discussed.

Chapter II – It includes a review of the existing SRAM cells configuration and their best practices. A visual glimpse of the recent design schematics have also been illustrated in the same.

Chapter III – A novel 10T SRAM cell designed to operate in near threshold voltage region is discussed in this chapter in a great detail. The power-gating based write assist technique has also been put light upon and various modes of its operation are given an in-depth explanation.

Chapter IV – A novel 11T SRAM cell designed to operate in near threshold voltage region is discussed in this chapter in a great detail. The feedback cutting based write assist technique has also been put light upon and various modes of its operation are given an in-depth explanation.

Chapter V – The proposed cells have been compared with recently proposed designs. There results have been presented and comments on crucial design metrics have been made

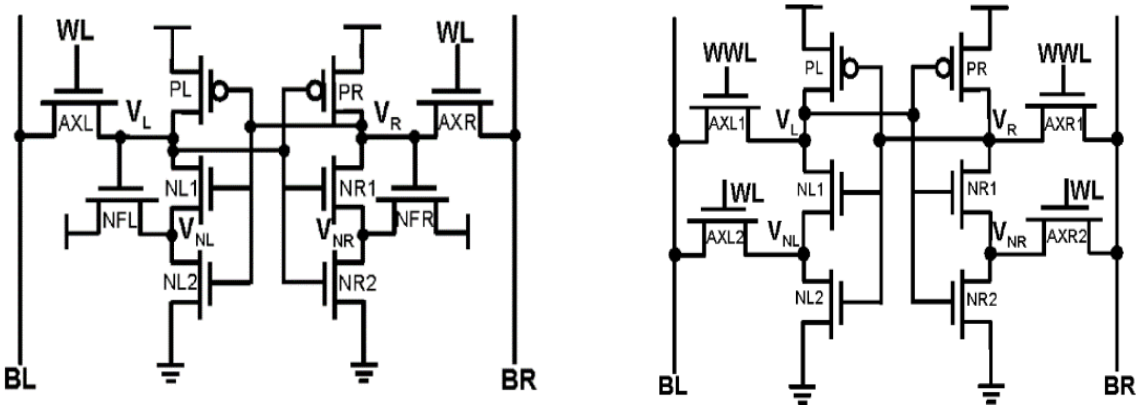
Chapter VI – Concluding remarks about the said designs have been recorded in this section and further scope has been discussed.

CHAPTER 2

LITERATURE REVIEW

2.1 DIFFERENTIAL SRAM CELLS

To overcome the challenges faced by 6T SRAM cell, certain modifications have been proposed in the 6T SRAM cell. The conventional 6T SRAM is augmented with two p type access transistors in [4]. A completely differential cell encompassing eight transistors is presented to bearing higher hold stability and expanded WSNM. The p-type transistors are utilized for the role of pass gates in read cycle and write logic is manifested through transmission gates. However, these benefits bear a cost of high standby power and slower speed. It fails to isolate the bitlines from the data storage nodes thereby inducing read disturbance. Another method widely seen in the literature involves leveraging Schmitt trigger (ST) based SRAM design. The Schmitt trigger topology brings the RSNM to the hold static noise margin as in [5]. The ST-based SRAM bitcells address the read versus write conflict 6T SRAM cell. Enhanced read-stability and write-ability are guaranteed by ST based SRAM than 6T [6]



(a) (b)

Fig 2.1 (a) ST 10T-1 (b) ST 10T-2

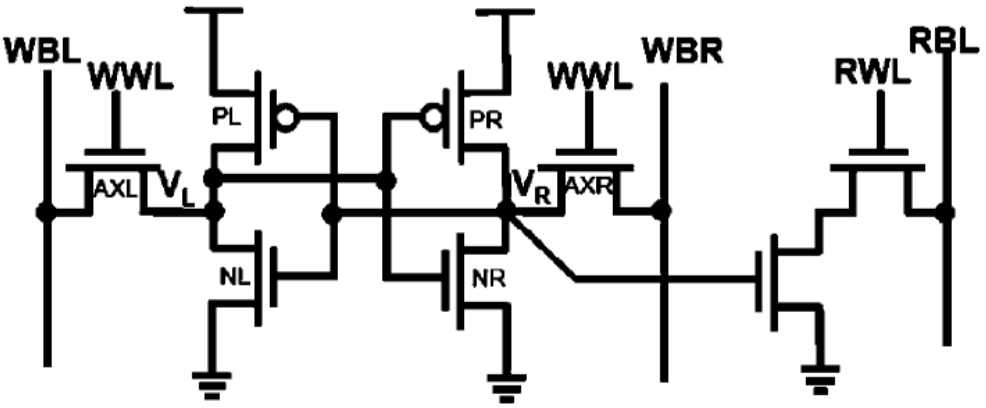


Fig 2.2 6T SRAM with read buffer [7]

With an intention to reduce the gap between read and hold static noise margins thereby equalising them, the read disturbance issue is totally eliminated in [7] by incorporating a novel read buffer. However, Due to addition of the read buffer, additional transistors are added, leading to area and power overheads. Due to this reason, certain modifications in the read buffer circuitry have been proposed in the read buffer configuration. In D10T [8] the read buffer presented is connected to ground signal specific to the operation (VGND). It is only in the read operation than the pull-down network of the read buffer is connected to ground, in all other cases, it is dormant state, hence to reduce on the power consumption, the pull-down network of the read buffer is connected to VDD.

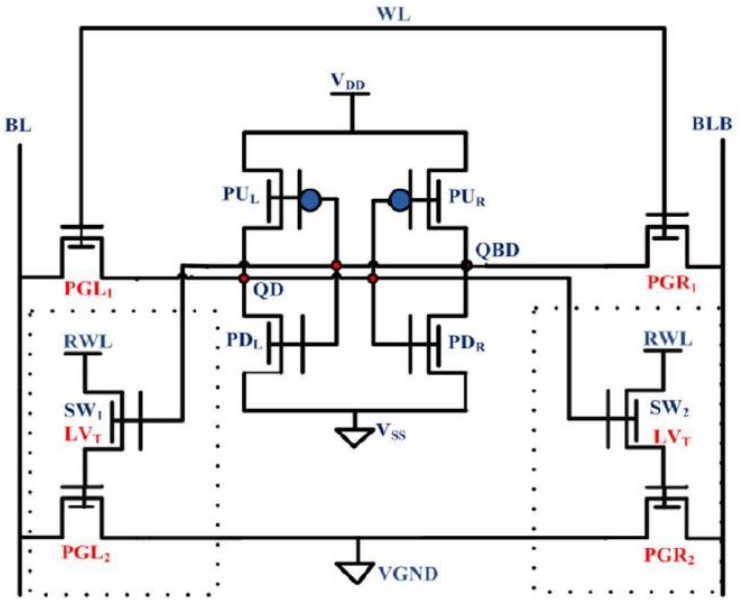


Fig 2.3 D 10T [8]

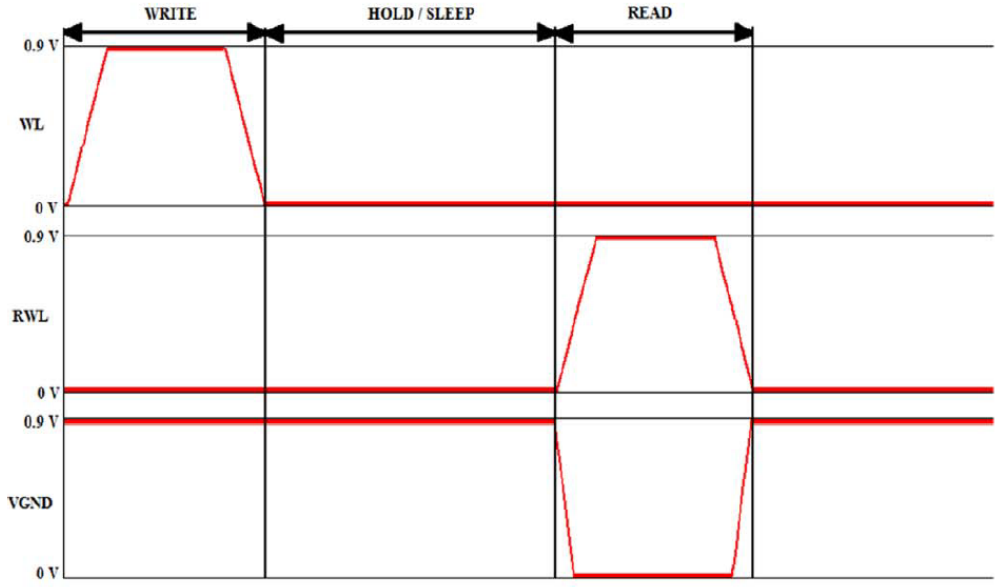


Fig 2.4 Timing diagram of D10T

A higher switching activity results in power overheads [9]. A one-sided read scheme is introduced in [10] with modified read buffers to counter on the leakage currents. by the additional transistors encompassing the read circuitry, certain modifications to the read buffer arrangement have been put forward in [11] All of the designs incorporate of back-to back inverters (PUL-PDL and PUR-PDR) and a pair of pass gates (ACL and ACR). NMOS (R1, R2, R3 and R4) make the architecture for read buffer. While the first has higher data-dependent bit-line leakage of the read line and is meant for better operational metrics. The latter two showcase a fully data-independent leakage values at the read line and are designed towards a reduced power but high packaging.

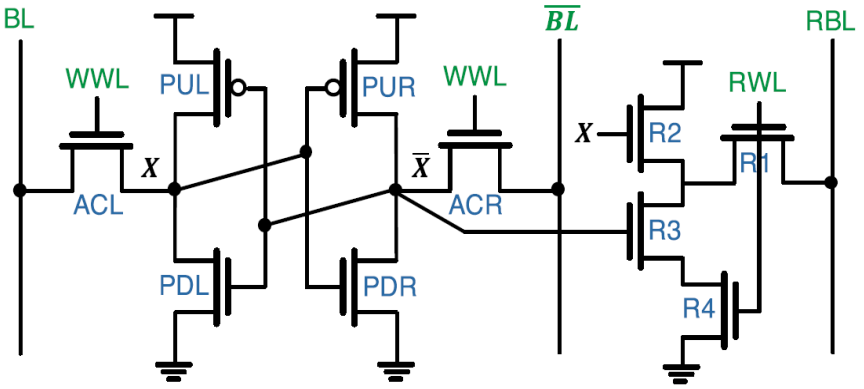


Fig 2.5 Modified read part- a [11]

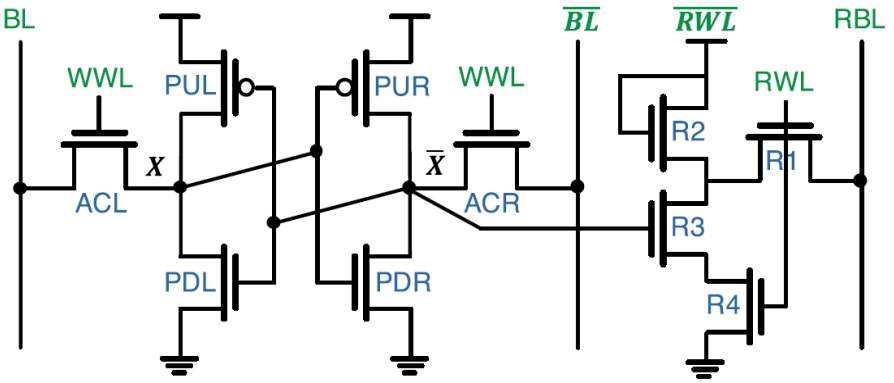


Fig 2.6 Modified read part- b [11]

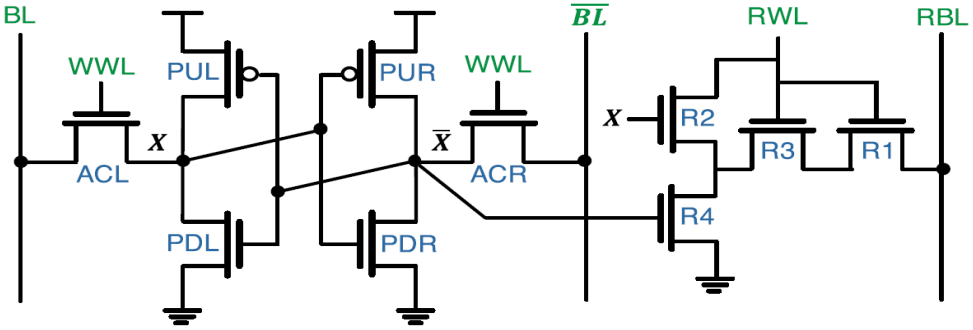
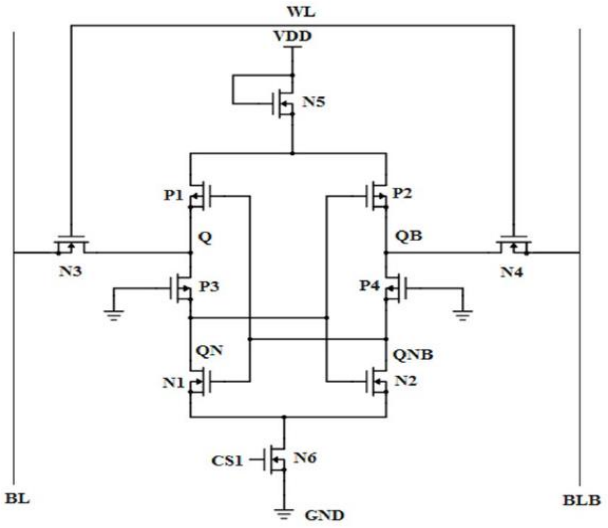


Fig 2.7 Modified read part-c [11]

Claiming an increased noise margin and a low power, the design in [12] is 10T-SRAMaugmented by NMOS transistors to check the power overhead. The design has a core circuit akin to 6T SRAM, with two standard inverters but an addition transistor between the supply rail. It is in diode connected mode to tone down the supply. A transistor gated via CS1, intended to reduce static power takes place between the cross coupled latch and the ground rail. However, stability is proportional to VDD, which is compromised in near threshold regimes. Towards a direction of increased stability, a PMOS transistor is added between N3, N4 and N1, N2 on either half. Not only it prevents the chances of data corruption at low voltages, it adds on by separating data storage nodes and write operation nodes.

2.2 SINGLE ENDED SRAM CELLS

The single ended SRAM cell designs present a considerable advantage of reduction of the bitline charging probability per operation by a whopping 50% [4]. The bitlines employed in the SRAM cells are capacitive in nature. A significant amount



Fog 2.8 Power improved 10T [12]

of the total power consumed goes towards charging of these highly capacitive bitlines. Another advantage posed by the lesser number of bitlines is the reduction in the leakage current. [13].

The LP10T SRAM cell [14] comprises an effectively latched up core circuit encompassing an inverter embedded with an NMOS cross coupled to a ST inverter with a higher 'L' pull -up transistor. A read path decoupled to data repository nodes makes the circuit a read disturb free design mechanism enhances the write performance. Even though RSNM matches HSNM in LP10T, but the design uses two different bitlines for read and write operations. The design may not seem like a read disturbance free architecture, but equivalence of RSNM to HSNM confirm the elimination of read noise.

On the other hand, asymmetric ST9T [15] adopts a structure comprising of a

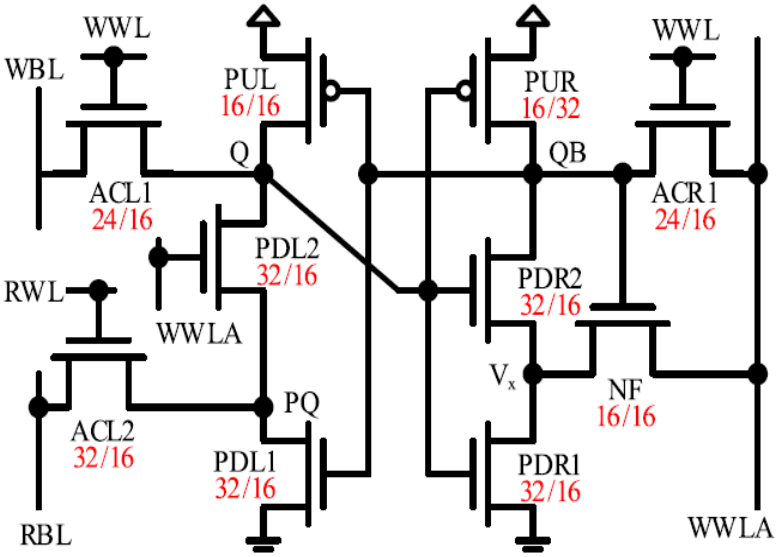


Fig 2.9 LP 10T

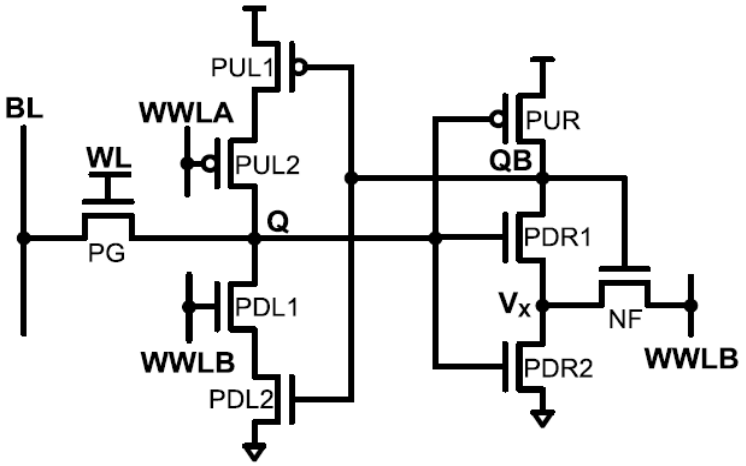


Fig 2.10 ST9T [15]

Schmitt trigger inverter cross coupled with a tristate inverter. A single bitline is utilized in the said design to perform both read and write operations. The occurrence of single bitline reduces the pawer consumption significantly. ST9T also presents low leakage power due to presence of stacking effect. The power gating-based write assist technique showcased in ST9T cuts off pull up/pull down network during write '0'/ '1' operations thereby enhancing the write-ability to a great extent. Another read disturbance free architecture which uses a single ended scheme is presented in [16]. This design uses a single bitline as well as a read buffer which eliminates the read disturbance. Notably, VVSS is driven by the write-0 cells as a single cell performs write '1' in a particular row. Thereby countering the half select problem. However, the enhancement in write-1 ability is not as pronounced due to VVSS

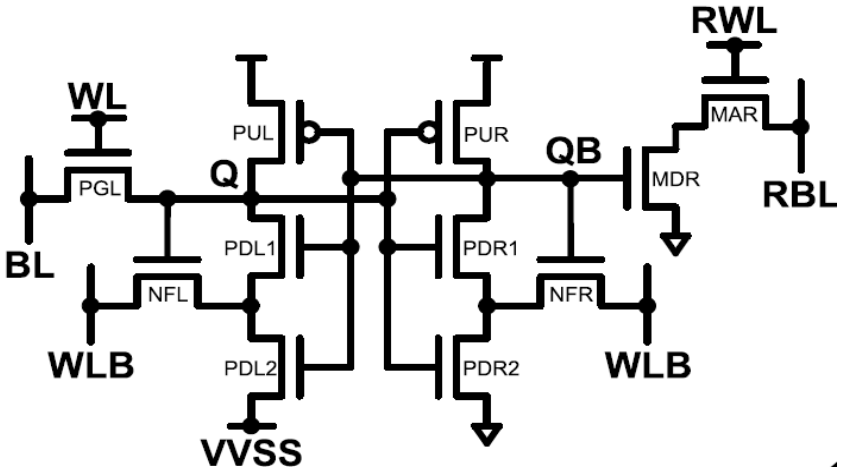


Fig 2.11 ST 11T [16]

being controlled by write ‘0’ cells. A SRAM design with improved stability and power has been proposed in [17]. Though it uses a single bitline and has a separate reading path from true internal storage nodes, but the structure suffers low reading speed.

SLE10T [18] is designed to be extremely stable and dissipate reduced power especially when operating at near threshold and sub threshold voltages. Its core circuit encompasses a combination of an inverter with a tristate inverter. In the course of read cycle, the tristate inverter is turned OFF making the data repository node to be in a free-float state for a transient duration. This makes it easier to overwrite the new logic into the SRAM cell. The cell is also extremely stable when it comes to reading the data as it showcases separate read path for the read current and pulling the node storing ‘0’ to ground state. The cell can dissipate reduced powers due to its one -sided design and transistor stacking effect. Nevertheless, the cell displays a complex structure and a slow operational speed. A single ended 11T structure presented in [19] exhibits RSNM equivalent to HSNM due to fully isolating data storage nodes and enhanced WSNM because of feedback cutting technique. The bit-line however, needs discharging after every write operation, resulting in power intensive operations.

2.3 READ OPERATION WITHOUT PRECHARGE CIRCUITRY

In an effort to save on the power consumption caused by frequent charging/discharging of bitlines, [20] and [21] have proposed cells designed to function at near-V_{th} voltages, presenting relatively higher read and write stabilities.

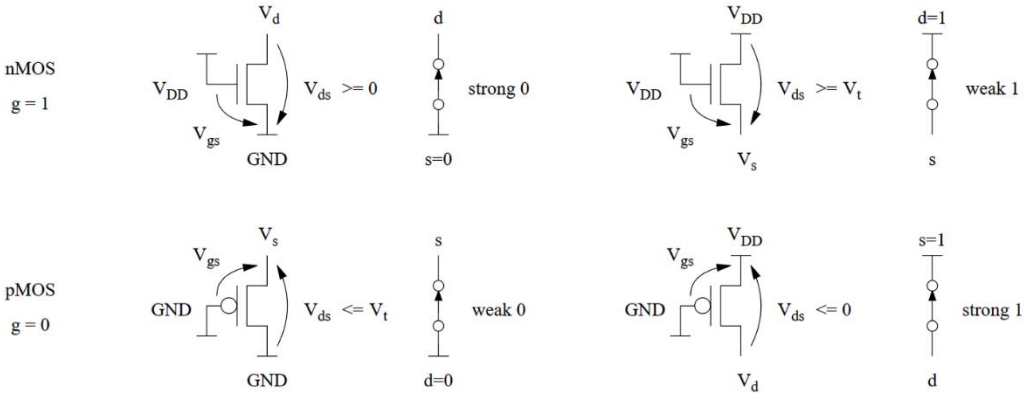


Fig 2.12 NMOS passes strong 0 and PMOS passes strong 1

They refrain from pre-charging the bit-lines preceding read cycle rather they pass the stored value to the bitline itself. It can be compared to writing the values of stored data on the bitline. However,

a) In case of a PMOS transistor, the source is connected to the positive power supply (VDD) and the drain is connected to the output node. When a logic 1 (high voltage) is applied to the gate of a PMOS transistor, it turns off the transistor, allowing the output to be connected to VDD. Therefore, PMOS transistors are efficient at passing logic 1 signals because they conduct when the input is low (0) and block when the input is high (1), which is the opposite behaviour required for passing a logic 1 signal.
b) In an NMOS transistor, the source is connected to ground (0V) and the drain is connected to the output node. When a logic 0 (low voltage) is applied to the gate of an NMOS transistor, it turns on the transistor, allowing the output to be connected to ground. NMOS transistors are efficient at passing logic 0 signals because they conduct when the input is high (1) and block when the input is low (0), which is the opposite behaviour required for passing a logic 0 signal.

Nonetheless, n-type access transistors utilised poses difficulty as they are unable to translate logic ‘1’ effectively during read cycle, thereby passing weak logic ‘1’ to the bit-line.

CHAPTER 3

A SINGLE ENDED NEAR-THRESHOLD 10T SRAM CELL WITH ENHANCED STATIC NOISE MARGINS

3.1 STRUCTURE OF THE PROPOSED 10T

This section introduces a distinctive single ended 10T SRAM cell for operations in near-threshold region characterized by high hold and read stability (HSNM/ RSNM) as well as improved write-ability (WSNM). The core-latch comprises an asymmetric structure consisting of standard inverter cross coupled with a tri-state inverter. The proposed cell eliminates read disturbance by employing an additional read circuitry decoupled from the internal storage nodes. Enhanced write-ability is achieved through a selective power-gating based write assist technique, which interrupts pull up/pull down network during write 0/1 operations. Furthermore, the low leakage power is attributed to single bit-line structure and operation specific grounding of read circuitry.

The schematic of deliberated cell along with status of various control signals is depicted in Fig. 3.1 and Table , respectively. This cell, a 10T SRAM variant with single bitline is designed for operations in the near-threshold region. Notably, N1 to N3 and P1 to P4 comprise the cross coupled latch (a tristate inverter and a standard inverter) and the nodes Q and QB serve as repositories of data

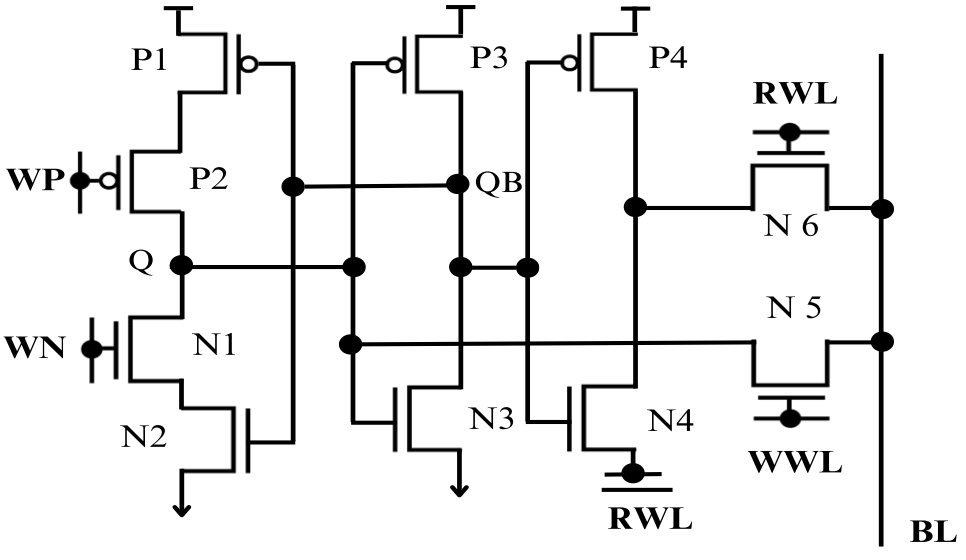


Fig 3.1 Proposed 10T cell schematic

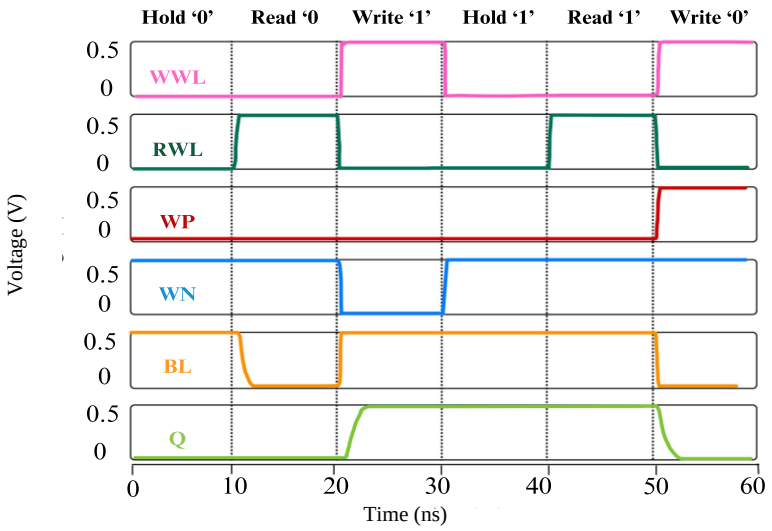


Fig 3.2 Timing Diagram of the proposed 10T cell

storage to retain the data. Transistor N5, controlled through WWL is a write access transistor. On the other hand, P4, N4 and N6 consists of read circuitry. The functionality of initiating write operations in the proposed SRAM cell heavily relies on the power gating signals WP and WN. Moreover, the timing diagram depicted in Fig. 3.2 outlines the timing sequence.

3.2 HOLD STATE

During the hold mode of the depicted SRAM cell, Fig. 3.3 showcases the cell status being utilised. Throughout the hold operation, the latch core preserves the originally stored data. In order to maintain data retention, the storage nodes (Q and QB) are buffered BL by rendering WWL '0'. WP and WN are 0 and

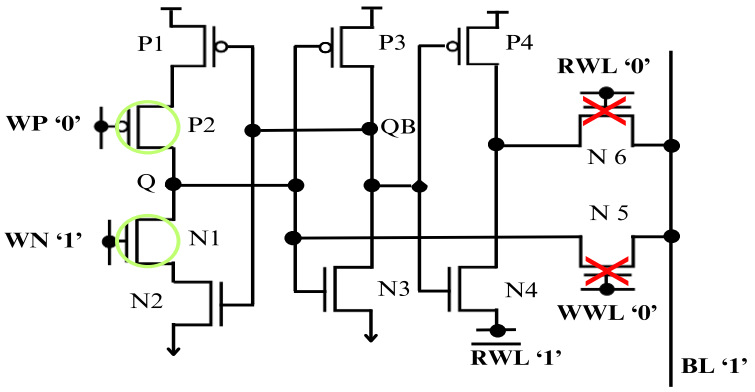


Fig 3.3 Hold State of the Proposed 10T Cell

1 respectively to facilitate data retention. The bitline (BL) is precharged to logic '1' in anticipation of the upcoming read/write operation. Notably, RWL is 0 and N4 is connected to $\overline{\text{RWL}}$ instead of GND rail to reduce leakage power. It must be noted that majority of time during the course of operation of a memory cell, the cell remains in idle or hold state [22]. Hence ensuring a strong cross coupled structure in the core circuit is of primary importance.

TABLE 3.1 STATUS OF CONTROL SIGNALS OF PROPOSED 10T

Signals	**Operations**			
	Hold	***Read***	***Write '0'***	***Write '1'***
WWL	0	0	1	1
RWL	0	1	0	0
WP	0	0	1	0
WN	1	1	1	0
BL	1	1	0	1

3.3 READ STATE

Preceding the execution of the read cycle, BL undergoes an initial precharge to the supply voltage V_{DD}. To ensure data storage in the latch core and to isolate data storage nodes from BL, WWL is pulled to GND while WP and WN are 0 and 1 respectively. The read cycle is initiated by asserting RWL. Transistors P4, N4 (collectively a standard inverter) and N6(read access transistor) perform the read operation. Node QB is connected to gates P4 and N4 acting as the input to the standard inverter based read buffer. In case of logic '0' stored at 'Q' or logic '1' in 'QB', as in Fig. 3.4 (a), current flows into read circuitry from the BL to GND via N6 and N4 thereby discharging the BL, while P4 remains off as it is gated by QB (logic '1' in this case).

Conversely, in case of read '1' the BL, as in Fig. 3.4 (b) retains its initial precharged voltage state with P4/N4 in ON /OFF states respectively. The cell data is retrieved by monitoring the fluctuation of BL. The presented SRAM cell mitigates read disturbance by utilizing a standard inverter based read buffer.

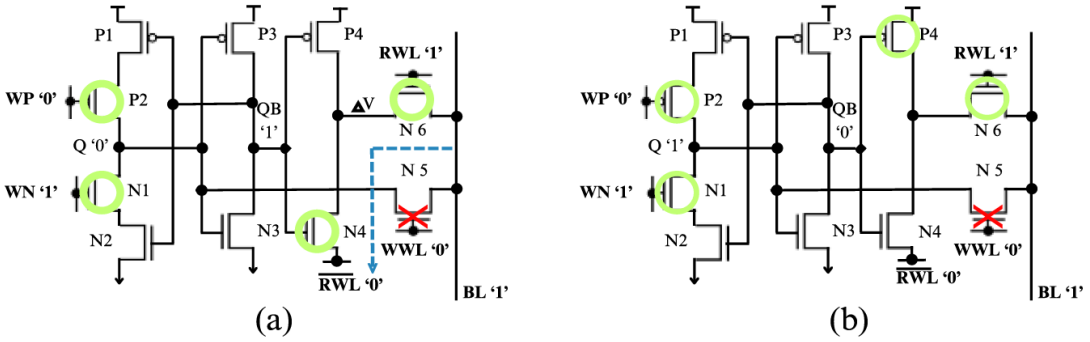


Fig 3.4 (a) Read '0' schematic of Proposed 10T (b) Read '1' of schematic of proposed 10T

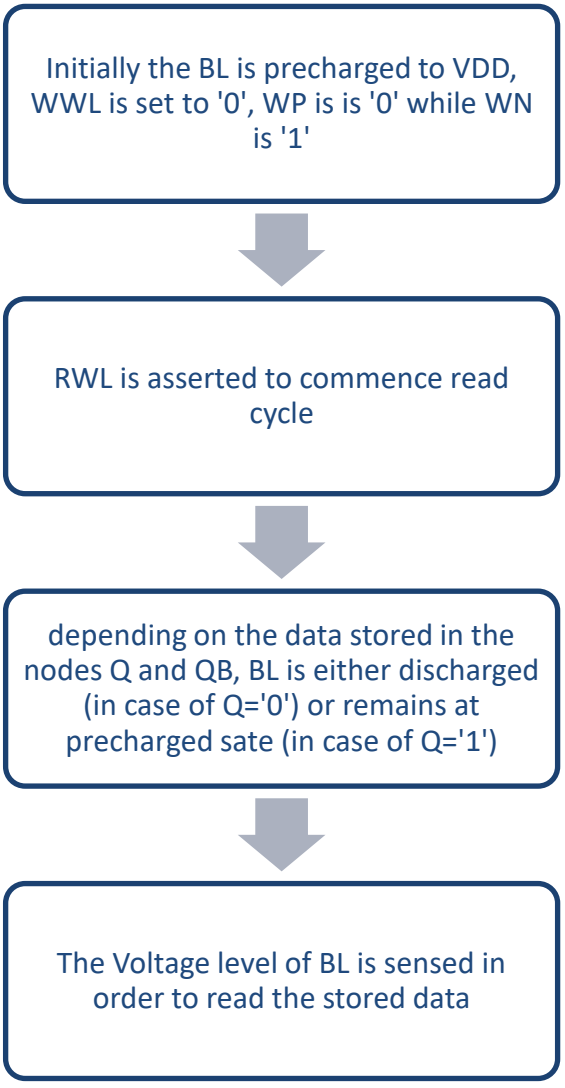


Fig 3.5 Flow chart of read operation

3.4 WRITE OPERATION

The write operation is designed to be specific to the input logic. In the course of write '0'operation, outlined in Fig. 3.6(a), BL is driven to '0', WP transitions from '0' to '1', deactivating P2. This renders pull up network in an off state. Subsequently, write access transistor N5 is turned on by asserting WWL. The power-gated node Q is then forced to '0'. Simultaneously, as Q keeps falling below the threshold voltage, N3 gets turned off as Q is gating N3 and logic '1' is manifested on QB, flipping the contents of standard inverter eventually. During write '1' operation, as portrayed Fig. 3.6 (b), BL is driven to logic '1', WP remains '0' while WN transitions from '1' to '0' to disconnect the path from GND thereby turning off N1. This renders pull down network in an off sate. After this, write access transistor N5 is turned on by asserting WWL. The power-gated node Q is then forced to '1'. It is completely cut off.

Rendering better write-ability as well as relatively lower write access time. It should be noted that WWL is asserted slightly later than BL, WP and WN control signals are stabilized so that pull up/pull down network are turned off.

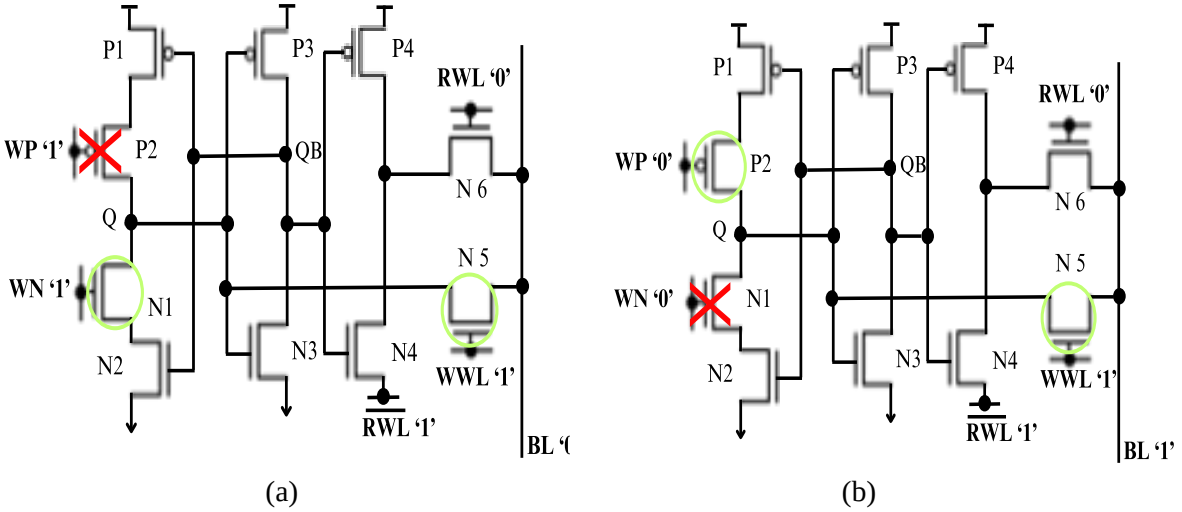


Fig 3.6 (a) Write '0' schematic of Proposed 10T (b) Write '1' of schematic of proposed 10T

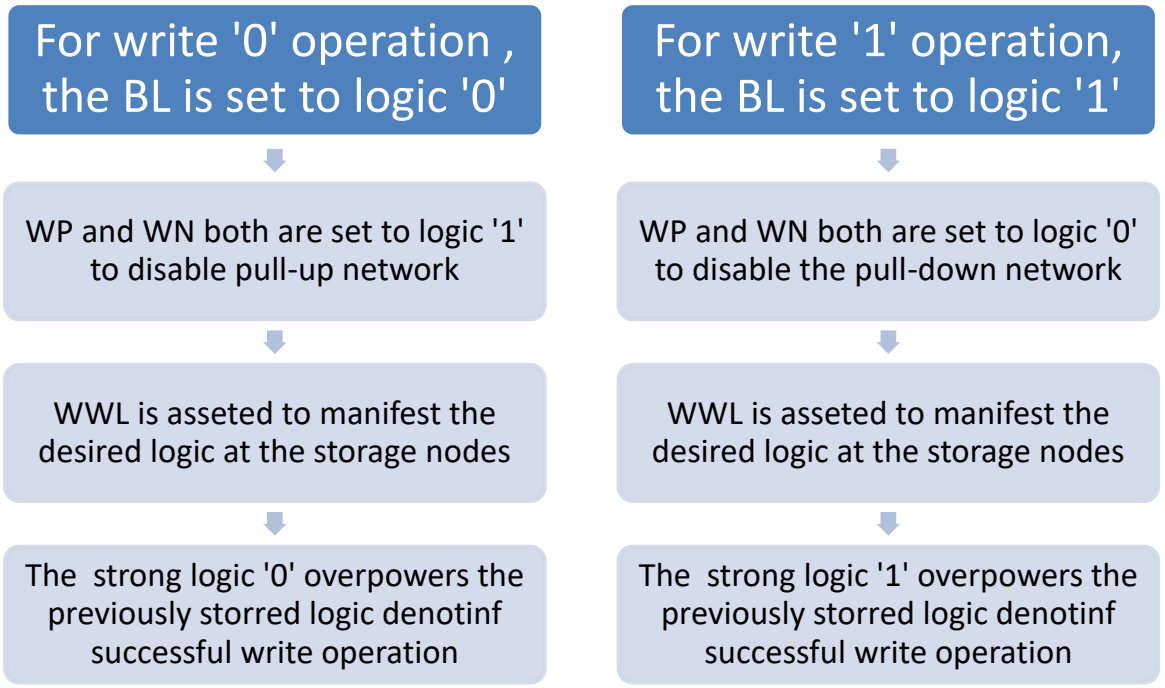


Fig 3.7 Flow chart of write operation

CHAPTER 4

A LOW LEAKAGE NEAR-THRESHOLD 11T SRAM CELL WITH ENHANCED STATIC NOISE MARGINS

4.1 STRUCTURE OF PROPOSED 11T

This paper presents a distinctive 11T SRAM cell for near threshold operation, characterised by high stability (hold/read/write static noise margins) in addition to reduced leakage power. The core circuit comprises an asymmetric design of a transistor infused standard inverter cross coupled with a Schmitt trigger inverter. Whereas read disturbance is eliminated via an additional read circuitry for decoupling internal storage nodes, higher writability is achieved through a write assist technique which disrupts the internal feedback during the write cycle.

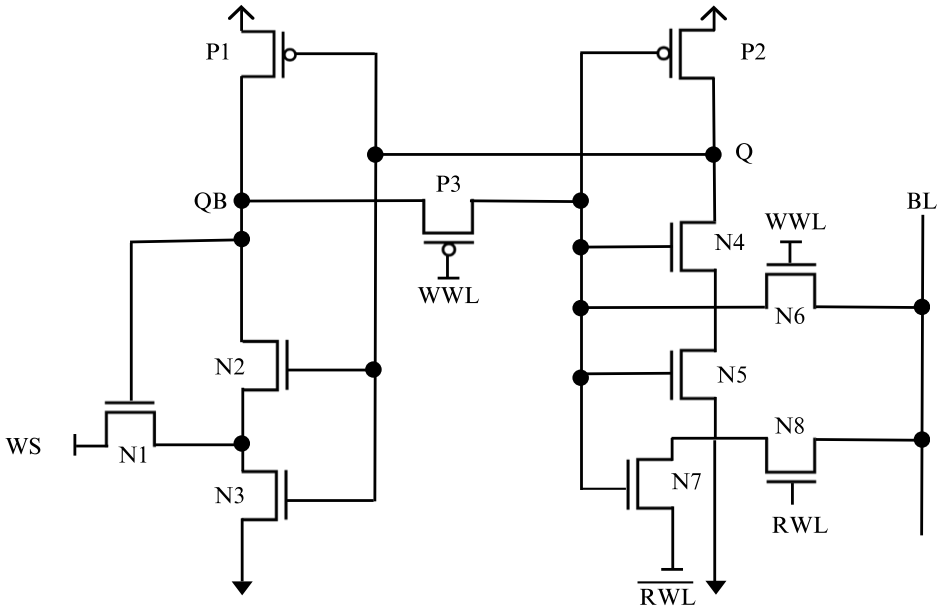


Fig 4.1 Proposed 11T cell schematic

TABLE 4.1 STATUS OF CONTROL SIGNALS OF PROPOSED 11T

Signals	***Operations***			
	Hold	***Read***	***Write '0'***	***Write '1'***
BL	1	1	1	0
WWL	0	0	1	1
RWL	0	1	0	0
WS	1	1	1	0

Fig. 4.1 and Table 4.1, show the schematic and status of control signals for the deliberated SRAM cell, respectively. The put-forward 11T SRAM cell with a single bitline architecture is designed for near-threshold voltage operations. The cross coupled core circuit is structured by transistors P1-P2, N1-N5 and a feedback disruption transistor P3, alternatively Q and QB serve as internal storage nodes. Transistor N6 is the write access transistor while transistor N7 and N8 comprise the read circuitry. The write word line signal (WWL) performs dual function providing access to BL as well as cutting of the internal feedback during the write cycle.

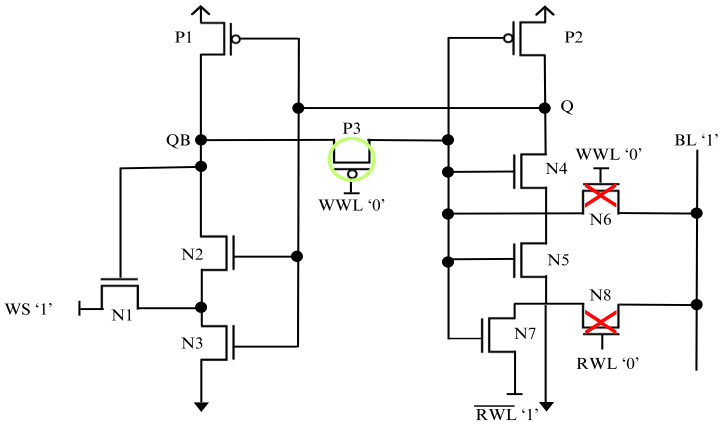


Fig 4.2 Hold State of the Proposed Cell

4.2 HOLD STATE

During the hold mode presented in Fig. 4.2, the core latch circuit preserves the data stored originally. In that order, WWL and RWL are set to '0' disrupting the access of BL towards QB and Q. The signal WS is set to '1' which increases the

trip voltage of N2, manifesting better hold stability. Notably, N7 is connected to $\overline{RWL}$ instead of GND rail to reduce leakage power. The presence of a ST inverter in the core cell increases the hold stability further more. The timing diagram can be referred in Fig. 4.3.

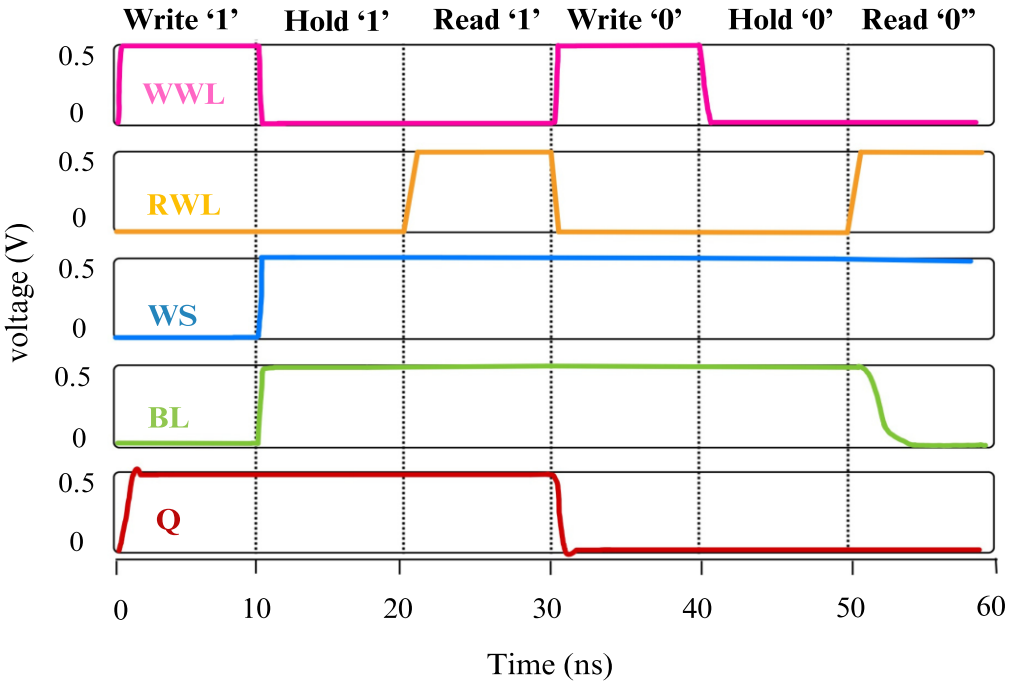


Fig 4.3 Timing Diagram of the proposed cell

4.3 READ OPERTATION

To ensure data retention in the course of read operation, WWL retained at '0' while WS is given a value '1'. Preceding the read cycle initiation, BL passes through an initial precharge. RWL is asserted to commence the read operation by turning on N8. In the course of read '0' (Fig. 4.5(a)), the gate of N7 is connected to logic '1' (manifested through QB) thereby facilitating the current flow from BL to $\overline{RWL}$ (ground in this case) via N8 and N7. The consequent discharge of BL is perceived via the sense amplifier, leading to a successful read '0' operation. On the other hand, for an operation to read logic '1' (Fig. 4.5(b)), the gate of N7 is linked to logic '0' (manifested by QB) which turns transistor N7 OFF. As a consequence, there is no current flow from BL via N7, so the BL remains at its initial state, containing the value of logic '1'. Notably, throughout the read

operation, there is no transient change in the logic stored at either of the internal nodes (Q and QB). The presence of an isolated read circuitry which makes the read path decoupled from data storage nodes hence rendering the proposed design as read disturbance free.

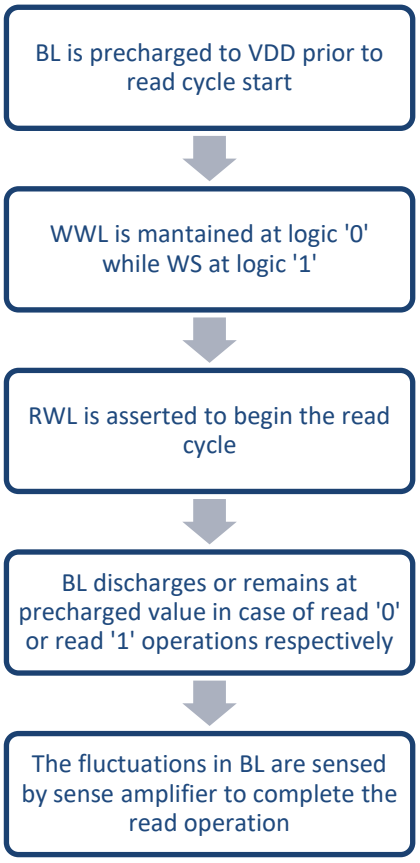


Fig 4.4 Flow chart of read operation of proposed 11T

4.4WRITE OPERATION

The internal feedback due to cross-coupling of inverters in a SRAM core circuit controls its writability. The preceding value stored within the cell poses a degree of inertia to the incoming logic in 6T SRAM as QB gates the node containing Q. Hence feedback cutting based write assist technique is utilized in

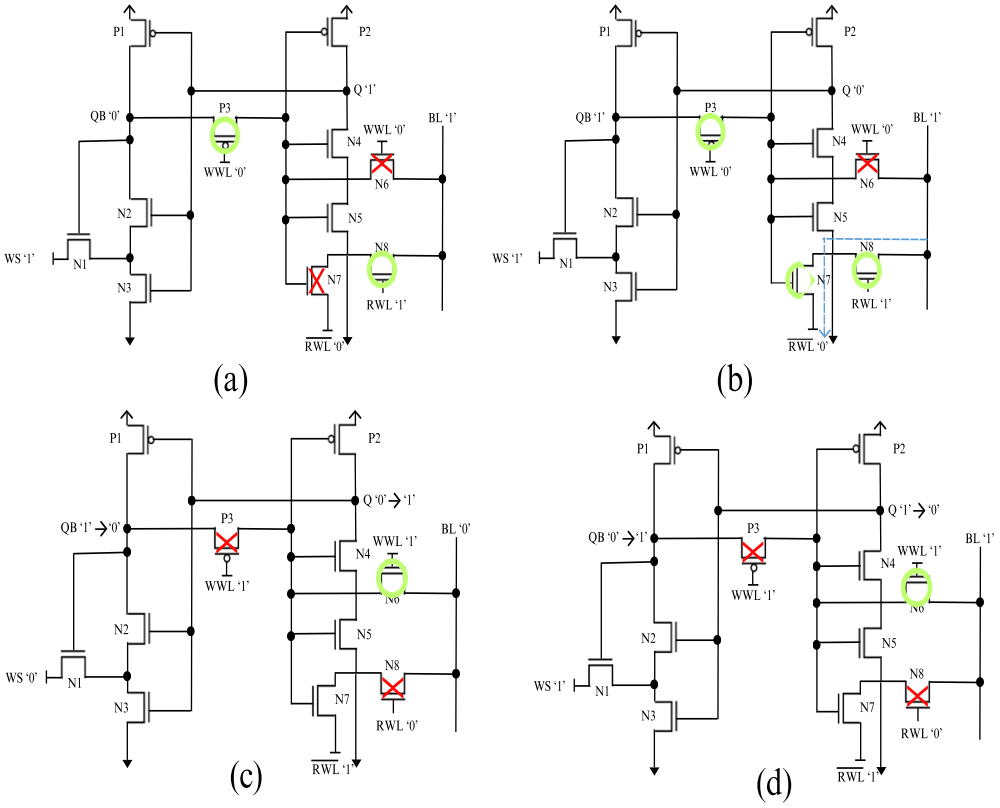


Fig 4.5 Operations of Proposed SRAM Cell
(a) Read ‘0’, (b) Read ‘1’, (c) Write ‘0’, (d) Write ‘1’

the proposed design which collapses the internal feedback during the write cycle thereby rendering a high writability. The commencement of write cycle is marked by setting WWL to logic ‘1’. This performs the dual function of proving BL access via N6 as well as cutting the internal feedback through P3. Status of the BL and WS is specific to the logic being written while RWL is set to ‘0’ throughout the read operation. In the course of write ‘0’ operation (Fig. 4.5(d)), BL and WS both are driven to logic ‘1’. This manifests a logic ‘0’on Q and an eventual manifestation of logic ‘1’ (Q being connected to input of ST inverter). On similar lines, during the course of write ‘1’ operation, WS and BL are driven to logical low, manifesting logic ‘1’ onto Q and eventually translating logic ‘0’ at QB. The presumption of setting WS to ‘0’ in this case aides the process of translation of logic ‘0’ on QB by reducing the effective threshold voltage of the ST inverter and aids the write operation in latent fashion. Owing to the feedback cutting mechanism, the writing data becomes swift as the prestored data does not interfere

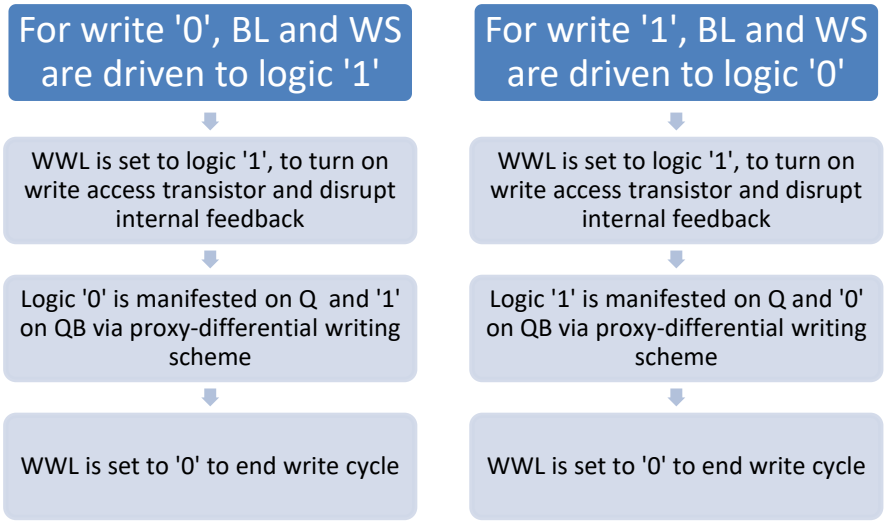


Fig 4.6 Flow chart of write operation of proposed 11T

with the incoming logic. Additionally, the signal WS helps with operation specific manipulation of the trip voltage of the Schmitt trigger.

CHAPTER 5

SIMULATION RESULTS AND COMPARISON

5.1 EVALUATION OF PROPOSED 10T

The proposed SRAM cell undergoes assessment against a range of design metrics, juxtaposed with recently published LP10T, D10T, ST9T and conventional 6T SRAM cells. To ensure fairness of comparison, all the SRAM cells referenced previously are crafted employing 90nm CMOS technology. A supply voltage of V_{DD}= 0.5V has been applied for the simulation purposes. For evaluation of stability, static noise margins are utilised which are calculated using butterfly curves. Leakage power is calculated in the hold state. The speed of the device on the other hand is calculated using read delay and write delay values.

5.1.1 HOLD STABILITY

In the hold state, the Hold static noise margin (HSNM) serves as quantitative metric, indicating the magnitude of noise voltage that the SRAM cell can withstand in the hold state without altering the data stored [14]. Higher HSNM is preferable as it indicates better data retention amidst noise. To determine HSNM, the side length of the minimum of the maximum squares formed in either lobe of the butterfly curve of the hold state is taken [14]. Fig 5.1 depicts butterfly curve for hold state. In comparison to previously proposed designs, as in Fig. 9 the proposed design showcases greatest value of HSNM measured at 0.168V. It demonstrates enhancements of 22.62%, 11.25%, 7.69%, 5% in HSNM in contrast to 6T, LP10T, D10T & ST9T respectively. The augmented static margin in the hold state is attributed to a robust latch core comprising a tri-state inverter (utilising stacking effect) connected in cross couple with a standard inverter.

5.1.2 READ STABILITY

Read stability is ascertained by determination of read static noise margin. RSNM reflects the SRAM cell's capacity to execute read operation without altering the contents retained in the latch core. Higher value of RSNM is preferable to ensure uninterrupted read operation without data flipping. Here, RSNM is quantized via butterfly cure analysis, as in Fig. 5.2. The minimum out of the maximum squares possibly accommodated in either of the lobes of the butterfly curve is called SNM [14]. The proposed design and D10T are considered to be immune to read disturbance as they incorporate a read buffer circuitry, separating the storage nodes during read operation. Hence RSNM and HSNM for both of them are equivalent. However, ST9T and 6T are not read disturbance free as their read paths involve the data storage nodes. Temporary increase in the stored value of logic '0' during the read-0 operation makes the design more vulnerable to data corruption thereby resulting in smaller RSNM. In 6T, the only way to improve RSNM is to alter the transistor sizing. However, ST9T improves read stability by the virtue of strong Schmitt-trigger transistor, reducing the effect of this transient voltage increase during read '0'. Read disturbance seems to occur while storing '0' in the LP10T as

well, but the RSNM is further enhanced by a distinct read route and a pull-up transistor in the ST inverter that is twice as long. The cell offers the highest read static noise margin of 0.168V amongst the cells under comparison, visualized in Fig. 9. It shows 281.81%, 57%, 11.25% and 7.69% enhancement in RSNM in comparison to 6T, ST9T, LP10T and D10T cells respectively.

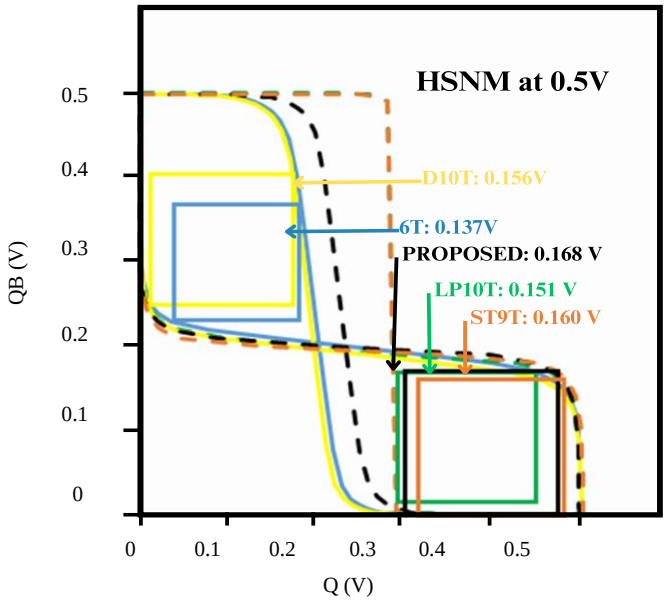


Fig 5.1 Hold Static Noise Margin

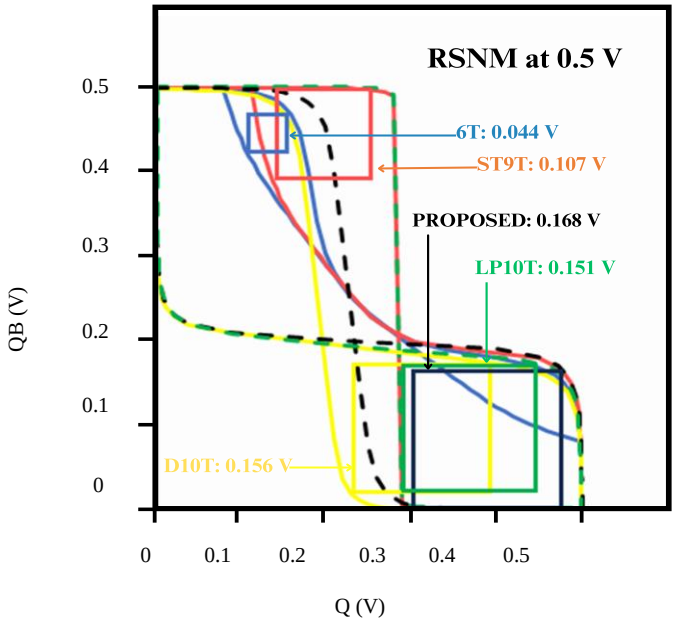


Fig 5.2 Read Static Noise Margin

5.1.3 WRITE -ABILITY

Assessing an SRAM cell's capacity to accurately write data amidst noise involves calculating its WSNM using butterfly curve analysis as elaborated in the earlier sections. The process is visually represented in Fig. 5.3. Given differing conditions in write '1' and write '0' operations for single ended structures, calculation of WSNM for the worst-case operation has been taken into consideration. The conventional 6T and D10T have low write SNM due to absence of any write assist mechanism. Conversely ST9T exhibits higher WSNM owing to power-gating write assist technique. LP10T, leveraging its ST inverter-based latch core, a proxy-differential writing scheme and write assistance shows further enhancement in WSNM.

The proposed device has a tristate inverter-based latch core and a power-gating scheme which cuts off the V_{DD}/ GND rail from the storage node during write '0'/ '1' operations. Proposed design increases WSNM by 12.84% / 7.71% / 4.12% / 2.29

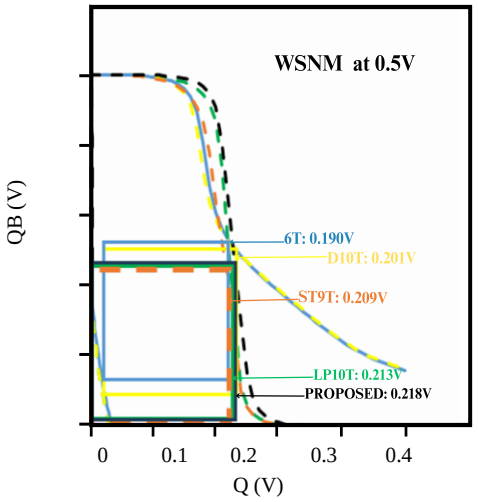


Fig 5.3 Write static Noise Margin

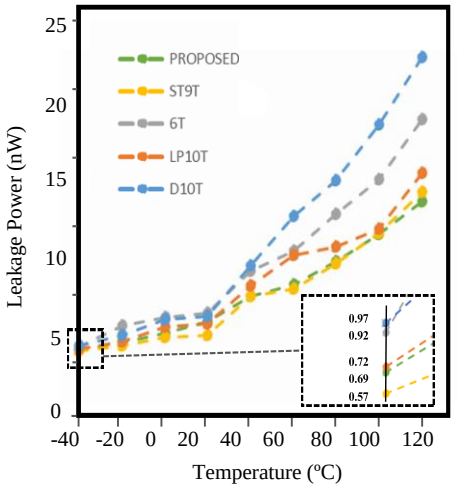


Fig 5.4 Variation of Leakage Power with Temperature of SRAM cells

compared to 6T / D10T / ST9T / LP10T cells respectively. The Fig. 7 shows write butterfly curves of devices under comparison. Fig. 9 depicts the HSNM, RSNM and WSNM of the corresponding SRAM cells graphically.

5.1.4 LEAKAGE POWER

In low power SRAM design, leakage power is a critical metric, especially since SRAM cells frequently stay in the whole state without undergoing read or write operations [2]. Subthreshold leakage current and gate leakage current are the two primary components of the total leakage current. The latter has a dominant value compared to the other. Leakage current increases as a result of inclusion of more circuitry [6]. In our proposed design, transistor N4, which is a part of the read circuitry, is selectively grounded by connecting it to $\overline{\text{RWL}}$ instead of the group aiming to reduce additional leakage current. The current value of 3.37nW would have resulted in a 73.36% increase in leakage power if this connection had been made to GND rail instead. The higher bitline count of the dual ended D10T results in high leakage power. Conversely, because standard 6T does not possess any additional read circuitry, its leakage power consumption is marginally lower. LP10T demonstrates a further decrease in leakage power owing to a stacked transistor in the latch core and a twofold length pull up transistor in the ST inverter. Our proposed device exhibits even lower leakage power, primarily due to two factors First, the latch core's tri-state inverter creates a stacking effect that aids leakage reduction. Second, as discussed earlier, selectively grounding transistor N4 of the read buffer reduces leakage current.

Unlike others ST9T does not use additional read circuitry and is a single ended structure, employing a Schmitt Trigger inverter and a tri-state inverter in its latch core. The Schmitt trigger effectively increases the threshold voltage, thus reducing the leakage power. Among the compared devices, our proposed cell demonstrates the second-best leakage power. It exhibits 1.650x/1.658x/1.431x smaller leakage power compared to 6T/D10T/LP10T. The variation in leakage power with different temperatures is demonstrated in Fig. 5.4.

5.1.5 PROBABILITY OF BITLINE CHARGING

The bitlines of static random-access memory are capacitive in nature. They frequently need to be charged/ discharged depending on the operation performed. Due to their high capacitance, a significant portion of total power consumed per operation is used up for charging of bitlines. Hence, low BL charging probability quantifies lower power consumption for BL charging. For this computation, the

probability of read and write operation is assumed to be 50% each [11]. The chances of holding logic '0' are 60% while that of logic '1' are 40% [4]. A differential structure is used by 6T and D10T for both read and write operations. The likelihood of bitline charging for each for both is calculated to be 80%. LP10T employs a pseudo-differential write operation and single bitline for read operation where bitline charging probability is 65%. Both read and write operations are performed on one BL in ST9T & proposed design, which reduces the chances of BL charging per operation to 40%. Hence employment of a single BL reduces the likelihood of BL charging per event by half in contrast to differential bitlines for both read and write, while the same is reduces by 38.46% when compared differential writing and

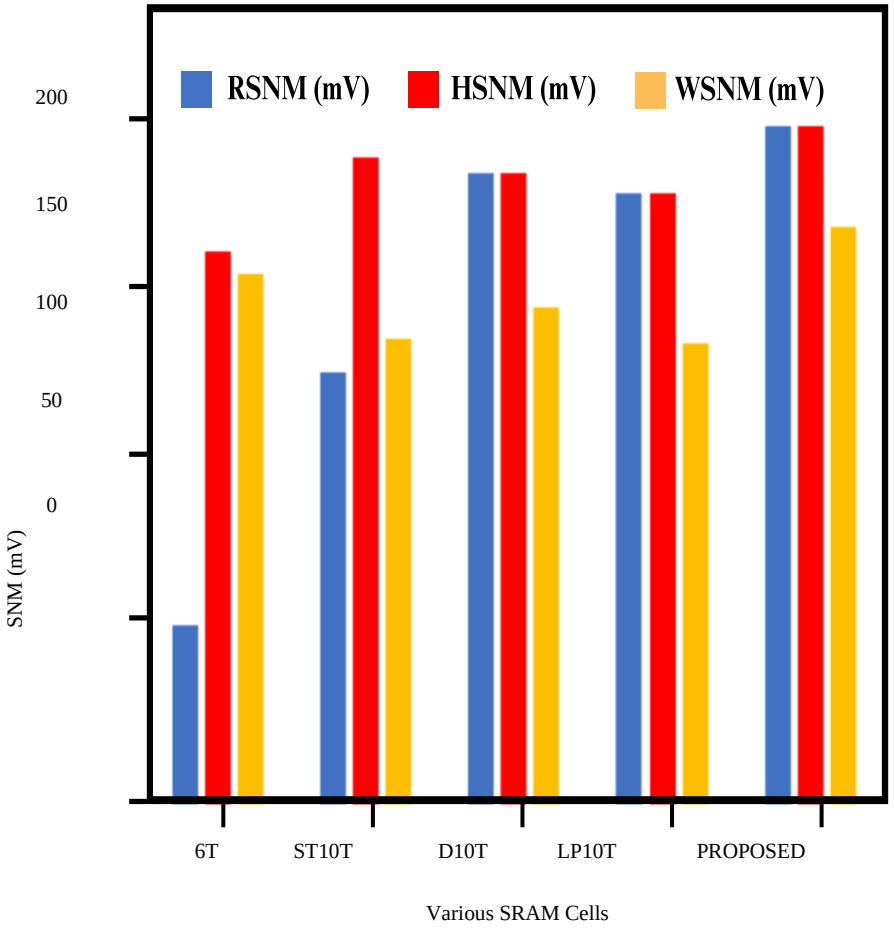


Fig 5.5 Comparison of HSNM/ RSNM/ WSNM of Various SRAM Cell

single ended reading. A graphical representation of bitline charging probabilities is presented in Fig. 5.6.

5.1.6 SPEED

The analysis of read and write delays is necessary for the quantization of the SRAM cell's operating speed. The determination of read delay differs between single ended and differential SRAM cells. When applied to differential cells, it indicates the amount of time needed after the start of the read cycle to generate a 50-mV voltage difference between two bitlines. Conversely, in single ended design, it refers to the span of time that elapses before the bitline transition to halfway from its onset precharged state. In comparative study, 6T and D10T designs showcase lower read delay in contrast to peers due to their fully differential configuration. Three serially linked transistors in the read current flow, however, prompts the single ended ST9T to have the highest read delay. On the flip side, with two transistors connected serially in the read current flow, LP10T and the proposed device both demonstrate a lower read delay than ST9T. With regard to the read operation, the proposed cell exhibits a 3.17x/3.07x/1.08x slower performance to 6T/D10T/LP10T cells respectively.

Write delay refers to the time elapsed after the initiation of the write cycle, for the storage node to reach 90% (10%) of V_{DD} during write '1'('0') respectively. The superior write speed of LP10T can be credited to the presence of differential writing (in proxy) and write assist technique. While 6T and D10T leverage their fully differential configuration,

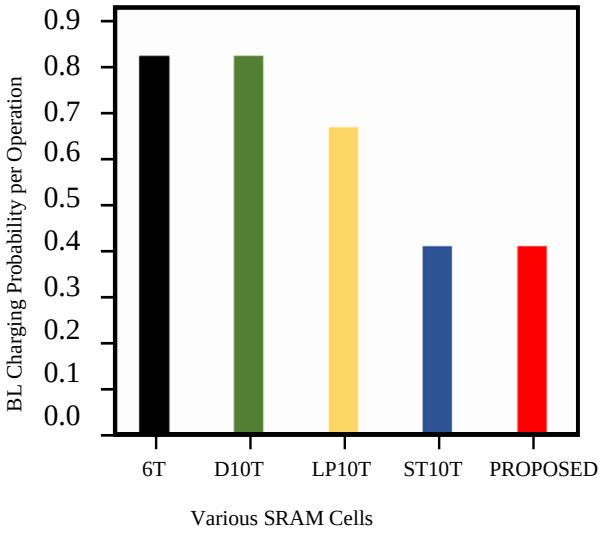


Fig 5.6 BL Charging probability per operation of SRAM cells

both ST9T and this work utilise a power gating write assist technique. ST9T has an extra advantage over the proposed device by regulating the trip voltage of the Schmitt trigger inverter through negative voltages. In juxtaposition with 6T/ D10T/ LP10T/ ST9T, the proposed cell performs 1.3x/ 1.29x/ 1.14x/1.01x slower. A graphical contrast of these delays is displayed in Fig. 5.7.

TABLE 5.1 COMPARITIVE ANALYSIS OF VARIOUS SRAM CELLS WITH PROPOSED 10T

Parameters	SRAM Cell				
	6T	***D10T***	***LP10T***	***ST9T***	***PROPOSED***
No. of Transistors	6	10	10	9	10
Read/Write operation	D^1/D	D/D	S^2/D	S/S	S/S
Read Disturb Problem	Yes	No	No	Yes	No
HSNM (V)	0.137	0.156	0.151	0.160	**0.168**
WSNM (V)	0.190	0.201	0.213	0.209	**0.218**
RSNM (V)	0.044	0.156	0.151	0.107	**0.168**
Leakage Current (nA)	11.13	11.16	9.662	6.06	6.25
Leakage Power (nW)	5.5691	5.581	4.831	3.03	3.375
Write Delay (ns)	0.964	0.981	0.646	1.25	1.27
Read Delay (ns)	0.487	0.503	1.428	1.783	1.546

5.1.7 EVALUATION OF PROPOSED 11T

The presented SRAM cell design is assessed on various design metrics, in contrast to the recently proposed OS9T, DIFF10T, NM10T and conventional 6T SRAM cells respectively. For an unbiased evaluation presenting fair results, all the devices under the purview of this paper have been implemented using 90nm CMOS technology at a supply voltage of 0.5V.

Static Noise margins are utilised to comment of stability, which are calculated through butterfly curve analysis. Leakage power is evaluated in the standby mode of the SRAM cell, while read and write delays are assessed to comment on speed of the SRAM cells.

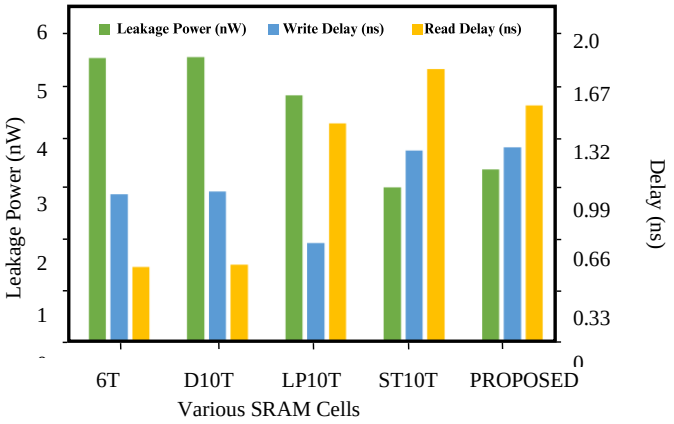


Fig 5.7 Comparison of Leakage Power, Read Delay and Write Delay of SRAM Cells at 27ºC

i. **HOLD STABILITY:** Hold static noise margin (HSNM) is a metric used to evaluate magnitude of noise (in V) that the SRAM cell can tolerate in hold state without corrupting the retained data. The side length of minimum out of the maximum sized squares formed in either lobe of the butterfly curve in hold mode is defined HSNM [17]. The magnitude of HSNM indicates the strength of the latch core. The proposed cell offers highest HSNM among its peers showing 27.2%/ 9.375%/ 15.89%/ 12.17% increase than 6T/ OS9T/ NM10T/ DIFF10T cells respectively. This high HSNM is manifested via a strong core circuit comprising a transistor infused standard inverter and a ST inverter. A comprehensive visual presentation of HSNM comparison of juxtaposed cells is demonstrated in Fig.5.8(a).

ii. **READ STABILITY:** The capacity of SRAM cell to execute read operation without tampering the withheld data in the presence of noise quantified via Read static noise margin (RSNM). The least of the largest square accommodated in either lobe of the read butterfly curve is utilised for calculation of RSNM. As the read path for 6T and OS9T passes through their data storage nodes, it makes both of the devices susceptible to read disturbances. However, the Schmitt trigger inverter of OS9T yields better RSNM. A RSNM as large as HSNM is exhibited in NM10T. The design at first glance might seem prone to read disturbance but is not in practice owing to a read path separated from the storage nodes. Notably, both DIFF10T and the presented device utilise a read buffer circuitry which shield the primary storage nodes from any transient voltage changes during the read cycle, thereby making them immune to read disturbance depicted in Fig 5.8(b). The put-forward device offers the highest RSNM with an enhancement of 297.72%/ 63.55%/ 15.89%/ 25% in contrast to 6T/ OS9T/NM10T/DIFF10T cells respectively.

iii. **WRITABILITY:** Writability is ascertained by determining the write static noise margin (WSNM). It signifies the SRAM cell's capability to perform write operation successfully in the presence of noise. Evidently, in Fig. 5.8(c). the low WSNM in DIFF10T and 6T circuits can be attributed to non-existence of any write assist scheme. A pseudo-differential writing mechanism visible in NM10T along with a ST inverter core is responsible for its increased WSNM. Furthermore, the power

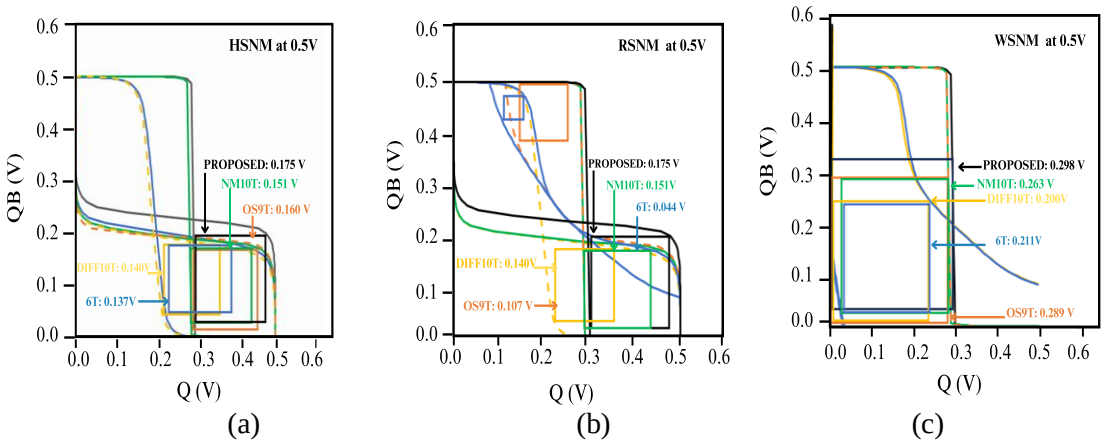


Fig 5.8 Butterfly Curves (a) HSNM, (b) RSNM, (c) WSNM

gating technique utilized in OS9T helps the structure bear an enhanced writability. The proposed device outperforms the peers by displaying greatest WSNM owing to feedback-cutting mechanism employed which totally nullifies the effect of resistance displayed by the stored logic towards the incoming logic. In contrast to 6T/OS9T/NM10T/DIFF10T the cell offers 41% / 3.14%/13.30% /49% increased WSNM. A graphical comparison of SNMs in shown in Fig. 5.10

iv. **LEAKAGE POWER:** During the lifecycle of a SRAM cell, a significant duration is elapsed in the hold sate. Hence the aim for energy efficient devices creates a natural call for minimizing leakage or standby power. This paper calculates leakage power by quoting the average power of the entire hold operation which takes into account the effect of transition of control signals as well. Owing to their dual ended structures, the 6T and DIFF10T show highest leakage power among the peers, as by design, they lack any leakage control devices. Among them, DIFF10T suffers most leakage power due to an additional read circuitry. On the flip side, the leakage power calculation for NM10T is a step lower, manifested by a single ended design and a ST core which increases the effective threshold voltage. Furthermore, the presence of stacking effect via a tristate and ST inverter core adds on to a lower leakage for OS9T. Variation in leakage power with various temperatures is showcased in Fig.5.9. The proposed devise surpasses all the juxtaposed designs by a strong margin showing 3.5x/ 3.45x / 2.62x/ 3.17x reduction in leakage power in contrast to DIFF10T/ 6T/OS9T/NM10T cells respectively.

v. **PROBABILITY OF BITLINE CHARGING**

During the course of different operations in the life cycle of a SRAM, the bitlines hold different operation specific logics. Being capacitive in nature, BL needs a frequent charge / discharge. A countable corpus of the average power comes from the said operation of high

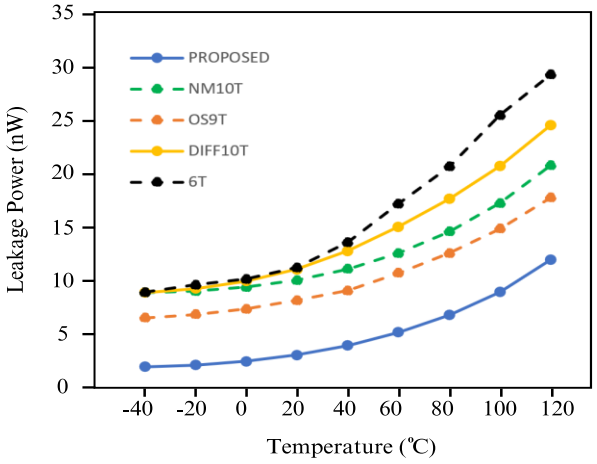


Fig 5.9 Variation of Leakage Power
with Temperature of SRAM Cells

capacitance BLs. With an assumption that the likelihood of read and write cycles are equal and the cell retains logic '0' 60% of the time, other 40% is for logic'1' [4], this analysis of bitline charging is carried forward. Due to a fully differential structure, the likelihood of BL charging/discharging in 6T and DIFF10T is 80%. While sone sided structure, reduces this value to half as presented in Fig. 8

vi. **SPEED**

To comment on the operating speed of a SRAM cell, read and write delays are analysed. By definition, read delay is the time elapsed for precharged bitline to discharge to V_{DD}-50mV ($V_{DD}/2$) for dual ended (single ended) structures. Due to slower sensing, the single ended cells offer higher read delays. Hence 6T and DIFF10T offer read delays towards the lower side. OS9T shows a greater read delay due to serially linked transistors in its read current flow. Conversely NM10T and the proposed device offer comparable read delays. The proposed cell demonstrates 3.18x / 0.93 x / 1.007x/ 2.90x the read delay compared to 6T/ OS9T/NM10T/DIFF10T cells respectively.

TABLE 5.2 COMPARITIVE ANALYSIS OF VARIOUS SRAM CELLS WITH PROPOSED 11T

Parameters	**SRAM Cell**				
	6T	***OS9T***	***NM10T***	***DIFF10T***	***PROPOSED***
No. of Transistors	6	9	10	10	11
Read/Write operation	D^1/D	S^2/S	S/S	D/D	S/S
Read Disturb.	Yes	Yes	No	No	No
HSNM (V)	0.137	0.160	0.151	0.140	**0.175**
WSNM (V)	0.211	0.289	0.2613	0.200	**0.298**
RSNM (V)	0.044	0.107	0.151	0.140	**0.175**
Leakage Current (nA)	5.575	4.227	5.115	5.78	**1.612**
Leakage Power (nW)	11.15	8.455	10.23	11.56	**3.224**
Write Delay (ns)	0.476	1.043	0.732	0.492	1.024
Read Delay (ns)	0.512	1.743	1.621	0.563	1.633

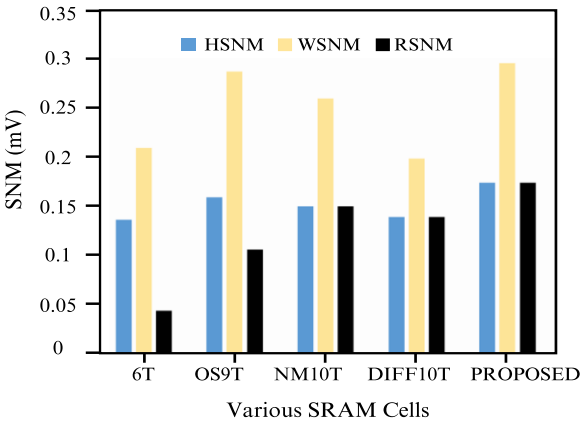


Fig 5.10 Static Noise Margins of Various SRAM Cells

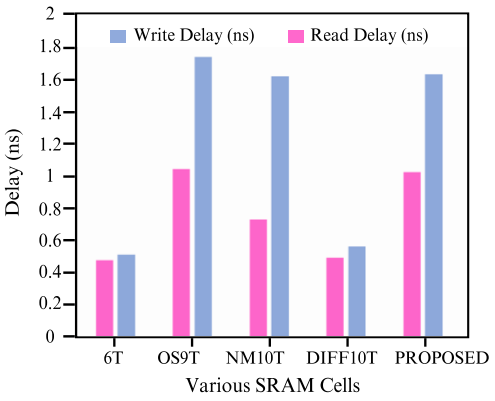


Fig 5.11 Read and Write delays of various SRAM

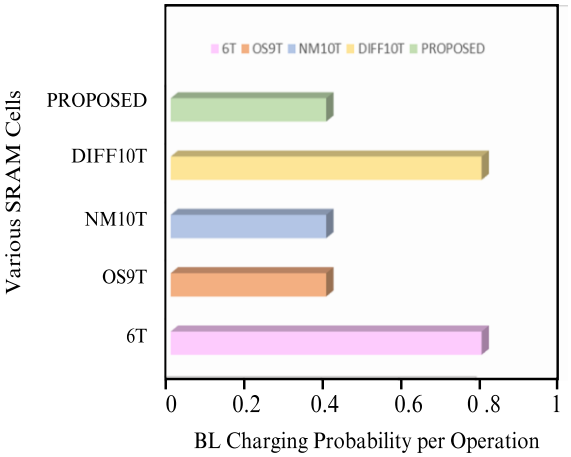


Fig 5.12 Bitline Charging probabilities of various SRAM Cells

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

This thesis introduces two novel SRAM designs. Firstly, a single-ended 10T SRAM designed for operation in the near-threshold region. Simulation results conducted in 90-nm CMOS technology at 0.5V demonstrate significant improvements in contrast to the conventional 6T SRAM. In particular, the suggested cell uses a tri-state inverter-based latch core and a read path that is isolated from the data storage nodes to improve HSNM/RSNM by 22.62%/281.81%. Furthermore, WSNM is increased by 12.84% through the implementation of a power gating scheme, which effectively cuts off V_{DD}/GND rails during write '0'/ '1' operations respectively. Notably, the adoption of a single bitline structure, along with transistor stacking and operation specific grounding of the read circuitry, contributes to a reduction in leakage power. The leakage power of the proposed cell is 1.65x lower than that of the 6T SRAM.

Additionally, one-sided 11T SRAM for near-threshold voltage regime. Simulation results conducted in 90-nm CMOS technology at 0.5V displays significant improvements in contrast to the conventional 6T SRAM. In particular, the proposed cell uses a Schmitt trigger inverter-based latch core and a read path decoupled from storage nodes to improve HSNM/RSNM by 27.2%/297.72%. Furthermore, WSNM is increased by 41% through the implementation of a feedback-cutting scheme, which effectively disrupts the internal feedback during write operation. The adoption of an ended configuration, along with transistor stacking and operation specific grounding of the read circuitry, contributes to a reduction in leakage power. The leakage power of the presented cell is 3.45x lower than 6T SRAM.

With the varied applications of memory cells, the study can further be incorporating dynamic stability analysis for the proposed cells. Due to large number of transistors, the cells suffer slow read/ write speeds. Novel design practices to improve on the speed of the cell can also be an area for expansion.

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