DESIGN, ANALYSIS, AND MODELING OF FERROELECTRIC FIELD EFFECT TRANSISTOR

Thesis submitted for the award of the degree

of

DOCTOR OF PHILOSOPHY

by

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Certificate

This is to certify that the thesis entitled **"Design, Analysis, and Modeling of Ferroelectric Field Effect Transistor"** being submitted by **Ms. Snehlata Yadav (2K19/PHDEC/03)** for the award of the degree of **Doctor of Philosophy** in the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, is the record of student's own work carried out by her under our supervision. The contents of this research work have not been submitted in part or fully to any other institute or university for the award of any degree.

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Snehlata Yadav

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ϕ	Electrostatic channel potential of the device
N_D	Doping concentration in channel region
ε_{si}	Silicon permittivity
ε_{IL}	Insulator/oxide permittivity
q	Electronic charge
V	Electron quasi-fermi potential
ϕ_{SP}	Surface Potential. In simplest terms, it is the difference between the voltage at the surface of the MOSFET capacitor.
ϕ_{CP}	Center Potential
ϕ_M	Work function of metal
ϕ_{si}	Work function of semiconductor
χ	Electron affinity
E_g	Energy band gap
N_D^+	Doping concentration in Source/drain regions
t_{CH}	Thickness of the channel layer
t_{FE}	Thickness of the ferroelectric layer
t_{IL}	Thickness of the insulator layer
Q_{TOT}	Total charge density over the entire channel(per unit gate area)
V_{FE}	Drop across ferroelectric layer
V_{IL}	Drop across insulator layer
V_{FB}	Flat band voltage which results due to the difference in the work function of the metal and semiconductors
V_{th}	Threshold voltage

Q_{MOB}	Mobile charge density over the entire channel
V_T	Thermal Voltage
I_D	Drain current
V_{GS}	Gate to source voltage
k	Boltzmann constant
T	Temperature
T_c	Curie temperature
C_{TOT}	Total gate capacitance
C_{IL}	Capacitance across insulator layer
C_S	Semiconductor capacitance
C_{FE}	Ferroelectric capacitance
C_G	Gate stack capacitance
Q	Surface charge
α, β, γ	The Landau-coefficients that depends on the ferroelectric material properties typical of HZO
g_m	Transconductance
V_{EA}	Early Voltage
A_V	Intrinsic Gain
W/L	Width to length ratio of the transistor
μ	Mobility of the charge carrier
U	Ferroelectric's free energy density
E	External applied electric field
P	Polarization

List of Abbreviations

ALD	Atomic Layer Deposition
APTES	(3-Aminopropyl)triethoxysilane
CLM	Channel Length Modulation
CMD	Carrier Mobility Degradation
CMOS	Complementary Metal Oxide Semiconductor
CNFET	Carbon Nanotube Field Effect transistor
CVT	Concentration, Voltage, and Temperature
DG	Double Gate
DGFET	Double Gate Field Effect transistor
DGFJL	Double Gate Ferroelectric Junctionless
DGNCFET	Double Gate Negative Capacitance Field Effect Transistor
DIBL	Drain Induced Barrier Lowering
DNA	Deoxyribonucleic Acid
FE	Ferroelectric
GAA	Gate-All-Around
GFP	Gain Frequency Product
GTFP	Gain Transconductance Frequency Product
HCI	Hot Carrier Injection
HZO	Hafnium Zirconium Oxide
IC	Integrated Circuits
IMOS	Impact Ionization MOS
JAM	Junctionless Accumulation Mode
JAMFET	Junctionless Accumulation Mode Field Effect Transistor

JLGAA	Junctionless Gate-All-Around
JLNW	Junctionless Nanowire
JLT	Junctionless Transistor
LK	Landau Khalatnikov
MFIS	Metal Ferroelectric Insulator Semiconductor
MFMIS	Metal Ferroelectric Metal Insulator Semiconductor
MFS	Metal Ferroelectric Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MTPG	Maximum Transducer Power Gain
NCFET	Negative Capacitance Field Effect Transistor
NCTFET	Negative Capacitance Tunnel Field Effect Transistor
PVD	Physical Vapour Deposition
PZT	Lead Zirconate Titanate
RCA	Radio Corporation of America
RF	Radio frequency
RTA	Rapid Thermal Annealing
SBT	Strontium Bismuth Tantalite
SCE	Short Channel Effects
SRAM	Static Random Access Memory
SRH	Shockley-Read-Hall
SS	Subthreshold Swing
TAT	Trap Assisted Tunneling
TGF	Transconductance Generation Factor
TFET	Tunnel Field Effect Transistor
TFP	Transconductance Frequency product

UPG	Unilateral Power Gain
UTB	Ultra thin body
VLSI	Very Large Scale Integration

Chapter 1

Introduction

1.1 Evolution of MOSFET

The mid-20th century marked the beginning of the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) era. The invention of the MOS (Metal-Oxide-Semiconductor) capacitor laid the groundwork for the MOSFET. Lilienfeld, a physicist, patented the concept of a field-effect transistor-like device based on a thin layer of semiconductor material in the 1920s [1]. Lilienfeld's work, however, remained purely theoretical. In the late 1950s, researchers began investigating the electrical properties of MOS capacitors [2]. M. Atalla and D. Kahng, physicists at Bell Laboratory, made substantial contributions to the invention of the MOSFET in 1959 [3]. They established the viability of fabricating a functional MOS capacitor by depositing a thin silicon dioxide (SiO_2) layer on a silicon substrate and using metal connections. They also observed current flow control across the oxide layer by applying a voltage to the metal gate. Later in 1963, Chih-Tang Sah and Frank Wanlass at Fairchild Semiconductor introduced the planar MOSFET [4]. The planar MOSFET used a more feasible structure, including a metal gate, a thin oxide layer, and a p-n junction beneath the channel region. This design enabled better device characteristics such as lower power consumption and faster switching speed. Throughout the 1960s and 1970s, researchers and engineers achieved substantial advances in MOSFET technology. During this time, notable advances included the advent of complementary MOS (CMOS) logic, which used both n-channel and p-channel MOSFETs for improved power efficiency and noise immunity [5]. Furthermore, scaling down MOSFETs, resulting in reduced transistor size and higher integration density, became a major focus.

1.2 MOSFET Scaling and Challenges

MOSFET scaling is the ongoing miniaturization of MOSFETs in order to improve their performance and density on integrated circuits. In 1965, Gordon Moore, co-founder of Intel, projected that the number of transistors on a semiconductor chip would double every two years, known as Moore's Law [6]. This doubling of transistor count has been made feasible by MOSFET scaling, which allows for smaller transistor sizes and the incorporation of a higher number of transistors on a chip as shown in Fig. 1.1 [7]. Moore's Law has been a guiding principle in the semiconductor industry for several decades, precisely describing the pattern of rising transistor density and performance. The fundamental reason for scaling MOSFETs is to minimize their size, which has various advantages, including increased performance, higher density, cost reduction, and low power consumption. However, as MOSFETs are scaled down to smaller dimensions, many significant challenges arise. Some of the significant challenges [8] are explained in following subsections.

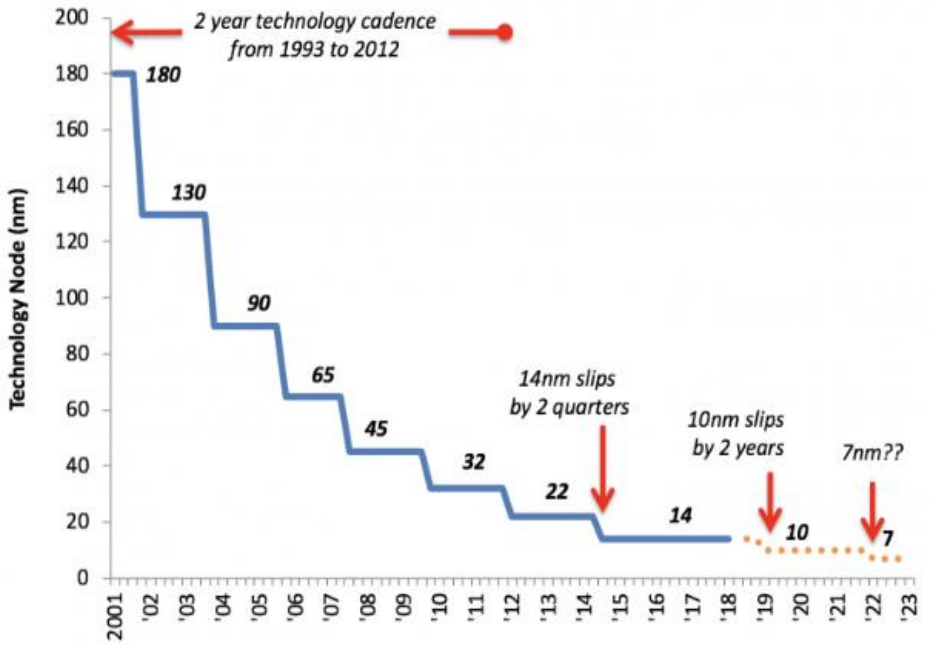


Fig. 1.1 Scaling Trend of MOSFET [7]

1.2.1 Short-channel effects: Short channel effects (SCEs) occur in MOSFETs when the channel length becomes comparable to the carrier mean free path or depletion zone width. As the channel length in modern integrated circuits reduces, these effects become more substantial, posing issues in transistor performance and device scalability. As channel lengths shorten, short-channel effects such as drain-induced barrier lowering (DIBL), hot carrier effects, mobility reduction, and increased leakage current become more evident [9]. The DIBL effect causes electrostatic coupling between the source and drain, rendering the gate inefficient as shown in Fig. 1.2 [10]. The power dissipation is increased by the leakage current. Hot carrier effects (as shown in Fig. 1.3) substantially degrade MOSFET performance and cause the device to behave differently than long-channel devices [11].

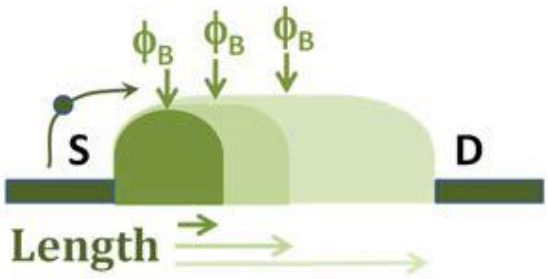


Fig. 1.2 Drain Induced Barrier Lowering (DIBL) [10]

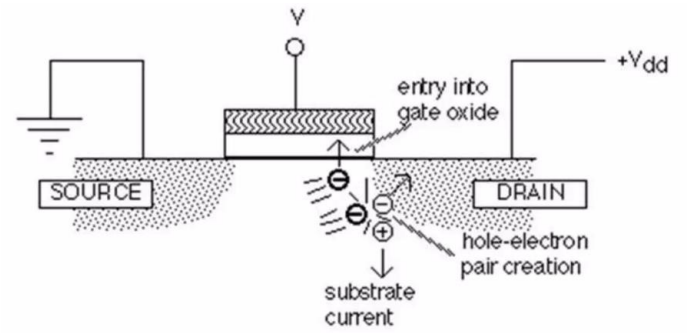


Fig. 1.3 Hot Carrier Effects [11]

1.2.2 Variability: Scaling introduces variances in transistor properties due to manufacturing processes and statistical variations. Quantum mechanical effects become more pronounced, adding to variability. Variations occur due to factors such as the number of carriers in the channel, carrier tunneling, and scattering phenomena [12]. These variances can have a negative impact on device performance and yield, making it difficult to ensure consistent and dependable operation over a large number of transistors.

1.2.3 Gate oxide thickness: As gate lengths are reduced, the thickness of the gate oxide layer must be reduced as well. However, decreasing the oxide thickness increases gate leakage currents, which can impact the power consumption and reliability of the device [13]. The thinner gate oxide raises concerns about reliability issues like hot carrier injection (HCI) and oxide breakdown. High-energy carriers affect the gate oxide, causing deterioration and potential failure.

1.2.4 Heat dissipation: As transistor density increases, so does power density, resulting in increased heat generation. As devices shrink, there is not as much space for heat to dissipate. Due to the smaller physical dimensions, thermal paths, such as the distance between the transistor and the heat sink, and the availability of metal layers for efficient heat conduction, are limited. This constraint makes it more difficult to manage heat dissipation, which might have an impact on device durability and performance [14].

It's crucial to remember that, despite the fact that Moore's Law has been valid for many years, maintaining traditional MOSFET scaling over certain logical and technical limits is becoming more difficult. To continue expanding semiconductor technology and sustaining the spirit of Moore's Law, the industry is investigating alternate transistor topologies, novel materials, and innovative manufacturing procedures.

1.3 Device Architectures to Overcome Scaling Challenges

In order to tackle the numerous challenges associated with miniaturization, including issues like short channel effects, complex fabrication requirements, and a notable rise in static power dissipation, researchers have proposed and extensively investigated several device technologies. These device technologies help in improving the gate control over the channel which results in lower leakage current, improved analog performance, and low power dissipation. Here, we outline some of the device technological advancements that aim to overcome the scaling challenges.

1.3.1 Multigate MOSFETs

Multigate transistors, commonly known as multi-gate FETs, are a type of transistor architecture in which the channel current is controlled by numerous gates. When compared to standard planar MOSFETs, they provide better electrostatic control, lower leakage current, and higher performance [15]. The following are the most prevalent types of multigate transistors:

1.3.1.1 Double Gate MOSFET

A Double Gate MOSFET (DG MOSFET) is a transistor with two gates rather than one. It is also referred to as a dual-gate or twin-gate MOSFET.

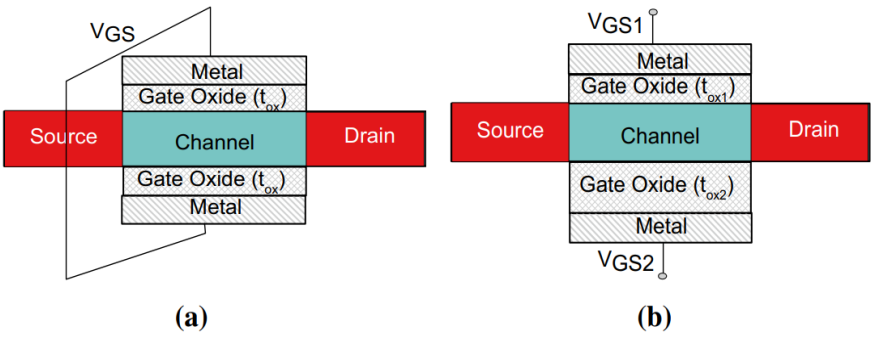


Fig. 1.4 Structure of Double Gate MOSFET (a) Symmetric and (b) Asymmetric [17]

The twin gate configuration allows for greater control over the flow of current through the transistor. A DG MOSFET has two gate electrodes, one on each side of the channel region. When the transistor is turned on, current flows across the channel. The gates are isolated from the channel by a thin insulating layer termed gate oxide [16]. DG MOSFET can be configured in two ways: Asymmetric DG MOSFET and Symmetric DG MOSFET as shown in Fig. 1.4 [17]. The front and back gates in Asymmetric DG are biased independently and also the thicknesses of oxide layers are distinct. In Symmetric DG, both oxide layers have the same thickness, and the two gates are connected by a common bias. The double gate configuration has various advantages over standard MOSFETs, including better control over the channel region, lower leakage current, higher drive current, better scalability, and improved analog performance [18].

1.3.1.2 FinFET

A FinFET (Fin Field-Effect Transistor) is a transistor structure that has grown in prominence in semiconductor technology. As feature sizes fall, it is intended to overcome the limitations of classic planar MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors). The channel in a FinFET is constructed as a thin, vertical fin that protrudes from the silicon substrate

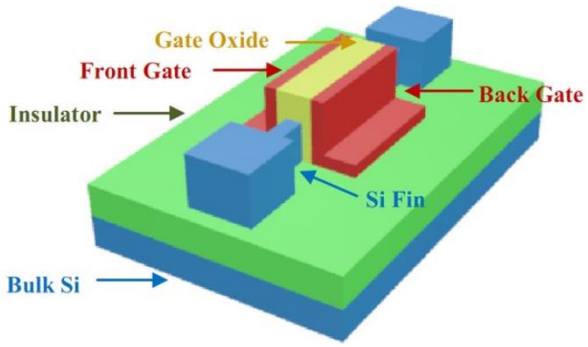


Fig. 1.5 Schematic 3D view of FinFET [19]

and is enclosed by two or more gate electrodes as shown in Fig. 1.5 [19]. The fin serves as the conducting channel, while the gates regulate the passage of current through it. The verticality of the channel is an essential feature of FinFET, which helps decrease short-channel effects and increases control over the transistor's behavior [20]. FinFET offers several advantages over planar MOSFET such as improved scalability reducing performance degradation and enabling continued transistor scaling, lower leakage current, and compatibility with existing fabrication processes, making it easier to adopt in semiconductor manufacturing [21].

1.3.2 Junctionless Transistor

All the MOSFETs have a p-n junction, having depletion layers that allow or block the current according to the voltage applied to the gate. Junctionless transistor (JLT) has no p-n junction as compared to the inversion mode device. The idea of the JLT has been reported by Colinge et.al in 2010 [22]. The challenging part of these inversion mode devices at nanoscale is the formation of ultra-sharp source/drain junctions due to which fabrication complexity increases and it requires precise control of doping and thermal conditions to form heterogeneous doping, like p-n junctions [23], [24]. The formation of source/drain junctions not only elevates the fabrication problem but also, consequently violates the electrical characteristics of the device. JLT presents an

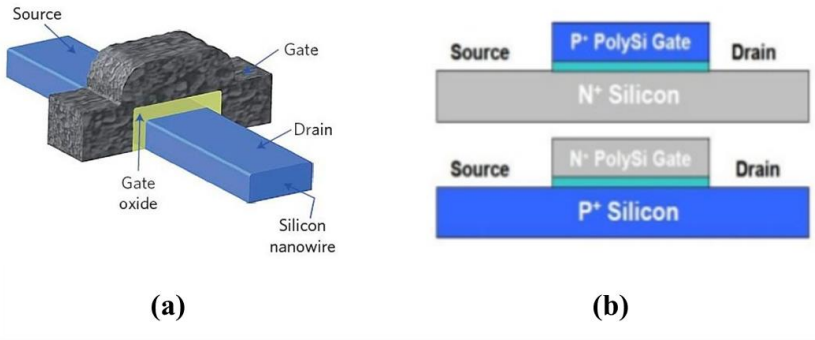


Fig. 1.6 Junctionless Transistor (a) 3-D view (b) 2-D cross sectional view [25]

optimal resolution for addressing the challenge of achieving the extremely sharp formation of the source/drain junction. The basic structure of the JLT is shown in Fig. 1.6 which has a uniform and homogeneous doping throughout the source-channel-drain (N+ -N+ -N+) region [25]. JLT is basically a fully depleted device and the gate metal work function should be high as compared to conventional transistors. Due to the full depletion of charge carriers, it provides better subthreshold characteristics. It also has better SCE immunity as compared to conventional MOSFETs. The JLT, being free from abrupt changes in doping, holds great promise as a potential solution to address the challenges associated with costly annealing techniques and thermal budget constraints. Additionally, its fabrication is straightforward, and it offers opportunities for enhancing the electrical properties of the device [26]. There are some disadvantages of JLT such as low ON current and low transconductance, which have been improved by another alternative structure of junctionless structure known as Junctionless Accumulation Mode (JAM) structure.

1.3.3 Junctionless Accumulation Mode FET

JLT has a number of advantages which have been discussed in our previous section but it has some disadvantages as well. The major disadvantages of the JLT are low drain current and low transconductance due to Carrier Mobility Degradation (CMD). The

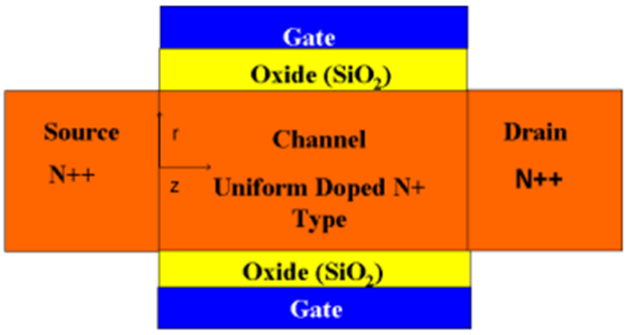


Fig. 1.7 Schematic structure of Junctionless Accumulation Mode FET [28]

CMD occurs due to high channel doping concentration. The limitations of JLT can be addressed with the alternate structure known as Junctionless Accumulation Mode (JAM) transistor [27]. It is a homogeneously doped structure with N+-N-N+/N++-N+-N++ homo-junctions where the concentration in the channel region is moderately low in comparison to the source/drain region as shown in Fig. 1.7 [28]. In JAM FET, where the channel region has lower doping, the flow of current is not constrained primarily to the central region of the silicon channel. This results in a variation in current from the center towards the surface. Additionally, in the case of higher doping levels, a higher value of gate metal work function is needed to completely deplete the channel for its transition into the off state [29]. Moreover, the JAM FET employs a lower channel doping, forming a homogeneous N+-N-N+/N++-N+-N++ junction, which facilitates a volume accumulation effect. JAM structure can also overcome the problem of CMD.

1.3.4 Steep Subthreshold Slope Devices

Steep subthreshold devices, also known as steep slope transistors, are electronic devices that allow for efficient operation at very low power supply voltages. They have sparked considerable interest in recent years because of their prospective uses in low-power integrated circuits and energy-efficient devices. Conventional devices feature significant leakage currents and decreased performance in subthreshold operation, where the transistor operates below its threshold voltage, rendering them inefficient for low-power applications. Steep subthreshold devices seek to overcome these constraints by achieving a steeper subthreshold slope. The subthreshold slope measures how well a transistor switches between on and off states at low voltages. The subthreshold slope in conventional transistors is restricted by thermal energy and the Boltzmann distribution of carriers. Steep subthreshold devices have the potential to significantly reduce power consumption in a variety of applications, including low-power

electronics, Internet of Things (IoT) devices, wearable electronics, and energy-efficient computer systems. They can improve battery life, minimize energy consumption, and facilitate the adoption of energy-autonomous devices by running efficiently at low power supply voltages. Researchers have investigated and developed some of the steep subthreshold slope devices. A few of them are explained below:

1.3.4.1 Tunnel FET (TFET)

A Tunnel Field-Effect Transistor (TFET) uses quantum mechanical

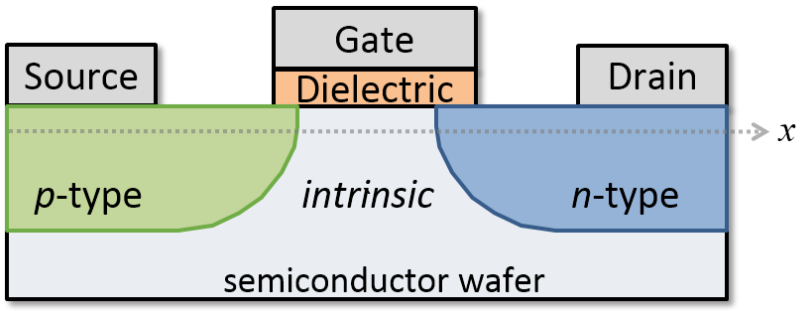


Fig. 1.8 Basic structure of Tunnel FET [30]

tunneling rather than typical thermionic emission to operate. TFETs are intended to alleviate the shortcomings of traditional MOSFETs, particularly with respect to power consumption and subthreshold slope. The channel region of a TFET is separated from the source and drain regions by a thin barrier known as the tunneling junction. Tunneling junctions are often made of high bandgap materials, such as strongly doped p-n junctions or heterojunctions as shown in Fig. 1.8 [30]. Due to the presence of a thin barrier, carriers (electrons or holes) can tunnel through the tunneling junction when a voltage is applied across the source and drain terminals [31]. This allows the TFET to toggle between on and off states. The main advantage of TFETs is their capacity to create a steep subthreshold slope.

TFETs can reach subthreshold slopes that are lower than this thermal limit, generally in the 10-100 mV/decade range or even below [32]. This enables transistor operation at lower power supply voltages to be more efficient. However, TFETs suffer limitations as well. The achievement of high on-state currents or drive currents is a considerable challenge, as quantum tunneling often results in lower current levels [33].

1.3.4.2 Impact Ionization MOS (IMOS)

IMOS is proposed as a method of switching from off to on by modulating the avalanche breakdown voltage of a gated structure [34]. Fig. 1.9 shows the basic structure of n-channel IMOS. A p-n junction diode is utilized in this type of transistor with voltages greater than the breakdown voltage [35]. The delay of an IMOS is proportional to the logarithm of the required gain, making it incredibly fast. This device can therefore achieve subthreshold swing values that are substantially lower than the (kT/q) ln10 limit of a normal MOSFET [36]. The fundamental issue with impact

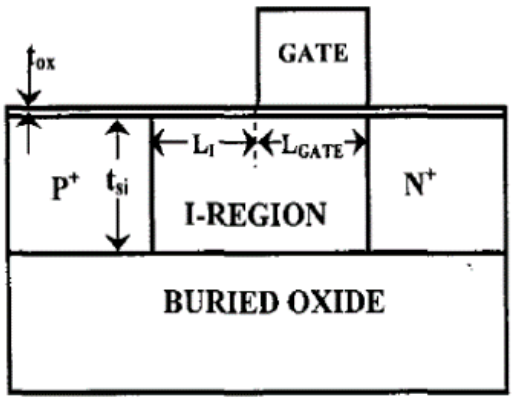


Fig. 1.9 Basic structure of an N-channel IMOS [35]

ionization MOSFETs is their long-term reliability. The existence of heated carriers in large densities is required for an avalanche breakdown, which affects reliability [37].

1.3.4.3 Ferroelectric based Negative Capacitance FET

The Negative Capacitance Field-Effect Transistor (NCFET) is a particular type of field-effect transistor that uses the unique features of ferroelectric materials to produce a negative capacitance effect [38]. The NCFET concept originated as a possible solution to the power dissipation issues that traditional transistors confront. The schematic structure of a ferroelectric negative capacitance FET is shown in Fig. 1.10. The basic idea behind

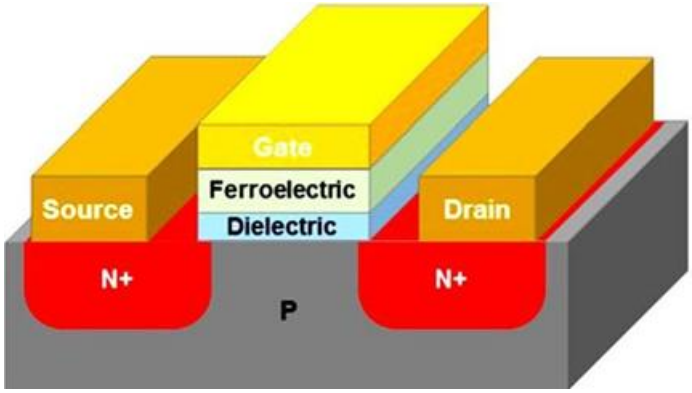


Fig. 1.10 Schematic structure of a Ferroelectric Negative Capacitance FET [39]

NCFET is that by using a ferroelectric material as the gate dielectric, the effective capacitance of the transistor can be decreased below the physical capacitance. This negative capacitance effect occurs due to the intrinsic characteristics of the ferroelectric material, where the polarization response opposes the external electric field. When a positive voltage is provided to the gate of an NCFET, the ferroelectric material undergoes polarisation reversal, resulting in an internal negative voltage. This negative voltage effectively magnifies the voltage across the transistor, causing the charge density in the channel region to shift more dramatically. As a result, the NCFET has a subthreshold slope of less than 60 mV/decade, surpassing the

limit of typical MOSFET (about 60 mV/decade) [40]. NCFETs can function at lower supply voltages while preserving the needed functionality by amplifying the voltage shift at the gate. This offers the possibility of reduced power consumption in integrated circuits and potential energy savings.

1.4 Motivation

The electronics industry has been driven to develop more features while also offering dense and quick integration over the past five decades as a result of CMOS technology scaling. The pursuit of enhanced performance and integration has been the driving force behind the scaling trends observed across various systems. As a result, present-day transistors exhibit speeds that are 20 times faster than their counterparts from half a century ago while occupying less than 1% of the space. However, these advancements have come at the cost of increased power consumption and power density, as highlighted in reference [14]. Furthermore, numerous parameters in VLSI design, such as supply voltage, gate dielectric constant, and leakage current, have undergone extensive customization to achieve the desired performance of integrated circuits (ICs). As per Moore's law, the reduction in oxide thickness and channel length poses a challenge to further scaling. To facilitate the dense integration of transistors, there is a need to linearly decrease the voltage supply and transistor size [41]. Dennard scaling laws state that reducing the size of a device lowers capacitance values and overall power usage. The limitation on the rate of increase in drain current with respect to the gate-source voltage to 60 mV/decade is attributed to the influence of Boltzmann statistics on the carriers in the source and drain regions of the MOSFET. As a result, this restriction prevents a further decrease in V_{DD} (supply voltage) and hinders the reduction of overall power consumption [42]. To cope up with these

challenges, various steeper subthreshold devices such as Tunnel FET, IMOS, and NCFET have been discussed in the previous section. However, the practical implementation of Tunnel FET and IMOS devices is constrained by a challenging fabrication procedure and poor reliability. Therefore, among these devices, NCFET has attracted the greatest interest due to its ability to achieve a steep subthreshold slope (SS) through a voltage amplification mechanism, all while maintaining a high drive current. Furthermore, NCFET offers additional advantages such as a high on-state current, minimal off-state current, and low power dissipation. Its straightforward construction, compatibility with existing fabrication processes, and exceptional performance characteristics, including a steep subthreshold swing (SS), a high on/off ratio, and adjustable hysteresis, further contribute to its appeal.

1.5 Thesis Outline

- **Chapter 1: Introduction**

  This chapter describes the evolution of MOSFET, the need for scaling the MOSFET, and various scaling challenges. Various device architectures have been explained to mitigate these challenges. This chapter also focuses on various steep subthreshold devices to overcome power challenge issues. Further, the main motivation behind this research work has been comprehended. Lastly, an overall organization of the thesis has been presented.

- **Chapter 2: Literature Review**

  This chapter includes a thorough description of ferroelectric material based Negative Capacitance (NC) FET. Various ferroelectric materials exhibiting a negative capacitance effect have been presented. Furthermore, this chapter covers a brief history of NCFET as well as the work done on this device so far. Lastly, the research gaps and objectives have been defined based on the provided literature review.

- **Chapter 3: Single Gate Junctionless Accumulation Mode Ferroelectric FET: Design & Analysis**

  This chapter involves the design and analysis of Single Gate Junctionless Accumulation Mode Ferroelectric FET. The main focus of this study is to combine the ferroelectric-induced NC effect with JAM architecture to get enhanced performance and fabrication feasibility. Methods used to model and simulate the device are discussed in detail. Many performance parameters such as DC, analog, and small signal parameters have been investigated to analyze the performance of the proposed device. The impact of temperature variation has also been studied on various parameters.

- **Chapter 4: Double Gate Junctionless Accumulation Mode Ferroelectric FET: Design, Analysis & Modeling**

  This chapter includes the development of a compact analytical model of the double gate junctionless accumulation mode ferroelectric FET. The analytical surface potential model and drain current model of the proposed structure have been developed by using Poisson's equation and Landau- Khalatnikov equation and Pao-Sah integral equation. Analytical results derived from the model in this way were validated with simulation results obtained using the ATLAS TCAD simulator, which shows good agreement. The impact of temperature variation has also been investigated through similar modeling on various parameters.

- **Chapter 5: Dual Gate Ferroelectric FET: Biosensor Design & Sensitivity Analysis**

  This chapter explores the biosensors application of the proposed dual gate ferroelectric structures. Label-free detection and ultra-sensitive detection of biomolecules are accomplished by integrating dielectric modulation and charge density concentration. The cavity is created inside the insulator layer as an immobilization site for the biomolecules to improve the drive current as well as sensitivity for biomolecule detection.

- **Chapter 6: Conclusion and Future Work**

  In this chapter, conclusions are drawn regarding NCFET potential in upcoming technology. The contributions of this work are described, along with suggestions for additional research based on this dissertation.

Chapter 2

Literature Review

2.1 Overview

In the preceding chapter, overview of various steep subthreshold devices which can handle the power challenge difficulties was presented. Among these devices, the NCFET has garnered the interest of researchers due to its ability to create a steep SS via a voltage amplification process. This chapter presents a literature review on several concepts of ferroelectric negative capacitance that was investigated and referenced during the research work. Several ferroelectric materials with negative capacitance effects have been reported. Furthermore, this chapter provides a brief history of NCFET as well as current research on this device. Finally, based on the provided literature review, the research gaps and objectives have been determined.

2.2 The Concept of Ferroelectric Negative Capacitance

2.2.1 Negative capacitance: Definition

The definition of capacitance (C) for a device is the rate at which the charge (Q) increases with respect to the voltage (V) ($C = dQ/dV$). In the case of a negative capacitor, the charge decreases as the voltage increases as shown in Fig. 2.1 (a). Capacitance can also be described in terms of the free energy (U). The energy landscape of a negative capacitor follows an inverted parabola as depicted in Fig. 2.1 (b) [43].

For a linear capacitor, the free energy density (U) can be expressed in terms of capacitance as $U=Q^2/2C$ or $C=(d^2U/dQ^2)^{-1}$. This capacitance and energy density relation also holds true for

a non-linear capacitor. To put it another way, the presence of a negative curvature zone in the energy landscape of an insulating material denotes the presence of a negative capacitance [44].

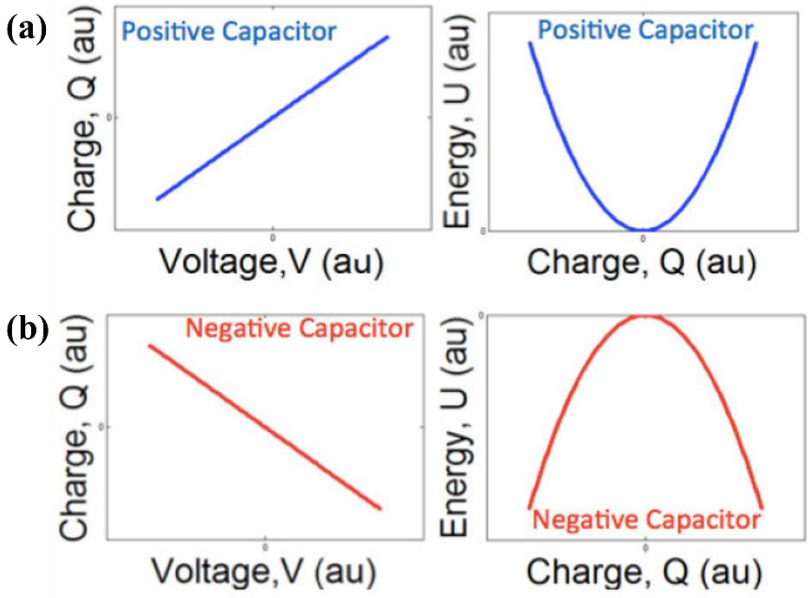


Fig. 2.1 Charge-voltage and energy landscapes of (a) Positive capacitor and (b) Negative capacitor [43]

2.2.2 Realization of Negative Capacitance through ferroelectric material

Figure 2.2 depicts the energy landscape of a ferroelectric material, displaying two degenerate energy minima [45]. This means that the ferroelectric material can have non-zero polarisation even when no electric field is provided. In general, the total charge density within a material can be stated as $Q = \varepsilon E + P$, where ε represents the ferroelectric's linear permittivity, E represents the external electric field, and P indicates polarization. Q is approximately equal to

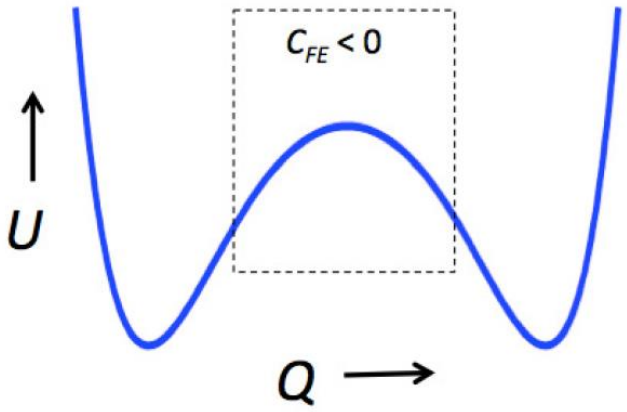


Fig. 2.2 The energy double well diagram of a ferroelectric material. The area under the dashed region represents negative capacitance region [45]

P, in common ferroelectric materials because *P* is much bigger than *E*. As a result, we can use *P* and *Q* interchangeably [46]. When we compare the energy landscapes of a typical ferroelectric material as in Fig. 2.2 and a regular capacitor as in Fig. 2.1 (b), we see that the curvature around Q = 0 in a ferroelectric material is opposite to that of a regular capacitor. This opposing curvature raises the potential of a negative capacitance for the ferroelectric material close to Q = 0, keeping in mind that the energy of a regular capacitor is given by $(Q^2/2C)$. As a result, a ferroelectric material can exhibit negative capacitance around this point [47].

2.2.3 Landau Theory of Negative Capacitance

The free energy (U) of a ferroelectric can be expressed as an even-order polynomial of the polarization P [48] as follows:

$$U = \alpha P^2 + \beta P^4 + \gamma P^6 - EP \tag{2.1}$$

where, $E=V/t$, denotes the electric field applied, with V representing the voltage applied across the ferroelectric and t representing the ferroelectric thickness respectively. The α, β, and γ are the ferroelectric material parameters. β is negative for a first order phase transition and positive for a second order phase transition, whereas γ is always positive. $\alpha = \alpha_0(T-T_C)$, where α_0 is independent of temperature and always positive, T and T_C are temperature and Curie temperature, respectively [49]. Consequently, when the temperature is below the Curie temperature, the α_0 coefficient is negative, which leads to the negative curvature of the energy landscape of a ferroelectric around $P = 0$. This negative curvature gives rise to the characteristic double-well energy landscape observed in ferroelectric materials [50].

Furthermore, at equilibrium, $dU/dP=0$, the following equation is obtained:

$$E = 2\alpha P + 4\beta P^3 + 6\gamma P^5 \tag{2.2}$$

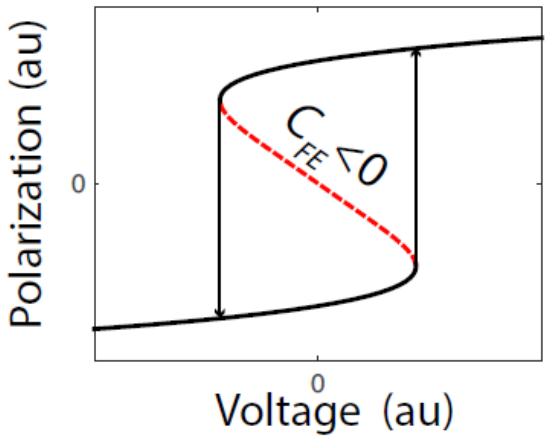


Fig. 2.3 Polarization characteristics of a ferroelectric material according to Landau theory [51]

Fig. 2.3 depicts the polarization-voltage characteristics of a ferroelectric capacitor as determined by equation 2.2 [51]. A ferroelectric capacitor exhibits non-linear charge-voltage properties, according to the Landau theory of ferroelectrics. There is a charge and voltage range, represented by the red dashed curve, where negative capacitance can be identified.

2.3 NCFET: Steep Switching

Field effect transistors are unable to efficiently control the heat generated, leading to the Boltzmann tyranny limit on the dimensional scalability of FETs. To circumvent this fundamental constraint and reduce power dissipation in electronic devices, negative capacitance employing ferroelectric materials has emerged as a promising solution. Fig. 2.4 (a) shows the schematic structure of NCFET which adds a ferroelectric layer in the gate stack of a conventional MOSFET [52]. The steep switching in Ferroelectric FET can be explained by using the following equation of SS obtained using the equivalent capacitance model in Fig. 2.4 (b) [53]:

$$SS = \frac{\partial V_g}{\partial log_{10} I_D} = \frac{\partial V_g}{\partial V_{int}} \frac{\partial V_{int}}{\partial \psi_S} \frac{\partial \psi_S}{\partial log_{10} I_D} = \frac{1}{A_v . m} \frac{\partial \psi_S}{\partial log_{10} I_D} \tag{2.3}$$

Here, V_{int} is the internal voltage and ψ_S is the surface potential. At room temperature, the final part in Equation 2.3 equates to a 60 mV/decade change. Since m is always less than one and A_v

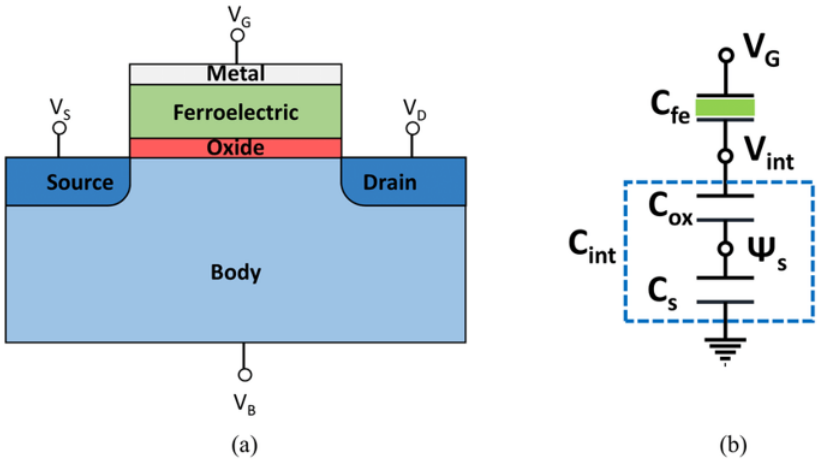


Fig. 2.4 (a) Ferroelectric material based negative capacitance FET (b) equivalent capacitance model [52]

is always one, the value of SS in a conventional transistor is always greater than one. In the case of an NCFET, however, the ferroelectric material can enter a negative capacitance state, resulting in a voltage amplification effect at the interface between the ferroelectric and oxide layers [53]. This leads the value of A_v to exceed one. This amplification factor offsets the effect of the m component in Equation 2.3, assisting in the suppression of the SS. If A_v is significantly bigger than m, SS can be reduced below the Boltzmann limit of 60mV/decade.

Due to its elegance and simplicity, as well as the pressing demand for a new transistor, as Moore's law nears its limits, numerous researchers in industry and academia have been captivated by the concept of the device. They have conducted extensive investigations into the physics and technology of the NCFET, leading to a significant volume of scholarly articles published on the subject since 2008.

2.4 Literature Review

Ferroelectricity was initially discovered in 1920, but the concept of negative capacitance is relatively recent. Many researchers have attempted to minimize the Boltzmann limit by modifying the structure and materials employed. In 2008, Salahuddin et al. were the first to

report that SS could be reduced below the fundamental limit by utilizing a ferroelectric material as the gate insulator in a MOSFET. In the same year, Giovanni A. Salvatore et al. conducted the first experimental demonstration of an NCFET, achieving a minimum SS of 13 mV/decade using a 40 nm P(VDF-TrFE)/SiO_2 gate stack [54]. Since then, the NCFET has garnered considerable attention worldwide. In 2011, Khan and his research group explained the impact of negative capacitance in nanoscale ferroelectric dielectric heterostructures. They utilized a ferroelectric bilayer of $Pb(Zr_{0.2}Ti_{0.8})O_3$ and a dielectric material $SrTiO_3$. The device exhibited a minimum SS of 13 mV/decade, accompanied by an impressive on/off current ratio of approximately 10^7 [55].

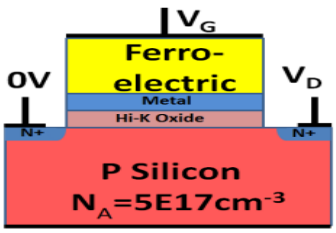
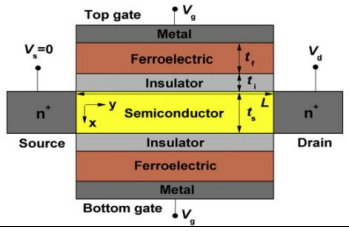
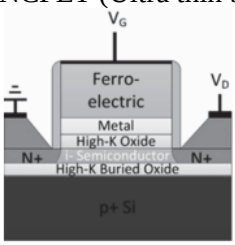
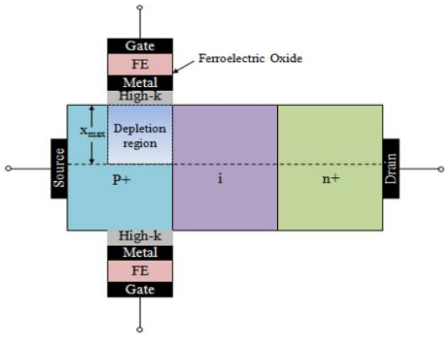
Researchers have employed various ferroelectric materials in the demonstrations of NCFETs. This includes conventional perovskite materials like $BaTiO_3$ and $PbZr_xTi_{1-x}O_3$, as well as organic polymer ferroelectrics such as $P(VDF_x\text{-}TrFE_{1-x})$ [56]. Initially, there was a focus on ferroelectric materials like strontium bismuth tantalite (SBT) and lead zirconate titanate (PZT) due to their desirable dielectric, ferroelectric properties, low leakage current, and long polarization retention. However, these materials exhibited unstable ferroelectric behavior in thin film morphologies and were incompatible with standard IC processing technologies [57]. A significant breakthrough occurred with the discovery of doped HfO_2 ferroelectrics. The discovery of hafnium oxide (HfO_2) based dielectrics presented a promising solution to overcome the limitations faced by previous ferroelectric materials. T. S. Boscke demonstrated ferroelectric properties in Si-doped HfO_2 materials in 2011 [58], and ferroelectric behavior was also discovered in Zr-doped HfO_2 in the same year [59]. Subsequent to that, research studies have demonstrated the ferroelectric properties of HfO_2 doped with Al [60], Y [61], Cd [62], La, and Sr [63]. Among these, HfO_2 materials doped with Zr have garnered significant attention due to their scalability to ultrathin films while maintaining desirable ferroelectric behavior.

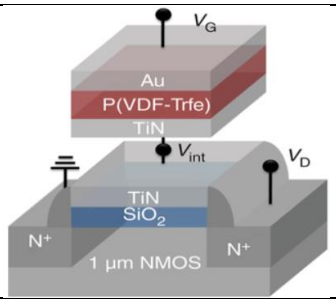
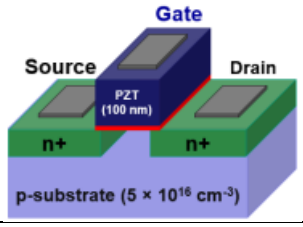
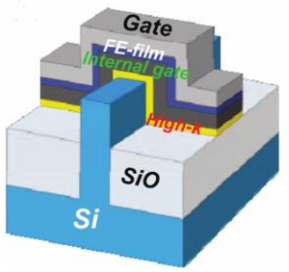
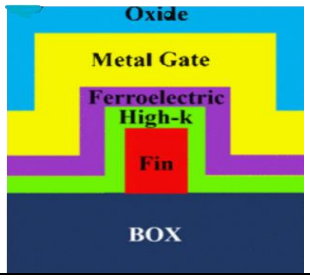
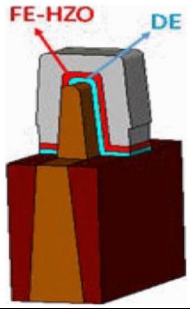
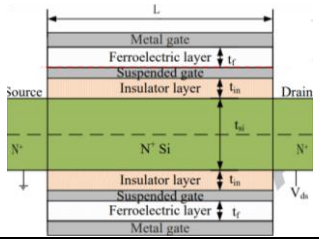
In 2018, the discovery of ferroelectric materials based on Zr-doped HfO_2 brought about a breakthrough. These materials allowed for the scaling of the ferroelectric layer below 5 nm while still preserving a sufficiently strong polarization intensity [64]. This achievement was crucial in incorporating the negative capacitance effect in highly scaled transistor devices. In 2019, D. Kwon conducted a study where NCFET was fabricated using Zr-doped HfO_2 with a thickness of 1.8 nm. The results showed a steep SS of 20 mV/decade and a 10 times reduction in off current at a channel length of 30 nm, along with a significant improvement in on current compared to baseline transistors based on undoped HfO_2 [65]. In 2020, D. Kwon et. al. further demonstrated the persistence of spontaneous and switchable polarization in Zr-doped HfO_2 down to a thickness of one nm. This achievement was accomplished through the use of the atomic layer deposition method [66]. Ferroelectric materials based on Zr-doped HfO2 (HZO) offer several advantages over other known ferroelectric materials. They are compatible with modern semiconductor fabrication processes, thermally stable, exhibit higher dielectric permittivity, and possess a wide bandgap that helps suppress leakage current. Additionally, they can be scaled down to a thickness of 1 nm or less while maintaining a strong polarization intensity, making them highly attractive for advanced device applications.

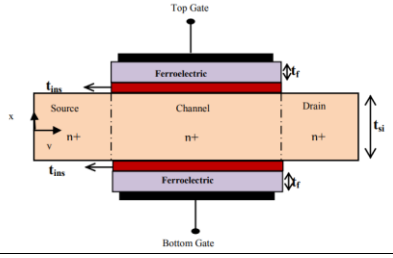
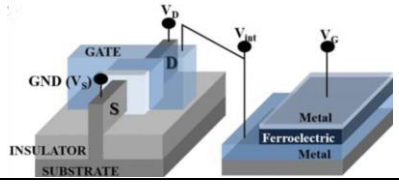
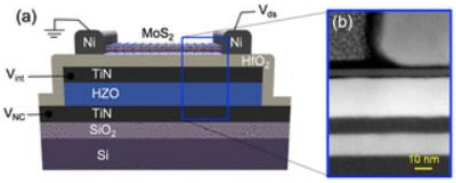
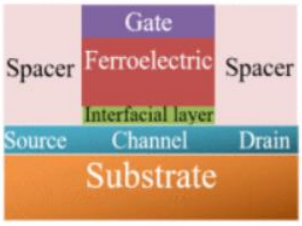
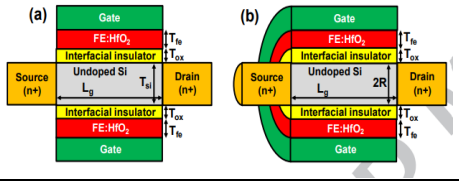
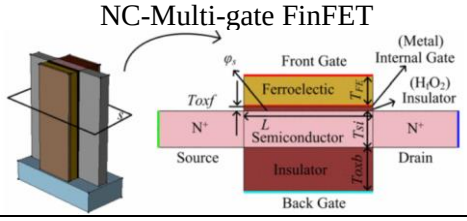
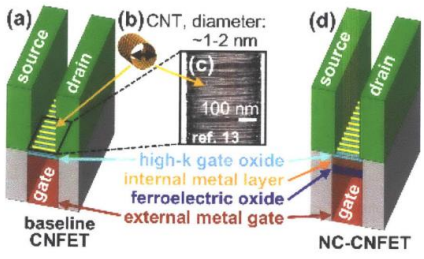
Furthermore, one of the primary benefits of the negative capacitance (NC) effect is its ability to be integrated into a variety of transistor architectures by simply inserting a ferroelectric material layer in the gate stack. Numerous NCFET modifications have been investigated and shown as a result of this great compatibility with various transistor configurations. Planar NC-FETs, 2D NC-FETs [67], NC-JL-FETs [68], NC-JLNW-FETs [69], NC-FinFETs [70], NC-TFETs [71], NC-GAA-FETs [72], NC-GAA-TFETs [73], and NC-JLGAA-FETs [74] have all been proposed and experimentally proved. These transistor architectures demonstrated sub-60mV/decade SS and improved on-state current, demonstrating the effectiveness of the NC effect in improving device performance. A comparative summary of various NCFET structures

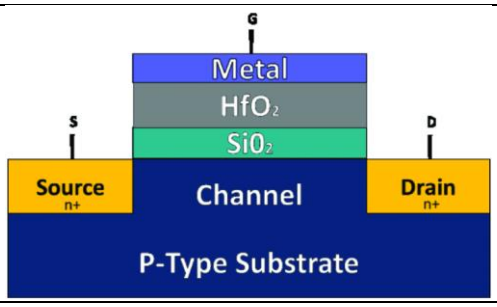
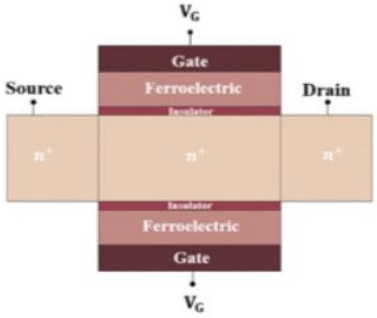
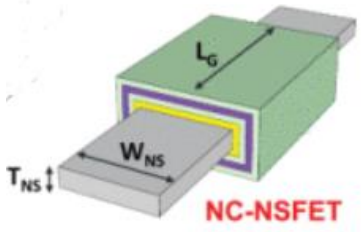
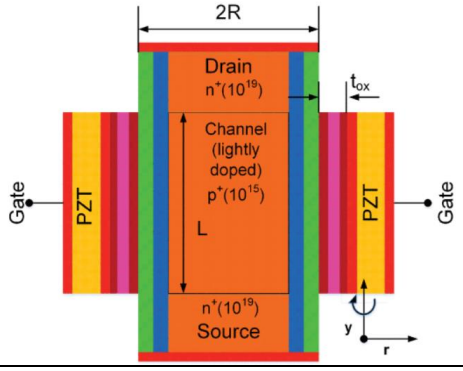
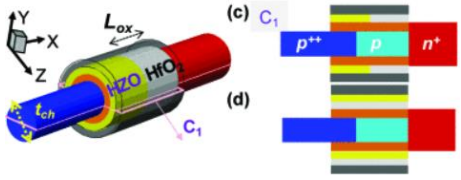
is reported in Table 2.1. In this table, various NCFET structures, ferroelectric materials, and their respective performance are presented.

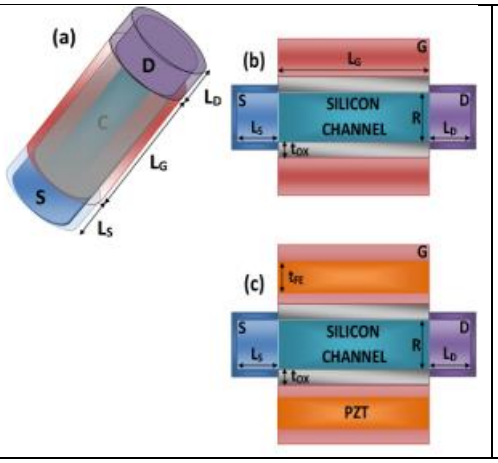
Table 2.1 Comparative summary of NCFET structures

Ref.	Author & Year	Ferroelectric NCFET Structures	Ferroelectric materials	Performance
[55]	A.I. Khan et. al. 2011	Planar 	$Pb(Zr_{0.2}Ti_{0.8})O_3$	• SS_{min}= 13 mV/dec • I_{on}/I_{off} ratio = 10^7
[75]	Y.G. Xiao et. al. 2012	Planar 	Strontium Bismuth Tantalite (SBT)	• SS_{min}= 28.9mV/dec • I_{on}/I_{off} ratio = 10^{12}
[76]	Yeung et. al. 2013	UTB- NCFET (Ultra thin body) 	Zr-doped HfO_2	• SS_{min}= 21 mV/dec • I_{on}/I_{off} ratio = 10^9
[77]	N. Chowdhary et. al. 2014	NC TFET 	$BaTiO_3$	• SS_{min}= 13.87mV/dec • I_{on}/I_{off} ratio = 10^{10}
[78]	J. Jo. et. al. 2015	Planar	$P(VDF_{0.75}$-$TrFE_{0.25})$	• SS_{min}= 18 mV/dec • I_{on}/I_{off} ratio = 10^7

				
[79]	S. Dasgupta et. al. 2015	Planar 	$Pb(Zr_{0.52}Ti_{0.48})O_3$	• SS_{min}= 13 mV/dec • I_{on}/I_{off} ratio = 10^8
[80]	K.S. Li. et. al. 2015	NC-FinFET 	$HfZrO_2$	• SS_{min}= 55 mV/dec • I_{on}/I_{off} ratio = 10^6
[81]	C. Hu. et. al. 2015	NC-FinFET 	PZT	• SS_{min}= 32 mV/dec • I_{on}/I_{off} ratio = 10^7
[82]	M.H. Lee et. al. 2016	NC-FinFET 	$HfZrO_x$	• SS_{min}= 52 mV/dec • I_{on}/I_{off} ratio = 10^{10}
[83]	C. Jiang et. al. 2016	NC-DG-Junctionless FET 	SBT	• SS_{min}= 10 mV/dec • I_{on}/I_{off} ratio = 10^{11}

[84]	H. Mehta et. al. 2016	NC-DG-Junctionless FET 	Si doped HfO_2	• SS= 10 mV/dec • I_{on}/I_{off} ratio = 10^{14}
[85]	Eunah Ko. et. al. 2017	NC-FinFET 	$HfZrO_2$	• SS_{min}= 36 mV/dec • I_{on}/I_{off} ratio = 10^{10}
[86]	F.A. McGuire et. al. 2017	NC-MoS2 2D FET 	$HfZrO_2$	• SS_{min}= 6.07 mV/dec • I_{on}/I_{off} ratio = 10^{9}
[87]	Dong et. al. 2017	UTB NC-FET 	Al:HfO_2	• SS_{min}= 53.9 mV/dec • I_{on}/I_{off} ratio = 10^{9}
[88]	Jang et. al. 2017	NC-DGFET and NC-GAA- Nanowire FET 	Fe:HfO_2	• SS_{min}= 40, and 30 mV/dec • I_{on}/I_{off} ratio = 10^{5}, 10^{6}
[89]	T. Yang et. al. 2018	NC-Multi-gate FinFET 	HfSiO	• SS_{min} = 42 mV/dec • I_{on}/I_{off} ratio = 10^{12}
[90]	T. Srimani 2018	NC-CNFET 	Al:HfO_2	• SS_{min} = 55 mV/dec • I_{on}/I_{off} ratio = 10^{11}
[91]	Rahman et. al.	Planar	Si-doped HfO_2	• SS_{min} = 30 mV/dec • I_{on}/I_{off} ratio = 10^{10}

	2019			
[73]	Y. Choi. et.al. 2019	Junctionless Gate-All-Around Nanowire NC- FET 	Si-doped HfO_2	• SS_{min} = 35 mV/dec • I_{on}/I_{off} ratio = 10^9
[92]	Fahimul Islam Sakib et. al. 2020	NC- nanosheet GAA FET 	Al:HfO_2	• SS_{min} = 31 mV/dec • I_{on}/I_{off} ratio = 10^8
[93]	K. Hosen et. al. et. al. 2021	GAA-WSe2-NCFET 	PZT	• SS_{min} = 18.9 mV/dec • I_{on}/I_{off} ratio = 10^{12}
[74]	N. Thoti et. al. 2022	Ferroelectric Nanowire Tunnel FET 	HZO	• SS_{min} = 33.3 mV/dec • I_{on}/I_{off} ratio = 10^{12}
[72]	L. R. Solay et. al. 2022	Gate-All-Around NC-Dopingless Nanowire Tunnel FET	PZT	• SS_{min} = 17.5 mV/dec • I_{on}/I_{off} ratio = 10^{12}

There have also been theoretical investigations into NCFETs by numerous research groups. Jiménez et al. developed a physics-based model for the surface potential and drain current of long-channel Double Gate Negative Capacitance FETs [94]. They investigated the impact of the NC phenomenon on device performance using the ferroelectric material SBT. Another study focused on analytical modeling of long-channel gate-all-around NC transistors by Xiao et al. [95]. When compared to typical gate-all-around FETs, these devices have sub-60 mV/dec SS and strong on-state current (I_{on}). This demonstrates NC transistors' potential for better device performance. In 2016, Mehta et. al. developed an analytical model for Double Gate Junctionless NCFET [84]. There was a significant improvement in terms of gain, minimum subthreshold swing values, and I_{on}/I_{off} ratio. Furthermore, it is challenging to fabricate the Metal-Ferroelectric-Semiconductor (MFS) structure and often leads to interface defects at the ferroelectric-silicon interface. To address this issue, several research groups [96]–[98] have demonstrated NCFETs with a structure similar to Metal-Ferroelectric-Insulator-Semiconductor (MFIS). In these devices, the insulator layer between the ferroelectric and semiconductor helps stabilize the NC effect, making MFIS structures more promising for future transistor applications. The impact of the interface layer on the electrical characteristics of NCFETs has been extensively investigated in various analytical studies [99]–[102]. Analytical models for NCFETs with MFIS structures have been developed for multiple gate geometries (single gate,

double gate, etc.) [52], [103], [104]. These studies have reported that the interface layer significantly affects the on-state current and SS of the device, leading to improved overall performance of NCFETs by stabilizing the NC effect.

As mentioned earlier, ferroelectric materials exhibit ferroelectric behavior up to their Curie temperature, and the NC effect is strongly temperature dependent [105], [106]. In light of this, both theoretical and experimental studies have been conducted to investigate the impact of temperature on the electrical characteristics of NCFETs [107]–[111]. These studies have reported that temperature serves as an effective tuning parameter for the NC effect. It has been observed that as the temperature increases, the step-up conversion capability of NCFETs diminishes, and the NC effect disappears above the Curie temperature of the ferroelectric material. In other words, the ability of the ferroelectric material to enhance the gate voltage and suppress the subthreshold swing is reduced at higher temperatures. This temperature dependence of the NC effect is an important consideration in the design and operation of NCFETs.

Moreover, in several experimental configurations, NCFETs have proven speed improvements over traditional FETs. In a ring oscillator experiment, for example, NCFETs outperformed conventional FETs in terms of speed [112]. This means that NCFETs can reach quicker switching speeds and higher operating frequencies, which is beneficial in digital circuit applications [113]. Furthermore, the usage of NCFETs has resulted in gains in other performance measures. Using NCFETs, for example, has been shown to improve inverter gain, device cut-off frequency, and Static Random Access Memory (SRAM) noise margin [114], [115]. These advancements imply that NCFETs have the potential to improve circuit performance, resulting in improved overall device operation and functionality in a variety of applications.

2.5 Research Gaps

Based on the literature survey, the following research gaps were identified:

- Fabrication feasibility is a difficult point to achieve when working with non-planar ferroelectric devices.
- The effect of temperature on device performance needs to be examined in order to meet the ongoing demand for transistors with high and low temperature tolerance.
- Analytical study is required to better understand the physics and low power requirement of negative capacitance based FE-FET.
- Small Signal Modeling of negative capacitance based FE-FET needs to be explored.
- The application of device in Biosensors needs to be explored.

2.6 Research Objectives

From the foregoing discussion the following objectives have been achieved in our thesis:

- To critically examine the ferroelectric FET for high frequency applications and its comparison with the existing device topologies.
- Analytical study of the various performance parameters of the negative capacitance based ferroelectric FET.
- To study the effect of temperature on the negative capacitance based ferroelectric FET.
- To study and analyze the application of negative capacitance based ferroelectric FET in Biosensors.

The purpose behind these objectives is to find a novel device structure that overcomes the fabrication complexity of the non-planar ferroelectric devices without deteriorating the overall performance of the device. Therefore, in this thesis, the impact of incorporating a ferroelectric layer in Junctionless Accumulation Mode FET has been studied and investigated to achieve the required objectives.

Chapter 3

Single Gate Junctionless Accumulation Mode Ferroelectric FET: Simulation Study

In the previous chapters, we have already covered the inception and development of MOSFETs throughout their history, as well as the concept of ferroelectric materials based NCFET and the exploration of the subsequent structures and principles in greater depth. In this chapter, a single gate Junctionless Accumulation Mode Ferroelectric Field Effect Transistor (JAM-FE-FET) has been proposed combining the merits of Junctionless Accumulation Mode and Negative Capacitance effect such as fabrication feasibility, low power dissipation, and reduced degradation in mobility. The benefit of JAM over existing FETs is that it combines the benefits of the junctionless transistor (JLT) and conventional FETs. It avoids excessive parasitic resistance due to stronger doping in the source and drain areas, resulting in higher conductivity and better characteristics than JLT. The proposed devices is assessed in terms of RF/analog specifications for varied channel lengths through simulations study. Major analog metrics like transconductance (g_m), intrinsic gain (A_V), output conductance (g_d), and early voltage (V_{EA}), I_{on}/I_{off} and Transconductance Generation Factor (TGF) are obtained for the JAM-FE-FET arrangement. Further, frequency analysis of the proposed device is performed using several critical RF parameters like cut-off frequency (f_T), Transconductance Frequency product (TFP), Gain Frequency Product (GFP), and Gain Transconductance Frequency Product (GTFP) respectively. This chapter also talks about the small signal parameters at various ferroelectric thicknesses. Further, the effect of temperature variation on the device performance parameters has also been analyzed.

3.1 Introduction

Various MOSFET structures have been realized over the last few decades, and their scaling has been quite successful down to the nanoscale, resulting in a significant increase in performance [116],[117]. However, when the size of such transistors is reduced, junctions become closer, which is difficult due to the significant doping concentration gradients required. In order to combat this problem, J. E. Lilienfeld in the 1920s introduced the concept of Junctionless transistors [1]. It was successfully fabricated at the Tyndall Institute by Colinge et al [118]. The major characteristic feature of this device is the absence of p-n junction which avoids the requirement of gradients in doping concentration [119]. Various analytical study of the surface potential for junctionless transistor has also been done [120],[121]. It has also been reported that cylindrical surrounding gate MOSFETs show good switching performance and also can be used for microwave frequency applications [122]–[124]. However, the junctionless transistor poses various limitations such as degraded mobilities due to high doping concentrations.

Also, some of the significant obstacles in the device include the higher gate work function for a completely depleted channel region in order to ensure turning off the device. To address the aforementioned issues, a newly modified structure known as the JAM FET was introduced [29], which has highly doped S/D regions and decreased doping in the channel, resulting in reduced mobility deterioration [28]. Another major issue that has arisen as a result of shrinking and the increased density of transistors on a chip is higher power consumption and heat dissipation, both of which slow down the data processing rate [8],[125]. This can be enhanced by overcoming the lower working voltage restriction known as ‘Boltzmann's Tyranny,' which allows the transistor operation voltage to be reduced, lowering power consumption. One such promising device is the ferroelectric field effect transistors (FE-FETs) [126]. Various investigations to understand the behavior of FE-FETs have been conducted in the past [75],

[127], [128]. The majority of the research, however, concentrated on hysteretic behavior in memory applications [98],[129].

The discovery of ferroelectric properties in hafnium oxide (HfO_2) [58] in 2011 has gained a lot of attention [130],[131] because of its CMOS compatibility. Higher remnant polarization and large coercive field, at minimal thickness [132],[133], and superior performance characteristics have been demonstrated in ferroelectric HfO_2[134]. Due to its lower annealing temperature [135] and customizable ferroelectric properties, zirconium-doped HfO_2 (HZO) has popped up as a potential material [96],[136]. Apart from realizing memory, ferroelectric hafnium oxide is the sole material system that may be utilized to realize a new form of steep slope device called a Negative Capacitance Field Effect Transistor (NCFET) that was proposed in 2008 [53]. NCFET has been studied both theoretically and practically for digital applications due to its ability to produce a subthreshold swing (SS) of 60 mV/decade [137],[138]. Although there are several demonstrations and investigations of digital and DC behavior of NCFET in the reported literature, the high frequency (RF) capabilities of NCFETs are yet to be fully explored. For RF applications of NCFET in the future, research in this direction is crucial. Most of the previous research on NCFET has focused on Metal ferroelectric metal insulator semiconductor (MFMIS) configuration structure [139]–[142]. This structure simplifies modeling since the ferroelectric–insulator interface has a uniform potential, but the leakage currents would render the negative capacitance of ferroelectric FET unstable. Because of this instability, it is difficult to bias MFMIS devices and circuits, making the MFMIS structure unsuitable for RF applications. A metal–ferroelectric–insulator–semiconductor (MFIS) structure, on the other hand, mitigates these issues [143] and produces different overall device properties as a result of a spatially changing ferroelectric potential than MFMIS devices. Thus, the MFIS structure have always been preferred for integrating in advanced technologies. RF performance of MFIS NCFETs has also been investigated in few research. Experiment in [112] revealed a modest

improvement in f_T, while simulations by [144] revealed circuit-level figures of merit. However, no report has been published on the RF performance of JAM-FE-FET. Quantum confinement is also investigated in relation to ferroelectric thickness (t_{FE}) and channel thickness (t_{ch}). The quantum confinement effect reduces when the valus of t_{FE} and tch are greater than 7 nm and 15 nm respectively [145]. In our study, quantum mechanical effect has not been considered and therefore, the channel thickness and ferroelectric thickness are restricted to 20 nm and 10nm respectively. Thus, motivated by these coexisting research findings, a novel device structure, JAM-FE-FET is reported in this chapter. This study takes the entire RF capabilities of NCFET with MFIS structure and incorporating the benefits of JAM FET.

3.2 Existing Device Topologies

3.2.1 JAM Structure

A significant development in semiconductor device technology is the development of Junctionless Accumulation Mode FET (JAMFET). To comprehend its evolution, let's start with the fundamental MOSFET. The MOSFET was first presented as a basic transistor design. It consists of a silicon dioxide or other thin insulating layer sandwiched between a metal gate and a semiconductor channel. The gate voltage controls the flow of current through the channel by altering the conductivity of the channel region. Over time, researchers and engineers sought to improve the performance and characteristics of MOSFETs. One significant challenge was reducing the fabrication complexity and costs associated with the device's structure. This led to the exploration of novel transistor designs, including the concept of a junctionless transistor. The junctionless transistor eliminates the need for traditional pn junctions, which are present in conventional MOSFETs. It has a number of benefits, such as streamlined fabrication procedures, superior electrostatic control, decreased leakage currents, and increased scalability. However, it has some drawbacks, such as low ON current and transconductance, due to carrier

mobility degradation, which have been addressed by another junctionless structure known as the Junctionless Accumulation Mode (JAM).

3.2.2 Ferroelectric FET

In Ferroelectric FET, a thin layer of ferroelectric material is integrated into the gate stack of the transistor. When a voltage is applied to the gate, the ferroelectric undergoes a phase transition, resulting in a negative capacitance effect. This causes the transistor to exhibit enhanced voltage amplification and improved subthreshold swing, allowing for lower power consumption and faster switching speeds. The previous chapter provides an extensive explanation of the ferroelectric FET, including comprehensive details about its functioning and characteristics.

3.3 Proposed Structure & Simulation Parameters

The schematic illustration of a JAM-FE-FET is shown in Fig. 3.1. All simulations are run on the TCAD Silvaco ATLAS simulator, with the Shockley-Read-Hall (SRH) recombination, ferro model, Lombardi CVT model, fermi and Landau-Khalatnikov (LK) models [146] being used. Landau-Khalatnikov (LK) ferroelectric interface model ATLAS has the ability to model a ferroelectric film as an interface model between a conventional gate insulator and a semiconducting channel. These models are discussed in Table 3.1.

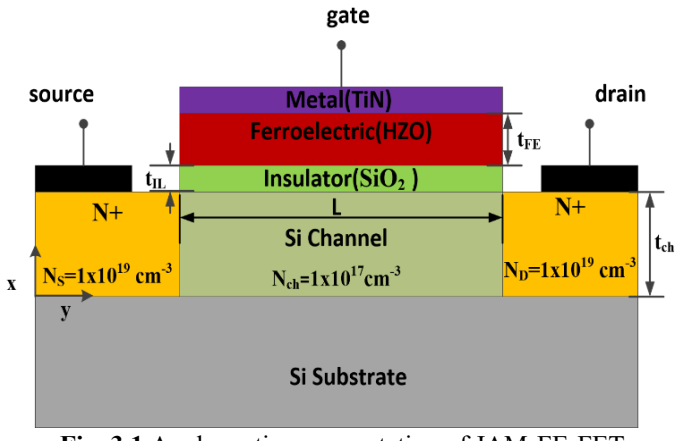


Fig. 3.1 A schematic representation of JAM-FE-FET

Table 3.1 Physical models used in the simulation

Models	**Description**
Lombardi CVT model	This model overrides any other mobility models which may be specified in the MODELS statement. The Lombardi CVT model is used because it considers a large temperature range with parallel and perpendicular field-dependent mobility.
Shockley-Read-Hall (SRH) recombination model	Shockley-Read-Hall (SRH) recombination model with concentration-dependent lifetimes accounts for minority recombination.
Fermi model	Includes the effects of Fermi statistics into the calculation of the intrinsic concentration in expressions for SRH recombination.
Landau-Khalatnikov Ferro model	The model is enabled by specifying the flag LKFERRO on the INTERFACE statement, along with the LKCORECIVE and LKREMNANT parameters.

According to previous research, the negative capacitance is caused by a unique relationship between the electric field (E_{FE}) and polarization (P) of the ferroelectric layer which is given by the following equation:

$$E_{FE} = \alpha P + \beta P^3 + \gamma P^5 + \rho \frac{dP}{dt} \qquad (3.1)$$

where α, β, and γ are the ferroelectric material parameters and ρ is the kinetic coefficient linked to the time constant associated with the change in ferroelectric polarization. The parameters for the compared devices are enlisted in Table 3.2. The proposed structure comprising a gate stack of TiN/HZO/SiO_2 is employed in the simulations. The channel length (L) is varied from 90 nm to 32 nm and channel thickness (t_{ch}) is taken 20 nm. A ferroelectric layer with a thickness (t_{FE}) of 10 nm and an insulator layer thickness (t_{IL}) of 0.9 nm in the gate stack. In JAM-FE-FET, the doping in the silicon channel is 1e17 cm^{-3} with n-type dopants, whereas the source and drain regions are doped strongly with 1e19 cm^{-3} n-type dopants. The doping level for the entire simulation is considered to be uniform. Titanium Nitride (TiN) having work function (ϕ_m) 4.65eV is used as gate material.

Table 3.2. Various parameters employed for the device simulation

Parameter	Symbol	JL-FE-FET	JAM-FE-FET
Channel length	L	90,45,32 nm	90,45,32 nm
Channel thickness	t_{ch}	20 nm	20 nm
Ferroelectric thickness	t_{FE}	10 nm	10 nm
Insulator thickness	t_{IL}	0.9 nm	0.9 nm
Source/Drain doping	$N_{S/D}$	$1x10^{19}$ cm^{-3}	$1x10^{19}$ cm^{-3}
Channel doping	N_{ch}	$1x10^{19}cm^{-3}$ (n-type)	$1x10^{17}cm^{-3}$(n-type)
Metal work function	ϕ_m	4.65 eV	4.65 eV

Thereafter, numerical approaches such as Gummel and Newton, have been contemplated to improve convergence. In addition to these, the specific properties of the ferroelectric material (HZO) are listed in Table 3.3, that induces the negative capacitance effect. The drain to source voltage (V_{ds}) was set to 50 mV and the gate to source voltage (V_{gs}) was varied from 0 to 1 V to obtain the transfer characteristics. Fig. 3.2 shows the drain current with and without quantum model. As seen in Fig. 3.2, quantum effects have no influence on the transfer characteristics and have thus been ignored in this study.

Table 3.3. Properties of ferroelectric material (HZO)

Parameter	Symbol	Values
Spontaneous Polarization	Ps	10-40μC/cm2
Remnant Polarization	Pr	1-40μC/cm2
Coercive Field	Ec	1-2MV/cm
Dielectric constant	ε	30

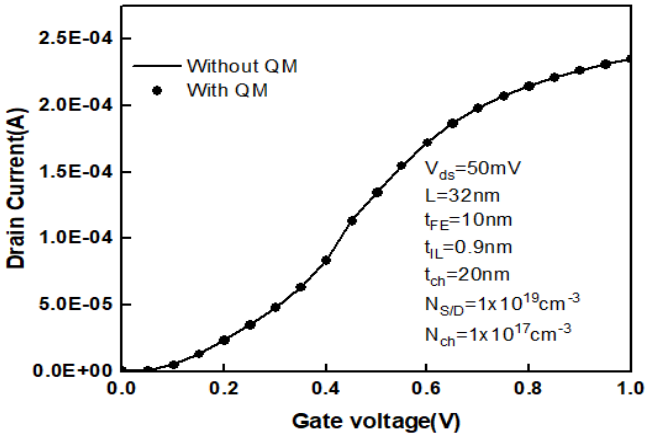


Fig. 3.2 The effect of the Quantum Model (QM) on the drain current

3.4 Device fabrication and calibration

3.4.1 Need for fabrication

The need for fabrication arises from the desire to translate theoretical concepts and designs into practical devices. Fabrication involves the manufacturing process of creating physical structures and components based on specific designs and specifications. It involves the precise implementation of the proposed transistor structure, including the integration of various materials and components. It enables scientists to experiment with various parameters, test and validate their theories, and assess the effectiveness of the fabricated devices. Fabrication also allows for customization and optimization of transistor designs based on specific requirements. It enables the integration of transistors into integrated circuits (ICs) and the realization of complex electronic systems. Overall, fabrication is vital for bridging the gap between theoretical concepts and practical applications. It plays a crucial role in the development, production, and optimization of transistors, including ferroelectric FETs, enabling their incorporation into various electronic devices and technologies.

3.4.2 Proposed fabrication details

The fabrication of ferroelectric negative capacitance field effect transistor has been explained by D. Kwon et al. in 2019 [147]. The transistor can be fabricated by taking a silicon substrate

followed by the active region formation using photolithography. Next, the exposed regions have to be etched deep down for the gate stack formation after RCA cleaning. On top of the wafer, rapid thermal annealing (RTA) treatment can be used to grow SiO_2 layer. Further, the ferroelectric gate oxide, an HZO film deposition using atomic layer deposition (ALD) has to be performed.

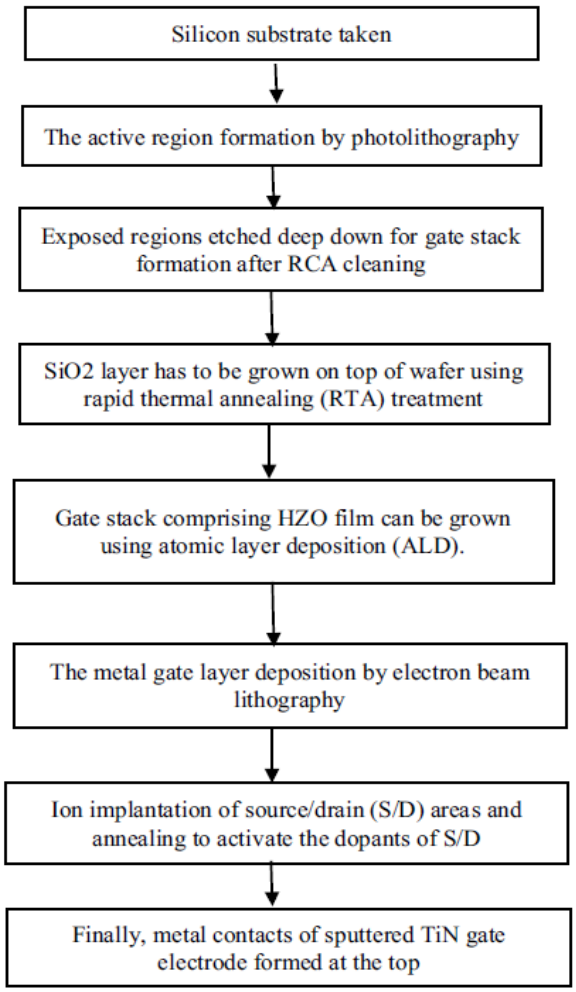


Fig. 3.3 Fabrication flowchart of proposed JAM-FE-FET

For short channel devices, electron beam lithography can be used to define the gate region. Ion implantation can then be performed on the exposed source/drain (S/D) areas. Next, the post metallization anneal in N_2 ambient can be performed for dopant activation and finally metal contacts of sputtered TiN gate electrode can be formed at the top. The steps of fabrication process are shown by a flowchart in Fig. 3.3. The proper calibration of this research work is

done with the experimental ferroelectric research under the same device dimensions [147]. The Shockley-Read-Hall (SRH) recombination, ferro model, Lombardi CVT model, fermi, and Landau-Khalatnikov (LK) models are used for calibration. The transfer characteristic curves in Fig. 3.4, are in good agreement with one other.

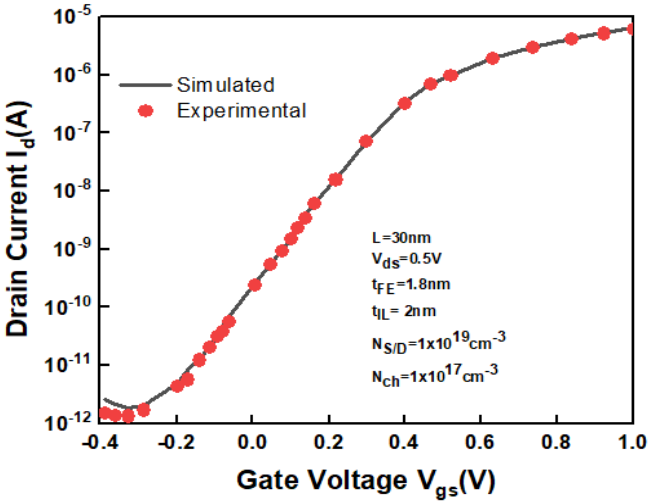


Fig. 3.4 Calibrated transfer characteristics of simulation data with experimental data [147]

3.5 Results & Discussions

3.5.1 Analog/RF performance parameters

Fig. 3.5 (a) demonstrates how the drain current of JAM-FE-FET and JL-FE-FET varies with gate voltage for various channel lengths. It depicts that JAM-FE-FET have higher drain current over JL-FE-FET. The greater mobility of carriers in the channel is responsible for this improvement. The on current (I_{on}) increases dramatically when the channel length L is scaled down from 90 nm to 32 nm, as shown in Fig. 3.5 (a). The results for I_{on} increment in short channel can be intuitively explained through velocity saturation theory in which the inversion region current is in proportion to the device total oxide capacitance [148].

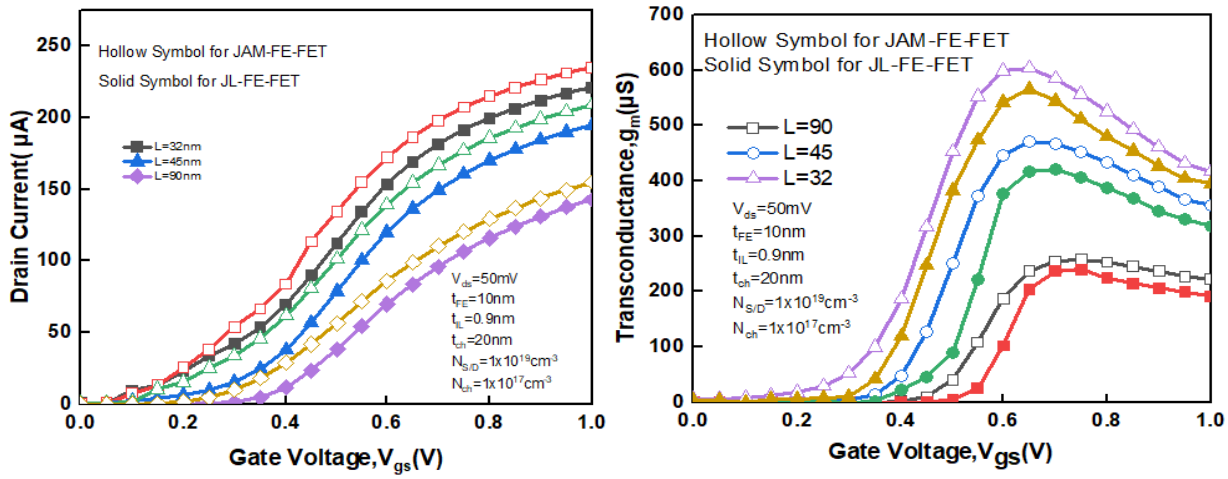


Fig. 3.5. (a) Drain current variation with V_{gs} (b) Transconductance variation with V_{gs}

Transconductance is a measurement of the relationship between the deviation in drain current and the change in V_{gs} at constant V_{ds}. As illustrated in Fig. 3.5 (b), g_m is calculated using the I_d-V_{gs} curve derivative. Since the gate control over channel has been enhanced, and short channel effects have been decreased, the JAM-FE-FET has the highest transconductance value when compared to JL-FE-FET. Additionally, gate-stack construction improves average carrier velocity, which leads to higher electron mobility and, eventually, increased g_m.

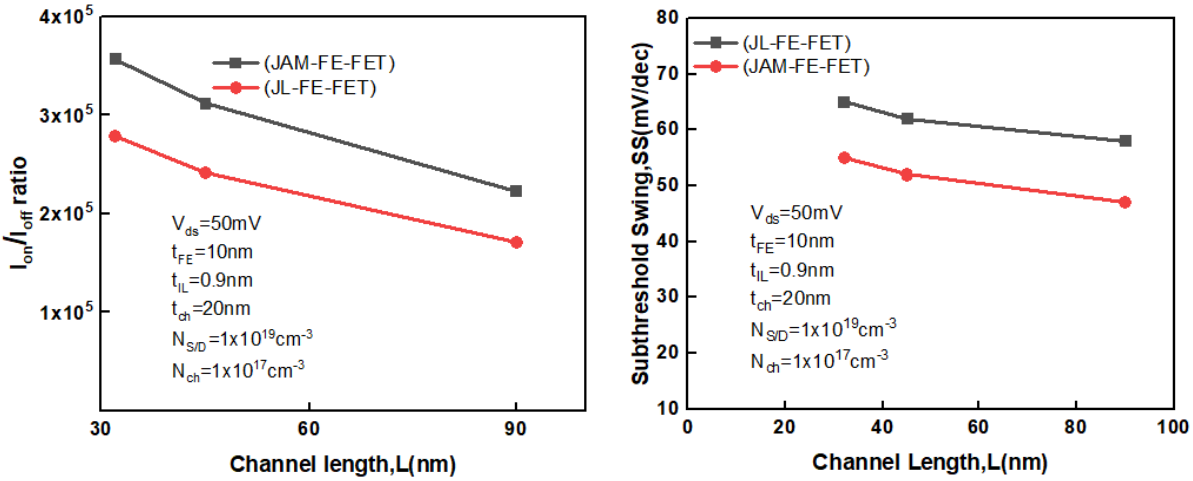


Fig. 3.6. (a) I_{on}/I_{off} variation with channel length (b) SS variation with channel length

Fig. 3.6 (a) shows the I_{on}/I_{off} ratio variation for JAM-FE-FET and JL-FE-FET for different channel lengths. I_{on} and I_{off} for these devices are obtained at V_{gs}= 1V and V_{gs}= 0V respectively

for V_{ds}= 50mV. It is one of the most critical parameters for digital applications. The I_{on}/I_{off} ratio for the compared devices is shown in Table 3.4. It can be assessed that I_{on}/I_{off} ratio for channel length L= 90 nm is low for digital devices. However, an improvement in I_{on}/I_{off} ratio of JAM-FE-FET over JL-FE-FET for channel length L= 32 nm has been obtained due to increased mobility in JAM configuration leading to an increase in drain current with the reduction in current leakage and consequently greater switching ratio. The subthreshold swings for the compared devices are shown in Fig. 3.6 (b). It has been discovered that both devices have steep SS behavior (<60mV/dec). Subthreshold slope values fewer than 60 mv/dec have also been seen in previous research studies. Hence the device can be switched quickly over a wide range of current. It can also be observed that as the gate length is reduced the subthreshold value increases.

SS can be expressed as [149]:

$$SS = \frac{\partial V_{gs}}{\partial log_{10} I_d} \tag{3.2}$$

Table 3.4. I_{on}/I_{off} Ratio

Parameter	**L=32nm**		**L=45nm**		**L=90nm**	
	JAM-FE-FET	JL-FE-FET	JAM-FE-FET	JL-FE-FET	JAM-FE-FET	JL-FE-FET
I_{on} (10^{-4})	2.35	2.21	2.09	1.95	1.54	1.43
I_{off} (10^{-10})	6.58	7.96	6.68	8.04	6.9	8.37
I_{on}/I_{off} (10^{4})	35.7	27.7	31.2	24.2	22.3	17.08

For V_{gs}= 1V, Fig. 3.7 (a) depicts the drain current variation with drain voltage. The figure clearly indicates that, similar to JL- FE-FET, in the linear region drain current is almost identical, but in the saturation region, device with shorter gate lengths display greater saturation currents. Fig. 3.7 (b) depicts the output conductance variation for the compared device structures. The output conductance can be calculated by varying the drain current with the

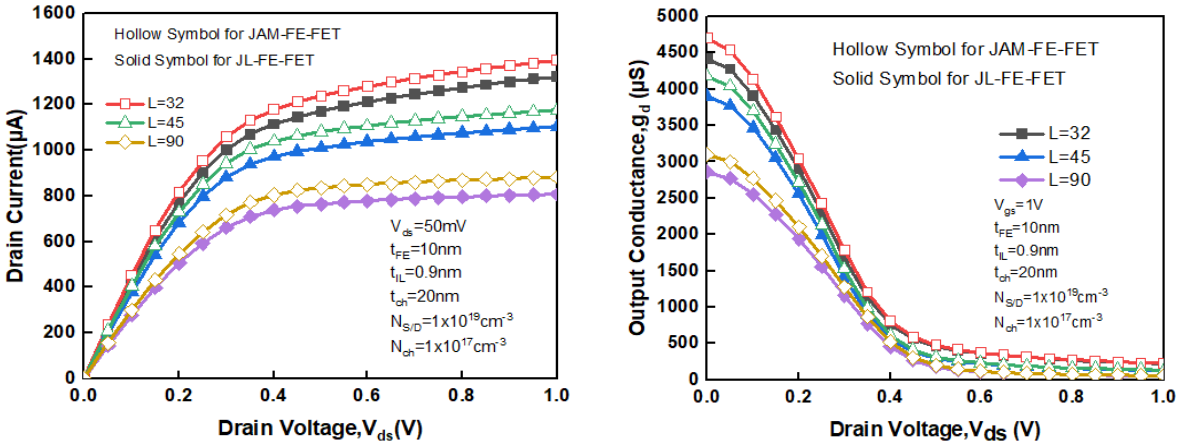


Fig. 3.7. (a) Drain current variation with V_{ds} (b) Output conductance variation with V_{ds}

drain to source voltage while maintaining the constant gate to source voltage. It can be expressed as [150]:

$$g_d = \frac{\partial I_d}{\partial V_{ds}} \tag{3.3}$$

It can be inferred from the figure that g_d is higher in the linear region and keep up a constant value in the saturation region. Thus, the driving capability of the proposed device is greater than the compared one. It can also be assessed from the graph that the output conductance increases when the scaling of channel length is done from 90 nm to 32 nm due to the suppressed short channel effects and the increased gate controllability.

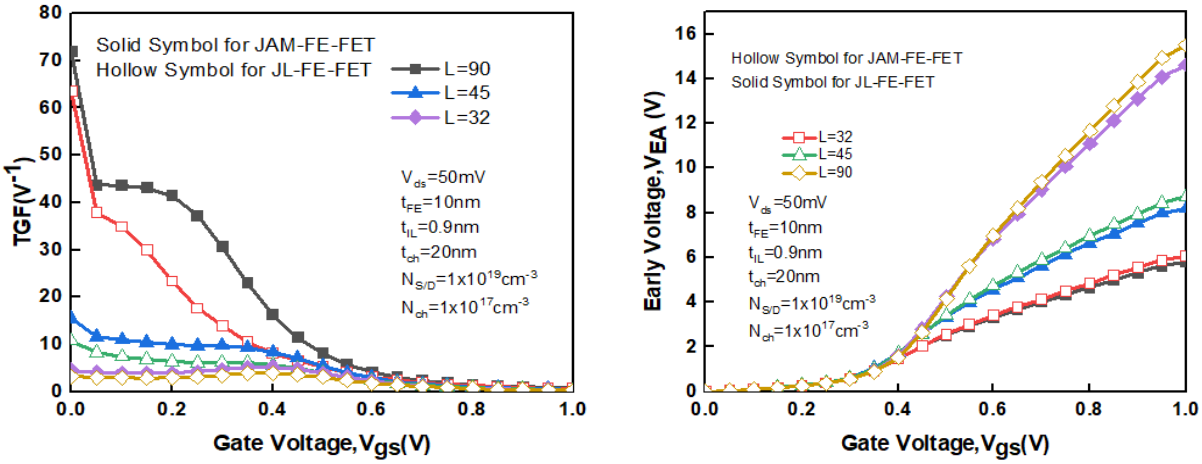


Fig. 3.8. (a) TGF as a function of V_{gs} (b) Early Voltage variation with V_{gs}

Transconductance Generation factor (TGF) can be defined as the accessible gain per unit power loss. It can be expressed as [150]:

$$TGF = \frac{g_m}{I_d} \tag{3.4}$$

The device that operates at lower supply voltage performs better for higher TGF values. It is clearly evident from Fig. 3.8 (a) that the proposed device structure attains the maximum TGF value. Since the drain current is higher, it corresponds to high value of transconductance and eventually high TGF.

Immunity to the channel length modulation (CLM) is provided by Early Voltage (V_{EA}) [151]. Early Voltage is expressed as:

$$V_{EA} = \frac{I_d}{g_d} \tag{3.5}$$

The drain current rise, I_d in JAM-FE-FET is greater than the decrease in transconductance, resulting in a higher V_{EA} than in JL-FE-FET. For varied channel lengths, Fig. 3.8 (b) depicts

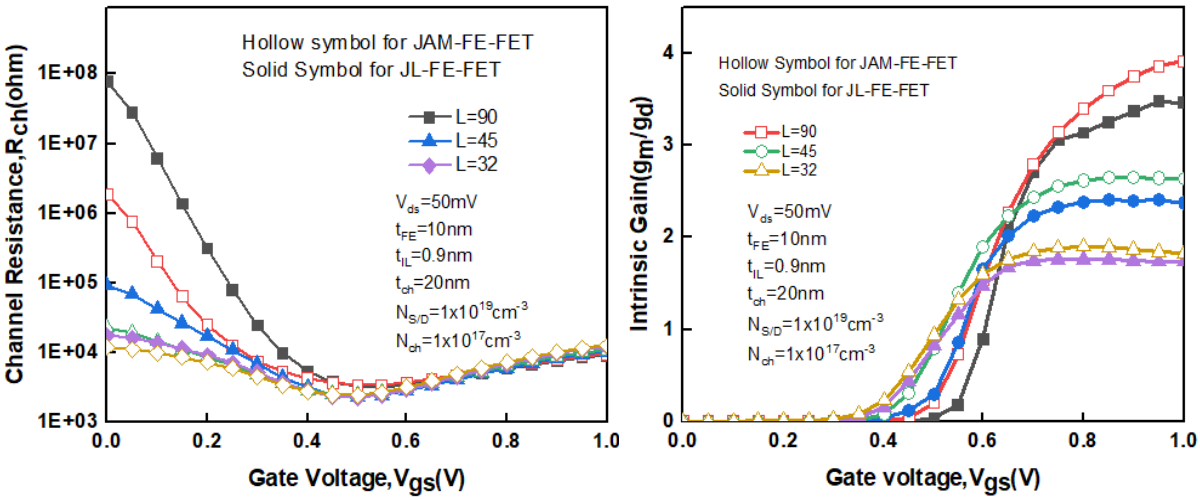


Fig. 3.9. (a) Channel resistance variation with V_{gs} (b) Intrinsic gain variation with V_{gs}

the early voltage shift as a function of gate bias. A greater V_{EA} indicates that the device will have higher gain and can be used in amplifiers [152].

Fig. 3.9 (a) shows the channel resistance variation with the gate voltage. The channel resistance should be minimum for higher driving current. As can be observed from the figure that the JAM-FE-FET exhibits lower channel resistance owing to its increased carrier density and velocity in the channel region.

The next figure of merit is the intrinsic dc gain which can be defined as the transconductance (g_m) to output conductance (g_d) ratio, i.e., g_m/g_d [152]. Since g_d is extracted from static I_d-V_{ds} curve, so it is the low frequency or quasi-static result. It is a critical parameter for practical transconductance amplifiers. The change of g_m/g_d with gate voltage is shown in Fig. 3.9 (b) for L= 32 nm, L= 45 nm and L= 90 nm for the compared devices. It can be observed from Fig. 3.9 (b) that the intrinsic gain is higher at channel length 90 nm because of low output conductance which is essential for analog applications.

The capacitive behavior of a device controls its high frequency functioning. Fig. 3.10 (a) shows how a change in gate bias (V_{gs}) affects total gate capacitance (C_{gg}) in JAM-FE-FET and JL-FE-FET. It can be observed that JAM-FE-FET reveals profiles that are considerably closer to those of JL-FE-FET.

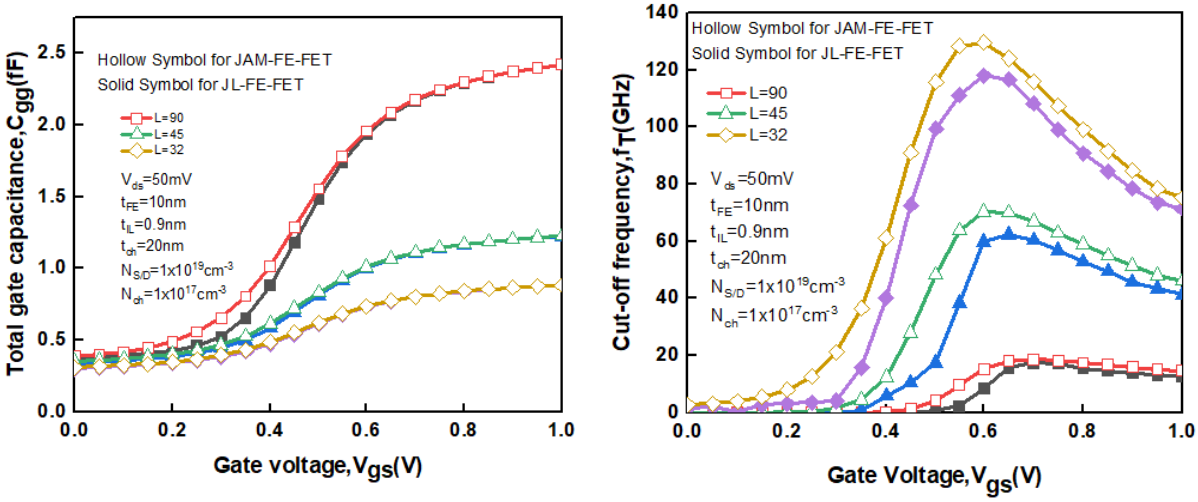


Fig. 3.10. (a) C_{GG} variation with V_{gs} (b) f_T variation with V_{gs}

Cut off frequency denoted as f_T is an intrinsic property of the device and represents a figure of merit for high frequency operation. It can be expressed as:

$$f_T = g_m/2\pi C_{GG} \qquad (3.6)$$

Cut-off frequency for different channel lengths with respect to gate voltage is shown in Fig. 3.10 (b). The high value of cut-off frequency is observed because of high g_m value and comparable C_{gg}. However the cut off frequency further reduces for high gate voltages due to the increase in total gate capacitance.

The transducer power gain (G_T) can be defined as the P_{load} to the P_{source} ratio, where P_{load} is the average power given to the load, and P_{source} is the average power available from the source. It can be expressed as:

$$G_T = \frac{P_{load}}{P_{source}} \qquad (3.7)$$

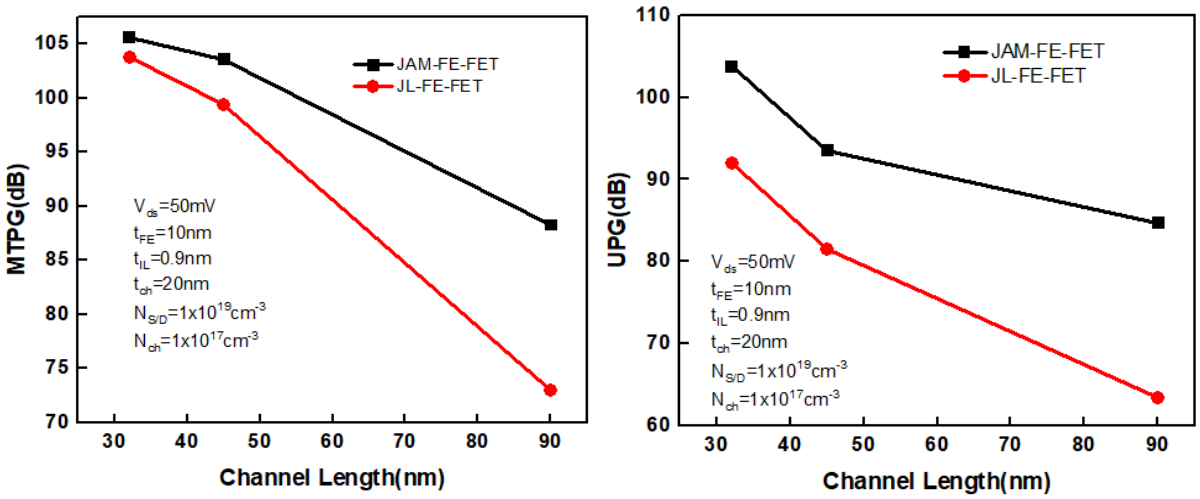


Fig. 3.11. (a) MTPG variation with channel length (b) UPG variation with channel length

Maximum-Transducer-Power-Gain (MTPG) is described as a power gain that can be obtained when load is driven with the identical inputs. The MTPGs for JL-FE-FET and JAM-FE-FET are shown in Fig. 3.11 (a) for channel lengths varying from 30 nm to 90 nm. From the Fig. 3.11 (a), it can be clearly interpreted that JAM-FE-FET has a higher gain owing to its architecture which overcomes the deterioration in mobility. It can also be inferred from the figure that as the channel length is scaled down from 90 nm to 45 nm the transducer gain increases drastically.

Variation in Unilateral Power Gain (UPG) for JAM-FE- FET and JL-FE-FET with respect to V_{gs} is depicted in Fig. 3.11 (b). When the gate bias is applied, the structure generates a larger electric field in addition to enhanced capacitance, resulting in increased electron velocity and therefore superior saturation velocity. As a result, it's reasonable to conclude that JAM-FE-FET has a greater UPG. It can also be inferred from the figure that as the channel length is increased from 45 nm to 90 nm there is a gradual decline in the unilateral power gain. Overall, the JAM-FE-FET possess high UPG.

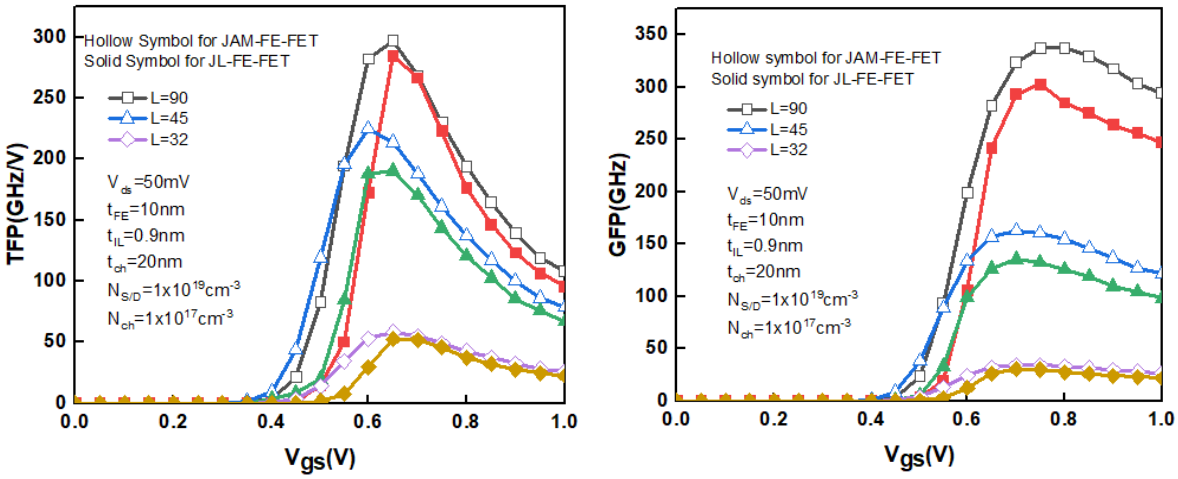


Fig. 3.12. (a) TFP variation with V_{gs} (b) GFP variation with V_{gs}

The total oxide capacitance also explains these trends. A better capacitance matching in Negative Capacitance FET helps in achieving a high oxide capacitance through which a higher TFP can be obtained.

The Gain Frequency Product (GFP) is another performance parameter for high frequency operational amplifier applications. TFP and GFP are expressed as follows:

$$TFP = \frac{g_m f_T}{I_D} \tag{3.8}$$

$$GFP = \frac{g_m}{g_d} \times f_T \tag{3.9}$$

GFP increases with V_{gs} due to increment in f_T and intrinsic gain. The curves begin to decline owing to the charge carriers' saturation mobility, which is what causes parasitic capacitances to exist.

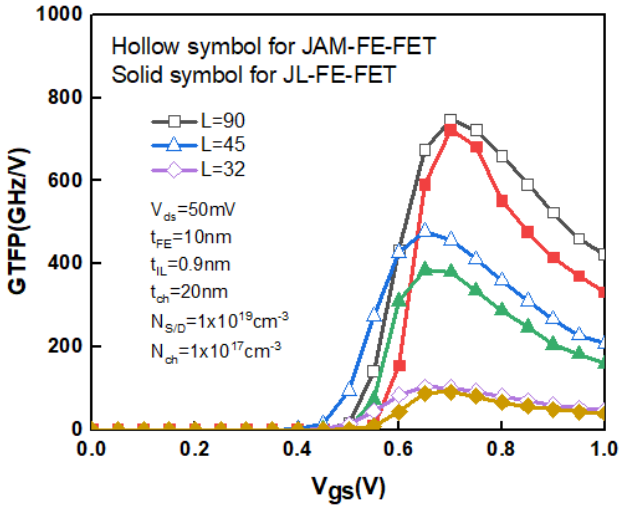


Fig. 3.13. GTFP variation with V_{gs}

Table 3.5. Performance parameters at channel length L = 32 nm

Parameters	JAM-FE-FET	JL-FE-FET	%Improvement
I_d(μA)	235.21	221.11	6.3
g_m(μS)	603.52	564.98	6.82
g_d(μS)	4700	4420	6.33
I_{on}/I_{off}(×10^6)	0.357	0.279	27.95
SS (mV/dec)	54	65	20.37
TGF(V^{-1})	4.54	3.27	38.83
V_{EA}(V)	6.07	5.80	4.65
A_V (dB)	1.82	1.73	5.20
C_{gg}(fF)	0.83	0.82	1.21
f_T (GHz)	124	116	6.89
MTPG (dB)	105.63	103.78	1.78
UPG (dB)	103.79	91.97	12.85
TFP(GHz/V)	58.50	52.52	11.38
GFP(GHz)	34.45	30.31	13.65
GTFP(GHz/V)	101.8	90.88	12.01

Fig. 3.12 (a) and Fig. 3.12 (b) shows the comparison of TFP and GFP of both the device configuration. It can be observed that JAM-FE-FET possess higher values for both parameters. The RF parameter which determines the entire performance of the device is Gain Transconductance Frequency Product (GTFP). It is expressed as:

$$GTFP = \frac{g_m}{g_d} \times \frac{g_m}{I_D} \times f_T \qquad (3.10)$$

Higher the GTFP value, better is the device performance. So, from the Fig. 3.13 it is clear that the proposed device achieves the high GTFP value which indicates better performance. This enhancement is due to the electric field reduction in JAM-FE-FET owing to its gate stack architecture resulting in an improvement of the parameters.

3.5.2 Small Signal parameters

The small signal analysis of both NC-JAM-FET and NC-JL-FET are studied in terms of reflection coefficients (S_{11} and S_{22}), transmission coefficient (S_{12} and S_{21}), total gate

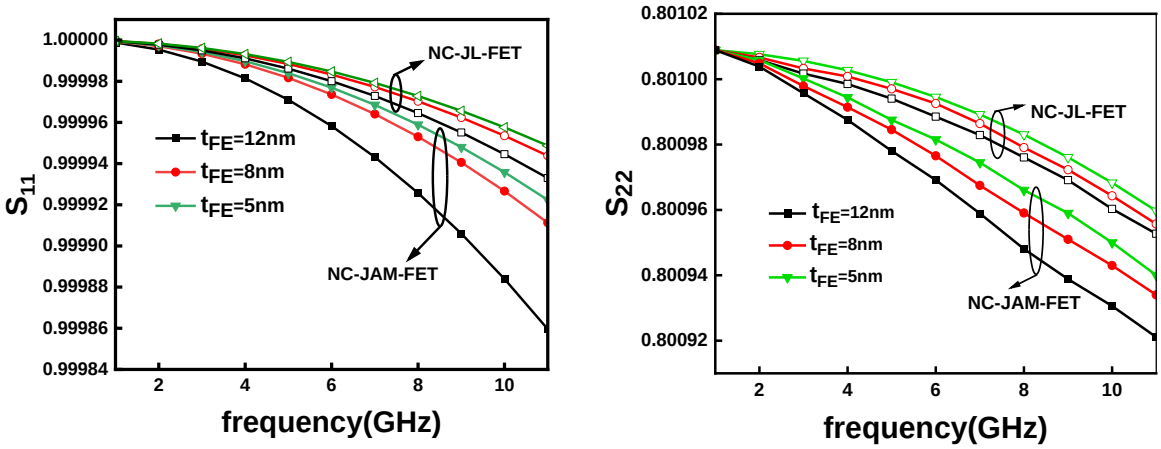


Fig. 3.14. (a) Variation of S_{11} with frequency (b) Variation of S_{22} with frequency

capacitance, cut-off frequency, MTPG, and UPG respectively. Fig. 3.14 (a) shows the reflection coefficient of input port for the compared devices. As observed from the figure that the reflection coefficient for NC-JAM-FET is low when compared to NC-JL-FET. This is due to the fact that JAM-FET provides minimum mobility degradation which further increases the current and thus reducing the reflection coefficient. Low reflection coefficient indicates the minimum data loss.

As seen from the figure that the reflection coefficient also decreases when the ferroelectric thickness for both the devices are increased. Fig. 3.14 (b) shows the reflection coefficient at output port for both the devices. The results are analogous to input reflection coefficient and hence it is minimum for NC-JAM-FET.

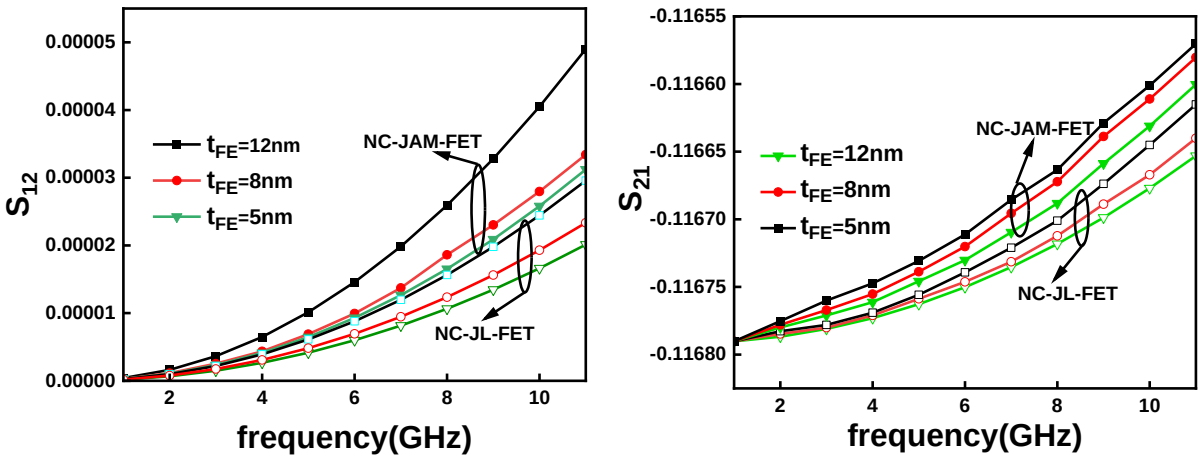


Fig. 3.15. (a) Variation of S_{12} with frequency (b) Variation of S_{21} with frequency

The variation of S_{12} with frequency for the compared devices is shown in Fig. 3.15 (a). It is known as the reverse transmission coefficient. As evident from the figure, the NC-JAM-FET shows higher transmission coefficient due to its enhanced performance in comparison to NC-JL-FET. The variation of S_{21} with frequency at different ferroelectric thickness for both the devices is shown in Fig. 3.15 (b). As observed from figure, S_{21} which represents the forward voltage gain is higher for NC-JAM-FET in comparison to NC-JL-FET. Fig. 3.16 (a) shows the total gate capacitance for both the devices at different ferroelectric thickness. It is found that the CGG is higher for NC-JAM-FET due to the structural difference when compared to NC-JL-FET. JAM provides concentration gradient which reduces the parasitics and improves the performance.

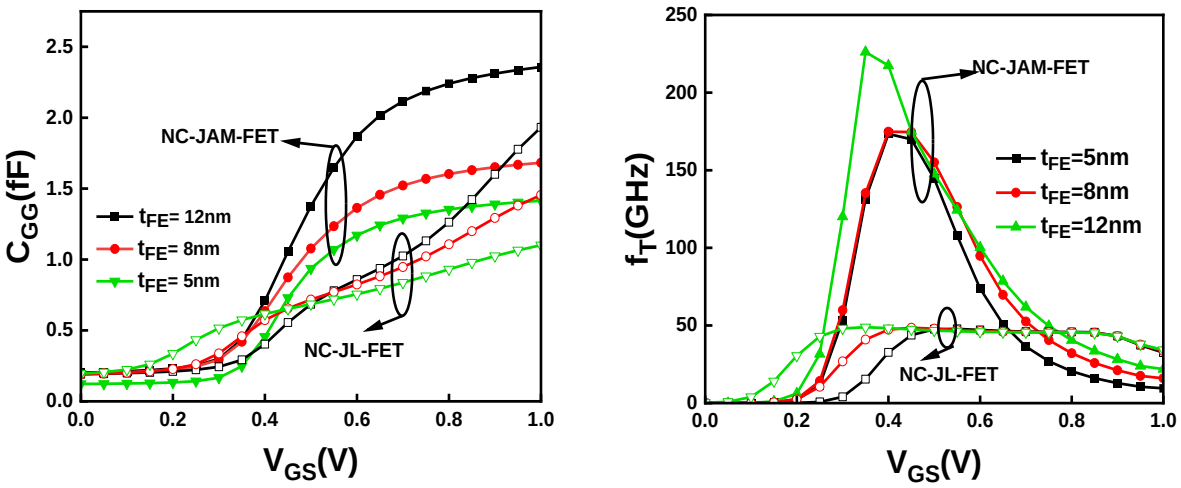


Fig. 3.16 (a) Variation of C_{GG} with V_{GS} (b) Variation of f_T with V_{GS}

Fig. 3.16 (b) shows the cut-off frequency variation with V_{GS} for both the devices. Despite the fact that C_{GG} is higher for NC-JAM-FET, cut-off frequency is high. This is because the transconductance for NC-JAM-FET is also higher and thus improving the frequency behaviour of the device.

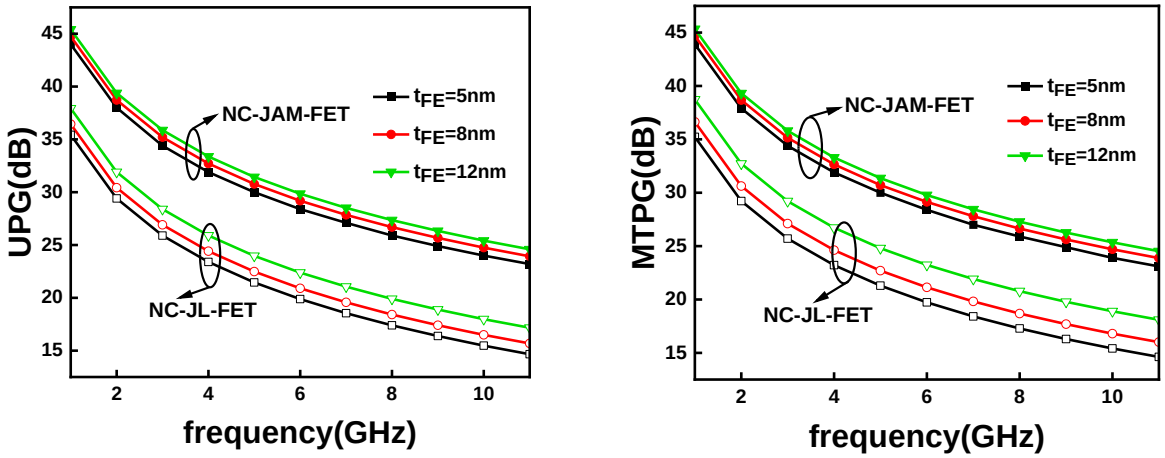


Fig. 3.17. (a) Variation of UPG with frequency (b) Variation of MTPG with frequency

Unilateral Power Gain (UPG) variation with frequency for both NC-JAM-FET and NC-JL-FET is shown in Fig. 8. It is clear from the figure that UPG for NC-JAM-FET is maximum in comparison to NC-JL-FET. This is due to the increased capacitance, which results in higher electron velocity and consequently higher UPG. The variation is also shown in terms of thicknesses of ferroelectric layer. As evident, the performance increases as the ferroelectric

thickness is increased because of negative capacitance effect. Maximum Transducer Power gain (MTPG) variation with frequency of both NC-JAM-FET and NC-JL-FET is shown in Fig. 9. The maximum transducer power gain (MTPG) specifies highest power increase possible when operating the load with similar inputs. As evident from the figure, MTPG for NC-JAM-FET is higher in comparison to NC-JL-FET. The larger gain is due to the structure's ability to withstand mobility deterioration. It can also be observed from the figure that when the ferroelectric thickness increases, the transducer power gain increases.

3.5.3 Temperature variation on DC parameters

This section reveals the influence of temperature fluctuation from 300K to 500K on HZO ferroelectric gate stack in both JAM and JL Ferroelectric FET along with SiO_2 dielectric and silicon channel. Fig. 3.18 (a) shows the influence of temperature on input characteristic of both the devices. It can be seen in this diagram that when the temperature rises, the drain current decreases. Large variation at lower gate voltages has been observed with temperature as compared to the super threshold region. This happens due to the SRH recombination as it has an exponential dependence on temperature.

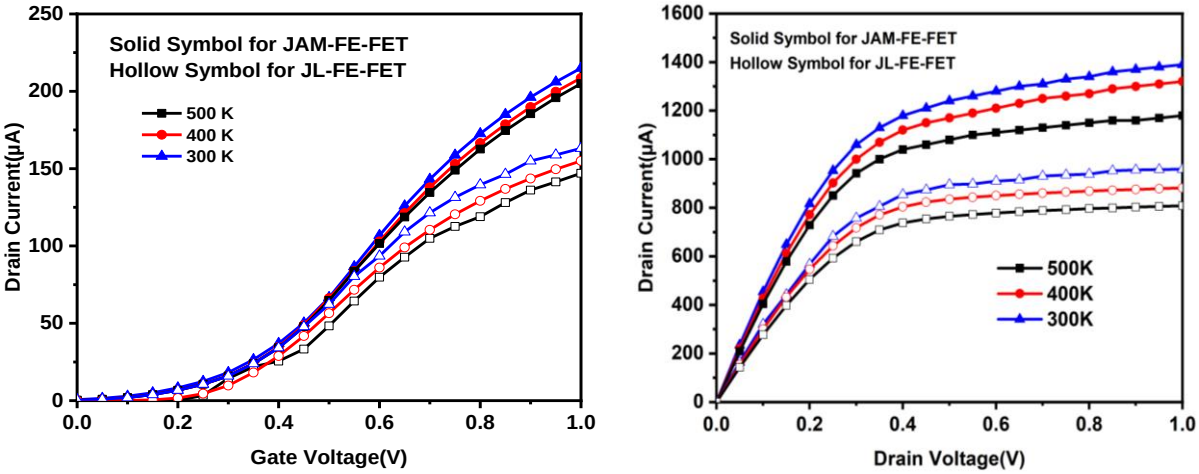


Fig. 3.18 (a) Input characteristics at different temperatures (b) Output characteristics at different temperatures

Fig. 3.18 (b) illustrates the output characteristics of both the device configuration at various temperatures. The figure clearly shows that the rise in drain current with drain voltage at lower temperatures is significant. Additionally, the detailed dc performance characteristics such as threshold voltage, SS, and I_{on}/I_{off} ratio with respect to the temperature is obtained and compared for JAM and JL ferroelectric FET device configurations as in Fig. 3.19, and Fig. 3.20. Fig. 3.19 (a) shows the threshold voltage variation at different temperatures.

It can be assessed from the figure that as the temperature increases, there is a decrease in threshold voltage, thereby showing a positive temperature coefficient due to the variation in the bandgap and fermi level. The change in threshold voltage is around 60mV when the temperature is varied from 300K to 500K. It can also be assessed that the threshold voltage is higher for JAM configuration when compared to JL ferroelectric configuration.

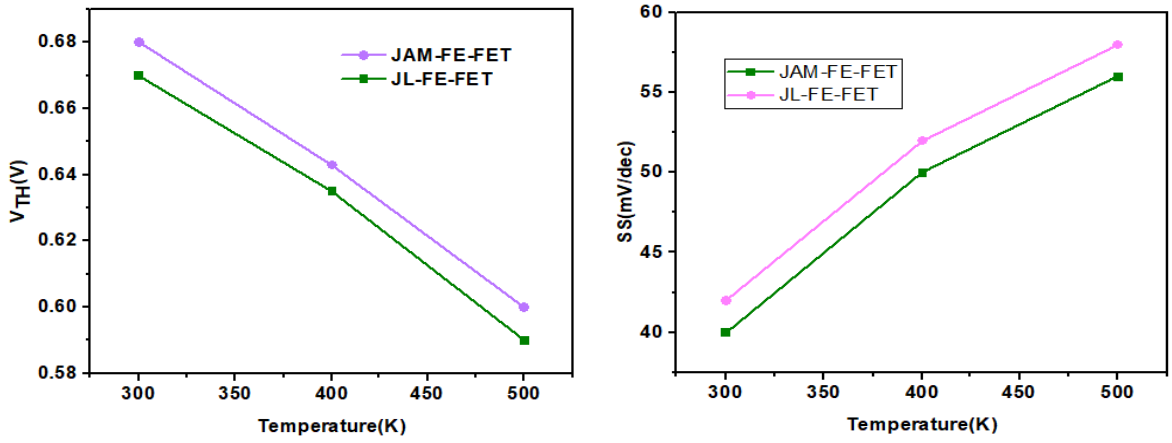


Fig. 3.19. (a) V_{TH} variation at different temperatures (b) SS variation at different temperatures

Fig. 3.19 (b) shows the subthreshold swing (SS) variation with respect to temperature. It can be assessed from the figure that SS increases with rise in temperature since SS is directly proportional to temperature as (SS=kT/q). Therefore, this plot verifies the steeper SS at low temperatures. Moreover, the SS is much steeper for JAM configuration than JL FE-FET configuration.

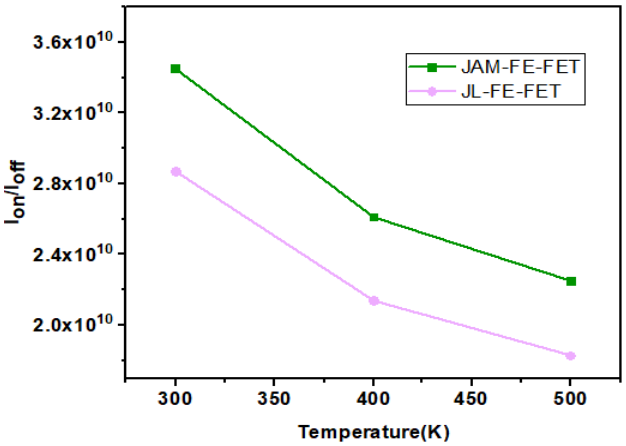


Fig. 3.20 I_{on}/I_{off} variation at different temperatures

Fig. 3.20 represents the variation in Ion/Ioff with respect to temperature. As observed from Fig. 3.20, the I_{on}/I_{off} ratio reduces with an increase in temperature. It is also evident from the figure that the I_{on}/I_{off} ratio is improved for JAM-FE-FET when compared to JL-FE-FET.

3.6 Summary

In this chapter, a simulation-based comparative analysis is done for proposed JAM-FE-FET with JL-FE-FET. The SILVACO ATLAS TCAD simulator was used to test the performance of proposed device in terms of analog and RF characteristics. In terms of switching ratio, the suggested JAM-FE-FET device achieves the best results. In comparison to JL-FE-FET, the subthreshold swing is also lowered by 20.37%. The proposed device's SS improves as a result of the negative capacitance effect in the MFIS structure. The proposed device also shows an improvement in terms of transconductance and TGF by 6.82% and 38.83% respectively. The I_{on}/I_{off} ratio also shows a significant improvement of 27.95% owing to the device architecture which overcomes the mobility degradation in the channel region. Also, the capacitive behavior of the proposed device is in close agreement with the JL-FE-FET. However, the enhanced behavior of transconductance results in high cut-off frequency which is a critical parameter in RF applications. Various RF parameters like f_T, TFP, GFP and GTFP are enhanced by 6.89%,

11.38%, 13.65%, and 12.01% respectively. Therefore, from the above obtained results the proposed JAM-FE-FET can be viewed as a promising device for applications in high frequency systems. A small signal analysis has also been carried out in terms of S-parameters for high frequency RF applications. Small signal parameters like scattering parameters (S_{11}, S_{12}, S_{21}, S_{22}), Gate Capacitance (C_{GG}), cut-off frequency (f_T), Maximum Transducer Power Gain (MTPG), and Unilateral Power Gain (UPG) have been analyzed. The performance analysis have also been done by varying the ferroelectric thickness (t_{FE}=12nm, 8nm, 5nm). It is found that the performance of NC-JAM-FET is better when compared to NC-JL-FET and therefore it can be considered a better candidate for RF applications. Furthermore, a comprehensive analysis of the dc performance dependence on temperature has been carried out for both JAM and JL ferroelectric FET. This research reveals that the highest I_{on}/I_{off} ratio and minimum SS as 3.45×10^{10} and 40 mV/decade have been obtained at 300K for JAM ferroelectric FET respectively. As a result of this investigation, the temperature has a substantial impact on the device's dc properties, making the JAM-FE-FET a viable choice for ultra-low power digital applications.

Chapter 4

Double Gate Junctionless Accumulation Mode Ferroelectric FET: Analytical Study

In previous chapter, a single gate configuration of the proposed device was studied. However, single gate face challenges in achieving precise control over the channel conductivity limiting the ability to turn the transistor fully off and affecting its ability to switch between on and off states effectively resulting in increased power consumption and reduced performance. Hence, to overcome these limitations a double gate configuration is used in this chapter for improved control, enhanced gate efficiency, increased current drive, and design flexibility. Previous chapter also focused on simulation study of the device which is not sufficient to understand the insight physics of the device. Therefore, in this chapter, an analytical drain current model for Double Gate Junctionless Accumulation Mode Negative Capacitance Field Effect Transistor (DG-JAM-NC-FET) has been developed using Poisson's equation and Landau Khalatnikov's (L-K) equation. The drain current is then determined by integrating the mobile charge using Pao–Sah integral. Various critical parameters such as surface potential, gain, capacitance, mobile charge density, drain current, threshold voltage, subthreshold swing, transconductance, and the switching ratio have been assessed extensively by varying ferroelectric layer and channel layer thicknesses, respectively. These parameters have also been analyzed extensively by varying the temperature from 200K to 500K. The analytical modeling is done in MATLAB, and its comparison is made with the TCAD numerical simulation. The obtained analytical results are validated with the numerical simulation results.

4.1. Introduction

Numerous types of research have been extensively investigated to analyze the behavior of FE-FETs, and different topologies have already been developed and researched for a better understanding of the core characteristic of negative capacitance, including metal ferroelectric insulator semiconductor (MFIS), metal ferroelectric metal insulator semiconductor (MFMIS), double gate negative capacitance FET (DGNCFET), double gate ferroelectric Junctionless (DGFJL) transistor and negative capacitance TFET (NCTFET) [153]–[156]. The hysteresis transition at the source end dipole, i.e., the capacitance divider produced thereby ferroelectric and internal MOS capacitances, determines the beginning of hysteresis in MFIS [44]. Various analytical research has also been conducted to assess the NC impact in DGFJL transistors [84], [104]. Several ferroelectric materials like $BaTiO_3$, SBT, PZT, and HZO [63], [157] have been published thus far to demonstrate the NC impact. HZO's compatibility with CMOS technology has made it clear that it is preferable to alternative ferroelectric materials in many circumstances. As discussed in earlier chapters, zirconium-doped hafnium oxide has a very low dielectric constant, a strong coercive field, and strong adhesive features with silicon, which indicates that its scaling can be done to meet the existing technology nodes [158]. Therefore, a comprehensive evaluation of their characteristics is necessary to merge this material into the current CMOS model for a variety of energy-efficient applications.

In the present chapter, an analytical model for the DG-JAM-NC-FET has been reported. The ferroelectric layer, which offers negative capacitance, is integrated with JAM-FET to decrease leakage current and lower subthreshold slope, resulting in high drive current and fast switching. A systematic drain current model for the DG-JAM-NC-FET transistor is developed using the Landau-Khalatnikov theory and the parabolic potential approximation to analyze the device properties. Various device parameters have been calculated using the model, including surface potential, gate capacitance, gain, threshold voltage, mobile charge density, drain

current, subthreshold slope, and switching ratio. This work also discusses the influence of ferroelectric, silicon channel thickness, and temperature on different device parameters. Analytical data are compared to simulated outcomes generated using the TCAD Silvaco ATLAS simulator, which proved the model's reliability.

4.2 Existing Device Topologies

4.2.1 Double Gate structure

Double gate field-effect transistors (FETs) offer several advantages over single gate FETs, providing improved performance and enabling enhanced device characteristics. Some of the key benefits of double gate FETs compared to single gate FETs are improved control and electrostatic integrity, increased gate control efficiency, enhanced current drive and scalability, improved threshold voltage control, and design flexibility. The structural details of double gate have been discussed in details in the previous chapter.

4.2.2 Junctionless Ferroelectric FET

The junctionless ferroelectric FET combines the advantages of junctionless FETs, such as improved electrostatic control and reduced short-channel effects, with the unique characteristics of ferroelectric materials, including negative capacitance. However, some limitations imposed by junctionless transistor, such as low ON current and transconductance, due to carrier mobility degradation, degrade the overall performance of the device. Therefore, JAM ferroelectric FET have been proposed and studied in the previous chapter. To further improve the device performance, a double gate configuration is used with JAM ferroelectric FET in the current chapter.

4.2. Device Structure & Simulation

In this analysis, we have used an n-type doped, symmetric double gate junctionless accumulation mode transistor with HZO as the ferroelectric layer and an insulator layer between the silicon channel and the ferroelectric layer, as shown in Fig. 4.1(a). The

thicknesses of the ferroelectric layer, insulator layer, and channel layer are represented by the symbols t_{FE}, t_{IL}, and t_{CH}, respectively. The device and material parameters used for the simulations are enlisted in Table 4.1. The body of the device is not floating for analytical calculations. The device is implemented on bulk Silicon wafers, modeled systematically, and compared with data obtained from device simulation. Leaving the body floating does complicate device behavior which causes fluctuations in body charge and propagation delay, which do not occur in bulk FETs. The simulations are performed on the Silvaco ATLAS TCAD simulator, with the Lombardi CVT model, Shockley-Read-Hall (SRH) recombination, fermi model, and Landau-Khalatnikov (LK) Ferro models [146]. Landau-Khalatnikov (LK) ferroelectric interface model ATLAS has the ability to model a ferroelectric film as an interface model between a conventional gate insulator and a semiconducting channel. The Landau-Khalatnikov formulation gives a relation between the field and polarization in the layer, resulting in a polarization curve versus the electric field. This particular curve is S-shaped and characterized by Remnant Polarization (P_r) and Coercive Field (E_C).

The setup is simulated on the ATLAS Silvaco simulator by incorporating the models specific to the ferroelectric devices only. The LKFERRO model is enabled on the INTERFACE statement while doing simulations on the ATLAS Silvaco simulator. It is applied to the

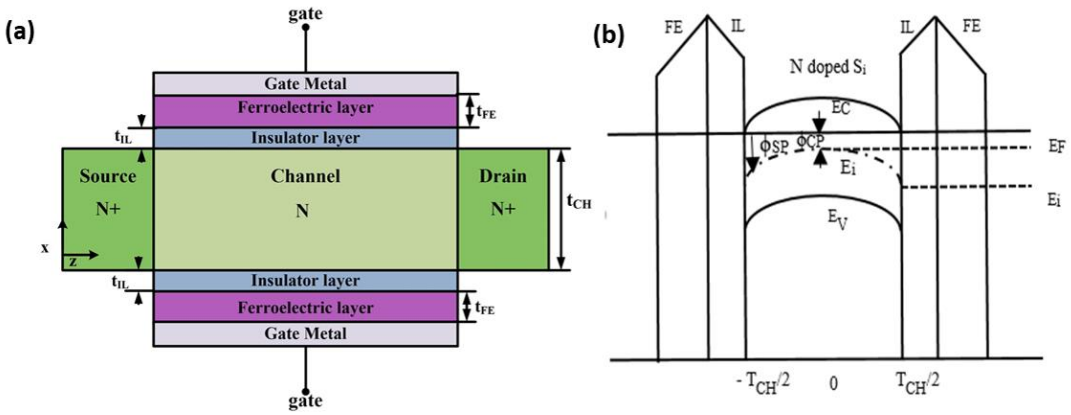


Fig. 4.1. (a) Structure of Double Gate Junctionless Accumulation Mode Negative Capacitance FET (DG-JAM-NC-FET). (b) Schematic of energy bands of the device in NC region towards the direction of the thickness of the channel. The channel bent upward in the accumulation mode.

interface between the channel and the gate oxide. The parameters such as coercive field (E_C) and remnant polarization (P_r) are also set up on the INTERFACE statement with the LKCORECIVE parameter and LKREMNANT parameter. LKNC statement is specified in the MODEL statement to enable the negative capacitance effect.

As we know, the ferroelectric material that we have utilized here has a thickness-dependent remnant polarization, and to achieve the negative capacitance in the device, we have to tune the parametric value mentioned in Table 4.1. Fig. 4.1(b) shows the energy bands of the device in NC region towards the direction of the thickness of the channel. The channel region is n-doped and bent upward in the accumulation mode. ϕ_{SP} and ϕ_{CP} are the surface and center potential, which are calculated analytically. E_i is referenced as the intrinsic Fermi level, while E_C and E_V are the conduction band and valence band, respectively, whose difference gives the energy band gap. This energy gap is further used to determine the work function of silicon.

Table 4.1. Device and Material Parameters

Parameter	**Symbol**	**Values**
Remnant Polarization	Pr	1-40 μC/cm^2
Coercive Field	Ec	1 MV/cm
Landau Parameters	α	-2.5×10^9 *Vm/C*
	β	6.0×10^{10} *Vm/C*
	γ	1.5×10^{11} *Vm/C*
Channel thickness	t_{CH}	8,10,12,15 nm
Ferroelectric thickness	t_{FE}	5,8,10,12 nm
Channel length	L	100 nm
Insulator thickness	t_{IL}	0.8 nm
Metal work function	ϕ_M	4.65 eV

Source/Drain doping	$N_{S/D}$	$1x10^{19}$ cm^{-3}
Channel doping	N_{CH}	$1x10^{17}cm^{-3}$ (n-type)

Quantum Mechanical effects play an essential role in the transport properties of nanoscale MOSFETs. It has been reported that threshold voltage increases by surface quantization in bulk MOSFET with high impurity concentration or by quantum confinement in an ultra-thin channel [159]. In ultra-narrow MOSFETs, threshold voltage depends on channel width because horizontal carrier confinement occurs in a narrower channel. This channel width dependency of threshold voltage by quantum confinement is referred to as the quantum mechanical narrow channel effect. It has been shown in [160], [161] that quantum confinement will enhance the channel potential barrier and increase the threshold voltage when the channel width is chosen to be less than 8 nm. We have neglected the quantum confinement in our work because the channel thickness is considered greater than 5 nm.

4.3. Calibration & Fabrication Feasibility

Devices based on ferroelectric insulators are easier to fabricate, with important fabrication processes being phosphorous implantation to generate the channel and source/drain areas, accompanied by quick thermal annealing that enables dopant activation. Using atomic layer deposition (ALD), a doped ferroelectric layer is formed, followed by the deposition of a metal gate using physical vapor deposition (PVD), and then ferroelectric films can be crystallized after metal annealing.

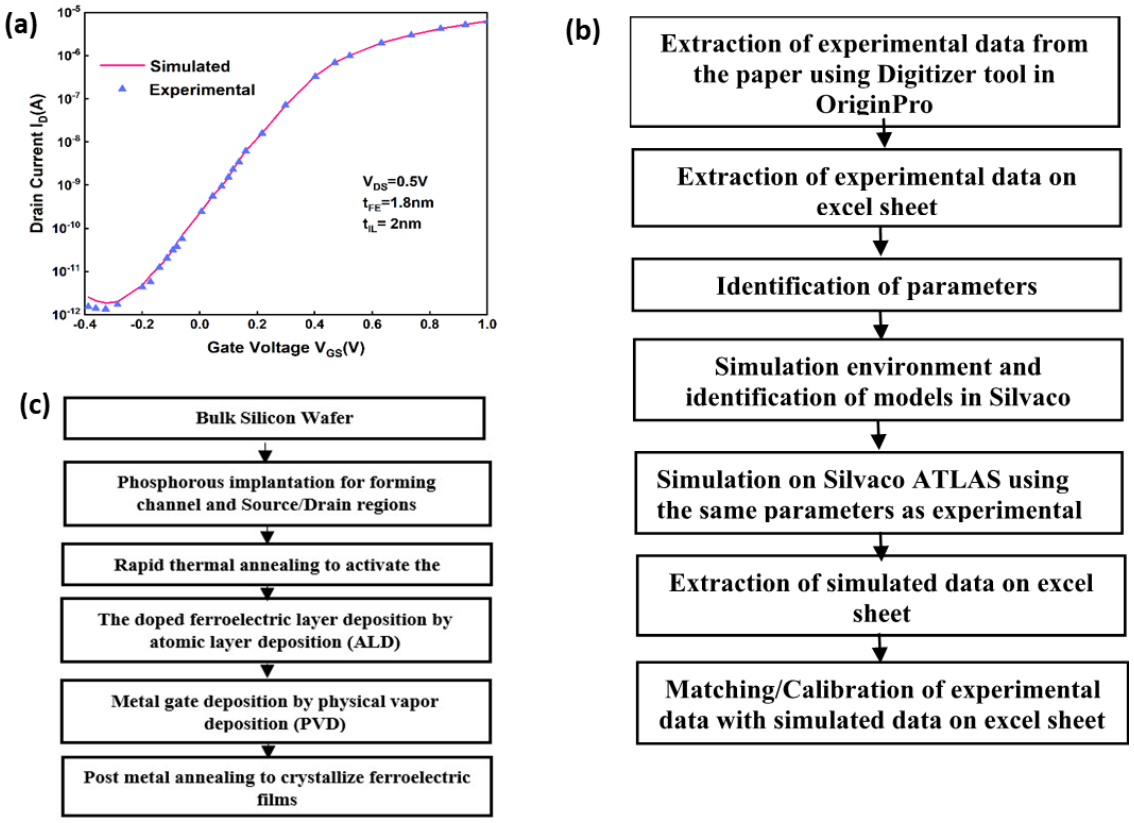


Fig. 4.2. (a) Calibration of transfer characteristics of simulated data with experimental (b) Calibration process flow and (c) Fabrication flowchart for the proposed device.

These fabrication techniques for ferroelectric-based devices have been experimentally proven [162]. The experimental research on ferroelectrics with identical dimensions is used to calibrate this work properly, as shown in Fig. 4.2 (a) [65]. The calibration process has been explained through the flowchart, as shown in Fig. 4.2 (b). No tuning parameters have been used in the calibration. The fabrication steps are shown by a flowchart in Fig. 4.2 (c). The contour plots for potential and electron concentration are illustrated in Fig. 4.3 (a) and (b), respectively, for different ferroelectric thicknesses. As evident, the voltage amplification grows as the ferroelectric layer thickness increases, which is the characteristic of the negative capacitance effect.

It can be interpreted from Fig. 4.3 (b) that the electron concentration in the channel increases as we increase the ferroelectric thickness. Therefore, in DG-JAM-NC-FET, surface conduction occurs under a high electric field. Due to this conduction, the varying depletion capacitance effectively matches ferroelectric and internal capacitance, reducing the hysteresis. Thus, this JAM-based ferroelectric structure solves the major issue of hysteresis in such FE-FETs [163][164].

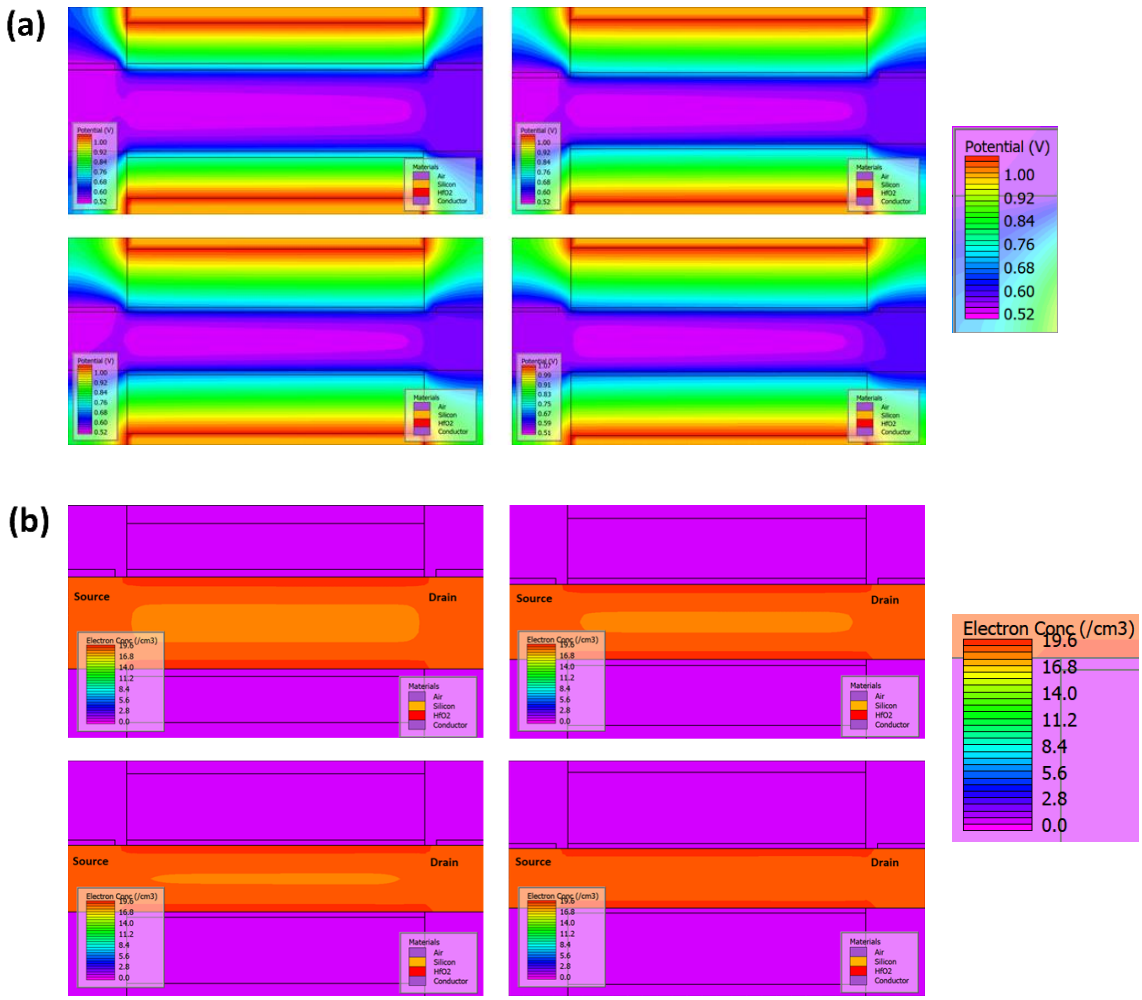


Fig. 4.3. Contour plots for (a) potential and (b) electron concentration at various ferroelectric thicknesses (t_{FE}= 5, 8, 10, 12 nm).

4.4. Model

4.4.1. Surface potential & threshold voltage

With the aid of Pao–Sah gradual channel approximation [165] and only mobile charges, the Poisson equation in the channel region is expressed as:

$$\frac{\partial^2 \phi}{\partial x^2} = \frac{-qN_D}{\varepsilon_{si}}\left(1 - e^{\left(\frac{\phi - V}{V_T}\right)}\right) \tag{4.1}$$

where ϕ is the electrostatic channel potential, N_D is the channel doping concentration, ε_{si} is the silicon permittivity, q is the electronic charge, V_T is the thermal voltage, and V is the electron quasi-Fermi potential.

The parabolic potential approximation is employed to obtain an expression for the channel potential [166], [155]. So, the following expression represents the channel potential:

$$\phi(x) = (\phi_{SP} - \phi_{CP})\left(\frac{4x^2}{t_{CH}^2}\right) + \phi_{CP} \tag{4.2}$$

$\phi(x)$ is the channel potential which satisfies the 1D Poisson's equation under parabolic potential approximation. The parabolic approximation is obtained by using a principle axis and neglecting the other axis. Here, the dependency of the channel potential along the horizontal axis is neglected. ϕ_{SP} and ϕ_{CP} represent the surface potential and the center potential. The following boundary conditions are used to obtain the surface potential and center potential:

$$\phi(0) = \phi_{CP} \tag{4.3}$$

$$\left.\frac{d\phi}{dx}\right|_{x=0} = 0 \tag{4.4}$$

$$\phi\left(\frac{t_{CH}}{2}\right) = \phi_{SP} \tag{4.5}$$

$$\left.\frac{d\phi}{dx}\right|_{x=\frac{t_{CH}}{2}} = \frac{4(\phi_{SP} - \phi_{CP})}{t_{CH}} \tag{4.6}$$

To determine the relationships among ϕ_{SP} and ϕ_{CP} and the gate to source voltage (V_{GS}), a boundary condition and Gauss's law are used at the interface as follows:

$$C_{TOT}(V_{GS} - V_{FB} - \phi_{SP}) = \frac{4\varepsilon_{si}}{t_{CH}}(\phi_{SP} - \phi_{CP}) \tag{4.7}$$

where

$$C_{TOT} = \frac{\varepsilon_{FE}\varepsilon_{IL}}{(t_{FE}\varepsilon_{IL} + \varepsilon_{FE}t_{IL})} \tag{4.8}$$

$$V_{FB} = \phi_M - \phi_{si} \tag{4.9}$$

Here C_{TOT} is the equivalent gate dielectric layer capacitance per unit area, V_{FB} is the flat band voltage, ε_{FE} is the ferroelectric material permittivity, $\varepsilon_{IL}$is the insulator layer permittivity, and ϕ_M is the metal work function. Since the source/drain portions of JAM-FETs have high doping concentrations than the channel region, a built-in potential *(ϕ_{bi})* exists at the source-channel and channel-drain interfaces and is expressed as:

$$\phi_{bi} = \frac{kT}{q} ln \frac{N_D^+}{N_D} \tag{4.10}$$

$$\phi_{si} = \chi + \frac{E_g}{2} - \phi_{bi} \tag{4.11}$$

Where N_D^+ is the doping concentration in S/D regions, ϕ_{si} denotes the silicon's work function, *k* is the Boltzmann constant, χ is the electron affinity of the semiconductor. It is one of the most important parameters of semiconductors, which plays an essential role in functional properties and device performance once interfaces or junctions are involved, for example, metal-semiconductor junctions in devices. E_g is the energy band gap. In equation (4.7), there are two unknowns ϕ_{SP} and ϕ_{CP} therefore, another equation between ϕ_{SP} and ϕ_{CP} is needed to obtain a solution. By integrating equation (4.1) twice, the electrostatic channel potential along the x-axis at any arbitrary point may be derived and stated as follows:

$$\phi - \phi_{CP} = \frac{-qN_D}{\varepsilon_{si}} \int_0^x \int_0^n \left(1 - e^{\left(\frac{\phi - V}{V_T}\right)}\right) dmdn \tag{4.12}$$

m and *n* represent the intermediate integral variables. These variables have been used to calculate the electrostatic potential at any arbitrary position along the channel thickness. Therefore, by considering the boundary conditions $\phi\left(\frac{t_{CH}}{2}\right) = \phi_{SP}\ and\ \phi(0) = \phi_{CP}$, equation (4.12) can be reformulated and get another equation between ϕ_{SP} and ϕ_{CP} as follows:

$$\phi_{SP} - \phi_{CP} = \frac{qN_D}{\varepsilon_{si}}\left(Ae^{\left(\frac{\phi_{CP}}{V_T}\right)} - \frac{t_{CH}^2}{8}\right) \tag{4.13}$$

where

$$A = e^{\left(\frac{-V}{V_T}\right)} \int_0^{\frac{t_{CH}}{2}} \int_0^n e^{\left(\frac{\phi_{SP}-\phi_{CP}}{V_T}\right)} dmdn \tag{4.14}$$

To solve equation (4.14), the difference between the surface and the center potential is assumed as constant [167]:

$$\phi_{SP} - \phi_{CP} = \frac{q}{\varepsilon_{si}} \frac{N_D}{2} \left(\frac{t_{CH}}{2}\right)^2 \tag{4.15}$$

Therefore, equation (4.14) can be evaluated as follows:

$$A = e^{\left(\frac{-V}{V_T}\right)} \int_0^{\frac{t_{CH}}{2}} e^{\left(\frac{\phi_{SP}-\phi_{CP}}{V_T}\right)} (m)_0^n \, dn \tag{4.15a}$$

$$= e^{\left(\frac{-V}{V_T}\right)} \int_0^{\frac{t_{CH}}{2}} e^{\left(\frac{\phi_{SP}-\phi_{CP}}{V_T}\right)} (n) \, dn \tag{4.15b}$$

$$= e^{\left(\frac{-V}{V_T}\right)} e^{\left(\frac{\phi_{SP}-\phi_{CP}}{V_T}\right)} \left(\frac{n^2}{2}\right)_0^{\frac{t_{CH}}{2}} \tag{4.15c}$$

$$A = e^{\left(\frac{-V}{V_T}\right)} N_D e^{\left(\frac{\phi_{SP}-\phi_{CP}}{V_T}\right)} \left(\frac{t_{CH}^2}{8}\right) \tag{4.16}$$

Substituting equations (4.15) and (4.16) in the right-hand side of equation (4.13) we get the second coupling equation between ϕ_{SP} and ϕ_{CP} as:

$$\phi_{SP} - \phi_{CP} = ae^{\left(\frac{\phi_{CP}}{V_T}\right)} + b \tag{4.17}$$

where

$$a = \frac{qN_D t_{CH}^2}{8\varepsilon_{Si}} e^{\left(\frac{\frac{qN_D t_{CH}^2}{8\varepsilon_{Si}} - V}{V_T}\right)}, b = -\frac{qN_D t_{CH}^2}{8\varepsilon_{Si}}$$

Now, the total charge density *(Q_{TOT})* over the entire channel can be determined by integrating it twice and expressed as follows [166]:

$$Q_{TOT} = qN_D t_{CH} - qN_D \int_{\frac{-t_{CH}}{2}}^{\frac{+t_{CH}}{2}} e^{\frac{(\phi(x)-V)}{V_T}} dx \tag{4.18}$$

$$Q_{TOT} = qN_D t_{CH} \left[1 - \left(\frac{e^{\frac{(\phi_{CP}-V)}{V_T}}}{2} \sqrt{\frac{\pi V_T}{\phi_{CP} - \phi_{SP}}}\right)\right] \tag{4.19}$$

The total gate voltage is expressed as the summation of drop across the insulator layer *(V_{IL})*, ferroelectric layer *(V_{FE})*, flat band voltage *(V_{FB})*, and surface potential as given below:

$$V_{GS} = V_{FE} + V_{IL} + V_{FB} + \phi_{SP} \tag{4.20}$$

where,

$$V_{IL} = \frac{Q_{TOT}}{C_{IL}}, C_{IL} = \frac{\varepsilon_{IL}}{t_{IL}}$$

To integrate the negative capacitance offered by the ferroelectric layer, V_{FE} is calculated by using Landau-Khalatnikov (LK) equation as follows:

$$V_{FE} = 2\alpha t_{FE} Q_{TOT} + 4\beta t_{FE} Q_{TOT}^3 + 6\gamma t_{FE} Q_{TOT}^5 \tag{4.21}$$

Here *α, β,* and *γ* are the material parameters determined by the equations using the material properties given in ref. [97]. The values of these parameters are mentioned in Table 4.1.

On solving equations (4.20) and (4.21), we get the following expression:

$$V_{GS} - V_{FB} - \phi_{SP} = \frac{Q_{TOT}}{C_{IL}} + 2\alpha t_{FE}\frac{Q_{TOT}}{2} + 4\beta t_{FE}\left(\frac{Q_{TOT}}{2}\right)^3 + 6\gamma t_{FE}\left(\frac{Q_{TOT}}{2}\right)^5 \quad (4.22)$$

Therefore, surface potential can now be determined by solving equations (4.7) and (4.22) simultaneously. To obtain the threshold voltage, a fully depleted channel is assumed, and ϕ_{CP} is approximated to zero in equation (4.19). Therefore, the expression for charge density is given as:

$$Q_{TH} = qN_D t_{CH}\left(1 - \frac{1}{2}\sqrt{\frac{\pi V_T}{-\phi_{SP}}}\right) \quad (4.23)$$

Similarly, from equation (4.16), ϕ_{SP}can be evaluated as:

$$\phi_{SP} = \frac{qN_D t_{CH}^2}{8\varepsilon_{si}} \quad (4.24)$$

Now, substituting equations (4.23) and (4.24) in (4.22), the threshold voltage can be obtained as follows:

$$V_{TH} = V_{FB} + \frac{qN_D t_{CH}^2}{8\varepsilon_{si}} + \left(\frac{1}{C_{IL}} + \alpha t_{FE}\right)Q_{TH} + 4\beta t_{FE}\left(\frac{Q_{TH}}{2}\right)^3 + 6\gamma t_{FE}\left(\frac{Q_{TH}}{2}\right)^5 \quad (4.25)$$

4.4.2. Drain current model

The expression for the mobile charge (Q_{MOB}) in the channel can be derived by substituting $\phi_{CP} - \phi_{SP} = \frac{t_{CH}}{8\varepsilon_{si}}(Q_{MOB} + qN_D t_{CH})$ [155] and $Q_{TOT} = (Q_{MOB} + qN_D t_{CH})$ along with simple mathematical computations of equations (4.19) and (4.22) as:

$$V_{GS} - V_{FB} - V + \frac{t_{CH}}{8\varepsilon_{si}}(Q_{MOB} + qN_D t_{CH}) + V_T\, ln\left(Q_{MOB}\sqrt{\frac{(Q_{MOB} + qN_D t_{CH})}{2\varepsilon_{si}\pi V_T q^2 N_D^2 t_{CH}}}\right)$$
$$= \left(\alpha t_{FE} + \frac{1}{C_{IL}}\right)(Q_{MOB} + qN_D t_{CH}) + 4\beta t_{FE}\left(\frac{Q_{MOB} + qN_D t_{CH}}{2}\right)^3$$
$$+ 6\gamma t_{FE}\left(\frac{Q_{MOB} + qN_D t_{CH}}{2}\right)^5 \quad (4.26)$$

Now, this mobile charge model is used to derive the drain current (I_D) expression. It is evaluated by using the Pao-Sah integral and integrating Q_{MOB} from source to drain as follows [168]:

$$I_D = -\mu \frac{W}{L} \int_0^{V_{DS}} Q_{MOB}\, dV = -\mu \frac{W}{L} \int_{Q_{MOBS}}^{Q_{MOBD}} Q_{MOB}\, dV \tag{4.27}$$

$$I_D = -\mu \frac{W}{L} \left[\frac{qN_D t_{CH}}{2} ln(\, Q_{MOB} + qN_D t_{CH}) - \frac{\alpha t_{FE} Q_{MOB}^2}{2} - 3\beta t_{FE}^2 Q_{MOB}^2 \left\{ \frac{Q_{MOB}^2}{8} + \frac{Q_{MOB} N_D q t_{CH}}{2} + \left(\frac{N_D q t_{CH}}{2} \right)^2 \right\} - \frac{Q_{MOB}}{2} \left(3V_T - \frac{Q_{MOB} t_{CH}}{8\varepsilon_{si}} + \frac{Q_{MOB} t_{CH}}{2\varepsilon_{IL}} \right) \right]_{Q_{MOBS}}^{Q_{MOBD}} \tag{4.28}$$

Here, Q_{MOBS} and Q_{MOBD} are obtained from (4.26) for $V=0$ and $V=V_{DS}$, respectively.

4.4.3. Gain, transconductance & subthreshold swing

The gain of this device is determined by taking the differentiation of surface potential [103].

$$gain = \frac{d\phi_{SP}}{dV_{GS}} \tag{4.29}$$

Transconductance is the rate of change of drain current to the gate voltage with constant drain voltage and can be expressed as follows [169]:

$$g_m = \frac{dI_D}{dV_{GS}} \tag{4.30}$$

Subthreshold swing (SS) is the alteration in the gate voltage for each decade of change of drain current and is given as [52]:

$$SS = \frac{\partial V_{GS}}{\partial\, log_{10}\, I_D} \tag{4.31}$$

4.5. Model Validation & Discussion

4.5.1 Impact of ferroelectric thickness and channel thickness on device parameters

Fig. 4.4 shows the validation of the proposed model against the reported work on NCFET [84]. The drain current is the most crucial parameter for any device because all other parameters are derived using this parameter. Here, both devices are varied for the same value of ferroelectric thickness. As observed, the proposed work shows an improvement in transfer characteristics as compared to the reported work [84]. Numerical simulations using the Silvaco ATLAS TCAD tool were used to validate the analytical model.

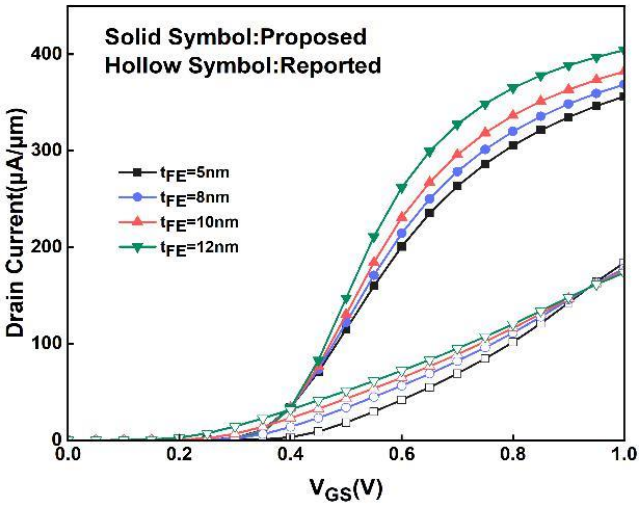


Fig. 4.4. A comparison of the transfer characteristics as reported in Ref. [23] with the results of the proposed model.

The surface potential variation with gate voltage for various values of tFE and tCH are plotted in Fig. 4.5 (a) and (b), respectively, to evaluate the step-up conversion abilities of the device [170]. It is obtained for the given channel length (L=100 nm). The plot has been obtained by solving equations (4.7) and (4.22) simultaneously. As shown in Fig. 4.5 (a) and (b), a peak in the surface potential of the DG-JAM-NC-FET indicates its voltage amplification capability because of the negative capacitance provided by the ferroelectric layer, demonstrating the

suitability of the device for extremely low-power applications. The NCFET operates on the principle of internal gate voltage amplification, which is more prominent than conventional FET. Voltage amplification is due to the nonlinearity nature of the ferroelectric materials and alteration in charge carriers due to ferroelectric voltage present in NCFET. Due to this, overall voltage decreases, and voltage amplification is obtained.

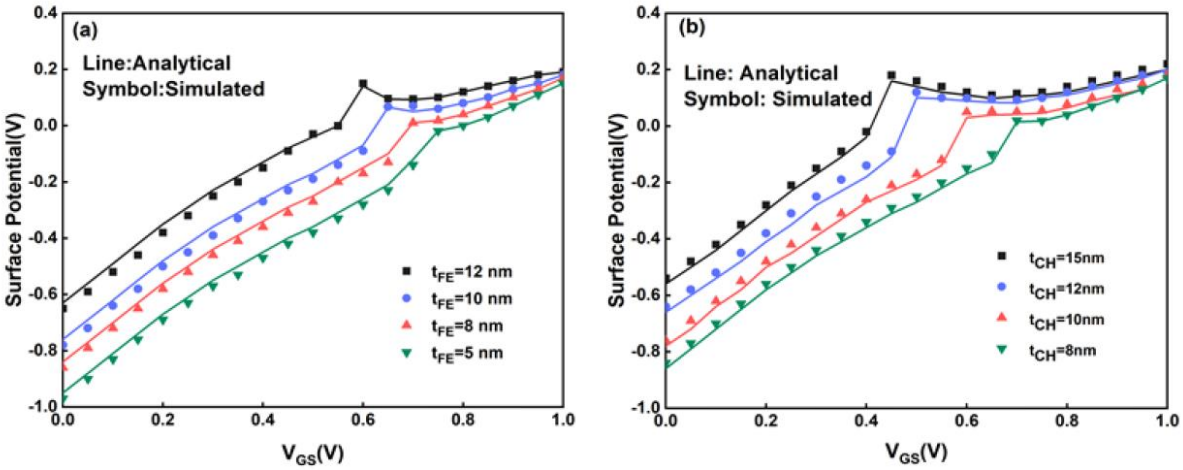


Fig. 4.5. Surface potential of DG-JAM-NC-FET with respect to gate voltage for different (a) ferroelectric thicknesses and (b) channel thicknesses compared with simulated results.

Also, the hysteretic behavior of the device decreases as the t_{FE} decreases, meaning that the step-up conversion capacity diminishes at low t_{FE} levels [84]. The gate capacitance variation with the gate voltage for various ferroelectric thickness values is demonstrated in Fig. 4.6 (a). As observed, there is a peak in the capacitance curve, which displays negative capacitance characteristic manifested by ferroelectric material in a limited range of voltage, which changes the device's total capacitance in a manner that a peak amplitude is observed, resulting in substantial gain and steep subthreshold slope, and hence the switching characteristic of the device is improved. As a result, it is clear that appropriately tuning t_{FE} in FE-FETs is critical for obtaining high gain and low hysteresis. The gate capacitance variation with different channel thicknesses t_{CH} is shown in Fig. 4.6 (b).

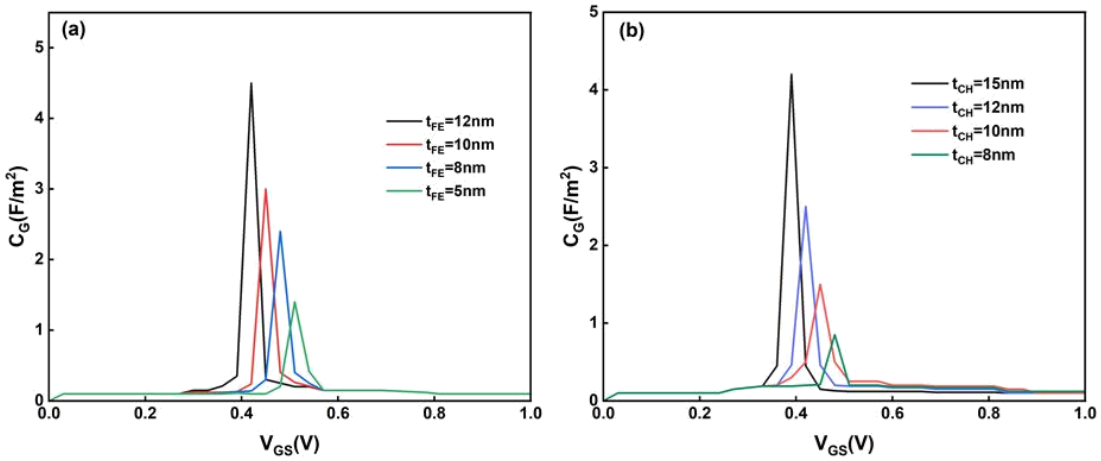


Fig. 4.6. Gate capacitance against gate voltage for various (a) thicknesses of ferroelectric layer and (b) silicon channel thicknesses of the model.

For a given V_{GS}, the total charge through the channel from source to drain is approximately proportional to the gate capacitance ($Q_{TOT} = C_G V_{GS}$). The total gate capacitance (C_G) is the sum of ferroelectric (C_{FE}), insulator (C_{IL}), and semiconductor (C_{SC}) capacitances [103] and is expressed as follows:

$$\frac{1}{C_G} = \frac{1}{C_{FE}} + \frac{1}{C_{IL}} + \frac{1}{C_{SC}} \tag{4.32}$$

Therefore, it is discovered that a narrower channel thickness increases the device's depletion capacitance, lowering total gate capacitance and reducing the influence of negative capacitance on the device performance, which results in lower gain values. As a result, the device's conversion capability can be improved by fine-tuning various device settings.

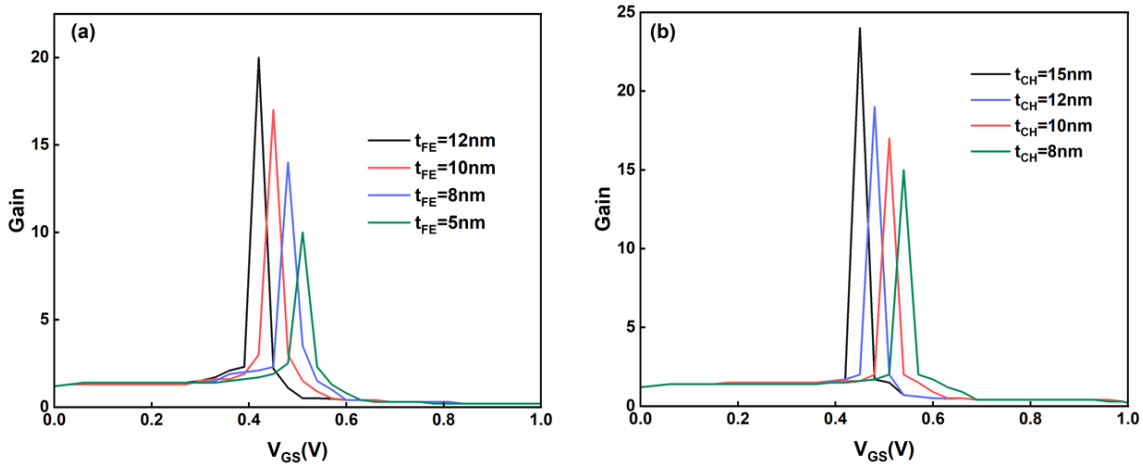


Fig. 4.7. Gain ($d\phi_{sp}/dv_{gs}$) variation with gate voltage at different (a) ferroelectric layer thicknesses and (b)

The gain variation with gate voltage at various ferroelectric and channel thicknesses for analytical data is depicted in Fig. 4.7 (a) and (b), respectively. The gain curve is obtained from equation (4.29). As observed, the gain is greater than 1 at different t_{FE} values, which signifies that this device can act as a step-up transformer. Here the gain is greater than 1, which indicates that the surface potential gets amplified when the device is operating in the

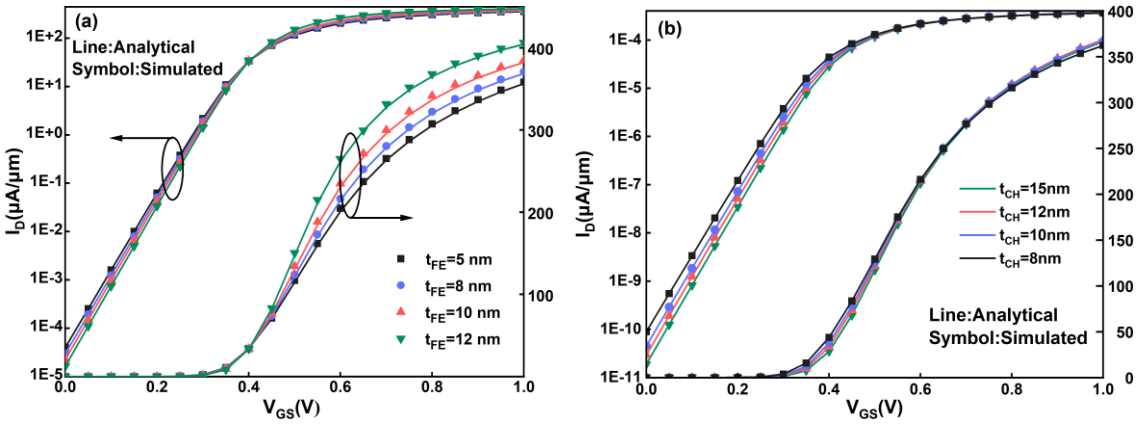


Fig. 4.8. (a) Transfer characteristics of the model at different ferroelectric layer thicknesses and (b) transfer characteristics of the model at different silicon channel thicknesses, compared with simulated data in both logarithmic (primary axis) and linear scale (secondary axis).

negative capacitance region.

When we decrease the thicknesses of these layers, the total gate capacitance increases, as evident from equation (4.8), which in turn reduces the gain and I_{on} of the device; hence, the

threshold voltage is increased. The reason is the increased gate control over the channel, and thus, the gain plot shifts left. If we further increase the thickness of these layers, the hysteretic behavior will increase.

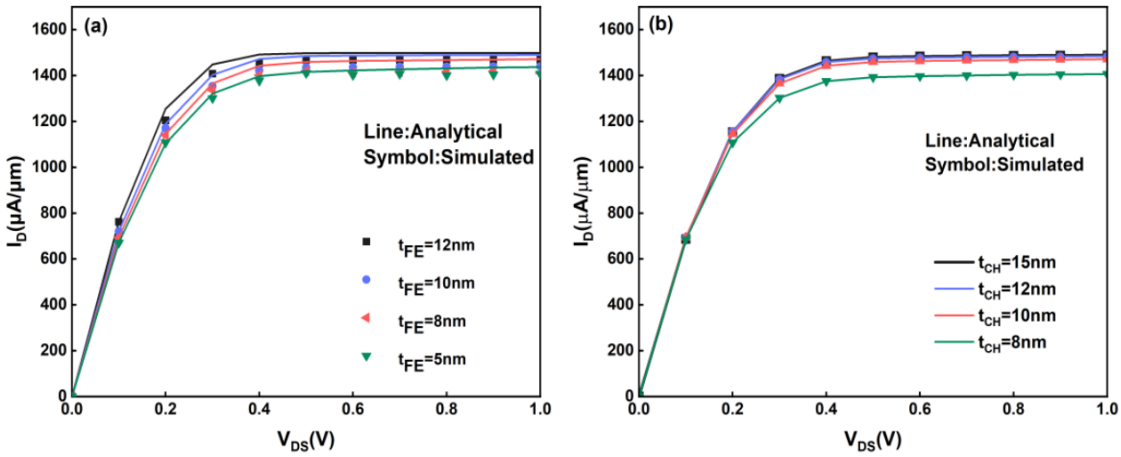


Fig. 4.9. Output characteristics of the model at different (a) ferroelectric layer thicknesses and (b) channel thicknesses, compared with simulated data.

In ferroelectric FETs, it is crucial to properly tune the thickness of the ferroelectric layer to obtain high gain and minimum hysteresis. As a general rule, the high ferroelectric layer thickness values give rise to hysteretic behavior. The thickness of the ferroelectric insulator to be less than a critical thickness defined as [16]:

$$t_{FE} \leq \frac{1}{2\alpha C_{SC}} \equiv t_C \tag{4.33}$$

This condition ensures that the ferroelectric capacitance is large enough (or the semiconductor capacitance CSC is small enough that the combination forms a stable positive capacitor, which corresponds to a very thick ferroelectric, and there is no hysteresis. Here, 12nm is taken as the critical thickness, and so we have neglected the hysteretic behavior. The transfer characteristics of the DG-JAM-NC-FET for various ferroelectric layer thicknesses and channel thicknesses are shown in Fig. 4.8 (a) and (b), which are obtained from equation (4.28). Owing to the ferroelectric's layer voltage amplification, the ON-current increases as

t_{FE} grows, and the switching curve gets steeper. A good level of agreement between analytical and simulated outcomes validates the proposed model.

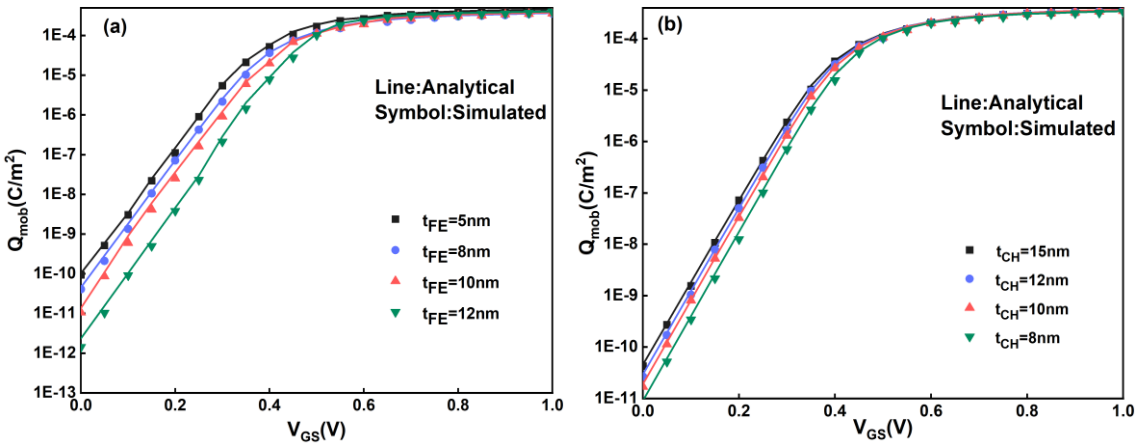


Fig. 4.10. Mobile charge density variation with gate voltage at various (a) ferroelectric layer thicknesses and (b) channel thicknesses, compared with simulated results.

Fig. 4.9 (a) and (b) demonstrate the drain current variation with drain voltage for V_{GS} = 1 V while varying the ferroelectric and silicon channel thicknesses. Drain currents are comparable in the linear zone, whereas devices with greater t_{FE} show larger saturation currents in the saturation mode. A similar case is observed for the drain current at different channel thicknesses. Fig. 4.10 (a) and (b) depict the fluctuation of modeled mobile charge density with the gate voltage for various ferroelectric layer thicknesses using equation (4.19). The analytical and the simulated data are compared, and the proposed model is shown to be valid. As observed, the channel gets easily depleted for the lower value of ferroelectric and channel thickness since the mobile charge density is less. This eventually helps in decreasing the subthreshold current in the device. Fig. 4.11 (a) illustrates the variation of subthreshold swing (SS) with ferroelectric layer thickness at different silicon channel thicknesses. As can be seen, the SS value is below 60 mV/dec, indicating that the proposed model improves subthreshold characteristics significantly, making it a favorable candidate for low-power switching applications.

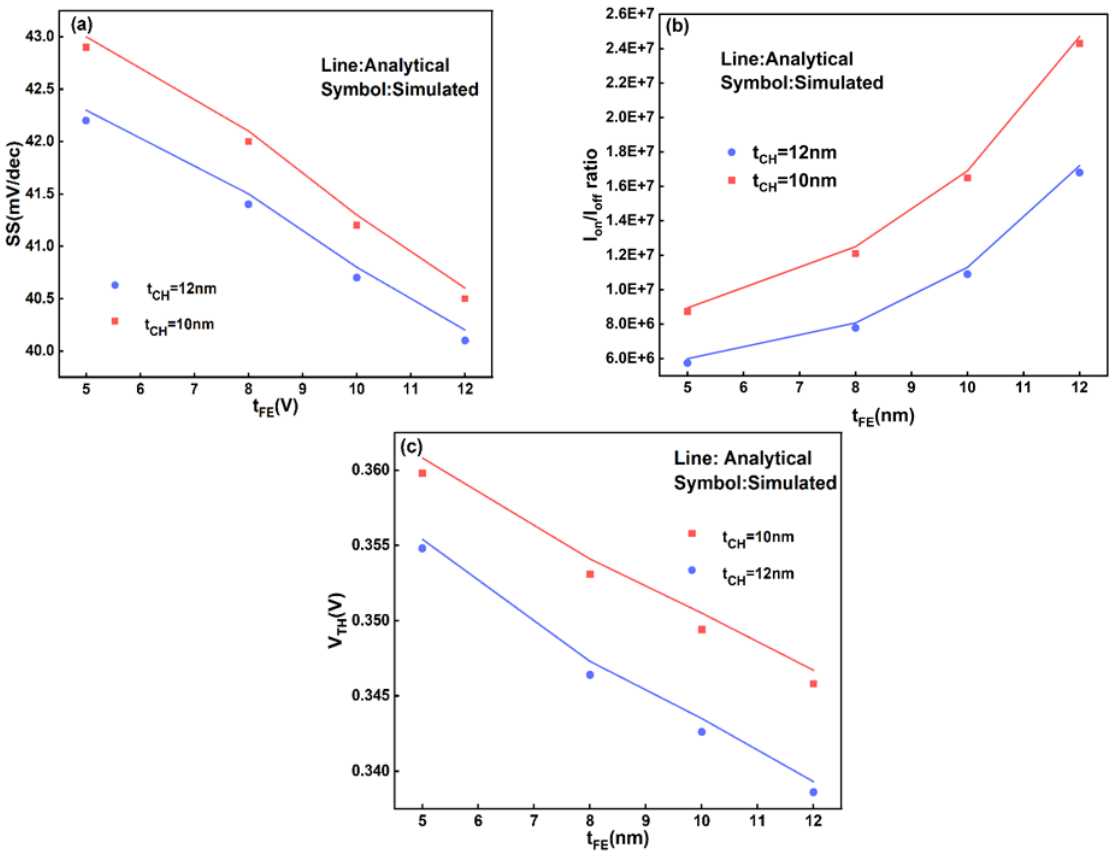


Fig. 4.11. (a) SS (b) I_{on}/I_{off} and (c) Threshold voltage variation with ferroelectric layer thickness at different channel thicknesses.

The SS values are calculated analytically from equation (4.31). The equation shows the dependency of SS on the gate voltage and the surface potential. The negative capacitance effects offered by the ferroelectric layer in the gate stack can provide differential amplification of the interface potential ($d\phi_{SP}/dV_{GS} > 1$), which can potentially lead to steep-slope behavior (SS < 60 mV/decade) in the transfer characteristics of ferroelectric FET. Fig. 4.11 (b) depicts the I_{on}/I_{off} ratio for DG-JAM-NC-FET with different ferroelectric and channel thicknesses. As observed, the on current (I_{on}) increases with increase in ferroelectric thickness, which enhances the I_{on}/I_{off} ratio of the device. In addition, higher silicon channel thickness values significantly impair the I_{on}/I_{off} ratio, as shown in Fig. 4.11 (b). It is obtained from the transfer characteristic curve of the model. Analytical and simulated data are perfectly matched to each other. The variability in threshold voltage with t_{FE} is shown in Fig.

4.11 (c). The threshold voltage is defined as the gate voltage at which the minimum surface potential of a MOS device is equal to two times of shift in Fermi Potential. The threshold voltage of negative capacitance FET is lower as compared to MOSFET. Threshold voltage decreases with increasing t_{FE} and t_{CH}, as shown in Fig. 4.11 (c) and also evident from equation (4.25). An increase in ferroelectric thickness leads to a decrease in ferroelectric capacitance, and hence threshold decreases. Threshold voltage changes substantially with increasing interface layer thickness, doping concentration, and silicon channel thickness, in conventional JL transistors [155], resulting in increased variability difficulties due to restricted control of design and doping concentration. Hence, this device can solve the junctionless transistor's variability difficulties.

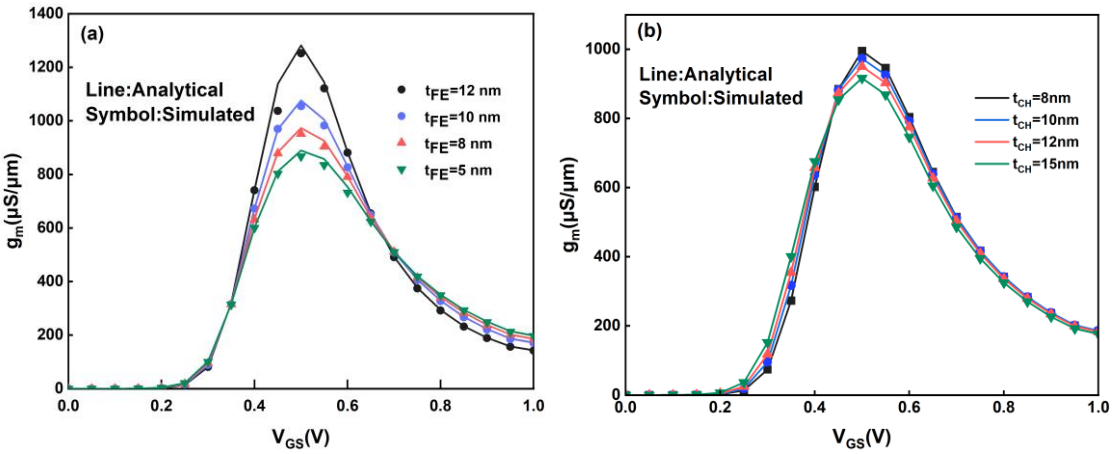


Fig. 4.12. Transconductance as a function of gate voltage at various (a) ferroelectric layer thicknesses (b) channel thicknesses, compared with simulated results.

Fig. 4.12 (a) and (b) show the transconductance variation at various ferroelectric thicknesses. The curve so obtained is calculated from equation (4.30). It can be observed that an increase in the ferroelectric thickness results in the enhancement of the amplification factor and hence a rise in the transconductance of the device. The transconductance is used to mathematically model any device where some current is a function of some voltage. The larger the transconductance for a device, the greater the gain (amplification) it is capable of delivering. The voltage amplification effect generated by the Negative Capacitance property

of the ferroelectric layer boosts the transconductance, which can improve the analog performance of the device. It can be seen that our model strongly matches the numerical simulations.

4.5.2. Temperature Analysis of double gate JAM-FET with and without ferroelectric

This section provides simulative comparisons of the electrical characteristics for the JAM FET configuration with and without a ferroelectric layer. The comparison shows the impact of temperature variation from 200K to 500K on the respective devices. Device parameters such as drain current, transconductance, output conductance, SS, and switching ratio are studied for the temperature range of 200K-500K to better understand how the negative

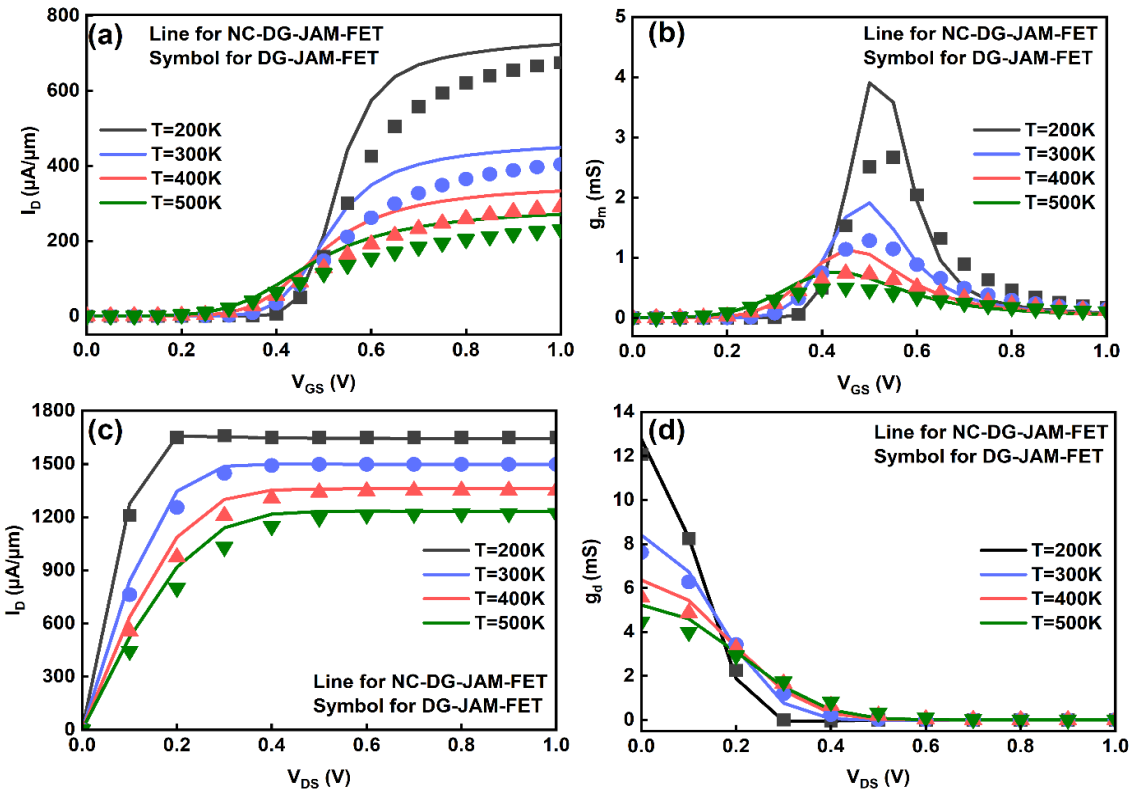


Fig. 4.13. Transfer characteristics (a), transconductance (b), output characteristics (c) and output conductance (d) of the devices with temperature variation.

capacitance affects the device. Fig. 4.13 (a) represents the transfer characteristics for DG-JAM-FET and NC-DG-JAM-FET. As observed, the drain current parameters of NC-DG-JAM-FET are sharper than DG-JAM-FET because negative capacitance leads to lower

leakage current. Regardless of the fact that the NC-DG-JAM-FET has superior performance over DG-JAM-FET, it is clear that the properties of NC-DG-JAM-FET decline at high temperatures owing to the elimination of the negative capacitance effect.

Fig. 4.13 (b) shows the transconductance variation for both devices at temperatures 200K, 300K, 400K, and 500K. The peak value of transconductance in NC-DG-JAM-FET is significantly higher than those of DG-JAM-FET, which makes it suitable for various CMOS

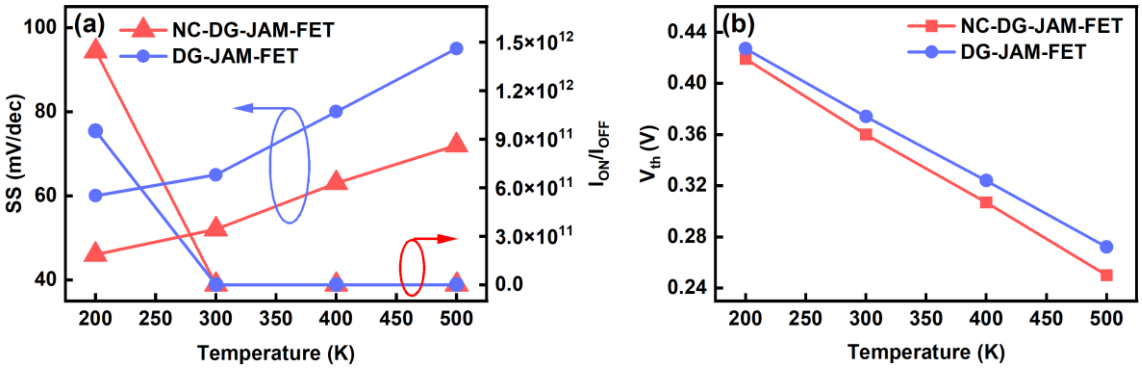


Fig. 4.14. (a) SS and I_{ON}/I_{OFF} ratio. (b) Threshold voltage of the devices with temperature variation.

applications. Fig. 4.13 (c) and (d) represent the output characteristics and output conductance at various temperatures for the respective devices. As observed, there is a decrease in drain current with temperature for both the devices but the characteristics of NC-DG-JAM-FET are still better than the DG-JAM-FET even at 500K. The output conductance depends on the region under which the device is operated. It is also observed that the output conductance

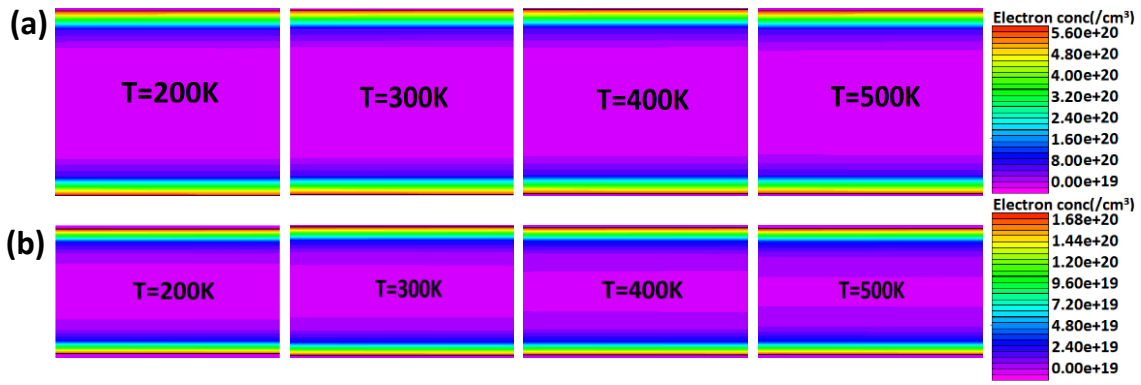


Fig. 4.15. Contour plot for electron concentration of DG-JAM-FET (a) and NC-DG-JAM-FET (b) at different temperatures.

values are higher for NC-DG-JAM-FET despite the fact that this parameter decreases with an increase in temperature.

Fig. 4.14 (a) and (b) represent the comparison between DG-JAM-FET and NC-DG-JAM-FET in terms of SS, I_{ON}/I_{OFF} ratio, and threshold voltage with respect to temperature. As shown, the SS is much steeper at lower temperatures, while V_{th} and I_{ON}/I_{OFF} are lower at higher temperatures. Since $SS = kT/q$, it is clear that the SS increases with the increase in temperature. The threshold voltage decreases with an increase in temperature showing the positive temperature coefficient because of the changes in the fermi level and bandgap [111]. The I_{ON}/I_{OFF} ratio achieves maximum value at lower temperatures, but the switching ratio of NC-DG-JAM-FET is still better than DG-JAM-FET.

Fig. 4.15 and 4.16 show the contour plots of the electron concentration and conduction band energy at various temperatures for both DG-JAM-FET and NC-DG-JAM-FET devices. It can be interpreted that the conduction happens through the bulk of silicon in NC-DG-JAM-FET, due to which the depletion capacitance exists from the off state to the on state of the transistor. This varying depletion capacitance offers an effective capacitance matching and thus reduces the major issue of hysteresis in FE-FETs [163].

Fig. 4.16. Contour plot for conduction band energy of DG-JAM-FET (a) and NC-DG-JAM-FET (b) at different temperatures.

4.5.3. Analytical results showing the effects of temperature on NC-DG-JAM-FET

The surface potential (ϕ_{SP}) variation with gate voltage (V_{GS}) for a particular temperature (T) range is shown in Fig. 4.17 (a) is directly calculated from equations (4.7) and (4.23). As evident, the step-up conversion capacity of NC-DG-JAM-FET gradually diminishes as the

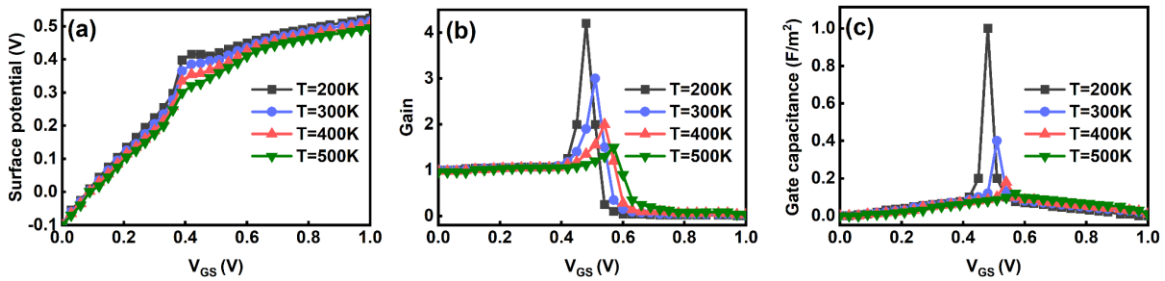


Fig. 4.17. Surface potential (a), gain (b), gate capacitance (c) as a function of V_{GS} at various temperatures.

temperature rises. This trend can also be seen in Fig. 4.17 (b). The voltage amplification factor or gain is defined in equation (4.30). This property indicates that the negative capacitance effect diminishes with rising temperature, which is consistent with experimental observations [171]. The ability to raise the surface potential in this arrangement when the ferroelectric is in

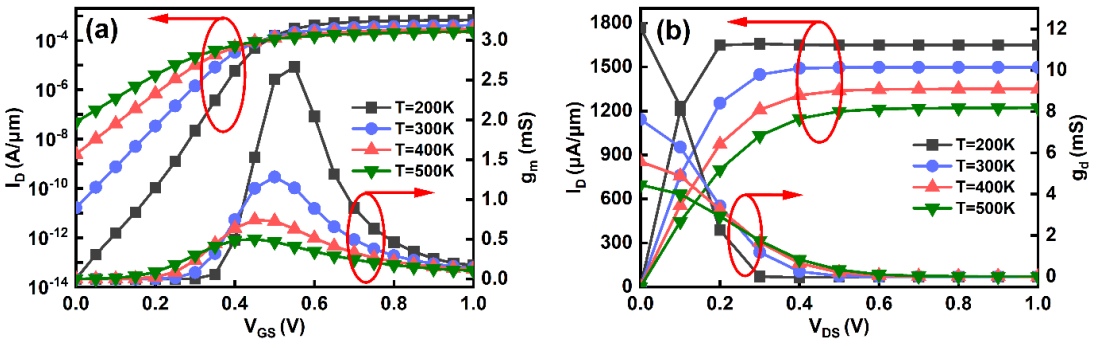


Fig. 4.18. Transfer characteristics and transconductance (a), output characteristics and output conductance (b) of NC-DG-JAM-FET at various temperatures.

the negative capacitance area can be used to increase gate electrode control over a FET channel, yielding steeper SS that surpasses the Boltzmann limit (SS < 60 mV/decade) [109].

We plotted the C-V characteristic curve of this structure at different temperatures in Fig. 4.17 (c) to study the temperature influence on gate capacitance in such devices. A significant gain is indicated by the peaked C-V characteristic, which decreases as temperature increases.

In other words, when the temperature increases from 200 to 500 K, the NC impact continues to decrease.

The SS is generally stated by measuring the transfer characteristics curve. The ferroelectric NC idea can explain values of SS < 60 mV/decade at room temperature. Fig. 4.18 (a) shows the input characteristics on the primary axis and transconductance on the secondary axis of our investigated NC-DG-JAM-FET structure. Fig. 4.18 (b) shows the effects of temperature on the output characteristics and output conductance of the proposed device when the gate voltage is maintained at 1V. As the temperature rises, the drain current decreases, leading to a fall in the I_{ON}/I_{OFF} ratio, as shown in the secondary axis of Fig. 4.19. This is how the phenomenon of the temperature-dependent negative capacitance of drain current can be explained. The gate stack capacitance ($C_G = Q/V_{GS}$) depends directly on the charge flowing across the channel while V_{GS} is constant.

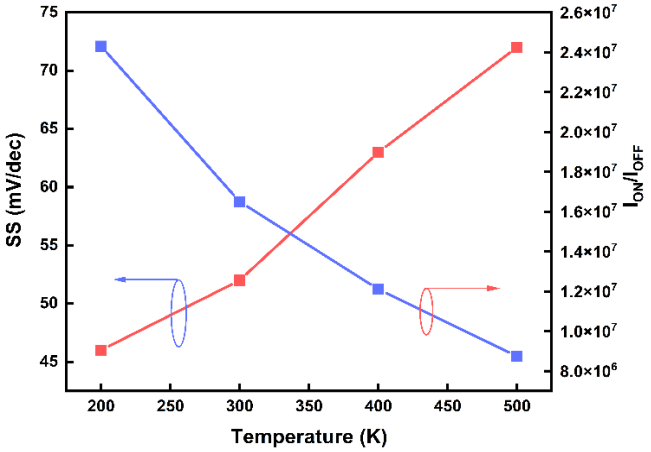


Fig. 4.19. SS and I_{ON}/I_{OFF} ratio at different temperature.

The SS values increased from 46 to 72 mV/decade with the increase in temperature, as evident in the primary axis of Fig. 4.19. The dependency of SS on temperature is evident from equation (4.32). On the other hand, when the temperature rises, the inverse of amplified voltage grows. The definition of ferroelectric capacitance might help you understand this: $1/C_{FE} = 2\alpha t_{FE} + 12\beta t_{FE}Q^2$ [172]. When the temperature approaches T_c, the maximum value of $2\alpha t_{FE}$, which overrides the negative capacitance, drops, causing the negative capacitance to

grow. However, once the V_{GS} rises to a particular level, the next term $12\beta t_{FE}Q^2$ emerges; therefore, it should not be overlooked. It will display nonlinear temperature dependency and counterbalance the negative component, resulting in a positive ferroelectric capacitance. As a result, as the temperature approaches T_c, C_{FE} drops. According to equation (4.32), there is a linear increase in the SS with temperature. Consequently, after an inevitable rise in temperature, the SS is significantly more than 60 mV/decade.

4.6. Summary

This chapter presents an analytical approach for calculating the surface potential and drain current of a symmetric long-channel DG-JAM-NC-FET. In contrast to existing work, the proposed analytical model shows an improvement in electrical characteristics. An analytical model for surface potential, threshold voltage, and drain current is developed using Poisson's equation, Landau Khalatnikov's (LK) equation, and Pao-Sah integral. The ferroelectric layer (HZO) was utilized to investigate the impact of negative capacitance. The alteration of surface potential, gate capacitance, gain, threshold voltage, and subthreshold swing with the applied gate voltage was investigated using the derived model, and the device's step-up conversion capabilities and better-switching characteristics were demonstrated. The impact of the ferroelectric thickness and channel thickness on the device performance was carried out in the investigation. The investigation also shows the critical ferroelectric thickness of 12 nm, which is the maximum thickness that ensures hysteresis-free operation at the device level. This model was further expanded to get the mobile charge density, transconductance, transfer characteristics, output characteristics, and I_{on}/I_{off} ratio. The alteration of surface potential, gate capacitance, gain, threshold voltage, and SS with the temperature ranging from 200K to 500K was also analyzed using the derived model. It has been found that the internal voltage amplification declines as temperature rises, but the SS increases from 46 to 72 mV/decade with the increase in temperature. Numerical simulations using the Silvaco ATLAS TCAD tool

were used to validate the analytical model. The acquired analytical results obtained were in good agreement with the simulated outcomes.

Chapter 5

Double Gate Ferroelectric FET for Biosensing Application

In previous chapter, a symmetric double gate negative capacitance based junctionless accumulation mode ferroelectric FET is introduced and analyzed. After designing of an optimized and improved performances of the Ferroelectric FET device incorporating JAM and NC effect, exploration of the applications based on the proposed device is the next step. In the current chapter, a biosensor based on double gate JAM ferroelectric FET has been designed and investigated. An analytical model for trap-assisted biosensing in Dual Cavity Negative Capacitance Junctionless Accumulation Mode FET is used for detecting various biomolecules. The nano-cavities are created inside the gate dielectric stack to collect biomolecules such as proteins and DNA. As the biomolecules are infused as traps in the cavity areas, electrical properties of the biosensor, like input characteristics, transconductance, threshold voltage, on-state current, and subthreshold swing change. The sensitivity of the proposed biosensor is obtained and also compared with the existing biosensor and found that it is best suited for susceptible low-power biosensing applications.

5.1 Introduction

The remarkable properties of biosensors sparked a great deal of interest in continuing research in this area. The development of technology-aided in pushing the field of biosensors to its limit and expanding its use in various industries, including pasteurization, environmental sensing, and national healthcare[173]. Because of its early detection, ongoing assessment, and diagnosis capabilities, the biosensor is crucial in the medical industry. The outbreak of corona (Covid-19) pandemic is the finest example of the significance of biosensors in medical diagnosis since early disease detection can prevent the virus's spread [174], [175].

A field-effect transistor (FET)-based biosensors draws interest due to their compressed area, great sensitivity, low energy utilization, accessible mass manufacture technique, and broad detection range [176]. Biosensors are primarily used in the early detection of biomarkers to prevent and diagnose the disease has been one of the interesting research fields. Systems with increased sensitivity are constantly required in biological research because even modest relative fluctuations in a biomarker's concentration can be significant [177]. The biosensor's current sensitivity is determined by the difference in current between conditions with and without the presence of biomolecules.

In order to recognize biomolecular entities at ultralow concentrations, higher current sensitivity is required [178]. Higher current sensitivity can be reached while the biosensor is running in the subthreshold region for FET-based biosensors. The highest current sensitivity that can be attained is however restricted by the Boltzmann limit of subthreshold swing (SS) to 60 mV/decade at ambient temperature in typical FET-related biosensors [179]. With the development of technology, efficiency has become much more in demand. Therefore, a transition to a different device that can handle these difficulties is required. A steep-switching device such as negative capacitance FETs (NCFETs) is a possible method for overcoming the Boltzmann limit. A ferroelectric (FE) material layer is used in the gate-stack to accomplish

internal voltage amplification and the requisite steep subthreshold slop of NCFETs [180]. Negative capacitance (NC) has a positive impact from two angles. Firstly, it decreases the SS, increasing current sensitivity in the weak inversion domain. Secondly, it significantly overdrives the sensor, lowering its power consumption [181]. The rapid source-drain junction formation, higher parasitics, and challenging fabrication process of traditional MOSFETs are further downsides [182]. To overcome such drawbacks, a negative capacitance based Junctionless Accumulation Mode Ferroelectric FET (JAM-FE-FET) is used, as discussed in previous chapters.

Therefore, a very sensitive biosensor is developed by acquiring the benefits of NC and JAMFET. The main impetus for researching the advantages of NC-based JAM-FET for biosensing applications is the need for faster and more accurate biosensors without adding extra burden on expensive manufacturing equipment. Hence, to address the need for highly sensitive and quick biosensing applications, a ferroelectric material-based Dual Cavity Negative Capacitance Junctionless Accumulation Mode FET (DC-NC-JAM-FET) based biosensor is proposed in this paper. The nano-cavities are created inside the gate dielectric stack to collect biomolecules with different dielectric constant, such as proteins and DNAs. Nano-cavities are filled with air if no biomolecules are present. The electrical properties of the biosensor, like threshold voltage, drain current, and SS change as the targeted biomolecules are infused in the nano-cavities because the effective oxide capacitance changes as a result of the biomolecules' dielectric constants [33].

Devices and circuits are connected through analytical and compact models. These models are also useful for gaining a deeper understanding of how devices work and for assessing how well biosensors perform. There are several analytical models of JLT and FE-FET accessible in the literature [183]–[185]. However, to the best of the author's knowledge, there isn't any analytical model of DC-NC-JAM-FET biosensing device. Thus, by incorporating the benefits of NC and

double-gate JAMFET, this chapter proposes an analytical model of DC-NC-JAM-FET biosensor architecture. The proposed device is used to detect biomolecules with better sensitivity because of its high On-state current, low power dissipation, and improved subthreshold swing.

5.2. Device Architecture and Simulation

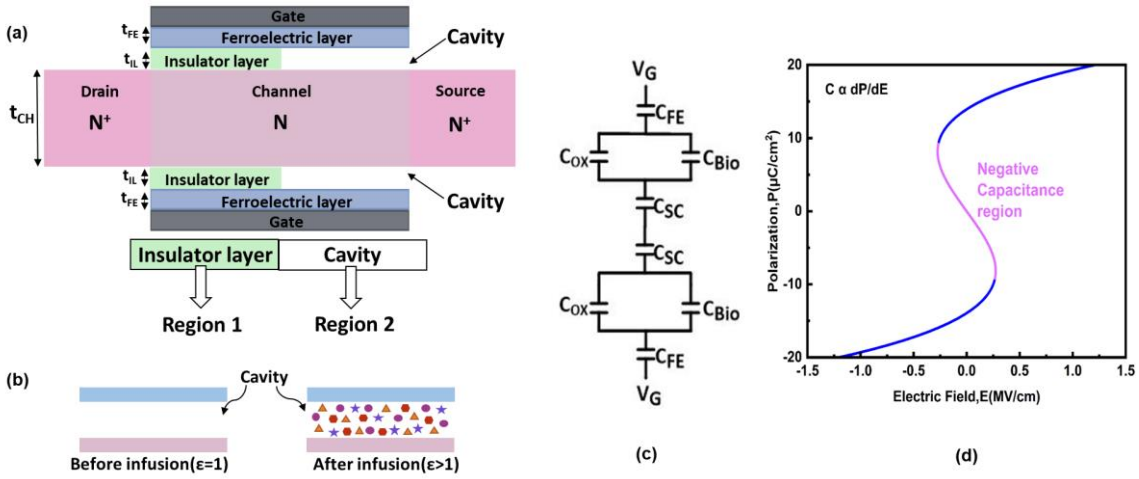


Fig. 5.1. (a) Structure of DC-NC-JAM-FET biosensor, (b) biomolecule infusion in the cavity region, (c) equivalent capacitance model (d) P-E curve for ferroelectric illustrating the negative capacitance region.

A 2D schematic cross-sectional view of the DC-NC-JAM-FET biosensor is shown in Fig. 5.1(a). The device employs two nano-cavities for biomolecules, and ferroelectric material layers made of hafnium zirconium oxide (HZO). TiN with work function 4.65 eV is used as gate metal [186]. In JAM structure source and drain are heavily doped (10^{19} cm^{-3}) and channel is moderately doped (10^{17} cm^{-3}). Ferroelectric, insulator, and channel layer thicknesses are assumed to be 5nm, 2nm, and 20nm, respectively. DC-NC- JAM-FET detects biomolecules such as streptavidin, biotin, APTES, protein A, and DNA having different dielctric constants. The dielectric constant for biomolecules is shown in Table 5.1. Fig. 5.1(b) shows the cavity region with no biomolecule, i.e., air (ε=1) and infusion of the biomolecules having different dielectric

Fig. 5.1(c) shows the equivalent capacitance model, and Fig. 5.1(d) represents Polarization-Electric field curve obtained from the following equation:

$$E = 2\alpha P + 4\beta P^3 + 6\gamma P^5 \quad (5.1)$$

Since capacitance (C) is proportionate to the gradient, dP/dE, this curve exhibits a negative gradient region from which the negative capacitance originates. The Silvaco ATLAS TCAD simulator is used for the simulations, which include the Lombardi CVT model, Shockley-Read-Hall (SRH) recombination, fermi, and Landau-Khalatnikov (LK) models [146]. The calibration of this work [187] is done to validate and give a realistic simulation environment as depicted in Fig. 5.2(a).

Table 5.1. Biomolecules and corresponding dielectric constants

Biomolecules	Dielectric Constant
Streptavidin [188]	2.1
Biotin [185]	2.63
APTES [188]	3.57
Protein A [189]	4
DNA [190]	8

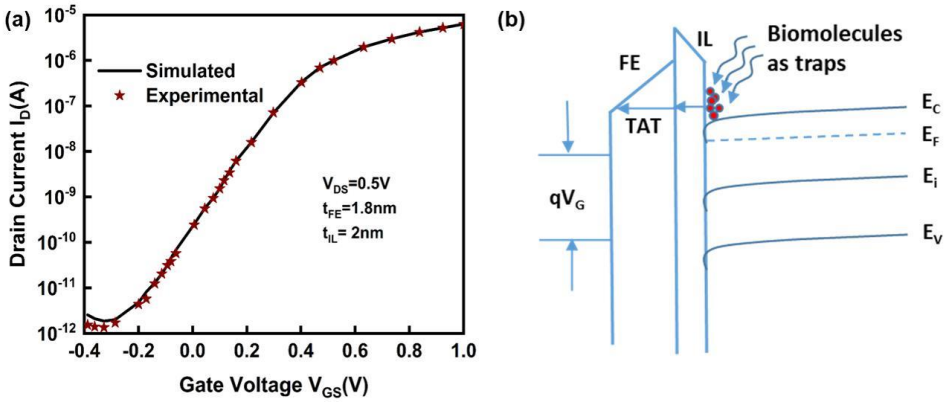


Fig. 5.2. (a) Calibration with the reported work. (b) Energy band diagram showing trap assisted tunneling (TAT) of biomolecules through ferroelectric layer.

Fig. 5.2 (b) depicts the relevant energy band representing the trap assisted phenomenon of biomolecules through the layers of the biosensor. Trap assisted tunnelling (TAT) component is one of the major components which have a significant impact on biosensor [191]. The trap

tunnelling rate increases significantly in the presence of an electric field, which dramatically enhances the electron-hole production rate [192].

5.3. Analytical Model Formulation

The two major regions are taken into account in the development of an analytical model for the proposed device. Region I is the insulator layer, and region II is the cavity layer which is to be filled with biomolecules. The equivalent capacitance model of these regions is presented in Fig. 5.1 (c) and is given by the following equations:

$$C_{IL} = \frac{\varepsilon_{IL}}{t_{IL}} \tag{5.2}$$

$$C_{bio} = \frac{\varepsilon_{bio}}{t_{bio}} \tag{5.3}$$

where $\varepsilon_{IL}, \varepsilon_{bio}, t_{IL}, and\ t_{bio}$ are permittivity and thickness of the insulator layer and cavity layer to be filled with biomolecules, respectively. For the sake of simplicity, the thickness of the biomolecule layer and the insulator is considered to be equal.

The total capacitance (C_{Total}) for region 1 and region 2 is expressed as:

$$C_{Total} = C_{IL} + C_{bio} \tag{5.4}$$

The total gate capacitance of the device is given by:

$$\frac{1}{C_G} = \frac{1}{C_{FE}} + \frac{1}{C_{IL} + C_{bio}} + \frac{1}{C_{SC}} \tag{5.5}$$

Additionally, the drain current and charge density models are combined with the Landau-Khalatnikov (L-K) equation in order to build the analytical model [49]. Drops across the insulator layer and cavity layer ($V_{IL} + V_{bio}$), ferroelectric layer (V_{FE}), flat band voltage (V_{FB}), and surface potential (ϕ_{SP}) are added to determine the overall gate voltage:

$$V_{GS} = V_{FE} + V_{IL} + V_{bio} + V_{FB} + \phi_{SP} \tag{5.6}$$

where

$$V_{IL} = \frac{Q_{TOT}}{C_{IL}}, \qquad V_{bio} = \frac{Q_{TOT}}{C_{bio}}, \qquad V_{FB} = \phi_M - \phi_{si}$$

$$\phi_{si} = \chi + \frac{E_g}{2} - \frac{kT}{q} ln\left(\frac{N_D^+}{N_D}\right) \tag{5.7}$$

where N_D^+ is the doping concentration in source/drain regions of JAMFET and (ϕ_{si}) is the work function of silicon. The following equation determines the charge density (Q_{TOT}) over the entire channel [166]:

$$Q_{TOT}(x = t_{CH}) = qN_D t_{CH} - qN_D \int_{\frac{-t_{CH}}{2}}^{\frac{+t_{CH}}{2}} e^{\frac{(\phi - V)}{\frac{kT}{q}}} dx \tag{5.8}$$

The ferroelectric layer's negative capacitance is included into the computation of using the Landau-Khalatnikov (L-K) equation as shown below [43]:

$$V_{FE} = 2\alpha t_{FE} Q_{TOT} + 4\beta t_{FE} Q_{TOT}^3 + 6\gamma t_{FE} Q_{TOT}^5 \tag{5.9}$$

Here *α, β,* and *γ* are the material parameters, which are determined as given in ref [97]. On solving (5.6) and (5.9) the following expression is obtained:

$$V_{GS} - V_{FB} - \phi_{SP} = \frac{Q_{TOT}}{C_{IL} + C_{bio}} + 2\alpha t_{FE} \frac{Q_{TOT}}{2} + 4\beta t_{FE} \left(\frac{Q_{TOT}}{2}\right)^3 + 6\gamma t_{FE} \left(\frac{Q_{TOT}}{2}\right)^5 \tag{5.10}$$

To obtain the threshold voltage, a fully depleted channel is assumed, and hence, the total charge density can be expressed as:

$$Q_{TH} = qN_D t_{CH} \left(1 - \frac{1}{2}\sqrt{\frac{\pi kT}{q\phi_{SP}}}\right) \tag{5.11}$$

ϕ_{SP} can be evaluated from [168] as:

$$\phi_{SP} = \frac{qN_D t_{CH}^2}{8\varepsilon_{si}} \tag{5.12}$$

Now, the threshold voltage is obtained by substituting (5.11) and (5.12) in (5.10):

$$V_{TH} = V_{FB} + \frac{qN_D t_{CH}^2}{8\varepsilon_{si}} + \left(\frac{1}{C_{IL} + C_{bio}} + \alpha t_{FE}\right) Q_{TH} + 4\beta t_{FE} \left(\frac{Q_{TH}}{2}\right)^3 + 6\gamma t_{FE} \left(\frac{Q_{TH}}{2}\right)^5 \tag{5.13}$$

The mobile charge in the channel is obtained by putting $\phi_{SP} = \frac{t_{CH}}{8\varepsilon_{si}}(Q_{MOB} + qN_D t_{CH})$ [155] and $Q_{TOT} = (Q_{MOB} + qN_D t_{CH})$ along with simple mathematical computations of (5.8) and (5.10) as:

$$V_{GS} - V_{FB} - V + \frac{t_{CH}}{8\varepsilon_{si}}(Q_{MOB} + qN_D t_{CH}) + V_T\, ln\left(Q_{MOB}\sqrt{\frac{(Q_{MOB} + qN_D t_{CH})}{2\varepsilon_{si}\pi V_T q^2 N_D^2 t_{CH}}}\right)$$

$$= \left(\alpha t_{FE} + \frac{1}{C_{IL} + C_{bio}}\right)(Q_{MOB} + qN_D t_{CH}) + 4\beta t_{FE}\left(\frac{Q_{MOB} + qN_D t_{CH}}{2}\right)^3$$

$$+ 6\gamma t_{FE}\left(\frac{Q_{MOB} + qN_D t_{CH}}{2}\right)^5 \tag{5.14}$$

The drain current expression is derived using the above mobile charge model. It is determined by integrating Q_{MOB} from source to drain using the Pao-Sah integral [166] as follows:

$$I_D = -\mu\frac{W}{L}\int_0^{V_{DS}} Q_{MOB}\, dV \tag{5.15}$$

$$I_D = -\mu\frac{W}{L}\left[\begin{array}{l}\frac{qN_D t_{CH}}{2} ln(\, Q_{MOB} + qN_D t_{CH}) \\ -\frac{\alpha t_{FE} Q_{MOB}^2}{2} - 3\beta t_{FE}^2 Q_{MOB}^2 \\ \left\{\begin{array}{l}\frac{Q_{MOB}^2}{8} + \frac{Q_{MOB} N_D q t_{CH}}{2} \\ +\left(\frac{N_D q t_{CH}}{2}\right)^2\end{array}\right\} \\ -\frac{Q_{MOB}}{2}\left(3V_T - \frac{Q_{MOB} t_{CH}}{8\varepsilon_{si}} + \frac{Q_{MOB} t_{CH}}{2\varepsilon_{IL} + \varepsilon_{bio}}\right)\end{array}\right]_{Q_{MOBS}}^{Q_{MOBD}} \tag{5.16}$$

Here, Q_{MOBS} and Q_{MOBD} are obtained from (5.14) by varying the voltage from zero to drain to source voltage (V_{DS}). The expression for transconductance can be expressed as follows [193]:

$$g_m = \frac{dI_D}{dV_{GS}} \tag{5.17}$$

5.4. Results and Discussion

5.4.1. DC-NC-JAM-FET as a Bio-sensing Device for different biomolecules

In this section, the dielectric modulated DC-NC-JAM-FET is used as biosensing device for detecting various biomolecules with different dielectric constants. These biomolecules include Streptavidin, Biotin, APTES, Protein A, and DNA. The biomolecules in the cavity influences the electrical behavior of the device. The ability to detect biomolecules is made possible by

adjusting a material's permittivity since a change in permittivity also affects a material's capacitance.

Fig. 5.3 (a) depicts the electron concentration contour plots. It also shows the concentration remaining unchanged when no biomolecule is present. However, when additional biomolecules are added,the area below the cavity region are induced with charges. As evident from the figure, the charges that are induced depends on the various biomolecules. Fig. 5.3 (b) shows the energy band profile of DC-NC-JAM-FET based biosensor at different dielectric constant. It can be observed that the bands bend more at junction regions when the dielectric value of biomolecules rises, which improves the coupling between the source and the channel. Fig. 5.3 (c) show the surface potential along the horizontal direction with different dielectric constant of the biomolecules. It can be observed that, in the absence of biomolecules (ε = 1), the surface potential has a smaller value underneath cavity region. On the other hand, in the existence of

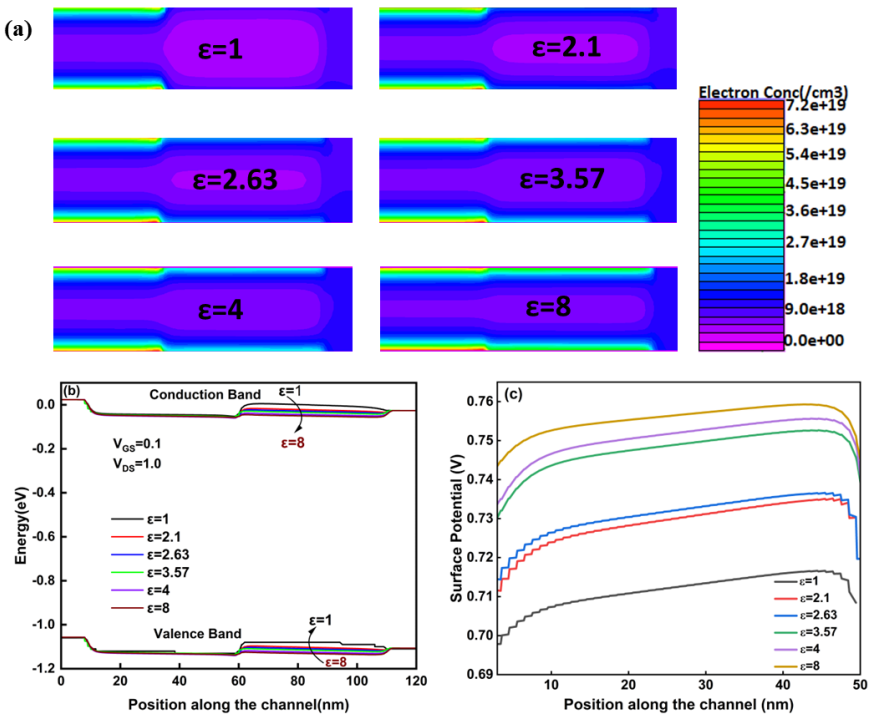


Fig. 5.3. (a) The contour plot for electron concentration with different biomolecules (b) Energy band plots against position along the channel showing the conduction and valence band of DC-NC-JAM-FET at different dielectric constants (c) Surface potential along the lateral direction for different dielectric constants

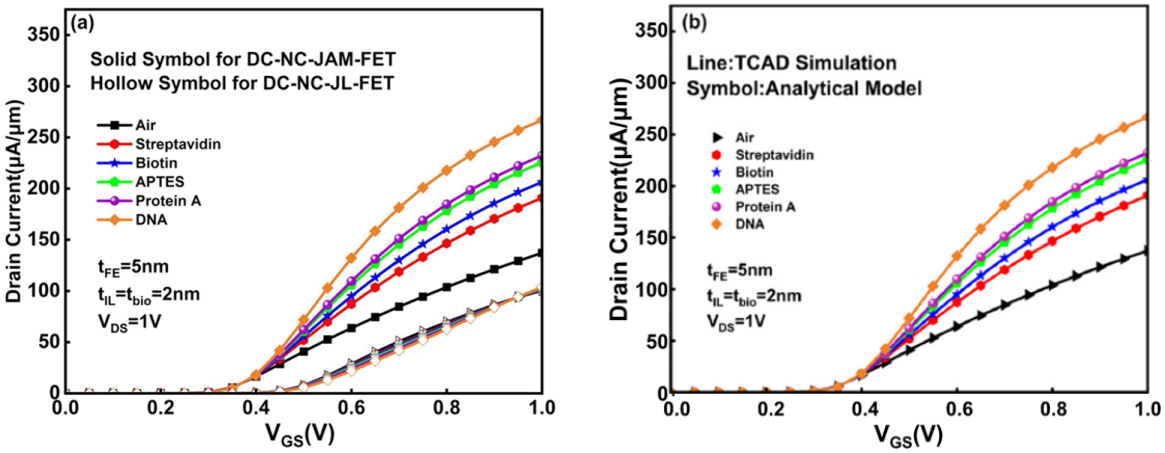


Fig. 5.4. (a) Drain current characteristics of the devices for different biomolecule dielectric constant, (b) analytical drain current characteristics.

biomolecules at ε > 1, the surface potential achieves a higher value in the cavity region. As the dielectric constant increases (ε), the coupling between gate and channel increases which leads to surface potential. Fig. 5.4 (a) implies that the DC-NC-JAM-FET attains superior drain current when compared to DC- NC-JL-FET. The suggested device's higher drain current is caused by the high electron mobility mobility provided by the JAM structure's high doping concentration in the source/drain regions which reduces the parasitics. Fig. 5.4 (b) shows the analytical results analogous to the TCAD simulated results. The figure makes it quite evident that the analytical and simulated outcomes agree closely. Additionally, it is deduced that the drain current increases with the biomolecules' dielectric constant. As a result of the insertion of a biomolecule, the surface potential changes because of its dependency on the dielectric constant.

Fig. 5.5 (a) shows the transconductance behavior of both the simulated architectures. The proposed device has a greater drift in transconductance as contrasted to the conventional device. This is because the transconductance is proportional to the drain current. Fig. 5.5 (b) shows the analytical results for the transconductance variation of the proposed device and its comparison with the TCAD simulation. The results appear to be relatively close to one another,

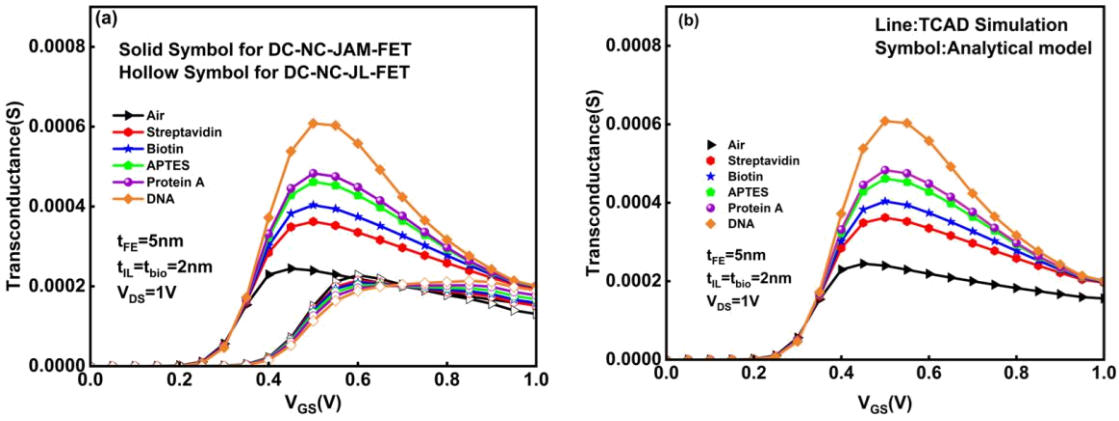


Fig. 5.5. (a) Transconductance of different devices for different dielectric constant, (b) analytical transconductance variation of the proposed device for various biomolecules.

and it is also evident that the transconductance value increases with the increase in the dielectric constant of the biomolecules.

The crucial factor for any type of sensor is its sensitivity, and a high sensitivity level is always desirable. The sensitivity of DC-NC-JAM-FET is analyzed in terms of Threshold voltage (V_{TH}), On Current (I_{on}), and Subthreshold Swing (SS), respectively. The expressions for sensitivity for each of the parameters can be expressed as below:

$$S_{V_{TH}} = \frac{V_{TH,bio} - V_{TH,air}}{V_{TH,air}} \tag{5.18}$$

$$S_{I_{ON}} = \frac{I_{ON,bio} - I_{ON,air}}{I_{ON,air}} \tag{5.19}$$

$$S_{SS} = \frac{SS_{bio} - SS_{air}}{SS_{air}} \tag{5.20}$$

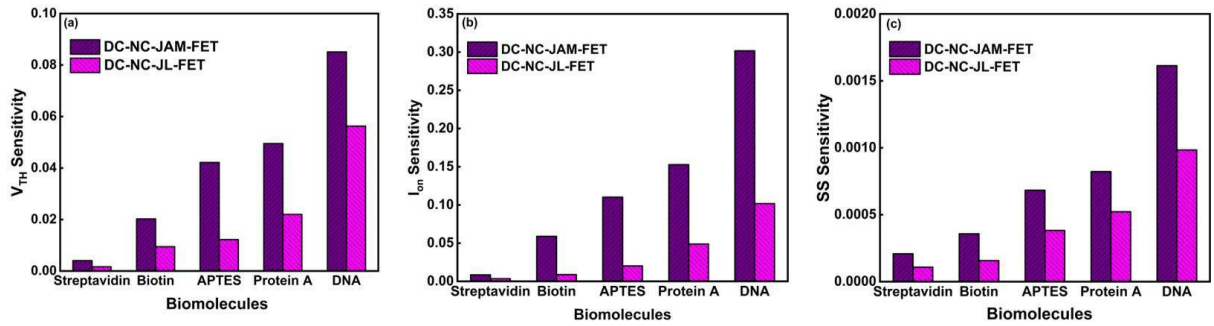


Fig. 5.6. Comparison of different devices with respect to (a) Threshold voltage sensitivity, (b) On Current sensitivity and (c) SS sensitivity at different dielectric constants.

Here, $V_{TH,\ bio,}$ and $V_{TH,\ air}$ is the threshold voltage values when the cavities are filled with biomolecules at dielectric constants of biomolecules (Ɛ=2.1, 2.63, 3.57, 4, 8) and no biomolecules, i.e., air (Ɛ=1). Fig. 5.6 (a), (b), (c) shows the sensitivity comparison between the proposed and existing biosensor. It is observed that as the dielectric constant increases, the sensitivity increases for both devices. It can also be inferred from the figures that the proposed device possesses higher sensitivity as compared to existing device. Therefore, the proposed device can be used as a biosensor for detecting various biomolecules such as Streptavidin, Biotin, APTES, Protein A, and DNA.

5.4.2. Impact of biomolecule concentration on DC-NC-JAM-FET:

The drain current characteristics of different device architectures for various biomolecule concentrations is shown in Fig. 5.7 (a). It is observed from Fig. 5.7 (a) that the drain characteristics are higher for the proposed device. This is owing to the fact that the mobility degradation in the JAM structure is negligible because of moderate doping in the channel region of the JAM structure when compared to the JL transistor, and thus, it improves the drain current. The analysis is carried out for various biomolecule concentrations, i.e., for positively charged (1e12 cm^2), negatively charged (-1e12 cm^2), and neutral biomolecules (0 cm^2). The

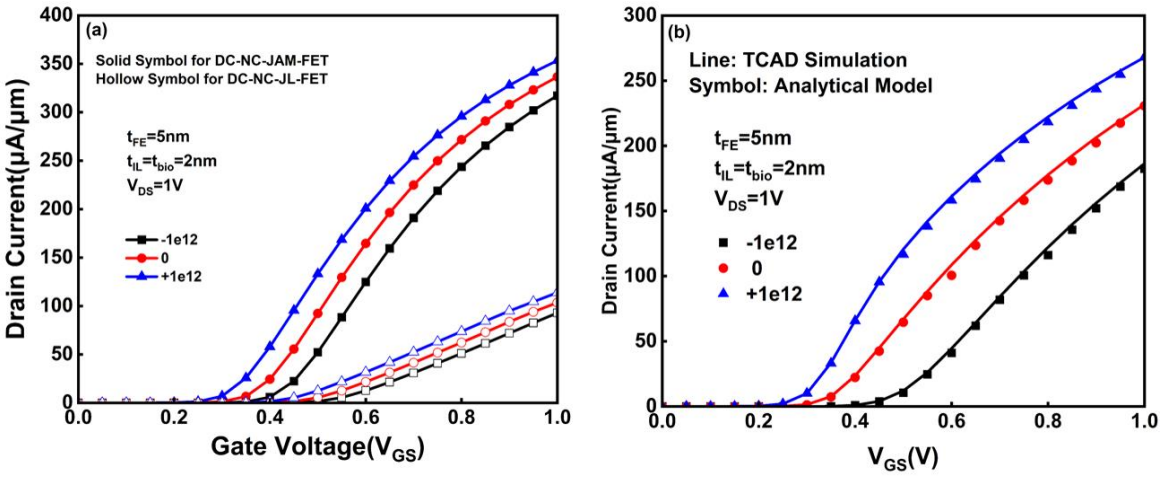


Fig. 5.7. (a) Drain current characteristics of the devices for different biomolecule concentration. (b) Analytical drain current characteristics of the proposed device.

analytical drain current characteristics of DC-NC-JAM-FET biosensors for different biomolecule concentrations is shown in Fig. 5.7 (b). It is observed that there is a good agreement between the analytical results and TCAD simulations.

It is also inferred from the figure that the drain current characteristics are higher for positively charged biomolecules. This is due to the change in the surface potential of the device.

Fig. 5.8 (a) and (b) represent the transconductance values for the different dielectric constants of the compared devices. The figure clearly illustrates that the transconductance drift is larger for the DC-NC-JAM-FET at different biomolecule concentrations. As the transconductance

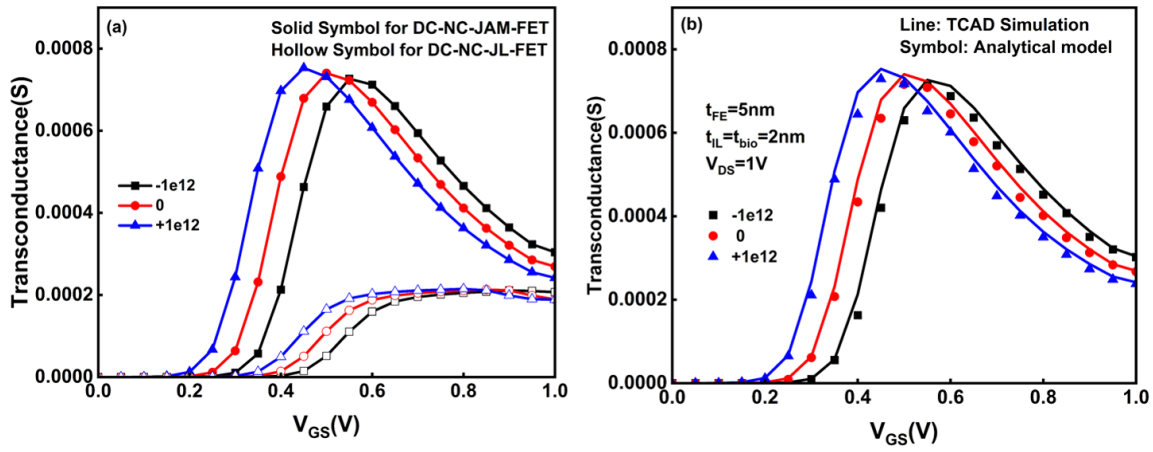


Fig. 5.8. (a) Transconductance of diiferent devices for various biomolecule concentartions
(b) Analytical transconductance values for various biomolecule concentrations.

value of the device is dependent on the drain current, it increases with an increase in drain current. Fig. 5.8 (b) illustrates the analytical results for different biomolecule concentrations. As observed, the analytical results are analogous to the simulated results. It can also be interpreted from the results that the g_m value is higher positively charged biomolecules are inserted and lower when negatively charged biomolecules are inserted in the cavities. This is a result of the biomolecules' insertion altering the surface potential.

The impact of biomolecule concentration on the Sensitivity parameters is also carried out in this section. The sensitivity comparison of the proposed biosensor with the existing, in terms

of parameters such as threshold voltage, on-current and subthreshold swing is shown in Fig. 5.9 (a), (b), and (c).

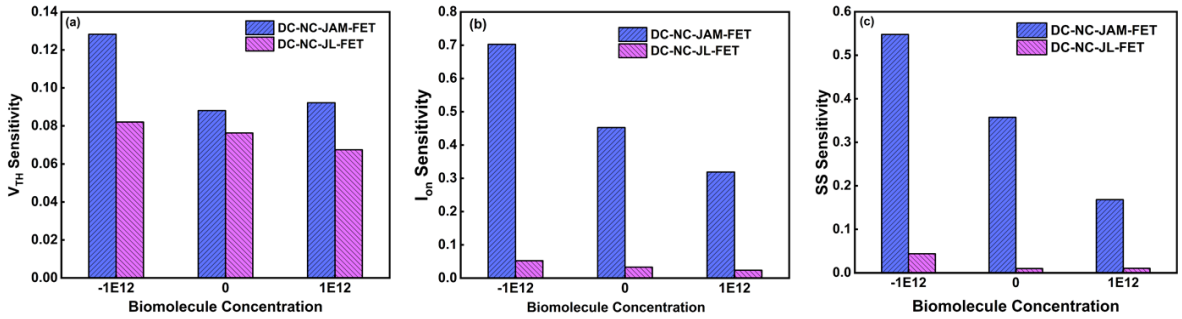


Fig. 5.9. Sensitivity comparison of different devices in terms of (a) threshold voltage (b) On current (c) Subthreshold Swing at different biomolecule concentrations.

As observed from Fig. 5.9 (a), the threshold voltage sensitivity for the DC-NC-JAM-FET is higher in comparison to DC-NC-JL-FET. The reason for this is that the threshold voltage can be modulated by biomolecule concentration by changing the capacitance. Also, the sensitivity at negatively charged biomolecule concentration is higher because the threshold voltage decreases as the biomolecule concentration is increased from negative to positive. Fig. 5.9 (b) shows the On current sensitivity of the DC-NC-JAM-FET with the compared device. As evident, the sensitivity of the device concerning to on-current is enhanced because the JAM structure lowers the mobility degradation, which in turn increases the On-current. Additionally, the On current value is higher for positively charged biomolecules, so its sensitivity is low. Fig. 5.9 (c) shows the sensitivity for both devices at different biomolecule concentrations in terms of SS. As observed, the SS sensitivity is higher for the proposed device because when the biomolecules' dielectric properties in the cavities are increased, the subthreshold swing reduces, and hence the sensitivity increases. It is also observed that as the biomolecule concentration increases, the subthreshold swing value increases, and thus the sensitivity is lower at positively charged biomolecules. The device is highly sensitive to negatively charged biomolecule concentrations. Therefore, after these critical analyses, the

proposed device can be a better alternative to detect several biomolecules and can be used as a biosensing device.

5.5. Summary

A physics-based analytical model for trap assisted biosensing in Dual Cavity Negative Capacitance Junctionless Accumulation Mode FET (DC-NC-JAM-FET) has been proposed for its better sensing ability. The device incorporates the ferroelectric interfaced negative capacitance with the junctionless accumulation mode FET and the biomolecules are used as traps which tunnels through ferroelectric layer. When biomolecules immobilize in the cavity region, electrical characteristics like drain current, transconductance, and sensitivity have been regarded as biosensing parameters for detecting them. The comparison of the proposed device with the existing device is carried out and found that the proposed device exhibits a larger shift in drain current. The sensitivity is calculated in terms of V_{TH}, I_{ON}, and SS. Additionally, it has been discovered that the proposed device has a threshold voltage sensitivity for DNA detection that is almost two to three times higher. The On-state current sensitivity and subthreshold sensitivity are also improved to a greater extent. Hence, the research work carried out shows that DC-NC-JAM-FET is an excellent candidate for a low-power ultra-sensitive biosensing device.

Chapter 6

Conclusions and Future Scope

6.1 Summary of Thesis Work

The main aim of this thesis is to investigate the performance of ferroelectric (FE) material-based FETs, specifically Negative Capacitance FETs (NCFETs) for low-power and high-frequency analog and digital applications. As devices reach the nanometer scale, reducing leakage currents becomes challenging due to the lower limit of voltage operation, which is roughly 60 mV/dec. While various ferroelectric structures have been documented in the literature, different issues have been encountered by these device configurations, whether related to performance or fabrication. Therefore, to overcome these challenges, ferroelectric layer, which offers negative capacitance, has been integrated with JAM FET. The benefit of JAM over existing FETs is that it combines the benefits of the junctionless transistor (JLT) and conventional FETs. It avoids excessive parasitic resistance due to stronger doping in the source and drain areas, resulting in higher conductivity and better characteristics than JLT. Hence, a novel Junctionless Accumulation Mode Ferroelectric FET has been proposed and thoroughly studied in this thesis.

The performance of a Single Gate Junctionless Accumulation Mode Ferroelectric Field Effect Transistor has been studied in **Chapter 3.** The device has been assessed in terms of RF/analog specifications for different channel lengths through simulations using TCAD Silvaco ATLAS TCAD tool, using the Shockley-Read-Hall (SRH) recombination, Ferro, Lombardi CVT, fermi, and LK models. Major analog metrics like transconductance (g_m), intrinsic gain (A_V), output conductance (g_d), and early voltage (V_{EA}) are obtained for the JAM-FE-FET

arrangement. Further, frequency analysis of the proposed device is performed and several critical RF parameters have been enhanced. This chapter also talks about the small signal parameters such as reflection coefficients (S_{11}, S_{22}), transmission coefficients (S_{12}, S_{21}), Gate Capacitance (C_{GG}), f_T, Maximum Transducer Power Gain (MTPG), and Unilateral Power Gain (UPG) at various ferroelectric thicknesses. Further, the effect of temperature variation on the device performance parameters has also been analyzed.

To further improve the performance and gate controllability, a Double Gate Junctionless Accumulation Mode Ferroelectric Field Effect Transistor has been proposed in **Chapter 4**. A systematic drain current model of the proposed device is developed using the Landau-Khalatnikov theory and the parabolic potential approximation to analyze the device properties. Various device parameters have been calculated using the model, including surface potential, gate capacitance, gain, threshold voltage, mobile charge density, drain current, subthreshold slope, and switching ratio. This work also discusses the influence of ferroelectric, silicon channel thickness, and temperature on different device parameters. Analytical data are compared to simulated outcomes generated using the TCAD Silvaco ATLAS simulator, which proved the model's reliability.

Further, the application of the proposed device structure has been explored for biomolecule detection in **Chapter 5**. The proposed biosensor is capable of detecting biomolecules by creating nano-cavities inside the gate dielectric stack to collect biomolecules such as proteins and DNA. The device incorporates the detection of charged and uncharged biomolecules in terms of dielectric constants and biomolecule concentration. As the biomolecules are infused as traps in the cavity areas, electrical properties of the biosensor, like input characteristics, transconductance, threshold voltage, on-state current, and subthreshold swing change. The sensitivity of the proposed biosensor is obtained and also compared with the existing biosensor and found that it is best suited for susceptible low-power biosensing applications.

6.2 Future Scope

In addition to the above conclusions drawn, the present work suggests several potential areas for future research work.

- This work can be further extended by performing quantum analytical modeling of NCFET.
- The effects of interface trap charges on various performance parameters of NCFET can be explored.
- The circuit response of the NCFET can also be done to employ for digital circuit applications such as inverters, RAM, and other gated logic designs.
- Moreover, the device design can be utilized as a gas sensor that can sense harmful gases.

Publications

Publications in Journals

1. **Snehlata Yadav**, Sonam Rewari, and Rajeshwari Pandey, "Junctionless Accumulation Mode Ferroelectric FET (JAM-FE-FET) for High Frequency Digital and Analog Applications," Silicon, vol. 14, pp. 7245–7255, Aug. 2022.

2. **Snehlata Yadav**, Sonam Rewari, and Rajeshwari Pandey, "Impact of temperature on a ferroelectric interfaced negative capacitance double gate junctionless accumulation mode field effect transistor-compact model," Proceedings of Royal Society A Math. Phys. Eng. Sci., vol. 479, no. 2271, March 2023.

3. **Snehlata Yadav**, Sonam Rewari, and Rajeshwari Pandey, "Surface potential and mobile charge based drain current modeling of double gate junctionless accumulation mode negative capacitance FET (DG-JAM-NC-FET)," International Journal of Numerical Modeling, vol. 37, no. e3172, Sep. 2023.

4. **Snehlata Yadav**, Sonam Rewari, and Rajeshwari Pandey, "Gate Engineered Ferroelectric Junctionless BioFET for Label-Free Detection of Biomolecules," Journal of Electronic Materials, vol. 53, pp. 683-692, Dec. 2023.

5. **Snehlata Yadav**, Sonam Rewari, and Rajeshwari Pandey, "Physics-based analytical model for trap assisted biosensing in dual cavity negative capacitance junctionless accumulation mode FET," Microelectronics Journal, vol. 143, no. 106032, Jan. 2024.

Publications in International Conferences

1. **Snehlata Yadav**, Sonam Rewari, and Rajeshwari Pandey, "Impact of temperature on negative capacitance based Junctionless Accumulation Mode Ferroelectric FET(JAM-FE-FET) ", Proc. of the International Conference on Electrical, Computer and Energy Technologies (ICECET 2022), 20-22 July 2022, Prague-Czech Republic

2. **Snehlata Yadav**, Sonam Rewari, and Rajeshwari Pandey, "Sensitivity analysis of Dielectric Modulated Dual Gate Ferroelectric Junctionless Transistor based Biosensor", International Conference of Electron Devices Society Kolkata Chapter (EDKCON), 26-27 November, 2022, Kolkata, India.

3. **Snehlata Yadav**, Sonam Rewari, and Rajeshwari Pandey, "Analysis of small signal parameters of NC-JAM-FET for high frequency RF applications", India Council International Conference (INDICON 2022), 24-26 November, 2022, Kerala, India.

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