STUDY AND IMPLEMENTATION OF POWER REDUCTION TECHNIQUES IN COMPLEX CIRCUIT

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VLSI DESIGN AND EMBEDDED SYSTEMS

by

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I, **Farheen Safdar (2K22/VLS/05)** hereby certify that the work which is being presented in the thesis entitled "**Study And Implementation Of Power Reduction Techniques In Complex Circuit"** in partial fulfillment of the requirements for the award of the Degree of Master of Technology submitted in the Department of Electronics and Communication Engineering, Delhi Technological University is an authentic record of my own work carried out during the period from August 2022 to May 2024 under the supervision of Dr. Deva Nand.

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Certified that Farheen Safdar (2K22/VLS/05) has carried out their project work presented in this thesis entitled "**Study And Implementation Of Power Reduction Techniques In Complex Circuit"** for the award of **Master of Technology** from the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi under my supervision. The thesis embodies results of original work, and studies are carried out by the student herself and the contents of the thesis do not form the basis for the award of any other degree to the candidate or to anybody else from this or any other University/Institution.

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ABSTRACT

The sensing amplifier has become the focal point of memories and peripheral circuits. The increasing need for portable devices has posed a significant challenge for high-speed memories in terms of achieving longer battery life. SRAM, also known as static random-access memory, performs a crucial function in achieving lesser power and faster in performance in the era of digital technology and VLSI circuits. The present trend of nanoscale devices has caused an increase in sub-threshold leakage current in VLSI circuits. This is due to the continuous lowering in the threshold voltage and the thinning of the gate oxide, which enhances tunnelling leakage current and poses a problem. Reducing power consumption enhances the reliability and efficiency of a device. Consequently, CMOS innovation emerged as the most favoured choice for devices that require low power consumption. Therefore, leakage power reduction techniques have become a necessity for sustainment of this scaling in the VLSI circuits.

Memories created using CMOS includes sensing amplifiers. The stored data are retrieved via Sensing Amplifiers. The sensing amplifier (SA), which plays a critical role in the read circuitry of volatile and non-volatile memories, including FLASH, has a substantial impact on memory performance. The four main performance parameters for SA are physical footprint, power utilization, energy consumption, and access time. This thesis presents a redesigned design of a sense amplifier that incorporates several power reduction approaches into the "Conventional Charged Sense Amplifier (CSA)". The charged sense amplifier (CSA) is an essential element of SRAM and memory systems. In one of the publications, improved CSA has been proposed by implementing the Stacked transistor approach for leakage power reduction. Taking inspiration from the same, other conventional leakage power reduction techniques namely Galeor, Lector, Sleep transistor, Sleepy Keeper have been integrated in CSA. Apart

from leakage current reduction techniques, some of the other power reduction techniques proposed in different publications namely SAPON, Drain Gating, ECRL(Adiabatic), Isolated Sleepy keeper have been applied to the CSA. Their transient analysis has been done and a comparative study of power dissipated in each configuration has been presented.

The different configurations of CSA have been proposed and compared in this thesis, with each one being explained in some detail. The simulations have been carried out in LTSpice in 45 nm technology node and 1V power supply. The power is calculated at 0.9V for all the configurations. All the power reduction techniques have shown promising results, however some like SAPON and Sleepy keeper have led to extraordinary power reduction. As far as adiabatic techniques are concerned, only ECRL was analyzed as the area compensation is very large in Adiabatic techniques and has the potential to overshadow the power reduction benefits.

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LIST OF ABBREVIATIONS

S. No.	Abbreviation	Full Name
1.	CSA	Conventional Sense Amplifier
2.	VLSI	Very Large-Scale Integration
3.	GALEOR	Gated Leakage Transistor
4.	SAPON	Stackly Arranged low Power ON transistor
5.	SRAM	Static Random Access Memory
6.	CMOS	Complementary MOSFET
7.	ECRL	Efficient Charge Recovery Logic
8.	LCNT	Leakage Control NMOS Transistor
9.	DOIND	Domino logic with Clock and Input Dependent transistors
10.	VBODY	Body Voltage
11.	VTCMOS	Variable Threshold Conventional MOSFET
12.	SA	Sense Amplifier
13.	IVC	Input Vector Control
14.	IC	Integrated Circuit
15.	SRAM	Static Random Access Memory

CHAPTER 1

INTRODUCTION

In the electronics sector, consumption of low power has emerged as a critical theme. For the designing of chips in VLSI, managing power dissipated is now as crucial as speed and size. Shrinking technology and increased complexity below 100nm have made lowering power consumption and overall power management the primary issues. As a result, the research community is devoting considerable attention to ultra-low-power VLSI circuits, which are crucial to many current and future applications, such as wearable computing, smart grids, biomedical and implantable devices and networks.

One of the fundamental components in almost every integrated circuit is high-speed "SRAM." The sensing amplifier is particularly important among the peripheral circuits surrounding embedded SRAMs. The sense amplifier's ability to amplify small signals on large capacitive bitlines is closely tied to the access time of the SRAM. The SRAM typically consists of four or six transistors in a grid, each of which serves a vital function in the information processing.

The multiplexer of bitline and the interface of sense amplifier, two vital circuits, are primarily responsible for limiting the speed of an SRAM memory core. In addition to speed, low-leakage power and low noise margin in memory are critical considerations in SRAM design. The speed at which SRAM operates is one of the critical factors that necessitates the usage of sense amplifiers.

The increasing demand for lesser power and faster circuits in modern memory systems has led to renewed interest in sense amplifiers. Static random-access memory (SRAM) typically embeds faster memory, with data retention dependent on the application of power. The SOCs i.e. System on Chip frequently include Static RAMs which are integrated and used in

circuits for cache memory and latches, and caches are arrays of SRAM bit cells. However, the engagement between write and read equilibrium is a significant challenge in SRAM circuits. Research indicates that the cell ratio must balance read access and data change sensitivities. The increasing demand for low power, area, and delay in enhanced SRAM bit cells largely depends on sense amplifiers.

Sense amplifier's (SA) primary function is to read memory contents formed by CMOS and identify information stored in bit cell. Fast, lesser delay, and power reduction techniques, like adiabatic techniques and MTCMOS, VTCMOS can be essential to reduce the speed and power of SA.

High speed and low power in a small area are critical considerations for SRAM bit cells and SAs. Designing a SA with the minimum required number of transistors for a limited area can be a significantly challenging. To minimize power usage and delay of propagation, the bit lines' voltage swing must be kept below the supply voltage. The aspect ratio is another factor that affects the operational performance of the SA, particularly regarding voltage level sequencing. The W/L ratio of PMOS and NMOS transistors in Sense Amplifier should be appropriate as well as conventional. This analysis done dimensionally has been extensively studied over several years for practical pull-up and cell ratios.

In this report, several low power reduction strategies have been integrated in the conventional Charged sense amplifier (CSA), their transient analysis done and their performance in terms of power has been compared. In order to design this circuit, only one power supply has been used. A comparison has also been done with the already proposed "Improved CSA" that involves the Stacked transistor technique for leakage power reduction.

1.1 Motivation

The requirement for digital systems and electronic appliances is rising, necessitating suitable memory in electronic circuits to fulfill these requirements. CMOS memory circuits are widely known for their

authentication and are among the most prevalent in the VLSI design industry. Given that consumption of power is a primary issue in all fields, the priorities have shifted to circuits with less power consumption, fast i.e. less delay, less area and high energy efficiency.

The block of the sense amplifier plays a crucial role in determining the speed of the memory. The memory access is overseen by the sense amplifier, transforming the variations in voltage of the bit-line into the data of the output. The techniques to sense have undergone significant development, leading to memory circuits that are compact, faster, less power consumption, and efficient Advancements in sensing techniques have led to the development of memory circuits that possess the qualities of being compact, fast, energy-efficient, and highly effective. The requirement for reliable as well as mobile electronic devices in our day-to-day lives has spurred a great deal of research in low-voltage, low-power technologies, that may be be achieved by reduction of dimensions, modifying present topologies, and reducing the supply voltage.

Therefore, low-power as well as high-speed design techniques are highly desirable in modern technology. The usage of sense amplifier in circuit having memory is critical to reducing delay and power consumption and ensuring optimal functioning, performance, and durability. Since SRAM is a fundamental component of the sensing amplifier, it is necessary to develop an industry-standard sensing amplifier that can support traditional designs of the Static RAMs without having a negative impact on the applications of Static RAM.

At the end, this study presents a less power consuming circuit configuration of charged sense amplifier with fast and high energy efficiency while using a lesser supply voltage. The CSA configurations presented are composed of a modified CSA structure with an optimization between power and better performance.

1.2 Objective

Conducting a thorough evaluation of information allows for the

emergence of new questions, ideas, and insights. The major objective of this research is to uncover new avenues of possibility by delving into uncharted areas.

The fundamental goals of this thesis are outlined below:

- Analyze several sense amplifier configurations with similar technology nodes, power supply, and transient responses to identify the pattern of utilizing SA in low-power contexts.
- Perform a comparison between existing and modified SA structures to evaluate their performance and identify the best-performing circuit.
- Designing and analysis of a modified CSA (charged sense amplifier) structure that incorporates power reduction capabilities from various published works.
- Develop an updated and superior structure of a CSA that utilizes lesser power and energy efficient components for use in applications demanding low power.
- Compare several charged sensing amplifier configurations with the with the same W/L ratios, and similar technology node, to identify the best-performing design.
- Compare the performance of existing SA design to the modified SA design to improve performance.
- Improve speed and functionality by addressing significant capacitance on the bit-lines in modern memory systems.

1.3 Methodology:

The conventional charged sense amplifier is integrated with the generic leakage current reduction techniques like GALEOR (Gate LEakage transistor), Stacked, Sleepy transistor, Sleepy keeper, ONOFIC, Drain Gating, and Lector. Furthermore, various other power reduction techniques proposed in the publications like SAPON, Isolated Sleepy Keeper, ECRL,

LCNT etc. have been implemented in conventional CSA. All the configurations have been simulated in LTSpice in 45 nm technology node and 1V power supply. Transient analysis has been done for each of the configuration and the results in the already published works have been verified and the results of the modified designs show similar results in terms of transient response. The input power, clock power and total power of the configurations have also been measured and a comparative analysis has been put forth. Some of the configurations show tremendous reductions as far as power is concerned as compared to the conventional CSA with a nominal compensation of increase in area.

1.4 Thesis Organization:

There are 6 chapters in this thesis, beginning with the 1st Chapter that contains the introduction of the sense amplifier concept and covers the aim, motivation, approaches, and arrangement of this thesis. The 2nd Chapter discusses the reassessment of the literature and the technology gap, while Chapter 3 provides an overview of the power dissipation sources in circuits in VLSI. Chapter 4 presents conventional charged Sense amplifier (CSA) and power reduction techniques that have been integrated with the CSA in this thesis. Chapter 5 describes the comparative study of different configurations proposed and analyzed in this thesis. Finally, 6th Chapter offers the conclusive results and improvement scope for the future.

- CHAPTER 1- This chapter has introduction to SRAM and sense amplifiers, detailing their basic operation at lesser power and supply voltage. This also includes the aim of this study, its motivation, approach, and arrangement.
- CHAPTER 2- This chapter contains previous work done in domain in terms of sense amplifier, SRAM and different power reduction techniques introduced in the VLSI domain have been highlighted in this chapter. The technical gap existing in the previously proposed works and the ideologies presented in this thesis have been

mentioned explicitly.

- CHAPTER 3- The focus of this chapter is the various sources which lead to power dissipation in the circuits in VLSI. Brief description of dynamic, static, short circuit and leakage power have been provided. A generic idea of the possible reasons of these power expenditures have been established.
- CHAPTER 4- In the 4th chapter, firstly the conventional CSA is discussed. Further, the conventional leakage power reduction techniques integrated in the CSA are presented along with the Stacked CSA already proposed in previous work. Moving ahead, novel ideas presented in the previous publications have been integrated in the CSA. The descriptive analysis of the all the above along with the simulation results have been presented. The simulations contain transient responses, plots of input power, clock power and total power for each configuration. All the simulations have been performed in 45nm technology node using LTSpice.
- CHAPTER 5- This chapter mainly presents the comparative analysis of the various configurations that have been simulated. Data in tabular and graphical form has been demonstrated for the ease of comparison.
- CHAPTER 6- The 6th chapter consists of a summary of key findings and outcomes from each preceding chapter, as well as future directions for further study.

As a concluding step, a comprehensive list of references is provided to acknowledge and cite existing research that guided the direction of our current study.

CHAPTER 2

LITERATURE REVIEW

Literature review in this thesis aims to establish a foundation of knowledge about SRAM and sense amplifiers, identify areas of previous expertise, recognize contradictions and research gaps in past studies, and address technical gaps. In this chapter there's a division in 2 sections: (1) previously published works and (2) Gap in the technical arena. The review provides crucial context to the research problem and potential solutions.

2.1 PREVIOUS REPORTED WORK:

A. Prakash, S. Garg, N. Chauhan, D. Singh [1], Presented the method of designing and implementing an optimized pre-charged Sensing Amplifier (CSA) with low power capabilities by adding the Stacking Technique for leakage power reduction to the conventional CSA. The transient response of the differential outputs is also provided. Further, the power analysis demonstrates a reduction of 8% in the power of the "Stacked CSA" as compared to Conventional CSA.

D. Mittal [2], Proposed Leakage Power Reduction Methods for Static RAM Cell with Lesser Leakage in Cache Memories in which conventional leakage reduction techniques namely, Galeor, Lector, MTCMOS, Drain Gating and Sleepy Keeper are applied to the six Transistors SRAM cell. The Sleepy keeper transistor has improved static power and noise margin (NM) than the various configurations proposed in this paper.

S. Selvan, M. Bharathi [3], have provided a comparative study between multiple leakage power reduction methodologies for circuits consisting of CMOS, and have provided a comprehensive comparative analysis of CMOS circuits with circuit technique, Lector, DOIND, Sleepy transistors stacked

with Keep transistors, Sleepy transistors with Keeper, control system using VBODY and Stacked Sleep techniques, along with the merits and demerits of each configuration. Conclusions are: The Lector technique is well-suited for fast circuits for operations, while the control system using VBODY is appropriate for complex circuits with CMOS. Moreover, the DOIND approach is compatible to logic gates with domino approach.

C. Ganguly, M. Z. Meem, M. A. Faruque, et.al [4], Provided Comparative study of a Low-Power NOR Gate using Adiabatic techniques proposed in the paper, in which different Adiabatic techniques for power reduction has been integrated in the CMOS NOR Gate circuit and their results have been compared. The ECRL design proposed in this paper has been the motivation for applying the same technique in conventional CSA. Other adiabatic techniques demonstrated in this paper have not been implemented in CSA as the area compensation overshadows the power reduction benefits. A new architecture namely, LP PTM NOR gate has been proposed and found to be better in terms of power, energy dissipation, and propagation delay than other adiabatic techniques with the drawback of complex layout.

S. Banu, S. Gupta [5], Provided analysis of techniques for Leakage Reduction in Subthreshold region for Circuits with CMOS. This research publication delves into the comprehensive analysis of several power components, followed by an in-depth evaluation of different leakage power reduction techniques at the circuit level, including Dual Threshold transistors, Multiple Threshold CMOS, Variable Threshold CMOS, Dynamic Threshold CMOS, Transistor & pin restructuring, Input Vector Control (IVC), and Stacked Transistor techniques. Each technique's advantages and disadvantages are also discussed.

A. Kumari, V. Pandey [6], Explored Non-Dynamic Power Reduction Methods for VLSI Circuits in digital domain and proposed a new power reduction mechanism, Isolated Sleepy Keeper. The Isolated Sleepy Keeper method offers the ability to maintain the sleep mode state even when disturbances occur which is lacking in the conventional sleepy keeper or

sleep stack techniques. The proposed approach provides static power reduction while maintaining the logical state with minimum delay and a negligible increase in the required area.

N. Arumugam, M. S. Priya, S. Subramanian [7], Proposed SAPON approach: An innovative approach to designing VLSI circuits with reduced power consumption. This study investigates the origin of power consumption in both static and dynamic leakage power and introduces a novel approach called the SAPON (Stackly Arranged low Power ON transistor) technique to mitigate power consumption in circuits. The efficacy of the suggested SAPON methodology has been assessed in comparison to traditional methods such as LECTOR, LCNT, and Stacked ONOFIC, to ascertain its applicability in low-power VLSI. The findings suggest that SAPON exhibits lower power consumption in comparison to conventional reduction strategies.

A. Raghunath, S. Bathla [8], Analyzed and compared Reduction Techniques for VLSI Design targeted for leakage power, it was observed that LECTOR technique demonstrated better power dissipation compared to ONOFIC. However, when it comes to propagation delay, ONOFIC outperformed LECTOR. This may thus be used for less power, fast execution of VLSI circuit.

M. R. Islam, S. Karmaker, M. A. Ibtesham, I. Rahman [9], Proposed A Novel Low Power Single Bit SRAM Cell Using Quasi-Adiabatic Logic. The 6 Transistor SRAM cell has been modified and compared to other Adiabatic activity logic-based SRAMs. The comparison reveals that the suggested structure outperforms others in terms of the average power consumption of the SRAM. This report also presents the findings of the latency results for read and write operations.

G. Munirathnam, Y. M. M. Babu [10], Examination of Static Power Reduction Approaches in Deep Submicron CMOS Device Technology for Digital Circuitry has been done in terms of delay, number of transistors, PDP

and power consumption. To summarize this paper, the ICLRT (Input Controlled Leakage Restrain Transistor) methodology appears to be very practical for power dissipation in static mode, while the GALEOR technique is preferred for faster performance of the circuit.

2.2 TECHNICAL GAP

Upon careful observation and review of all the reported work, a technical gap has been identified. It is obvious that different techniques of reducing power have been proposed in previous works. Also, a wide range of publications have explored the possibility of improvements in the 6 Transistor Static RAM cell. Therefore, integration of proposed techniques with conventional CSA circuit is yet to be explored.

However, all the techniques are not feasible to be integrated in the CSA due to the architectural limitations. For instance, in the adiabatic logic, only ECRL has been used since using other methods would lead to increase in area by several folds such that it will overshadow the reduction in power. The overall objective of this thesis is aimed at providing alternative low power CSA configurations that can be used in modern day circuits. In some papers, Sleepy keeper showed the best reduction among others. However, after applying the other proposed methods, it has been found out that, there are other methods like Drain Gating and SAPON which show be results. There is a definite trade-off of area compensation to improve the power of the CSA. But, depending upon the applications, an appropriate technique for CSA can be chosen. The choice of CSA is eased by the comparative analysis provided in this thesis.

CHAPTER 3

POWER DISSIPATION SOURCES

Power dissipation is the measure of power that is released from a chip in the form of heat [2]. Power dissipation can be classified into four main categories:

- Static Power
- Dynamic Power
- Leakage Power Dissipation
- Short Circuit Power

$$P_{Total} = P_{dynamic} + P_{static} + P_{leakage} + P_{short} \quad (3.1)$$

Where, P_{total} is the complete average power.

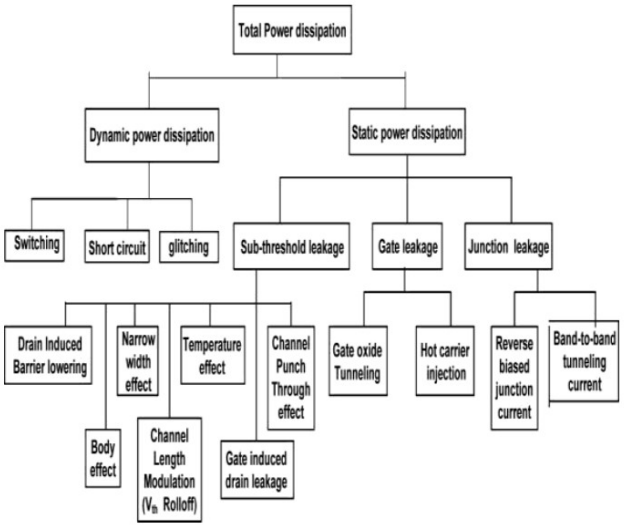

Figure 3.1 Power Dissipation Sources [2]

These power dissipation sources can be explained with respect to CMOS inverter circuit as demonstrated in the figure below.

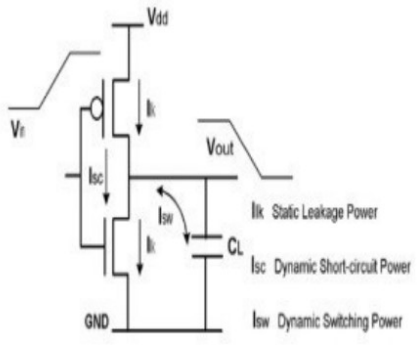

Figure 3.2 CMOS -Inverter Power Dissipation [2]

This chapter consists of four sections:

- In the first section, Static power dissipation has been discussed.
- Section 3.2 contains the Dynamic power dissipation.
- In Section 3.3, Leakage Power along with the leakage current sources have been discussed.
- Section 3.4 contains short circuit power dissipation.

3.1 Static Power

Static Power is the power that is dissipated when the device is in ideal condition. The possible sources of static power dissipation are: subthreshold current and reverse bias diode current. In an ideal situation, CMOS circuits would not consume any static (DC) power as there does not exist any direct connection from Vdd to GND in a stable state. However, due to imperfections in MOS transistors, this cannot be achieved in reality. As a result of currents due to leakage and substrate injection, there'll always be a static power dissipation in CMOS. If we consider a NMOS device in sub-micron region having effective W/L ratio of 10/0.5, the current due to substrate injection remains within the range of 1 to 100 micron Amps when V_{dd} is 5V. Since gate voltages are transient and are in the range of 0.4Vdd for a brief time during device switching, the substrate current reaches its maximum. However, when compared to other contributors, the power caused by current due to substrate injection is much smaller. Similarly,

CMOS structure consists of parasitic diodes that lead to reverse-bias junction leakage currents in the order of nA, which has minimal influence on the total power utilization [11].

$$P_{static} = V_{dd}. I_{static} \quad (3.2)$$

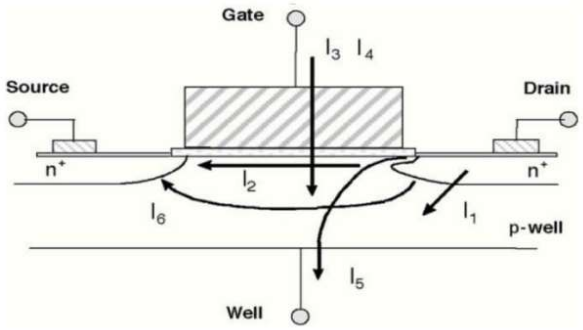

Figure 3.3 Static Power Dissipation in Transistor [11]

The above figure represents different currents that flow in a P-N junction under different conditions - I_1 denotes the leakage current under reverse bias, I_2 represents leakage current due to sub-threshold, I_3 corresponds to current due to oxide tunneling, I_4 represents current from gate terminal, I_5 denotes current due to drain leakage induced by the gate terminal, and I_6 corresponds to current due punch-through in the channel.

3.2 Dynamic Power

Dynamic power is the power that is released from a circuit during the process of charging and discharging. Power dissipation can be classified into three categories: switching power, short circuit power, and glitch power dissipation [7].

$$P_{dynamic} = \alpha C V_{dd}^2 f \quad (3.3)$$

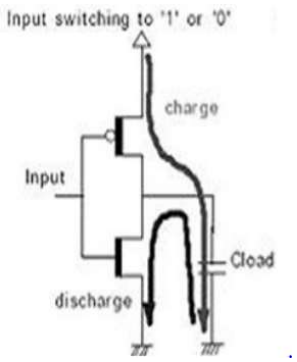

Figure 3.4 Dynamic Power Dissipated in inverter [11]

3.3 Short Circuit Power

Static power dissipation is the term used to describe the power that is dissipated from a circuit when it is in an ideal state. To calculate this, one must consider the sub-threshold and reverse biased diode discharge current. Short circuit power can be estimated using the following equation:

$$P_{Static} = I_{Static} * V_{DD} \quad (3.4)$$

Where V_{DD} = Voltage of Power Supply, I_{Short} = Short Circuit Current, P_{Short} = Static Power.

3.4 Leakage Power Dissipation

This power consumption that occurs when a circuit is in standby mode is known as leakage power dissipation. Various strategies employed in VLSI design to tackle this problem include sub-threshold (weak inversion) leakage, gate-induced drain leakage, and reverse-biased junction leakage current. Sub-threshold leakage current is the power that flows from the source (VS) to the drain terminal (VD) when the voltage at the gate terminal (VG) is lower than the threshold voltage (VT) [7]. This current can be mathematically represented using the following equation:

$$I_{sub} = K_1 W e^{-Vth/nV_\theta} (1-e^{-V/V_\theta}) \quad (3.5)$$

Where I_{sub} = Leakage current in subthreshold region; n, K_1 are the values found out by experiments; W= Width of the transistor; V_θ = transistor Thermal voltage; V_{th} = transistor threshold voltage

CHAPTER 4

CONVENTIONAL CSA AND MODIFIED CSA USING POWER REDUCTION TECHNIQUES

4.1 Conventional Charged Sense Amplifiers (CSA)

Almost all integrated circuits today rely on high-speed SRAM as a fundamental component. Sensing amplifiers are a crucial peripheral circuit in embedded systems that can impact the access time of SRAM by amplifying small signals on capacitive bit lines. The processing of information in SRAM depends on the function of four to six transistors. The bit line multiplexer and sense amplifier interface are essential circuits in SRAM's memory core. Meeting low leakage power and noise margin requirements is crucial for SRAM design. The operational speed of SRAM necessitates the usage of sense amplifiers, making them a critical factor. To create low-power, low-voltage integrated circuits, a common technique is Vth scaling, which involves lowering the Vth along with the supply voltage. One vital factor that enables high-speed SRAM is the sense amplifier, which has two phases - reset and active. The clock is active low in reset phase, and in active phase, it is active high [3].

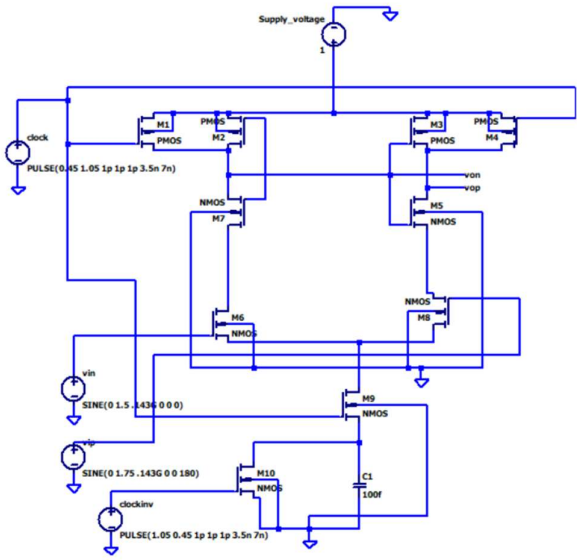

Figure 4.1 Conventional Charged Sense Amplifier

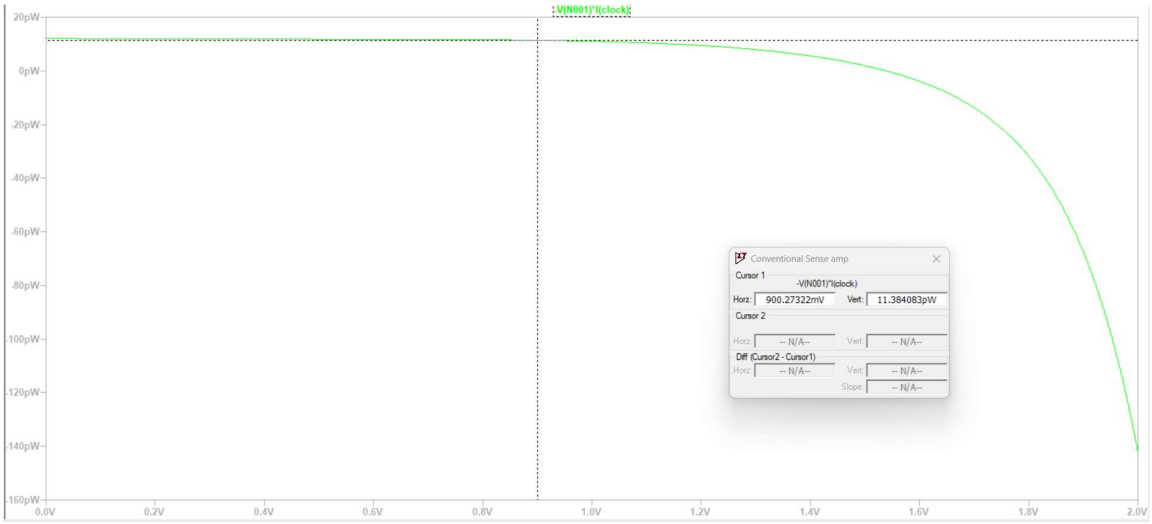

Fig 4.2 Power consumption by input clock (conventional CSA) at Supply voltage = 0.9V is 11.38pW

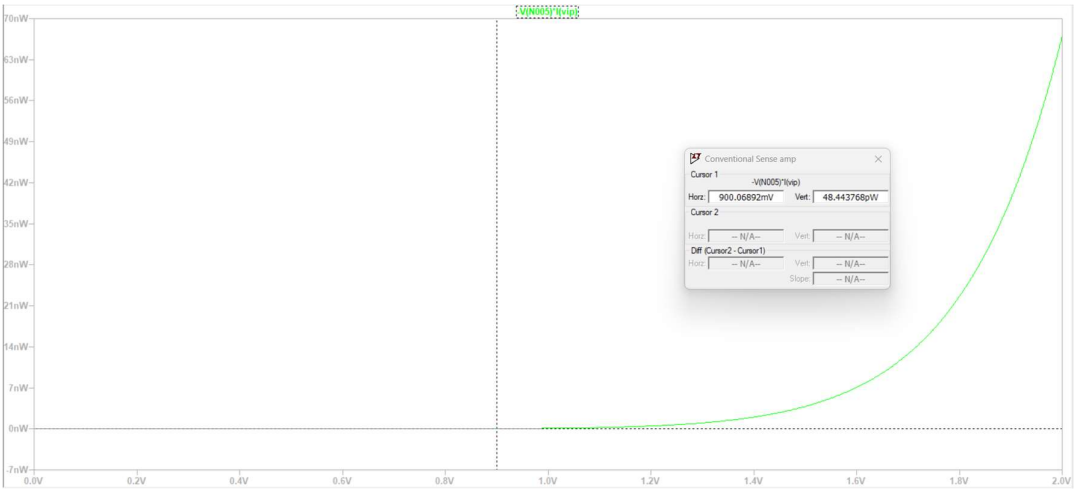

Fig 4.3 Power consumption of input Vip for Conventional CSA for input = 0.9V is 48.44pW

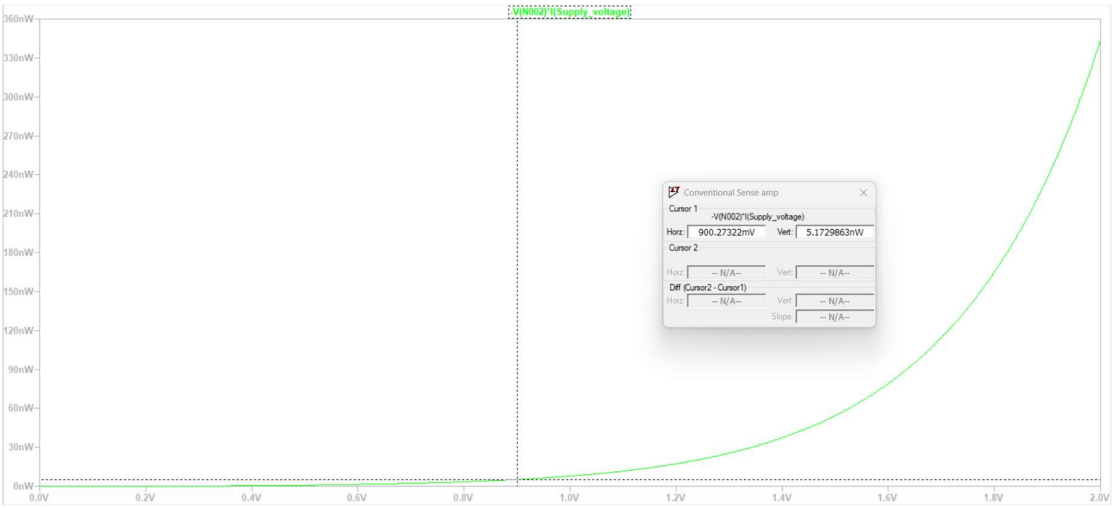

Fig 4.4 Total power consumption by Conventional CSA at Supply voltage = 0.9 V is 5.17nW

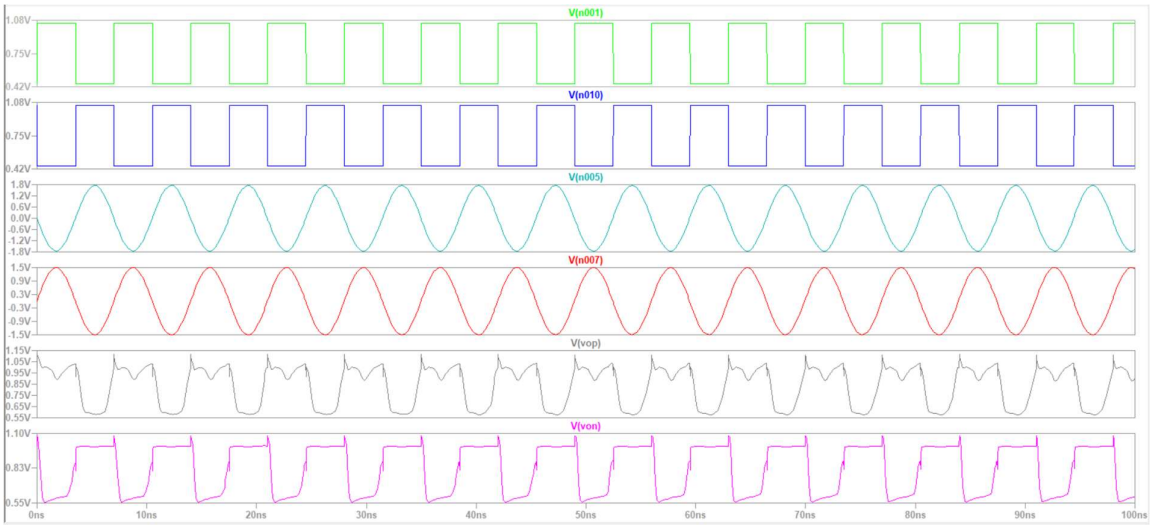

Fig 4.5 Transient Analysis of Traditional CSA

4.2 Stacked CSA

Transistor stacking is a method used to reduce the quantity of leakage power in the active mode. The reduction in leakage current that happens when several transistors in a series are switched off is known as the stack effect, also known as the self-reverse bias effect. In a stack construction, more transistors can be added to save even more leakage power. Forced stacking is a workaround for circuits without a stacking structure. When two transistors of width "W/2" are used in place of one single transistor, the leakage current is reduced when both transistors turn off simultaneously. The ratio of the leakage current in a stack of two or more off devices to the leakage voltage is known as the stack effect factor [3]. In the active state, this technique is used to lower outflow power usage. The outflow current drops when two or more series transistors are turned off. The weak inversion current's reliance is exploited by the electronic transistor stacking effect, which causes the sub-threshold outflow current to decrease exponentially with an increase in supply voltage. There may be a greater outflow of power savings when a stack structure has more transistors. A method known as forced stacking [4].

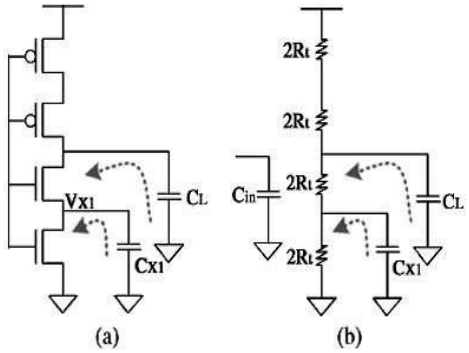

Fig 4.6 Forced Stacked Technique [4]

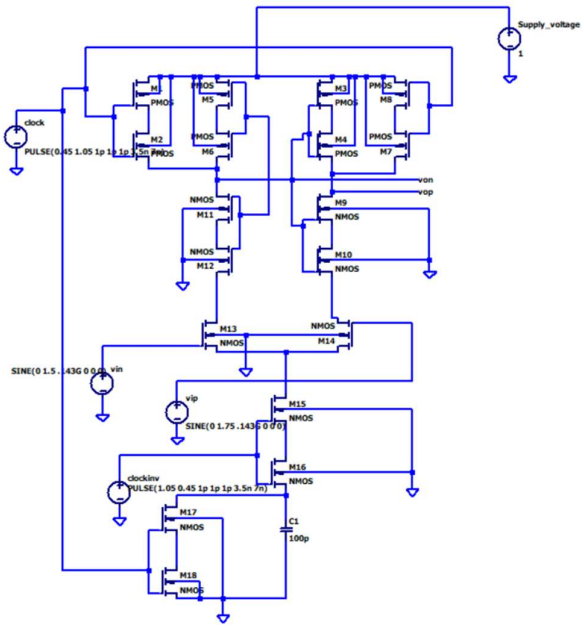

Figure 4.7 Stacked CSA

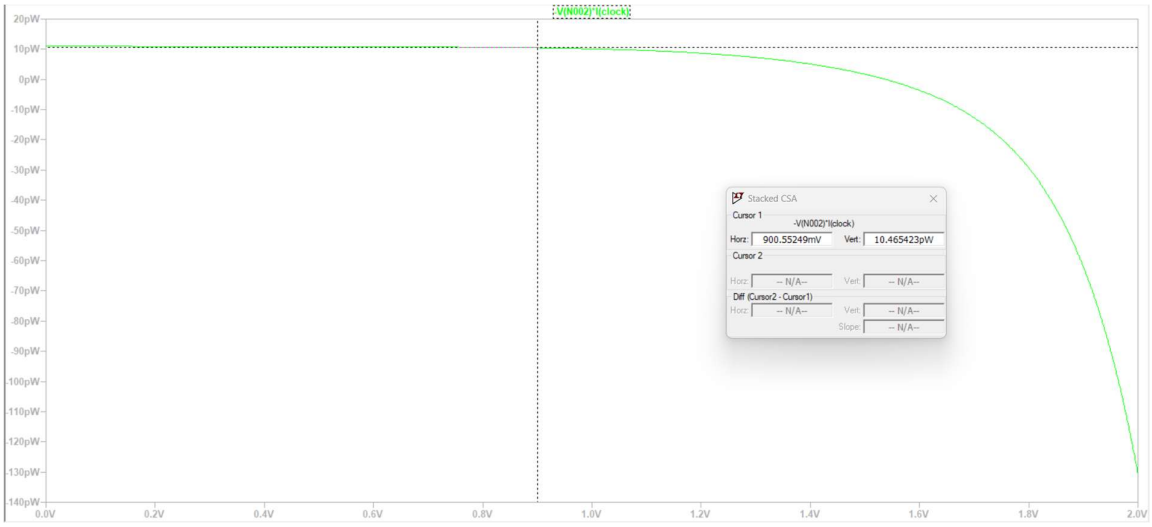

Figure 4.8 Power consumption by input clock (Stacked CSA) at Supply voltage = 0.9V is 10.46pW

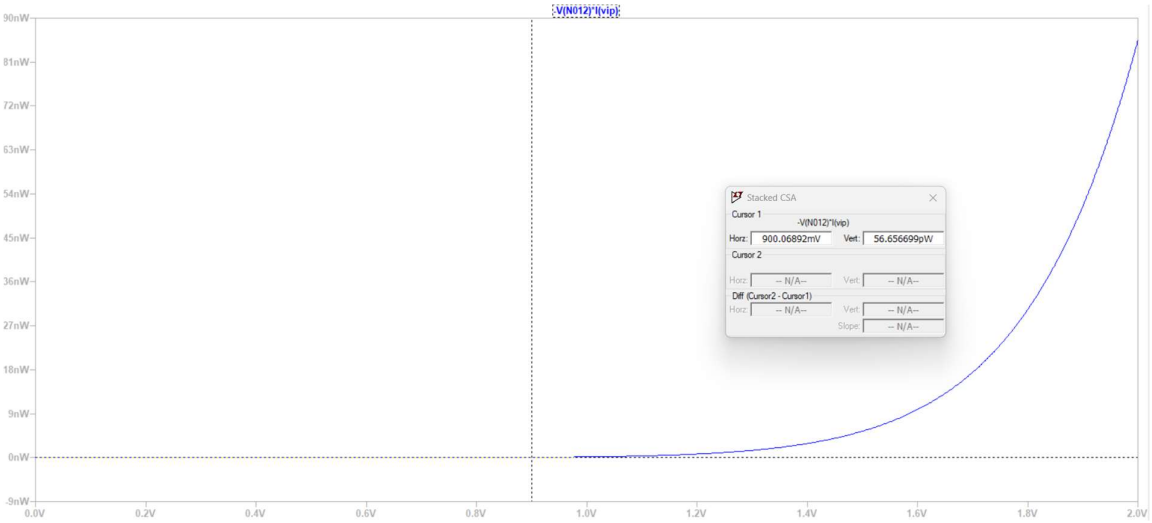

Figure 4.9 Power consumption of input Vip for Stacked CSA for input = 0.9V is 56.65pW

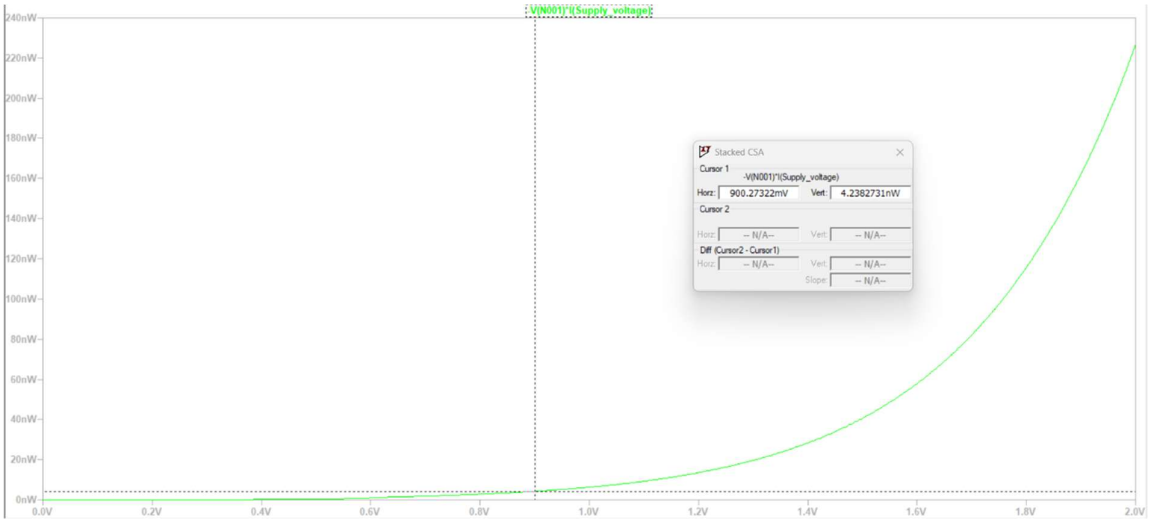

Figure 4.10 Total power consumption by Stacked CSA at Supply voltage = 0.9 V is 4.23nW

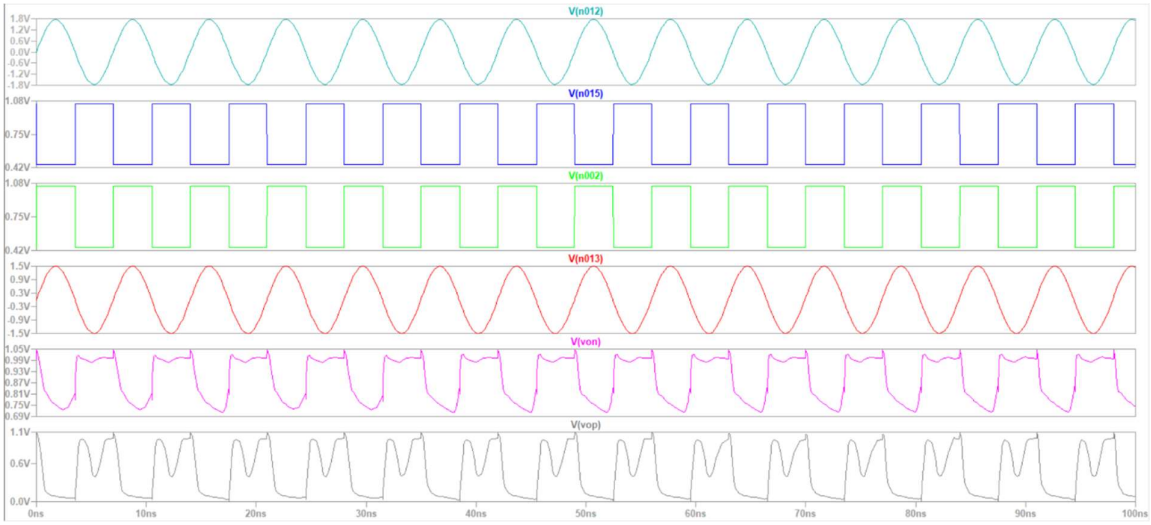

Fig 4.11 Transient Response of Stacked CSA

4.3 Lector CSA

There are two leakage control transistors in the Lector method logic circuit, one of which is getting close to cut-off. Because of leakage, this configuration significantly reduces current by raising the route resistance from source to ground [12]. This method works well in standby as well as active modes. The transistor drains are combined to generate an output because of the way the structure is connected. The circuit's logic part is

coupled to the transistor supply. The voltage potentials at each transistor's node regulate the transistors. Two more transistors, LCT1 and LCT2 (Leakage Controlled Transistor - PMOS, NMOS), are introduced into the circuit between the PUN and PDN networks in order to use this technique. The output is created by combining the LCTs' drain terminals. No matter what inputs are applied, one LCT is always under cutoff because its gate terminals are connected to its source. Low leakage is produced by this configuration's high resistance path from Vdd to Gnd. But as technology advances, this configuration experiences problems with signal quality [16].

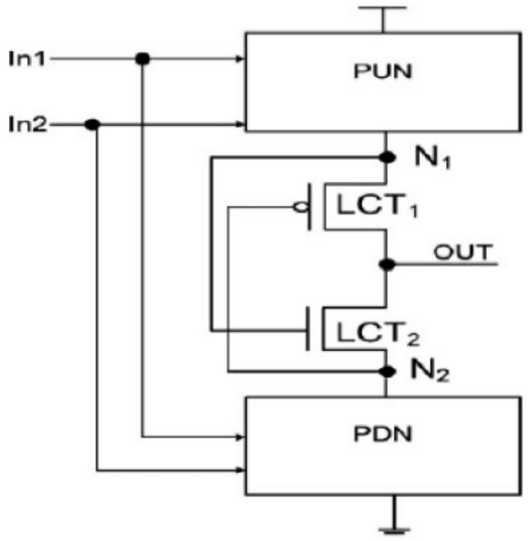

Figure 4.12 Lector Technique [16]

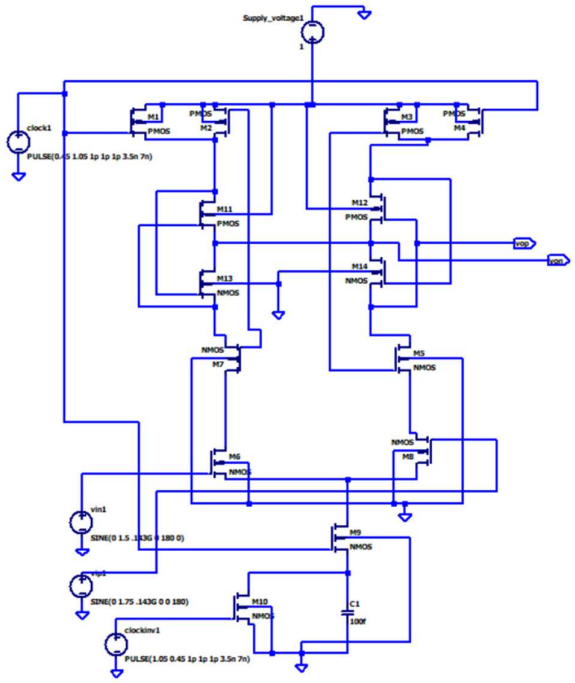

Fig 4.13 Lector Technique CSA

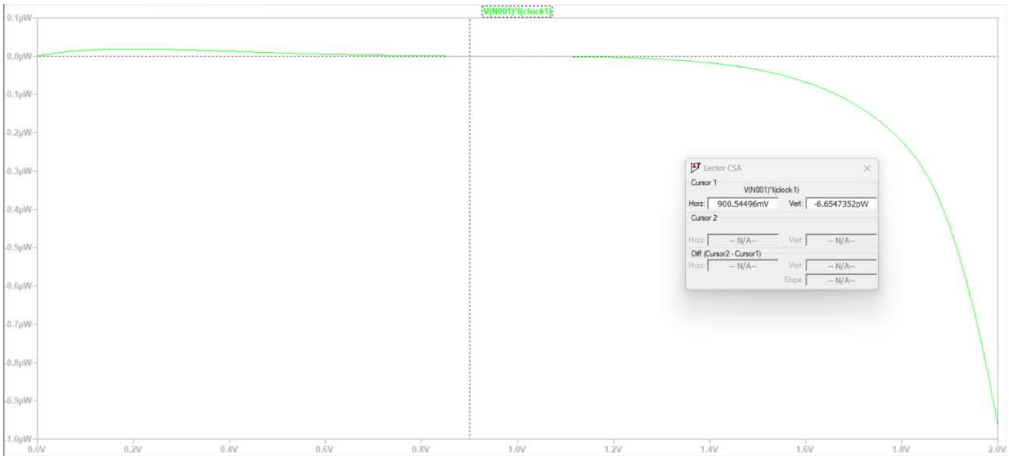

Fig 4.14 Power consumption by input clock (Lector CSA) at Supply voltage = 0.9V is 6.6547352pW.

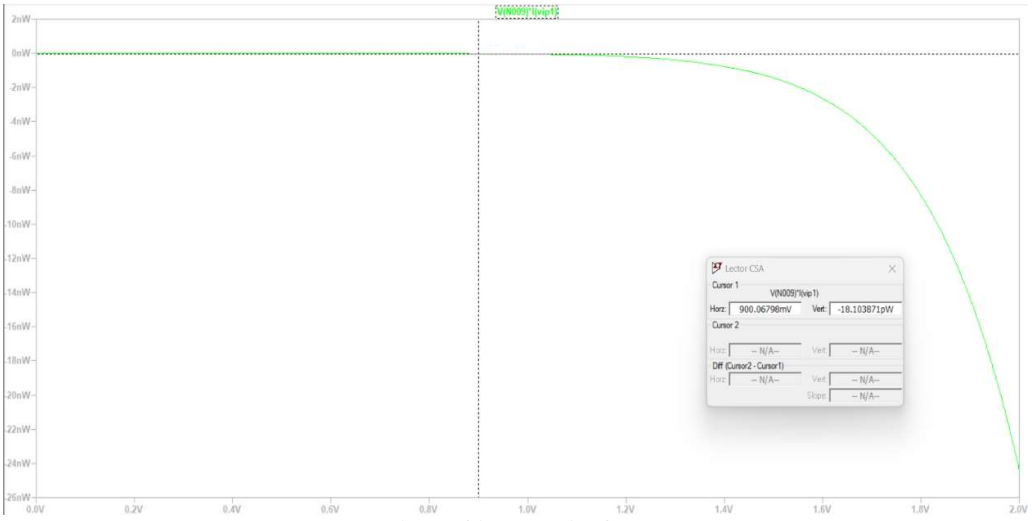

Fig 4.15 Power consumption of input Vip for Lector CSA

for input = 0.9V is 18.103871pW.

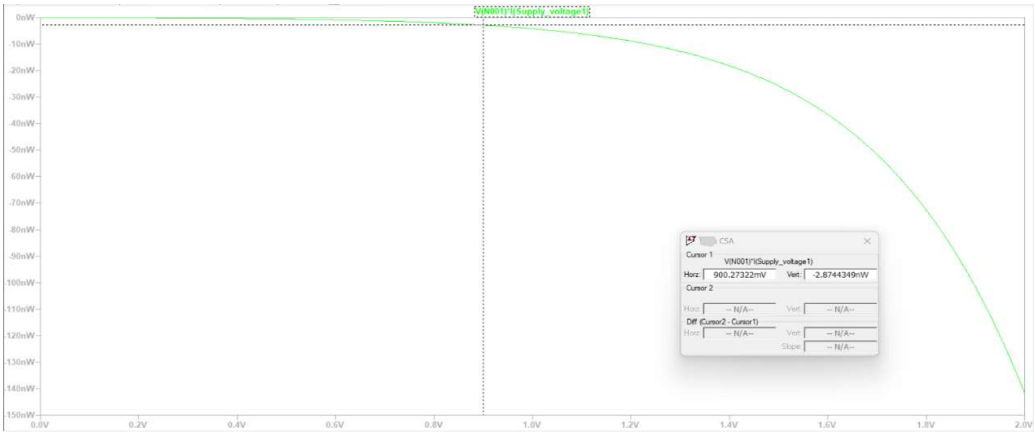

Fig 4.16 Total power consumption by Lector CSA at

Supply voltage = 0.9 V is 2.8744349nW

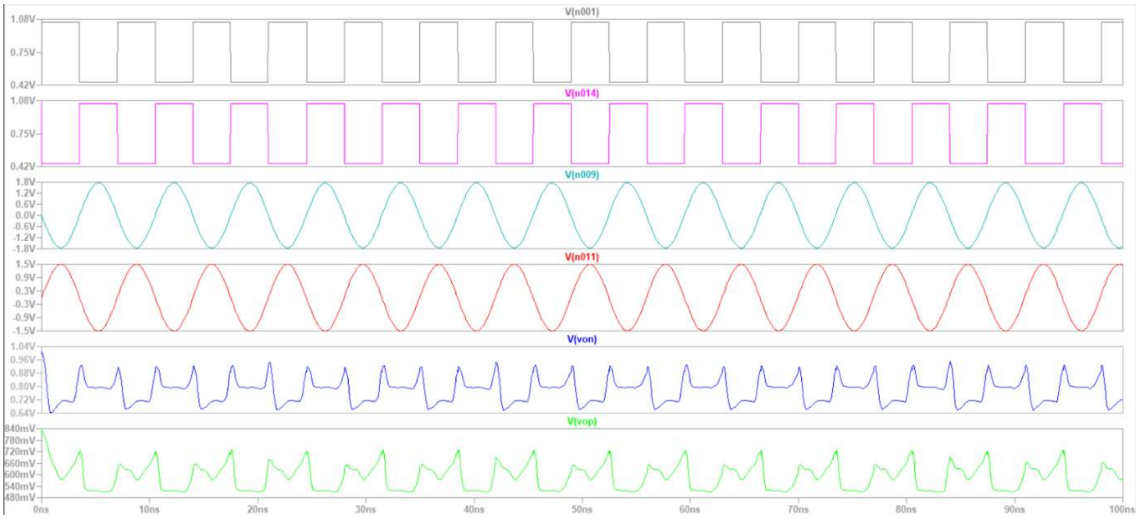

Fig 4.17 Transient Response of Lector CSA

4.4 Galeor CSA

While GALEOR's self-controlled approach is similar to LECTOR's, it is limited to one Vth rise in the logic low output and one Vth drop in the logic high output. The circuit and implementation of the CSVCO/NAND gate Two high voltage transistors are included in the pull-up and pull-down network using the Galeor approach. By shorting their gates to their self-source terminals, these transistors prevent leakage by forming a stack. But this also lengthens the output voltage delay and lowers the threshold voltage [11]. This circuit makes use of the GLT1-NMOS and GLT2-PMOS gated leakage transistors. They are placed, in turn, along PDN and output and PUN and output. Comparable to LECTOR, but with the transistors reversed, is this design. Because one of the GLTs is constantly close to its cut-off, which lowers the leakage current, both GLTs are high threshold voltage devices that guarantee strong resistance between V_{dd} and Gnd. Because the high logic level will be far lower than the supply voltage and the low logic level will be much higher than 0V, this might potentially cause problems with signal quality during scaling [16].

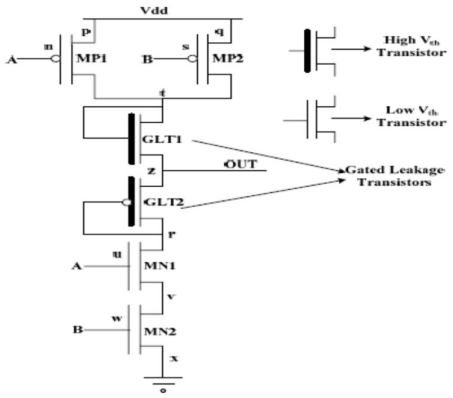

Fig 4.18 GALEOR Technique [11]

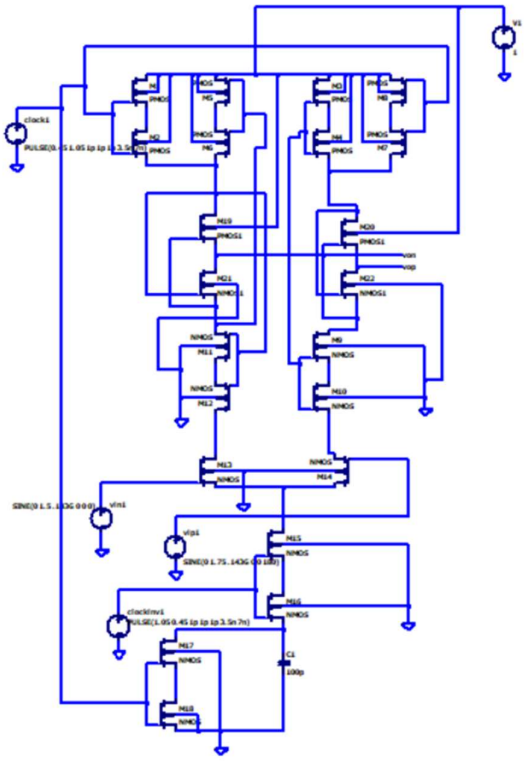

Fig 4.19 Galeor Technique CSA

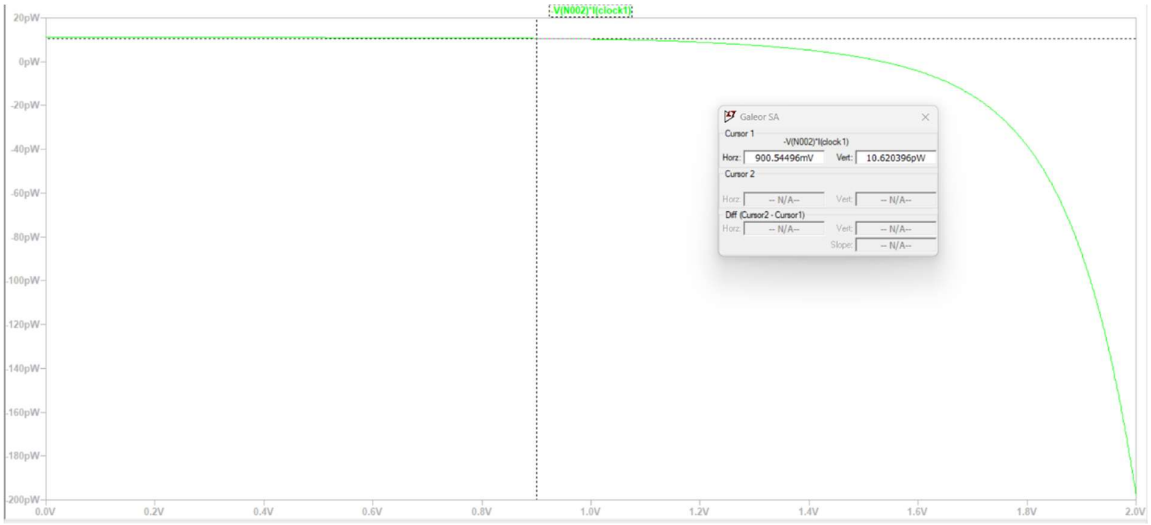

Fig 4.20 Power consumption by input clock (Galeor CSA) at Supply voltage = 0.9V is 10.62pW

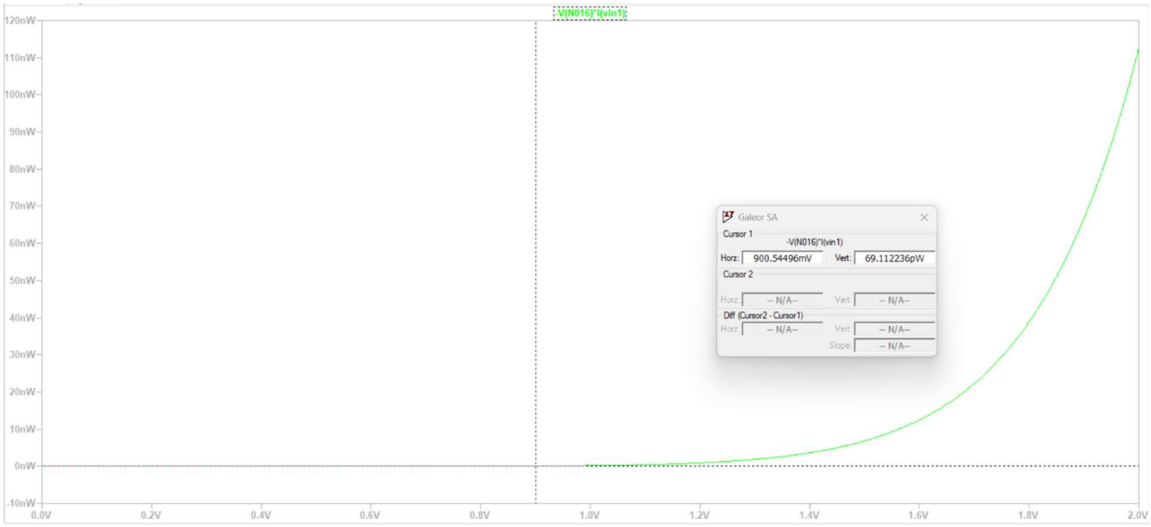

Fig 4.21 Power consumption of input Vin for Galeor CSA for input = 0.9V is 69.11pW

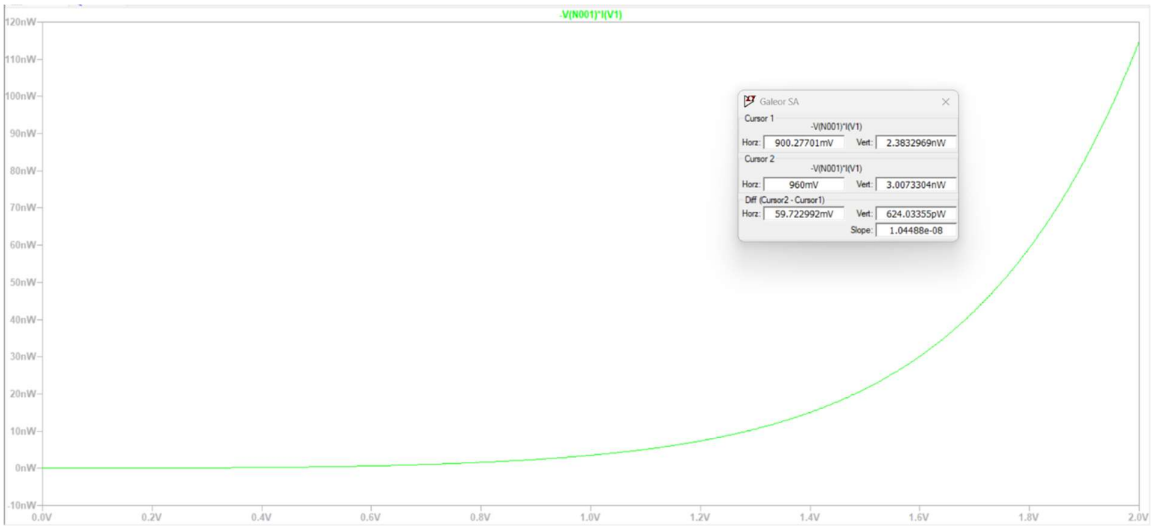

Fig 4.22 Total power consumption by Galeor CSA at Supply voltage = 0.9 V is 2.36nW

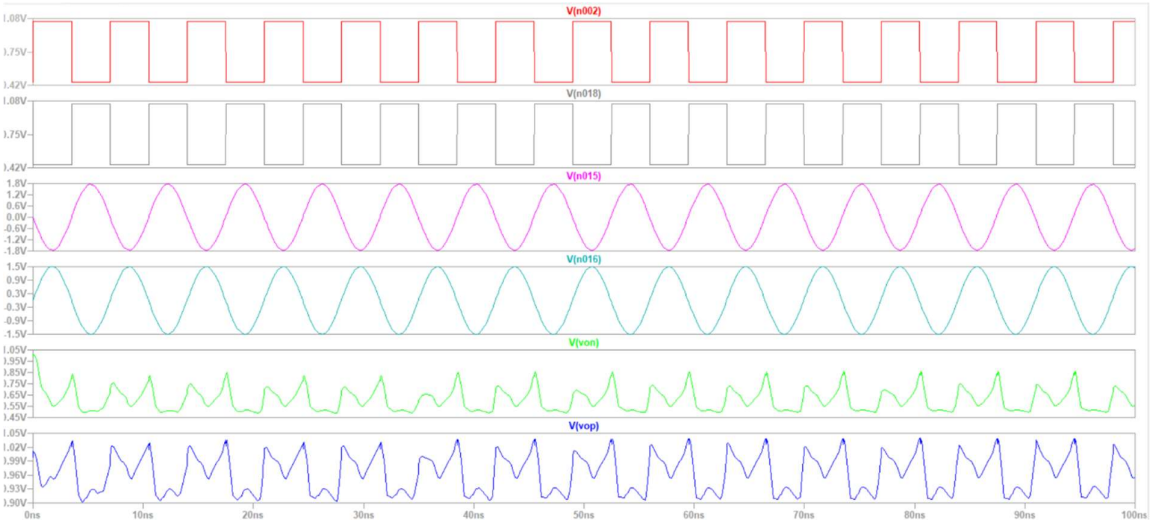

Fig 4.23 Transient Response of Galeor CSA

4.5 Sleepy CSA

The sleep approach is employed to mitigate sub-threshold leakages by interconnecting either PMOS or NMOS transistors, known as sleep transistors. Delay stages are specifically designed to function in either the sleep (sometimes referred to as standby) mode or the active mode. In sleep mode, the sleep transistors are deactivated, resulting in a reduction in leakages. This approach utilizes two sleep transistors, namely PMOS and

NMOS, which possess high threshold voltages. These transistors are interconnected as depicted in the diagram below. During active mode operation, the Sleep signal is set to logic-1 and the slab signal is set to logic-0 state. As a result, the voltage at VP is lower than the voltage at VDD, while the voltage at VG is higher than the ground (GND) terminal. Consequently, the amount of power passing through the inverter circuit is decreased, resulting in a reduction in power dissipation. However, in standby operation, Transistors M3 and M4 are deactivated, causing a high impedance between VP and VG. As a result, the power dissipation from the circuit is reduced [7].

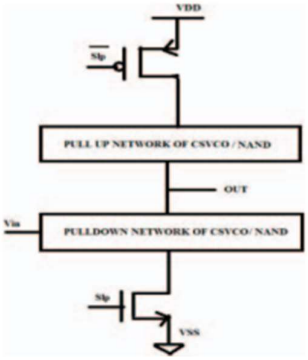

Figure 4.24 Sleep Technique

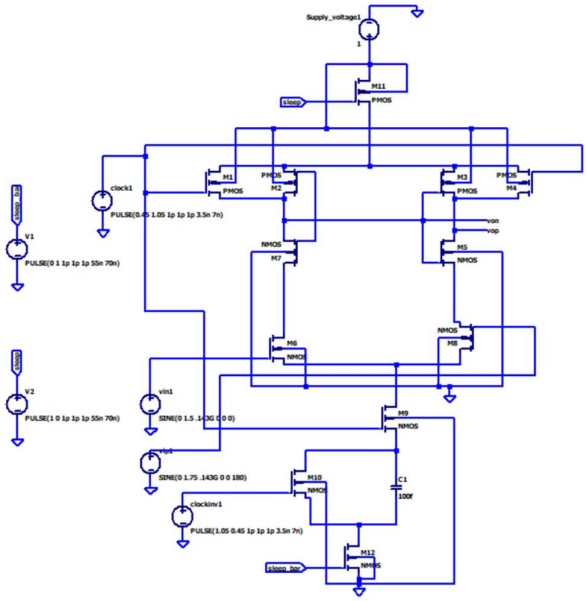

Fig 4.25 Sleepy CSA [7]

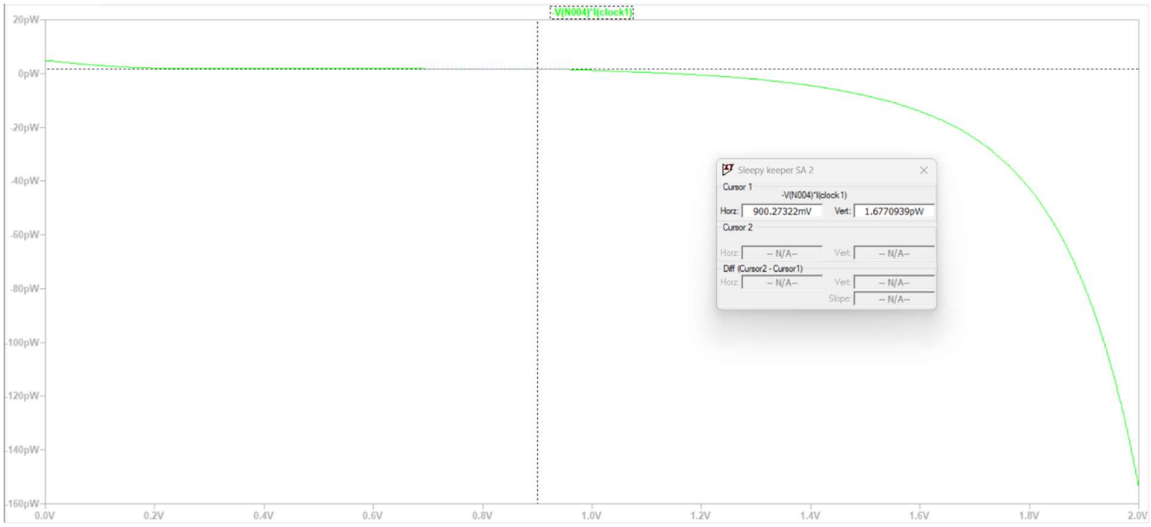

Fig 4.26 Power consumption by input clock (Sleepy CSA) at Supply voltage = 0.9V is 1.67pW

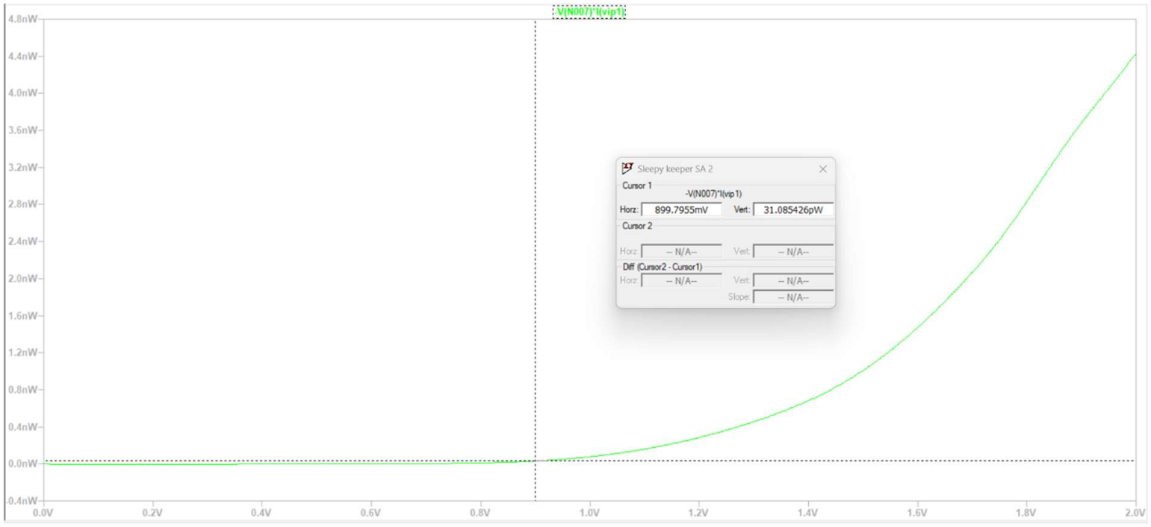

Fig 4.27 Power consumption of input Vip for Sleepy CSA for input = 0.9V is 31.08pW

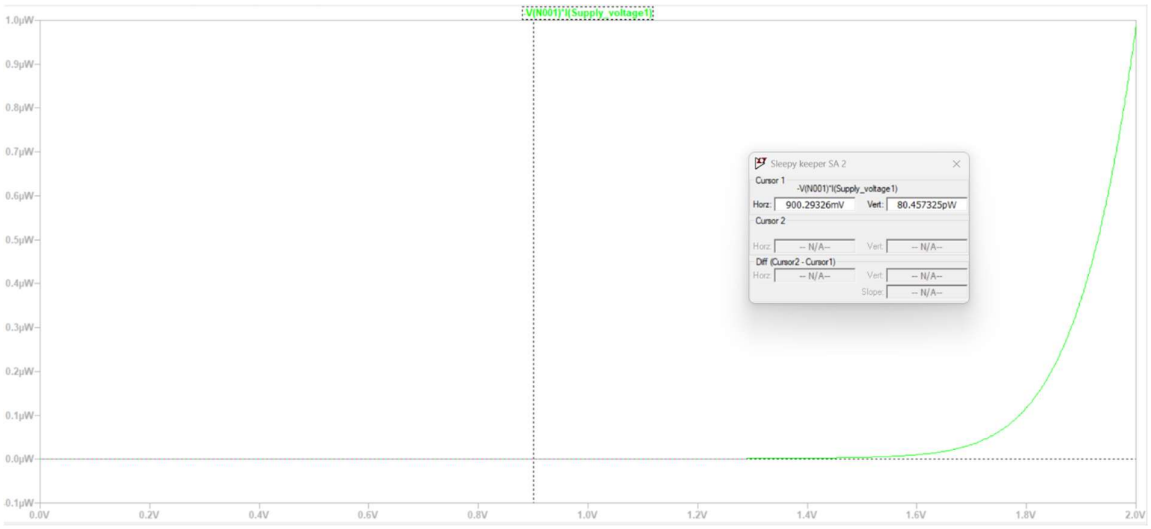

Fig 4.28 Total power consumption by Sleepy CSA at Supply voltage = 0.9 V is 80.45pW

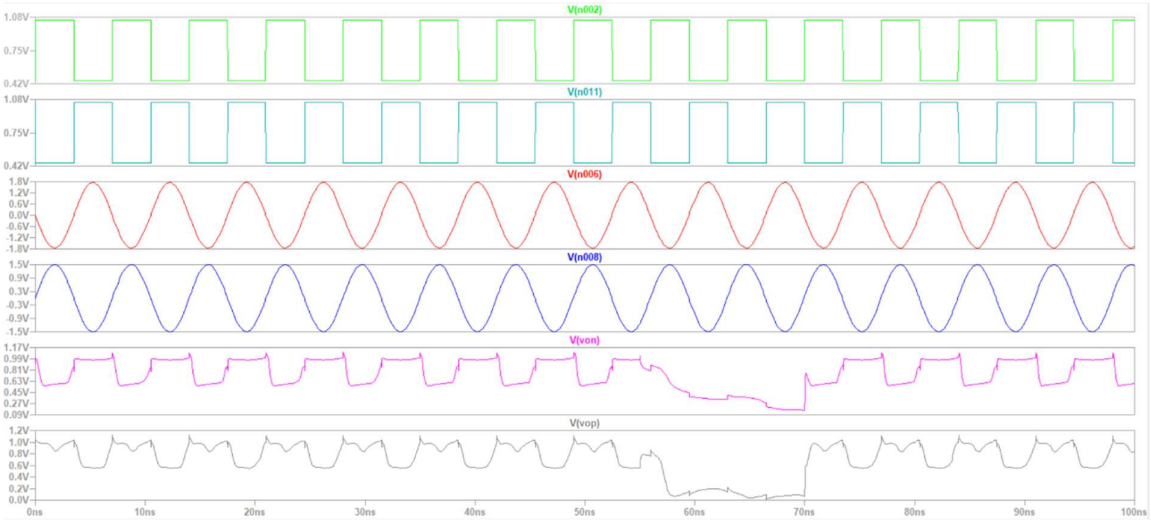

Fig 4.29 Transient Response of Sleepy CSA

4.6 Sleepy Keeper CSA

The Sleepy keeper technique is an enhanced version of the sleepy transistor technique that includes 2 additional transistors. First is a P-type MOSFET that is placed in parallel to the transistor at the foot with one of the terminals attached to GND, and the second is an N-type MOSFET that is placed in a parallel manner to the transistor at the head with one of the terminals at power supply V_{dd}. These extra transistors, commonly called

keeper transistors, are used to address the output that floating issue that is a major demerit of the prior sleepy transistor approach. The keep transistor's input is the output received from the central circuit [13]. The Sleepy keeper technique uses a sleepy transistor and single keep transistor positioned above the pull-up Positive MOS network and below the pull-down Negative MOS network. This approach can overcome the area consumption of the sleep stack method. The circuit can be used in inactive mode based on the sleepy input of the sleepy mode transistor or based on the keep transistor [1]. The state of the output can be preserved by the keep transistor when the sleepy transistor is not turned on. In this technique, sleep transistors are employed to put off the power supply voltage (V_{dd}) during sleep mode, effectively reducing power due to leakage current. These sleepy transistors automatically turn off at the time of sleep. In addition to the sleep transistors, two other keeper transistors are also utilized [19].

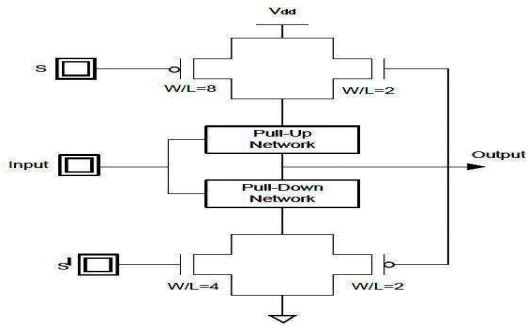

Fig 4.30 Sleepy Keeper Approach [1]

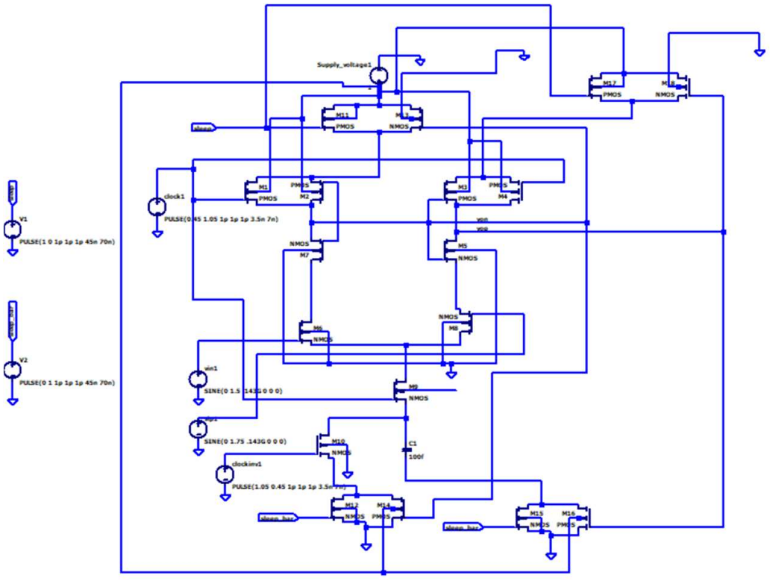

Fig 4.31 Sleepy Keeper CSA

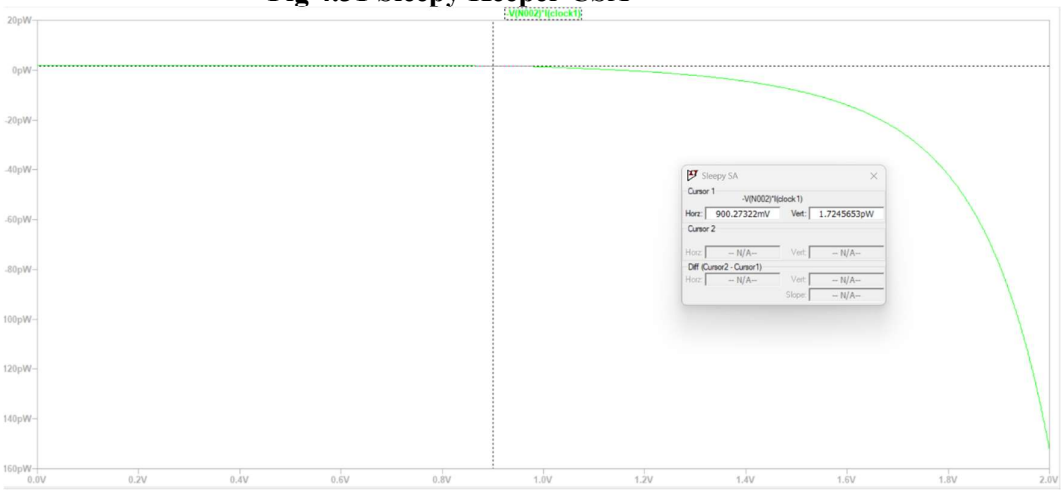

Fig 4.32 Power consumption by input clock (Sleepy Keeper CSA) at Supply voltage = 0.9V is 1.72pW

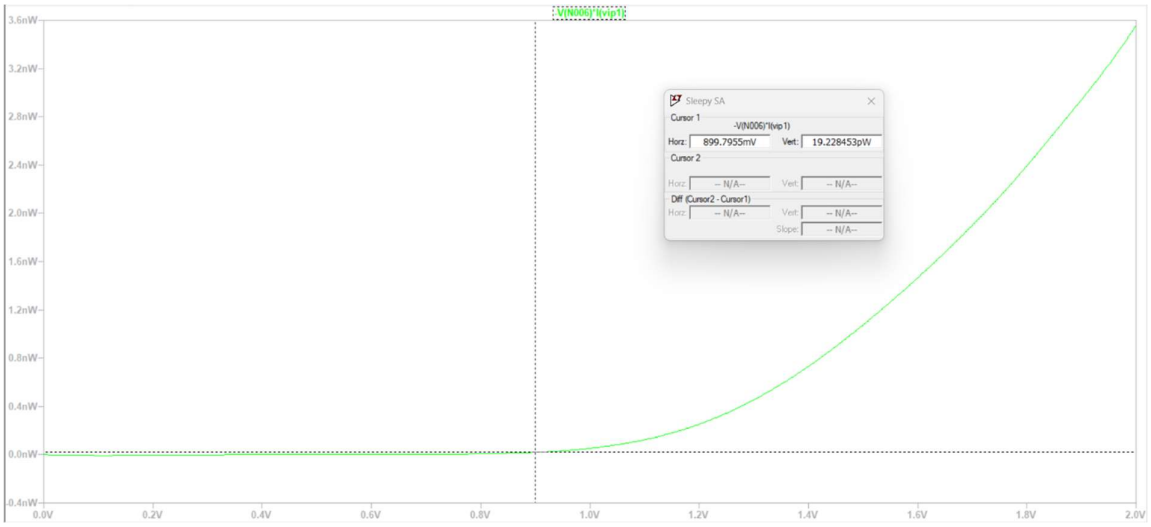

Fig 4.33 Power consumption of input Vip for Sleepy Keeper CSA for input = 0.9V is 19.22pW

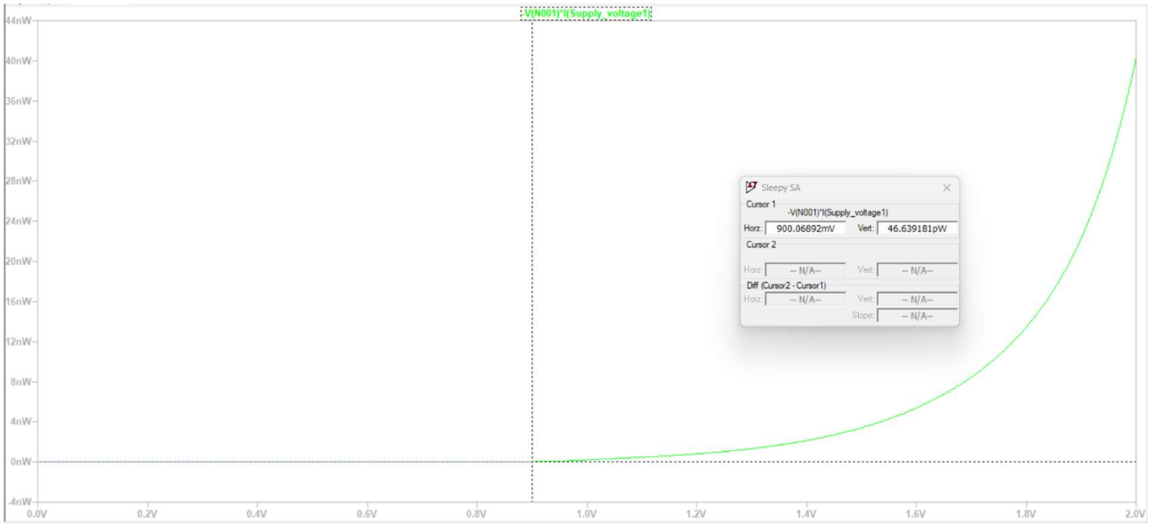

Fig 4.34 Total power consumption by Sleepy Keeper CSA at Supply voltage = 0.9 V is 46.63pW

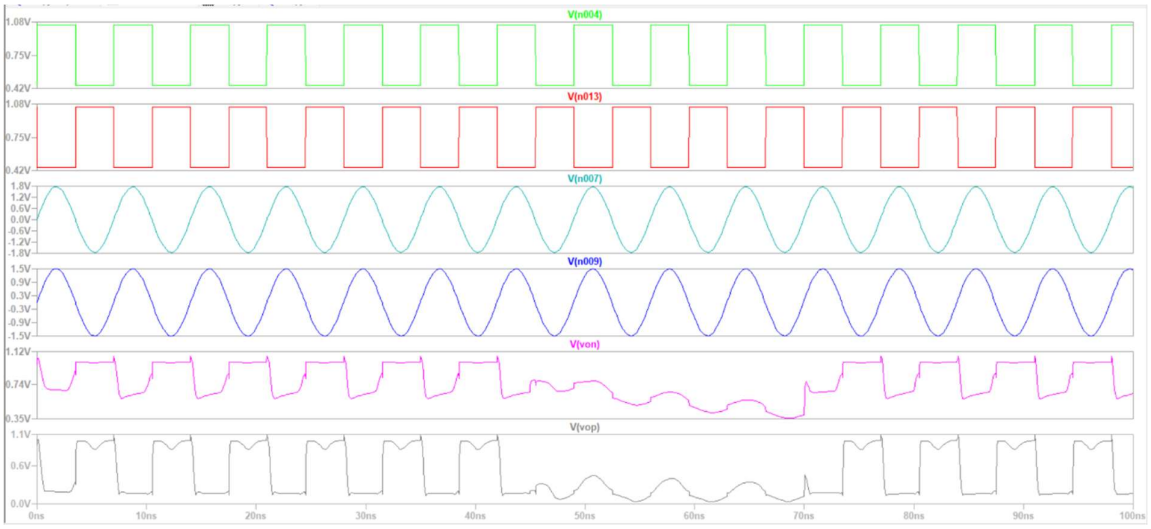

Fig 4.35 Transient Response of Sleepy Keeper CSA

4.7 Drain Gating CSA

This can be achieved by introducing transistors that sleep occasionally between the positive MOSFET and negative MOSFTET networks. S which is the transistor which goes to sleep mode is placed between the pull-up network and the output, while another transistor 'Sbar' which also sleeps occasionally is positioned amidst the pull-down circuit and the output. When employing the sleep mechanism, the transistors which sometimes enter sleep mode are deactivated, resulting in a stacked structure that causes the resistance between power supply line and ground to be increased, thus reducing the current due to leakage. Conversely, during the normally activated state, the transistors that can potentially enter sleep state at times, are active to provide an additional state of logic. However, one demerit of this method is the necessity for an additional controlling signal to manage the transistors that can enter sleep mode [16].

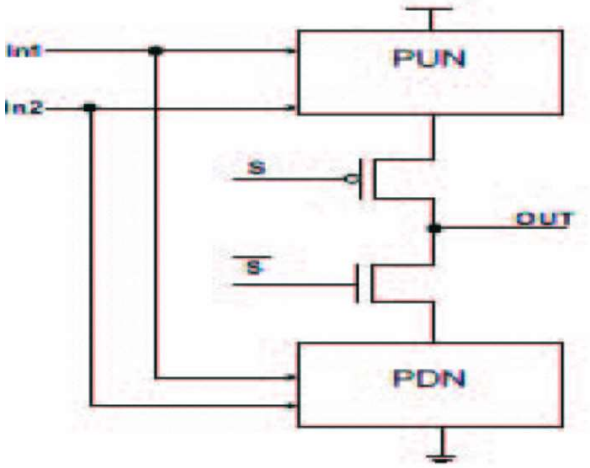

Fig 4.36 Drain Gating Technique [16]

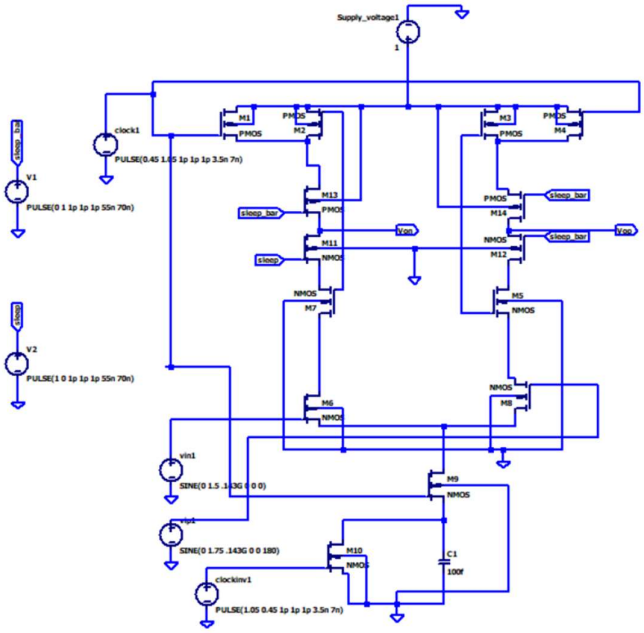

Fig 4.37 Drain Gating CSA

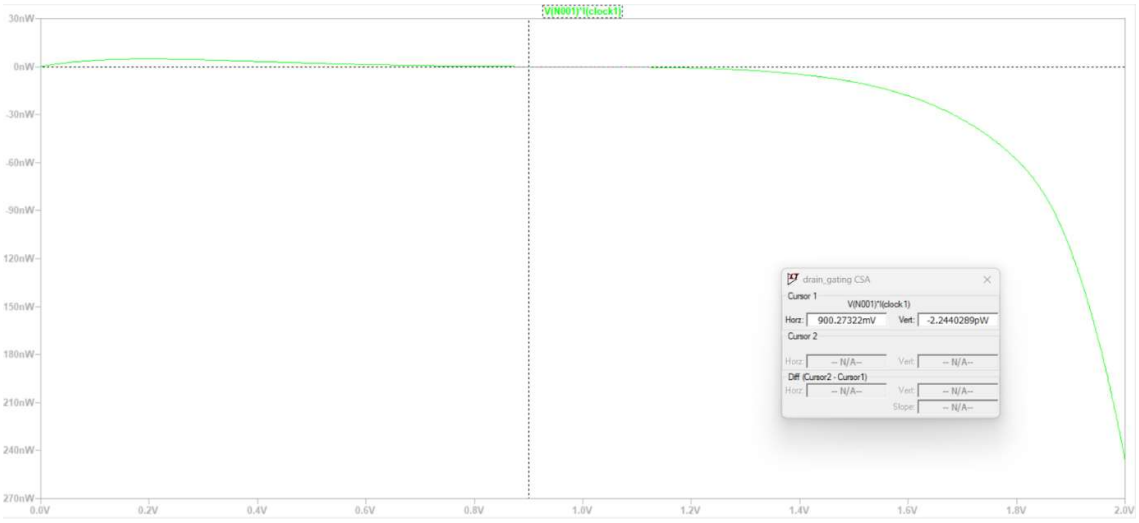

Fig 4.38 Power consumption by input clock (Drain Gating CSA) at Supply voltage = 0.9V is 2.2440289pW

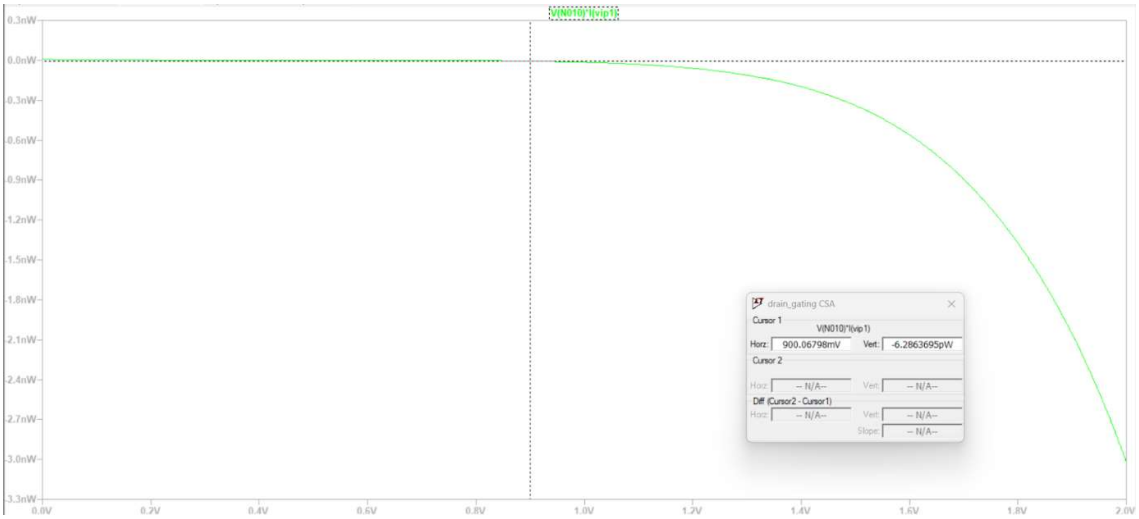

Fig 4.39 Power consumption of input Vip for Drain Gating CSA for input = 0.9V is 6.2863695pW

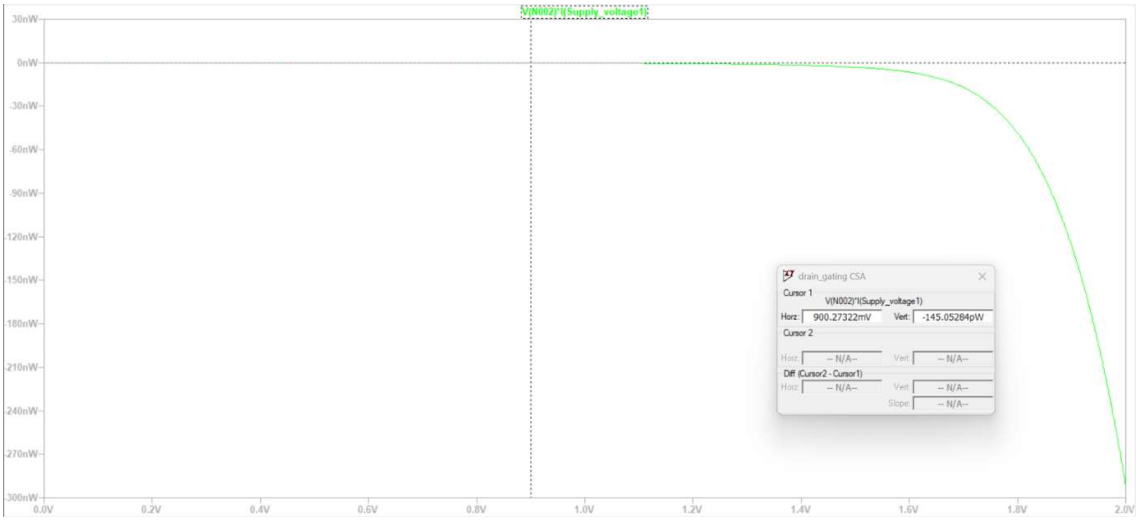

Fig 4.40 Total power consumption by Drain Gating CSA at Supply voltage = 0.9 V is 145.05284pW

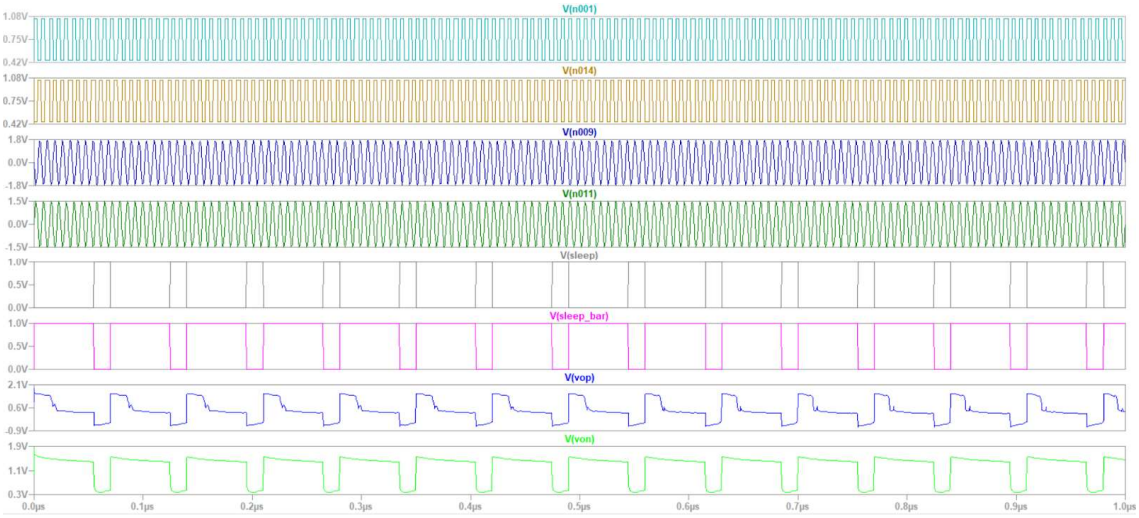

Fig 4.41 Transient Response of Drain Gating CSA

4.8 ONOFIC CSA

This is a technique at the level of circuits that can reduce current leakage and delays in CMOS circuits [8]. What distinguishes this method is the position of a logical unit between the Pull Up Network and Pull Down networks to reduce the leakage current. This new addition to the circuit is referred to as the ON OFF IC block, and consists a pmos as well as an nmos. The term "ONOFIC" refers to the fact that this logical block should be either

in turned on or turned off condition for any output logic level. The focus of this method is on the newly proposed property of turning on and off. When in the state when transistors are on, both ON OFF IC transistors exist in the triode region, while in the state when its off, they move in the depletion mode. Consequently, this approach can provide an accurate level of at the output terminal and minimize leakage current in both normal operation and sleepy modes [4].

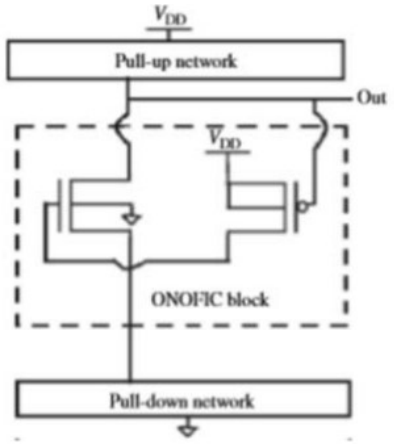

Fig 4.42 ONOFIC Technique

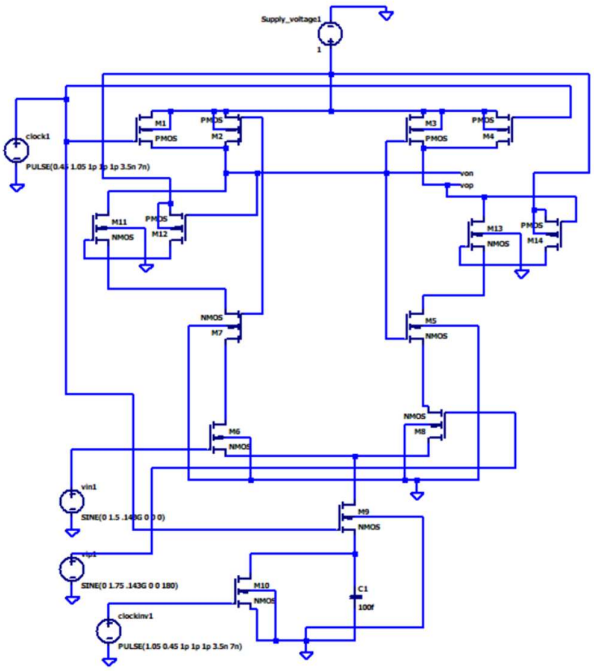

Fig 4.43 ONOFIC CSA

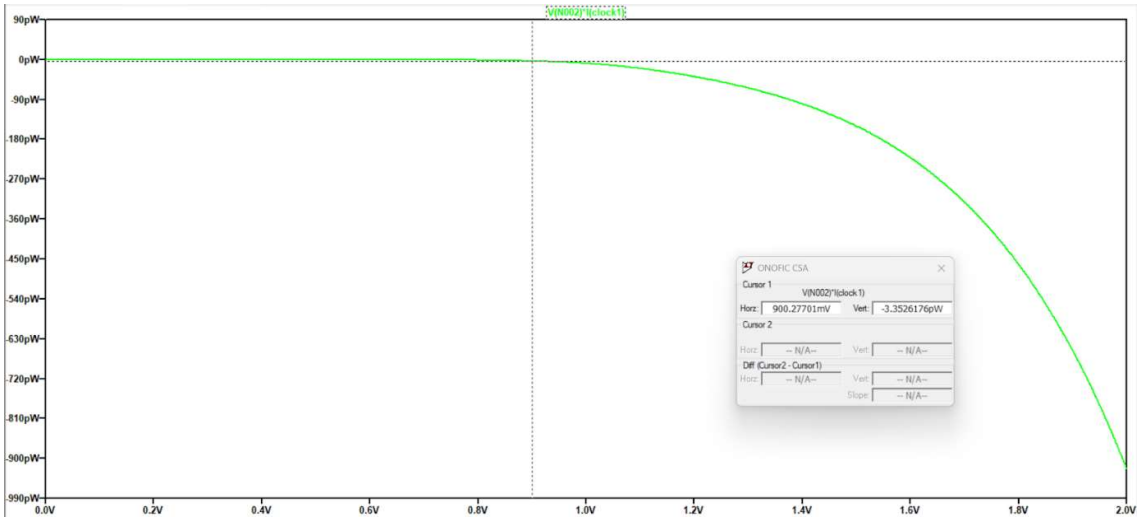

Fig 4.44 Power consumption by input clock (ONOFIC CSA) at Supply voltage = 0.9V is 3.3526176pW

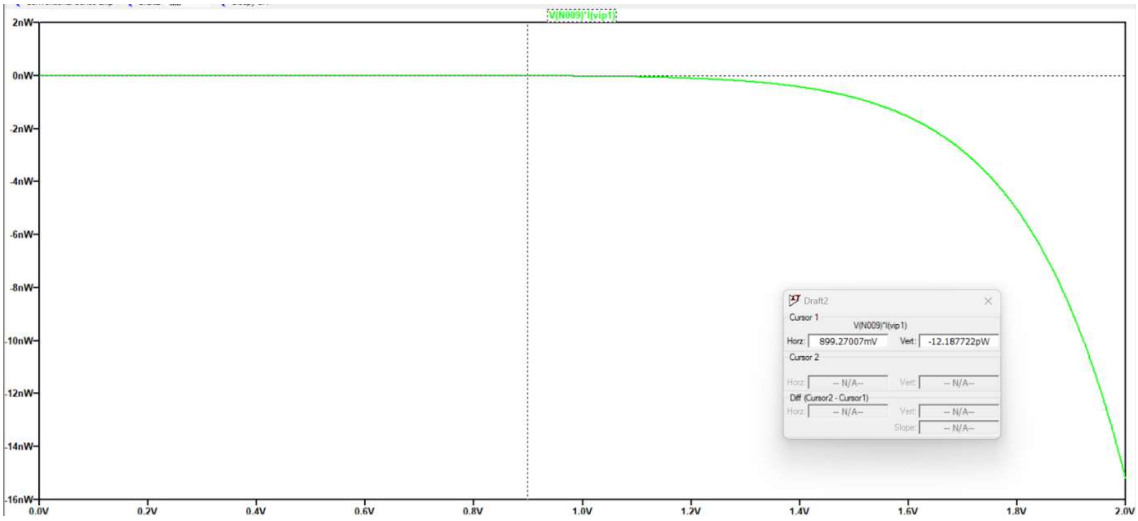

Fig 4.45 Power consumption of input Vip for ONOFIC CSA for input = 0.9V is 12.187722 pw

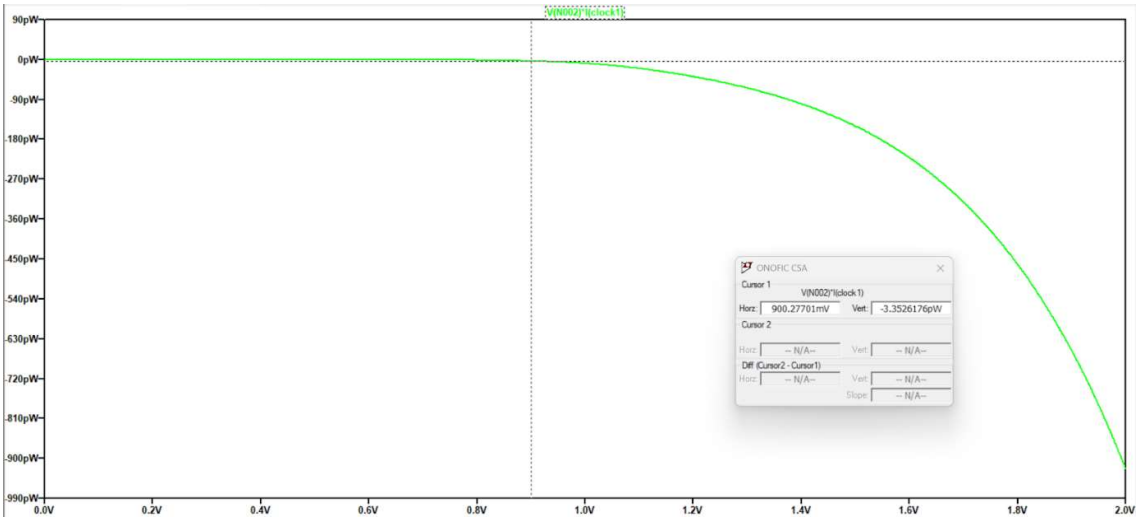

Fig 4.46 Total power consumption by ONOFIC CSA at Supply voltage = 0.9 V is 337.9885 pW.

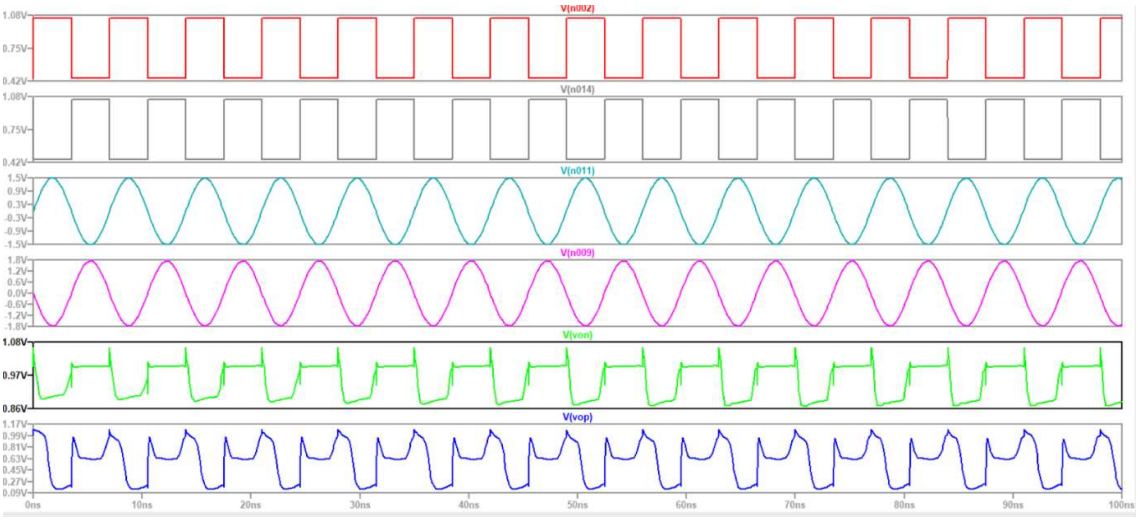

Fig 4.47 Transient Response of ONOFIC CSA

4.9 LCNT CSA

This technique also serves as a method for reducing leakage, and it involves inserting two Negative MOSFET transistors Q3 and Q4 for controlling the leakage current, amidst the logical cells. In this technique, gates together are connected to the output terminal. As a result, there is an increase in the resistance path between V_{dd} and GND, that leads to decrease in

the power consumption. However, one drawback of this method is that it may not be able to draw up or draw down to the exact value required, that limits its usefulness in driven circuits [19].

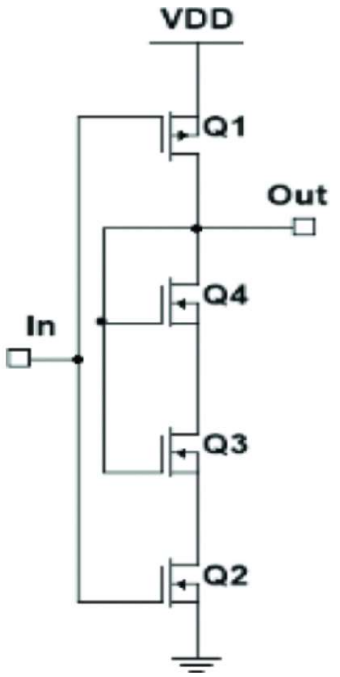

Fig 4.48 LCNT Technique in CMOS Inverter

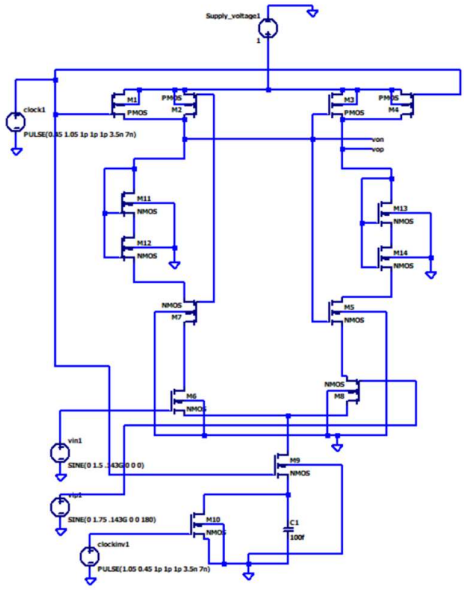

Fig 4.49 LCNT CSA

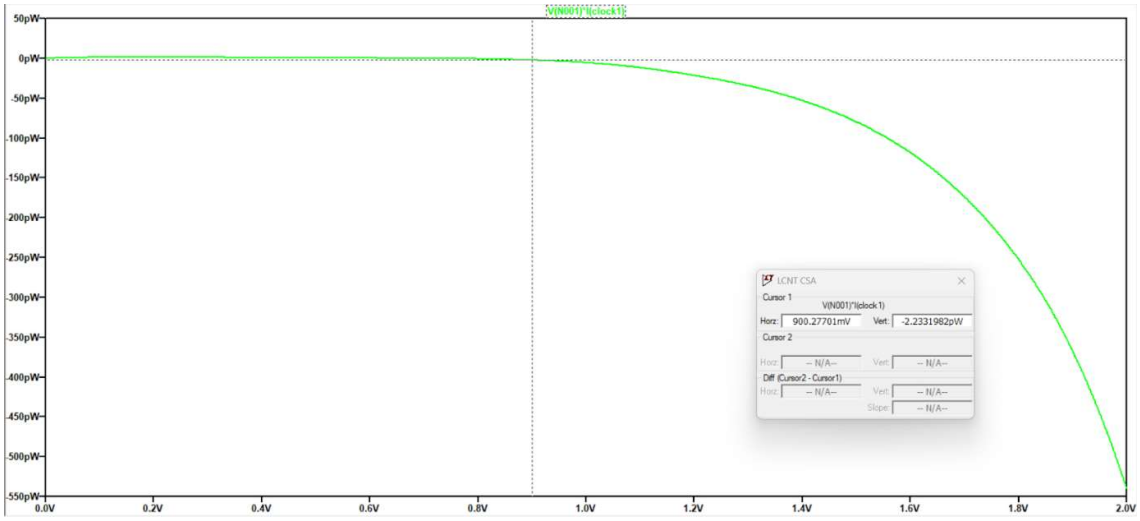

Fig 4.50 Power consumption by input clock (LCNT CSA) at Supply voltage = 0.9V is 2.2331982pW.

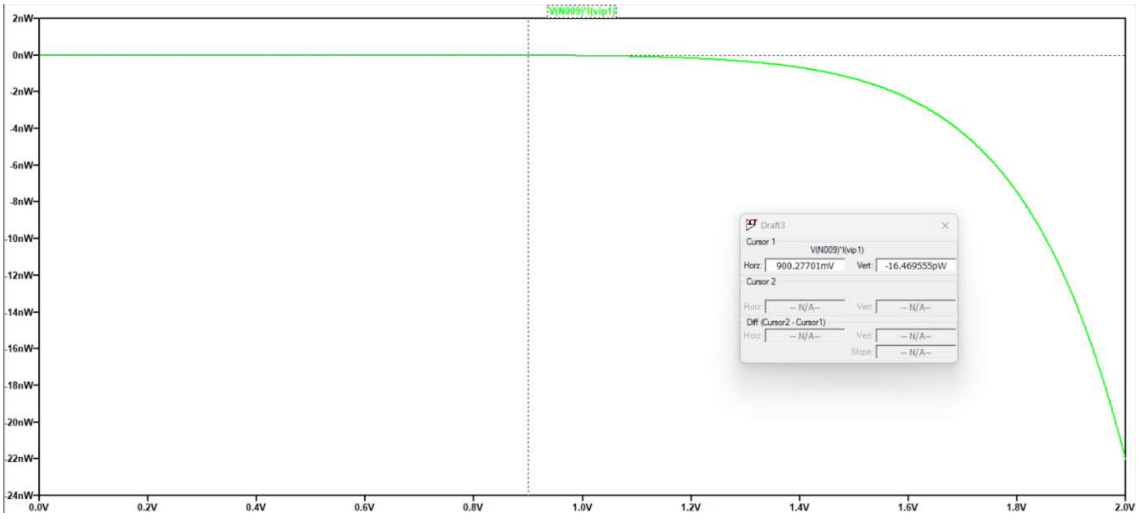

Fig 4.51 Power consumption of input Vip for LCNT CSA for input = 0.9V is 16.469555 pW

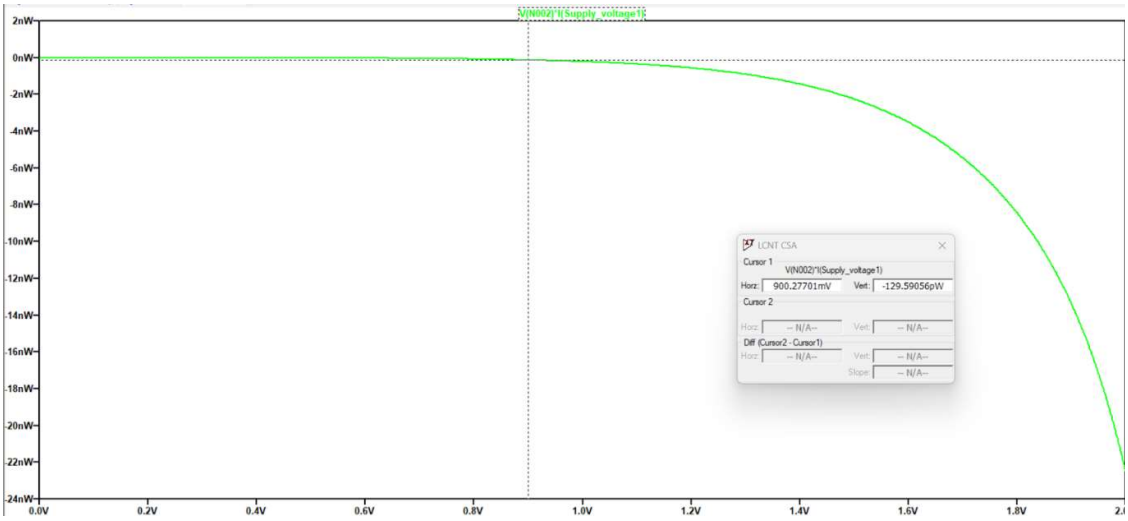

Fig 4.52 Total power consumption by LCNT CSA at Supply voltage = 0.9 V is 129.59112pW.

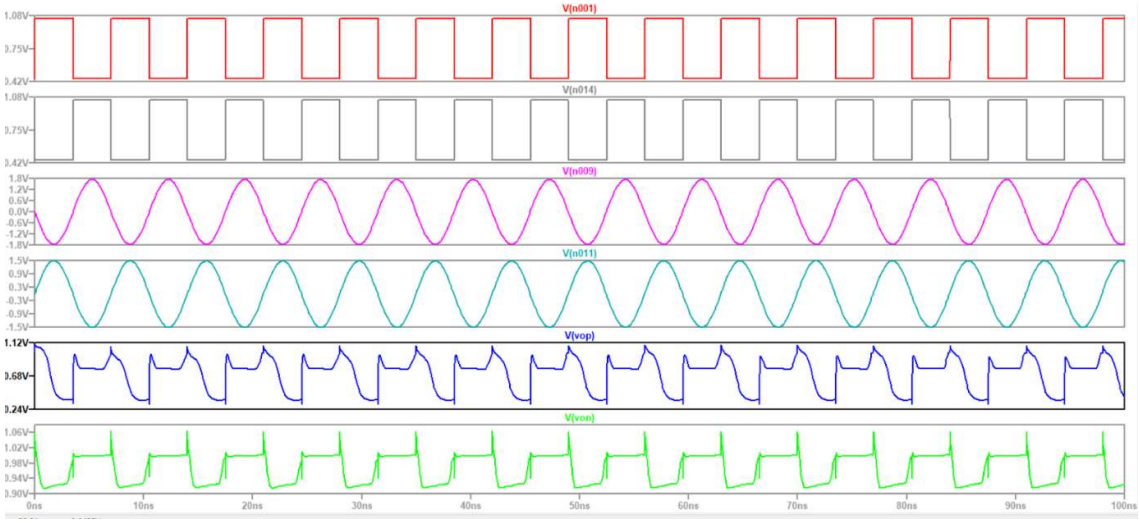

Fig 4.53 Transient Response of LCNT CSA

4.10 Isolated Sleepy Keeper CSA

To prevent input disturbances during the time when sleep transistors are activated, from impacting output, the Isolated Sleepy Keeper method uses a transmission gate to isolate the actual circuit from the portion from which output is taken. A transmission gate can efficiently transmit both high and low, which is not the case for a pass transistor. In order to activate the transmission gate and sleepy transistors they are applied with matching

control signals, with 'S' controlling the positive MOSFET and 'S_bar' controlling the negative MOSFET. When circuit operates normally in the active mode, 'S' is kept high and 'S_bar' is kept low, resulting in the transmission of the circuit outcome at the output node. However, during the sleep mode, 'S' is set to '1' and '$\overline{S}$' to '0', that makes both the transistors of the transmission gate to switch off thereby isolating the base network from the output part. As there is a direct connection between the gate of the “Keep” transistors and the output terminal, the output state is maintained soon before the sleep mode is entered. Creating an isolation between the input and output, the effect of input variations on the output is restricted, resulting in good resolution even in the presence of disturbances. This method significantly improves total and dynamic power, but there are no significant reductions in static power [20].

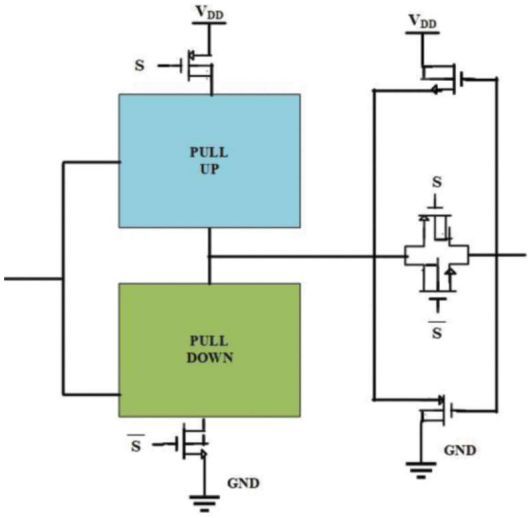

Fig 4.54 Isolated Sleepy Keeper Technique [20]

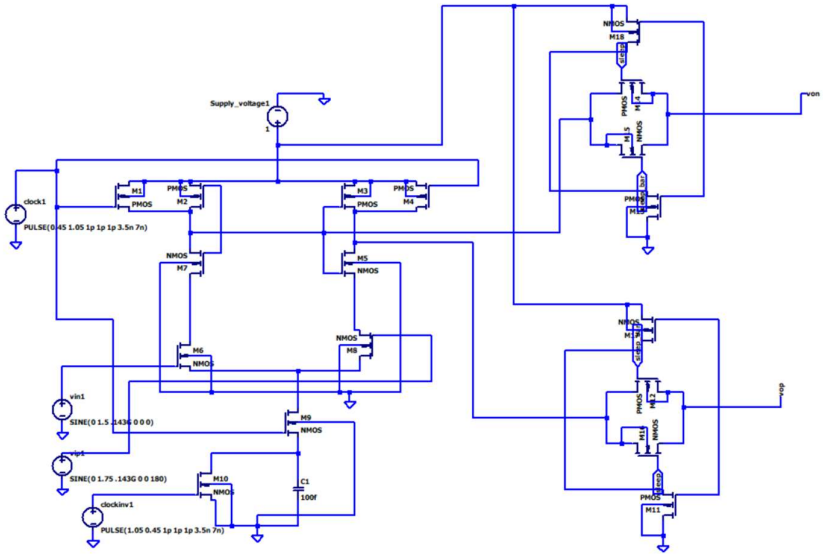

Fig 4.55 Isolated Sleepy Keeper CSA

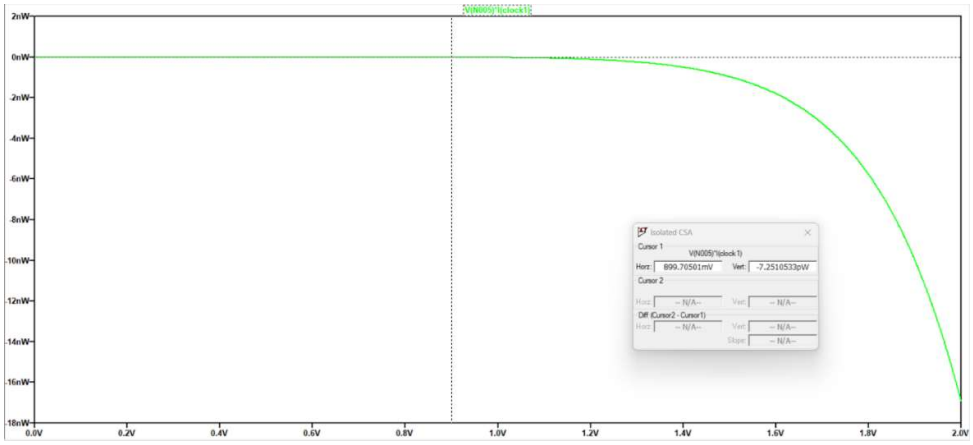

Fig 4.56 Power consumption by input clock (Isolated Sleepy Keeper CSA) at Supply voltage = 0.9V is 7.2510533pW.

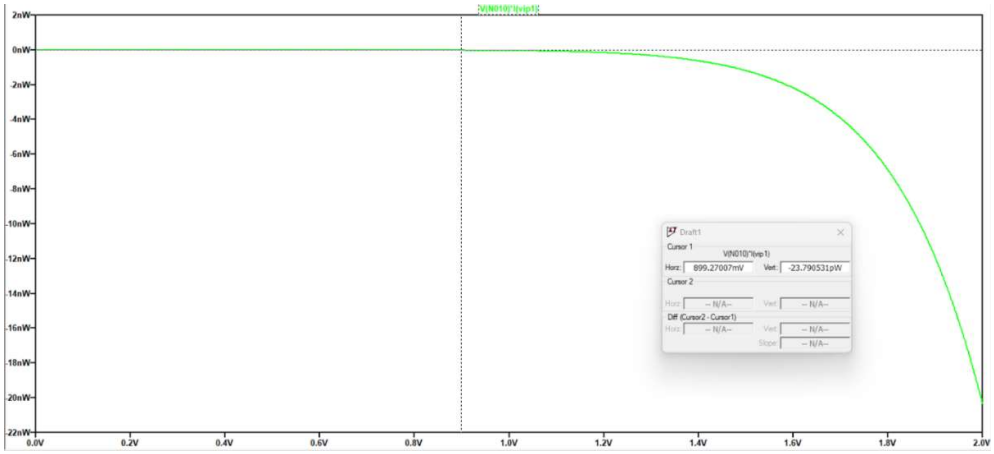

Fig 4.57 Power consumption of input Vip for Isolated Sleepy Keeper CSA for input = 0.9V is 23.790531pW.

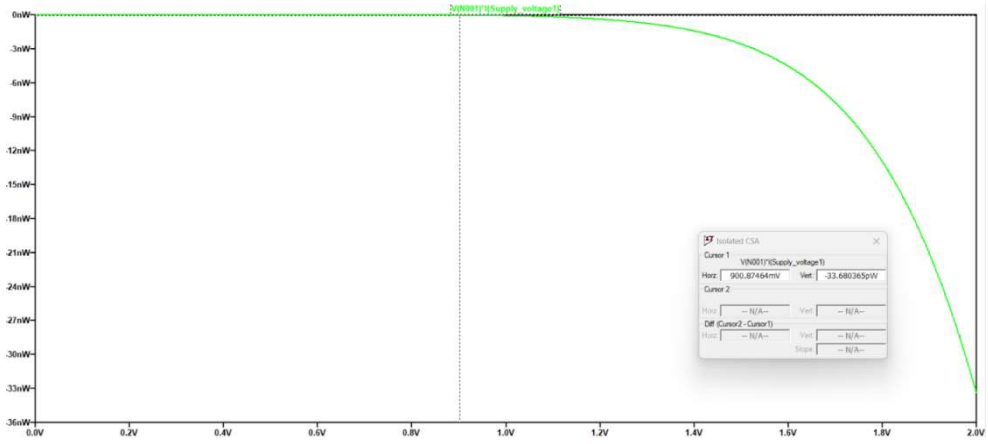

Fig 4.58 Total power consumption by Isolated Sleepy Keeper CSA at Supply voltage = 0.9 V is 33.680365pW.

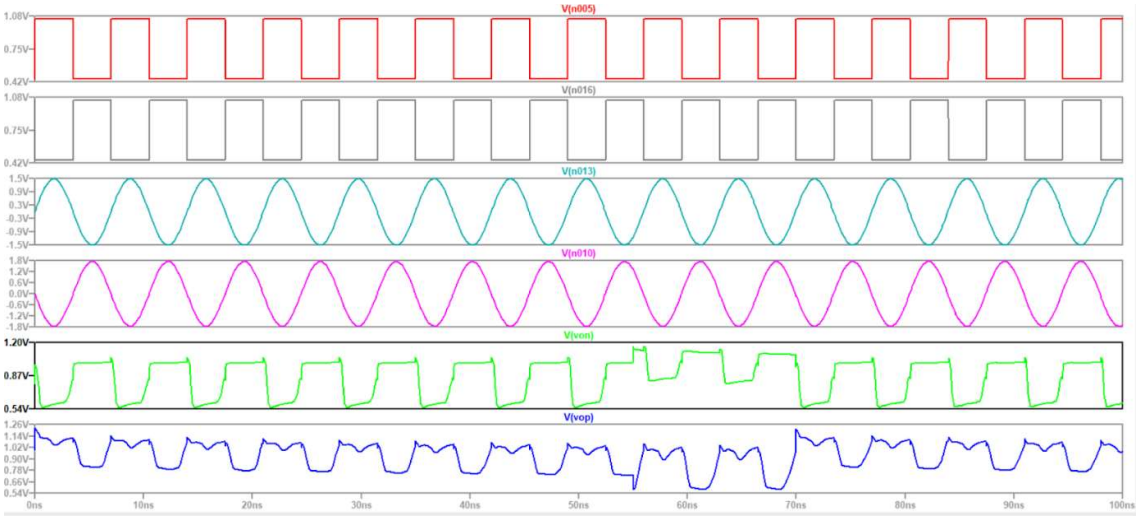

Fig 4.59 Transient Response of Isolated Sleepy Keeper CSA

4.11 ECRL CSA

The Efficient Charge Recovery Logic (ECRL) employs pull-down NMOS devices on both sides to execute the truth table of any circuit's logic. To preserve the state, two PMOS devices are used on the upper side of the circuit, but complete recovery of the clock of power is not feasible through these devices, making it work as quasi-adiabatic logic. As the power clock surges from GND to V_{dd}, the output as well as output bar initiate charging up to voltage 0 and Vdd, respectively. In the provided illustration, the NOR gate also features pull-down NMOS devices and two PMOS devices on the upper side to uphold the state [21].

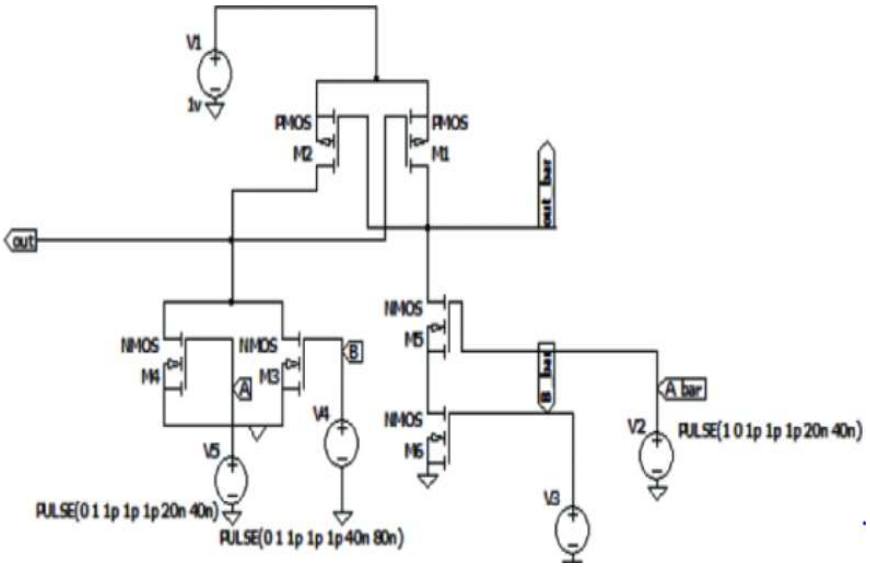

Fig 4.50 ECRL Technique in CMOS NOR

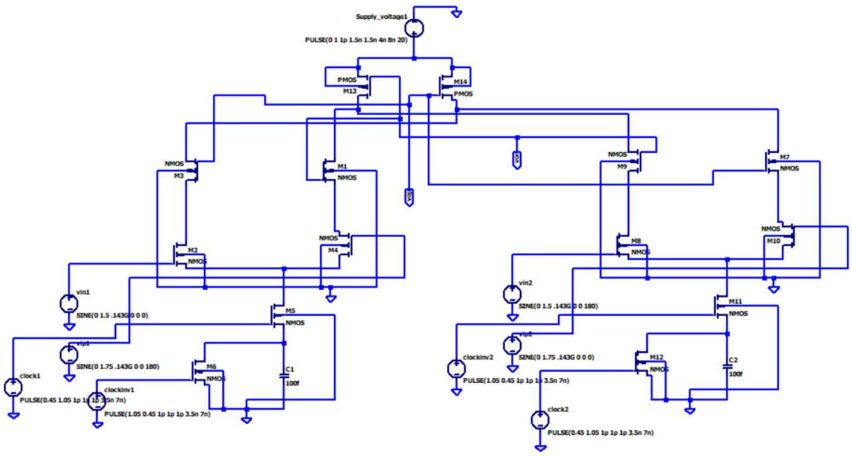

Fig 4.51 ECRL CSA

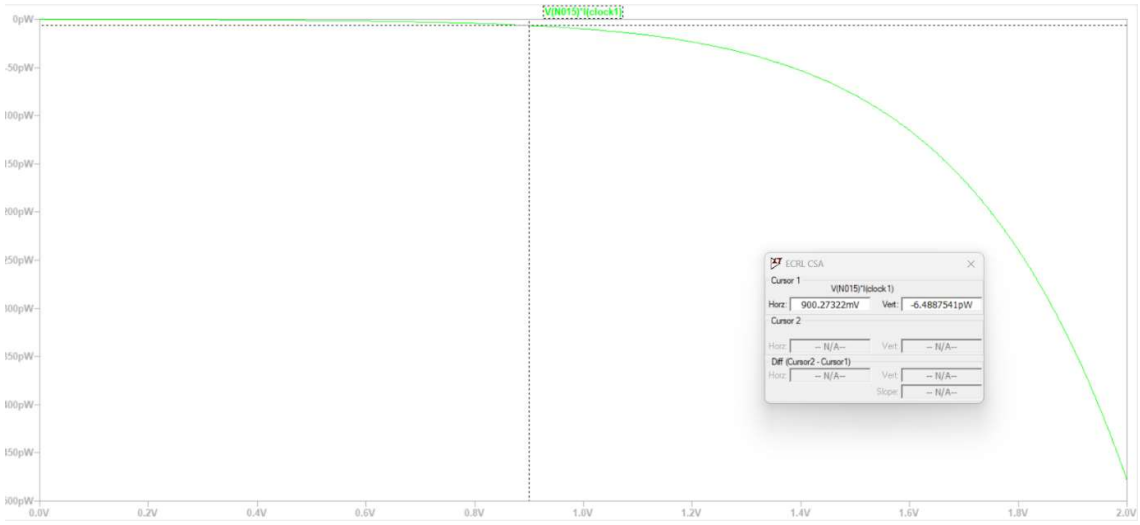

Fig 4.52 Power consumption by input clock (ECRL CSA) at Supply voltage = 0.9V is 6.4887541pW.

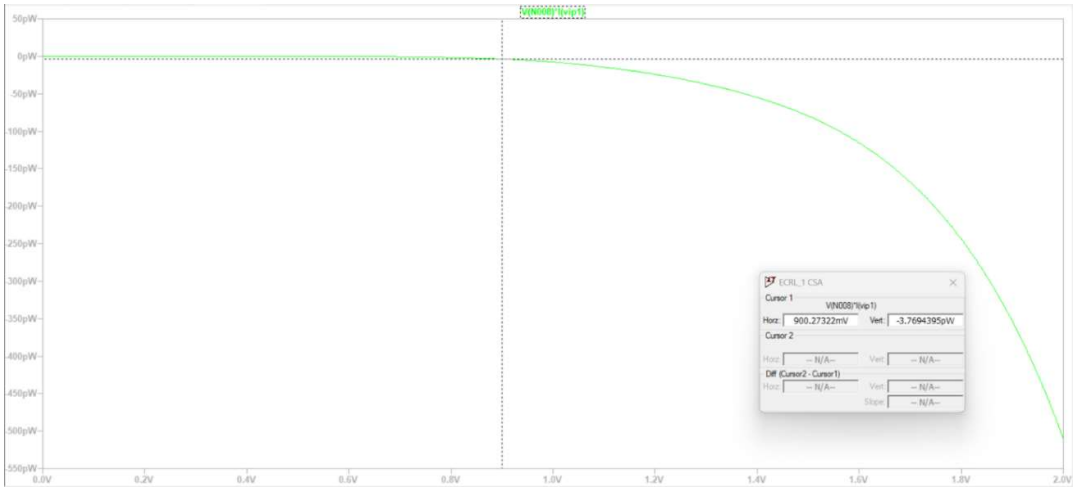

Fig 4.53 Power consumption of input Vip for ECRL CSA for input = 0.9V is 3.7694395pW.

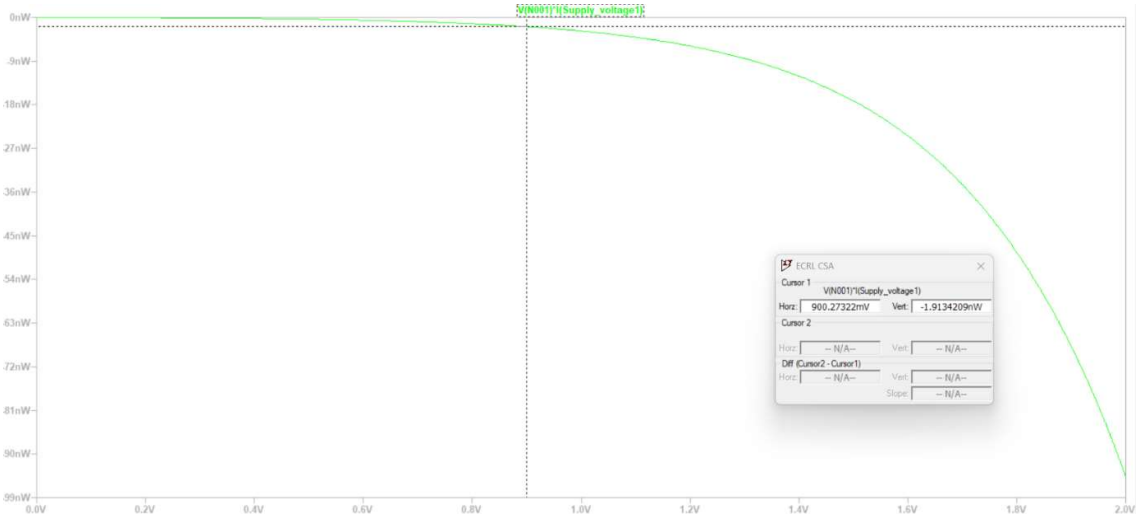

Fig 4.54 Total power consumption by ECRL CSA at Supply voltage = 0.9 V is 1.9134209nW.

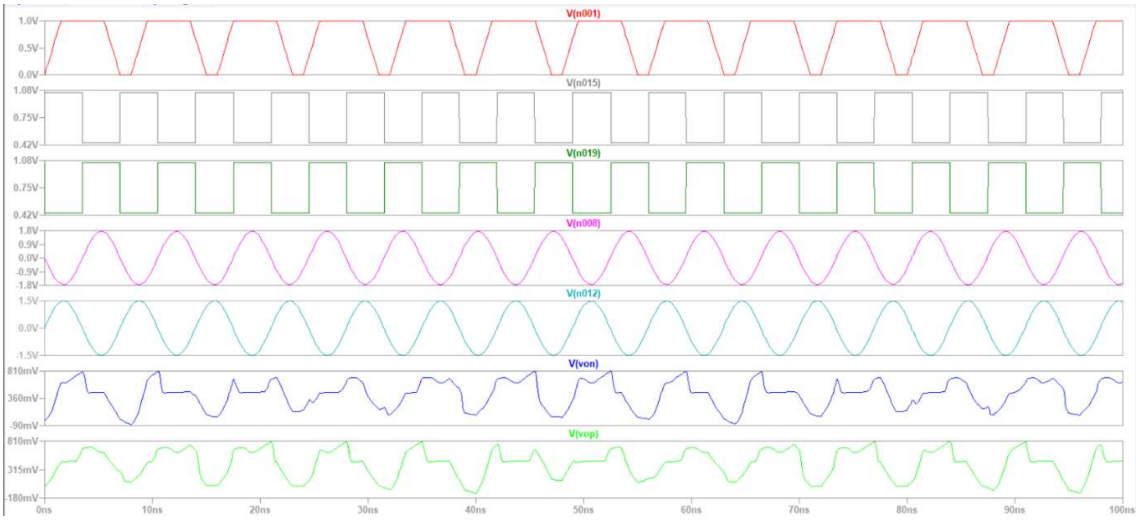

Fig 4.55 Transient Response of ECRL CSA

4.12 SAPON CSA

This method, known as the "Stackly Arranged low Power ON transistor technique," is constructed outside of the logic and uses two transistors to control leakage, which raises the resistance between Vdd and GND. Using SAPON transistors of Complementary MOS (Q3 and Q4) positioned in series between Vdd and GND, this effectively forces the leakage current owing to short circuit during the phase of transition and also restricts the leakage

current in the sub-threshold region during the phase of leveling. The ground and Vdd are linked to the gate terminals of the PMOS and NMOS SAPON transistors, respectively. Positioned above the pull-up network is the SAPON Positive MOSFET (Q3), and below the pull-down network is the SAPON Negative MOSFET (Q4). These two transistors must be run in the active region in order for them to be active during all phases and provide the necessary output by allowing the circuits to dissipate less power [19].

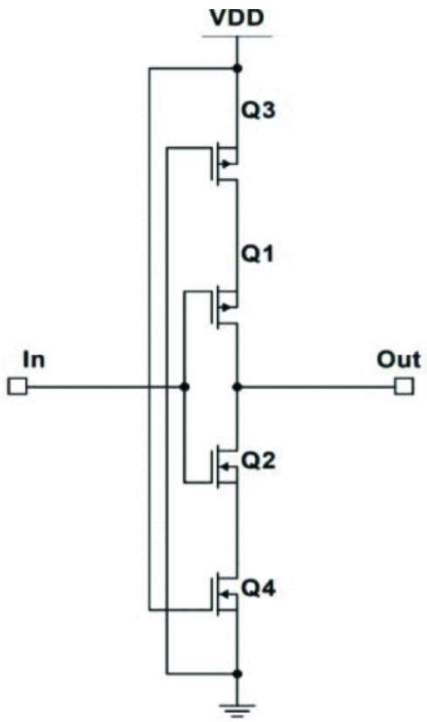

Fig 4.60 SAPON Technique

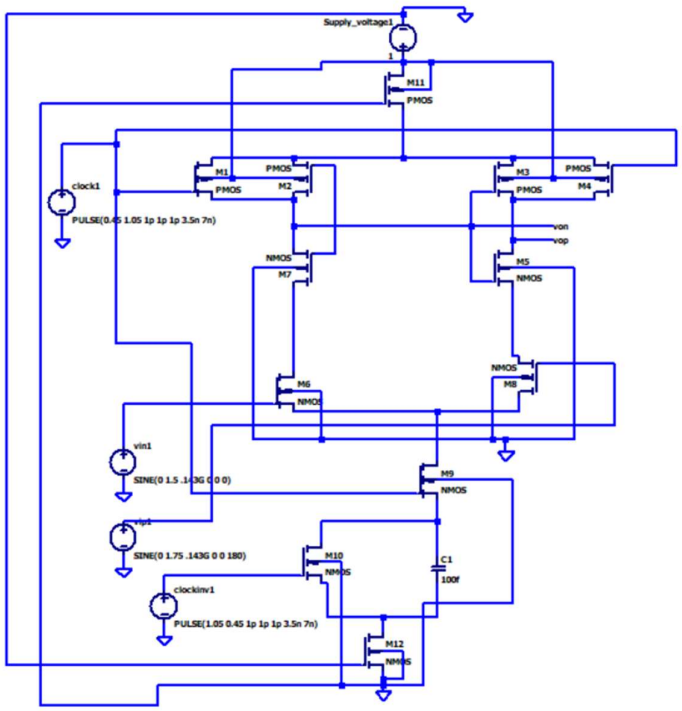

Fig 4.61 SAPON CSA

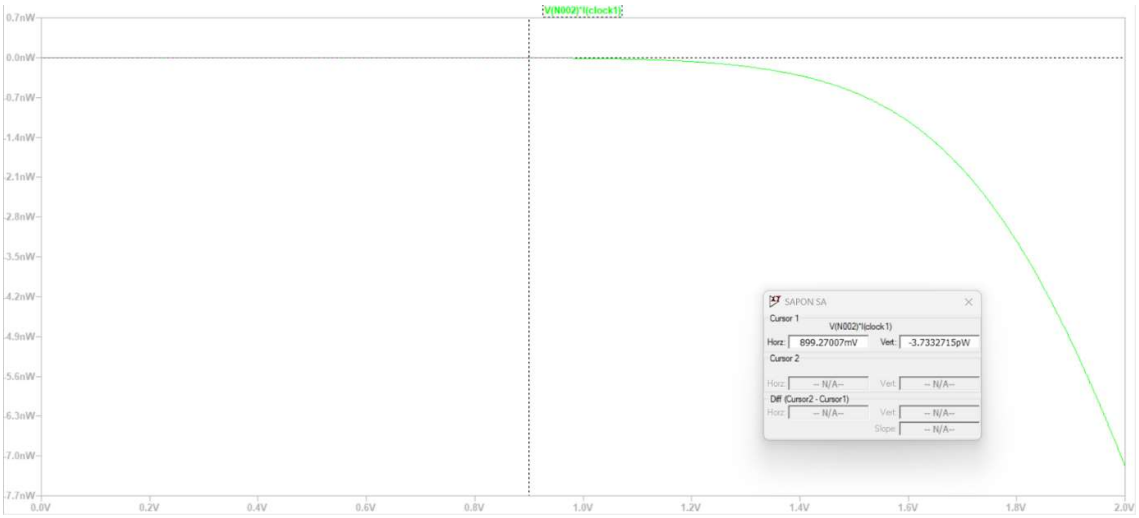

Fig 4.62 Power consumption by input clock (SAPON CSA) at Supply voltage = 0.9V is 3.7332715pW.

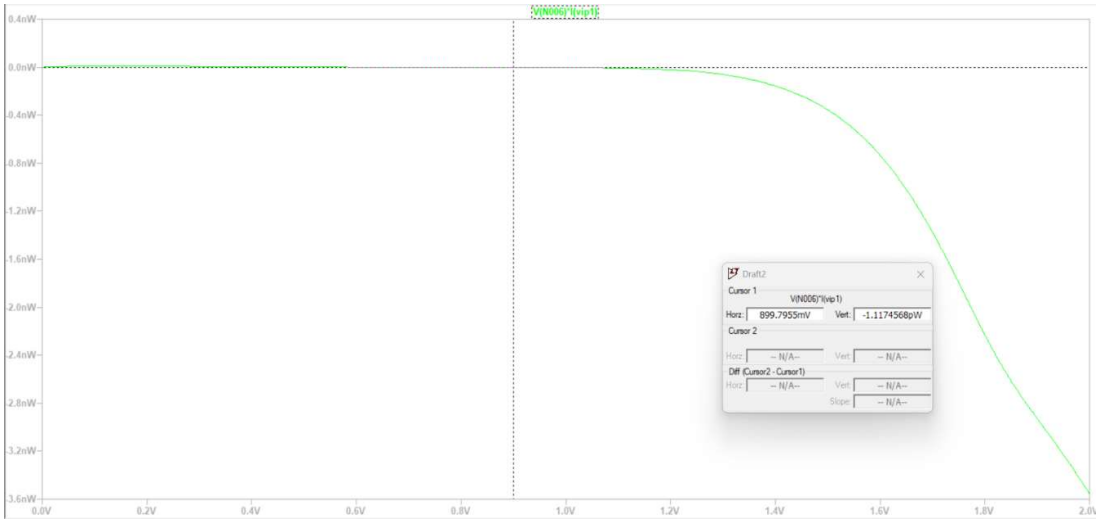

Fig 4.63 Power consumption of input Vip for SAPON CSA for input = 0.9V is 1.1174568pW.

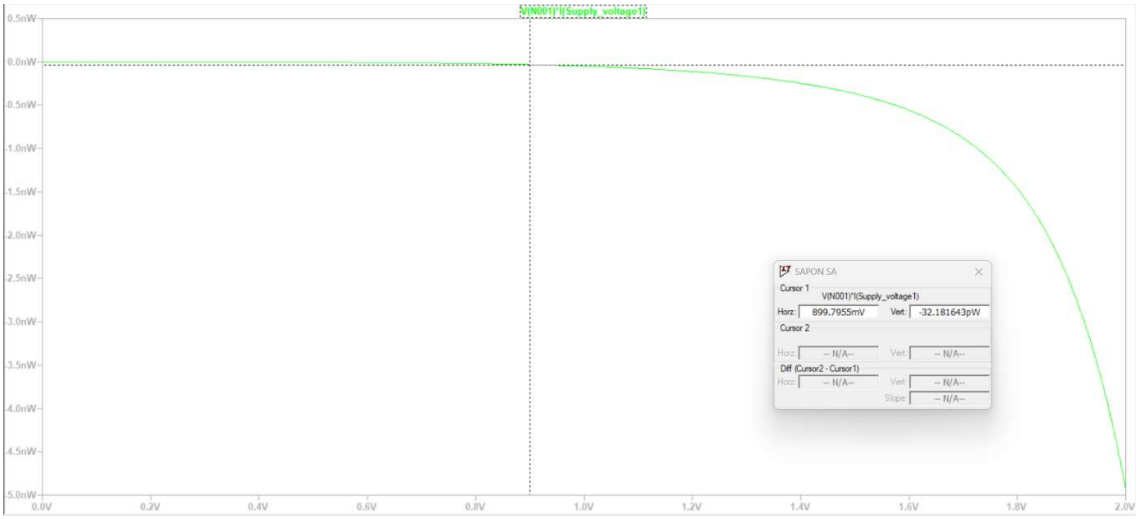

Fig 4.64 Total power consumption by SAPON CSA at Supply voltage = 0.9 V is 32.181643pW.

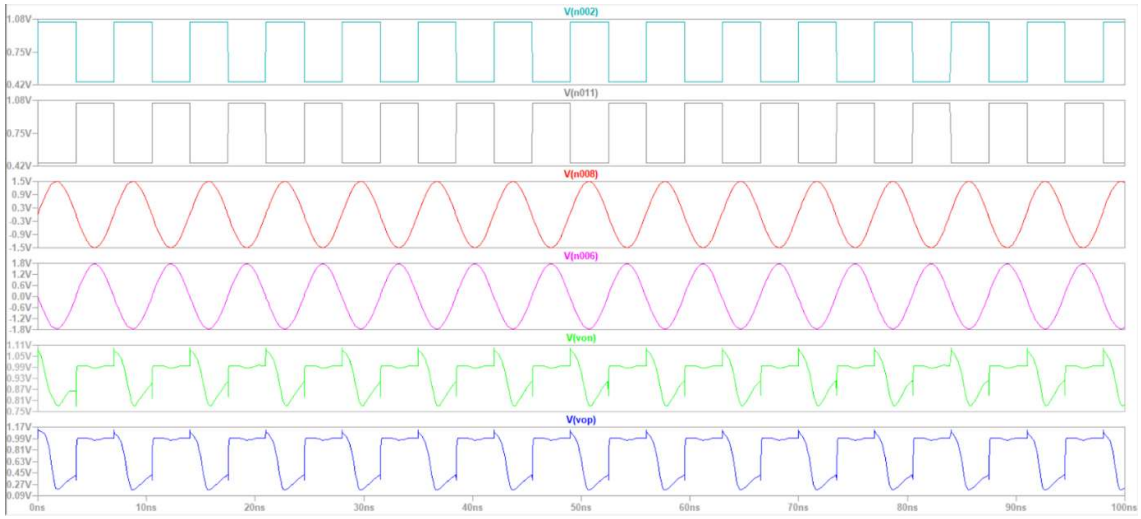

Fig 4.65 Transient Response of SAPON CSA

CHAPTER 5

COMPARATIVE ANALYSIS

A comparison of all the outcomes obtained with respect to clock power, input signal power as well as total consumption of power can be done for conventional CSA, Stacked CSA, Galeor CSA, Sleepy CSA, Sleepy Keeper CSA, Lector CSA, Drain Gating CSA, ONOFIC CSA, Isolated Sleepy Keeper CSA, LCNT CSA and SAPON CSA and can be shown in the table and figure below.

Table 5.1 Result of Comparison of various CSA

S. No.	Type of CSA	Clock Power (pW)	Input Power (pW)	Total Power (nW)
1	Conventional	11.38	48.44	5.17
2	Stacked	10.46	56.65	4.23
3	Galeor	10.62	69.11	2.36
4	Sleepy	1.67	31.08	0.08045
5	Sleepy Keeper	1.72	19.22	0.04663
6	Lector	6.65	18.1	2.874
7	Drain Gating	6.48	3.76	1.913
8	ONOFIC	3.35	12.18	0.337
9	Isolated Sleepy Keeper	7.25	23.79	0.03368
10	ECRL	6.48	3.76	1.91
11	LCNT	2.23	16.46	0.129
12	SAPON	3.73	1.11	0.03218

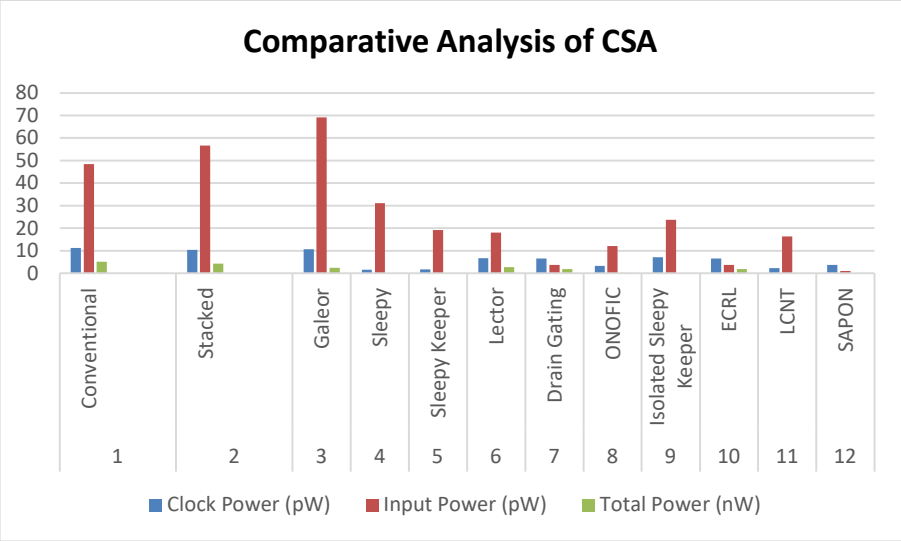

Fig 5.1 Comparative representation of CSA

All the simulations are carried in LTSpice in 45nm technology node. The peak voltages are kept being 1.8 V and power is calculated at 0.9 V. The frequency of clock, Vin and Vip is 0.143 GHz. The W/L= 3 has been applied to the transistors, with W=135n and L=45n, W/L ratio is 8 for PMOS with sleep signal, the ratio of W/L is 4 for NMOS with sleep_bar signal and W/L= 2 for the Positive MOS and Negative MOS that are connected at the output terminal.

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

In this research, several power reduction techniques have been integrated into the Charged Sense amplifier which is an important part of the SRAM. Therefore, it is logical to imply the low-power techniques to Charged sense amplifier to increase its utility in low-power devices and make it easier to use them in compact devices with limited battery life.

The techniques that have been newly applied in CSA apart from the Stacked CSA already proposed in previous publications are Galeor, Sleepy transistors, Sleepy Keeper, ONOFIC, Lector, Drain Gating, LCNT, SAPON, Isolated Sleepy Keeper and ECRL. Their circuits have been simulated and the simulation results have been shown. The results obtained have been compared in tabular form and plotted in graphical form.

It is evident from the tabular data provided above that the better reduction in power is obtained in Isolated Sleepy Keeper and SAPON CSA. There is a massive decline in the power dissipation in comparison to the traditional CSA as well as the stacked CSA. The reduction is also observed in clock power and input power. Earlier, even Sleepy CSA and Sleepy Keeper CSA exhibited wonderful results in terms of reducing the dissipated power.

Nonetheless, it is clearly evident that the power consumption comes with an area trade-off in almost all the configurations demonstrated in this thesis. But, as the power reduction is tremendous, some area compensation can be adjusted. The decision making now lies upon the use-case so as to choose a suitable configuration with optimized area and power or a balance between

these criteria.

6.2 FUTURE SCOPE

Charged sense amplifiers (CSA) are vital to the functioning of SRAMs which is an integral part of all the integrated circuits. Therefore, it is imperative to explore ways to decrease the consumption of power in the CSA. Like mentioned above that the power dissipated due to current by leakage is majority contributor to the total consumption of power in nanoscale devices, several other power reduction techniques such as Input vector control (IVC)/ Input Controlled Leakage Restrain Transistor (ICLRT), etc. can be implemented in the circuit. New configurations published in recent publications can also be considered as is evident from the results obtained that these have potential to show promising reduction in power. Also, a detailed comparative performance analysis can be done with all the power reduction techniques along with power, area and delay. The PDP, i.e., Power Delay Product can be used for comparison and area can be estimated roughly by using the W/L ratios and number of transistors used. The ultimate aim can be to create an optimized CSA so that top-notch performance and power requirements may be achieved. Also, better simulation tools such as Cadence Virtuoso can be used. A lower technology node or a device change altogether from MOSFET to FINFET, etc. can also be considered for significant improvements in performance as far as area, speed and power are concerned. Some organic as well as flexible electronics also show promising results and can be considered as alternative options for device change. In conclusion, the aim is always to obtain most optimized configuration depending upon the use-case.

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