ANALYSIS OF SINGLE STAGE OP-AMP

A DISSERTATION

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE AWARD OF THE DEGREE OF

MASTER OF TECHNOLOGY
IN
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I hereby certify that the Project Dissertation titled **"Analysis of Single Stage op-Amp"** which is submitted by Divya Kumar 2k18/vls/03, Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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Date:9/10/2020 **Divya Kumar**

ABSTRACT

Demand for higher performance and more functionality for hand-held systems have been continually growing in the recent years. Improved performance and more functionality, however, often come with more power consumption. This is why new low power design techniques and circuits have become one of the major subjects of research and innovation.

Active RC filters as a part of many systems that are integrated on the chip are no exception. That is they must be low power and the area that they occupy on the silicon chip must be as small as possible. In conventional active RC filters, operational amplifiers (Op-amps) are used as integrators, thus, power consumption of the filters are directly related to that of Op-amps.

In high performance analog integrated circuits, such as switch-capacitor filters, delta-sigma modulators and pipeline A/D converters, op amps with very high dc gain and high unity-gain frequency are needed to meet both accuracy and fast settling requirements of the systems. In order to achieve high-gain, the folded Cascode amplifier is often adopted as the first-stage of two-stage amplifiers.

This project report presents a highly adaptive operational amplifier with high gain, high bandwidth, high speed and low power consumption. By adopting the recycling folded Cascode topology along with an adaptive biasing circuit, this design achieves high performance in terms of gain-bandwidth product (GBW) and slew rate (SR)

All the simulation in this project and result verification is done on ORCAD 16.6 software using 180nm technology.

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CHAPTER 1

INTRODUCTION

Operational amplifiers (op amps) are an integral part of many analog and mixed-signal systems. Op amps with extremely different levels of complexity are used to realize functions ranging from dc bias generation to high-speed amplification or filtering.

We loosely describe an op amp as a "high-gain differential amplifier. Since op amps are generally used to implement a feedback system, their open-loop gain is selected according to the precision essential of the closed-loop circuit.

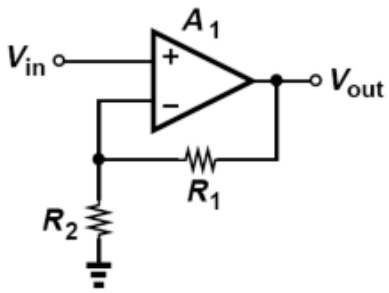

Fig 1.1: Basic Op-amp circuit

Up to two decades ago, most op amps were designed to help as "general-purpose" building blocks, satisfying the requirements of many different applications. Such efforts required to create an "ideal" op-amp, e.g., with very high voltage gain (several hundred thousand), high input impedance, and low output impedance, but at the cost of many other aspects of the performance, e.g., speed, output voltage swings, and power dissipation.

By contrast, today's op amp design proceeds with the recognition that the trade-offs between the parameters eventually require a multi-dimensional compromise in the overall implementation, making it necessary to know the adequate value that must be achieved for each parameter. For example, if the speed is critical while the gain error is not, a topology is chosen that favors the former, possibly sacrificing the latter.

An “ideal” or perfect op-amp is a device with certain special characteristics such as infinite open-loop gain A_O, infinite input resistance R_{IN}, zero output resistance R_{OUT}, infinite bandwidth 0 to ∞ and zero offset (the output is exactly zero when the input is zero).

There are a very large number of operational amplifier IC's available to suit every possible application from standard bipolar, precision, high-speed, low-noise, high-voltage, etc. in either standard configuration or with internal Junction FET transistors.

Operational amplifiers are available in IC packages of either single, dual or quad op-amps within one single device. The most commonly available and used of all operational amplifiers in basic electronic kits and projects is the industry standard **µA-741**.

The implementation of a two-stage, fully-differential and capacitance compensated CMOS operational amplifier has been presented in this report. The high gain enables this circuit to operate efficiently in a closed loop feedback system, whereas, the high bandwidth makes this circuit suitable for the high-speed applications.

The high gain in op-amps is one of the desired figures of merit for all kind of signal processing applications while simultaneously optimizing all the parameters of the op-amp is also desirable. In two-stage CMOS op–amps, the phase margin could easily reach to less than the amount, which is just enough for stable operation, i.e., below 45º, because of the two dominant poles. This serious problem should be taken care of by designers, otherwise there is a good possibility that the op-amp output will oscillate and, instead of an amplifier, it will become an oscillator.

Performance Metrics:

1) Gain,
2) Speed,
3) Output Swing
4) Linearity
5) Power Dissipation
6) Noise
7) Input CM Range
8) Supply Rejection
9) Input Offset Voltage

Gain : The open-loop gain of an op amp determines the precision of the feedback system employing the op amp. the required gain may vary by four orders of magnitude according to the application. Trading with such parameters as speed and output voltage swings, the minimum required gain must therefore be known. A high open-loop gain may also be necessary to suppress nonlinearity.

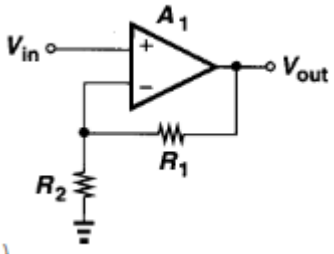

Fig 1.1 : Basic Op-amp circuit

Small-Signal Bandwidth: The high-frequency behavior of op amps plays a critical role in many applications. For example, as the frequency of operation increases, the open-loop gain begins to drop creating larger errors in the feedback system. The small-signal bandwidth is usually defined as the "unity-gain" frequency, *fu.* which exceeds GHz in today's CMOS op-amps. The 3-dB frequency may also be specified to allow easy prediction of the closed-loop frequency response.

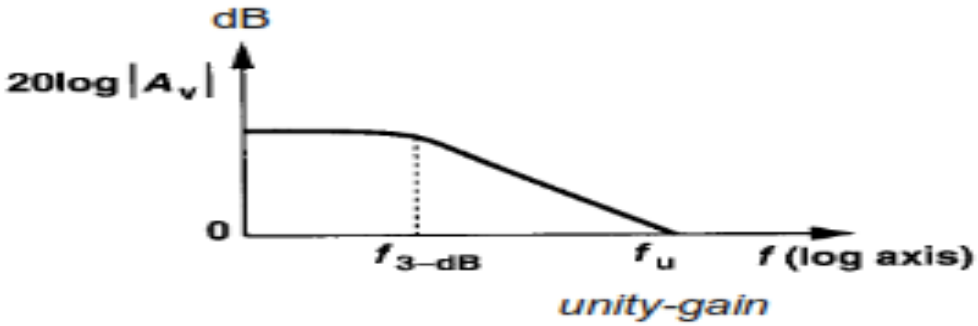

Fig 1.2 Gain Roll –off With Frequency

Large-Signal Bandwidth

In many of today's applications, op amps must operate with large transient signals. Under these conditions, nonlinear phenomena make it difficult to characterize the speed by merely small-signal properties such as the open-loop response As an example, suppose the feedback circuit incorporates a realistic op amp (i.e., with finite output impedance) while driving a large load capacitance. How does the circuit behave if we apply a 1-V step at the input? Since the output voltage cannot change instantaneously, the voltage difference sensed by the op amp itself at t=0 is equal to 1 V. Such a large difference momentarily drives the op amp into a nonlinear region of operation. (Otherwise, with an open-loop gain of, say, 1000, the op amp would produce 1000 V at the output.)

Output Swing

Most systems employing op amps require large voltage swings to accommodate a wide range of signal amplitudes. For example, a high-quality microphone that senses the music produced by an orchestra may generate instantaneous voltages that vary by more than four orders of magnitude, demanding that subsequent amplifiers and filters handle large swings (and/or achieve a low noise). The need for large output swings has made fully differential op amps quite popular. Similar to the circuits, such op amps generate "complementary" outputs, roughly doubling the available swing. Nonetheless, as mentioned in Chapters 3 and 4 and explained later in this chapter, the maximum voltage swing trades with device size and bias currents and hence speed. Achieving large swings is the principal challenge in today's Op-amp design.

Linearity

Open-loop op- amps suffer from substantial nonlinearity. The input pair M1-M2 exhibits a nonlinear relationship between its differential drain current and input voltage. The issue of nonlinearity is tackled by two approaches: using fully differential implementations to suppress even-order harmonics and allowing sufficient open-loop gain such that the closed-loop feedback system achieves adequate linearity. It is interesting to note that in many feedback circuits, the linearity requirement, rather than the gain error requirement, governs the choice of the open-loop gain

Noise and Offset

The input noise and offset of op amps determine the minimum signal level that can be processed with reasonable quality. In a typical op amp topology, several devices contribute noise and offset, necessitating large dimensions or bias currents. We should also recognize a trade-off between noise and output swing.

Supply Rejection

Op amps are often employed in mixed-signal systems and sometimes connected to noisy digital supply lines Thus, the performance of op amps in the presence of supply noise, especially as the noise frequency increases is important for this reason fully differential topologies are preferred.

1.1 OBJECTIVE

The main objective of this project implementing recycling folded cascode along with an adaptive-biasing circuit to achieve high gain, high bandwidth and high slew rate specifications.

This single stage operational amplifier is capable of providing high gain of around 70dB along with a high bandwidth of 250 MHz and a slew rate of around 100V/μs which is approximately twice as that of the recycling folded cascode without the additional adaptive-biasing circuit.

A single-stage Op-amp as opposed to multi-stage is used to avoid the need for compensation capacitor and to save the second stage power consumption. This is made possible because the load resistors are not directly connected to the op-amps output, hence eliminating the need for a driver stage.

To alleviate the problem of instability, the second pole of the Op-amp at the mirror nodes is nulled and pushed to higher frequencies by a negative capacitance circuit.

In high performance analog integrated circuits, such as switch-capacitor filters, delta-sigma modulators and pipeline A/D converters, op amps with very high dc gain and high unity-gain frequency are needed to meet both accuracy and fast settling requirements of the systems. However, as CMOS design scales into low-power, low-voltage and short-channel CMOS process regime, satisfying both of these aspects leads to contradictory demands, and becomes more and more difficult, since the intrinsic gain of the devices is limited.[1]

In order to achieve high-gain, the folded cascode amplifier is often adopted as the first-stage of two-stage amplifiers. Actually, in the deep-submicron CMOS technology, high-gain amplifiers are difficult to be implemented because of the inherent low intrinsic gain of the standard threshold voltage MOS transistors. At the same time, because of the reliability reasons in the deep-submicron processes, the output swing of amplifier is severally restricted with the lower power supply voltage.

To efficiently increase operational amplifier's gain and output swing, multi-stage fully-differential operational amplifier topology is appreciated. The operational amplifier with three or

even more stages equipped with the Nested-Miller compensation or the Reversed Nested-Miller compensation shows high efficiency in the gain enhancement, while they require additional large compensation capacitors compared to the traditional two-stage operational amplifier, which will lead to a larger die area and the limited slew rate. Besides, additional common mode feedback (CMFB) circuits would consume additional power.

1.2 ORGANIZATION OF REPORT

This report has been organized into 5 chapters. Chapter 1 deals with the introduction of Op-Amps. It also includes performances metrices of an Op-amp and objective of the report. Chapter 2 deals with Literature Survey. In chapter 3, Recycling folded cascade topology and adaptive biasing is discussed. In chapter 4 circuit and simulation results are being shown. And in Chapter 5 Conclusion and Future Scope is given.

CHAPTER 2

LITERATURE SURVEY

2.1 SINGLE STAGE OP-AMPS

All of the differential amplifiers can be considered as op' amps. Two such topologies with single-ended and differential outputs. The small-signal, low-frequency gain of both circuits is equal to GmN(roN||rop), where subscripts N and P denote NMOS and PMOS, respectively.This value hardly exceeds 10 n submicron devices with typical current levels. The bandwidth is usually determinedby load capacitance,CL

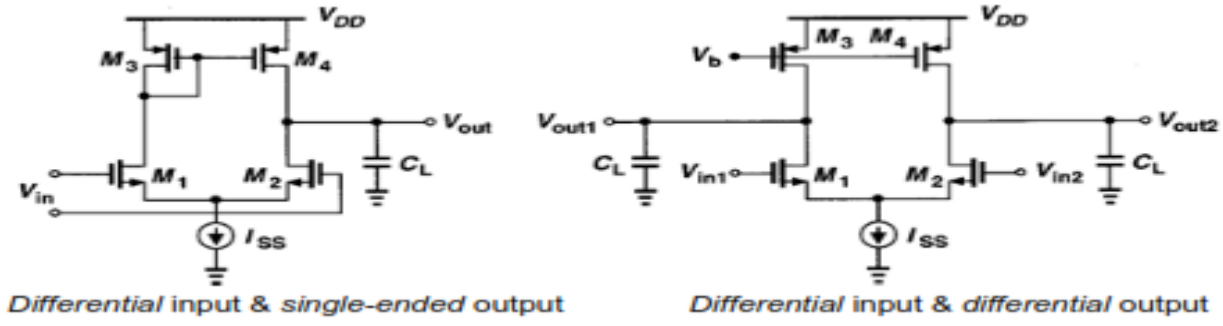

Fig 2.1 Differential input with single ended and differential output

For small-signal:

Low frequency gain ,In general, this value hardly exceeds 20 in submicron devices with typical current levels. The bandwidth is usually determined by the load capacitance.

The circuits suffer from noise contributions of *M*1-*M4* In all op amp Topologies, at least four devices contribute to the input noise: two input transistors and two “load” transistors

2.1.1 TELESCOPE CASCODE OP-AMPS

In order to achieve a high gain, the differential Cascode topologies can be used. Shown in Fig for single-ended and differential output generation, respectively. Low frequency gain $A_v = g_{mN}[(g_{mN} r_{oN}^2) \parallel (g_{mP} r_{oP}^2)]$, but at the cost of output swing and additional poles.

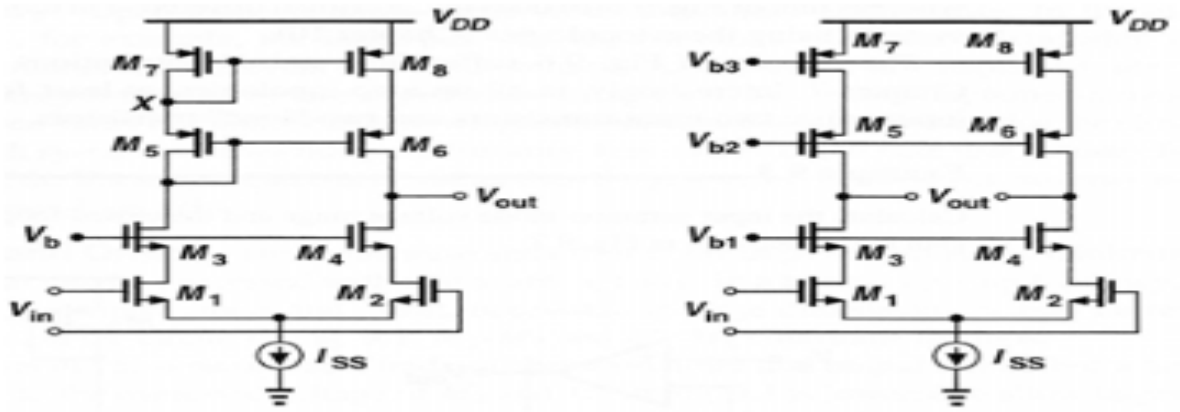

Fig 2.2 : Telescopic Cascode for Single Ended and differential output generation

The circuit providing a single-ended output suffers from a mirror pole at node *X*, creating stability issues.

Relatively high gain :Mirror pole in single-ended circuit not good. (Both output swing and mirror pole point to a differential circuit as the better choice.) . but It is difficult to short the output to the input of a telescopic op amp.

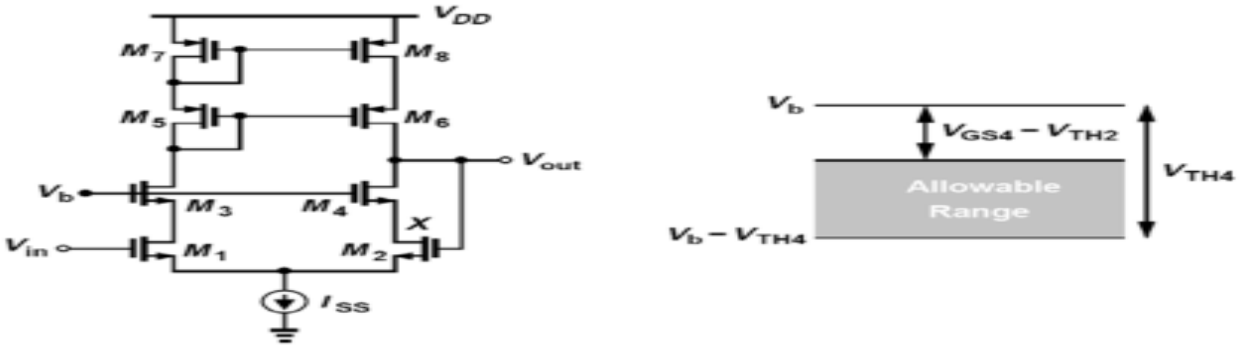

Fig 2.3 : Telescopic Cascode opamp with input and output shorted.

Speed somewhat degraded with respect to simple op amp. (But less Miller effect.)

Summary: Telescopic op amp usually provides the best trade-off between gain, power dissipation, speed, and noise. But its output swing is limited and shorting the input and output is difficult.

2.1.2 FOLDED CASCODE OP-AMP

The folded cascode amplifier is a single stage amplifier, which consists of a common source transistor cascoded with a common gate transistor of the opposite polarity. In the operational amplifier implementation of this type of amplifier, a differential pair is used as the input stage to amplifier, acting as the common source portion of the cascade. The drains of the input transistors are then linked to two opposite polarity common gate transistors. The common gate transistors are then connected to an active current source load to complete the circuit. The goal of using this topology is to achieve the simplicity and small size of a single stage amplifier, while achieving the gain of a multi-stage amplifier. By “folding” the cascode over into a pair of opposite polarity transistors, this decreases the required headroom for the circuit, giving the same performance as a typical cascode amplifier, but with a lower required supply voltage. The cascoded transistors in this design serve to increase the output resistance of the circuit, which increases the small signal gain of the amplifier. This is the main benefit of the topology. Since the current mirror’s output resistance appears in parallel with the output resistance of the amplifying portion of the circuit, it is important that the current source be cascoded as well, so as not to extinguish all of the benefits that were gained by the cascode in the first place. Due to the high threshold voltages of the PMOS transistors in this process, some slight modifications were made to the general implementation of this circuit. Instead of connecting the current mirrors at the output of the amplifier in a gate-drain configuration, as is typically done, the gate of the uppermost transistors were connected to the drain of the casocde transistors and the cascode transistors were biased externally. The deeper details of this type of modification can be found in [1]. The final circuit topology was modeled after this modification and is provided .

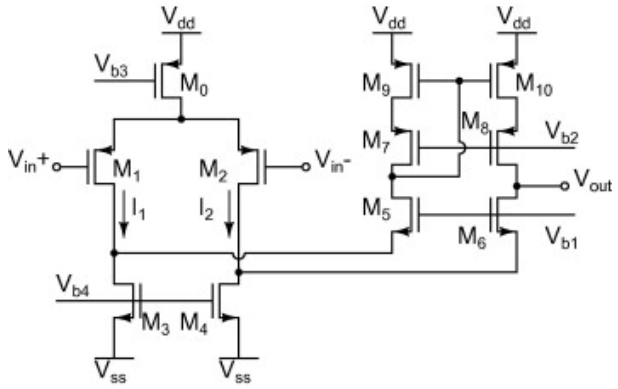

Fig: 2.4 Folded Cascode Op-Amp

Figure shows typical structure of a folded cascode op-amp Folded cascade topology is called as 'folded cascode' because it comes from a folding down n-channel cascode active loads of a different-pair and changing the MOSFET to the p-channel. These topologies allow the input common-mode level of being close to the power supply voltage as well as providing a high output swing, wide input common-mode range and preferably steering in low voltage supply circuits. However, this topology has higher noise compare to the telescopic op-amp

Folded cascode amplifier is a single-pole operational amplifier with large output swing and has higher gain compared to the ordinary op-amp. It is very suitable for deep negative feedback because of its small signal gain that can be very large. Comparing to the ordinary telescopic amplifiers, folded cascode operational amplifiers have a larger output swing (E. Rajni, "Design of High Gain Folded-Cascode Operational Amplifier Using 1.25 um CMOS Technology," Int. J. Sci. Eng. Res., vol. 2, no. 11, pp. 1–9, 2011). Input and output can be short circuited to make it easier for the selection of input common-mode level due to its relatively large output swing. The input common-mode level can be close to the power supply voltage by using folded cascode op-amp. By using NMOS input, the common mode level of the gate pole can reach V_{DD}. While PMOS input can lower the input common-mode level to 0V.

In order to alleviate the drawbacks of telescopic cascode op amps, namely, limited output swings and difficulty in shorting the input and output, a "folded cascode" op amp can be used. The primary advantage of the folded structure lies in the choice of the voltage levels because it does not "stack" the cascode transistor on top of the input device.

The folding idea depicted can easily be applied to differential pairs and hence operational amplifiers as well. the resulting circuit replaces the input NMOS pair with a PMOS counterpart. Note two important differences between the two circuits. .one bias current, Iss, provides the drain current of both the input transistors and the cascode devices, whereas in the input pair requires an additional bias current. In other words, Issi = lss/2 + /D3. Thus, the folded

cascode configuration generally consumes higher power. In Fig, the input CM level cannot exceed Vb1-Vas3 + VTH1. Whereas, it cannot be less than Vb1 -Vas3 +VTHl It is therefore possible to design the latter to allow shorting its input and output terminals with negligible swing limitation.

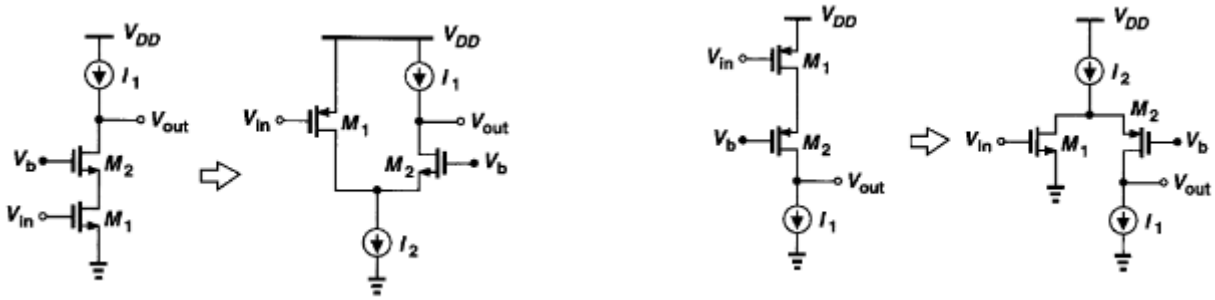

Fig 2.4 : Folded cascade amplifiers

Telescopic & folded-Cascode op amps: Discussion

The overall voltage swing of a folded-cascode op amp is only slightly higher than that of a telescopic configuration. This advantage comes at the cost of higher power dissipation, lower voltage gain, lower pole frequencies, and higher noise.

Folded-cascode op amps are used quite widely, even more than telescopic topologies, because the input and outputs can be shorted together and the choice of the input common-mode level is easier.
In a telescopic op amp, Three voltages must be defined carefully: the input CM level and the gate bias voltages of the PMOS and NMOS Cascode transistors.

Folded-Cascode configurations only the latter two are critical. In folded-cascode op amps, the capability of handling input CM levels are close to one of the supply rails.

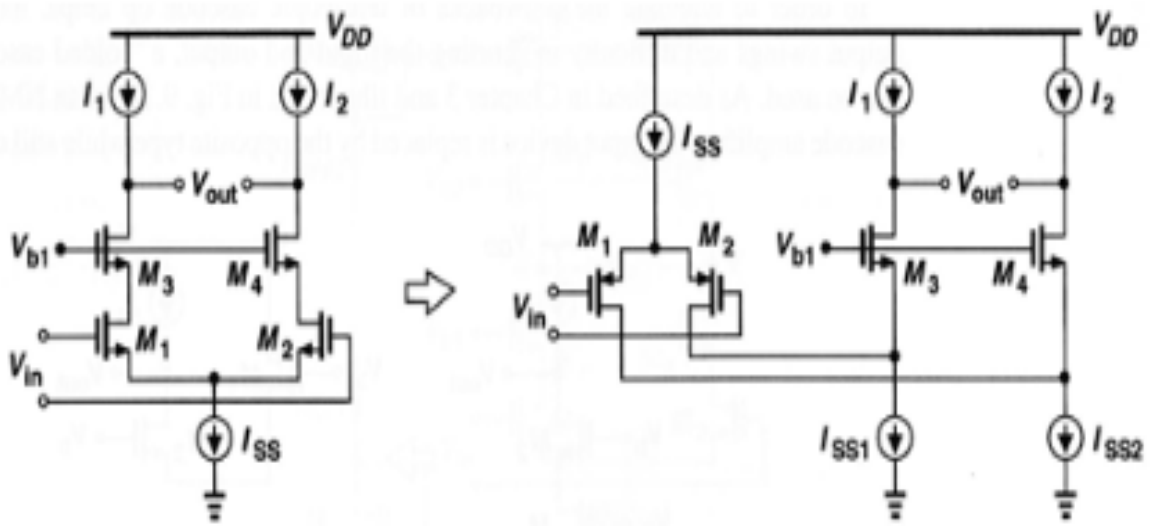

Fig 2.5 : Telescopic and folded Cascode topologies

2.2 TWO-STAGE OP AMPS

The below figure, Figure 2, shows the basic block diagram with all the building blocks of a simple two-stage op-amp. Each box in the figure, i.e. Amplifier A1 and A2, Compensation circuit and Biasing circuit, can be replaced with an actual circuit implemented in modern VLSI technology.

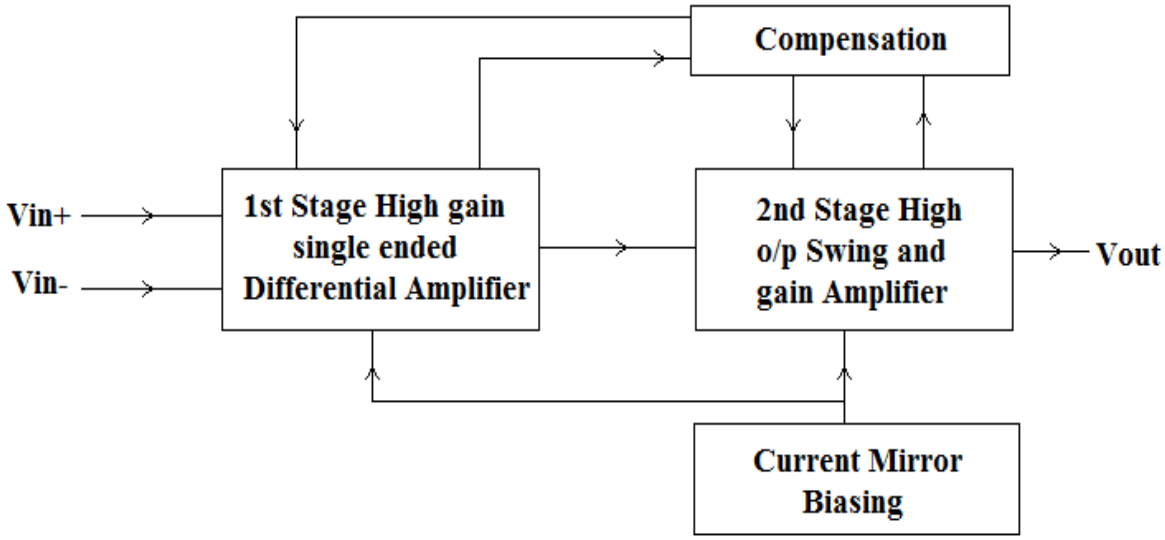

Figure 2.6: Basic block diagram of two-stage op-amp.

For the design of a two-stage op-amp, we have two amplifiers: A1 and A2. We have chosen a simple differential pair amplifier with high immunity to noise signals for the input amplifier A1 and a common source amplifier with a high gain for the output amplifier A2.

Apart from the two amplifiers, we have chosen a current mirror circuit as the biasing circuit and Capacitance compensation for the compensation circuit block. The chosen current mirror circuit is free from voltage sources; utilizing single current reference source. The frequency compensation circuit consists of Capacitor between the output of stage 1 and output of stage 2.

The amplification of signal is a very essential function in most of the analog circuits as well as the digital circuits. In the design for input amplifier (A1), a fully differential (in and out) pair with current mirror biasing has been employed. One of the important advantages of the differential operation over

The single-ended one is its higher immunity to the environmental noise. For output stage, a common source amplifier has been used in order to provide a large gain in the output stage. The advantage of a simple common source (CS) amplifier over a differential pair (Diff –amp) is its high output swing.

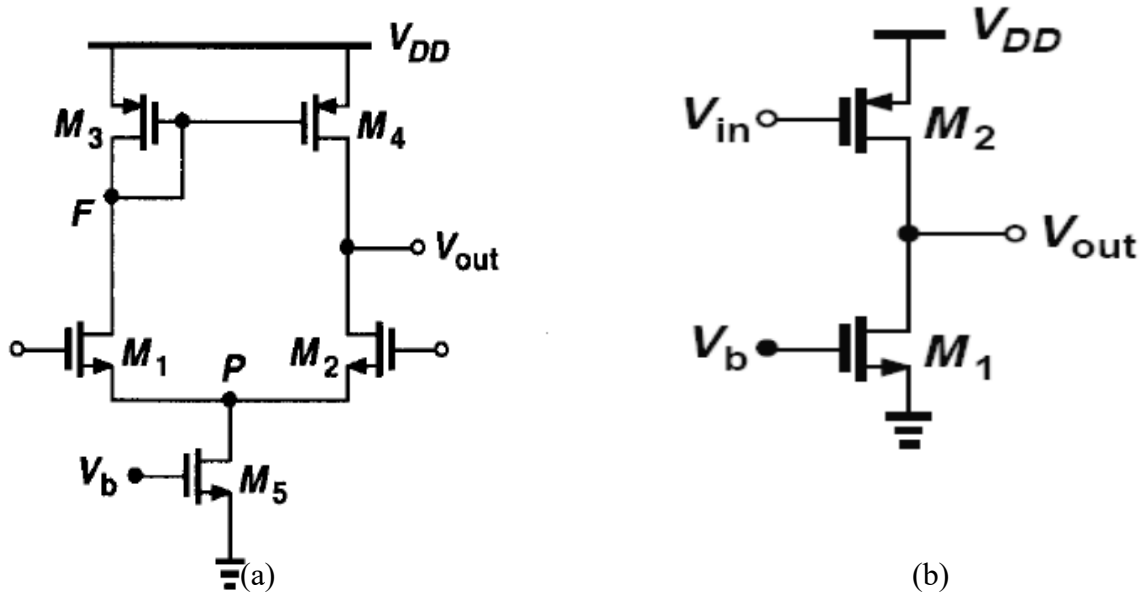

Figure 3: Input and Output stage amplifier:
(a) Differential pair amplifier (A1)
(b)Common source amplifier (A2)

Input Stage Amplifier:

In Differential pair amplifier A1 stage, M1 and M2 are the input NMOS devices and whose transconductances appear in the expression for the dc gain of the op-amp. These devices should be kept wide enough, operating with small overdrive voltage, so that they can produce a high gain and a high Input Common Mode Rejection Ratio (ICMR). The PMOS devices M3 and M4 devices should exhibit high output resistance when we want high gain, thus we need to keep them long enough. The tail transistor M5 should roughly have overdrive voltage which is twice the overdrive voltage of the input devices. This makes all the transistors to have the dimensions which roughly are of the same order. The output intrinsic resistances of M1 or M2 device should be roughly be equal to the M3 or M4 device so as to get a high effective output resistance, and thus, the high DC gain.

Output Stage Amplifier:

In common source output amplifier A2 stage, the transconductance of input PMOS device, M2, should have a larger value and the NMOS device M1, should have larger value of output resistance. Equalizing of output resistance of devices will optimize the overall effective resistance, thus the gain of overall system. Biasing voltages Vb1and Vb2 will be derived by the current mirror circuit by deciding the dimensions of devices used in biasing circuit.

The op amps studied thus far exhibit a "one-stage" nature in that they allow the small-signal current produced by the input pair to flow directly through the output impedance; The gain of these topologies is therefore limited to the product of the input pair transconductance and the output impedance. We have also observed that cascoding in such circuits increases the gain while limiting the output swings.

In some applications, the gain and/or the output swings provided by cascode op amps are not adequate. For example, an op amp used in a hearing aid must operate with supply voltages as low as 0.9 V while delivering single-ended output swings as large as *0.5* V

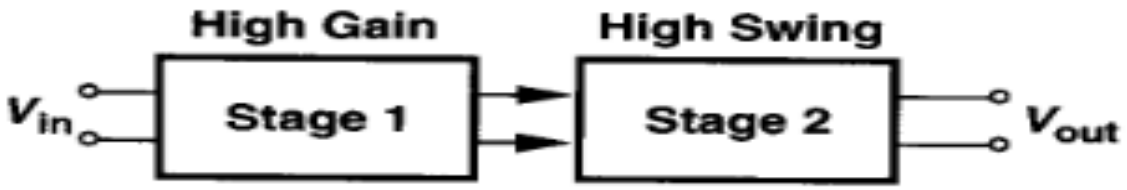

Fig 2.6: Block diagram of two stage Op-amp

Each stage can incorporate various amplifier topologies studied in Previous sections, but the second stage is typically configured as a simple common-source Stage so as to allow maximum output swings.

Can we cascade more than two stages to achieve a higher gain?

Each gain stage introduces at least one pole in the open-loop transfer function, making it difficult to guarantee stability in a feedback system using such an op amp. For this reason, op amps having more than two stages are rarely used.

Simple implementation of a two-stage op amp

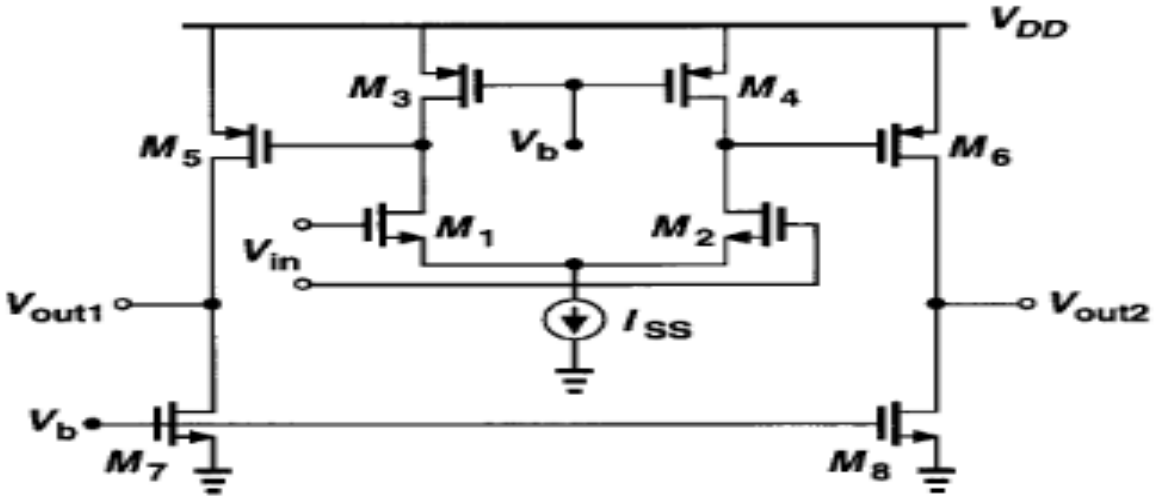

Fig 2.7 : Simple Implementation of Two stage opamp

To obtain a higher gain, the first stage can incorporate cascode devices, as depicted Fig 2.8 With a gain of, say, 10 in the output stage, the voltage swings at X and Y quite small, allowing optimization of M_1 - M_8 for higher gain.

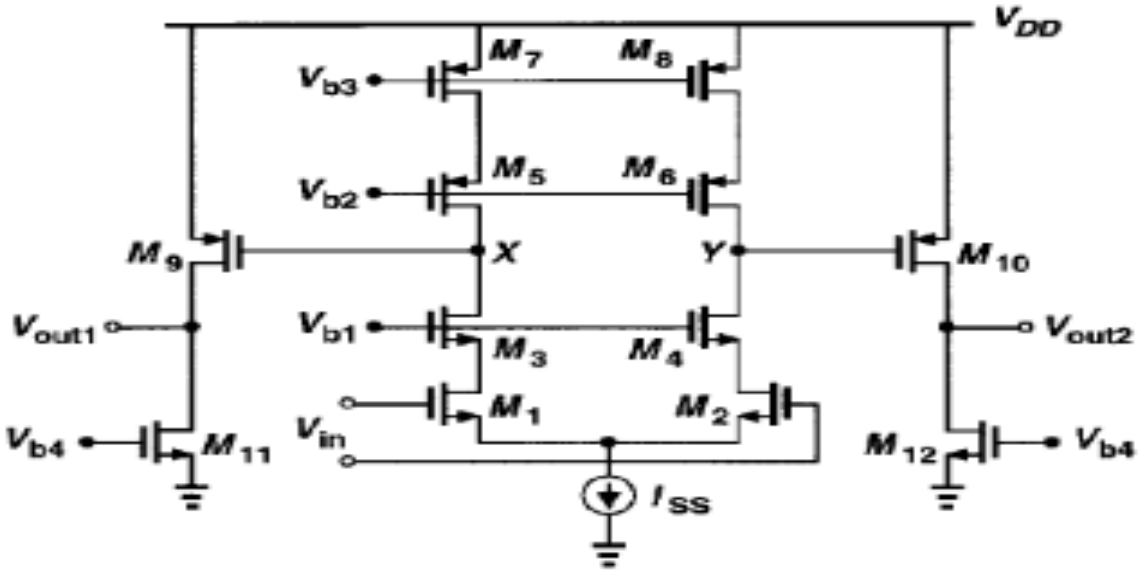

Fig 2.8 : Two stage opamp employing cascoding

TABLE 2.1 :COMPARISON OF PERFORMANCE OF VARIOUS OP AMP TOPOLOGIES

	Gain	Output Swing	Speed	Power Dissipation	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded Cascode	Medium	Medium	High	Medium	Medium
Two stage	High	Highest	Low	Medium	Low

CHAPTER 3

RECYCLING FOLDED CASCODE TOPOLOGY AND ADAPTIVE BIAISNG

Recycling folded Cascode is basically a modified folded Cascode where the load transistor also acts as a driving transistor, hence, enhancing the current carrying capability of the circuit. Recycling folded Cascode is obtained by splitting the input transistors and the load transistor. The cross-over connections of these current mirrors ensure that the small signal currents are added at the sources of M1, M2, M3 and M4 and are in phase.

This is called as recycling folded cascode (RFC), as it reuses/recycles the existing devices and currents to perform an additional task of increasing the current driving capability of the circuit. The proposed modification in the recycling folded cascode topology involves replacing the transistor M0 with an adaptive-biasing circuit which further enhances the current driving capability of this circuit and hence the speed.

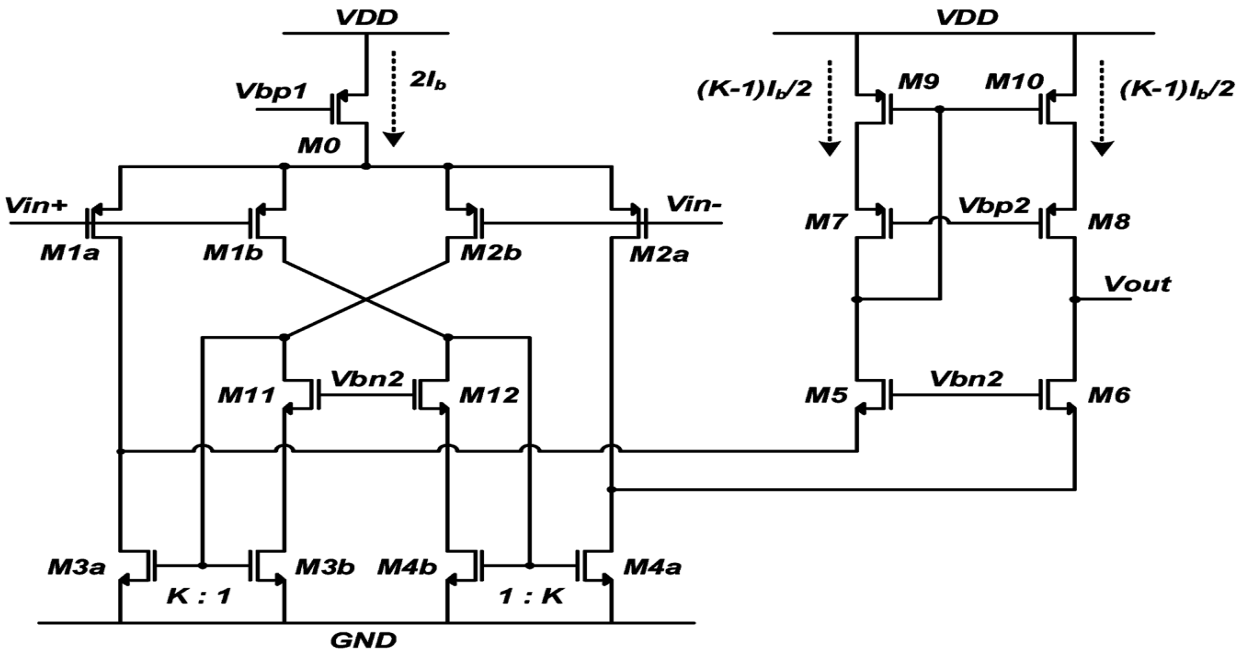

Fig 3.1: The Recycling Folded Cascode (RFC) Amplifier

3.1 ADAPTIVE BIASING DESIGN

Adaptive biasing circuit consists of two level shifters and a current sources .They have a very low output resistance (typically in the range of 20 – 100 ohms). Quiescent current in M1 and M2 is the well-controlled bias current I of the level-shifter transistors assuming M1, M2, M1a and M1b are matched.

Since the ac input signal is applied to both the gate and the source terminals of M1 and M2, the transconductance of this input stage is twice as that of a conventional differential pair.

It is clear that for large Vin,d the output current increases with it, enhancing quadratically the current boosting.The minimum supply voltage of the circuit is vth +3*vdsat. where vdsat is the minimum vds for operation in saturation region. Vth=0.7 and vdsat =0.2 It yields 1.3V. Hence, the circuit is suitable for low voltage operations.

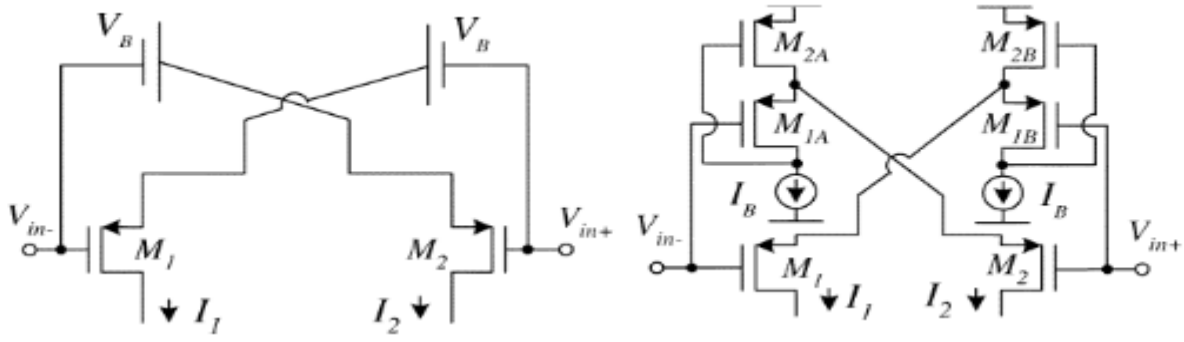

Fig 3.2: Adaptive biasing design using two level shifters (a) Design (b) Circuit

3.2 ANALYSIS AND DESIGN OF THE PROPOSED STRUCTURE

3.2.1 LOW FREQUENCY GAIN

The open loop gain of an operational amplifier determines the precision of the feedback systems employing it. A high open loop gain is a necessity to suppress linearity [6]. The low frequency gain of OTAs is frequently expressed as the product of the small signal transconductance, Gm and the low frequency output impedance, Ro. The low frequency gain of the adaptive recycling folded cascode is almost the same as that of the recycling folded cascode topology.

Both the RFC and adaptive RFC (ARFC) have similar noise injection gains from either supply. Although there is no discernable change in low frequency gain, but extended bandwidth of the adaptive RFC ensures high GBW. Moreover, the extended GBW of the adaptive RFC extends the improved PSRR performance to higher frequencies than the RFC.

3.2.2 PHASE MARGIN

The phase margin is often viewed as a good indicator to the transient response of an amplifier, and is determined by the poles and zeros of the amplifier transfer function. The adaptive RFC shares a dominant pole wp1 determined by the output impedance and capacitive load and a non-dominant pole wp2 determined by the parasitic at the source of M15/M16 .It has a pole zero pair wp3 and wpz (=(k+1)wp3) associated with the current mirrors M7:M8 and M9:M10 However, this pole-zero pair is associated with NMOS devices, which puts it at a high frequency. In addition, adaptive RFC also have a pole due to adaptive current source, ωp4. Due to low Impedance at that node it is pushed to a high frequency.

3.2.3 SLEW RATE

Slew rate is one of the most critical design aspects especially for the kind of circuits where high speed is necessity. To achieve a high slew rate, adaptive biasing circuit plays a vital role. The upper part of the proposed design [5] that is the adaptive biasing circuit consists of four matched transistor M1 M2 M3 M4 cross coupled by two dc level shifters .each level shifter is but using two transistors M1a M2a and M1b M2b and a current source. These level shifters are called Flipped Voltage Followers (FVFs). The dc level shifters must be able to source large currents when the circuit is charging or discharging a large load capacitance. Moreover, they should be simple due to noise, speed, and supply constraint

Analysis of the proposed design shows that there is a significant improvement in its slew rate over the RFC topology. Suppose Vin+ goes high, it follows that M1 and M2 turn off, which forces M9 and M10 to turn off. Consequently, the drain voltage of M9 rises and M2 is turned off whereas M3 is driven into deep triode. This directs drain current into M4 and in turn is mirrored by a factor of 3(K) (M7 ,M8) into M15 , and again by a factor of 1 into (M11 M12). For simplicity, if we ignore any parasitic capacitance at the sources of M1-M2-M3-M4 and follow the similar derivation steps but assuming Vin+ goes low, the result is symmetric slew rate .

Due to presence of the adaptive biasing circuit, this circuit changes current according to the input voltage and hence remains self-biased. It also causes minimal increase in power dissipation as the current only increase proportional to the voltage in one branch and correspondingly decreases in the other one. Since the ac input signal is applied to both the gate and the source terminals of M1-M2 and M3-M4 , the transconductance of this input stage is twice as that of a conventional differential pair. The ac small-signal differential current of the input stage is

Clearly ac small signal current is twice as that in the case of RFC without adaptive biasing circuit. Hence, slew rate has improved in the proposed circuit.

TABLE 3.1 DEVICE SIZES IN IMPLEMENTATION

Device	Proposed design
M_0	-
M_{1a}, M_{1b}	100um/500nm
M_{2a}, M_{2b}	128um/360nm
M_1, M_2, M_3, M_4	64um/360nm
M_{11}, M_{12}	64um/360nm
M_{13}, M_{14}	64um/360nm
M_5, M_6	8um/180nm
M_{15}, M_{16}	10um/180nm
M_7, M_{10}	24um/500nm
M_8, M_9	8um/500nm

TABLE 3.2 BIAS CURRENT IN PROPOSED STRUCTURE

Device	$I_{bias}(\mu A)$
M_{1a}, M_{2a}	181.1
M_{1b}, M_{2b}	86
M_1, M_4	48.79
M_2, M_3	46.29
$M_{11}, M_{12}, M_{13}, M_{14}, M_{15}, M_{16}$	90.63
M_5, M_6	46.29
M_7, M_{10}	139.4
M_8, M_9	46.29

CHAPTER 4

CIRCUIT AND SIMULATION RESULTS

All the simulations were done on OrCAD 16.6 with 0.18 µm technology using a VDD of 1.8V. The load capacitance was taken to be 5.6pF for all the simulations.

Here is the procedure for all the simulations. First of all DC analysis was done to ensure saturation for all transistors. After that, the AC analysis with differential input signal as 1VPP was done to measure the gain, Phase margin.

CIRCUIT IN DC ANALYSIS

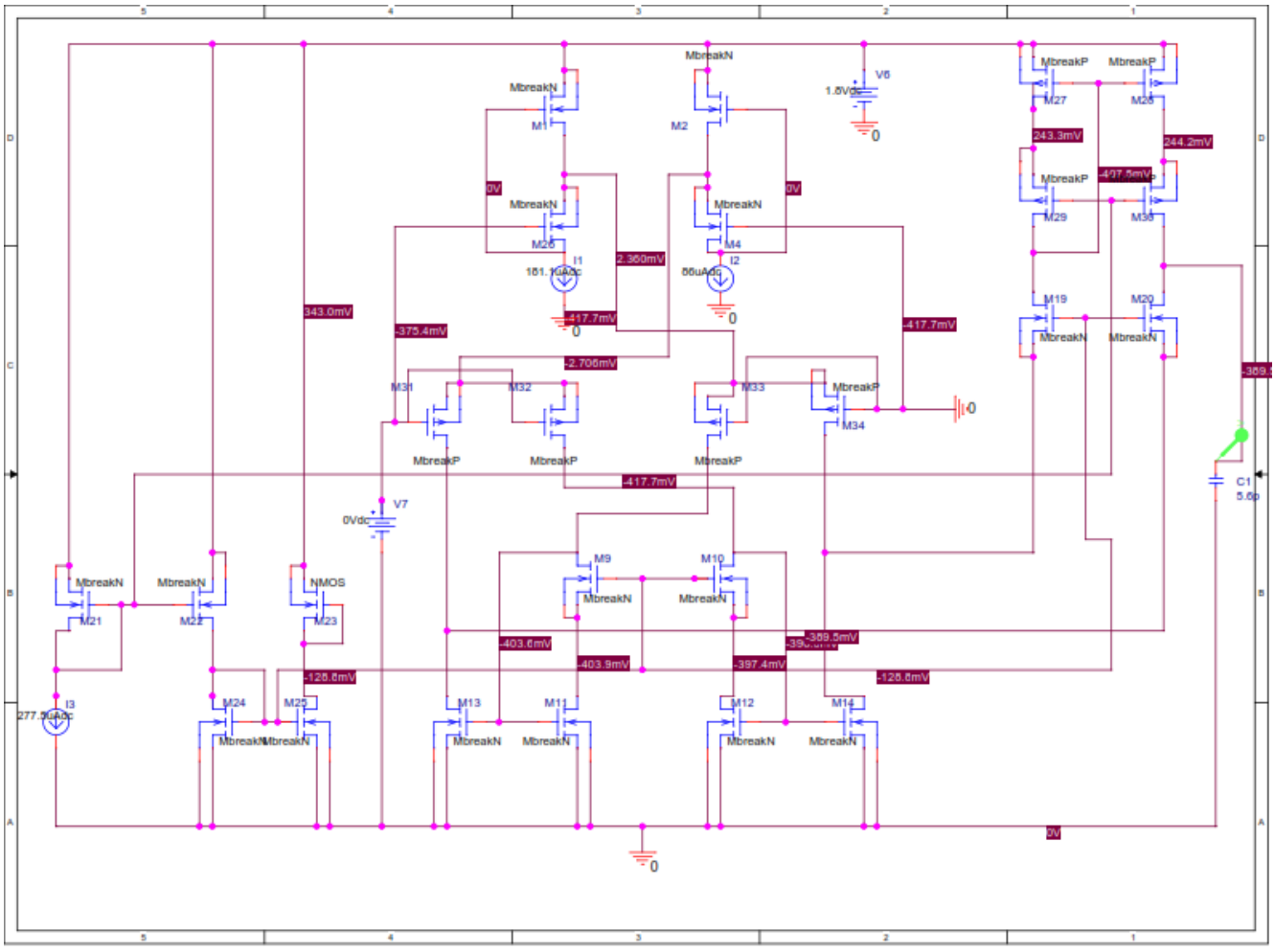

Fig 4.1 : Circuit Diagram in Dc Analysis

DC ANALYSIS OUTPUT

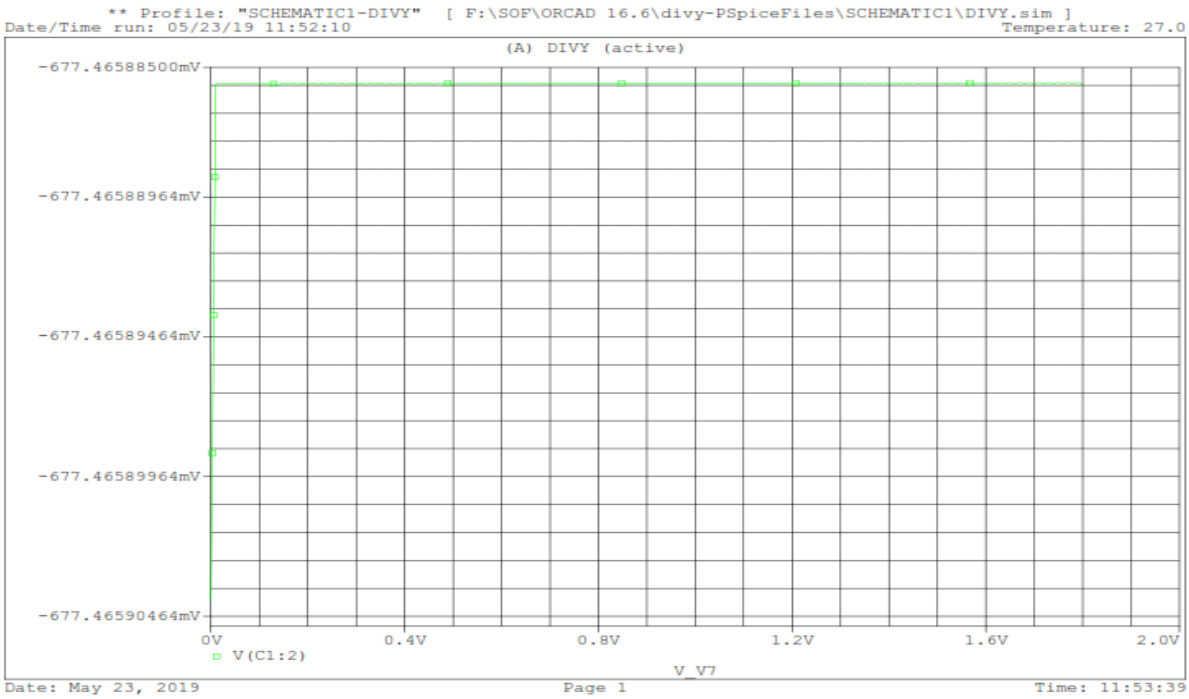

Fig 4.2 : Output in Dc Analysis

Gain is obtained as negative as in cascode amplifier, ensuring all transistors operating in saturation.

CIRCUIT IN AC ANALYSIS

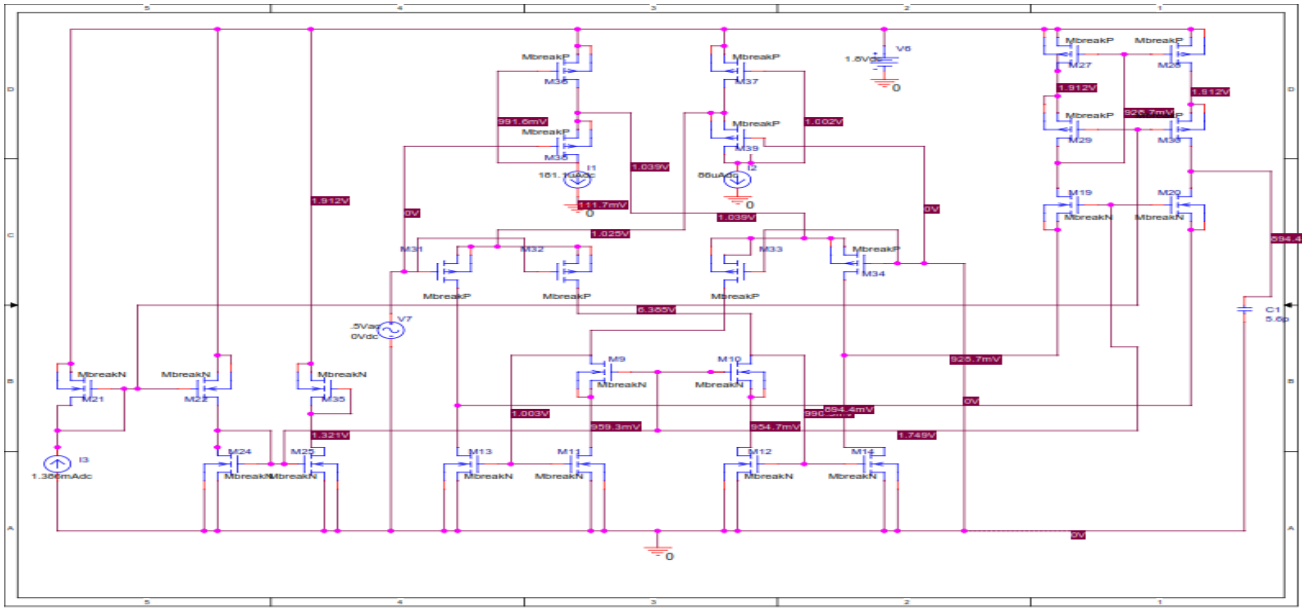

Fig 4.3 : Circuit Diagram in Ac Analysis

GAIN AND PHASE PLOT :

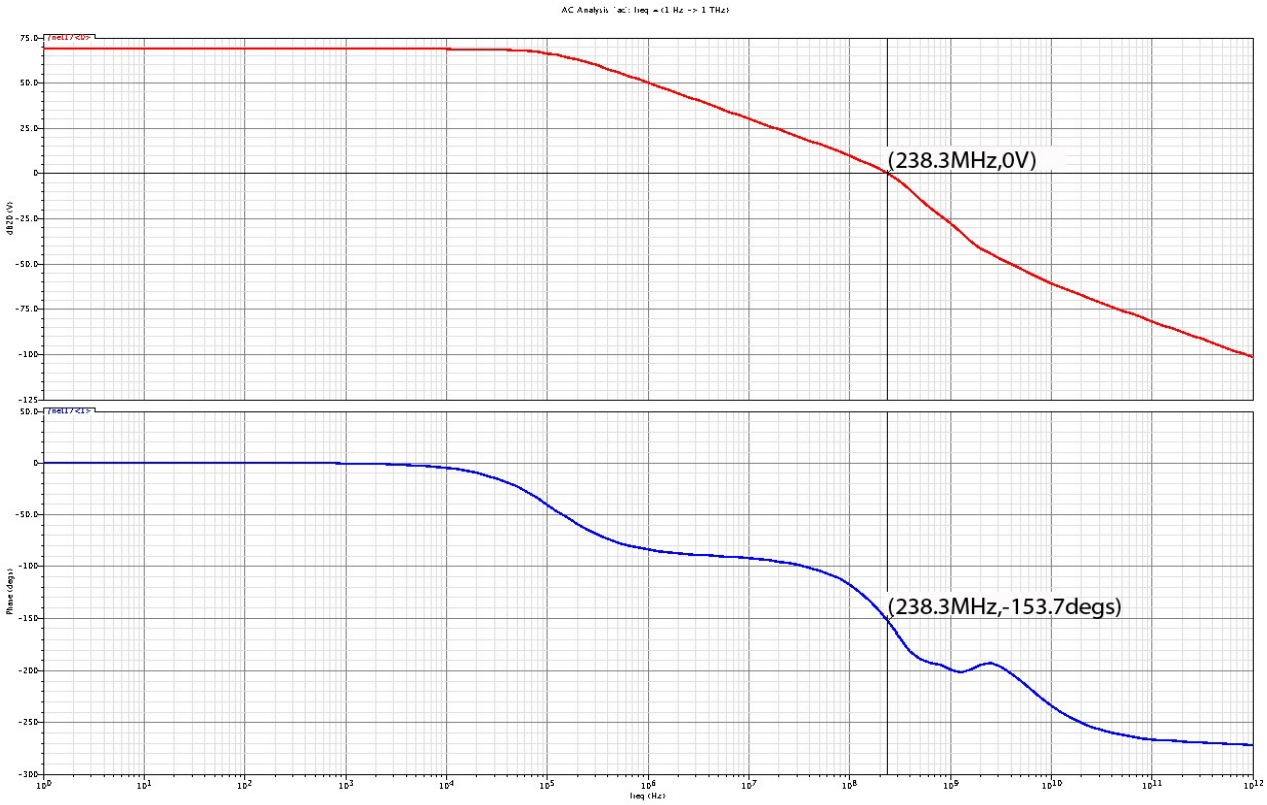

Fig 4.4 Gain and Phase plot (plotted in Virtuoso)

Table 3.3. Results comparison with RFC

Parameters	Proposed structure	RFC
DC Gain(dB)	68.48	71
UGB(MHz)	247.1	153
GBW(MHz)	335.5	172.26
Phase Margin	26.3^{o}	58.1^{o}
Power Dissipation(mW)	2.493	2.18
I(total) (mA)	1.385	1.215
Capacitive load	5.6 pF	5.6 pF
Technology	0.18µm	0.18µm

CHAPTER 5

CONCLUSION

In this report, It has been demonstrated that the proposed design shows a significant improvement over the conventional RFC in terms of UGB, GBW with nearly the same power consumption. The additional adaptive biasing circuit added to the RFC, not only improves its speed and frequency response but also makes the circuit very adaptive to the changes in input voltage and noise fluctuations. With the RFC itself having an adaptive load, this addition of a self-adjusting current source makes it a very flexible, adaptive and self-biased circuit. This feature of the circuit also helps reducing the power consumption by changing currents corresponding to the changes in the input voltage.

FUTURE SCOPE

Given design can be used as a basic building block to implement various op amp Applications.

Operational Amplifier as a Voltage Follower

The proposed design can be implemented with a negative feedback in a voltage follower configuration to test the stability of the design. An input pulse of 1V was given at 5MHz to check its response and functioning. Figure 9 below shows the input and output pulses in a voltage follower configuration. It is evident from the output graph that the delay introduced by the voltage follower is very small. Also, a distortion less and non-sluggish output is achieved as a result of high slew rate and bandwidth provided by the ARFC. Due to high slew rate and bandwidth characteristics, ARFC finds application in various other speed critical circuits such as switched capacitor circuits, comparators etc.

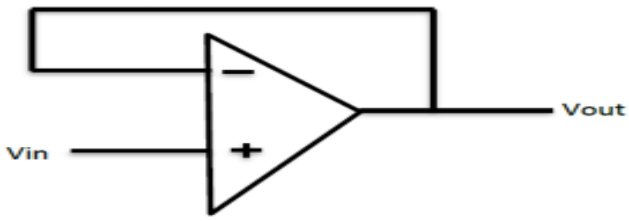

Fig 5.1 : Voltage Follower using Op amp

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