M. Tech (Power Electronics and Systems)

DESIGN AND CONTROL OF VIENNA RECTIFIER FED FULL BRIDGE LLC RESONANT CONVERTER BASED TWO STAGE OFF-BOARD EV CHARGER WITH CC-CV CHARGING ALGORITHM

DISSERTATION/THESIS

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Submitted by:

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CANDIDATE'S DECLARATION

I, **KUSHANK SINGH**, Roll No. 2K21/PES/08 student of M. Tech (Power Electronics & Systems), hereby declare that the project Dissertation titled **"Design and Control of Vienna Rectifier fed Full Bridge LLC Resonant Converter based Two Stage off-Board EV Charger with CC-CV Charging Algorithm"** which is submitted by me to the Department of Electrical Engineering Department, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously submitted for the award of any Degree, Diploma.

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CERTIFICATE

I hereby certify that the project Dissertation titled **"Design and Control of Vienna Rectifier fed Full Bridge LLC Resonant Converter based Two Stage off-Board EV Charger with CC-CV Charging Algorithm"** which is submitted by Kushank Singh, Roll No. 2K21/PES/08, Department of Electrical Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ABSTRACT

This work has three objectives, first objective is designing and controlling of Vienna rectifier. In this objective a complete analysis of three phase Vienna rectifier considering the effect of parasitic in the system for off-board EV charging application is discussed. To improve the dynamic response a modified dual loop control using d-axis and q-axis current controller including the effect of system parasitic in control loops is proposed. The proposed algorithm is compared with different control algorithms viz., dual loop control using hysteresis current controller and dual loop control using d-axis and q-axis current controller with SVPWM. A comparative performance analysis is discussed in terms of dynamic response during system disturbances like load variation, reference DC bus voltage variation and grid side variations. A 50 kW Vienna Rectifier operating at a switching frequency of 200 kHz is used for performance evaluation of all three control algorithms and is validated using MATLAB-Simulink. The second objective is the designing of full bridge LLC resonant converter as well as designing of magnetics for high frequency transformer. In this objective voltage control of LLC resonant converter is designed using pulse frequency modulation (PFM) for controlling the output voltage and analyze the effect of load side and input side variations on the converter. In this, the input is constant 700V DC rather than the Vienna rectifier output to analyze the performance of the converter and it is validated using MATLAB-Simulink. The third objective combines all the analysis involved in first and second objective. In this objective a 50 kW two stage off-Board EV charger is designed for charging a lithium ion battery using constant current (CC)-constant voltage (CV) algorithm. First stage includes three phase Vienna rectifier with power factor correction. The output of the first stage is the DC bus, which acts as an input to the second stage. Second stage includes full bridge LLC resonant converter and a lithium ion battery is connected to the output of second stage. To maintain constant DC bus voltage of 700V and to ensure unity power factor, dual loop control using d-axis and q-axis current control using space vector pulse width modulation (SVPWM) is adopted for controlling Vienna rectifier. Closed loop control for full bridge LLC resonant converter is designed using CC-CV control algorithm and pulse frequency modulation (PFM) to charge the rated 280 V/112 Ah lithium ion battery. The designed system outcomes are validated using MATLAB-Simulink.

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LIST OF ABBREVIATIONS

EV	Electric Vehicle
p.f.	Power Factor
THD	Total Harmonic Distortion
SAE	Society of Automotive Engineers
CHAdeMO	CHArge de MOve
BMS	Battery Management System
PHEV	Plug In Hybrid Vehicle
SoC	State of Charge
C-Rate	Charging/ Discharging Rate
PFC	Power Factor Correction
DBR	Diode Bridge Rectifier
EMI	Electro Magnetic Interference
CICM	Continuous Inductor Current Mode
CC	Constant Current
CV	Constant Voltage
ZVS	Zero Voltage Switching
ZCS	Zero Current Switching
LLC	Inductor Inductor Capacitor
q-axis	Quadrature- axis
d-axis	Direct- axis
PFM	Pulse Frequency Modulation
SVPWM	Space Vector Pulse Width Modulation
PI	Proportional Integral
ESR	Equivalent Series Resistance
FFT	Fast Fourier Transform
FHA	First Harmonic Approximation
AWG	American Wire Gauge
MLT	Mean length turn
MPL	Magnetic path length
Ah	Ampere Hour

LIST OF SYMBOLS

Q_a, Q_b, Q_c	Bidirectional switches in Vienna rectifier
V_{abc} ,I_{abc}	rms grid voltage, rms grid current
V_{c1}, V_{c2}	Bus capacitors voltage
I_N	Capacitor midpoint current
f_{sw}	switching frequency
Δi_{ppmax}	maximum ripple in the current through filter inductor
f_s	grid frequency
C_o, r_c	bus capacitor, ESR
L_s, (r_s)	input filter inductance, source resistance
ΔV_c	mismatch between the bus capacitors voltage
I_{abc}*	reference grid current
V_{dc}*	reference bus voltage.
V_{qref}, V_{dref}	reference q-axis, d-axis voltage
I_{qref}, I_{dref}	reference q-axis, d-axis current
I_{SWrms}, V_{SWavg}	rms current, average voltage across bidirectional switch
I_{Crms}	rms current through bus capacitor
I_{Srms}	input rms current
V_{Davg}, I_{Drms}	average diode voltage, rms diode current
$R_{DS(on)}$, r_D	on resistance of switch, diode
t_s	settling time
Q_1,Q_2,Q_3,Q_4	controlled switches on primary side
f_o	resonating frequency
L_r ,C_r	Resonating inductor, Resonating capacitor
L_m ,L_x	Magnetizing inductance, inductance ratio
Q	Quality factor
K_{pv} and K_{iv}	PI controller gains for the voltage control loop of FBLLC converter
V_{bus}	DC bus voltage
V_{bus}^*	reference DC bus voltage
Kp_{vbus} and Ki_{vbus}	PI controller gains for output bus voltage loop
Kp_{vc} and Ki_{vc}	PI controller gains for bus capacitors voltage balance loop
Kp_{iq} and Ki_{iq}	PI controller gains for q-axis current loop
Kp_{id} and Ki_{id}	PI controller gains for d-axis current loop
V_{bat}	Battery voltage
V_{bat}*	reference battery voltage
f_{sw}*	reference frequency
I_{bat}	Battery current
I_{bat}*	reference battery current
K_{pcv} and K_{icv}	PI controller gains for CV charging
K_{pcc} and K_{icc}	PI controller gains for CC charging
V_{bat}^{th}	Battery threshold voltage
I_{bat}^{lim}	Limiting current

CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION

In today's growing world the fossils fuel are diminishing at an alarming rate, which leads to the researchers to find alternative fuel for vehicles [1]-[3]. That's why development in EV batteries is going on to achieve higher power density and also reduce the size of battery. An efficient Battery Management System (BMS) also required along with the battery which helps the battery to avoid certain threshold parameters, like prevents battery to achieve temperature rise beyond certain limits [4]. The growing future of EVs needs more reliable and efficient power electronics systems [5]. Advancements in power electronics converters involve a complex control algorithm. The EV charging system has a great involvement of the AC grid. A battery can be charged using a charging station but its impact on the AC grid has to be analyzed [6]. There are many power factor correction methods that have been adopted in literature which include advancement in PFC boost using wide band gap devices in which we can operate at high switching frequency which indirectly reduces the size of the system [7]. For off-board EV charging applications a three-phase power factor correction method needs to be implemented to improve the injected grid current. One of these topologies includes Vienna Rectifier with power factor correction.

The major concerns with the electric vehicle is the range of vehicle in a single charge and charging time required for battery. Fast charging is the only available option when the vehicle owner is in between the journey. There are both unidirectional and bidirectional EV chargers for charging the battery [8]. Both have some advantages and limitations, unidirectional chargers are easy to interconnect as compare to bidirectional charger as well have less tedious control, as controllable switches are also less. But bidirectional charger features supply of battery energy to the grid. The range anxiety in other way can be minimized by using plug in hybrid vehicle (PHEV) [9], [10], in which the vehicle can switched to the fuel system when battery is discharged and provides an upper hand for the vehicle owner.

In the growing market of EVs globally, unavailability of fast charging stations at certain distance is the main reason for the range anxiety among the EV users [11]. Therefore, the main focus of various charging companies is towards the charging of electric vehicles at higher charging rates under the EV standards [12]. Fast charging requires efficient power converters which are capable of transferring higher power to achieve high C-rate. Most of researchers working on the new topologies to make grid more stable during charging, as the THD in the injected grid current without any power factor correction (PFC) control is more than 5% which is not acceptable according to Indian EV standards [6].

There are various level of charging: level 1, level 2 and level 3 charging [5], [13]. Level 1 are mostly used in residential areas and have low ratings of up to 2 kW, which supports only slow charging and can take around 12 hours to charge to 100% SOC. Level 2 charging is adopted in residential as well as working premises, public places etc. which is capable of improving the C-rate of the battery and take around 6 hours to charge to 100% SOC. The ratings of level 2 charging goes up to 20 kW. Level 3 or DC fast charging are the most focus area nowadays due to their higher ratings ranging from 50 kW to several hundred kW. These charging station are provided among various areas of the cities and are expanding at a rising rate. Level 3 provides higher C-rates which helps the user to charge their vehicles up to 80% SOC in about 20 minutes and can take up to 1 hour depending on the rating of charging station. Level 1, level 2 chargers are characterized as on- board chargers and level 3 chargers as off board chargers.

The various levels of charging can be classified as:

a) **Level 1 charging:**

   Level 1 charging is considered as slow charging which is mostly used by the user at residential area and have around 2 kW power rating. Level 1 charging can take up to 12 hours for full charge.

b) **Level 2 charging:**

   Level 2 charging is considered as moderate charging which is mostly used by the user at private or public outlets and have up to 20 kW power rating. Level 2 charging can take up to 4-6 hours for full charge based on EV charger rating.

c) Level 3 charging:

Level 3 charging is considered as DC fast charging which is available at charging stations and have around 50 kW- 100's of kW power rating. Level 3 charging can take up to 30-40 minutes for charging up to 80% SoC based on EV charging station rating.

Level 1 and level 2 charging are classified as on-board charging and level 3 charging is considered as off-board charging. SAE J1772 connector can be used for level 1 and level 2 charging which consists of AC pins on top for ac charging and two DC connectors at bottom for dc charging as in Fig.1.1. For level 3 charging CHAdeMO connectors are widely considered [14].

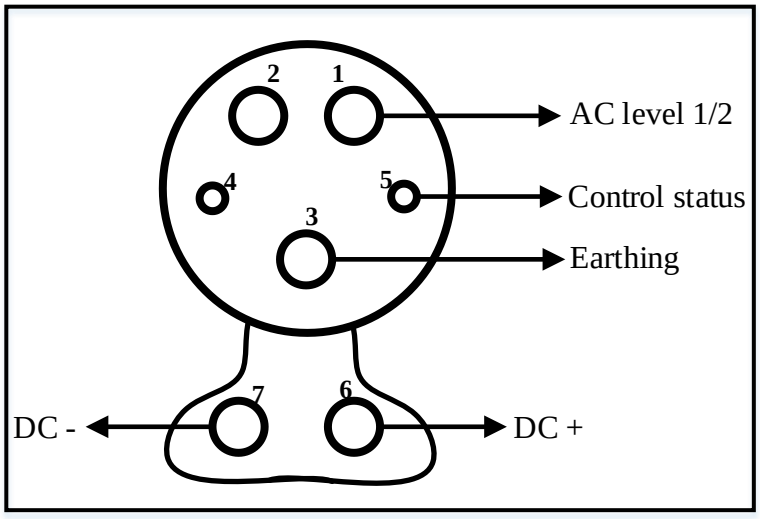


Fig.1.1. Port diagram of SAE J1772

But the main concern regarding EV charging is the availability of fast charging stations at certain distance which requires more efficient and high power density power converters. High power density can provides charging of EV battery at higher C-rate which also reduces the range anxiety among the EV users. Another concern is the grid side disturbances when charging the electric vehicles. As, AC/DC converters are used to convert AC to DC due to which the grid side current becomes distorted and THD becomes quite high which is not recommended according to EV standards in India. Various power factor correction (PFC) methods are employed when designing an EV charger to make grid current in phase with the grid voltage [15]-[18].

There are various power factor correction topologies which are adopted for improving the Total Harmonic Distortion (THD) of the grid current injected to the grid and one of them is boost PFC [19],[20]. The circuit description includes the AC grid at the input, followed by the Diode Bridge Rectifier (DBR) which provides a pulsating DC at the output. This pulsating DC acts as an input to the DC-DC boost converter which consists of inductor at the input which features to make input current continuous. In boost converter the controlling switch is the low side switch which ease its hardware designing as low side is connected to the ground. At the output, a capacitor is connected to maintain a certain level of DC bus voltage. A load is connected across the bus capacitor as in Fig.1.2.

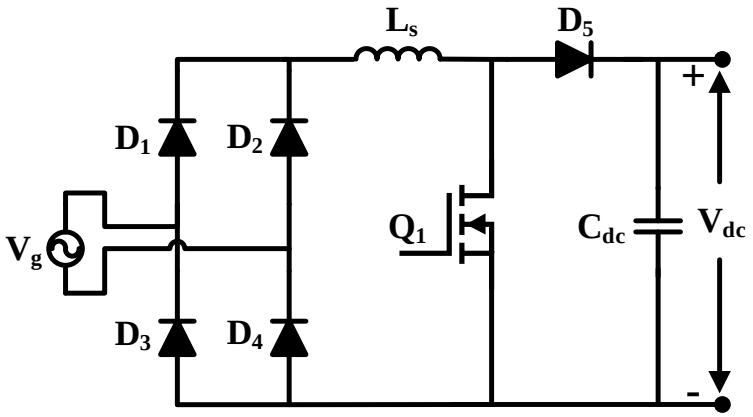


Fig.1.2. Circuit description of boost PFC

Interleaving of input inductors provide the features of reduced inductor and also minimizes the inductor current ripple [21], [22] as in Fig.1.3.

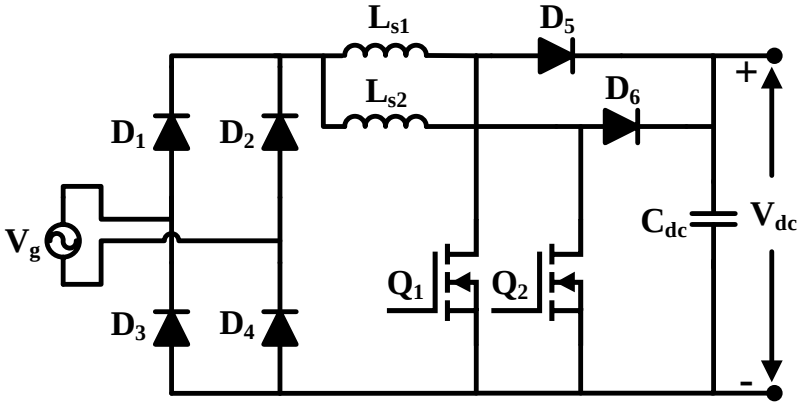


Fig.1.3. Circuit description of interleaved boost PFC

1.2 BACKGROUND

There are on-board chargers as well as off-board charger for charging the EV battery. On-board charger includes single phase power factor correction (PFC) to mitigate the effect on the grid side by reducing the THD below 5% as per Indian EV standards. In [23], the authors have discussed the various PFC topologies for on-board charger. The various PFC topologies also reduces EMI, reduces higher order harmonics. The interleaved boost PFC significantly reduces the EMI due to interleaving which provides the 180˚ phase shifting between the interleaved inductor currents. It also features operation in continuous inductor conduction mode (CICM). In this topology the device count is high with medium costing but it offers efficiency between 91%-97% [24], [25]. In bridge-less boost the EMI is high as input voltage is always floating w.r.t. output voltage. It also operates in the CICM and this topology offers reduced less number of devices as compare to previous one, due to which the cost is less and it offers efficiency between 94%-96% [26]. In bridge-less interleaved boost the EMI gets reduced due to interleaving. It also operates in the CICM and requires more number of devices due to which the costing is increased. It offers the efficiency between 94%-99% [24], [27]. In semi-bridgeless boost the EMI is medium as input and output voltage have same ground. It also works in CICM with moderate number of devices due to which the cost is moderate and offers efficiency between 96%-99% [28]. In phase shifted semi-bridgeless boost the EMI is medium and it also works in CICM. The number of devices in operation is moderate due to which costing is moderate but it offers efficiency between 93%-99% [24]. In bridgeless dual boost the EMI is high but the number of devices used is very less due to which the cost is very less compared to other topologies and also works in CICM [29]. In totem-pole bridgeless boost the EMI is high as it works in discontinuous inductor conduction mode but number of devices used is less due to which cost is less and it offers efficiency between 96%-98% [30].

Various power factor corrections topologies are considered to make the grid current in phase with the voltage to minimize the THD below 5% based on the EV standards [31]. These topologies include interleaved boost PFC which is the simplified topology for power factor correction and features minimized inductor current ripples. In [32] the authors proposed a bridge less boost PFC topology for an EV charger which features no diode bridge

rectifier and improved efficiency. A comparison was also made among PFC boost, interleaved boost, semi-bridge less boost and totem pole boost on the basis of the system complexity and efficiency.

For off-board EV chargers three phase power factor correction is required at the front end to minimize the disturbances in the grid. In [33], the authors proposed three phase interleaved buck-boost with power factor correction is proposed. In this topology the working is in discontinuous current conduction mode. It provides high power density and efficient power conversion with reduced THD of 2.52 % and near to unity power factor. Other three phase power factor correction is implementing Vienna rectifier with power factor correction. Vienna rectifier is a 3-level converter which provides the operation of AC/DC conversion and with proper control algorithms design, power factor can be achieved near to unity and THD less than 5%. This will mitigate the effects of grid current in the system. Vienna rectifier provides high power density and efficient power conversion that's why it can be utilized in higher ratings off-board charger.

In [34] balancing of the output capacitor voltages in Vienna Rectifier using modified Discontinuous PWM to reduce the error between the bus capacitor voltages and to operate at high frequency is proposed. The authors in [35] proposed a hysteresis current control which reduces the computation complexity and is easy to implement. To reduce the THD of grid current a lot of research involves Space Vector PWM control [36]-[37]. In [38], the authors also included the system parasitic in Vienna Rectifier but the effect of parasitic is not included in the controlling loops.

For off-board EV charging, non- isolated dc-dc converters are not significant due to their limitations in power ratings and size. The full bridge LLC converter features higher power density, can be operated at higher switching frequency and also features ZVS of the primary side controlled switches based on the design consideration of the converter which minimizes the losses to a greater extent. The size of the converter can also be reduced when we are operating at higher switching frequency. But the designing of LLC converter is a tedious task due to various design consideration but its features attracts it for EV charging applications [39], [40].

There are various types of batteries which includes lead acid (Pb/PbO_2) battery, lithium ion polymer (LiPo), nickel metal hydride (NiMH) batteries. Lithium ion batteries are preferred over other batteries in electric vehicles (EVs) due to their lighter weight and decent life cycle. To maximize the life of the lithium ion batteries CC-CV charging algorithm is preferred over CC or CV charging as it is more likely to mimic the chemistry involved in the battery. CC charging for fast charging can lead to temperature rise when the threshold voltage is reached. In CC-CV charging the CV mode is activated when the battery is charged up to a threshold voltage. In [41] the authors compared various charging algorithm including CC-CV, multi- stage CC, fuzzy logic etc. and conclusion are made on the basis of charging time and temperature effect on the battery.

1.3 THESIS MOTIVATION

In the current scenario of EV market, availability of off-board EV charger at certain distance is the major concern. This will reduce the range anxiety among the users and will rise the sales of EVs and make growth of EV market in India stable. That's why this research area was selected to work upon and to add some contribution in the power converters for off-board EV charging. In this work a complete two stage off-board is designed for EV charging using constant current (CC) - constant voltage (CV) algorithm. Vienna rectifier is designed for power conversion from AC to DC and three control algorithms is designed for controlling the DC bus as well improve the power factor by mitigating the grid side effects. All the three control algorithms is compared in terms of dynamic variations and grid side variations in the system. In second stage a full bridge LLC resonant converter is designed by ensuring zero voltage switching (ZVS) in the primary side controlled switches and zero current switching (ZCS) in the secondary side diodes. A lithium ion battery is charged using proposed CC-CV charging algorithm. The charging will be at higher C-rate which will reduce the charging time.

1.4 THESIS OBJECTIVE

This work has three objectives, first objective is designing and controlling of Vienna rectifier. In this objective a complete analysis of three phase Vienna rectifier considering the effect of parasitic in the system for off-board EV charging application is discussed. To

improve the dynamic response a modified dual loop control using d-axis and q-axis current controller including the effect of system parasitic in control loops is proposed.

The second objective is the designing of full bridge LLC resonant converter as well as designing of magnetics for high frequency transformer. In this objective voltage control of LLC resonant converter is designed using pulse frequency modulation (PFM) for controlling the output voltage and analyze the effect of load side and input side variations on the converter. In this, the input is constant 700V DC rather than the Vienna rectifier output to analyze the performance of the converter.

The third objective combines all the analysis involved in first and second objective. In this objective a 50 kW two stage off-Board EV charger is designed for charging the rated 280 V/112 Ah lithium ion battery using constant current (CC)-constant voltage (CV) charging algorithm.

1.5 THESIS ORGANIZATION

This thesis consists of complete design and control of the two stage off-board EV charger for charging a lithium ion battery using CC-CV charging algorithm. The outline of this this thesis is as follows:

Chapter 1: This chapter gives brief introduction regarding EV charging issues, different levels of EV charging and different type of connectors. It also provides brief background of this research topic. This chapter also provides motivation and objective of this thesis and then thesis organization.

Chapter 2: This chapter consist of circuit analysis of Vienna rectifier which includes its modelling, design as well as different modes of operation.

Chapter 3: This chapter explains the three control algorithms i.e. dual loop control using hysteresis current controller, dual loop control using d-axis and q-axis current controller with SVPWM and proposed modified dual loop control using d-axis and q-axis current controller including the effect of system parasitic in control loops. A comparative performance analysis is discussed in terms of dynamic response during system disturbances like load variation, reference DC bus voltage variation and grid side variations.

Chapter 4: This chapter includes full bridge LLC resonant converter description and analysis. It also includes various modes of operations and complete design of LLC circuit as well as magnetic design is explained with proper calculations.

Chapter 5: This chapter explains the controlling of full bridge LLC resonant converter which includes pulse frequency modulation (PFM) control and its dynamic performance is evaluated.

Chapter 6: In this chapter, by considering all the analysis performed in previous chapters, a two stage off-board charger is discussed. CC-CV charging algorithm is also discussed for charging a rated lithium ion battery.

Chapter 7: In this chapter conclusion of this work is summarized and future work is discussed.

CHAPTER 2

DESIGN AND ANALYSIS OF VIENNA RECTIFIER

2.1 INTRODUCTION

Vienna Rectifier is a three-level AC-DC converter that maintains a desired DC voltage at the output. It also features input power factor correction and eliminates harmonics which leads to a reduction in Total Harmonic Distortion (THD) [42]. The circuit includes three input filter inductances, one for each phase, which helps out in the reduction of input current ripples and also performs the function of boosting. The second stage includes the diode bridge rectifier containing six power diodes, two diodes for each phase. The additional elements in the Vienna Rectifier are the three bi-directional switches Q_a, Q_b and Q_c in each phases due which it is called as multilevel converter. The last stage is the DC bus capacitors which helps to maintain the required DC bus voltage and also reduce the ripples in the output voltage. The circuit diagram of Vienna rectifier is shown in Fig.2.1.

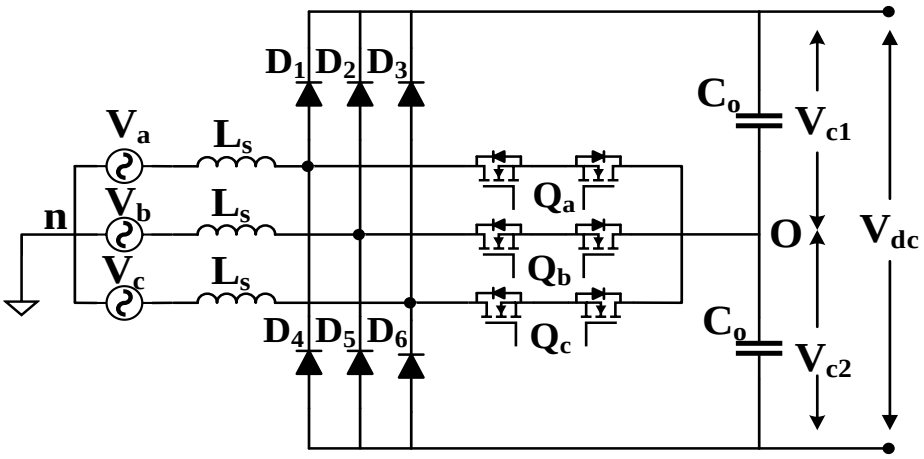


Fig.2.1. Three phase Vienna Rectifier circuit diagram

The voltage applied between the phase and capacitor midpoint is decided by the current direction as well as the switching of the bi-directional switches. When all the bidirectional switches are ON then voltage is zero, when bidirectional switch is OFF and

either of D1, D2, D3 conducts then voltage is $+V_{dc}/2$. Voltage is $-V_{dc}/2$ when either of D4, D5, D6 conducts. This can be generalized as,

$$V_{xo} = \frac{V_{dc}}{2} * sign(i_x)\{1 - Q_x\} \tag{2.1}$$

Where, $sign(i_x)$ is decided by the current direction, Q_x is switching state of the bi-directional switch and x = a, b, c.

The voltage between neutral (n) and capacitor midpoint is,

$$V_{no} = \frac{V_{dc}}{6}(Q_a + Q_b + Q_c) \tag{2.2}$$

The voltage between rectifier input and neutral 'n' is,

$$V_{xn} = V_{xo} - V_{no} \tag{2.3}$$

Space vectors for Vienna rectifier can be depicted as,

$$\vec{V}_{ref} = \frac{V_{dc}}{3}\left[Q_a e^{j0} + Q_b e^{j\frac{2}{3}\pi} + Q_c e^{-j\frac{2}{3}\pi} \right] \tag{2.4}$$

Table 2.1. Space vectors of Vienna rectifier

Vectors	No. of vectors	Magnitude
Long vectors	6	$2V_{dc}/3$
Medium vectors	6	$V_{dc}/\sqrt{3}$
Short vectors	6	$V_{dc}/3$
Zero vector	1	0

2.2 MODES OF OPERATION

Vienna rectifier consists of three bi-directional switches which makes eight switching states possible for operation. Based on grid current direction there are six sectors possible, which makes 48 possible states but some of them are redundant states which leads to 25

modes of operation. But in this paper all possible modes of operation for sector 1 is stated in Table 2.2 and in Fig.2.2 to Fig.2.9.

Table 2.2. Sector classification based on grid current polarities

Sector 1	i_a, i_b, i_c = + , - , -	**Sector 4**	i_a, i_b, i_c = - , + , +
Sector 2	i_a, i_b, i_c = + , + , -	**Sector 5**	i_a, i_b, i_c = - , - , +
Sector 3	i_a, i_b, i_c = - , + , -	**Sector 6**	i_a, i_b, i_c = + , - , +

Table 2.3. Voltage magnitude and capacitor mid-point current during each switching state

Switching State	V_{ao}	V_{bo}	V_{co}	I_N
000	$V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$	0
001	$V_{dc}/2$	$-V_{dc}/2$	0	i_c
010	$V_{dc}/2$	0	$-V_{dc}/2$	i_b
011	$V_{dc}/2$	0	0	$-i_a$
100	0	$-V_{dc}/2$	$-V_{dc}/2$	i_a
101	0	$-V_{dc}/2$	0	$-i_b$
110	0	0	$-V_{dc}/2$	$-i_c$
111	0	0	0	0

In Table 2.3 V_{ao}, V_{bo} and V_{co} are the voltage magnitude between phases and capacitor mid-point and I_N is capacitor mid-point current. All modes for a complete sector 1 is explained below,

Mode I: Switches Q_a, Q_b, Q_c are OFF

In this mode of operation, all three bi-directional switches Q_a, Q_b, Q_c are OFF due to which the capacitor mid-point current is zero and the different voltage levels are,

$$V_{ao} = V_{dc}/2,\ V_{bo} = -V_{dc}/2,\ V_{co} = -V_{dc}/2$$

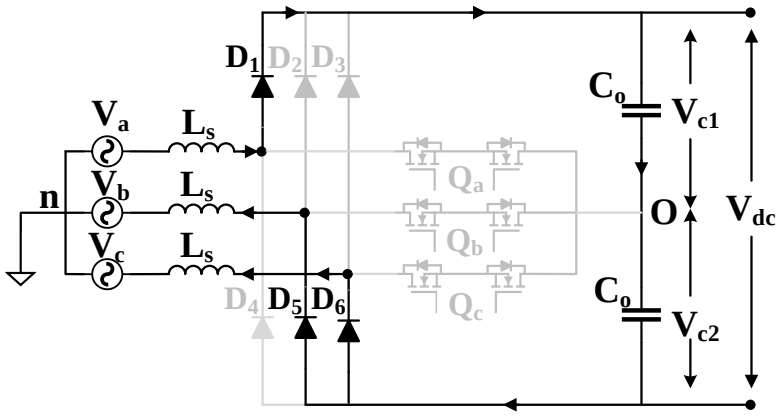


Fig.2.2. Vienna rectifier operation at switching state 000

Mode II: Switches Q_a, Q_b are OFF and Q_c is ON

In this mode of operation, two bi-directional switches Q_a, Q_b are OFF and Q_c is ON due to which the capacitor mid-point current is equal to phase c current and the different voltage levels are,

$$V_{ao} = V_{dc}/2,\ V_{bo} = -V_{dc}/2,\ V_{co} = 0$$

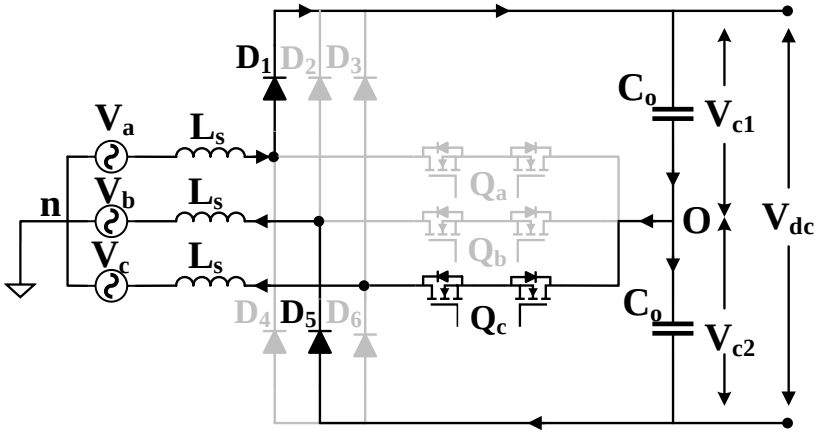


Fig.2.3. Vienna rectifier operation at switching state 001

Mode III: Switches Q_a, Q_c are OFF and Q_b is ON

In this mode of operation, two bi-directional switches Q_a, Q_c are OFF and Q_b is ON due to which the capacitor mid-point current is equal to phase b current and the different voltage levels are,

$$V_{ao} = V_{dc}/2,\ V_{bo} = 0,\ V_{co} = -V_{dc}/2$$

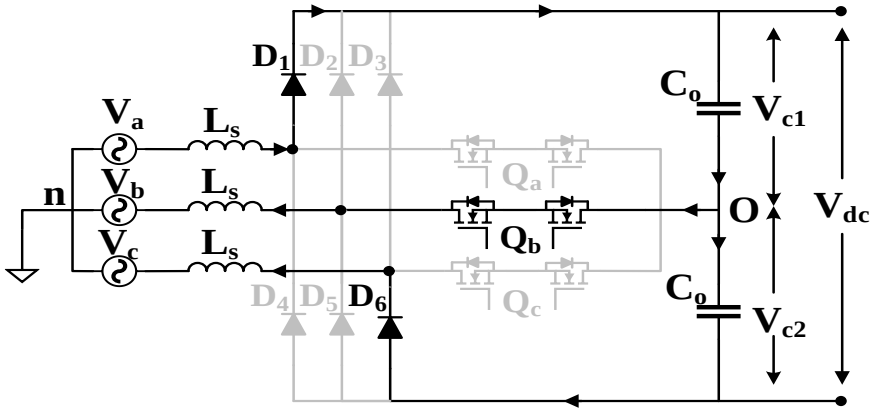


Fig.2.4. Vienna rectifier operation at switching state 010

Mode IV: Switches Q_b, Q_c are ON and Q_a is OFF

In this mode of operation, two bi-directional switches Q_b, Q_c are ON and Q_a is OFF due to which the capacitor mid-point current is equal to phase a current but in opposite direction and the different voltage levels are,

$$V_{ao} = V_{dc}/2,\ V_{bo} = 0,\ V_{co} = 0$$

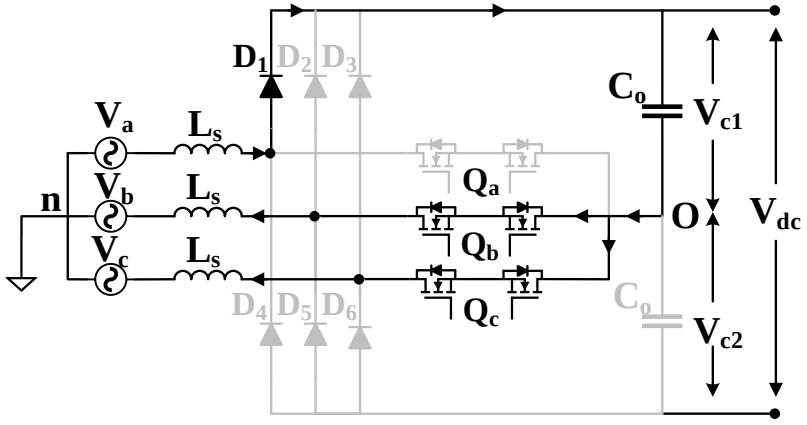


Fig.2.5. Vienna rectifier operation at switching state 011

Mode V: Switches Q_b, Q_c are OFF and Q_a is ON

In this mode of operation, two bi-directional switches Q_b, Q_c are OFF and Q_a is ON due to which the capacitor mid-point current is equal to phase a current and the different voltage levels are,

$$V_{ao} = 0,\ V_{bo} = -V_{dc}/2,\ V_{co} = -V_{dc}/2$$

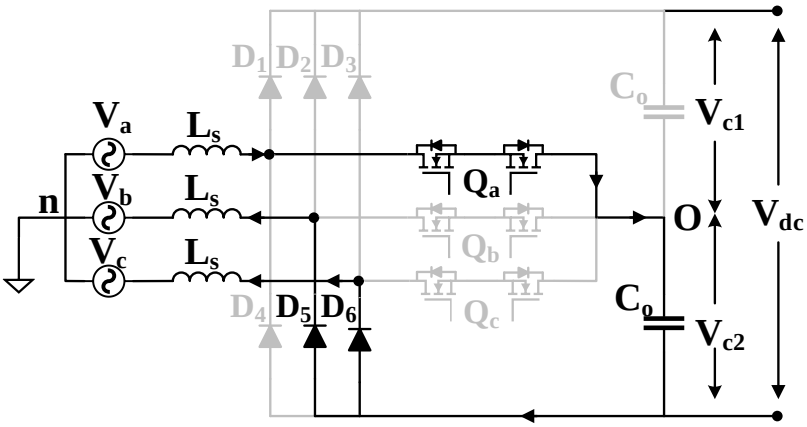


Fig.2.6. Vienna rectifier operation at switching state 100

Mode VI: Switches Q_a, Q_c are ON and Q_b is OFF

In this mode of operation, two bi-directional switches Q_a, Q_c are ON and Q_b is OFF due to which the capacitor mid-point current is equal to phase b current but in opposite direction and the different voltage levels are,

$$V_{ao} = 0,\ V_{bo} = -V_{dc}/2,\ V_{co} = 0$$

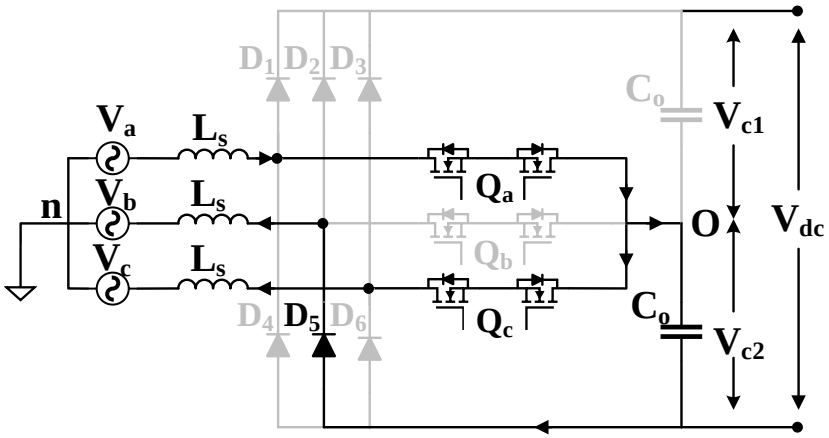


Fig.2.7. Vienna rectifier operation at switching state 101

Mode VII: Switches Q_a, Q_b are ON and Q_c is OFF

In this mode of operation, two bi-directional switches Q_a, Q_b are ON and Q_c is OFF due to which the capacitor mid-point current is equal to phase c current but in opposite direction and the different voltage levels are,

$$V_{ao} = 0,\ V_{bo} = 0,\ V_{co} = -V_{dc}/2$$

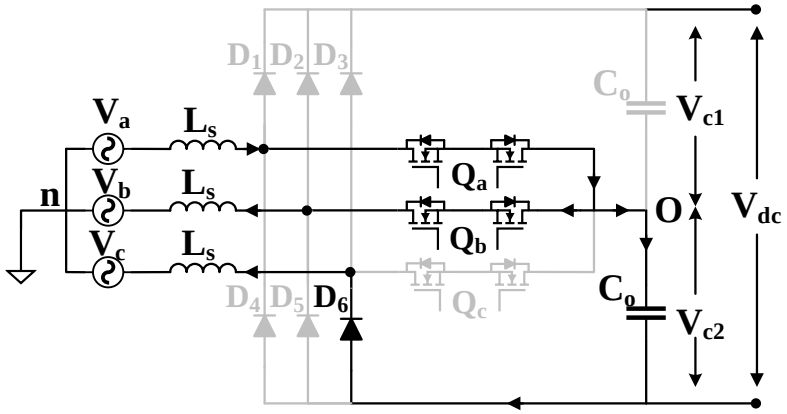


Fig.2.8. Vienna rectifier operation at switching state 110

Mode VIII: Switches Q_a, Q_b and Q_c are ON

In this mode of operation, two bi-directional switches Q_a, Q_b and Q_c are ON due to which the capacitor mid-point current is zero and the different voltage levels are,

$$V_{ao} = 0,\ V_{bo} = 0,\ V_{co} = 0$$

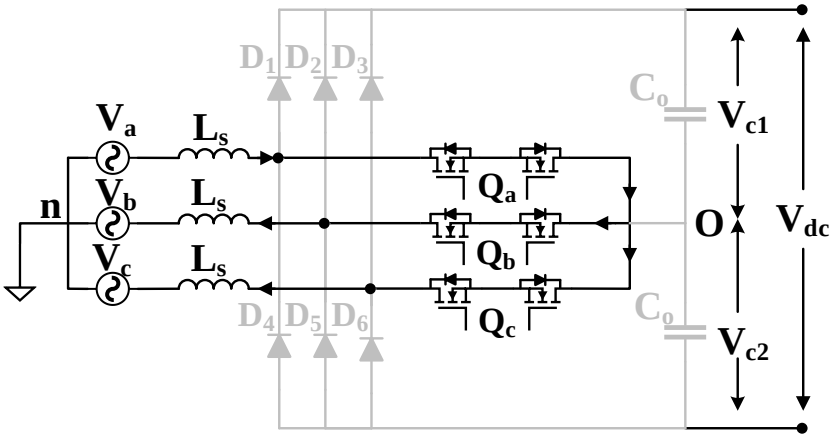


Fig.2.9. Vienna rectifier operation at switching state 111

2.3 DESIGN OF VIENNA RECTIFIER

The system parameters for the Vienna Rectifier can be calculated using [43]. The input filter inductance can be calculated using (2.5),

$$L_s = \frac{\left(V_{dc}/2\right)}{4 * f_{sw} * \Delta i_{pp_{\max}}} \tag{2.5}$$

Where, V_{dc} is the output DC bus voltage of Vienna Rectifier, f_{sw} is the operating switching frequency of Vienna Rectifier and Δi_{ppmax} is the maximum ripple in the current through filter inductor. The filter inductance value is inversely proportional to the switching frequency. For the system analysis, f_{sw} =200 kHz is opted for off-board EV charging application due to which the size of the inductor gets reduced and the THD can be minimized using control loops.

The output capacitance value is calculated using (2.6),

$$C_o = \left(\frac{1}{3}\right)\frac{P_{ac}}{4 * f_s * \left(V_{dc}^2 - \left(V_{dc} - \Delta V_{dc}\right)^2\right)} \tag{2.6}$$

Where P_{ac} is the power ratings of the system, f_s is grid frequency, ΔV_{dc} is the bus voltage ripple and V_{dc} is the DC bus voltage. The design specifications considered in this work are tabulated in Table 2.4.

Table 2.4. Design specifications for Vienna rectifier

Parameters	Value
L-L rms grid voltage (V_{abc}), grid frequency (f_s)	400 V, 50 Hz
Output DC bus voltage (V_{dc})	700V
Power rating (P_{ac})	50 kW
Output current (I_o)	71.4285 A
Switching frequency (f_{sw})	200 kHz
Bus capacitor (C_o), ESR (r_c)	4300 μF, 3.8 mΩ
Input filter inductance (L_s), source resistance (r_s)	41 μH, 0.1 Ω
Input current THD	< 2%

2.4 SMALL SIGNAL MODELLING OF VIENNA RECTIFIER

The small signal modelling of Vienna rectifier can be analyzed using [44] and by applying KVL,

$$V_x = L_s \frac{di_x}{dx} + \frac{V_{dc}}{2}\left[sign\left(i_x\right) * \left(1 - d_k\right)\right] + V_{On} \tag{2.7}$$

Where, $x = \{a, b, c\}$; $k = \{1, 2, 3\}$ and,

$$sign\left(i_x\right) = \begin{Bmatrix} +1 & if\ i_x > 0 \\ -1 & if\ i_x < 0 \end{Bmatrix} \tag{2.8}$$

Where, V_x and i_x are the grid voltages and current respectively.

For balanced system,

$$V_a + V_b + V_c = 0 \tag{2.9}$$

$$i_a + i_b + i_c = 0 \tag{2.10}$$

$$V_a = L_s \frac{di_a}{dt} + \frac{V_{dc}}{3}\left[2\,sign(i_a)(1-d_1) - sign(i_b)(1-d_2) - sign(i_c)(1-d_3)\right] \tag{2.11}$$

$$V_b = L_s \frac{di_b}{dt} + \frac{V_{dc}}{3}\left[-sign(i_a)(1-d_1) + 2sign(i_b)(1-d_2) - sign(i_c)(1-d_3)\right] \tag{2.12}$$

$$V_c = L_s \frac{di_c}{dt} + \frac{V_{dc}}{3}\left[-sign(i_a)(1-d_1) - sign(i_b)(1-d_2) + 2sign(i_c)(1-d_3)\right] \tag{2.13}$$

From above equations, it can be depicted that the voltage is current direction dependent, so to make it independent from it, the following control variable is determined,

$$d_k = 1 - d_k^{'}\left[sign(i_x) - \frac{\Delta V_c}{V_{dc}}\right] \tag{2.14}$$

Where, ΔV_c is the mismatch between the bus capacitors voltage.

$$V_x = L_s \frac{di_x}{dt} + \frac{V_{dc}}{6} M d_k^{'} \tag{2.15}$$

Where,

$$M = \begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix}$$

$$C_o \frac{dV_{dc}}{dt} = \sum_{k=1}^{3}(1-d_k)\,sign(i_x)\,i_x - I_o \tag{2.16}$$

$$C_o \frac{d\Delta V_c}{dt} = \sum_{k=1}^{3} d_k^{'}\left[sign(i_x) - \frac{\Delta V_c}{V_{dc}}\right] i_x \tag{2.17}$$

The above equations is also time dependent so using *abc* to *dq* transform to get following control equations,

$$\frac{di_d}{dt} = \frac{1}{L_s}\left(V_d + L_s\omega_s i_q - \frac{V_{dc}}{2}d_d^{'}\right) \tag{2.18}$$

$$\frac{di_q}{dt} = \frac{1}{L_s}\left(V_q - L_s\omega_s i_q - \frac{V_{dc}}{2}d_q^{'}\right) \tag{2.19}$$

$$\frac{dV_{dc}}{dt} = \frac{1}{C_o}\left[\frac{3}{2}\left(d_d^{'}\, i_d + d_q^{'} i_q\right) - \alpha\frac{\Delta V_c}{V_{dc}}d_o^{'}\, i_d - I_o\right] \tag{2.20}$$

$$\frac{d\Delta V_c}{dt} = \frac{1}{C_o}\left[-\frac{3}{2}\frac{\Delta V_c}{V_{dc}}\left(d_d^{'}\, i_d + d_q^{'} i_q\right) - \alpha d_o^{'}\, i_d\right] \tag{2.21}$$

Where, $\alpha = \frac{2}{\pi} = 0.64$

The static duty cycle in dq0 reference frame is written as,

$$D_d^{'} = \frac{2V_d}{V_{dc}^*};\quad D_q^{'} = \frac{2L_s\omega_s I_d}{V_{dc}^*}; D_o^{'} = 0 \tag{2.22}$$

The nominal points are calculated as,

$$\begin{bmatrix} V_d \\ V_q \\ V_o \end{bmatrix} = \begin{pmatrix} \sqrt{2}V_{abc} \\ 0 \\ 0 \end{pmatrix} \begin{bmatrix} I_d \\ I_q \\ I_o \end{bmatrix} = \begin{pmatrix} \sqrt{2}I_{abc}^* \\ 0 \\ 0 \end{pmatrix} \tag{2.23}$$

$$V_{dc} = V_{dc}^* \tag{2.24}$$

Where V_{abc}= rms grid voltage, I_{abc}*= reference grid current, V_{dc}*= reference bus voltage.

The small signal modelling leads to,

$$\dot{\tilde{X}}(t) = A\tilde{X}(t) + B\tilde{d}(t) + E\tilde{V}(t) \tag{2.25}$$

Where $\tilde{X}$ = state variable vector; $\tilde{d}$ = control input vector; $\tilde{V}$ = input disturbance vector and *A, B, E* are their respective matrices.

$$\tilde{X} = \begin{bmatrix} \tilde{i}_d \\ \tilde{i}_q \\ \tilde{v}_{dc} \\ \Delta\tilde{v}_c \end{bmatrix}; \tilde{d} = \begin{bmatrix} \tilde{d}_d^{'} \\ \tilde{d}_q^{'} \\ \tilde{d}_o^{'} \end{bmatrix}; \tilde{v} = \begin{bmatrix} \tilde{v}_d \\ \tilde{v}_q \end{bmatrix} \tag{2.26}$$

The matrices *A, B, E* can be evaluated as,

$$A = \left(\frac{\partial f}{\partial X}\right)_{X=X_o}, \; B = \left(\frac{\partial f}{\partial d}\right)_{X=X_o}, \; E = \left(\frac{\partial f}{\partial v}\right)_{X=X_o} \tag{2.27}$$

$$A = \begin{bmatrix} 0 & \omega_s & -\dfrac{\sqrt{2}V_{abc}}{L_s V_{dc}^*} & 0 \\ -\omega_s & 0 & \dfrac{\omega_s\sqrt{2}I_{abc}^*}{V_{dc}^*} & 0 \\ \dfrac{3\sqrt{2}V_{abc}}{C_o V_{dc}^*} & -\dfrac{3\sqrt{2}L_s\omega_s I_{abc}^*}{C_o V_s^*} & -\dfrac{1}{C_o R_o} & 0 \\ 0 & 0 & 0 & -\dfrac{6V_{abc}I_{abc}^*}{C_o V_{dc}^{*2}} - \dfrac{1}{C_o R_o} \end{bmatrix} \tag{2.28}$$

$$B = \begin{bmatrix} -\dfrac{V_{dc}^*}{2L_s} & 0 & 0 \\ 0 & -\dfrac{V_{dc}^*}{2L_s} & 0 \\ \dfrac{3\sqrt{2}I_{abc}^*}{2C_o} & 0 & \dfrac{\alpha\sqrt{2}I_{abc}^*}{C_o} \end{bmatrix}; \; E = \begin{bmatrix} \dfrac{1}{L_s} & 0 \\ 0 & \dfrac{1}{L_s} \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{2.29}$$

Using laplace transform,

$$\tilde{X}(s) = (sI - A)^{-1} B\tilde{d}(s) + (sI - A)^{-1} E\tilde{v}(s) \tag{2.30}$$

Using (2.30) various transfer function can be analyzed accordingly.

For example,

$$\frac{\Delta V_c(s)}{d_0^{'}(s)} = \frac{2\sqrt{2}R_o}{\pi} * \left[\frac{1}{2+(R_oC_o)s}\right] \tag{2.31}$$

The bode plot of above transfer function is shown in Fig.2.10.

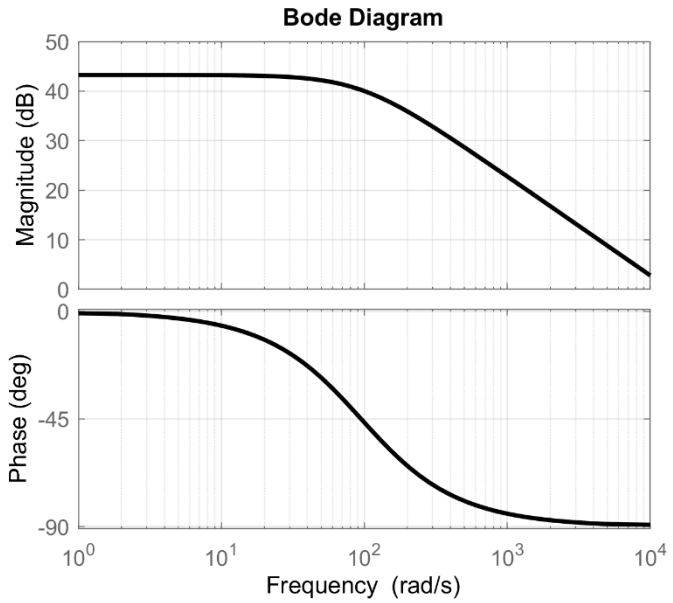


Fig.2.10. Bode plot of $\Delta V_c(s)/d_0'(s)$

2.5 CHAPTER SUMMARY

In this chapter complete analysis of Vienna rectifier is discussed with all modes of operation for a complete sector 1. It also includes designing of Vienna rectifier to achieve required DC bus voltage and near to unity power factor. The small signal modelling is also studied to design the controlling loops for mitigating both the grid side and load side variations.

CHAPTER 3

CONTROL OF VIENNA RECTIFIER

3.1 INTRODUCTION

The need for higher power ratings and efficient AC-DC conversion led to opting of Vienna Rectifier for off-board electric vehicle (EV) charging applications. In this chapter, a complete analysis of three phase Vienna Rectifier considering the effect of parasitic in the system for off-board EV charging application is discussed. To improve the dynamic response a modified dual loop control using d-axis and q-axis current controller including the effect of system parasitic in control loops is proposed. The proposed algorithm is compared with different control algorithms viz., dual loop control using hysteresis current controller and dual loop control using d-axis and q-axis current controller with SVPWM. A comparative performance analysis is discussed in terms of dynamic response during system disturbances like load variation, reference DC bus voltage variation and grid side variations. A 50 kW Vienna Rectifier operating at a switching frequency of 200 kHz is used for performance evaluation of all three control algorithms and is validated using MATLAB-Simulink. Fig.3.1. depicts the circuit diagram of Vienna rectifier considering system parasitic.

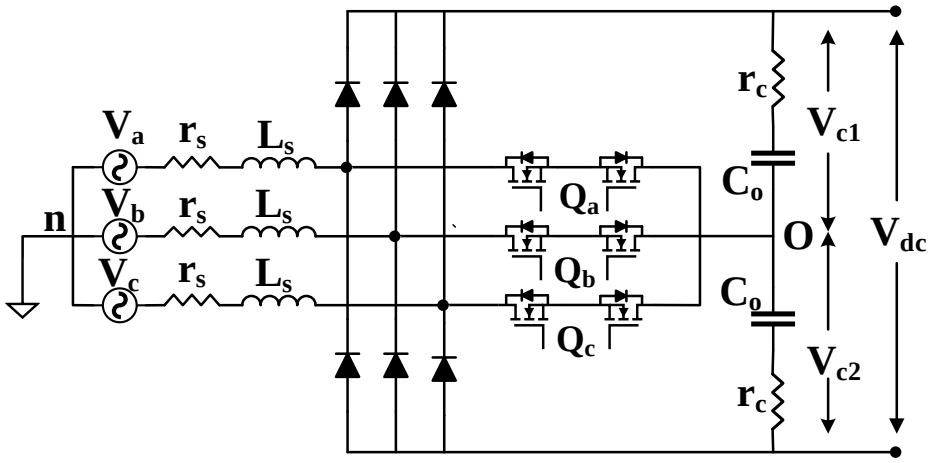


Fig.3.1. Three phase Vienna Rectifier circuit diagram including parasitic

3.2 DUAL LOOP CONTROL USING HYSTERESIS CURRENT CONTROLLER

In this control strategy, there involves different controlling loops, an outer control loop for DC bus voltage uses a PI controller to provide reference signals. The generated reference signals are provided to the inner current control loops and hysteresis controllers which are used instead of PI controller. Three-phase PLL is designed to provide clocking frequency theta/ωt for abc/dq0 and dq0/abc transformations. The three-phase voltages are transformed into alpha-beta and thereafter to d-q transform to extract three phase reference voltages, V_a*,V_b* and V_c*. Finally the output of hysteresis controller for the inner control loops is compared with V_a*, V_b* and V_c* respectively. Switching pulses for controlled bidirectional switches are obtained and Fig.3.2 depicts control block diagram for this control strategy [35].

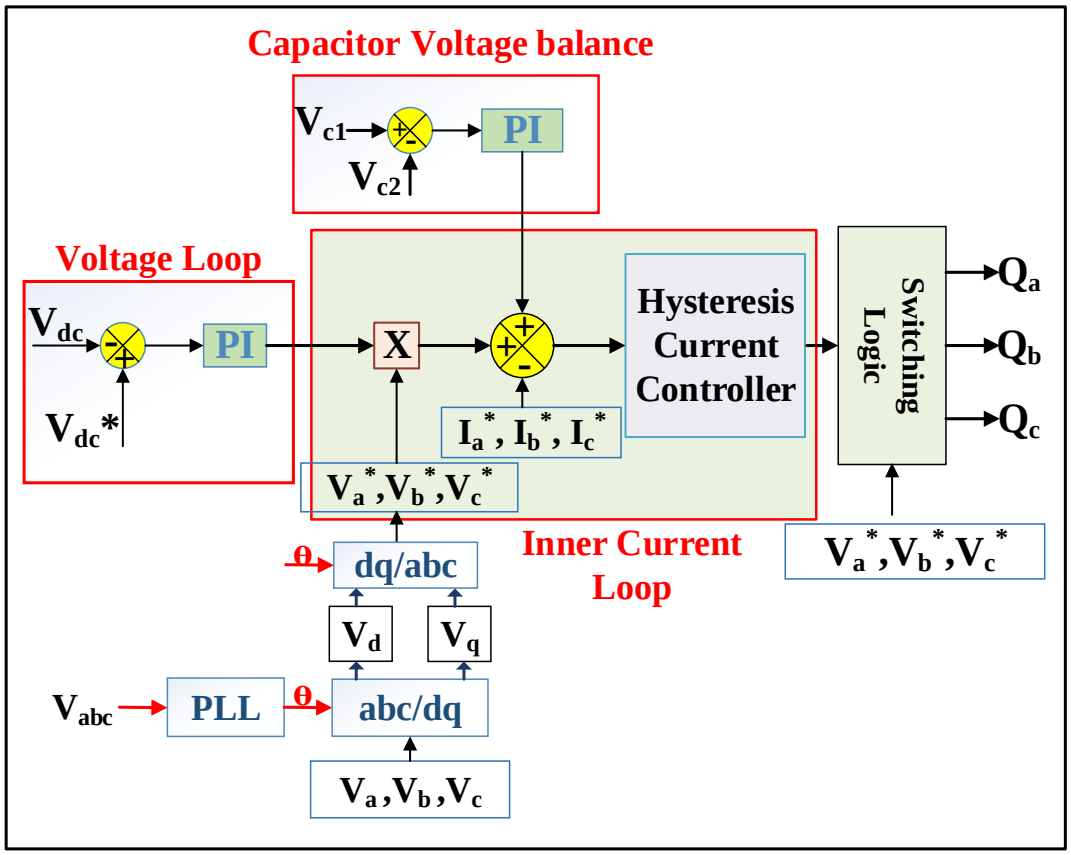


Fig.3.2. Block diagram of dual loop control using hysteresis current control scheme

3.3 DUAL LOOP CONTROL USING D-AXIS AND Q-AXIS CURRENT CONTROLLER WITH SVPWM

The dual loop control strategy using hysteresis controller is able to provide power factor which tends to unity and able to achieve the THD under EV standards but it is not able to mitigate the 1% variations in grid frequency. So, a dual loop control using d-axis and q-axis current control strategy is adopted for further analysis of Vienna Rectifier [36]. In this strategy one loop will be the inner control loop which includes the d-axis current, I_d and q-axis current, I_q control. Second loop is the outer voltage control loop where the output voltage is compared with the DC bus reference voltage and the voltage error is provided to a PI controller and output of this PI controller is reference d-axis current, I_{dref} and compared with the I_d and the error is provided to a PI Controller and generated output is summed with the expression, $V_d+2\pi f_s L_s I_q$ using (3.4) to generate reference d-axis voltage V_{dref}. Similarly for q-axis controller, I_q is compared with 0 to reduce or eliminate reactive component. The error is provided to the PI controller and the generated output is differenced from an expression, $2\pi f_s L_s I_d$ using (3.1) to generate reference q-axis voltage V_{qref}. Next step is to convert V_{dref}, V_{qref} and 0 to three phase reference voltage, V_{abc}* using dq0 to abc transformations. Clarke and Park transformation are utilized to transform the three phase grid voltages and current to alpha-beta and then to d-q respectively. Three-phase PLL is used to generate theta/ωt for the clarke and park transformations. I_d and I_q are transformed to three phase reference current, I_{abc}* using dq0 to abc transform. In Vienna Rectifier, the main concern is the capacitor voltage balancing. So, here a proportional controller is incorporated to ensure that the voltage across the capacitors remains balanced under various dynamic changes in the system, to ensure the desired output bus voltage. Fig.3.3 depicts block diagram for this control strategy [36]. The final step includes generation of pulses for the three bi-directional switches using SVPWM. The input Control parameters to the SVPWM pulse generator are V_{abc}*, I_{abc}* and controller output for the capacitor voltage balancing.

The control loops are designed using following calculated equations,

$$V_{q_{ref}} = \begin{Bmatrix} -\left(K_{p_{i_q}}(0 - I_q) + K_{i_{i_q}} \int (0 - I_q) dt\right) \\ -2\pi f_s L_s I_d \end{Bmatrix} \tag{3.1}$$

$$I_{d_{ref}} = K_{p_{v_{dc}}}(V_{dc}^{*} - V_{dc}) + K_{i_{v_{dc}}} \int (V_{dc}^{*} - V_{dc})dt \tag{3.2}$$

$$\Delta V_c = K_{p_{v_c}}(V_{c_1} - V_{c_2}) + K_{i_{v_c}} \int (V_{c_1} - V_{c_2})dt \tag{3.3}$$

$$V_{d_{ref}} = \begin{Bmatrix} K_{p_{i_d}}\left(I_{d_{ref}} - I_d\right) + \\ K_{i_{i_d}} \int \left(I_{d_{ref}} - I_d\right) dt \\ +V_d + 2\pi f_s L_s I_q \end{Bmatrix} \tag{3.4}$$

$$V_{dc} = V_{c_1} + V_{c_2} \tag{3.5}$$

Where V_{qref}, V_{dref} and I_{qref}, I_{dref} are the reference voltages and currents for q-axis and d-axis respectively. V_{dc}* is the reference output voltage. V_{c1} and V_{c2} are voltages across output bus capacitors. In (3.1)-(3.4) the different parameters K_p and K_i are PI controller gains for different loops.

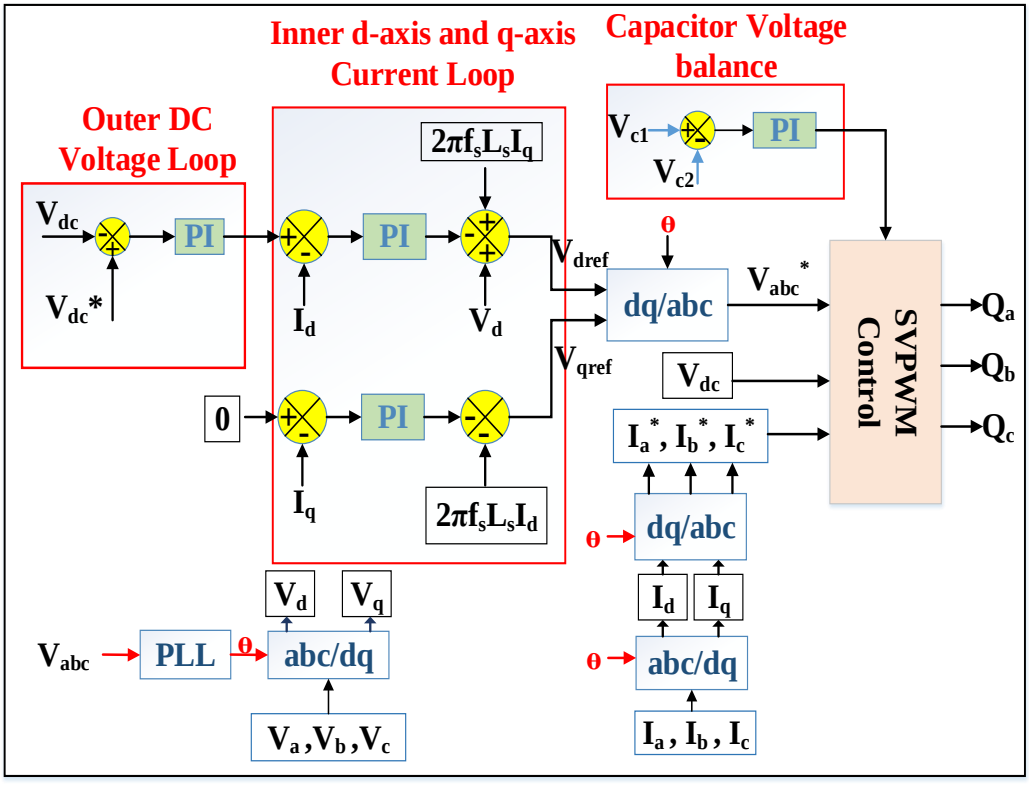


Fig.3.3. Block diagram of dual loop control using d-axis and q-axis current control strategy with SVPWM

3.3.1 SVPWM Control

Vienna Rectifier control using SVPWM can be summarized as in [45], first step is the sector identification on the basis of current direction through each phases. For multilevel Vienna Rectifier it is different from conventional converters as in this case, the current polarity is taken into account. Second step is to normalize the angle calculated from sector identification for simplification. Third step is the calculation of sub-vectors and calculations of dwell time. Next step is to calculate dwell times in case of over modulation and a saturation is used to limit the output such that the magnitude of sum of dwell times should not exceed the switching time. Next step is the capacitor voltage balancing where the redundant switching states are determined which generate the opposite but similar voltage vectors, this definitely have to be considered for the pulse generation. The pulses are generated by calculating on and off timings w.r.t. the bidirectional switches and comparing it with reference values and finally PWM signals are generated. Fig.3.4 shows Vienna Rectifier space vector diagram of all existing voltage vectors.

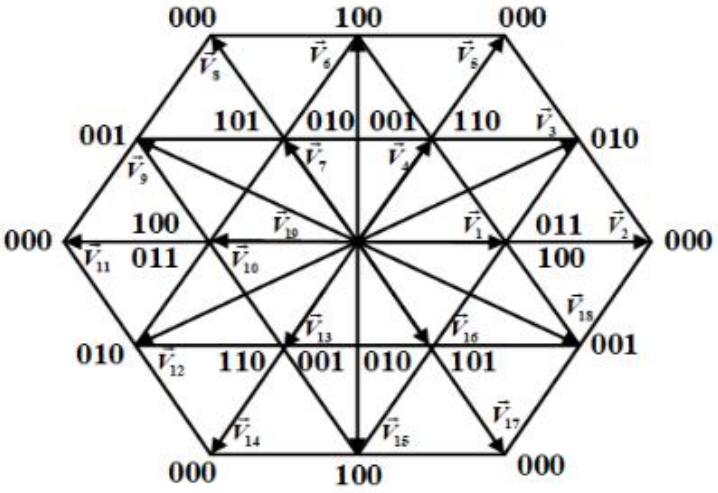


Fig.3.4. Diagram of space vectors for Vienna Rectifier

Sector identification:

As previously discussed the sectors are defined based on the current direction. This can now be utilized through angle as in Table 3.1.

Table 3.1. Sector classification based on angle

Sector	***θ***	**Sector**	***θ***
Sector 1	$-\pi/6 \le \theta < \pi/6$	Sector 4	$5\pi/6 \le \theta < -5\pi/6$
Sector 2	$\pi/6 \le \theta < \pi/2$	Sector 5	$-5\pi/6 \le \theta < -\pi/2$
Sector 3	$\pi/2 \le \theta < 5\pi/6$	Sector 6	$-\pi/2 \le \theta < -\pi/6$

Angle Normalization:

Angle normalization is used to simplify the calculations of vector. This is utilized by rotating the vectors from nearest sector to sector 1 and can be calculated using (3.6),

$$\varphi = \theta - \left[\text{Sec}tor\left(I\right) - 1\right] * \frac{\pi}{3} \tag{3.6}$$

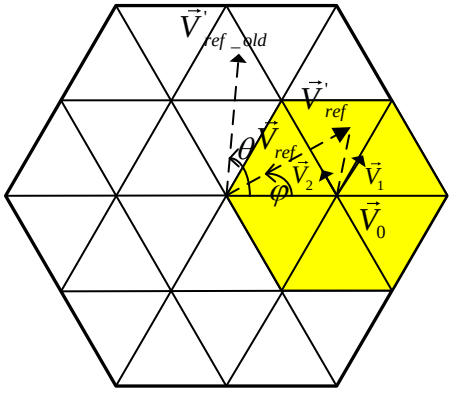


Fig.3.5. Angle normalization

Sub-vector calculations:

Sub-vector are recognized based on whether it is in top half of hexagon or bottom half of hexagon. After utilizing this, dwell times are calculated according to the position of vectors in various triangle.

The location of vector in triangle is decided using (3.7)-(3.8). (3.7) is for triangle 1 and (3.8) for triangle 3, otherwise triangle 2.

$$|V_{ref}| \le \frac{\cos\left(\frac{\pi}{6}\right)}{\sin\left(\frac{\pi}{3}+|\varphi|\right)} \tag{3.7}$$

$$|V_{ref}| \ge \frac{\cos\left(\frac{\pi}{6}\right)}{\sin\left(\frac{\pi}{3}-|\varphi|\right)} \tag{3.8}$$

The dwell times for triangle 1 is calculated as,

$$V_1 = 1-|V_{ref}|\frac{\sin\left(\frac{\pi}{3}+|\varphi|\right)}{\cos\left(\frac{\pi}{6}\right)}\ ;\ V_2 = |V_{ref}|\frac{\sin(|\varphi|)}{\cos\left(\frac{\pi}{6}\right)} \tag{3.9}$$

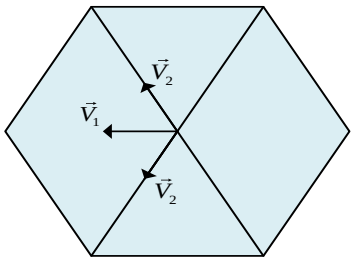


Fig.3.6. Dwell times for triangle 1

The dwell times for triangle 2 is calculated as,

$$V_1 = |V_{ref}|\frac{\sin\left(\frac{\pi}{3}+|\varphi|\right)}{\cos\left(\frac{\pi}{6}\right)}-1\ ;\ V_2 = 1-|V_{ref}|\frac{\sin\left(60^{\circ}-|\varphi|\right)}{\cos\left(\frac{\pi}{6}\right)} \tag{3.10}$$

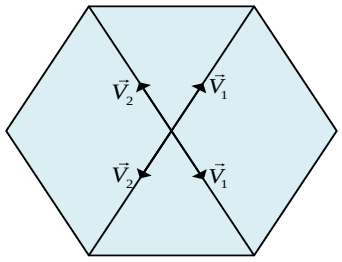


Fig.3.7. Dwell times for triangle 2

The dwell times for triangle 2 is calculated as,

$$V_1 = |V_{ref}|\frac{\sin\left(\frac{\pi}{3}-|\varphi|\right)}{\cos\left(\frac{\pi}{6}\right)}-1 \; ; \; V_2 = |V_{ref}|\frac{\sin(|\varphi|)}{\cos\left(\frac{\pi}{6}\right)} \tag{3.11}$$

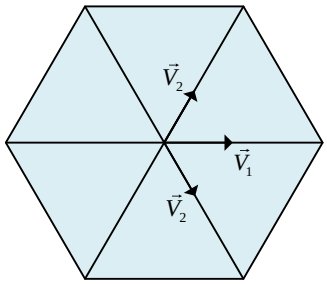


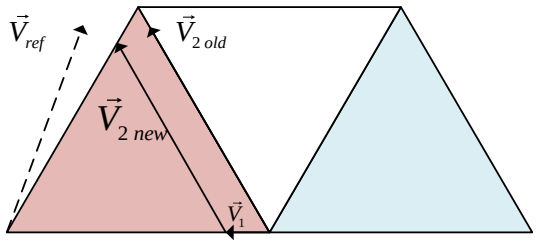
Fig.3.8. Dwell times for triangle 3

The redundant vector is calculated as,

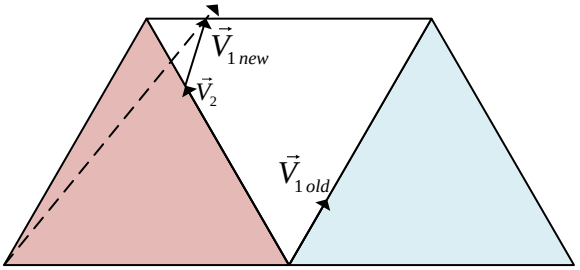
$$V_0 = 1 - V_2 - V_1 \tag{3.12}$$

Shortening of sub-vectors:

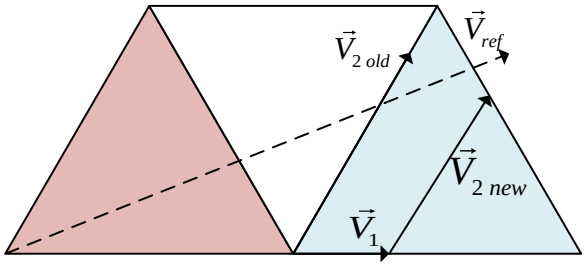
The sum of dwell times should not exceed 1 to avoid over-modulation that's why shortening is required when the sum is exceeding by 1 as in Fig.3.9.



(a)



(b)



(c)

Fig.3.9. Shortening of sub-vectors for (a) Triangle 1 (b) Triangle 2 (c) Triangle 3

Generation of switching pulses:

The pulses are generated by calculating on and off timings w.r.t. the bidirectional switches and comparing it with reference values and finally PWM signals are generated.

3.4 PROPOSED MODIFIED DUAL LOOP CONTROL USING D-AXIS AND Q-AXIS CURRENT CONTROLLER WITH SVPWM

In this proposed control strategy, a modification in the controlling loops is introduced where the effect of system parasitic i.e. source resistance 'r_s' in the inner current control loops and ESR of bus capacitance 'r_c' in the capacitor voltage balance loop. The small signal analysis of the proposed modified control can be analyzed and modified using [44] and control loops are designed using (3.13)-(3.18). Fig.3.10 depicts the block diagram of the proposed modified control strategy.

$$V_{c_1} = V_{c_2} = \frac{V_{dc}}{2} \tag{3.13}$$

$$\Delta V_c = V_{c_1} - V_{c_2} \tag{3.14}$$

$$\frac{di_d}{dt} = \frac{1}{L_s}\left(V_d + 2\pi f_s L_s I_q + r_s I_q - \frac{V_{dc}}{2} d'_d\right) \tag{3.15}$$

$$\frac{di_q}{dt} = \frac{1}{L_s}\left(V_q - 2\pi f_s L_s I_d - r_s I_d - \frac{V_{dc}}{2} d'_q\right) \tag{3.16}$$

$$\frac{dV_{dc}}{dt} = \frac{1}{C_o}\begin{Bmatrix}\frac{3}{2}\left(d'_d I_d + d'_q I_q\right) - \frac{V_{dc}}{2r_c} - \frac{2}{\pi}\frac{\Delta V_c}{V_{dc}} d'_o I_d \\ -I_o d'_q\end{Bmatrix} \tag{3.17}$$

$$\frac{d\Delta V_c}{dt} = \frac{1}{C_o}\begin{Bmatrix} -\frac{3}{2}\frac{\Delta V_c}{V_{dc}}\left(d'_d I_d + d'_q I_q\right) - \frac{V_{dc}}{2r_c} \\ -\frac{2}{\pi} d'_o I_d \end{Bmatrix} \quad (3.18)$$

Where ΔV_c is the mismatch between capacitor voltages and $d_d{}'$, $d_q{}'$ and $d_0{}'$ are the duty ratio for dq0 reference frame.

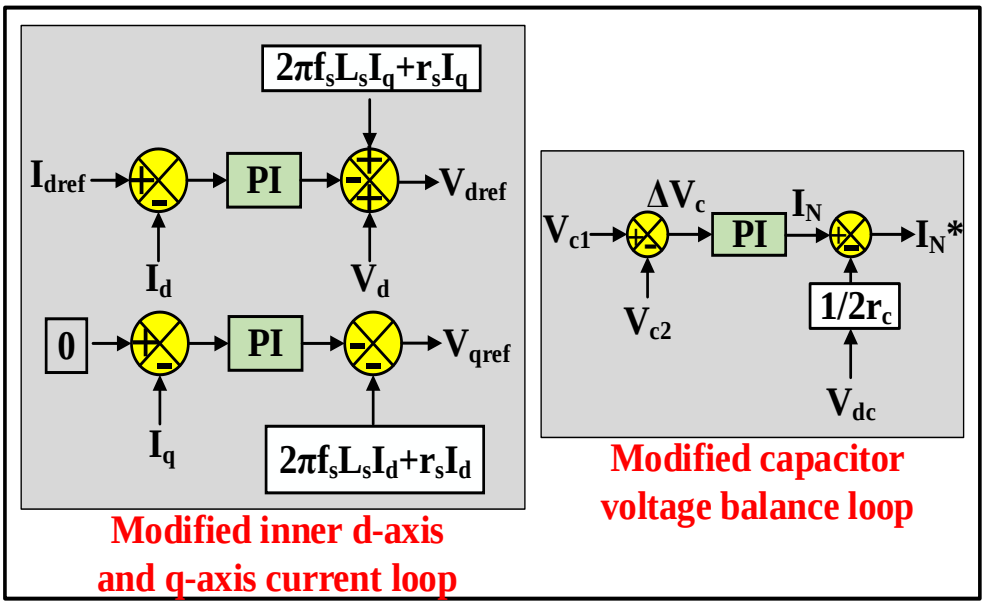


Fig.3.10. Block diagram of proposed modified dual loop control using d-axis and q-axis current control strategy

Conduction Power Losses in the System

The conduction loss in source resistance is,

$$P_{r_s} = r_s * I^2_{S_{rms}} \quad (3.19)$$

The conduction loss in ESR of bus capacitance is,

$$P_c = P_{c1} = P_{c2} = r_c * I^2_{C_{rms}} \quad (3.20)$$

The conduction loss in bidirectional switch is,

$$P_M = V_{SW_{avg}} * I_{SW_{avg}} = R_{DS(on)} * I^2_{SW_{rms}} \quad (3.21)$$

The conduction loss in power diodes is,

$$P_D = V_{D_{avg}} * I_{D_{avg}} + r_D * I^2_{D_{rms}} \quad (3.22)$$

Where, I_{SWrms} and V_{SWavg} is the rms current and average voltage across bidirectional switch, I_{Crms} is the rms current through bus capacitor, I_{Srms} is the input rms current. V_{Davg} and I_{Drms} are the average diode voltage and rms current respectively. $R_{DS(on)}$ and r_D are the on resistance of switch and diode respectively. The voltage and current across bidirectional switch can be calculated using Fig.3.13 (f). The total conduction losses can be calculated using (3.19)-(3.22). Conduction losses for a complete sector 1 is evaluated in Table 3.2.

Table 3.2. Conduction losses for all switching states of sector 1

Switching States	Conduction Loss
000	$3P_{r_s} + 3P_D + 2P_c$
100	$3P_{r_s} + 2P_D + P_M + P_c$
001	$3P_{r_s} + 2P_D + P_M + 2P_c$
101	$3P_{r_s} + P_D + 2P_M + P_c$
010	$3P_{r_s} + 2P_D + P_M + 2P_c$
110	$3P_{r_s} + P_D + 2P_M + P_c$
011	$3P_{r_s} + P_D + 2P_M + P_c$
111	$3P_{r_s} + 3P_M$

3.5 RESULTS AND PERFORMANCE EVALUATION

A 50 kW Vienna Rectifier considering the system parasitic has been analyzed for off-board EV charging application at the switching frequency of 200 kHz. The study has been performed for the three control algorithms, using control 1 i.e. dual loop control using hysteresis current controller, control 2 i.e. Dual loop I_d and I_q control using SVPWM and control 3 (proposed model) i.e. modified dual loop I_d and I_q control. Performance of all controlling strategies under various dynamic changes in the system has been compared in Table 3.3. The complete analysis has been verified through MATLAB-Simulink. The DC bus voltage response during load variations, grid voltage variations, reference DC bus voltage variation and FFT analysis during grid frequency variation for control 1, control 2 and control 3 is depicted in Fig.3.11, Fig.3.12 and Fig.3.13 respectively.

Load Variation

The analysis was performed during the load current variations and Fig.3.11 (a), 3.12 (a), 3.13 (a) clearly depicts the load current variation at t= 0.3s from 100% to 50% as in for control 1, 2 and 3 respectively, which indirectly is the effect of load perturbation in the system. At t=0.3s, the load current was suddenly reduced to 50% and the effect of this load variation was analyzed on the DC bus voltage. It was observed from Fig.3.11 (b) that for hysteresis control algorithm, at t= 0.3s the DC bus voltage was able to reach steady state of 700V but the dynamic response was slightly sluggish with some oscillations in transient state and having settling time, t_s= 60ms. When the system was analyzed for dual loop SVPWM control algorithm, it can be observed from Fig.3.12 (b) that at t=0.3s the dynamic response was improved and oscillations during transient state were reduced significantly and settling time was, t_s= 50ms. It can be depicted from Fig.3.13 (b) that the proposed modified dual control loops for SVPWM algorithm which also includes the effects of system parasitic in the controlling loops shows an improved dynamic response with settling time, t_s=20ms. Fig.3.11 (c), 3.12 (c), 3.13 (c) shows that capacitor voltages are balanced after load variations. For all the control algorithms it was observed that THD was less than 5% and achieving near to unity pf.

Reference DC Voltage Variation

Further analysis includes the flexibility in the reference DC bus Voltage variations, V_{dcref} = 600V. From Fig. 3.11 (d), 3.12 (d), 3.13 (d), it can be observed that all the controlling algorithms were able to adapt the provided reference DC bus voltage of 600 V at t= 0.3s. Fig.3.11 (d), 3.12 (d), 3.13 (d), clearly depicts that dynamic response varies among different control strategies and it resembles the dynamic response achieved after load variation analysis and settling time was t_s=40ms, 50ms, 30ms for control 1, 2 and 3 respectively.

Grid Voltage Variation

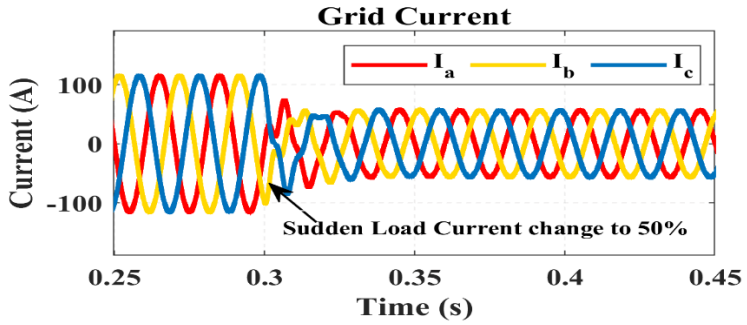
The results clearly depict that all the control algorithms are able to maintain a constant DC bus voltage when the grid voltage varies by 5% i.e., V_{abc} = 420 V at t=0.15s. From Fig.3.11 (e) it can be observed that the grid voltage varies from 400 V to 420 V and Fig.3.11

(f) and Fig.3.12 (e) clearly depicts that the system maintains constant bus voltage for control 1 and control 2 respectively. Control 3 behaves similarly as control 2.

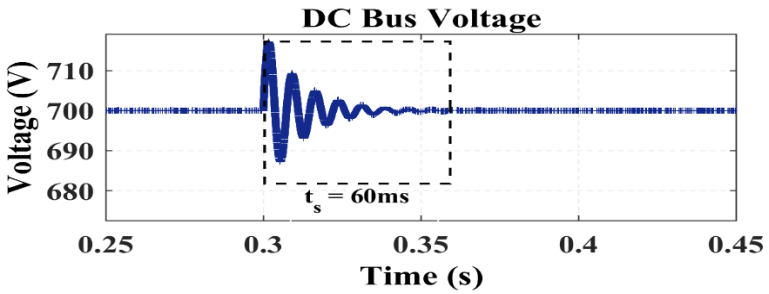
Grid Frequency Variation

From Fig.3.11 (g) it can be observed that control 1 algorithm is unable to mitigate the grid frequency variations of 1% i.e., f_s = 50.5 Hz. After the FFT analysis it was observed that THD for f_s = 50.5 Hz was 8.29%, which is not acceptable according to EV standards in India and affects the performance of the system. In the comparative analysis, from Fig.3.12 (f) an observation can be made that control 2 algorithm is able to mitigate the variations in the grid frequency and FFT analysis at 50.5 Hz depicts the THD as 1.96%. From Fig.3.13 (e) an observation can be made that proposed control 3 algorithm is also able to mitigate the variations in grid frequency and provided with the THD of less than 5% and FFT analysis at 50.5 Hz depicts the THD as 1.83%.

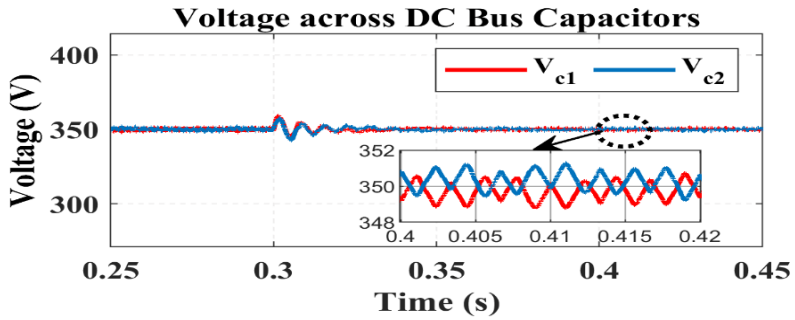
In off-board EV charging application, the required operation of AC/DC converter is to ensure a desired DC bus voltage at disturbances either from grid side or the load side. So, this analysis can also be useful for other applications.



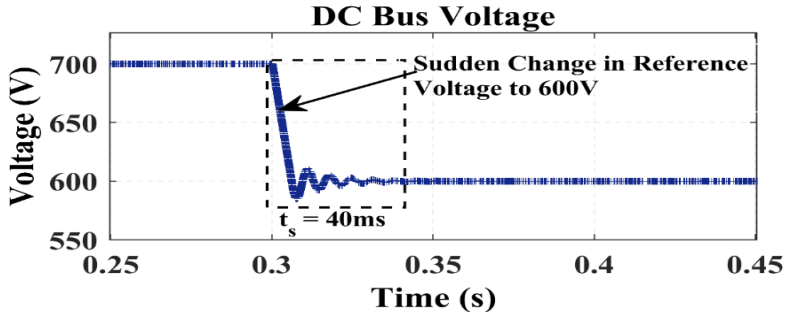
(a) Grid current during load variations



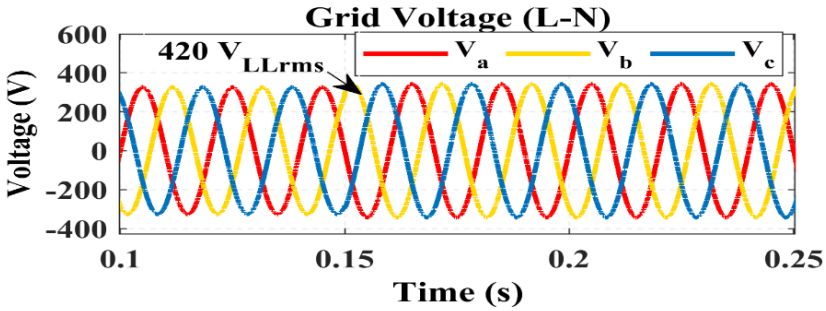
(b) DC bus voltage adaption to load variations



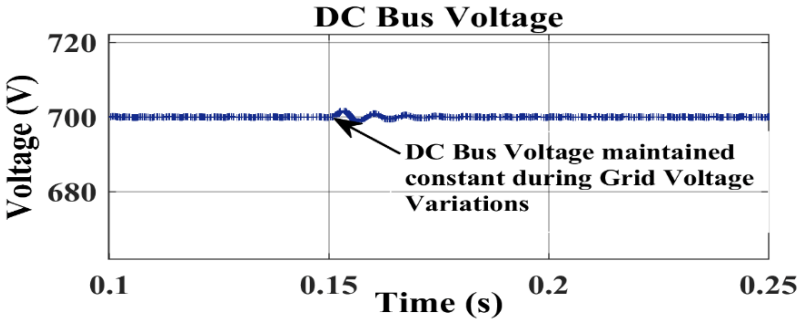
(c) DC bus capacitor voltage



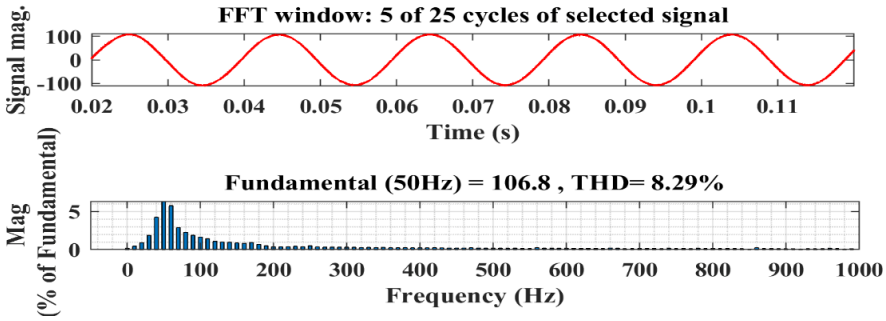
(d) System adaption to reference DC voltage variation



(e) Grid voltage variation

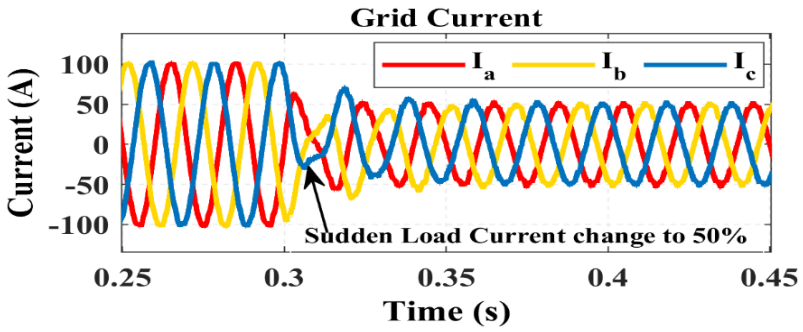


(f) System adaption to grid voltage variation

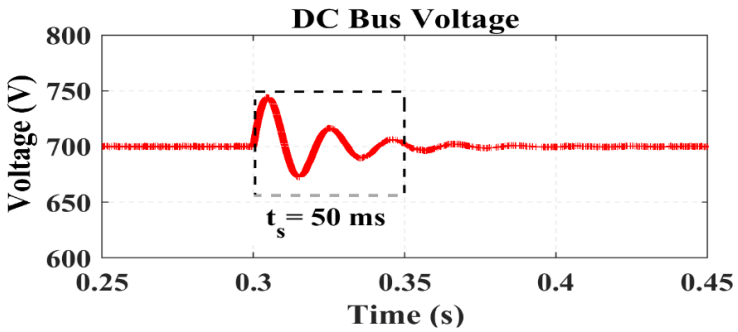


(g) System non-adaption to grid frequency variation at 50.5 Hz

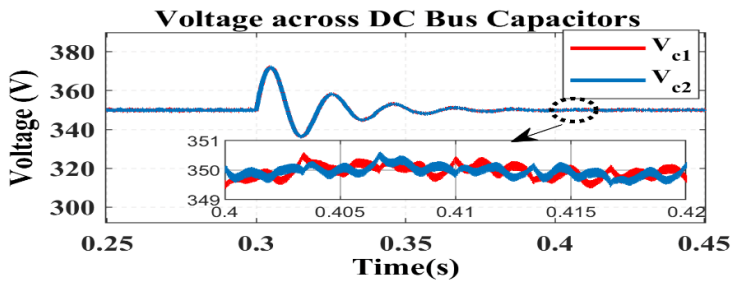
Fig.3.11. Simulation results for dual loop control using hysteresis current control strategy



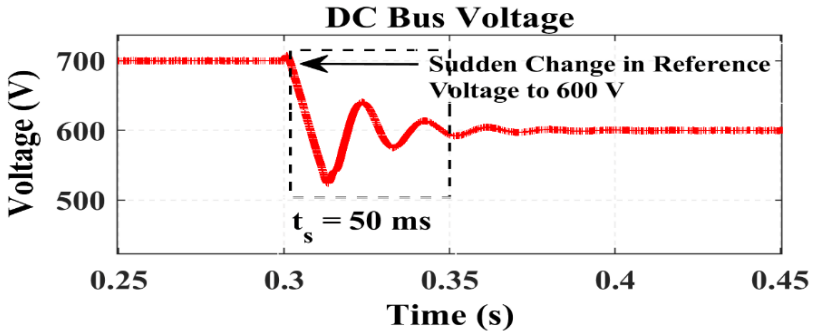
(a) Grid current during load variations



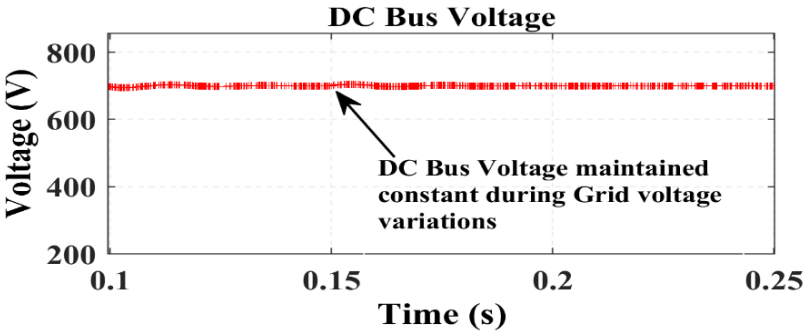
(b) DC bus voltage adaption to load variations



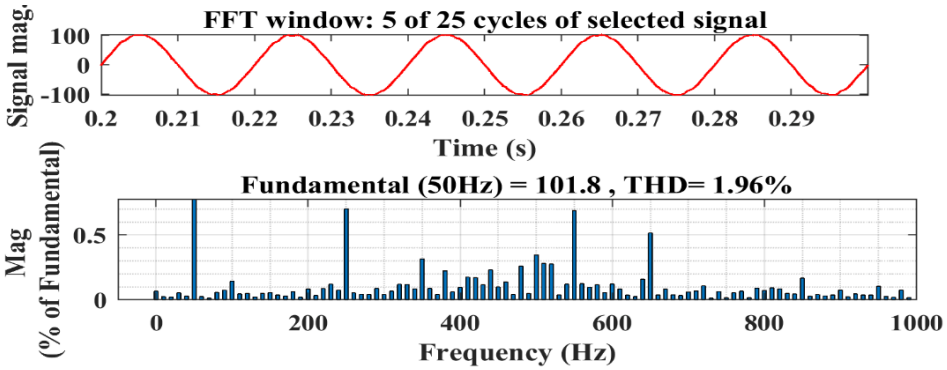
(c) DC bus capacitor voltage



(d) System adaption to reference DC voltage variation

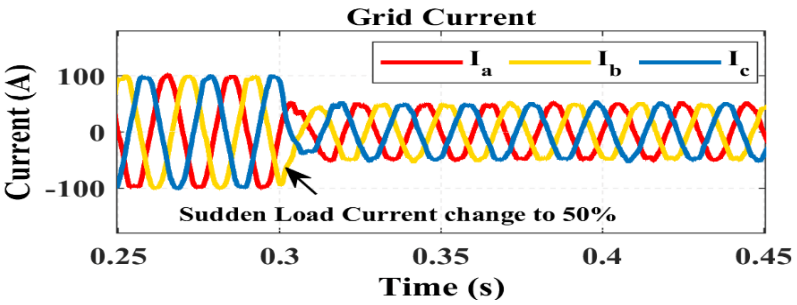


(e) System adaption to grid voltage variation as in Fig.3.11 (e)

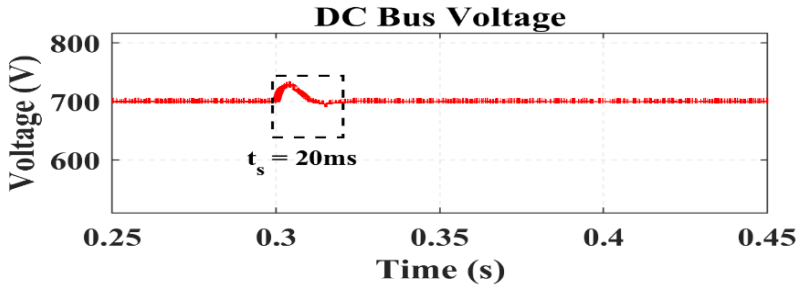


(f) System adaption to grid frequency variation at 50.5 Hz

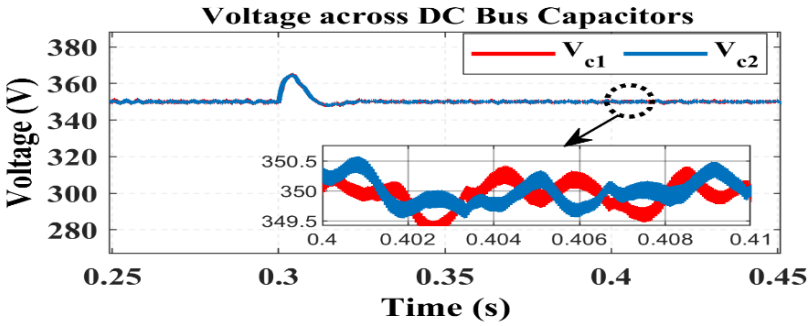
Fig.3.12. Simulation results for dual loop control using d-axis and q-axis current control strategy with SVPWM



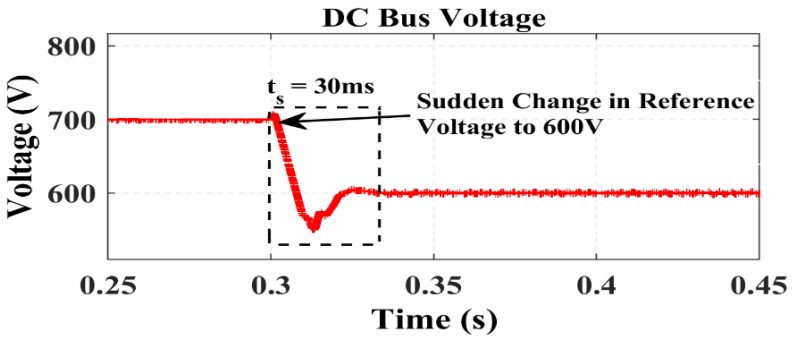
(a) Grid current during load variations



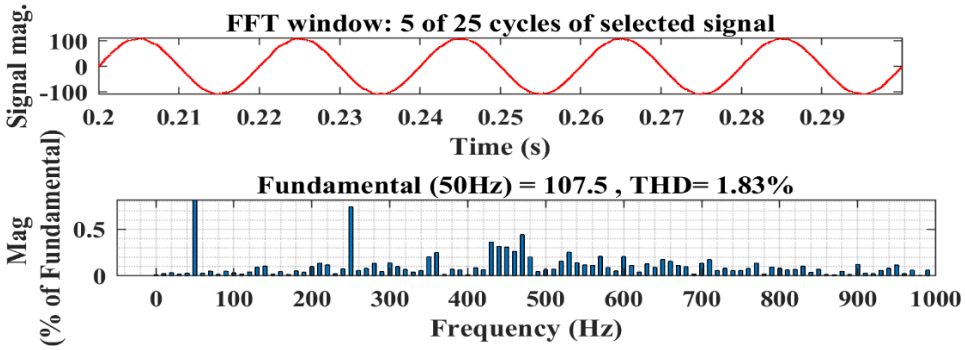
(b) DC bus voltage adaption to load variations



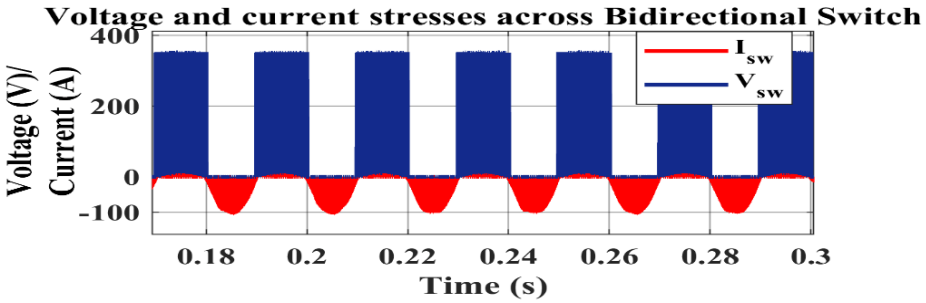
(c) DC bus capacitor voltage



(d) System adaption to reference DC voltage variation



(e) System adaption to grid frequency variation at 50.5 Hz



(f) Voltage and current stresses across bidirectional switch

Fig.3.13. Simulation results of proposed modified dual loop control using d-axis and q-axis current control strategy with SVPWM

3.6 CHAPTER SUMMARY

In this paper, a 50 kW Vienna Rectifier considering system parasitic is analyzed using three control algorithms: dual loop using hysteresis current control, dual loop using q-axis and d-axis current control using SVPWM and modified dual loop using q-axis and d-axis current control using SVPWM. The control algorithms are implemented in MATLAB-Simulink. The dual loop hysteresis current control algorithm was adaptive to the grid voltage variations but not adaptive to the grid frequency variations and is able to mitigate the sudden load variations and reference DC Bus voltage variation but with a sluggish dynamic response with oscillations in transient state. The dual loop control using d-axis and q-axis current control algorithm using SVPWM was adaptive to both grid voltage and grid frequency variations including sudden load variations and reference DC Bus voltage variation but with an improved dynamic response with minimal oscillations in transient state. The proposed

modified dual loop control using d-axis and q-axis current control algorithm using SVPWM was able to improve the dynamic response by reducing the settling time and eliminating the oscillations in transient state. So, this is the preferred control algorithm compared to other two. To support the proposed modified control, small signal analysis was performed. All the control algorithms were able to achieve near to unity p.f. with varied performance. In this paper, the adopted power ratings are high due to its application, so conduction losses are also analyzed for a complete sector. The system designed is efficiently mitigating the load variations and grid side variations which suits its application in emerging EV charging topologies.

Table 3.3. Comparison of Different Control Algorithms due to Dynamic Variations in the System

Control Strategy	**Dynamic Variations in the system**			
	Grid frequency adaptive	***Grid Voltage adaptive***	***Load variation (t_s)***	***Reference DC voltage variation (t_s)***
Control 1	No	Yes	60ms	40ms
Control 2	Yes	Yes	50ms	50ms
Control 3 (proposed model)	Yes	Yes	20ms	30ms

CHAPTER 4

DESIGN AND ANALYSIS OF FULL BRIDGE LLC RESONANT CONVERTER

4.1 INTRODUCTION

Nowadays isolated DC-DC converters are widely used for various power electronics applications. One of this application includes EV charging, which requires higher power density and efficient power converters. This features are fulfilled by a LLC resonant converter. Unlike other DC-DC converters which are controlled or regulated by using pulse width modulation (PWM) which provides Duty ratio *D*, LLC is controlled by modulating the frequency according to the calculated frequency range which makes the designing as well as the control of LLC converter tedious. The key working of the LLC converter includes the variation in the output voltage by varying the switching frequency. This basically vary the input impedance of resonant tank circuit due to which the output voltage changes. There are basically two topologies of LLC, series resonant converter and parallel resonant converter.

During light load, high frequency is required as it is tedious to regulate the output due to high impedance of the load. Parallel resonant converter is not opted for high power densities due to its considerable amount of circulating current in the circuit. These demerits can be overcome by using combinations of these topologies which results in LLC or LCC resonant converters. LLC resonant converters are widely used due to their adaptability for wide operation of load regulation and line regulation. This can be achieve by modulating the frequency for a very small range. It also features zero voltage switching among the primary side controlled switches, which leads to minimized losses which leads to improved efficiency. This can be only be achieved when operating the converter in the inductive region in the gain vs normalized frequency curve. It also features ZCS among the secondary side diodes of diode bridge rectifier.

Full bridge LLC is opted before half bridge LLC resonant converter when higher power rating is required for certain application. In this work FBLLC is adopted and analyzed

for off-board EV charging. FBLLC converter consists of full-bridge inverter which is utilized for generating bipolar voltage square wave having duty $D=0.5$ due to which switches Q_1, Q_4 are ON for positive cycle and switches Q_2, Q_3 are ON for negative cycle. This bipolar square voltage acts as a switching waveform for the resonant tank circuit which consists of resonating inductor (L_r), resonating capacitor (C_r) and magnetizing inductance (L_m) of high frequency transformer. This tank circuit drives power to the secondary side. Secondary side includes diode bridge rectifier which converts AC to DC and filter out using output capacitor C_o and power is transferred to the load R_L.

At resonant frequency f_o, the resonant tank circuit provides the minimum impedance and the maximum current or power is delivered to the load. The impedance of the resonant tank circuit depends on the switching frequency of the applied switching voltage waveform V_{sw}. In LLC resonant tank due to the influence of the transformer magnetizing inductance, L_m. The peak resonance does not occur at resonant frequency, f_o. The peak resonance occurs at f_{co} and it depends on load and range of f_{co} is, $f_p \leq f_{c_o} \leq f_o$, where,

$$f_p = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}} \tag{4.1}$$

Operation at resonance:

During this mode of operation as in Fig.4.1 the switching frequency is kept equal to resonant frequency, i.e. $f_{sw}=f_o$. The switches Q_1 ,Q_4 are ON for positive cycle of switching voltage, the resonant current is sinusoidal in nature. At t=t_1, when switches Q_1, Q_4 are OFF, the resonant current becomes equal to magnetizing current I_m during region t_1 to t_2. As, $f_{sw}=f_o$, wide range of operation is not possible. This delay time for switching ON the switch Q_2, Q_3 between t_1 to t_2 helps in achieving ZVS for primary side controlled switches and ZCS for secondary side diodes.

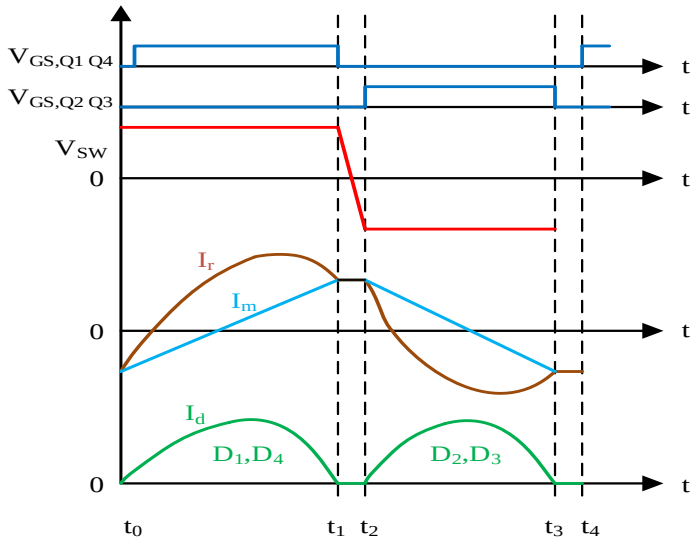


Fig.4.1. Operation at resonance

Operation below resonance:

During this mode of operation as in Fig.4.2 the switching frequency is kept below the resonant frequency, i.e. $f_{sw}<f_o$. In this the resonant current becomes equal to the magnetizing current I_m quite before t=t1, which leads to more circulating current demand and considerable conduction losses across switches. The diode current also becomes discontinuous in this mode of operation and switching frequency should not be reduced below a certain f_o to prevent circuit to lose ZVS.

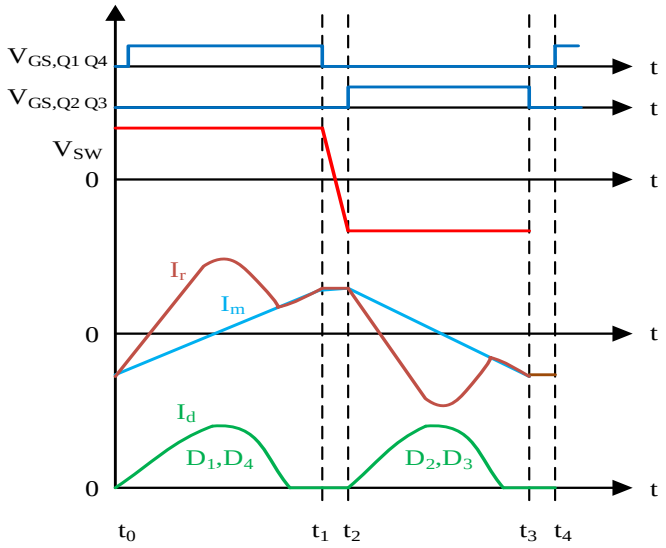


Fig.4.2. Operation below resonance

Operation above resonance:

During this mode of operation as in Fig.4.3 the switching frequency is kept above the resonant frequency, i.e. $f_{sw}>f_o$. In this the resonant current becomes continuous and sinusoidal, which leads to less circulating current demand and very less considerable conduction losses across switches. The diode current is reduced to zero after $t=t_1$ which means secondary side diodes are not soft commutated and leads to increased reverse recovery losses.

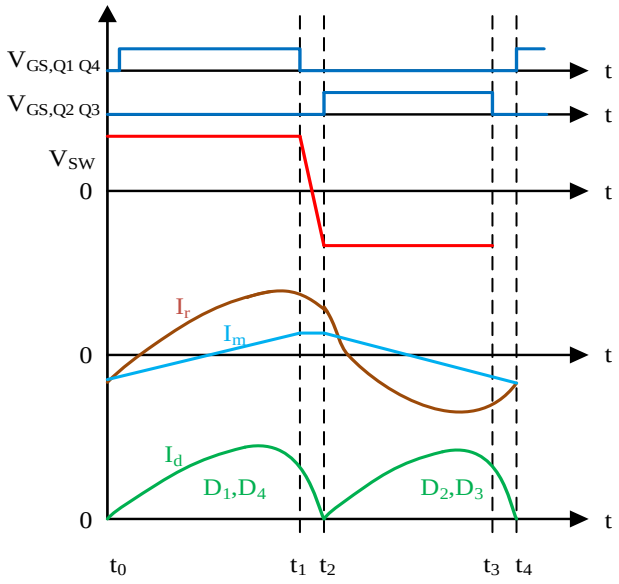
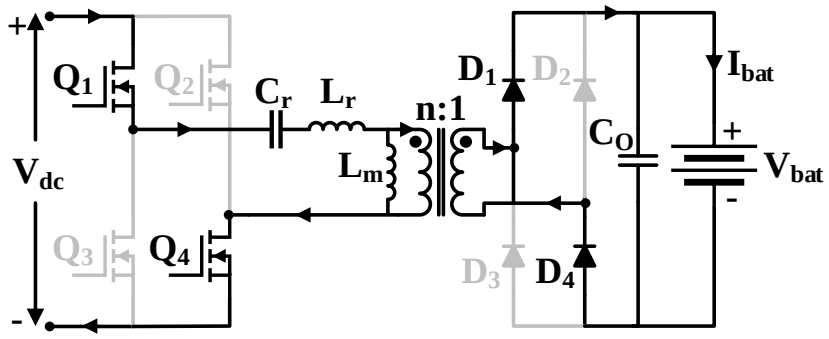


Fig.4.3. Operation above resonance

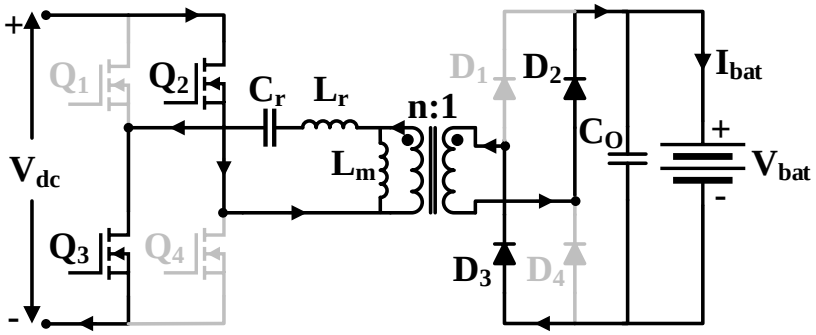
4.2 MODES OF OPERATION

The various modes of operation of the LLC resonant converter involves positive cycle operation, negative cycle operation and freewheeling operation. In positive cycle operation, the gate pulse is provided to the controlled switches Q_1, Q_4 which is responsible for positive half square wave at the input of resonating circuit as in Fig.4.4 (a). In negative cycle operation, the gate pulse is provided to the controlled switches Q_2, Q_3 which is responsible for negative half square wave at the input of resonating circuit as in Fig.4.4 (b). These two modes are responsible to deliver power from primary side to secondary side. This is then utilized to charge the lithium ion battery. Fig.4.4 (c) describes the mode when the resonating

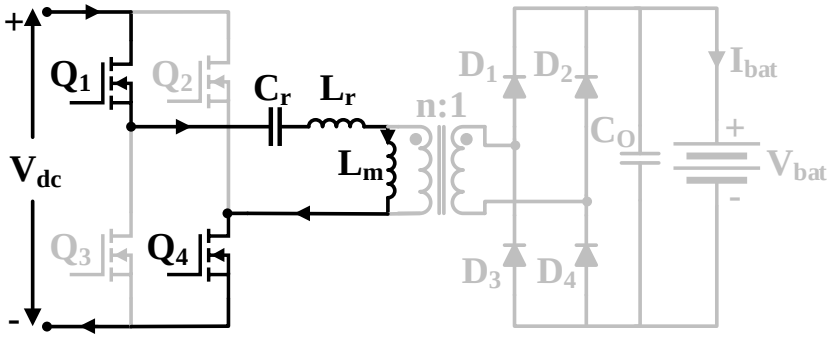
current become equals to magnetizing current and no current flows to the secondary side of the converter and Fig.4.4 (d) shows the freewheeling mode for positive magnetizing current [46].



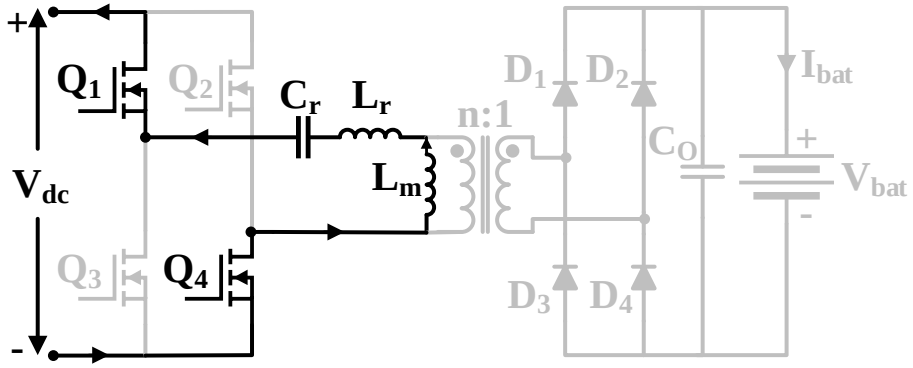
(a)



(b)



(c)



(d)

Fig.4.4. FBLLC modes of operation for (a), (b) Power delivery (c), (d) No power delivery

4.3 DESIGN OF FULL BRIDGE LLC RESONANT CONVERTER

LLC resonant converter can be analyzed using First Harmonic Approximation (FHA) when not including the higher order harmonics using Fig.4.5.

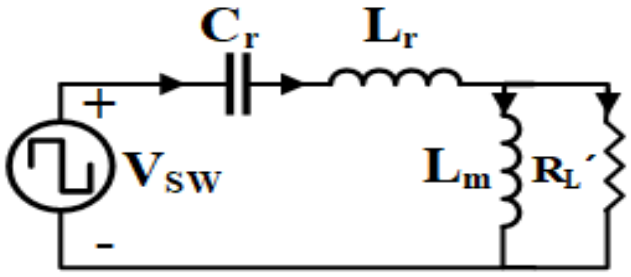


Fig.4.5. LLC equivalent circuit

The designing steps followed for designing LLC converter can be summarized as in Fig.4.6 using [47]. The gain is calculated as,

$$M_g = \frac{V_{oe}}{V_{ge}} = \left| \frac{jX_{L_m} \,||\, R_e}{\left(jX_{L_m} \,||\, R_e\right) + j\left(X_{L_r} - X_{C_r}\right)} \right| \tag{4.2}$$

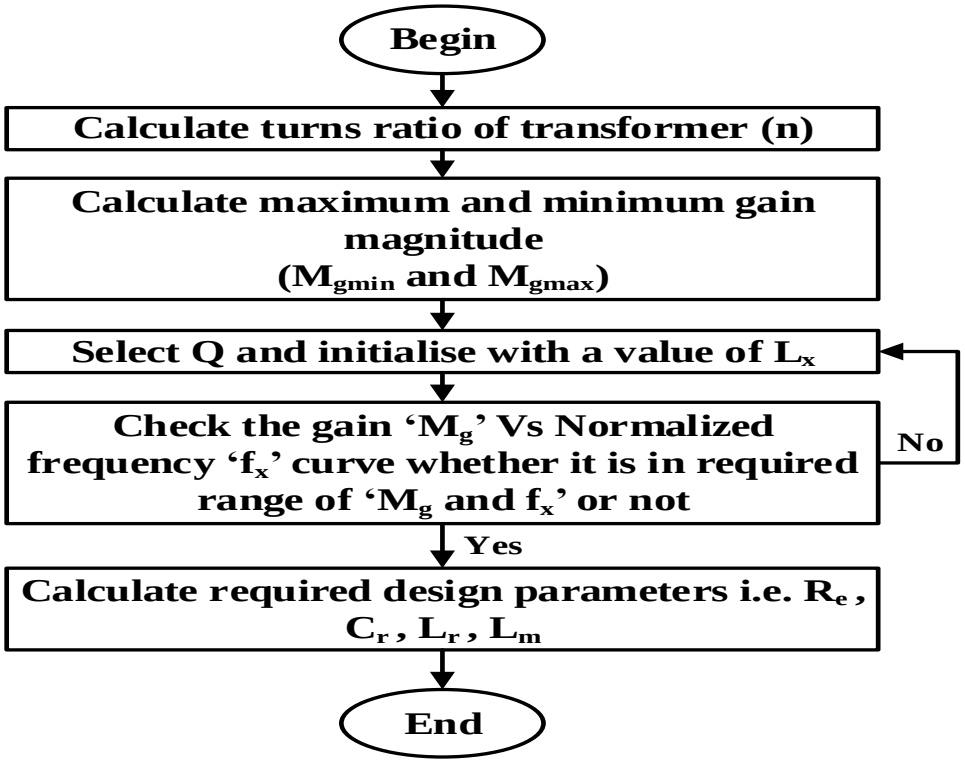


Fig.4.6. Designing Steps of LLC resonant circuit

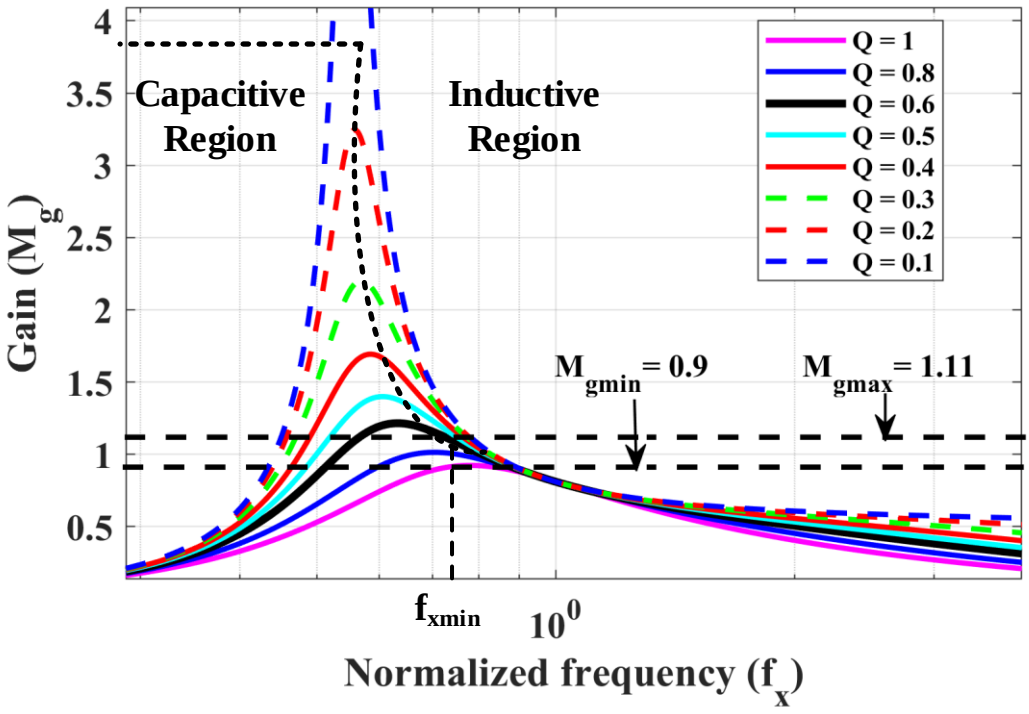


Fig.4.7. Gain magnitude Vs normalized frequency curve

The output voltage depends on the gain magnitude,

$$V_o = M_g \times \frac{1}{n} \times V_{dc} \tag{4.3}$$

The gain magnitude is the function of L_x, f_x and Q. The optimum value of the Q and L_x is achieved using gain curve. So the only controlled variable is the normalized frequency, f_x. The gain magnitude in terms of f_x can be written as,

$$M_g = \left| \frac{L_x * f_x^2}{\left[\left(L_x + 1 \right) * f_x^2 - 1 \right] + j \left[\left(f_x^2 - 1 \right) * f_x * Q * L_x \right]} \right| \tag{4.4}$$

The quality factor is described as,

$$Q = \frac{1}{R_e} \sqrt{\frac{L_r}{C_r}} \tag{4.5}$$

The normalized frequency is described as,

$$f_x = \frac{f_{sw}}{f_o} \tag{4.6}$$

The turns ratio of transformer can be calculated as,

$$n = M_g * \frac{V_{dc}}{V_o} = \left. \frac{V_{dc\_nom}}{V_{o\_nom}} \right|_{M_g = 1} = \frac{7}{3} \tag{4.7}$$

The maximum and minimum gain can be calculated as,

$$M_{g_{\min}} = \frac{n \times \left(V_{o\_\min} + V_D \right)}{V_{dc\_\max}} = 0.9 \tag{4.8}$$

$$M_{g_{\max}} = \frac{n \times \left(V_{o\_\max} + V_D \right)}{V_{dc\_\min}} = 1.11 \tag{4.9}$$

The rms value of primary side load current can be calculated as,

$$I_{oe_{rms}} = \frac{\pi}{2\sqrt{2}} \times \frac{1}{n} \times I_o = 79.34\,A \tag{4.10}$$

The rms value of magnetizing current at minimum f_{sw} can be evaluated as,

$$I_m = \frac{2\sqrt{2}}{\pi} \times \frac{nV_o}{\omega L_m} = 53.5\,A \tag{4.11}$$

The resonant current can be calculated as,

$$I_r = \sqrt{I_m^2 + I_{oe}^2} = 95.7\,A \tag{4.12}$$

The L_x and Q can be selected from gain Vs normalized frequency as in Fig.4.7 and f_{xmin} can be obtained as around 0.74 and minimum f_{sw} as around 150 kHz. In (4.8) and (4.9), V_D =0.7 V is the forward voltage drop across diodes. The capacitive and inductive region can also be identified using this gain curve to select the values of L_x and Q at which primary controlled switches can achieve ZVS as, *Q = 0.6, L_x = 3.3* and design specifications of FBLLC converter is tabulated in Table 4.1.

Equivalent load resistance can be calculated as,

$$R_e = \frac{8}{\pi^2} \times n^2 \times R_L = 7.945\,\Omega \tag{4.13}$$

Resonant circuit parameters can be calculated as,

$$C_r = \frac{1}{2\pi * Q * f_o * R_e} = 167\,nF \tag{4.14}$$

$$L_r = \frac{1}{\left(2\pi * f_o\right)^2 \times C_r} = 3.8\,\mu H \tag{4.15}$$

$$L_m = L_x \times L_r = 12.5\,\mu H \tag{4.16}$$

The dead time to ensure ZVS can be calculated as,

$$\tau_{dead} \geq 16 \times C_{eq} \times f_{sw} \times L_m \approx 150\,ns \tag{4.17}$$

Table 4.1. Design Specifications for LLC Resonant Converter

Parameters	**Value**
Bus voltage range (V_{dc_min}-V_{dc_max}), Nominal bus voltage (V_{dc_nom})	675-725 V, 700 V
Output voltage range (V_{o_min}-V_{o_max}), Nominal output voltage (V_{o_nom})	280-320 V, 300 V
Transformer turns ratio (n)	7:3
Quality factor (Q)	0.6
Resonating inductor (L_r)	3.8 µH
Resonating capacitor (C_r)	167 nF
Magnetizing inductance (L_m)	12.5 µH
Resonating frequency (f_o)	200 kHz
Inductance ratio (L_x)	3.3

4.4 MAGNETIC DESIGN OF LLC CONVERTER

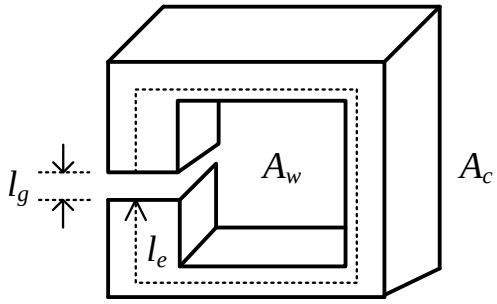


Fig.4.8. Basic core specification

Magnetic design is one of the essential design requirement while designing a LLC resonant converter for any application. Major challenge in magnetic design is the selection

of the required core as well as the wire used for transformer winding. The magnetic design can be evaluated using various design methods but in this section, two methods are explained: Transformer design using area product (A_P) and using core geometry (K_g). In this work, magnetic design is evaluated using core geometry.

Transformer design using area product (A_P):

The voltage across the winding is defined as in (4.18)-(4.19),

$$V = L\frac{dI}{dt} \tag{4.18}$$

$$V = n\frac{d\phi}{dt} \tag{4.19}$$

From (4.18)-(4.19),

$$L\frac{dI}{dt} = n\frac{d\phi}{dt} \tag{4.20}$$

Taking integral both sides,

$$L\int_0^{I_{pk}}\left(\frac{di}{dt}\right)dt = nA_c\int_0^{B_{\max}}\left(\frac{di}{dt}\right)dt \tag{4.21}$$

On solving (4.21),

$$LI_{pk} = nA_cB_{\max} \tag{4.22}$$

After rearranging (4.22), cross-section area of core, A_c can be determined as,

$$A_c = \frac{LI_{pk}}{nB_{\max}} \tag{4.23}$$

The current density can be written in terms of wire cross-section area as,

$$J = \frac{I_{rms}}{W_A} \Rightarrow W_{A_i} = \frac{I_{rms_i}}{J} \tag{4.24}$$

Winding area A_w can be calculated using (4.25),

$$A_{w_i} = \frac{n_i W_{A_i}}{k} = \frac{n_i I_{rms_i}}{Jk} \tag{4.25}$$

Where, k = fill factor and it depends on how the winding is packed with what amount of voids, k<1.

For primary and secondary side windings total winding area, A_w can be calculated as,

$$A_w = A_{w_1} + A_{w_2} \tag{4.26}$$

$$A_w = \frac{n_1}{Jk} \sum_i \frac{n_i}{n_1} I_{rms_i} \tag{4.27}$$

$$n = \frac{LI_{pk}}{A_c B_{\max}} \Rightarrow A_c = \frac{LI_{pk}}{nB_{\max}} \tag{4.28}$$

Product area will be the product of core cross-section area and winding area as,

$$A_p = A_c * A_w = \frac{L_1 I_{pk_1} \sum_i \frac{n_i}{n_1} I_{rms_i}}{B_{\max} Jk} \tag{4.29}$$

Transformer design using core geometry (K_g):

Table 4.2. Design specifications for transformer design

Input Voltage (V_{in}, V_{inmin}, V_{inmax})	700V, 675V, 725V
Output Voltage (V_o)	300 V
Output current (I_o)	166.67 A
Frequency (f)	200 kHz
Diode voltage drop (V_d)	0.7 V
Flux density (B_{ac})	0.1 T
Regulation (α)	0.5 %
Efficiency (η)	98 %
Window utilization (K_u)	0.69
Maximum duty ratio (D_{max})	0.5

Using core geometry [48],

Skin depth can be calculated as,

$$\varepsilon = \frac{6.62}{\sqrt{f}} = 0.0148\,cm \tag{4.30}$$

Wire diameter is determined as,

$$D = 2\varepsilon = 0.0296\,cm \tag{4.31}$$

The area of bare wire can be calculated as,

$$A_w = \frac{\pi D^2}{4} = 0.000688\,cm^2 \tag{4.32}$$

By calculations, the wire selected is AWG 29 having specifications as in Table 4.3.

Table 4.3. Wire specifications

AWG	29
Area cm^2 (10^{-3})	0.6470
Diameter (inches)	0.0113
Resistance (μΩ/cm)	2664

Transformer output power can be calculated as,

$$P_o = I_o\left(V_o + V_d\right) = 50126.7W \tag{4.33}$$

Input power can be calculated as,

$$P_{in} = \frac{P_o * 1.1}{\eta} = 56264.66327W \tag{4.34}$$

Electrical coefficient is calculated as,

$$K_e = 0.145 * f^2 * \Delta B^2 (10^{-4}) = 5800 \tag{4.35}$$

Core geometry can be calculated as,

$$K_g = \frac{P_{in} * D_{\max}}{\alpha K_e} = 9.7 \tag{4.36}$$

On the basis of calculated core geometry Kg, DU 75 lamination core is used for designing purpose and all the specifications are tabulated in Table 4.4.

Table 4.4. Core specifications

Core type	DU-75
Copper weight (W_{tcu})	1467 gm
Core weight (W_{tfe})	985.2 gm
Mean length turn (MLT)	14.2 cm
Magnetic path length (MPL)	34.3 cm
Iron area (A_c)	3.448 cm^2
Window area (W_a)	29.032 cm^2
Area product (A_p)	100.091 cm^4
Core geometry (K_g)	9.7136 cm^5
Surface area (A_t)	537.1 cm^2

Number of primary turns can be calculated as,

$$N_P = \frac{V_{in_{\min}} * D_{\max} * 10^4}{f * A_c * \Delta B} = 49\, turns \tag{4.37}$$

Current density can be calculated as,

$$J = \frac{2P_{in} * \sqrt{D_{\max}} * 10^4}{f * A_c * \Delta B * W_a * K_u} = 2108.27\, A/cm^2 \tag{4.38}$$

Primary side rms current can be calculated as,

$$I_P = \frac{P_{in}}{V_{in_{\min}} \sqrt{D_{\max}}} = 117.9\, A \tag{4.39}$$

Area of primary bare wire can be calculated as,

$$A_{wp(B)} = \frac{I_P}{J} = 0.056\, cm^2 \tag{4.40}$$

Number of secondary turns can be calculated as,

$$N_S = \frac{N_P * (V_o + V_d)}{D_{\max} * V_{in_{\min}}} \left\{ 1 + \frac{\alpha}{100} \right\} = 44 turns \quad (4.41)$$

Secondary side rms current can be calculated as,

$$I_S = \frac{I_o}{\sqrt{2}} = 117.87\, A \quad (4.42)$$

Area of secondary bare wire can be calculated as,

$$A_{ws(B)} = \frac{I_S}{J} = 0.056\, cm^2 \quad (4.43)$$

4.5 CHAPTER SUMMARY

In this chapter complete background of LLC resonant converter is discussed and operation at resonant frequency, below resonant frequency, above resonant frequency is also studied. Various modes of operation for full bridge LLC converter is also discussed. A complete design of full bridge LLC resonant converter is also discussed and it was ensured to operate circuit to achieve ZVS. Magnetic design was also studied to design the high frequency transformer for the designed LLC converter.

CHAPTER 5

CONTROL OF FULL BRIDGE LLC RESONANT CONVERTER

5.1 INTRODUCTION

In this chapter controller of full bridge LLC resonant converter is designed and explained in detail. Voltage control is designed for controlling the gate pulses for the controlled switches Q_1, Q_2, Q_3, and Q_4. In this analysis, input voltage is not the output of Vienna rectifier, it is stated in the next chapter. In this case 700 V DC voltage is utilized for the complete analysis. The designed control is validated for both the load side as well as the input side variations, and the results are analyzed using MATLAB-Simulink.

5.2 VOLTAGE CONTROL OF LLC RESONANT CONVERTER

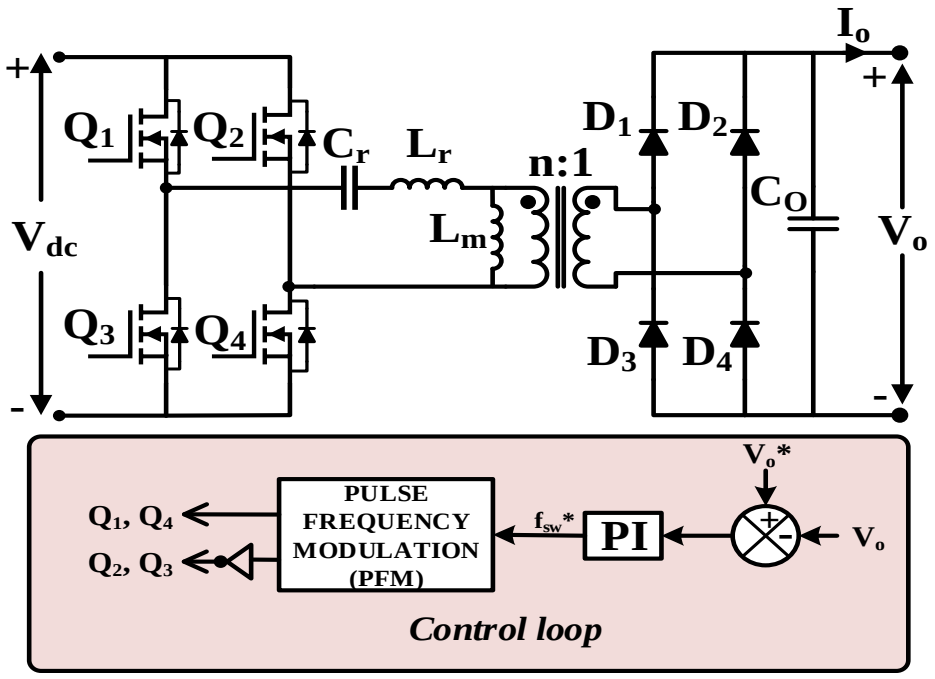


Fig.5.1. Voltage control of LLC resonant converter

The full bridge LLC resonant converter is designed using closed loop voltage control where voltage loop is designed using (5.1) which provides variable switching frequency, f_{sw}^{*}. This acts as an input to the pulse frequency modulation which is explained in the next section of this chapter to generate pulses for the controlled switches Q_1, Q_4 and complementary pulses to Q_2, Q_3 as in Fig.5.1.

$$f_{sw}^{*} = \left\{K_{p_v}(V_o^{*} - V_o) + K_{i_v}\int(V_o^{*} - V_o)\,dt\right\} \tag{5.1}$$

Where, K_{pv} and K_{iv} are PI controller gains for the voltage loop.

5.3 PULSE FREQUENCY MODULATION (PFM) CONTROL

In pulse width modulation the variable is the duty ratio (D) which is varied to achieve the desired output voltage and make regulation easier for the converter. But in pulse frequency modulation (PFM) the duty ratio is kept constant but the switching frequency varies based on the load which is the drawback in the PWM as the switching frequency is constant so at the light load conditions the switching losses are high. Pulse frequency modulation is based on either on-time fixed and variable off-time or off-time fixed and variable on-time. At higher load, switching frequency increases and at light load condition it decreases as in Fig.5.2. This provides higher efficiency due to minimized switching losses across the controlled switches.

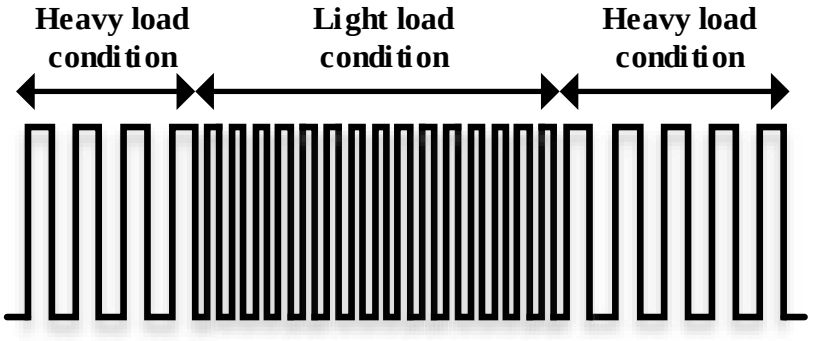


Fig.5.2. Variation in switching frequency (f_{sw}) or number of cycles based on loading condition to generate train of pulses

PFM as operating with variable switching frequency leads to difficulty in designing filter as the frequency cannot be predicted at particular instant. If it comes within the 20 kHz audible range can leads to ringing. So, this have to be consider while controlling a switching converter using pulse frequency modulation (PFM) when designing it on hardware as in Fig.5.4.

In PWM, the duty ratio is varied for regulating the output voltage using (5.2)-(5.3),

$$D = \frac{t_{on}}{t_{on} + t_{off}} = \frac{t_{on}}{T} \tag{5.2}$$

$$T = t_{on} + t_{off} \tag{5.3}$$

For PWM, the output voltage is the function of duty ratio (D),

$$V_o = f^n(D) \tag{5.4}$$

For PFM, the output voltage is the function of switching frequency (f_{sw}),

$$V_o = f^n(f_{sw}) \tag{5.5}$$

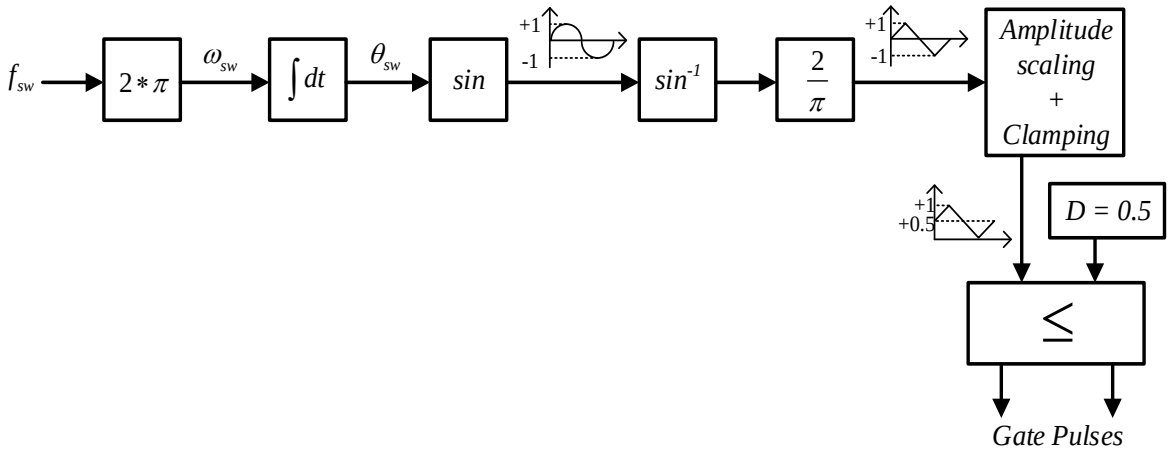


Fig.5.3. PFM control block diagram

Fig.5.3 shows the PFM block diagram where the variable frequency f_{sw} is provides at the input of the system which is the multiplied with 2π to get angular frequency ω_{sw}. This output is then passed through an integrator to produce theta Θ_{sw} and this theta is required to

generate sine wave having amplitude ranging between +1 and -1. This is utilized by forwarding it to the inverse sine to get reference theta which is multiplied by *2/π*, to get a triangular wave having amplitude ranging between +1 and -1. This wave is passed through amplitude scaling and clamping circuits to generate a triangular wave having same number of cycles but amplitude ranging between +1 and 0, zero crossing at +0.5. This generated carrier wave is compared with the duty ratio which is fixed in the case of PFM i.e. *D=0.5* and amplitude of carrier wave is compared with 0.5 and wherever amplitude is less than equal to 0.5, gate pulses are generated. For dead time, a time delay is added in series with the generated pulses to ensure ZVS.

$$\omega_{sw} = 2 * \pi * f_{sw} \tag{5.6}$$

$$\theta_{sw} = \int \omega_{sw} \cdot dt \tag{5.7}$$

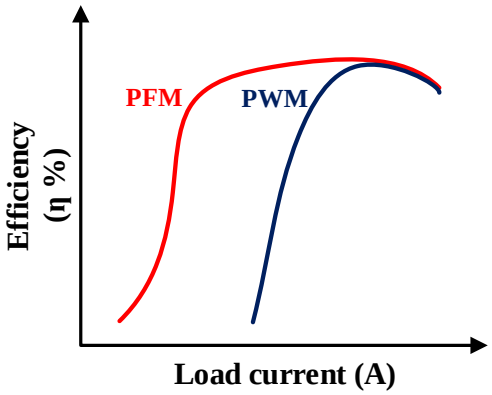
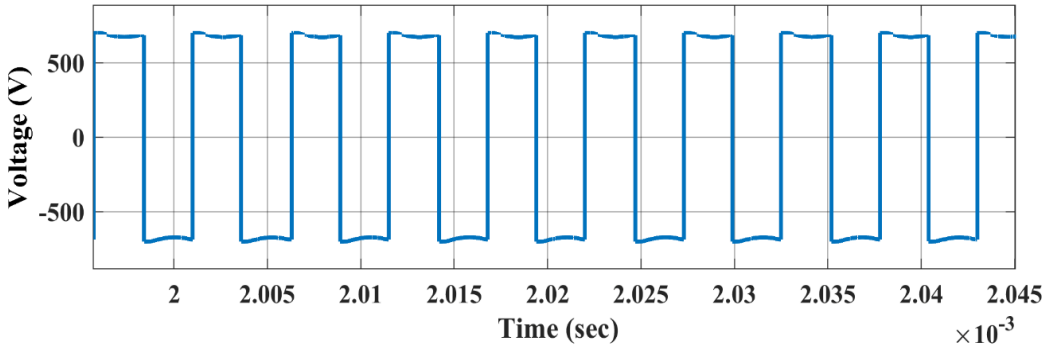


Fig.5.4. Comparison of efficiency for different modulation techniques w.r.t. load

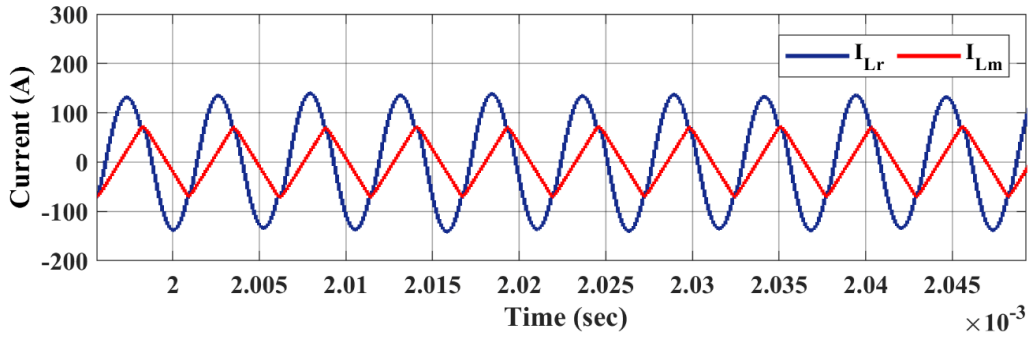
5.4 RESULTS AND PERFORMANCE EVALUATION

The LLC converter performance is evaluated by analyzing the effect of both load side variations and input side variations. Fig.5.5 (a) shows the switching voltage waveform across the LLC tank circuit which is a square waveform having duty, D = 0.5 with calculate delay time to maintain ZVS across primary side controlled switches. Fig.5.5 (b) shows the current through resonating inductor as well as magnetizing inductor. It shows that resonating current is sinusoidal. Fig.5.5 (c) depicts the voltage across resonating capacitor, Cr. Fig.5.5 (d) shows

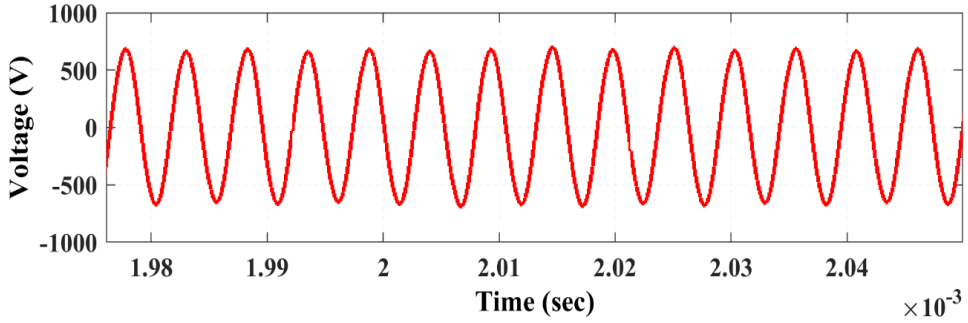
load current waveform and at t=0.01sec, load current is reduced to 50%. Fig.5.5 (e) shows the effect of load variation and it can clearly be depicted that output voltage remains constant after load variation with very less voltage overshoot at t=0.01 sec. Fig.5.5 (f) shows the adaption of the designed control at different reference voltage of 290V. Fig.5.5 (g) depicts the variable input voltage to the LLC converter and its effect on output voltage is shown in Fig.5.5 (h). It can clearly be depicted that output voltage is maintained constant at 300 V with very less voltage overshoot and having settling time of 20ms. Fig.5.5 (i) shows the voltage and current across controlled switch and it can be shown that switch current is lagging voltage which means operation is in inductive region and ZVS is achieving. Fig.5.5 (j) depicts the voltage and current across diodes and proving that ZCS is achieving on secondary side diodes.



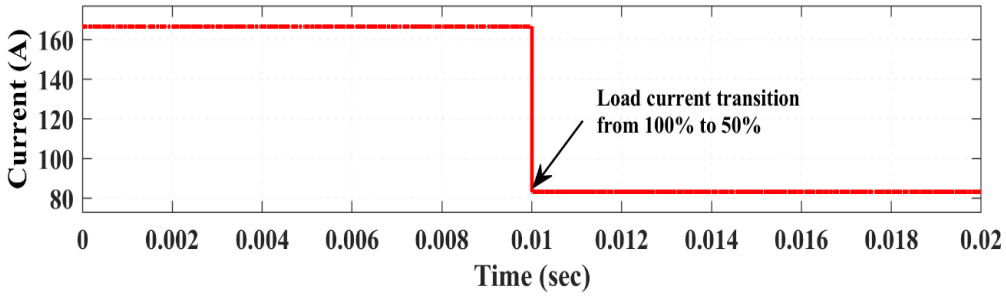
(a) Switching voltage



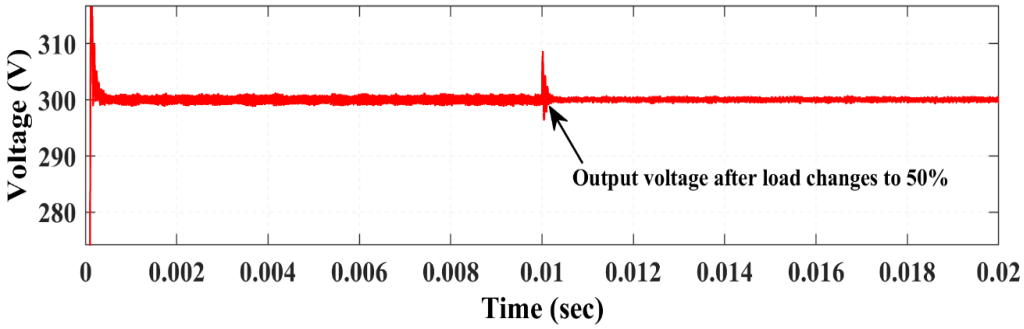
(b) Resonating and magnetizing inductor current



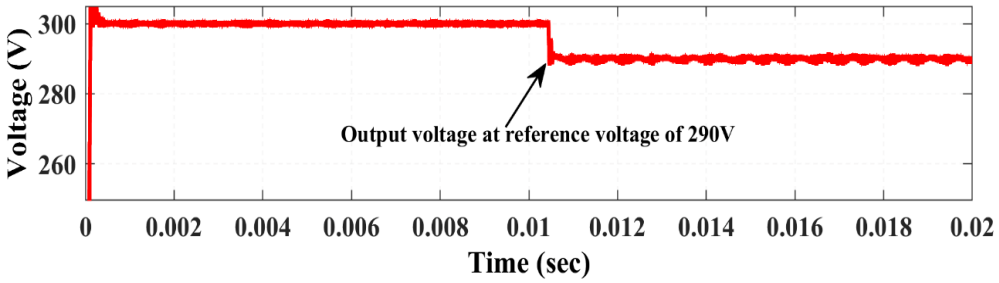
(c) Voltage across resonating capacitor



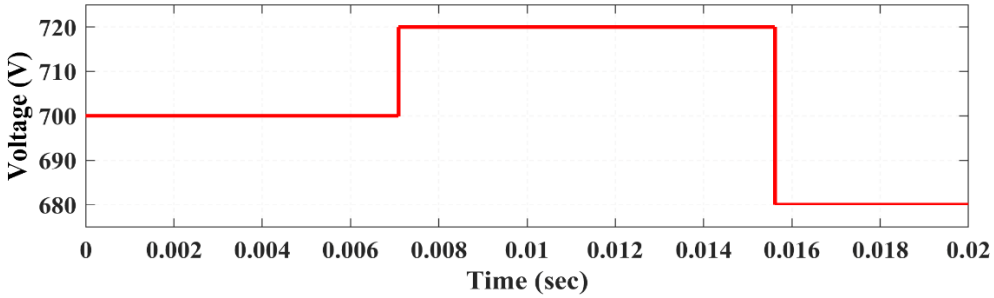
(d) Load current variation



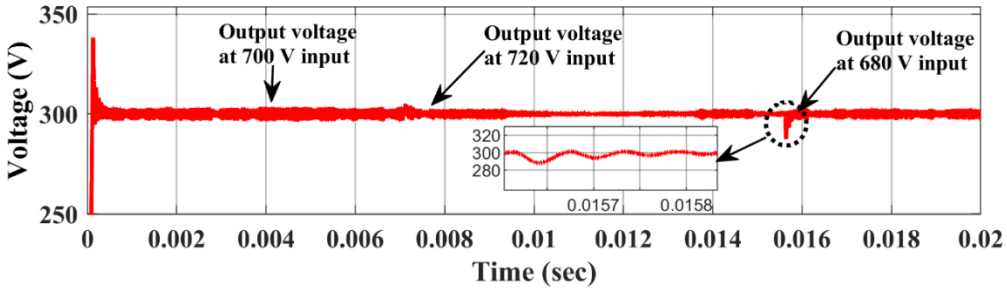
(e) Output voltage adaption due to load current variation



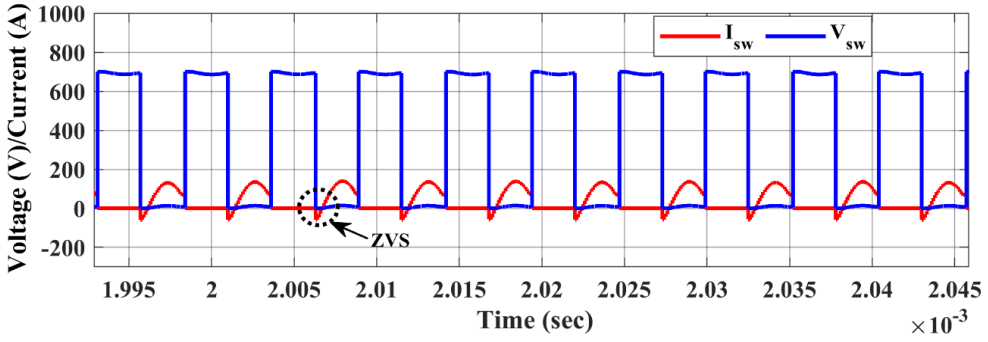
(f) Output voltage tracking at various reference output voltage



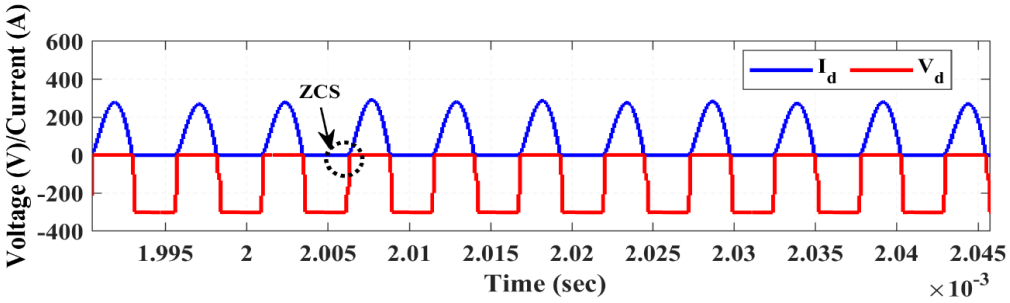
(g) Input voltage variations



(h) Output voltage adaption at various input voltage variation



(i) Voltage and current across primary side switch



(j) Voltage and current across secondary side diode

Fig.5.5. Simulation results of FBLLC resonant converter

5.5 CHAPTER SUMMARY

In this chapter voltage control of LLC resonant converter is designed using pulse frequency modulation (PFM) for controlling the output voltage and analyze the effect of load side and input side variations on the converter. The primary side controlled switches was achieving zero voltage switching (ZVS) and secondary side diodes was achieving ZVS. The control was able to maintain constant output voltage at different input voltage within selected range with very less voltage overshoot. The control was also able to track the reference output voltage and at various loading condition also it was performing effectively.

CHAPTER 6

TWO STAGE VIENNA RECTIFIER FED FULL BRIDGE LLC RESONANT CONVERTER BASED OFF- BOARD EV CHARGER WITH CC-CV CHARGING ALGORITHM

6.1 INTRODUCTION

In this chapter, a 50 kW two stage off-Board EV charger is designed for charging a lithium ion battery using CC-CV algorithm and block diagram of designed system is shown in Fig.6.1. First stage includes three phase Vienna rectifier with power factor correction. The output of the first stage is the DC bus, which acts as an input to the second stage. Second stage includes full bridge LLC resonant converter and a lithium ion battery is connected to the output of second stage. To maintain constant DC bus voltage of 700V and to ensure unity power factor, dual loop control using d-axis and q-axis current control using SVPWM is adopted for controlling Vienna rectifier. FBLLC converter is designed and controlled using CC-CV control algorithm and pulse frequency modulation (PFM) to charge the rated lithium ion battery. The designed system outcomes are validated using MATLAB-Simulink.

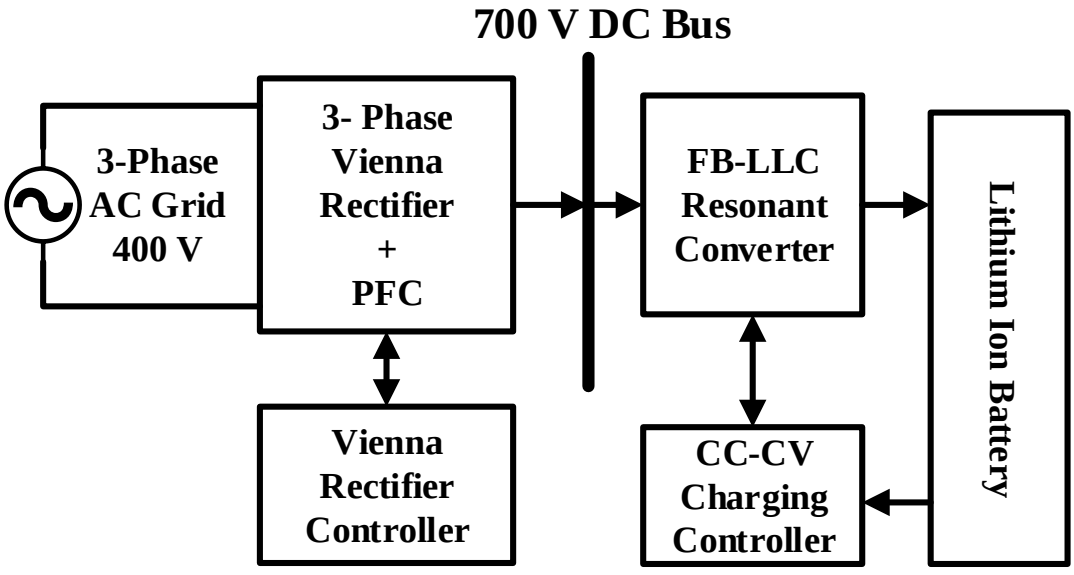


Fig.6.1. Block diagram of designed off-board EV charger

6.2 CIRCUIT DESCRIPTION OF EV CHARGER

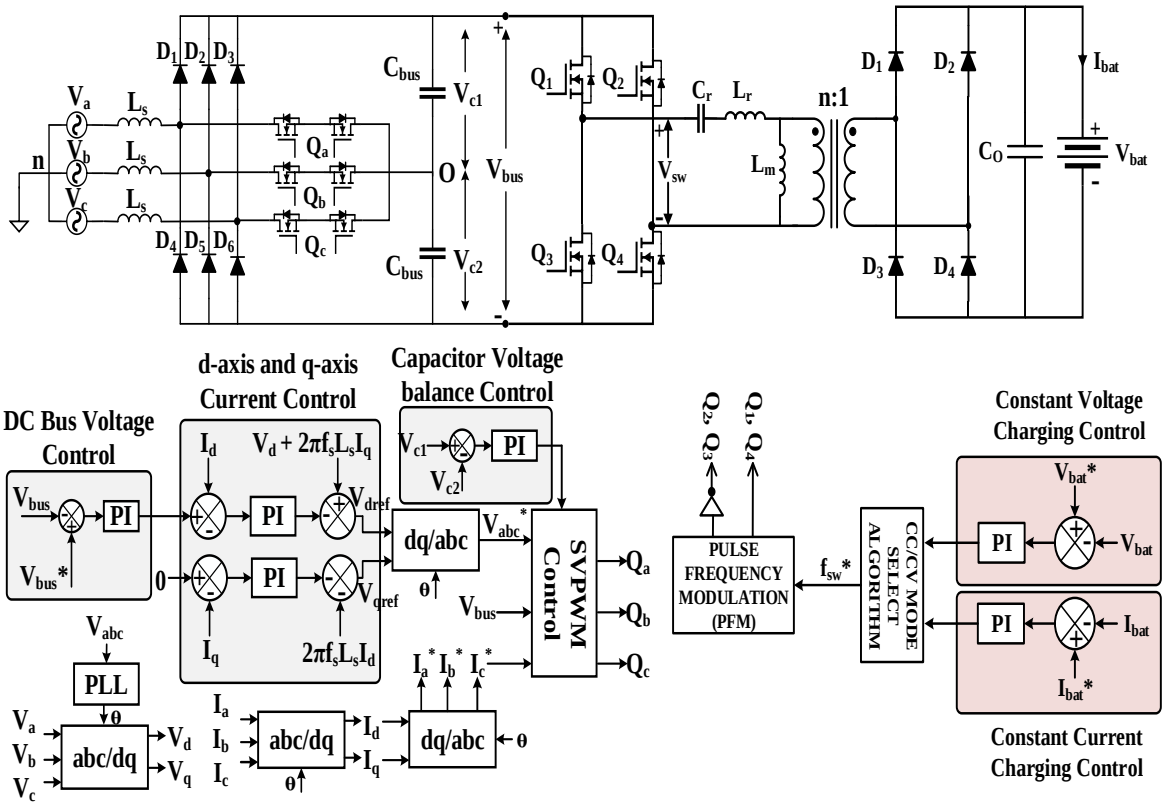


Fig.6.2. Circuit diagram and control diagram of designed off-board EV charger

Vienna rectifier consists of boosting source inductor *'L_s'* followed by a diode bridge rectifier (DBR) and then output bus capacitors *'C_{bus}'*. Vienna rectifier is a multilevel AC/DC converter due to three bidirectional switches Q_a, Q_b, Q_c connected between boosting source inductor and mid-point of bus capacitors. By using a control algorithm, power factor (p.f.) can be improved by reducing Total Harmonic Distortion (THD) [42]. It maintains a bus voltage of 700 V under all grid and load side variations. The output of the three phase Vienna rectifier acts as an input supply to the LLC resonant converter. This voltage is provided to a switching circuit which is basically a full bridge inverter to generate a bipolar square waveform to excite the LLC tank circuit. L_r, C_r resonates at resonant frequency f_o and behaves as series resonant circuit. After resonance, the LLC tank circuit provides a sinusoidal current which is resonating at resonant frequency. The magnitude of this current is controlled using the turns ratio of the high frequency transformer. This current is then transferred to the

secondary side which includes the diode bridge rectifier for rectification and followed by the output filter capacitance which gives DC at the output. This DC is utilized to charge a lithium-ion battery. Fig.6.2 shows the circuit diagram and control diagram for the designed off-board EV charger.

The designing of Vienna rectifier and full bridge LLC resonant converter is analyzed as discussed in chapter 2 and chapter 4 respectively and specification of first stage is tabulated in Table 6.1 and specification of second stage is tabulated in Table 6.2.

Table 6.1. Design specification for first stage Vienna rectifier

Parameters	**Value**
L-L rms grid voltage (V_{abc}), grid frequency (f_s)	400 V, 50 Hz
Output DC bus voltage (V_{bus})	700V
Power rating (P_{ac})	50 kW
Output current (I_o)	71.4285 A
Switching frequency (f_{sw})	200 kHz
Bus capacitor (C_{bus})	4300 µF
Boosting source inductance (L_s)	41 µH
Input current THD	< 3%

Table 6.2. Design specifications for second stage FBLLC resonant converter

Parameters	**Value**
Bus voltage range (V_{busmin}-V_{busmax}), Nominal bus voltage (V_{busnom})	675-725 V, 700 V
Output voltage range (V_{omin}-V_{omax}), Nominal output voltage (V_{onom})	280-320 V, 300 V
Transformer turns ratio (n)	7:3
Quality factor (Q)	0.6
Resonating inductor (L_r)	3.8 µH
Resonating capacitor (C_r)	167 nF
Magnetizing inductance (L_m)	12.5 µH
Resonating frequency (f_o)	200 kHz
Inductance ratio (L_x)	3.3

6.3 CONTROL OF EV CHARGER

6.3.1 Vienna Rectifier Control

Vienna rectifier is controlled using d-axis and q-axis current control. In this algorithm, three loops are designed, output DC bus voltage control loop, d-axis and q-axis current control loop and capacitor voltage balance control as in Fig.6.2. The pulses for controlled switches Q_a, Q_b and Q_c are generated using SVPWM [45]. The control loops are designed using (6.1)-(6.5),

$$V_{q_{ref}} = \begin{Bmatrix} -\left(K_{p_{i_q}}(0 - I_q) + K_{i_{i_q}} \int (0 - I_q) dt\right) \\ -2\pi f_s L_s I_d \end{Bmatrix} \tag{6.1}$$

$$I_{d_{ref}} = \begin{Bmatrix} K_{p_{v_{bus}}}(V^*_{bus} - V_{bus}) + \\ K_{i_{v_{bus}}} \int (V^*_{bus} - V_{bus}) dt \end{Bmatrix} \tag{6.2}$$

$$\Delta V_c = K_{p_{v_c}}\left(V_{c_1} - V_{c_2}\right) + K_{i_{v_c}} \int \left(V_{c_1} - V_{c_2}\right) dt \tag{6.3}$$

$$V_{d_{ref}} = \begin{Bmatrix} K_{p_{i_d}}\left(I_{d_{ref}} - I_d\right) + \\ K_{i_{i_d}} \int \left(I_{d_{ref}} - I_d\right) dt \\ +V_d + 2\pi f_s L_s I_q \end{Bmatrix} \tag{6.4}$$

$$V_{bus} = V_{c_1} + V_{c_2} \tag{6.5}$$

Where V_{dref}, V_{qref}, and I_{dref} ,I_{qref}, are the reference voltages and reference currents for d-axis and q-axis respectively. V_{bus}* is the reference output bus voltage. V_{c1} and V_{c2} are voltages across DC bus capacitors. In (6.1)-(6.4) the different parameters Kp_{iq} and Ki_{iq} are PI controller gains for q-axis current loop, Kp_{id} and Ki_{id} are PI controller gains for d-axis current loop, Kp_{vbus} and Ki_{vbus} are PI controller gains for output bus voltage loop, Kp_{vc} and Ki_{vc} are PI controller gains for bus capacitors voltage balance loop. Fig.6.3 shows different space vectors in Vienna rectifier control.

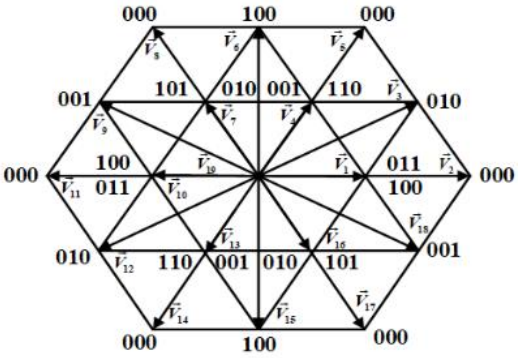


Fig.6.3. Diagram of space vectors for Vienna rectifier

6.3.2 FBLLC Resonant Converter Control

In constant voltage (CV) mode the sensed battery voltage V_{bat} is compared with the reference battery voltage V_{bat}* and the produced error is provided to a PI controller to generate a reference frequency f_{sw}*. In constant current (CC) mode the sensed battery current I_{bat} is compared with the reference battery current I_{bat}* and the produced error is provided to a PI controller to generate a reference frequency f_{sw}*. A CC-CV selector algorithm is designed to switch between CC mode and CV mode as in Fig.6.5. The generated reference frequency f_{sw}* is provided to the pulse frequency modulation (PFM) to generate pulses for switches Q_1, Q_4 and complementary pulses for switches Q_2, Q_3 as in Fig.6.2. This variable frequency f_{sw}* is responsible in controlling the output voltage as in (6.6)-(6.7),

$$f_{sw}^{*} = \begin{Bmatrix} K_{p_{CV}}(V_{bat}^{*} - V_{bat}) + \\ K_{i_{CV}} \int (V_{bat}^{*} - V_{bat})\, dt \end{Bmatrix} \tag{6.6}$$

$$f_{sw}^{*} = \begin{Bmatrix} K_{p_{CC}}(I_{bat}^{*} - I_{bat}) + \\ K_{i_{CC}} \int (I_{bat}^{*} - I_{bat})\, dt \end{Bmatrix} \tag{6.7}$$

Where K_{pcv} and K_{icv} are the PI controller gains for CV charging and K_{pcc} and K_{icc} are the PI controller gains for CC charging.

There is a lot of chemistry involved in a battery, various charging algorithms are adopted for charging different types of batteries. In EVs mostly lithium polymer batteries are in practice. For lithium-ion batteries constant current (CC) - constant voltage (CV) algorithm is preferred over other charging algorithms as in Fig.6.4. Firstly, the battery is charged using

constant current I_{bat}*, till the battery voltage reaches a certain level, V_{bat}^{th} which is the threshold for transition from CC mode to CV mode. After V_{bat}^{th} , the battery current starts to decrease until the battery current reaches 10% of battery current which is denoted as $I_{bat}^{lim} = 0.1I_{bat}$*, and battery voltage remains almost constant at V_{bat}^{th}.

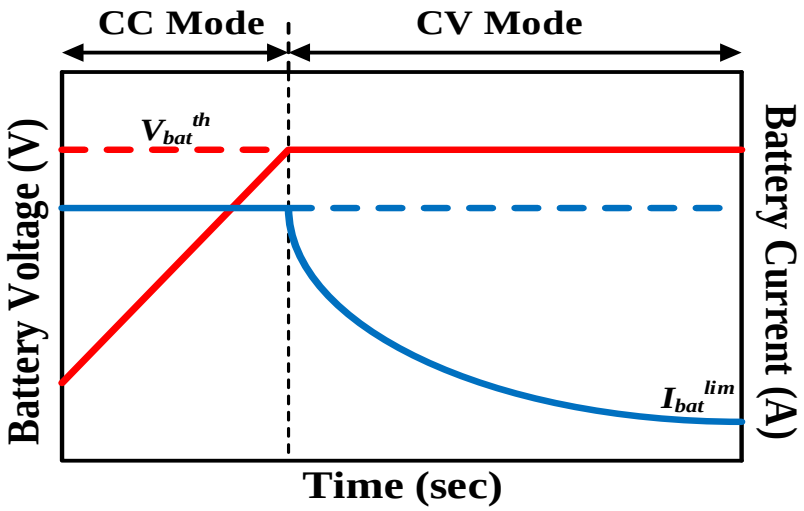


Fig.6.4. CC-CV charging curve

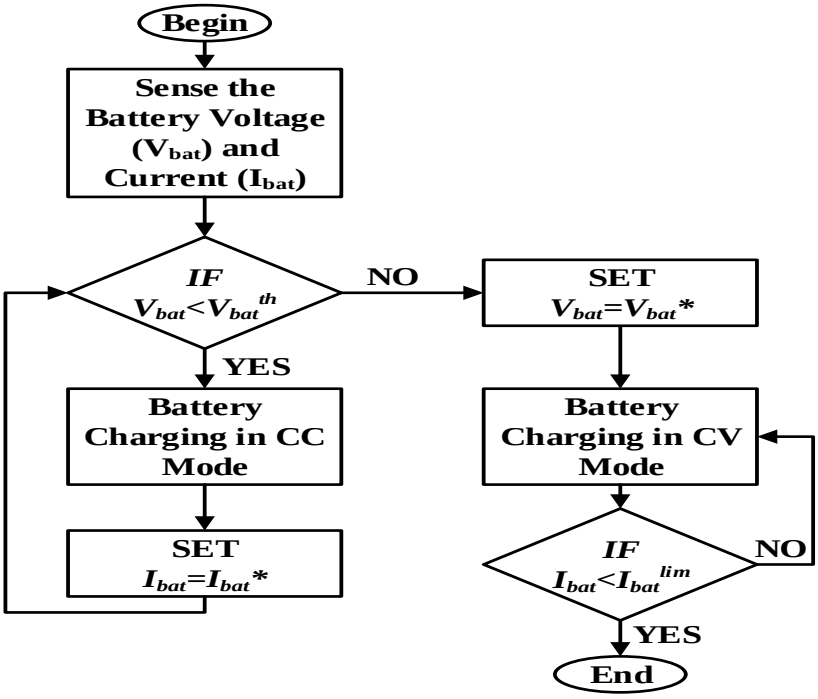


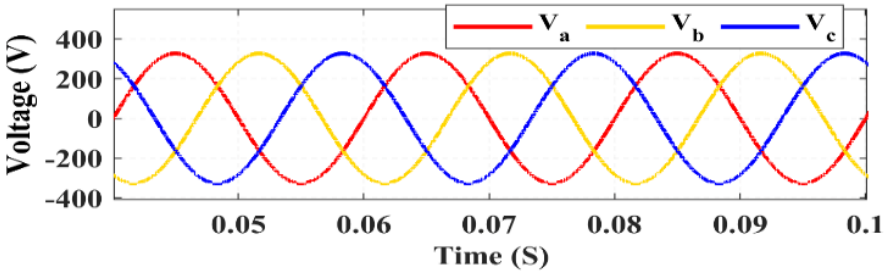
Fig.6.5. Proposed CC-CV charging algorithm

6.4 RESULTS

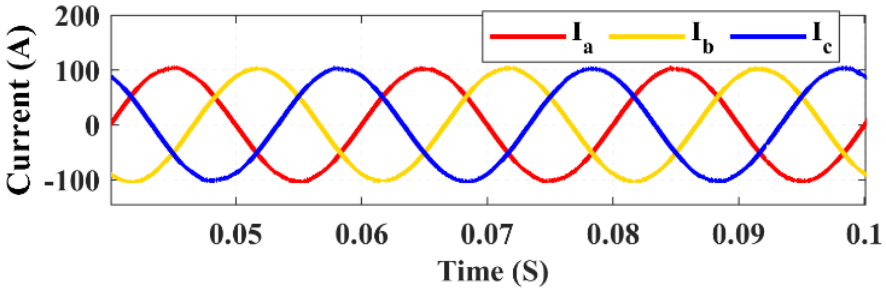
A 50 kW two stage off board EV charger is designed for charging a 280 V/ 112Ah lithium ion battery at high C-rate and the results and outcomes are validated using MATLAB-Simulink. Fig.6.6 (a) depicts the three phase line-to-line rms grid voltage. It can be clearly shown from Fig.6.6 (b) that three phase grid current is in phase with grid voltage. Fig.6.6 (c) shows that Vienna rectifier is able to maintain the 700 V bus voltage which acts as an input for LLC resonant converter. Fig.6.6 (d) shows that bus capacitor voltages are totally balance to provide constant 700 V bus voltage. From Fig.6.6 (e) the FFT analysis of phase 'a' grid current can be analyzed and THD comes out to be 2.35 %.

The LLC resonant converter is designed and outcomes are stated in Fig.6.7. Fig.6.7 (a) depicts the switching voltage V_{sw} having peak values as +700V and -700V which is the output of the full bridge inverter and this voltage is applied on the resonating circuit. Fig.6.7 (b) shows the output waveforms of the resonating inductor current, I_{lr} which resembles sinusoidal wave and magnetizing Inductor current, I_{lm}. Fig.6.7 (c) shows the resonating capacitor voltage, V_{cr}. The primary controlled switches are operated in ZVS and secondary diodes are operating in ZCS which can be proved using Fig.6.7 (d) and Fig.6.7 (e) respectively. From Fig.6.7 (d) it is clear that converter is operating in the inductive region and the current lags behind the voltage which leads to minimum losses and efficient operation.

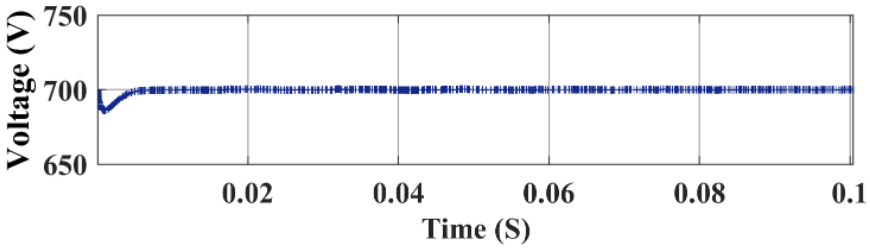
Fig.6.8 (a) shows the battery voltage, which increases till the battery voltage attains threshold voltage $V_{bat}^{th}=300\ V$ at t=0.141s and afterwards remains almost constant. Fig.6.8 (b) shows the battery current which remains constant at $I_{bat}*=150$ A till the battery voltage reaches V_{bat}^{th} and after that starts decreasing to reach the limit current, I_{bat}^{lim}. But here we have demonstrated the charging of lithium ion battery for a limited time duration for the verification of the charging algorithm. Fig.6.8 (c) depicts the state of charge (SOC) of the battery. Here, at 80 % SOC the battery voltage is determined as 298.5 V and at t=0.2s battery current I_{bat} is around 100 A based on control loops which will decrease further till I_{bat}^{lim}, which is used for validating the CC-CV control. Fig.6.8 (d) shows that, at 150 A battery can be charged at faster rate in around 44 minutes.



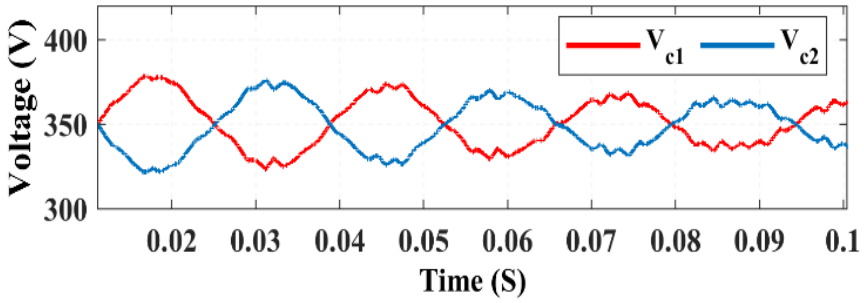
(a) 3-phase grid voltage



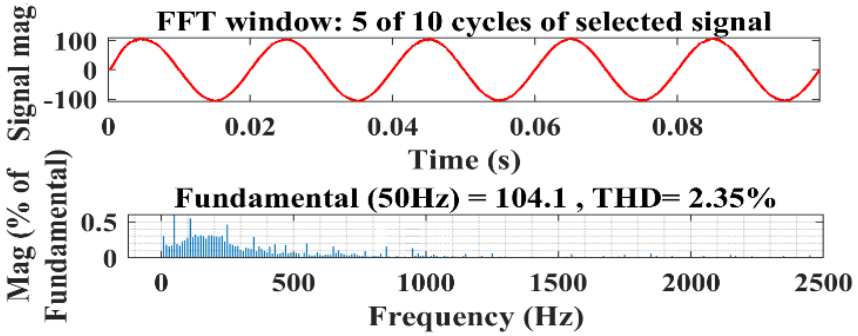
(b) 3-phase grid current



(c) DC bus voltage

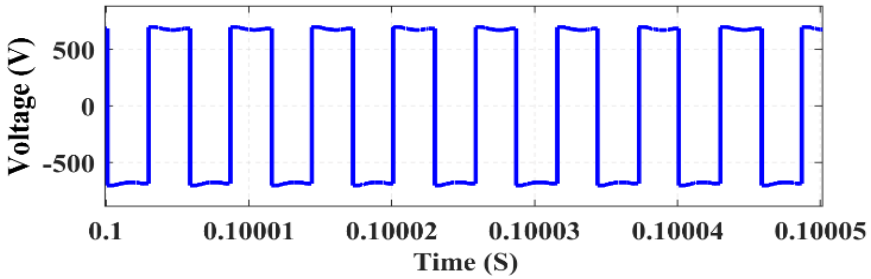


(d) Bus capacitors voltage balance

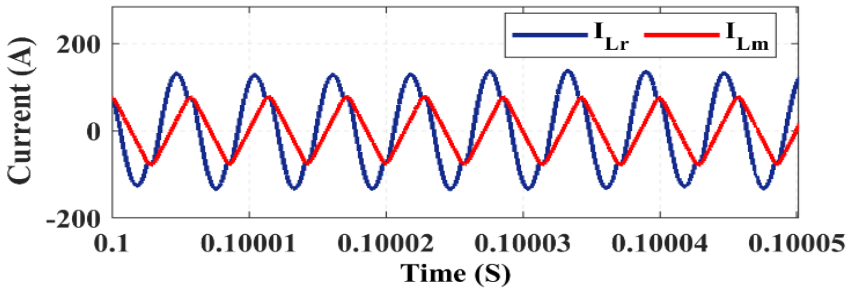


(e) FFT analysis of grid current

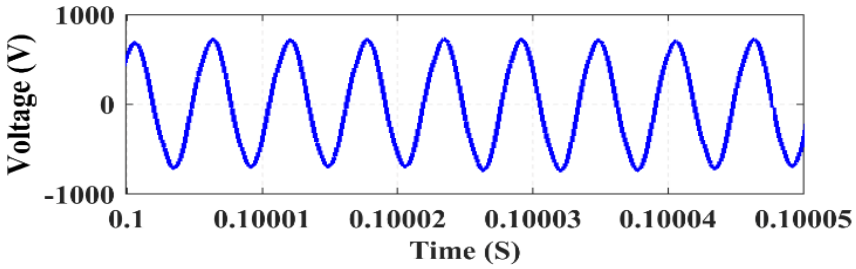
Fig.6.6. Simulation results of first stage Vienna rectifier



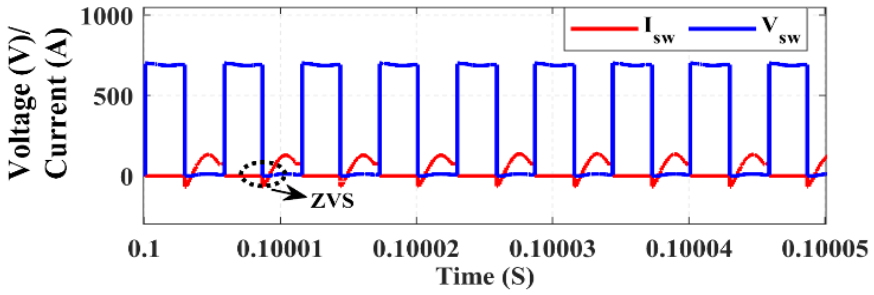
(a) Switching voltage



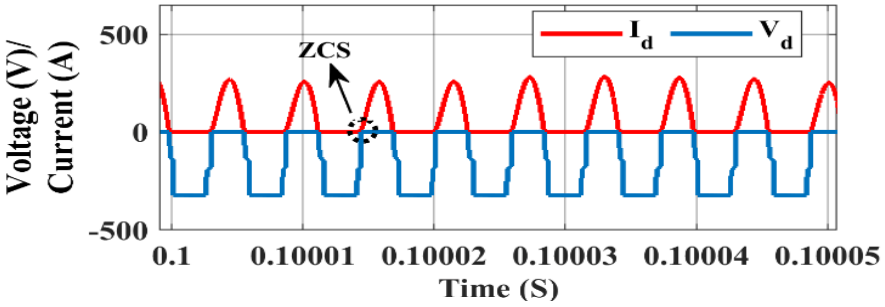
(b) Resonating and magnetizing inductor current



(c) Voltage across resonating capacitor

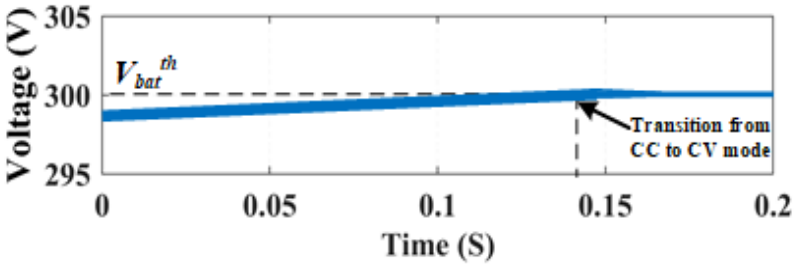


(d) Voltage and current across primary side switch

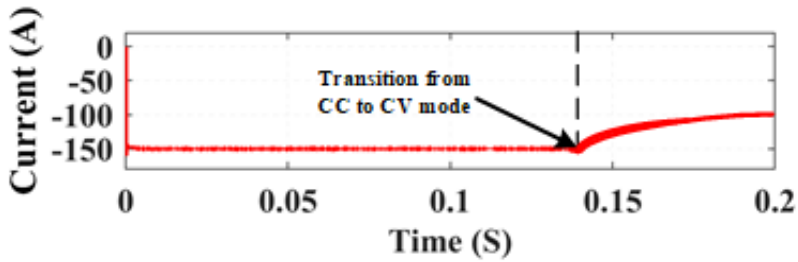


(e) Voltage and current across secondary side diode

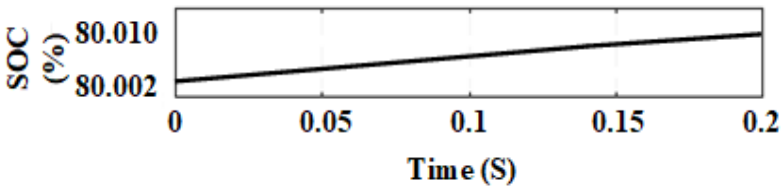
Fig.6.7. Simulation results of second stage FBLLC converter



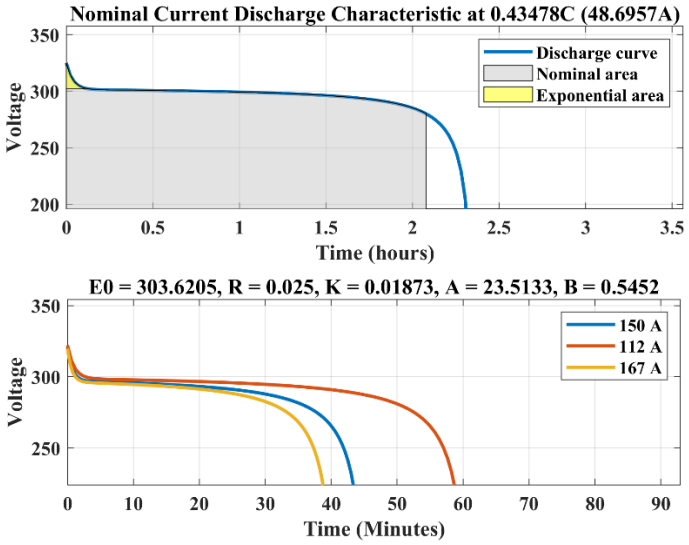
(a) Battery voltage



(b) Battery current



(c) Battery state of charge (SOC)



(d) Battery discharge characteristic at various C-rates

Fig.6.8. Simulation results of lithium ion battery

6.5 CHAPTER SUMMARY

In this chapter, a complete designing of a 50 kW two stage off-board EV charger for charging a 280 V/ 112 Ah lithium ion battery is discussed. All the design considerations were taken into account to ensure ZVS and provide efficient charging. In first stage three phase Vienna rectifier was designed and it was able to minimize the THD to 2.35%, providing almost u.p.f. and capable of maintaining 700 V bus voltage. In second stage full bridge LLC converter was designed to ensure ZVS in the primary side controlled switches and ZCS in secondary side diodes. The DC voltage at the output of the LLC converter is utilized for charging the battery using designed CC-CV algorithm. The designed off-board charger is capable of charging a battery while mitigating its effects on the grid side. All the results and discussion are validated using MATLAB-Simulink and presented in this chapter.

CHAPTER 7
CONCLUSION AND FUTURE SCOPE

7.1 CONCLUSION

In this work, a two stage off-board charger is designed and controlled using CC-CV charging algorithm. The work was divided into three objectives. First objective was designing and controlling of Vienna rectifier. In this objective, Vienna rectifier considering system parasitic was also studied and a modified dual loop control using q-axis and d-axis current control using SVPWM was proposed. In this objective, a 50 kW Vienna Rectifier considering system parasitic is analyzed using three control algorithms: dual loop using hysteresis current control, dual loop using q-axis and d-axis current control using SVPWM and modified dual loop using q-axis and d-axis current control using SVPWM. The control algorithms are implemented in MATLAB-Simulink. The dual loop hysteresis current control algorithm was adaptive to the grid voltage variations but not adaptive to the grid frequency variations and is able to mitigate the sudden load variations and reference DC Bus voltage variation but with a sluggish dynamic response with oscillations in transient state. The dual loop control using d-axis and q-axis current control algorithm using SVPWM was adaptive to both grid voltage and grid frequency variations including sudden load variations and reference DC Bus voltage variation but with an improved dynamic response with minimal oscillations in transient state. The proposed modified dual loop control using d-axis and q-axis current control algorithm using SVPWM was able to improve the dynamic response by reducing the settling time and eliminating the oscillations in transient state. So, this is the preferred control algorithm compared to other two. To support the proposed modified control, small signal analysis was performed. All the control algorithms were able to achieve near to unity p.f. with varied performance. In this paper, the adopted power ratings are high due to its application, so conduction losses are also analyzed for a complete sector. The system designed is efficiently mitigating the load variations and grid side variations which suits its application in emerging EV charging topologies.

The second objective was designing and control of full bridge LLC resonant converter. In this objective, LLC converter design as well as magnetic design was discussed in detail. In this objective voltage control of LLC resonant converter is designed using pulse frequency modulation (PFM) for controlling the output voltage and analyze the effect of load side and input side variations on the converter. The primary side controlled switches was achieving zero voltage switching (ZVS) and secondary side diodes was achieving ZVS. The control was able to maintain constant output voltage at different input voltage within selected range with very less voltage overshoot. The control was also able to track the reference output voltage and at various loading condition also it was performing effectively.

The third objective was completed by combining both stages and in this objective, a complete designing of a 50 kW two stage off-board EV charger for charging a 280 V/ 112 Ah lithium ion battery is discussed. All the design considerations were taken into account to ensure ZVS and provide efficient charging. In first stage three phase Vienna rectifier was designed and it was able to minimize the THD to 2.35%, providing almost u.p.f. and capable of maintaining 700 V bus voltage. In second stage full bridge LLC converter was designed to ensure ZVS in the primary side controlled switches and ZCS in secondary side diodes. The DC voltage at the output of the LLC converter is utilized for charging the battery using designed CC-CV algorithm. The designed off-board charger is capable of charging a battery while mitigating its effects on the grid side. All the results and discussion are validated using MATLAB-Simulink and presented in this work.

7.2 FUTURE SCOPE

- Interleaving of each phases of Vienna rectifier can be done to increase the power density of the converter and to develop the off-board charger which will be capable of charging at higher C-rate.
- Vienna rectifier can also be modified to provide bidirectional operation which will provide feature of vehicle-to-grid (V2G).
- As, Vienna rectifier have two bus capacitor at the output with common mid-point, so LLC resonant can be designed to provide multi-port charging. This will make charging operation fully utilized.

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