SIMULATION AND ANALYSIS OF III-V COMPOUND SEMICONDUCTING HETERO-MATERIAL BASED JUNCTION-LESS TUNNEL FET FOR IMPROVED PERFORMANCE.

Thesis submitted by

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In Partial Fulfilment of the Requirements for the Degree of

DOCTOR OF PHILOSOPHY

Under the Supervision of

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July-2022.

In the memory of my Late Father...

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CERTIFICATE

This is to certify that the thesis titled "***Simulation and Analysis of III-V Compound Semiconducting Hetero-Material based Junction-Less Tunnel FET for Improved Performance***" is being submitted by ***Ms. SAMRITI SHARMA*** with registration number ***2K18/PHDAP/21*** to the Delhi Technological University for the award of the degree of Doctor of Philosophy in Applied Physics. The work embodied in this thesis is a record of bonafide research work carried out by me in the Microelectronics Research Lab, Applied Physics Department, Delhi Technological University, New Delhi under the guidance of ***Prof. RISHU CHAUJAR***. It is further certified that this work is original and has not been submitted in part or fully to any other university or institute for the award of any degree or diploma.

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Ph.D is not a 100-metres race but a marathon, so winning a marathon cannot be an effort of a single individual. Although I am submitting my Ph.D thesis after four years of efforts but my learning during PhD has laid a solid foundation on which I can work in the future. The completion of this wonderful journey wouldn't be possible without the support of so many individuals.

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Samriti Sharma

ABSTRACT

SIMULATION AND ANALYSIS OF III-V COMPOUND SEMICONDUCTING HETERO-MATERIAL BASED JUNCTION-LESS TUNNEL FET FOR IMPROVED PERFORMANCE.

Tunnel FET has been proved to be the best alternative to the conventional MOSFET in low power electronic applications. In this thesis, various techniques have been proposed to enhance the performance of a TFET device by improving the key parameters like ON current (I_{ON}), threshold voltage (V_{th}), steeper subthreshold swing (SS), ambipolar conduction, and parasitic capacitances using Technology Computer Aided Design (TCAD).

The initial focus is to reduce the fabrication complexity of doping junctions with a charge plasma based junctionless TFET architecture by consolidating the advantages of both a junctionless FET (higher ON current, I_{ON}) and a TFET (steeper subthreshold swing, SS). To elevate the I_{ON} and suppress the leakage current (I_{OFF}), bandgap engineering has been implemented by utilizing the III-V compound semiconducting hetero-material (InAs/GaAs) source/channel (S/C) tunneling interface. Further, dual material gate (DMG) engineering has been applied by choosing a lower work function tunnel gate (TG) towards the source region and a higher work function supplementary gate (SG) towards the drain region. The 2-D TCAD simulations have been executed to explore the impact of TG process variations - work function and length on analog/RF and linearity figure of merits (FOMs) of DMG-HJLTFET. The extracted result parameters have also been compared to single metal gate (SMG)-HJLTFET and conventional Si-JLTFET. The work function and length of TG is optimized to attain the best device characteristics. A significant band bending has been established at the hetero-material tunneling interface of DMG-HJLTFET leading to narrower barrier width by the application

of DMG engineering. The SS of DMG-HJLTFET is 52.4% and 88.8% reduced in comparison with SMG-HJLTFET and Si-JLTFET due to the energy-band profile modulation obtained by dual-material gate technology and III-V compound semiconducting materials. The DMG-HJLTFET exhibits a high current switching ratio of 3.1×10^{11} as compared to SMG-HJLTFET (1.4×10^{11}) and Si-JLTFET (1.8×10^{6}).

The use of mono-dielectrics (low-k or high-k oxides) in the oxide region of H-JLTFET leads to poor I_{ON} due to the ambipolar conduction. Therefore, a heterogeneous gate dielectric (HD) engineering is executed by developing a heterogeneous gate dielectric stack having high-k and low-k material in the oxide region under control gate (CG) nearby the source and drain regions, respectively. The performance of HD-HJLTFET has been compared with mono-dielectric high-k HJLTFET and low-k HJLTFET. The selection of an appropriate high-k oxide for the hetero dielectric and length of the high-k oxide in HD-HJLTFET has been optimized using different dielectric materials - HfO_2 (k = 25), ZrO_2 (k = 22), Al_2O_3 (k = 9), Si_3N_4 (k = 7), and SiO_2 (k = 3.9) in the high-k region. The superior performance of HD-HJLTFET in terms of I_{ON}, current switching ratio (I_{ON}/I_{OFF}), device efficiency, and SS makes it an appropriate alternative for low power and fast switching applications.

However, developing a hetero-structure TFET using an amalgamation of InAs (binary)-AlGaSb (ternary, in place of GaAs-binary) III-V compound semiconducting materials provides a tunable bandgap at the S/C interface of H-JLTFET, where the energy bandgap of ternary material, $Al_xGa_{1-x}Sb$ depends on the Al-mole fraction value (x.composition). The properties of $Al_xGa_{1-x}Sb$ can be modified by changing the x-composition, therefore the device structure can be optimized for best outcomes by using this material in the channel and drain region. The suitability of lattice matched standard III-V growth and processing techniques are the prime reason for choosing these materials. The superior performance is attributed to the conduction band local minima induced at the channel yielding to narrower tunneling barrier width at an optimized Al-mole fraction (0.15) of AlGaSb. 77 times higher g_m of H-JLTFET led to 5×10^6 and 205 times higher device efficiency and f_T along with

~66% reduction in the parasitic capacitance making it favorable for high-speed switching applications as compared to Si JLTFET.

The interface trap charges (ITCs) at the semiconductor/oxide interface originating during the fabrication process of electronic device plays an important role in reliability issues. In real environment, a higher number of positive and negative ITCs develop at the Si-SiO_2 interface while fabricating the device. These ITCs strongly affect the reliability of the device. Therefore, the impact of ITCs polarity and density has been analyzed for HD-HJLTFET and has been compared with the ideal case of defect free device. The high-k dielectric towards S/C interface and low-k dielectric towards D/C interface in HD-HJLTFET results in enhanced analog/RF performance metrics with negligible variation against different ITC polarity than its counter device. The linearity parameters of HD-HJLTFET (VIP2, VIP3, IIP3, 1dB compression point, and IMD3) also showed marked improvement with negligible variation against different ITC polarity than its counter device, making it more reliable for low power microwave and distortion-free wireless communication systems.

Till now only polar gate (PG) and CG are considered responsible for the retention of hole plasma and electron plasma in JLTFET. However, polar gate is not the only one responsible for the retention of hole plasma in the p^+ prompted source but the hole plasma near the interface of source electrode metal and p^+ prompted source (SEM/S) is influenced by the choice of source electrode metal work function too. Therefore, a comprehensive investigation of the mutual significance of PG and SEM work function on p^+ prompted source has been done by considering three metals – W (4.55 eV), Mo (4.65 eV), and Pd (5.3 eV) as the source electrodes in HJLTFET. The Schottky tunneling phenomenon is considered by implementing the Universal Schottky Tunneling (UST) model to study the underestimated drain current of HJLTFET and the preference of ohmic contacts over Schottky contacts has also been discussed. However, the UST model becomes inconsequential for SEM work function higher than p^+ prompted source (Pd) as hole plasma is preserved by the ohmic contact formation.

LIST OF PUBLICATIONS

CHAPTER CONTRIBUTED IN A BOOK:

1. **Sharma, S**. and Chaujar, R., 2021. High Switching Performance of Novel Heterogeneous Gate Dielectric—Hetero-Material Based Junctionless-TFET. In *Microelectronics, Circuits and Systems* (pp. 3-12). ***Springer***, Singapore.

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2. **Sharma, S**. and Chaujar, R., 2022. RF, linearity and intermodulation distortion analysis with small-signal parameters extraction of tunable bandgap arsenide/antimonide tunneling interfaced JLTFET. *Microsystem Technologies*, pp.1-9. ***Springer (SCIE, IF-2.27).***

3. **Sharma, S**. and Chaujar, R., 2022. Impact of Tunnel Gate Process Variations on Analog/RF and Small Signal Parameters of Hetero-material Tunneling Interfaced Charge Plasma Junctionless TFET. *International Journal of Circuit, Theory and Applications.* ***Wiley Online Library (SCIE, IF-2.03).***

4. **Sharma, S.** and Chaujar, R., 2021. Performance enhancement in a novel amalgamation of arsenide/antimonide tunneling interface with charge plasma junctionless-TFET. *AEU-International Journal of Electronics and Communications*, *133*, p.153669. ***Elsevier (SCIE, IF-3.18).***

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CHAPTER-1

INTRODUCTION

This chapter describes the background enlisting the shortcomings of MOSFET and quest for steeper subthreshold devices. It describes the fundamental working principle and basic structure of tunnel field effect transistor (TFET). The major challenges faced by TFET and the possible solution to those issues are also discussed. Thereafter, various engineering techniques available in the literature are described to improve the performance of TFET for analog/RF and wireless applications. Further, the chapter includes the research gaps available in the literature and the research objectives of this thesis. Lastly, a brief summary of each chapter has been given for an overview of the thesis.

1.1 BACKGROUND

The metal oxide semiconductor field effect transistor (MOSFET) has been the crucial building block of integrated circuits (ICs) and global electronics industry [1]. The foundation of the electronic industry relies on Moore's law proposed by Gordon Moore (ITRS, 2015), which follows the phenomenon of doubling the number of transistors in every two years. The specifications of Moor's law for the 2016 technology node have been improvised from 120 nm (ITRS, 1999) to 100 nm (ITRS, 2001, 2002) by the International Technology Roadmap for semiconductors (ITRS) [2-5]. As the fabrication of first integrated circuits were achieved with a small number of MOSFETs, it eventually increased the hunger and necessity towards better complexed hardware circuitry and a higher number of transistors. The downscaling of the MOSFET dimensions seemed to be the most prominent key to accomplish this fast-increasing value, which is administered by the want of high switching speed, low operating power, and higher packing density. It also enhances the switching speed and cut-off frequency to Giga-Hertz regime making it suitable for high frequency and wireless applications [4-5].

However, the conventional MOSFET device is approaching near the limits of scaling. Therefore, investigation for alternate devices is under process. Even though downscaling has led to many benefits in the fabrication of transistors like enhanced speed and efficiency and area efficiency. however, many critical issues like short channel effects (SCEs) are also introduced [6]. Due to these SCEs, the subthreshold swing (SS) increases beyond the fundamental limit of MOSFET (60 mV/decade) and hence the leakage current is increased. The threshold voltage needs to be reduced to scale down the supply voltage of MOSFET. However, the non-scalability of SS leads to higher threshold voltage and hence the leakage current rises exponentially. It leads to supply voltage scaling issues and hence results in increased power consumption. The standby power dissipation can be

controlled by decreasing the leakage current. The researchers across the globe have proposed various novel materials and device engineering techniques to overcome these issues [7-9].

In digital applications of MOSFET, steeper ON to OFF transition is the prime requirement for which it should attain lower SS and higher I_{ON}/I_{OFF} ratio. For improved performance of MOSFET, the I_{ON}/I_{OFF} ratio should be higher. For lower static power dissipation, the SS should be lower. The techniques addressed by many researchers successfully achieved higher I_{ON}/I_{OFF} ratio. However, the SS of MOSFET is limited to be greater than 60 mV/decade due to the current switching process of MOSFET, which is the thermionic emission of carriers over the potential barrier [10-12].

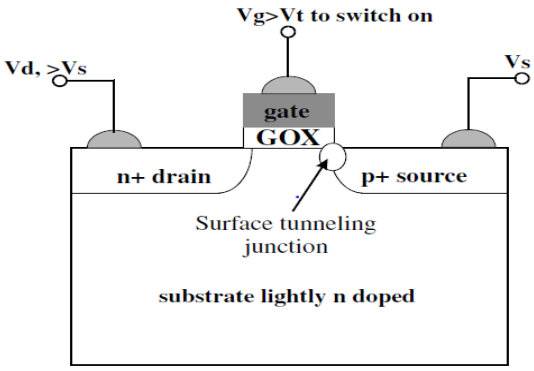
The research community has come forth with many alternatives to design more efficient downsized FETs with different underlying mechanism of carrier transport and better performance reliability as compared to MOSFET [13-14]. Various steeper subthreshold slope devices having working principle different than MOSFET like quantum tunnelling-based tunnel FET (TFET), Coulomb blockade based single electron transistor (SET), phase transition-based Mott-FET, mechanical switching-based nano-electro-mechanical switch (NEMS), ionization-MOS (IMOS), and negative gate capacitance transistor (NCFET) have been explored for replacing the conventional MOSFET [15-17].

The work in this thesis comprehends the TFET for enhanced performance in terms of high switching analog, RF, and linearity figure of merits (FOMs) to replace the conventional MOSFET for future CMOS technologies. The TFETs are considered as a potential candidate to deal with issues related to MOSFETs due to the fundamental technique of current switching, which makes a TFET more efficient than MOSFET. The band-to-band tunnelling (BTBT) in TFET led to exhibit smaller SS than MOSFET with a lower supply voltage. Here the majority carriers are injected into the channel from the source side by the alignment of conduction band and valence band at the source to channel junction leading to band overlapping. Hence, tunnelling probability of the carriers through the barrier is enhanced [14]. Therefore, the fundamental thermal limit of SS being approximately 60 mV/decade

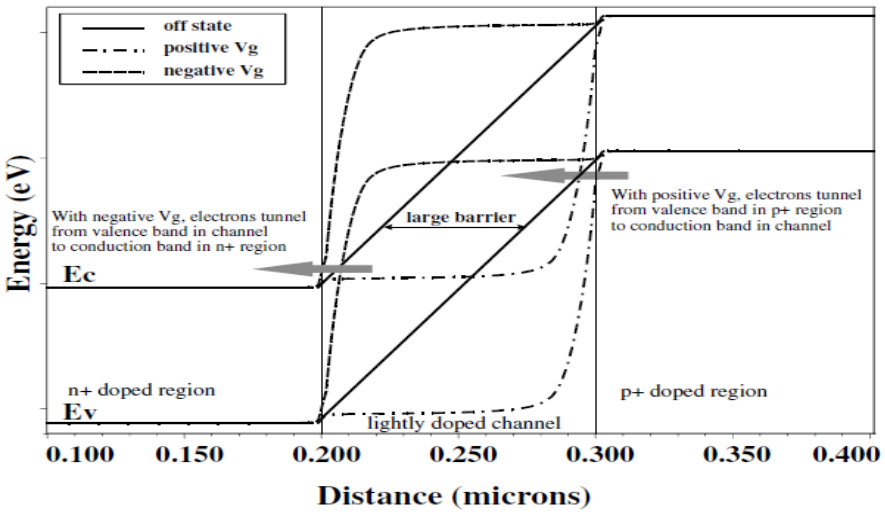
has been uplifted by using TFET as low as 20 mV/decade [18-21]. This thesis portrays the TFET as a suitable candidate for superior analog/RF, low power and high switching wireless applications.

1.2 TUNNEL FIELD EFFECT TRANSISTOR (TFET)

1.2.1 OPERATING PRINCIPLE



(a)



(b)

Fig. 1.1 (a) schematic structure of n-TFET and (b) energy band diagram of n-TFET in ON, OFF and ambipolar state [22].

The TFET is a metal gated reverse biased p-i-n structure having the metal gate deposited over the entire intrinsic channel region [22]. The prime difference between the MOSFET and TFET structure is the doping of the source and drain regions. The source and drain of TFET have asymmetric doping unlike MOSFET. The basic device structure of n-TFET is displayed in **Fig. 1.1(a).** The n-TFET and p-TFET is determined by the dominant carriers flowing in the channel region below the gate electrode in the ON state. The dominant carriers are electrons in n-TFET and holes in p-TFET, respectively. For an n(p)-TFET, the doping of the source is $p^+(n^+)$ and doping of the drain is $n^+(p^+)$. The fundamental mechanism of dominant carriers' injection is the Quantum Mechanical BTBT in TFET. On the application of gate voltage, the band bending at the source to channel interface (S/C) leads to BTBT across the potential barrier and hence tunnelling current flows. **Fig. 1.1(b)** illustrates the energy band diagram of n-TFET in the ON, OFF, and ambipolar state.

i. When $V_{gs} = 0$ V, the TFET is in the OFF state. The conduction band (CB) of the channel and the valence band (VB) of the source are far apart in such a way that the potential barrier at the S/C interface is quite large. Therefore, the BTBT is inhibited and hence very low subthreshold leakage current flows in the device.

ii. When $V_{gs} > 0$ V, the carrier density below the gate gets modulated by the gate voltage and hence this drags down the CB in the channel region and overlaps with the VB of the source region. Due to this band bending at the S/C interface, the width of the potential barrier reduces and hence BTBT from the VB of source to CB of channel is inhibited. Hence the tunneling current flows in the device.

iii. When $V_{gs} < 0$ V, an inverted p-channel is formed below the gate. The energy bands of the channel region are lifted upward and hence there is an overlapping of the channel VB and drain CB. Furthermore, the potential barrier width starts decreasing at the channel to drain (C/D) interface and hence the electrons start tunneling form the VB of channel to CB of drain. This leads to the ambipolar conduction of TFET (**Fig. 1.1b**).

1.2.2 MERITS AND CHALLENGES OF TFET

The scaling down of channel length to sub-nanometer regime in MOSFET gives rise to major issues of SCEs, which has been overcome by the quantum tunnelling of carriers across the S/C interface in TFET. There is a major scope of further downscaling in TFET because of its BTBT mechanism instead of drift-diffusion of carriers in MOSFET. Therefore, TFET is somehow immune to the temperature variation and hence can work in larger range of temperature [23]. Due to the advantage of lower SS than MOSFET, TFET can be operated at a lower supply voltage. Which in turn leads to lower static and dynamic power dissipation [24]. Since the tunnelling barrier width at the S/C interface is controlled by the gate voltage, therefore tunnelling of carriers at lower gate voltage is inhibited. Thus, only a minor current~10^{-15}A can flow leading to lower leakage as compared to MOSFET. This can significantly reduce the static power dissipation (proportional to supply voltage and leakage current).

Despite of these benefits, TFET suffers from various issues like inferior ON current (I_{ON}) and ambipolar conduction. The lower I_{ON} results in lower operational speed and higher threshold voltage (V_{th}). Many engineering techniques have been reported in the literature for improving the electron tunnelling rate across the S/C interface thereby overcoming the challenges of lower I_{ON} and higher V_{th} of TFET. Another challenge faced by TFET is the ambipolar conduction – conducting for both positive and negative gate voltage at the same supply voltage. It constitutes tunnelling at the S/C junction for positive gate bias and tunnelling at C/D junction for negative gate bias [25]. It is highly undesirable in logic devices like inverters which demands for perfect levels of OFF and ON states (unipolar conduction) [25].

1.2.3 ENGINEERING TECHNIQUES FOR OVERCOMING CHALLENGES FACED BY TFET

1.2.3.1 HETERO-STRUCTURE TFET OR BANDGAP ENGINEERED TFET

It comprises of utilising different source and channel materials to enhance the I_{ON}. It is termed as bandgap engineering because two materials with different bandgaps are used in the source and channel regions. The lower energy bandgap material is used in the source region and higher energy bandgap material in the channel region. Due to the lower bandgap source region, the width of potential barrier at the S/C interface is reduced and hence the electron tunnelling probability increases. This leads to higher I_{ON} [26-28].

1.2.3.2 JUNCTIONLESS TFET

In order to combine the benefits of TFET (low SS) and JLFET (high I_{ON}), proposal of a new architecture has been addressed named JLTFET, junctionless tunnel FET. JLTFET is a uniformly doped TFET which works on the principle of charge plasma [29-30].

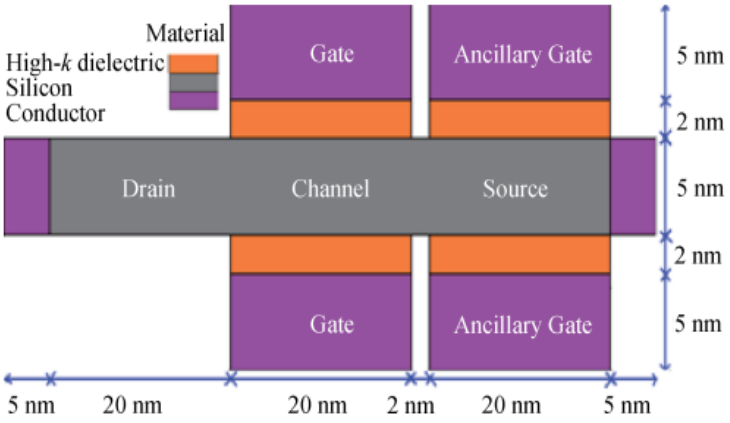


Fig. 1.2 schematic structure of junctionless TFET [29].

The basic idea of charge plasma concept is to convert a highly doped $n^+ - n^+ - n^+$ substrate into the conventional $p^+ - i - n^+$substrate with the use of an auxiliary-gate over the source region and a control gate over the channel region having different work functions as shown in **Fig. 1.2** [29-31]. As there are no metallurgical junctions, so it makes the fabrication process very easy and less expensive. It provides better switching performance and better analog behaviour as compared to conventional TFET.

1.2.3.3 III-V COMPOUND SEMICONDUCTING MATERIAL BASED TFET

III-V materials have potential of high-speed switching when transistors behave as switches in logic operations. It has advantage of high mobility and flexibility over huge range of bandgaps so that optimizations of I_{ON}, I_{ON}/I_{OFF}, and SS are easy [32-33]. In **Fig. 1.3** the InAs/$GaAs_{0.1}Sb_{0.9}$ hetero-structure is used at the source–channel interface, which improves the BTBT current through the hetero-structure of InAs/$GaAs_{0.1}Sb_{0.9}$ and a polarization electric field at the arsenic heterojunction is induced by the lattice mismatch in the arsenic alloy zinc blende crystal [32].

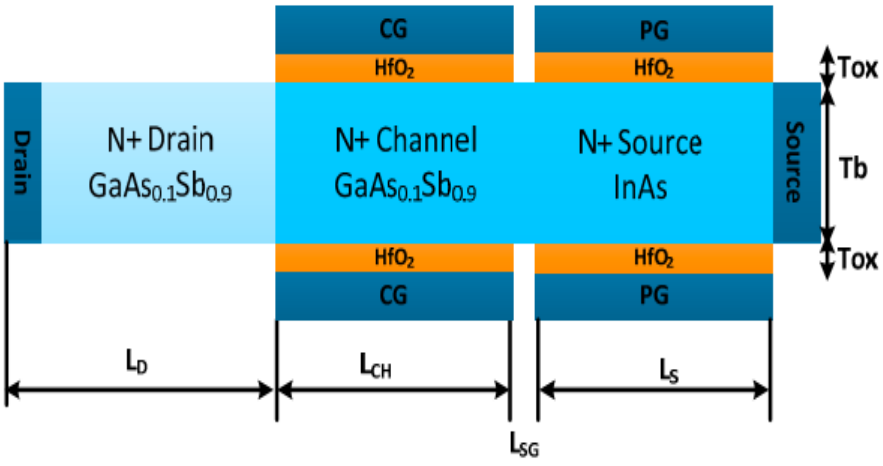


Fig. 1.3 Schematic structure of InAs/GaAsSb based TFET [32].

1.2.3.4 DUAL MATERIAL GATE (DMG) TUNNEL FET

Fig. 1. illustrates the cross-sectional view of the dual material gate tunnel FET, where the main gate is divided into two gates: the tunnelling gate and the auxiliary gate having materials of two different work functions [34]. The work functions of the two gates are optimized to obtain the best electrical characteristics of the device.

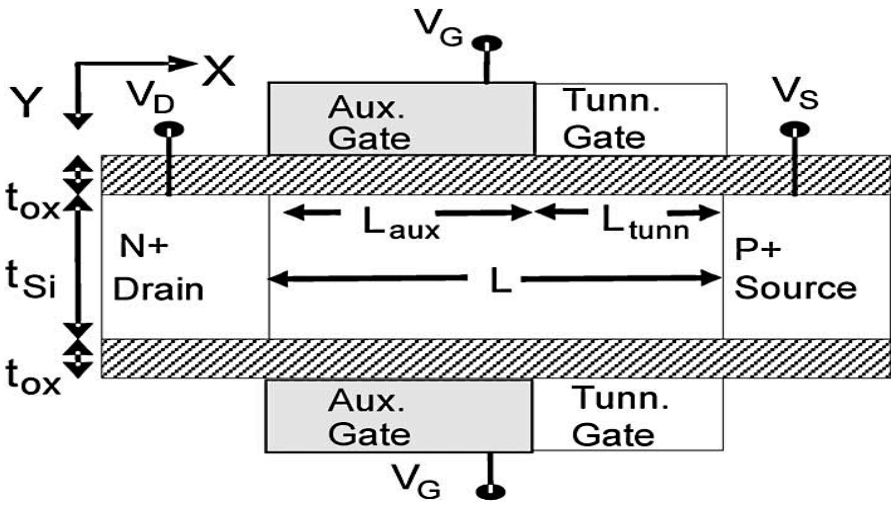


Fig. 1.4 Cross-sectional view of a DMG-DGTFET [34].

The results show that the DMG technique can be applied to TFETs with different channel materials, channel lengths, gate-oxide materials, gate-oxide thicknesses, and power supply levels to achieve significant gains in the overall device characteristics. The dual material gate technology used here provides higher I_{ON}, I_{ON}/I_{OFF}, and smaller SS [35].

1.2.3.5 HETERO-GATE DIELECTRIC TUNNEL FET

To suppress the unwanted conduction in TFET i.e., the ambipolar current, combination of hetero gate dielectrics is used (**Fig. 1.5**). It also enhances the I_{ON} and lower the SS of the device. The low-k dielectric is placed towards the drain side which suppresses the ambipolar conduction, while the high-k dielectric used towards the source region induces a local minimum of the conduction band at the

source/channel junction. Hence the tunnelling barrier width decreases by enhancing the I_{ON} and SS is also reduced to a great extent [36-38].

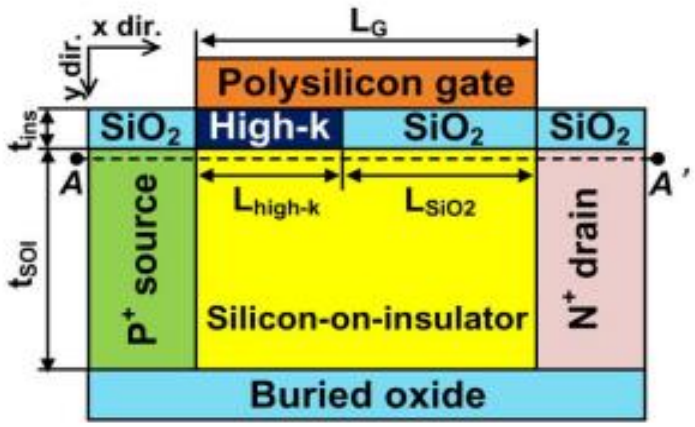


Fig. 1.5 3-D cross-sectional view of HD-TFET [36].

1.3 RESEARCH GAPS

- TFET has been proposed as an alternative to the CMOS transistors due to its lower SS and lower I_{OFF}. But one of the major issues faced by TFET is its I_{ON} than that of CMOS transistors according to the requirement set in the International Roadmap for Semiconductor. The major obstacle in the TFET performance is the lower tunnelling current, which is mainly attributed to the BTBT of the electrons from the VB of the source region to the CB of the channel region.
- The primary issue faced by TFET is the ambipolar conduction, which is the conduction in two directions or switching the device in reverse bias state also. The ambipolar current can lead to a higher OFF-state current in a TFET and instability for digital switching applications.
- Unlike conventional MOSFETs, TFETs are more immune to SCEs due to their basic mechanism of quantum-mechanical BTBT rather than thermal emission. However, as

TFETs are scaled down, fabricating the doping junctions becomes very difficult and expensive [39].

- Dual Material Gate engineering has been used in many research papers. Research work presented by Bal, Punyasloka, et al. showing the dual material gate engineering on a double gate junctionless TFET influences the V_{th} and I_{OFF} by creating an energy band minimum at the conduction band of the channel [40]. The substrate used was Si. An analysis of dual material gate engineering is also needed for junctionless TFET based on compound semiconducting materials.
- Designing the TFET structure using high-k dielectric improves the control of the gate over the channel. But when compound semiconducting materials are used in combination with Si or alone, the problem of absence of native oxides occurs [41]. Also, the problem of lattice mismatch arises when we put high-k dielectric in contact with III-V compound semiconducting materials. It can lead to defects at the dielectric/semiconductor interface [31]. These defects originate the interface trap charges (ITCs) and oxide charges, which are responsible for the alteration of ideal device characteristics. Hence, it is necessary to study the device reliability in the presence of these traps.
- Numerous studies have explored the impact of control gate and polar gate on the retention of hole and electron charge plasma to induce the source and channel region polarity in junctionless tunnel field effect transistor (JLTFET). However, along with polar gate (PG) the choice of source electrode metal (SEM) work function is also responsible for the retention of hole plasma in the p^+ prompted source. A comprehensive investigation of the mutual significance of PG and SEM work function on p^+ prompted source is required to study key characteristics of JLTFET, which is unexplored in the literature otherwise.

1.4 RESEARCH OBJECTIVES OF THESIS

- To analyse the JLTFET configuration using the charge plasma concept in order to reduce the doping junction fabrication complexity and cost and compare it with the conventional TFET for I_{ON}, I_{OFF}, SS and other electrical device parameters.
- To analyse the electrical characteristics of JLTFET using III-V compound semiconducting materials (binary and ternary) to uproots the major obstructions of lower I_{ON} and ambipolar conduction of TFET. The direct bandgap nature and band tunability of these materials is feasible for bandgap engineering (BGE) in comparison to the conventional indirect bandgap silicon material which has larger energy band gap so leads to lower tunnelling current. Therefore, hetero-material H-JLTFET with III-V compound semiconducting material having lower energy bandgap can be used as the source material, whereas channel and drain can be attained with a higher energy band gap material to enhance the analog/Radio Frequency (RF) performance metrics.
- To examine the device performance for different gate metal work functions for dual metal gate (DMG) engineering and then optimize the dual metal gate combinations in terms of a lower work function tunnel gate (TG) and a higher work function supplementary gate (SG) for optimum I_{ON}, I_{OFF}, current switching ratio (I_{ON}/ I_{OFF}), switching speed and high frequency analysis of DMG-HJLTFET.
- To investigate the impact of TG process variations on the viability and applicability of DMG-HJLTFET at RF and microwave frequencies (regarding various power gains and RF FOMs) and linearity and intermodulation distortion parameters for modern high frequency wireless communication systems.
- To study the electrical and analog characteristics of HJLTFET for different high-k gate dielectrics and then developing a heterogeneous gate dielectric (HD) stack (for HD

engineering) having an amalgamation of high-k and low-k dielectric material for optimum device (HD-HJLTFET) performance.

- To examine the impact of interface trap charges (ITCs) polarity and density on the device reliability by incorporating the donor (positively charged) and acceptor (negatively charged) interface traps.
- To investigate the influence of different source electrode metal (SEM) work functions in the formation of Schottky and ohmic contacts by including the most important (Universal Schottky Tunneling) UST model in simulation of HJLTFET. The inclusion of various underrated physical effects of HJLTFET in regards to ohmic and Schottky contacts may put the research of junctionless devices in the right direction owing to the hole plasma depletion consideration at the SEM/p^+ prompted Source interface, which has been overlooked before.

1.5 THESIS OVERVIEW

This thesis is organised into 7 chapters to accommodate all the research objectives. Each chapter is organised to be fully self-contained. The references to each chapter are listed at the end of the respective chapter.

Chapter 1 explains the drawbacks of MOSFET and the requirement of new operational mechanism-based device – TFET to overcome these drawbacks of MOSFETs. The chapter presents the comparison of both devices and challenges faced by TFET regarding lower I_{ON} and ambipolar conduction. Various engineering techniques related to material and device design such as heterostructure or bandgap engineered TFET, junctionless TFET, dual material gate TFET, heterogeneous gate dielectric TFET, III-V compound semiconducting material based TFET available

in the literature are also discussed to overcome the challenges of TFET. Further, various research gaps present in the literature are mentioned followed by the research objectives of the thesis. Last of all, the importance of the research work presented in this thesis has been discussed along with the overall thesis organisation.

Chapter 2 illustrates the structural design of the proposed device along with the device design parameters and materials parameters used in the simulation. Thereafter, the simulation models used in this work are enlisted along with the calibration of these models with fabrication based experimental data extracted from the literature. For the fabrication feasibility of the proposed device the step-by-step fabrication process flow has been presented. Further, the chapter describes the comparison of a dual material gate engineered-heteromaterial based junctionless TFET (DMG-HJLTFET) with single metal gate-heteromaterial based junctionless TFET (SMG-HJLTFET) and conventional silicon material-based Si-JLTFET for analog/RF, linearity, and intermodulation distortion performance. Moreover, the impact of tunnel gate process variations - length and work function on the DMG-HJLTFET performance has been investigated [42]-[43].

Chapter 3 examines the importance of heterogeneous gate dielectric engineering in SMG-HJLTFET (proposed in chapter 2) by replacing the conventional low-k oxide material (mono-dielectric) with a hetero-dielectric stack having the high-k dielectric material towards the source side and low-k dielectric material towards the drain side under the control gate. The performance of HD-HJLTFET has been compared with mono-dielectric high-k HJLTFET and low-k HJLTFET. The selection of an appropriate high-k oxide for the hetero dielectric and length of the high-k oxide in HD-HJLTFET has been optimized using different dielectric materials - HfO_2 (k = 25), ZrO_2 (k = 22), Al_2O_3 (k = 9), Si_3N_4 (k = 7), and SiO_2 (k = 3.9) in the high-k region. This study indicated the HD-HJLTFET to be an alternate to conventional mono-dielectric devices for high switching applications [44].

Chapter 4 investigates the optimization and performance of arsenide/antimonide tunable bandgap tunnelling interfaced H-JLTFET by replacing the binary channel material (GaAs) with ternary (AlGaSb) compound semiconducting material. The suitability of lattice matched standard III-V growth and processing techniques are the prime reason for selecting these materials. The material is chosen because of the tunable bandgap property, where the bandgap of AlGaSb can be modified by changing the mole fraction of Al to induce a charge plasma based tunable bandgap arsenide/antimonide tunneling source/channel (S/C) interface. The Al mole fraction of AlGaSb is optimized to get the superior result characteristics of H-JLTFET. The superior performance is attributed to the conduction band local minima induced at the channel yielding to narrower tunneling barrier width at an optimized Al-mole fraction (0.15) of AlGaSb. Various analog and RF FOMs such as I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, SS, transconductance, cut off frequency, device efficiency, parasitic capacitances have been analysed and compared with Si-JLTFET [45]-[46].

Chapter 5 investigates the reliability issues of HD-HJLTFET. The interface trap charges (ITCs) at the semiconductor/oxide interface originating during the fabrication process of electronic device plays an important role in reliability issues. In this chapter, the impact of semiconductor/oxide ITCs density and polarity – positive ITCs (donor) and negative ITCs (acceptor) has been examined for analog/RF FOMs. Since, HD-HJLTFET is based on hetero-material arsenide/antimonide tunneling interface so the impact of semiconductor/semiconductor ITCs has also been discussed. Various linearity and intermodulation distortion parameters of HD-HJLTFET such as g_{m2}, g_{m3}, VIP2, VIP3, IIP3, 1dB compression point, and IMD3 showed marked improvement with negligible variation against different ITC polarity than its counter device HJLTFET, making it more reliable for low power microwave and distortion-free wireless communication systems.

Chapter 6 features a comprehensive investigation of the mutual significance of polar gate (PG) and source electrode metal (SEM) work function on the retention of hole plasma in the p^+ prompted source to study the key analog characteristics of arsenide/antimonide tunneling interfaced hetero-material

JLTFET (HJLTFET), which is unexplored in the literature otherwise. Three metals – W (4.55 eV), Mo (4.65 eV), and Pd (5.3 eV) have been considered for simulation of HJLTFET. For SEM work function lesser than p^+ prompted source (W and Mo), the depletion of hole plasma near SEM/S interface results in immediate current inhibition at S/C interface caused by an undesired movement of electrons en route to the Schottky interface. The Schottky tunneling phenomenon is considered by implementing the Universal Schottky Tunneling model to study the underestimated drain current of HJLTFET. However, the Universal Schottky Tunneling model becomes inconsequential for source electrode metal work function higher than p^+ prompted source (Pd) as hole plasma is preserved by the ohmic contact formation [47].

Chapter 7 briefly summarises the research work of the thesis and discusses the future scope of the present work.

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CHAPTER-2

IMPACT OF TUNNEL GATE PROCESS VARIATIONS ON ANALOG/RF, LINEARITY, AND INTERMODULATION DISTORTION ANALYSIS OF HETERO-MATERIAL TUNNELING INTERFACED CHARGE PLASMA JUNCTIONLESS TFET.

This chapter represents a dual metal gate, hetero-material tunneling interfaced junction-less TFET, (DMG-HJLTFET), utilizing III-V compound semiconducting materials, InAs (low band-gap source material)/GaAs (higher band-gap channel and drain material) by applying the band-gap and dual material gate engineering. The 2-D TCAD simulations have been executed to explore the impact of Tunnel gate process variations - work function and length on DC and analog figure of merits (FOMs) of DMG-HJLTFET. The extracted result parameters have also been compared to SMG-HJLTFET and conventional Si-JLTFET. The DMG-HJLTFET attains improved ON current in the range of 88.5 $\times 10^{-6}$ A/μm and OFF current remains as low as 2.89 $\times 10^{-16}$ A/μm. It exhibits a high current switching ratio of 3.1 $\times 10^{11}$ as compared to SMG-HJLTFET (I_{ON} = 24 $\times 10^{-6}$ A/μm and I_{ON}/I_{OFF} = 1.4 $\times 10^{11}$) and Si-JLTFET (I_{ON} = 7 $\times 10^{-6}$ A/μm and I_{ON}/I_{OFF} = 1.8 $\times 10^{6}$). Further, the radio frequency/microwave (RF) parameters such as power gains (h_{12}, UPG, and Gma), f_{max}, and GBP have been compared for all three aforementioned devices. Moreover, the small signal admittance (Y) parameters have been examined to explore the possible scope of DMG-HJLTFET for future internet of everything communications and fast switching applications.

2.1 INTRODUCTION

Tunnel field effect transistors (TFETs) have attracted considerable interest in being energy-efficient devices and have been used in low power applications as compared to MOSFETs because of low leakage current along with steeper sub-threshold slope (SS). The SS of conventional MOSFETs is limited to a value greater than 60 mV/decade at 300 K. The performance degradation of MOSFET is due to its fundamental mechanism of thermionic emission of the carriers over the potential barrier, whereas TFET works on the principle of quantum tunneling of carriers through the potential barrier [1]-[3]. MOSFET suffers from various unwanted issues like SCEs, high leakage current, DIBL, and SS > 60 mv/decade [4]-[6]. TFET is immune to these severe issues except the problem of low ON-current (I_{ON}) [7]-[8], ambipolar conduction, and inadequate high-frequency response [9]. However, lower value of I_{ON} is an eminent issue, which need to be resolved along with keeping its leakage current and SS unelevated. The prime reason for low I_{ON} is the large bandgap of Si (~ 1.1 eV) [10]-[11], which brings on an inadequate quantum band-to-band tunneling through the barrier. This hitch can be solved by employing low bandgap semiconducting materials or III-V compound semiconducting materials like $InAs, GaAs, InP, SiGe$ [12]-[16], however, it becomes challenging to use III-V compound semiconducting materials for making selective oxide formation due to the problem of lattice incongruity.

In the downscaling approach, fabrication of doping junctions in TFETs becomes a tedious, and expensive task. One of the alternative devices proposed in past few years is JLFET based on the principle of Lilienfeld's architecture of first transistor [17]. Owing to the absence of doping junction, it makes the fabrication process very smooth and effortless. TFET constitutes efficient electrical parameters than MOSFET, however, suffers from the problem of large SS just like MOSFET [18]-[20]. Recently many research papers have addressed the proposal of a new architecture named junctionless tunnel field effect transistor (JLTFET), which consolidates the benefits of a JLFET

(elevated I_{ON}) and a TFET (low SS) [21]. A JLTFET is a uniformly doped junction-less TFET, whose fundamental mechanism of carrier polarity induction is charge plasma. The basic idea of charge plasma concept is to convert a highly doped $n^+ - n^+ - n^+$ substrate into the conventional $p^+ - i - n^+$substrate by using two different work function gates as the polar gate (PG) and a control gate (CG) [11], [16]. By using charge plasma concept, the involuted fabrication processes, arbitrary doping fluctuations, and scalability issues can be reduced adequately.

This chapter presents a novel amalgamation of III-V compound semiconducting materials, InAs (lower bandgap, [22]) and GaAs (higher bandgap, [14]) as the source and channel materials in a hetero-material tunnelling interfaced single metal gate (SMG) junctionless device (SMG-HJLTFET). The prime reason of using an amalgamation of InAs and GaAs is the larger energy bandgap and higher carrier mobility obtained at the source/channel (S/C) interface of the hetero-material structure in comparison to Si-JLTFET, which represents the homo-material based JLTFET device. The energy bandgap of InAs and GaAs is 0.35 eV and 1.42 eV, respectively [23]. The material properties of InAs and GaAs employed in present simulation framework are displayed in **Table 2.1**.

Table 2.1

Material properties of InAs and GaAs used in present simulation [22, 23].

Material parameters	InAs	GaAs
Relative permittivity	14.6	13.2
Energy Bandgap (eV)	0.35	1.42
Electron mobility (cm^2/Vs)	$\leq 4 \times 10^4$	1200
Hole mobility (cm^2/Vs)	$\leq 5 \times 10^2$	61
Electron affinity (eV)	4.9	4.07

Furthermore, in order to enhance the result characteristics of SMG-HJLTFET, the dual material gate (DMG) engineering is incorporated by dividing the CG of SMG-HJLTFET into a tunnel gate (TG) and a supplementary gate (SG). The prime utility of TG is to improve the excavation of the carriers

at the S/C interface; accordingly, the position of TG is optimized towards the S/C interface. The SG is used to increase the barrier height by placing it towards the channel/drain (DC) interface. The TG and SG work-functions are optimized to embellish the DC, analog/RF, and linearity characteristics of the device. Before applying the DMG, SMG-HJLTFET device has been proposed using the same materials and dimensions. Then DMG has been introduced to study the effect of dual metal work functions on the device performance metrics. The improvement of the result characteristics is also examined against Conventional Si-JLTFET (homo-material).

2.2 DEVICE STRUCTURE

This chapter is based on an n-type DMG-HJLTFET presented in **Fig. 2.1**.

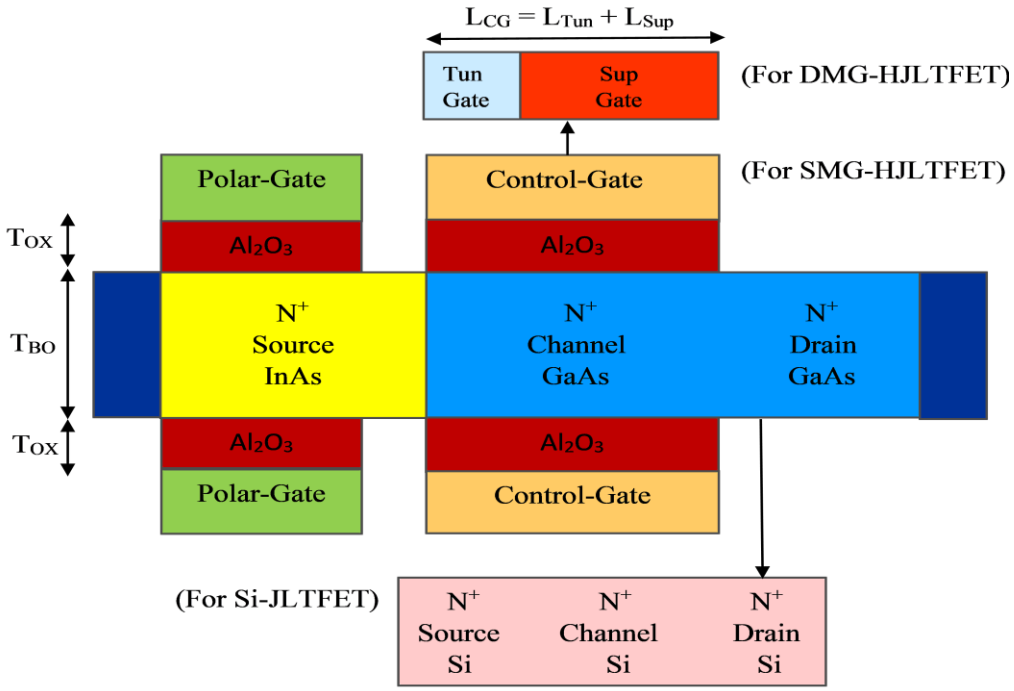


Fig. 2.1. Device schematic structure of Si-JLTFET, SMG-HJLTFET, and DMG-HJLTFET [24].

Table 2.2

Device Design Parameters [24]

Parameters	Si JLTFET	SMG HJLTFET	DMG HJLTFET	Units
Gate length (L_{CH})	20	20	20	nm
Oxide thickness (T_{OX})	2	2	2	nm
Isolation thickness (T_{ISO})	2	2	2	nm
Body thickness (T_{BO})	3	3	3	nm
Polar gate length (L_{PG})	15	15	15	nm
control gate length (L_{CG})	20	20	20	nm
PG Work function (ϕ_{PG})	5.93	5.93	5.93	eV
CG Work function (ϕ_{CG})	4.3	4.5	-	eV
TG Work function (ϕ_{tun})	-	-	4.1	eV
SG Work function (ϕ_{Sup})	-	-	4.5	eV

The proposed device DMG-HJLTFET has also been compared with SMG-HJLTFET and Si-JLTFET having the same parameters as shown in **Table 2.2**. A double gate technology has been used to increase the gate controllability over the channel. Two isolated gates - PG and CG with different work functions are employed in SMG-HJLTFET and Si-JLTFET, to achieve the required carrier concentration in the source and channel region, respectively. The drain region is reserved at the same doping concentration. The PG is utilized to induce p^+ source region and CG is used to make the channel intrinsic. Further, a dual material technique is used in CG, where the overall CG length ($L_{CG} = L_{tun} + L_{sup}$), is distributed into TG (L_{tun} = 4nm) and SG (L_{sup} = 16nm). The ON state corresponds to V_{GS} = 1.5V, V_{DS} = 1.5V and OFF state corresponds to V_{GS} = 0.0V, V_{DS} = 1.5V.

2.3 SIMULATION METHODOLOGY

All the models are incorporated in the simulation setup using a TCAD simulator, Silvaco-ATLAS [23]. The dimensions of the proposed device have been considered within the range prescribed by the ITRS roadmap [25]. To employ the effects of electron tunneling from valence band of the source to conduction band of the channel at S/C interface, the non-local band-to-band tunneling (BTBT) model is applied. The quantum tunneling meshing is implemented in the tunneling region to administer the generation rate and tunneling rate of carriers at each mesh node of the S/C interface. In TFETs, the band-to-band tunneling current depends on the band edge profile at the S/C interface and has a strong impact on the potential and band energies at and near the junction. However, as a result of this strong coupling, the issues of convergence appear in some situations. In such cases other standard tunneling models can also be implemented along with non-local band-to-band tunneling model. To include the effect of traps between the top of the valence band and the bottom of the conduction band, a trap assisted tunneling model is applied. For simulation accuracy, the quantum confinement model given by Hansch [26] is also invoked. The bandgap narrowing model, the Shockley-Read-Hall recombination model, and the Auger recombination model are also enabled. The Fermi Dirac statistics is also invoked during the simulation. The CVT model (Lombardi) is also enabled to include concentration-dependent mobility, mobility due to parallel and perpendicular electric field and temperature. To perform all the mathematical carrier transport equations, the Gummel and Newton's numerical methods are implemented in the simulations.

2.4 CALIBRATION

As InAs/GaAs hetero-material combination has not been applied in TFET so far, the simulation models of proposed device are calibrated with the information extracted from a fabrication-based

research work [27], in order to authenticate the model parameters and the device measurements. The design parameters and biasing conditions of proposed device are considered exactly the same as that of the published results reported in [27], for the calibration purpose. **Fig. 2.2** illustrates the comparison of the I_dV_g characteristics obtained from the extracted data of the experimental work [27] and present simulations. It validates all the model parameters due to the close propinquity of the compared results.

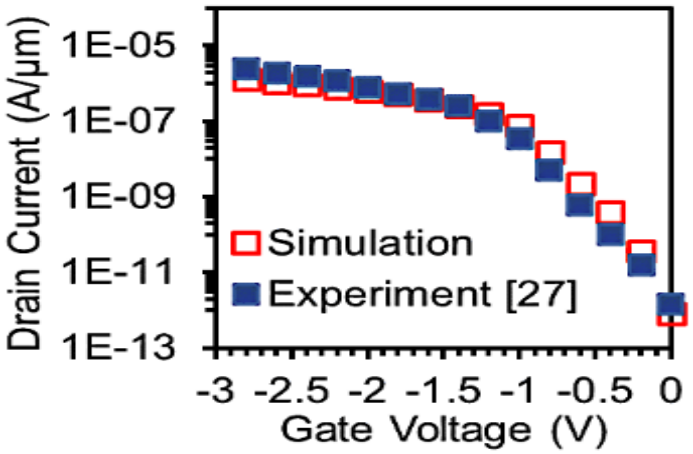


Fig. 2.2. Calibration plot for the comparison of experimental published results with simulation for transfer characteristics [24].

2.5 FABRICATION PROCESS FLOW OF DMG-HJLTFET

Fig. 2.3 illustrates the step-by-step fabrication process flow of the proposed device. The hetero-material source/channel interface is formed using the self-aligned optical lithography technique reported in [28]. Thereafter, the electron beam lithography and ultraviolet lithography are used to deposit the metal gates and spacer region [29-30]. Then, the dielectric layer is deposited using atomic layer deposition [31] and metal contacts are formed using electron beam evaporation [32]. Furthermore, the dual metal gate engineering (DMG) architecture can be implemented by two ways – the tilt angle evaporation technique [33] and metal interdiffusion process [34]. Thus, the DMG-

HJLTFET can be fabricated using the above device design outlines, in which the significance of hetero-material S/C interface and GME engineering scheme have been united with JLTFET for achieving improved characteristics.

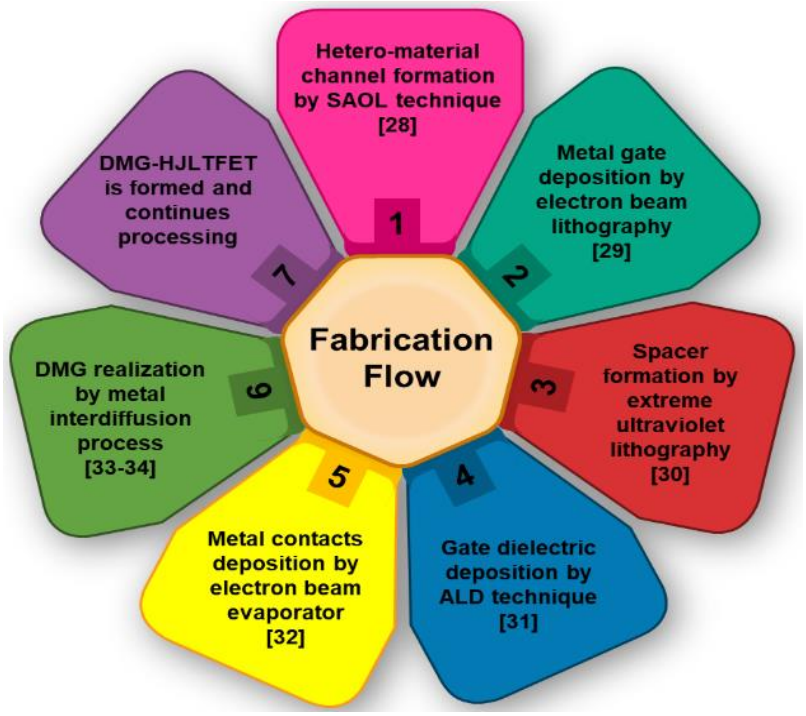


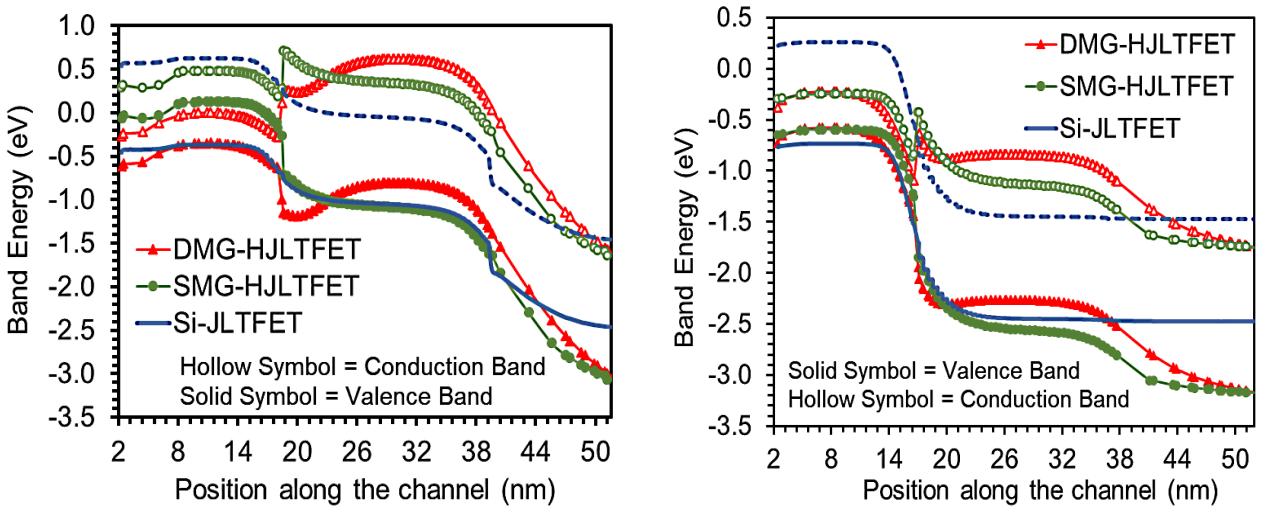
Fig. 2.3. Fabrication process flow of proposed DMG-HJLTFET [24].

2.6 RESULTS AND DISCUSSION

2.6.1 COMPARATIVE PERFORMANCE ANALYSIS OF BASIC DEVICE CHARACTERISTICS

This subsection presents the impact of InAs/GaAs hetero-material based S/C tunneling interface and the dual material gate application on the electrical characteristics of DMG-HJLTFET in the form of energy band diagram, carrier concentration, band-to-band electron tunneling rate, transfer characteristics and transconductance (g_m) and compared the same with SMG-HJLTFET and Si-

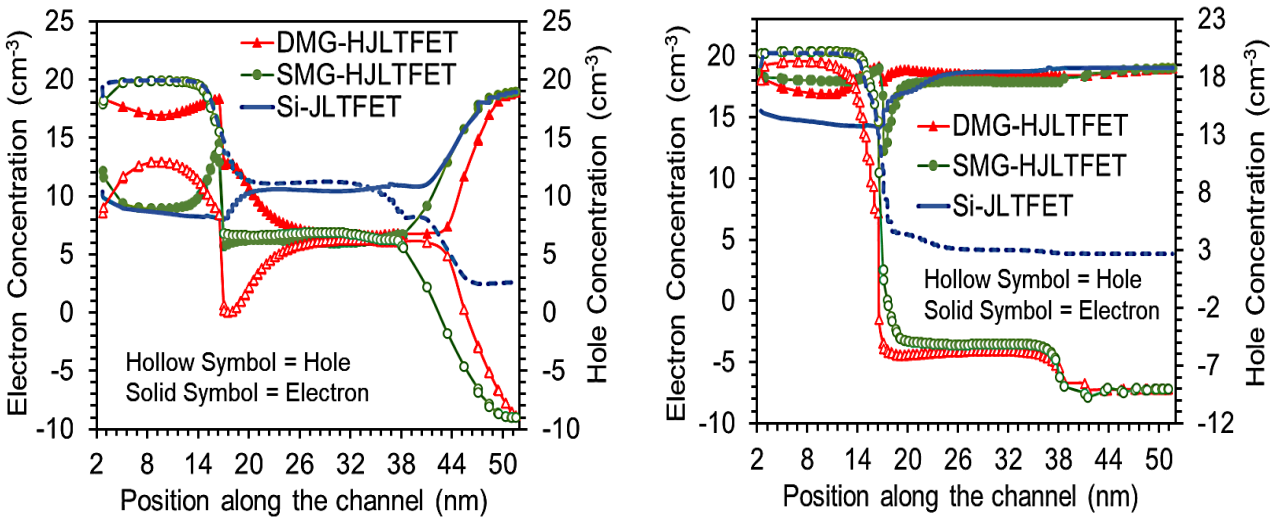
JLTFET devices. **Fig. 2.4(a)-(b)** represents the enhancement of DMG-HJLTFET characteristics over SMG-HJLTFET and Si-JLTFET in terms of energy diagram for the OFF and ON state, respectively at a depth of 1nm below the channel surface. The TG work function (ϕ_{tun}) is kept smaller than SG work function (ϕ_{sup}). When no gate bias is applied (OFF state), the conduction band of the channel is fetched up. The tunneling barrier thickness at the S/C boundary becomes much wider, thus prevents the overlapping of the bands. As an outcome, the electrons' tunneling probability from source to channel is negligible, which yields merely an inconsequential leakage current. Hence the BTBT rate is reduced, and the I_{ON}/I_{OFF} ratio is improved for DMG-HJLTFET in comparison with SMG-HJLTFET and Si-JLTFET. In the ON state, with the gradual increment in the gate voltage, the low band gap InAs source and ϕ_{tun} dragged down the conduction band to the left of the S/C boundary. The tunneling barrier becomes narrow and the electrons can easily excavate through the S/C interface, in DMG- HJLTFET. The I_{ON} surges exponentially with a fall in the tunneling barrier wideness. The high-k oxide material is accustomed to improve the I_{ON} parameter. However, Si-JLTFET leads to wider tunneling barrier due to its higher energy band gap and hence the I_{ON} degrades in comparison to the other two devices (**Fig. 2.4b**).



(a) (b)

Fig. 2.4. (a) OFF state and (b) ON state energy diagram along x-direction [24].

Fig. 2.5(a)-(b) represents the electron-hole concentration in the OFF and ON state for the three aforementioned devices at a depth of 1nm below the channel surface. By using appropriate CG and PG work functions (ϕ_{CG} and ϕ_{PG}) in the channel and source region, respectively, the device attains conventional $p^+ - i - n^+$ doped conformation without any physical doping (**Fig. 2.5a-b**).

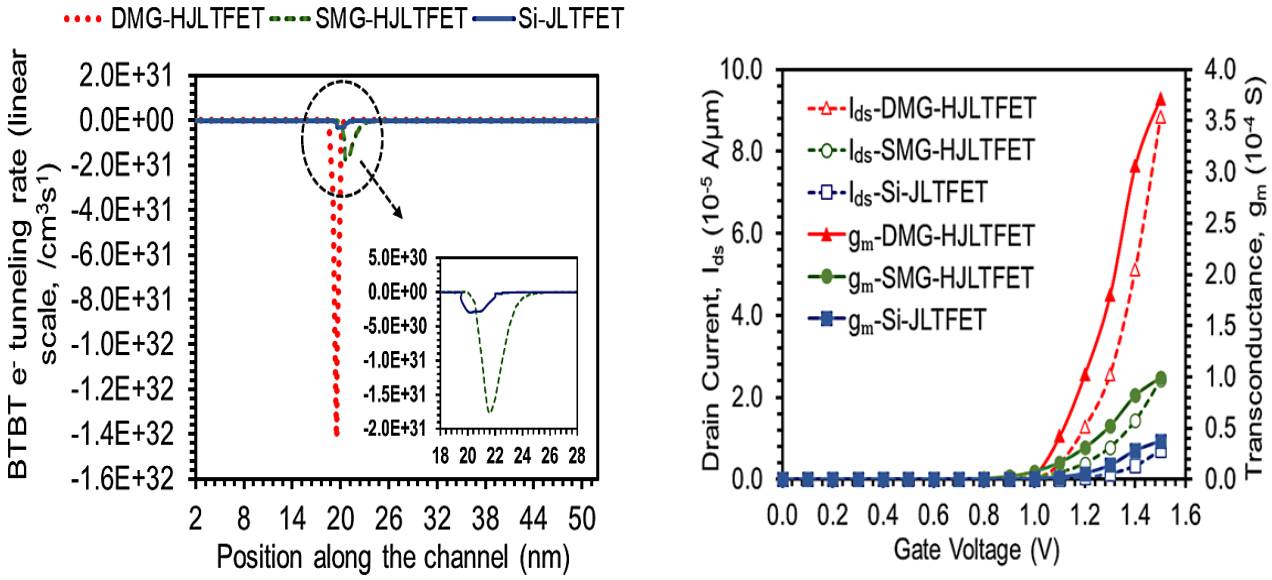


(a) (b)

Fig. 2.5. (a) OFF state and (b) ON state electron and hole concentration along x-direction [24].

The HJLTFETs being quantum mechanical devices, conduct the current through a different mechanism called band-to-band tunneling of carriers across the S/C interface, which is associated to the barrier thickness. **Fig. 2.6(a)** represents the BTBT electron tunneling rate alongside the channel direction, which depends upon the gate voltage and gate dielectric material as well. On the application of lower work function metal as TG, the excavation of charge carriers gets shifted towards the left of the interface. Thus, improves the I_{ON} of the device as compared to the other two. **Fig. 2.6(b)** indicates the deviation of drain current and g_m with gate voltage, which vindicates the prominent electrostatic reliability of DMG-HJLTFET over SMG-HJLTFET and Si-JLTFET. The g_m is an imperative factor

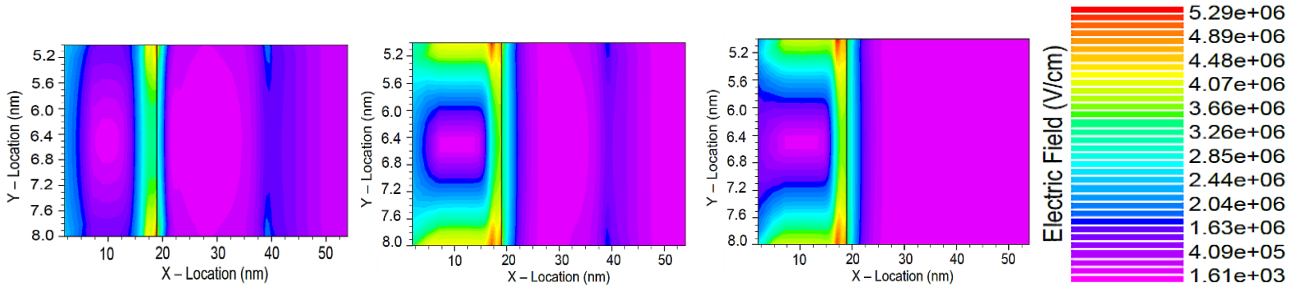
providing the gain of the device as a function of V_{GS} for analog circuit designs. In order to achieve high frequency and analog characteristics, the g_m should be upraised. In **Fig. 2.6(b)**, the g_m of DMG-HJLTFET is highest and Si-JLTFET has the least value of g_m among the three devices. In DMG-HJLTFET, the I_{ON} and hence the switching ratio, I_{ON}/I_{OFF} is also improved using the dual metal gate configuration, which is quite low SMG-HJLTFET and Si-JLTFET.



(a) (b)

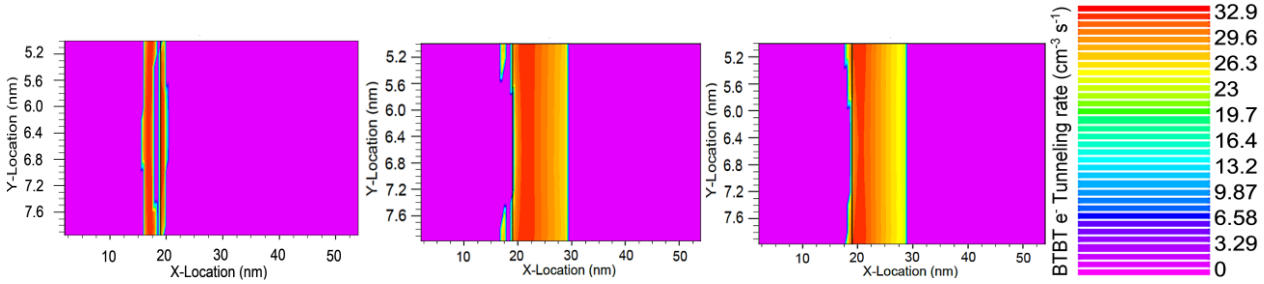
Fig. 2.6. (a) Electron tunneling rate alongside the channel and (b) Disparity of drain current and transconductance at $V_{GS} = 1.5\ V, V_{DS} = 1.5\ V$ [24].

Figs. 2.7-2.8 demonstrate the 2-D level curves of Si-JLTFET, SMG-HJLTFET, and DMG-HJLTFET, respectively, revealing the electric field and BTBT electron tunneling rate curves along the device length. In the ON state, the level curve of electric field varying along the body length specifies a positive extreme value at the S/C interface. **Fig. 2.8** displays the level curve of the BTBT electron tunneling rate along the device length. The electron tunneling gets shifted towards the left of the interface under the source to channel spacer region in case of DMG-HJLTFET due to the presence of lower ϕ_{tun}, giving rise to the tunneling current at the S/C interface.



(a) (b) (c)

Fig. 2.7. Level curve of electric field of (a) DMG-HJLTFET, (b) SMG-HJLTFET, and (c) Si-JLTFET along device length at $V_{GS} = 1.5\ V, V_{DS} = 1.5\ V$ [24].



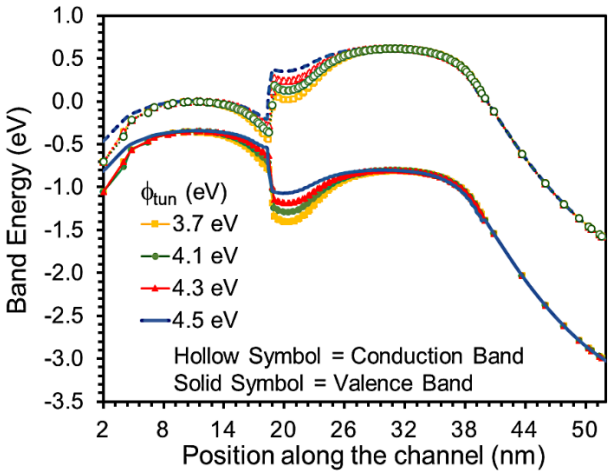
(a) (b) (c)

Fig. 2.8. Level curve of BTBT e^- tunneling rate of (a) DMG-HJLTFET, (b) SMG-HJLTFET, and (c) Si-JLTFET along device length at $V_{GS} = 1.5\ V, V_{DS} = 1.5\ V$ [24].

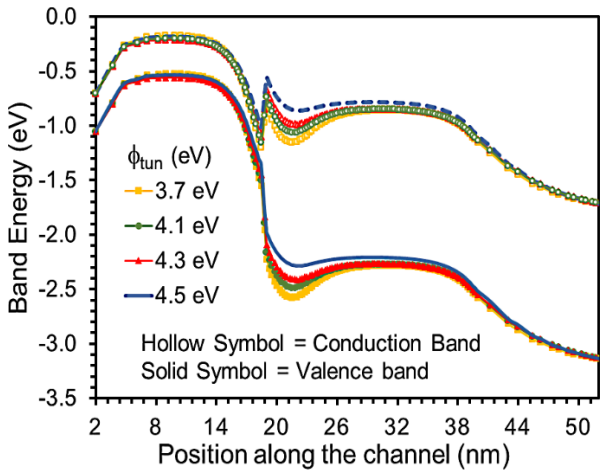
2.6.2 IMPACT OF ϕ_{TUN} VARIATION ON PERFORMANCE CHARACTERISTICS OF DMG-HJLTFET

This subsection describes the optimization and impact of ϕ_{tun} variation from 3.7 eV to 4.5 eV on DMG-HJLTFET performance. **Figs. 2.9(a-b)** expresses the relevance of ϕ_{tun} on the energy band profile of DMG-HJLTFET while the ϕ_{sup} is fixed to 4.5 eV. It represents the significance of ϕ_{tun}

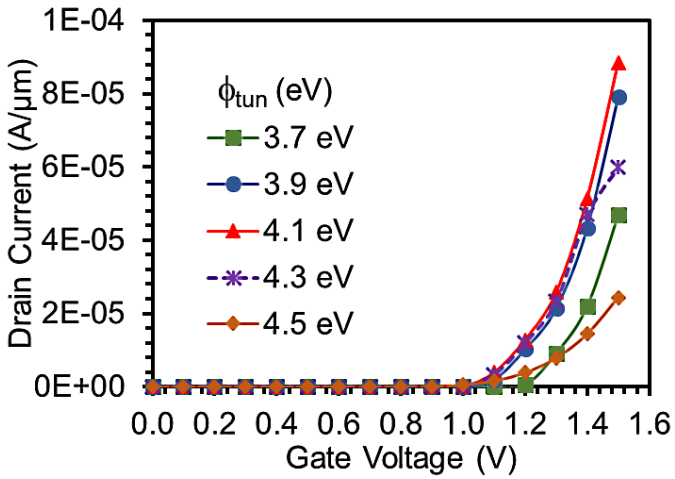
variation from 3.7 eV to 4.5 eV in the OFF-ON state, respectively. In the OFF-state on decreasing the ϕ_{tun} from 4.5 eV to 3.7 eV, there is an escalation in the tunnel barrier width at the S/C intersection.



(a)



(b)

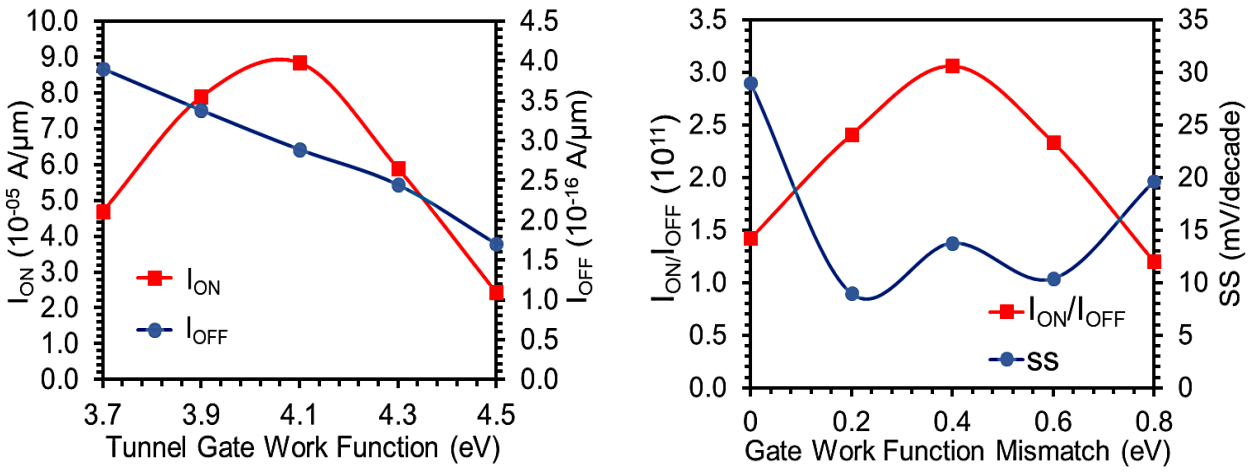


(c)

Fig. 2.9. (a) OFF state, (b) ON state energy diagram and (c) Transfer characteristics of DMG-HJLTFET for TG work function variation from 3.7 eV to 4.5 eV at $V_{GS} = 1.5\,V, V_{DS} = 1.5\,V$ [24].

Hence the significant overlapping between the conduction band/valence band of the channel/source regions declines. It diminishes the flow of charge carriers through the interface and hence the BTBT

rate is reduced. In the ON state, the decrement in ϕ_{tun} leads to band bending of conduction band/valence band of the channel/source regions at the S/C interface (**Fig. 2.9b**). The band bending shifts to the left of S/C interface, promoting higher tunneling rate due to the reduced tunneling barrier width. Hence, I_{ON} rises significantly. In **Fig. 2.9(c)**, the electrical transfer characteristics of DMG-HJLTFET are displayed by varying the ϕ_{tun} from 4.5 eV to 3.7 eV, keeping the ϕ_{sup} fixed at 4.5 eV. The maximum drain current is achieved for ϕ_{tun} = 4.1 eV, where the I_{ON} increases by 3.6 orders in magnitude than ϕ_{tun} = 4.1 eV and 1.8 orders in magnitude than ϕ_{tun} = 3.7 eV (**Fig. 2.9c**). The leakage current, I_{OFF} remains almost unaltered (2.89×10^{-16} A/μm to 1.72×10^{-16} for ϕ_{tun} = 4.1 eV to ϕ_{tun} = 4.5 eV).

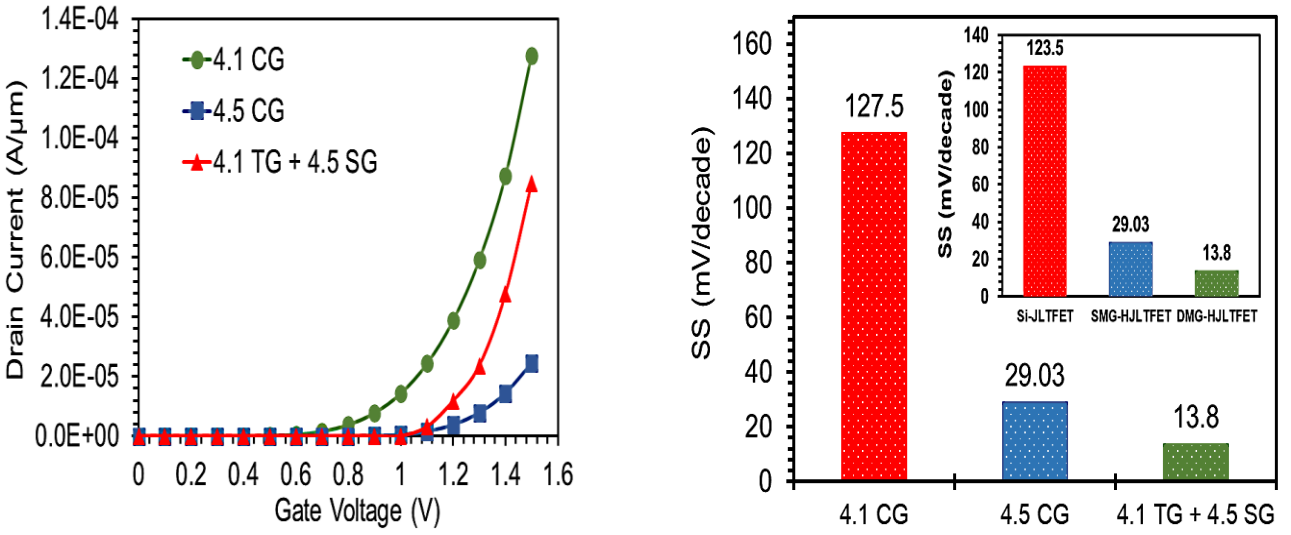


(a) (b)

Fig. 2.10. (a) ON current and current switching ratio (I_{ON}/I_{OFF}) with the tunnel gate work function (ϕ_{tun}) variation. (b) DMG-HJLTFET current switching ratio and SS variation with gate work function disparity [24].

Fig. 2.10(a) illustrates the I_{ON} and I_{OFF} by varying the ϕ_{tun} from 3.7 eV to 4.5 eV. The I_{ON} starts increasing as we vary the ϕ_{tun} from 3.7 eV and becomes maximum at 4.1 eV. On further varying the work function value up to 4.5 eV, the I_{ON} again decreases. The I_{OFF} decreases with the variation of

ϕ_{tun} (3.7 eV - 4.5 eV). The current switching ratio of DMG-HJLTFET is changing with respect to ϕ_{tun} disparity (3.7 eV - 4.5 eV, **Fig. 2.10b**). The simulated results reveal that when we increase the work function mismatch of the CG from 0 to 0.4 eV, the channel conduction band bends downwards and overlaps with the source valence band at the S/C interface. This leads to a higher I_{ON} and steeper SS. The further mismatch of the ϕ_{CG} leads to decrement in the current switching ratio. The optimized results are obtained at 0.4 eV work function difference. The I_{ON} of DMG-HJLTFET is about 3.6 orders higher in magnitude and the SS value is 52.4% less than SMG-HJLTFET and the I_{ON} is about 12.6 orders higher in magnitude and the SS value is 88.8% less than Si-JLTFET.



(a) (b)

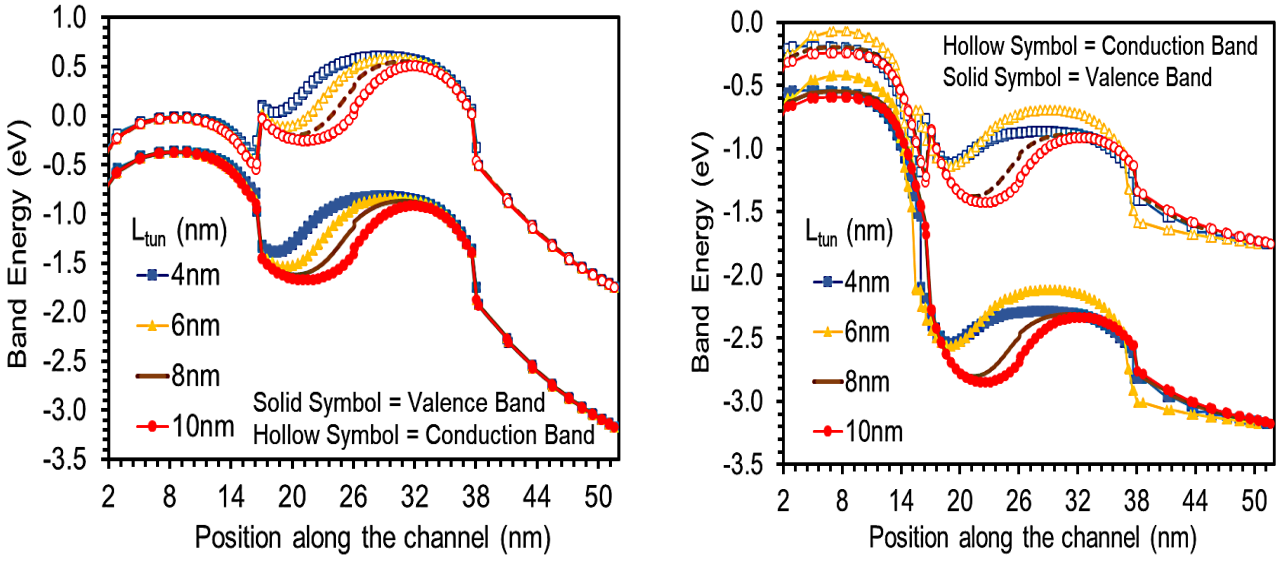
Fig. 2.11. (a) Transfer characteristics and (b) SS of DMG-HJLTFET (4.1 TG + 4.5 SG), SMG-HJLTFET (4.5 CG and 4.1 CG). (Inset) SS of three aforementioned devices [24].

Fig. 2.11(a) shows the transfer characteristics of single metal gate HJLTFET having ϕ_{CG} 4.1 eV, 4.5 eV and dual metal gate HJLTFET (CG is divided into TG and SG, (L_{CG} = L_{tun}, 4nm + L_{sup}, 16nm) having ϕ_{tun} = 4.1 eV and ϕ_{sup} = 4.5 eV. The I_{ON} for 4.1 CG-HJLTFET rises to 128 μA/μm and the I_{OFF} is 1.89×10^{-10} A/μm, so the I_{ON}/I_{OFF} is 6.7×10^{5}, which is very poor as compared to DMG-HJLTFET and SMG-HJLTFET (4.5 CG) as discussed earlier. The SS of DMG-HJLTFET- 4.1 TG + 4.5 SG

(13.8 mV/decade) is also smaller as compared to SMG-HJLTFET-4.5 CG (29.03 mV/decade) and SMG-HJLTFET-4.1 CG (123.5 mV/decade) as shown in **Fig. 2.11(b)**, reflecting its effectiveness in low leakage-improved performance application. The inset of **Fig. 2.11(b)** illustrates the comparison plot of SS of three devices.

2.6.3 IMPACT OF L_{TUN} VARIATION ON PERFORMANCE CHARACTERISTICS OF DMG-HJLTFET

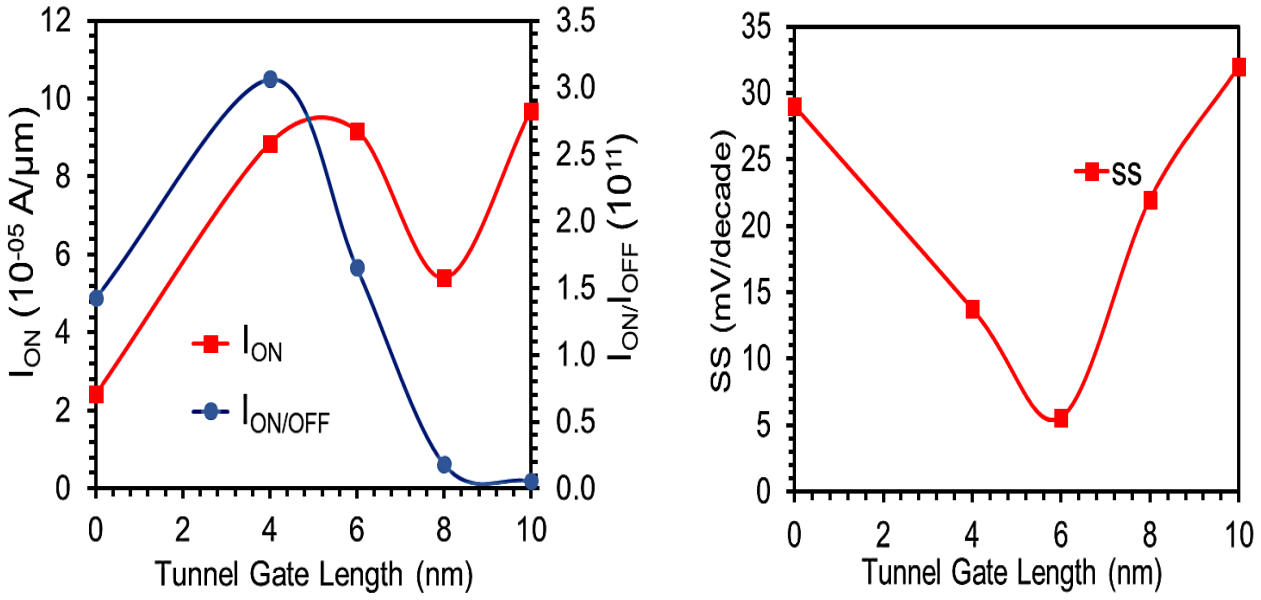
This subsection describes the optimization of L_{tun} in DMG-HJLTFET by varying the L_{tun} from 4nm to 10nm. **Fig. 2.12(a)** displays the OFF-state energy diagram demonstrating position of bands in DMG-HJLTFET alongside the channel direction on shifting L_{tun} from 4 nm to 10 nm. When L_{tun} is increased beyond 4 nm, the channel conduction band and the source valence band start bending downwards. The barrier width becomes narrow, leading to the tunneling of minority carriers across the interface and hence, leakage current rises.



(a) (b)

Fig. 2.12. (a) OFF state and (b) ON state energy diagram of DMG-HJLTFET with tunnel gate length varying from 4nm to 10 nm [24].

In **Fig. 2.12(b)**, when the device is turned on, the distance between the bands across the S/C interface is swayed directly by L_{tun}. The conduction/valence band at the channel/source region starts overlapping. The potential barrier becomes very narrow, contributing to the significant flow of electrons across the interface. The suitable L_{tun} is optimized at 4 nm.



(a) (b)

Fig. 2.13. (a) Comparison of current switching ratio (I_{ON}/I_{OFF}), ON current (I_{ON}), and (b) SS for tunnel gate length variation in DMG-HJLTFET [24].

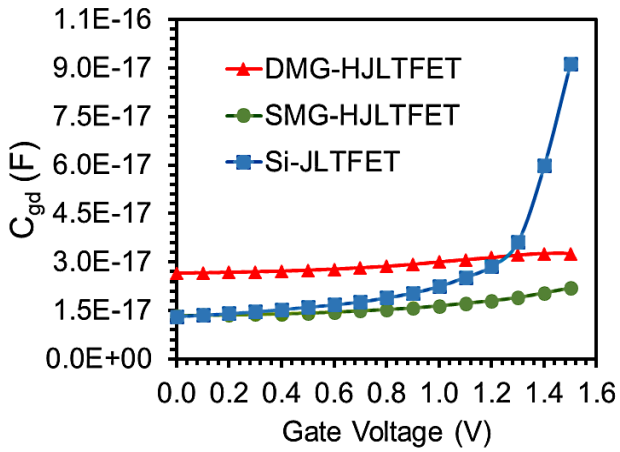
In **Fig. 2.13(a)**, the contrast between the I_{ON}/I_{OFF} and I_{ON} of DMG-HJLTFET is displayed with respect to the disparity of L_{tun}. The L_{tun} is increased from 0 to 10 nm, managing the entire CG length unchanged ($L_{CG} = L_{tun} + L_{sup}$). At 0.0 nm L_{tun} (SMG-HJLTFET), the I_{ON} is 24.3 μA/μm and I_{ON}/I_{OFF} is 1.4×10^{11}. When the L_{tun} starts increasing, the I_{ON} starts rising to 88.5 μA/μm at 4 nm and the I_{ON}/I_{OFF} is 3.1×10^{11}. Once it reaches 8 nm, the I_{ON} falls down (54 μA/μm) and the I_{ON}/I_{OFF} decreases to 1.8×10^{11}. At 10 nm, the I_{ON} rises to 96.9 μA/μm and I_{OFF} escalate sharply to 2.9×10^{-15} A/μm, resulting into lower value of the I_{ON}/I_{OFF} of 5.79×10^{9}. So, the optimized results are obtained at 4 nm L_{tun}. **Fig. 2.13(b)** signifies the variation of SS of DMG-HJLTFET by modifying L_{tun} from 0 nm to

10 nm. At 0 nm L_{tun}, the SS value is 29.03 mV/decade, which is the value for SMG-HJLTFET; at 10 nm, the SS value is 32 mV/decade. The variation in the SS value is due to the band profile modulation as described before. The optimized value of SS is 13.8 mV/decade at 4 nm L_{tun} due to the better I_{ON}/I_{OFF} and I_{ON}.

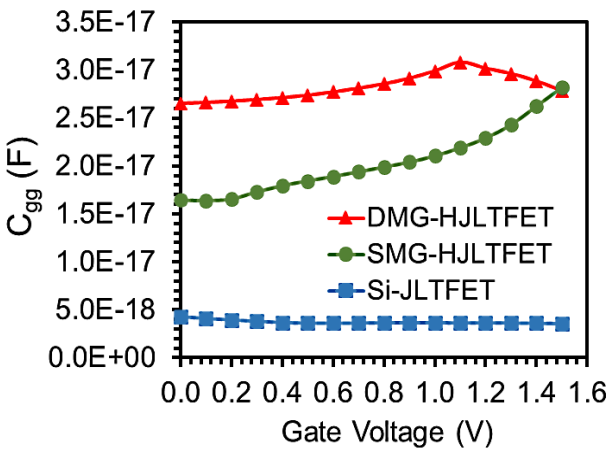
2.6.4 COMPARATIVE ANALOG/RF PERFORMANCE ANALYSIS

This section presents the detailed analysis of analog/RF characteristics of the aforementioned three devices. For the designing of TFET based high switching speed circuits, the parasitic capacitances play a vital role. Therefore, the reliance of parasitic capacitances of the aforementioned devices with respect to gate bias has been investigated in this section. Due to the different inversion charge distribution in TFET, the drain bias has lesser impact at the gate/source (G/S) interface and therefore lesser is the impact of C_{gs} (gate source capacitance) on C_{gg} (total gate capacitance, $C_{gg} = C_{gd} + C_{gs}$) in comparison with C_{gd} (gate drain capacitance). As the gate bias is increased, the inversion layer shifts from the drain to the source and hence C_{gd} increases. As there is minor influence of C_{gs} on C_{gg}, therefore the variation of C_{gg} resembles C_{gd} for DMG-HJLTFET and SMG-HJLTFET. However, the variation of parasitic capacitances is different in case of Si-JLTFET (**Fig. 2.14a-b**).

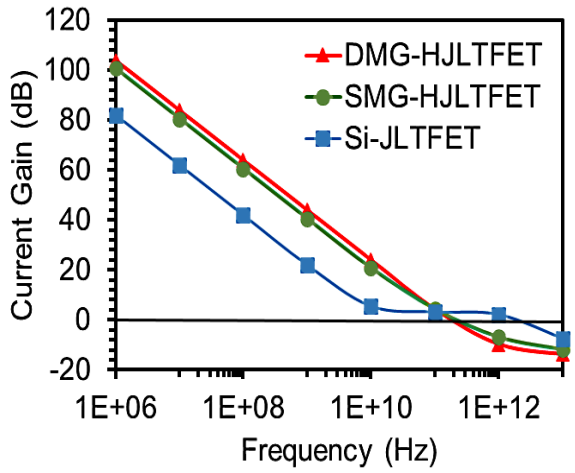
Fig 2.14(c) illustrates the variation of current gain (h_{21}) of three aforementioned devices with frequency at constant V_{GS} = 1.5V and V_{DS} = 1.5V. For the most commonly used cellular communication frequency of the order of 10^6 Hz (1 MHz), the DMG-HJLTFET attains 3.35% and 26.8% higher h_{12} than SMG- HJLTFET and Si-JLTFET, which indicates a substantial enhancement in h_{12} by the application of DMG engineering. This enhancement is attributed to the enhanced I_{ON} and current switching of DMG-HJLTFET as compared to the other two. Similar pattern is observed with unilateral power gain (UPG) of DMG-HJLTFET as compared to the other two, where DMG-



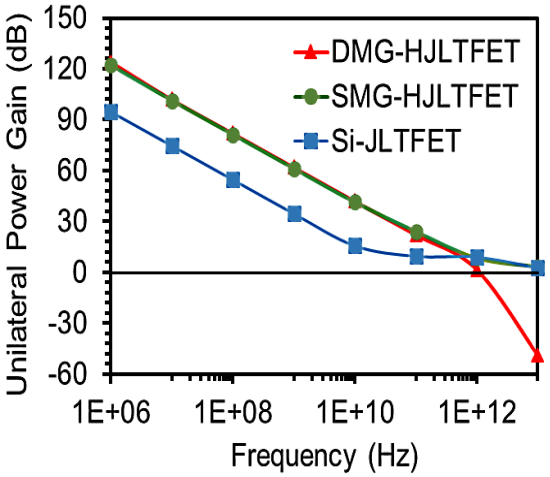
(a)



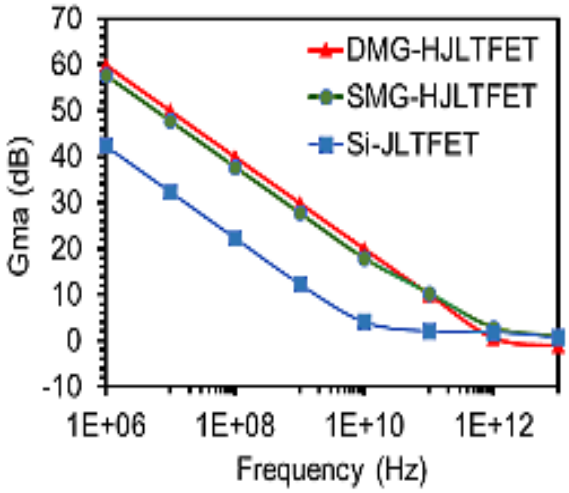
(b)



(c)



(d)



(e)

Fig. 2.14. Parasitic capacitances (a) C_{gd}, (b) C_{gg}, (c) Current gain, (d) Unilateral power gain, and (e) Maximum available power gain (Gma) [24].

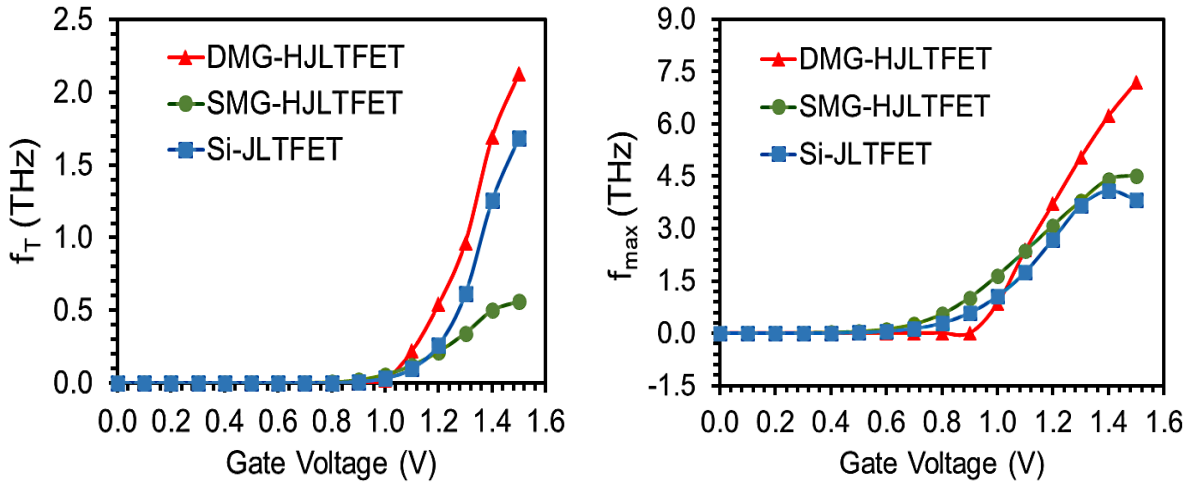
HJLTFET attains 1.63% and 31.4% higher UPG than SMG-HJLTFET and Si-JLTFET for the entire range of frequencies under consideration (**Fig. 2.14d**). It specifies the comparison of the activity and passivity of two port system and measures the highest achievable power. Hence, DMG and SMG systems are more active than Si-JLTFET for the entire frequency range under consideration. **Fig. 2.14(e)** shows the improvement of another important RF parameter, maximum available power gain (Gma) of three aforementioned devices. It is the maximum power gain accessible to the device, which cannot be exceeded. Hence, it is desirable to propose devices with higher Gma. The improved tunneling of carriers and hence higher I_{ON} of DMG-HJLTFET leads to higher Gma (3.6% ↑ and 41.4%↑) as compared to SMG-HJLTFET and Si-JLTFET (**Fig. 2.14e**).

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \quad (2.1)$$

$$f_{max} = \sqrt{\frac{f_T}{8\pi(R_{gd}C_{gd})}} \quad (2.2)$$

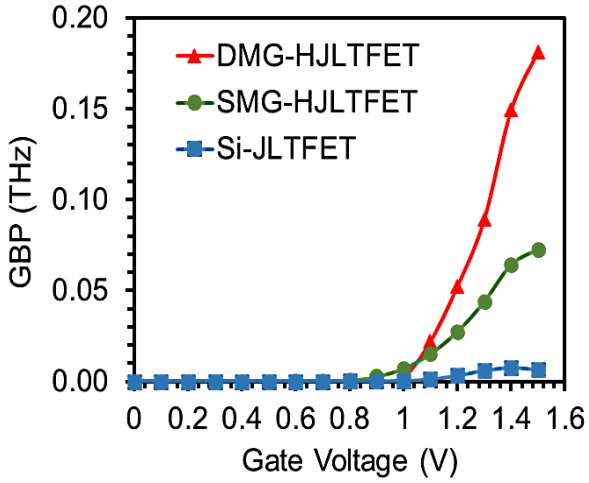
$$GBP = \frac{g_m}{20\pi(C_{gd})} \quad (2.3)$$

Fig. 2.15(a-c) illustrates the disparity of cut off frequency (f_T), maximum oscillation frequency (f_{max}) and gain bandwidth product (GBP) with gate bias for aforementioned devices. The frequency at which the current gain turns to unity (0 dB) is f_T. The value of f_T is considered by extracting g_m, C_{gs}, and C_{gd} using the AC small-signal analysis at an operating frequency of the order of 1 THz along with DC voltage ramped from 0 V to 1.5 V. The enhancement in f_T with gate bais for DMG-HJLTFET is due to the enhancement in g_m by the application of DMG engineering (**Eq. 2.1**) [28]. However, the SMG-HJLTFET attains lower f_T due to the rise in transit time of electrons and degraded parasitic capacitances than Si-JLTFET. Quantitatively, DMG-HJLTFET leads to 3.7- and 1.26-times higher f_T against SMG-HJLTFET and Si-JLTFET resulting in highest switching speed amongst the three (**Fig. 2.15a**).



(a)

(b)



(c)

Fig. 2.15. Variation of (a) Cut-off frequency (f_T), (b) Maximum oscillation frequency (f_{max}), and (c) Gain bandwidth product (GBP) as a function of gate voltage for DMG-HJLTFET, SMG-HJLTFET, and Si-JLTFET [24].

The **Eq. 2.2** illustrates the mathematical expression of f_{max}. It is the frequency at which the maximum unilateral power gain turns to unity (0 dB). The value of f_{max} is calculated by extracting f_T, R_{gd}, and C_{gd} in the same way as done for calculating f_T with DC voltage ramped from 0 V to 1.5 V. From **Eq (2.2-2.3)** [28], it is clear that f_{max} and GBP depends on g_m and parasitic capacitances, so the variation of both follows almost the same fashion. The GBP represents the product of the bandwidth and gain of an amplifier. The peak value of GBP signifies the frequency at which the device attains maximum

gain. In **Fig. 2.15(b-c)**, the f_{max} and GBP shows increment with rise in gate bias. The DMG-HJLTFET, SMG-HJLTFET, and Si-JLTFET attain 7.2(0.18) THz, 4.5(0.07) THz, and 3.8(0.006) THz peak value of f_{max} (GBP), respectively at 1.5 V gate bias.

The comparison of the result characteristics of all three devices is shown in **Table 2.3**, showing superiority of DMG-HJLTFET amongst the three devices in terms of analog/RF parameters.

Table 2.3

Result Characteristics of Si-JLTFET, SMG-HJLTFET and DMG-HJLTFET [24]

	Si-JLTFET	**SMG-HJLTFET**	**DMG-HJLTFET**
I_{ON} (μA/μm)	7	24.3	88.5
I_{OFF} (A/μm)	3.87×10^{-12}	1.72×10^{-16}	2.89×10^{-16}
I_{ON}/I_{OFF}	1.8×10^{6}	1.4×10^{11}	3.1×10^{11}
SS (mV/decade)	123.5	29.03	13.8
g_m (S)	0.37×10^{-4}	0.99×10^{-4}	3.7×10^{-4}
f_{max} (THz)	3.8	4.5	7.2
GBP (THz)	0.006	0.07	0.18

In RF communication systems, the mathematical modeling and study of the admittance (Y) parameters along with the parasitic capacitances for the small signal equivalent circuits is essential. Such investigation has not been given due attention in charge plasma based junctionless TFET devices. In RF communication systems, modeling the parasitic capacitances in the power area scaling has become very crucial as reported in the 2017 edition of IRDS [35]. As shown in **Eq (2.4)** and **(2.5)** [36], there is a direct reliance of parasitic capacitances on these Y parameters and frequency.

$$C_{gs} = \frac{Im(Y_{11})+Im(Y_{12})}{\omega} \qquad (2.4)$$

$$C_{gd} = \frac{-Im(Y_{12})}{\omega} \qquad (2.5)$$

Y_{11}, Y_{22}, Y_{12}, and Y_{21} are the short circuit input admittance, output admittance, forward transfer admittance, and reverse transfer admittance, respectively.

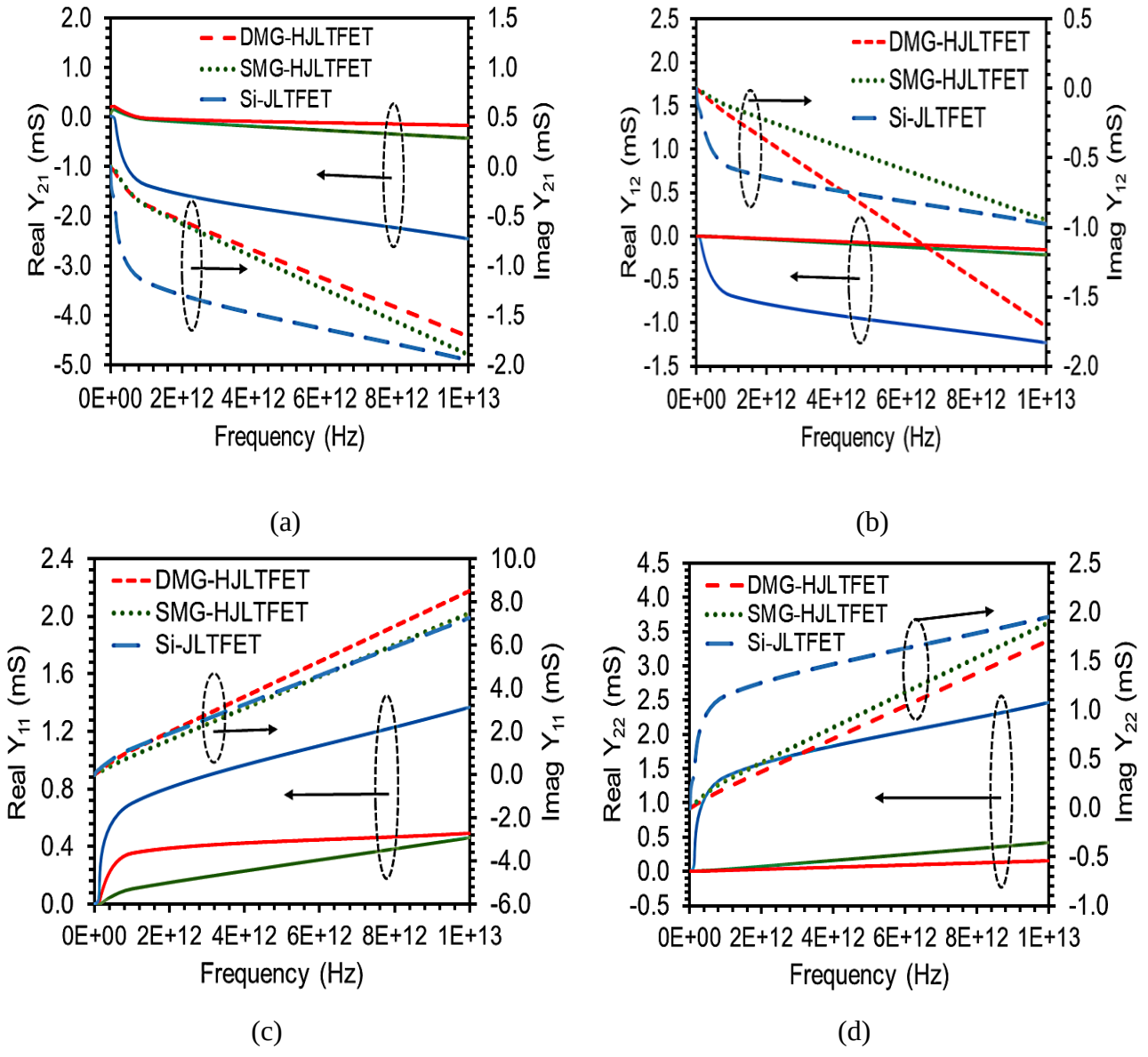


Fig. 2.16. The Variation of real and imaginary components of the admittance (Y) parameters: (a) Y21, (b) Y12, (c) Y11, and (d) Y22 as a function of frequency for DMG-HJLTFET, SMG-HJLTFET, and Si-JLTFET [24].

Fig. 2.16 (a-d) illustrates the comparison of real and imaginary components of Y-parameters of three devices. The Y_{11} and Y_{22} show similar variation of gradual increment with increment in frequency for all three devices, however the variation of real and imaginary components of Y_{11} and Y_{22} is lower in DMG-HJLTFET and SMG- HJLTFET than Si-JLTFET. The Y_{12} and Y_{21} are gradually decreasing with rise in frequency, however the magnitude of variation is lower in DMG-HJLTFET and SMG-HJLTFET than Si-JLTFET.

Table 2.4 presents the comparison of present DMG-HJLTFET device with the recently designed TFET devices [15], [37], showing the superior RF performance of DMG-HJLTFET.

Table 2.4

Comparison of RF FOMs of DMG-HJLTFET with previously published devices [24].

	DMMG-HJLTFET [15]	**HJ-HD-DLTFET [37]**	**DMG-HJLTFET (Present)**
C_{gd} (F)	3.6×10^{-15}	8.0×10^{-15}	3.26×10^{-17}
C_{gg} (F)	3.7×10^{-15}	–	2.82×10^{-17}
f_T (GHz)	9.17	107	2120
GBP (GHz)	0.17	16.3	180

Table 2.5 displays the comparison of analog result characteristics of the proposed device with previously published hetero-material-junctionless structures based on different materials in the literature, where the proposed device appears to have promising result characteristics in terms of I_{ON}, SS, and g_m.

Table 2.5

Comparison of analog FOMs of DMG-HJLTFET with previously published devices [24].

	DMMG-HJLTFET [15]	**H-JLTFET [23]**	**DMG-HJLTFET [11]**	**DMG-HJLTFET (This work)**
I_{ON} (A/μm)	10×10^{-6}	6×10^{-6}	10×10^{-4}	88.5×10^{-6}
I_{OFF} (A/μm)	6.5×10^{-19}	1.72×10^{-18}	7.8×10^{-14}	2.89×10^{-16}
I_{ON}/I_{OFF}	1.5×10^{13}	2.3×10^{12}	1.2×10^{10}	3.1×10^{11}
SS (mV/decade)	52	> 60	29	13.8
g_m (S)	1.2×10^{-5}	5.5×10^{-6}	2.8×10^{-4}	3.7×10^{-4}

2.7 COMPARATIVE LINEARITY AND INTERMODULATION DISTORTION ANALYSIS

It is critical to study the linearity parameters of a device to analyse its behaviour in the high-frequency regime. The modern communication system must achieve minimum signal distortion and better linearity along with high speed. Here, the significance of using the III-V compound semiconducting materials (InAs/GaAs) and DMG engineering has been examined on the linearity performance and intermodulation distortion in the form of VIP2, VIP3, IIP3, IMD3, 1-dB compression point, and g_{m3} as below.

$$g_{mn} = \frac{1}{n!}\frac{d^n I_{DS}}{dV_{GS}^n}, \quad where\ n = 1,2,3 \tag{2.6}$$

$$VIP2 = 4 \times \frac{g_{m1}}{g_{m2}} \tag{2.7}$$

$$VIP3 = \sqrt{24 \times \frac{g_{m1}}{g_{m3}}} \tag{2.8}$$

$$IIP3 = \frac{2}{3} \times \frac{g_{m1}}{g_{m3} \times R_S} \quad (2.9)$$

$$IMD3 = R_S\,[4.5 \times (VIP3)^3 \times g_{m3}]^2 \quad (2.10)$$

$$1 - dB = 0.22 \sqrt{\frac{g_{m1}}{g_{m2}}} \quad (2.11)$$

In **Eq. (2.10)**, $R_S = 50\ \Omega$ is imputed owing to its practical applications in RF systems. The VIP2 is extrapolated input voltage at which first- and second-order harmonic voltages are equal and the VIP3 is extrapolated input voltage at which first- and third-order harmonic voltages are equal [38]. For high linearity, VIP2 and VIP3 must be high. The third-order intercept input power (IIP3) is defined as extrapolated input power at which the first- and third-order harmonic powers are equal. The third-order intermodulation distortion power (IMD3) is defined as the third-order intermodulation distortion corresponding to extrapolated intermodulation power at which the first- and third-order intermodulation harmonic powers are equal [38]. In **Eq. (2.8)-(2.10)**, the third-order transconductance coefficient, g_{m3} determines the lower limits on the distortion, and hence, the amplitude of g_{m3} must be low for better linearity and low distortion applications. **Eq. (2.11)** defines the 1dB compression point which is the input power due to which the gain drops by 1dB.

For wireless applications, the third-order transconductance parameter is more dominant than the second-order transconductance because it leads to non-linearity due to the frequency interference and is responsible for output signal distortions. **Fig. 2.17** illustrates the variation of g_{m3} with V_{GS}. Among the three devices, DMG-HJLTFET has the lowest g_{m3} at $V_{GS} = 1.5$ V and its amplitude is 9 times lower than SMG-HJLTFET and 20.6 times lower than Si-JLTFET. However, above a certain gate bias, there is a considerable variation in g_{m3} with gate voltage for DMG-HJLTFET in comparison with other devices. The large variation of g_{m3} with gate voltage in DMG-HJLTFET represents the

non-linear behaviour of g_{m3} due to the harmonic distortion. The increment in gate voltage beyond a certain point gives rise to harmonic distortion generated by g_{m3}, which results in reduced gate control over the channel; this, however can be avoided by setting the gate bias close to g_{m3} zero-crossover point (mentioned in **Fig. 2.21c**). Because of almost symmetrical variation of g_{m3} around the zero cross-over point (**Fig. 2.17**), the harmonic distortion generated from it can be nullified for a small signal [39].

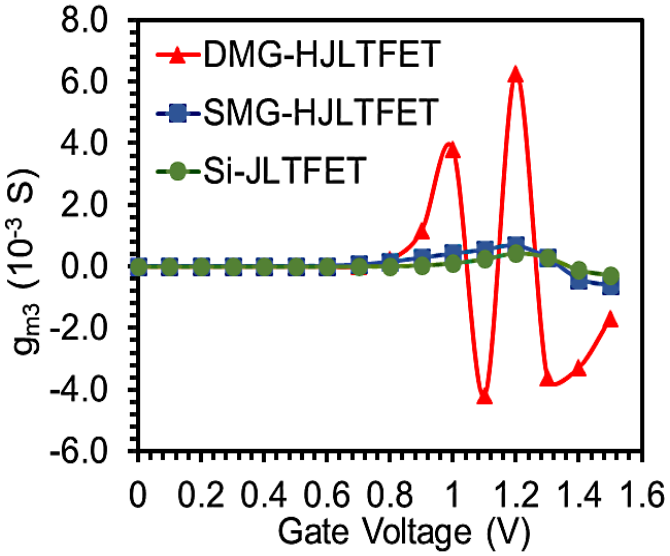
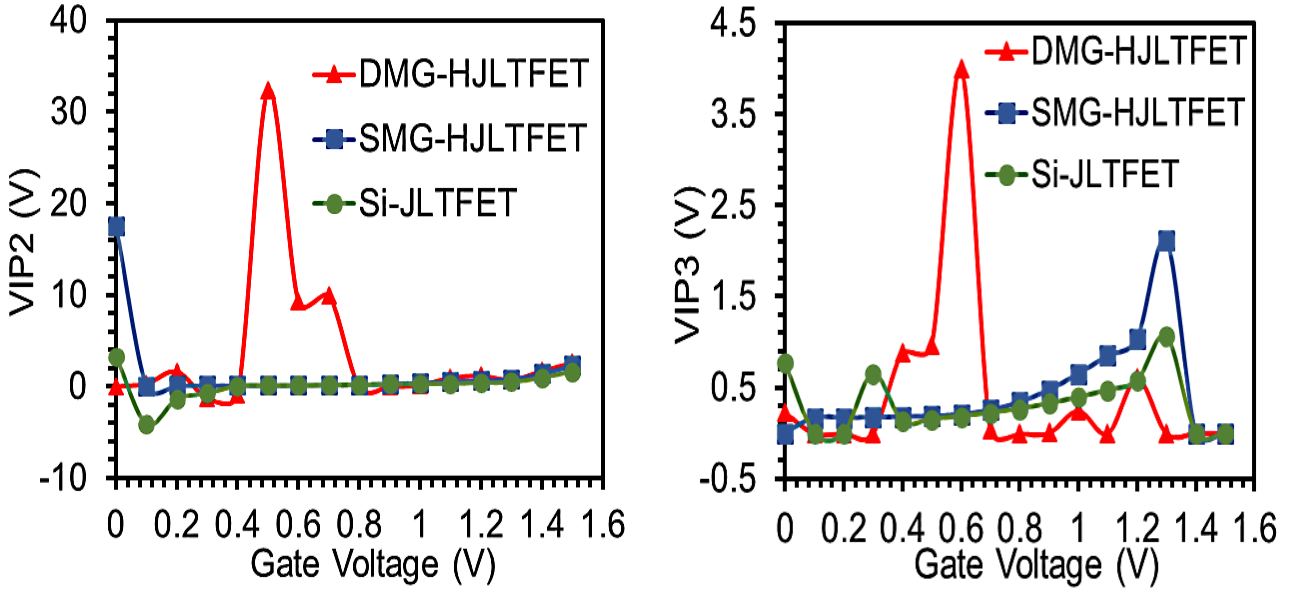


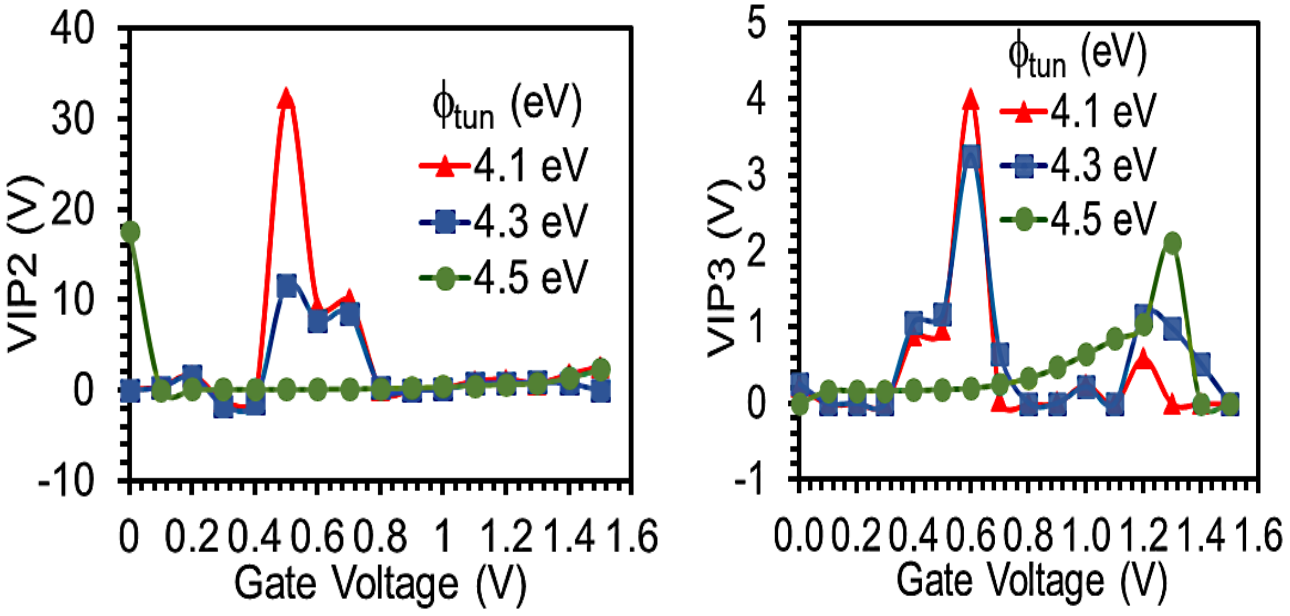
Fig. 2.17. g_{m3} of DMG-HJLTFET, SMG-HJLTFET and Si-JLTFET [24].

In **Fig. 2.18(a)-(b)**, DMG-HJLTFET attains maximum peak value of VIP2 and VIP3 at very low V_{GS}, which signifies that in order to preserve high linearity, low driving voltage is required. Si-JLTFET has the lowest value of the VIP3 peak among three devices. The DMG and the lower bandgap compound semiconducting material in the source and higher bandgap material in the channel and drain in our proposed device fosters higher current driving proficiency and hence lead to higher VIP2 and VIP3 peak values towards the lower gate voltage side. DMG-HJLTFET attains 220 times higher value of VIP2 than SMG-HJLTFET and 276 times higher value than Si-JLTFET and it also achieves 19.3 times higher value of VIP3 than SMG-HJLTFET and 21.9 times higher value than Si-JLTFET.



(a) (b)

Fig. 2.18. Disparity of (a) VIP2 and (b) VIP3 as a function of gate voltage for DMG-HJLTFET, SMG-HJLTFET, and Si-JLTFET [24].



(a) (b)

Fig. 2.19. Plot of (a) VIP2 and (b) VIP3 as a function of gate voltage for TG work function variation [24].

Fig. 2.19(a)-(b) signifies the disparity of VIP2 and VIP3 as a function of gate voltage for TG work function variation. The maximum peak value of VIP2 and VIP3 gets shifted towards the lower gate voltage for DMG configuration by using TG of 4.1 eV work function towards the source region, whereas when the TG work function increases to 4.3 eV, the peak values of VIP2 and VIP3 decrease. The 4.5 eV TG work function attains the lowest VIP2 and VIP3, shifting the peaks towards the higher gate voltage.

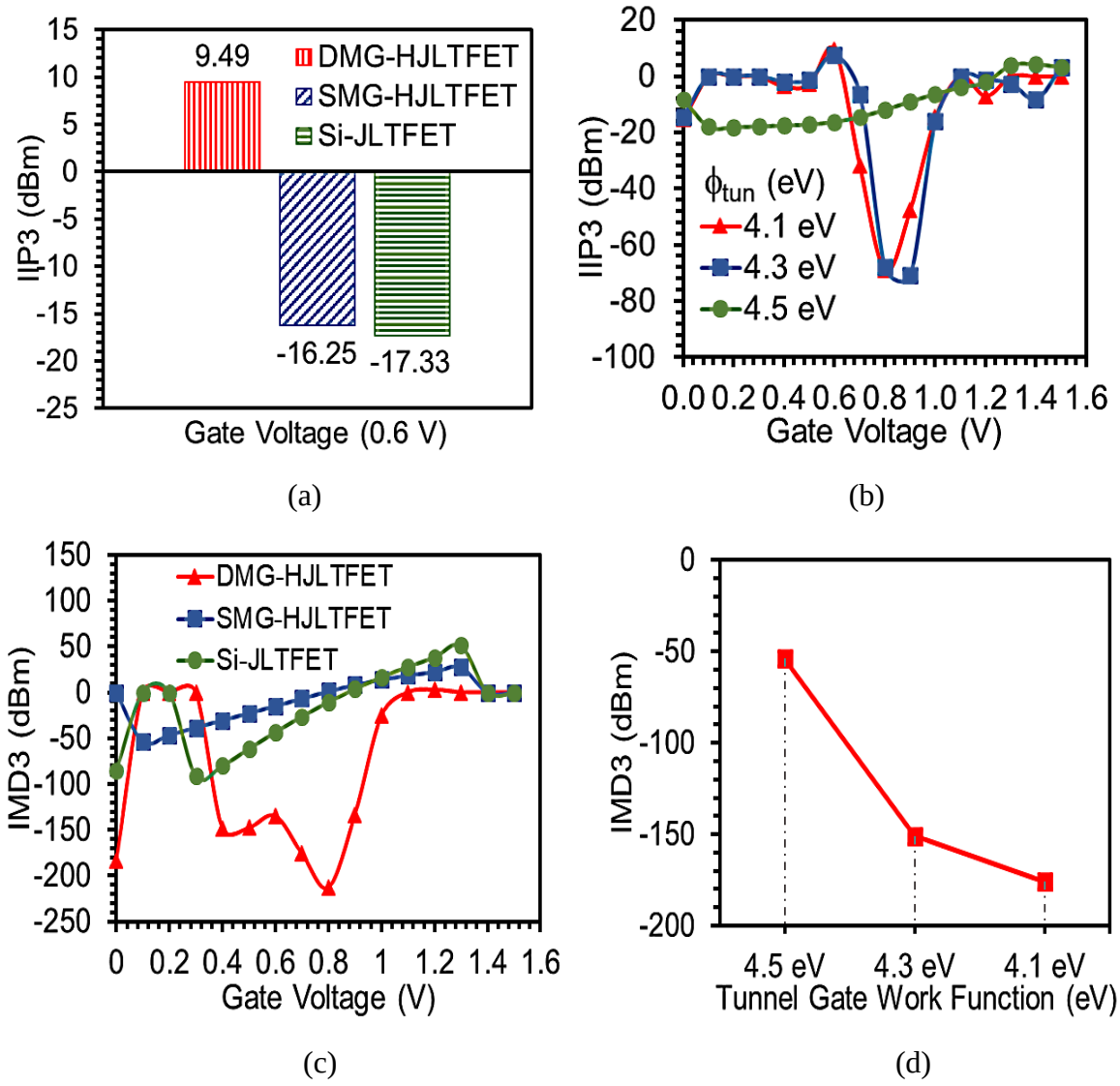


Fig. 2.20. Disparity of (a) IIP3 and (c) IMD3 as a function of gate bias for DMG-HJLTFET, SMG-HJLTFET, and Si-JLTFET. Disparity of (b) IIP3 and (d) IMD3 as a function of gate bias TG work function variation [24].

Fig. 2.20(a) illustrates the IIP3 peak value of DMG-HJLTFET, SMG-HJLTFET, and Si-JLTFET at $V_{GS} = 0.6$ V. IIP3 of DMG-HJLTFET is 158.4% higher than SMG-HJLTFET and 154.7% higher than Si- JLTFET. Si-JLTFET has the lowest value (-17.33 dBm) among the three devices, which indicates the potential of DMG-HJLTFET for high linearity applications. The difference between the IIP3 peak values of DMG-HJLTFET and SMG-HJLTFET is the consequence of DMG design, as discussed before. It aids in attaining the maximum peak value of IIP3 at lower gate voltage, indicating its higher linearity attributes at low gate bias. The same is observed in **Fig. 2.20(b)**, where the disparity of IIP3 as a function of gate voltage is shown by varying the TG work function. On applying lower work function TG of 4.1 eV towards the source and higher work function SG of 4.5 eV towards the drain, the maximum peak value of IIP3 can be achieved at just 0.6 V gate bias. For better linearity and distortion-free operations, IIP3 needs to be high and IMD3 needs to be low. IIP3 shows approximately similar variation for TG work function 4.1 eV and 4.3 eV and when we increase the work function to 4.5 eV, the peak value is attained at 1.3 V of gate voltage, which is not favourable when compared with lower work function values. It implies that the optimized value of the TG work function is 4.1 eV.

Fig. 2.20(c) illustrates the disparity of IMD3 for DMG- HJLTFET, SMG-HJLTFET, and Si-JLTFET as a function of gate bias. DMG-HJLTFET exhibits the lowest value of IMD3 as -212.9 dBm, whereas SMG-HJLTFET attains 1.24 dBm and Si-JLTFET attains 10.4 dBm with IMD3 of DMG-HJLTFET being 171.8 orders lower than SMG-HJLTFET and 20.5 orders lower than Si-JLTFET, which is essential for a distortionless communication system. **Fig 2.20(d)** clarifies that the hetero-material JLTFET with 4.1 eV TG work function exhibits lowest value of IMD3 as compared to 4.3 eV and 4.5 eV TG work function. The 4.1 eV TG work function gives IMD3 approximately 16.4% lower than 4.3 eV TG and 225.8% lower than 4.5 eV TG work function. Thus, the optimized TG work function value of 4.1 eV reduces the amplitude distortion at low gate bias.

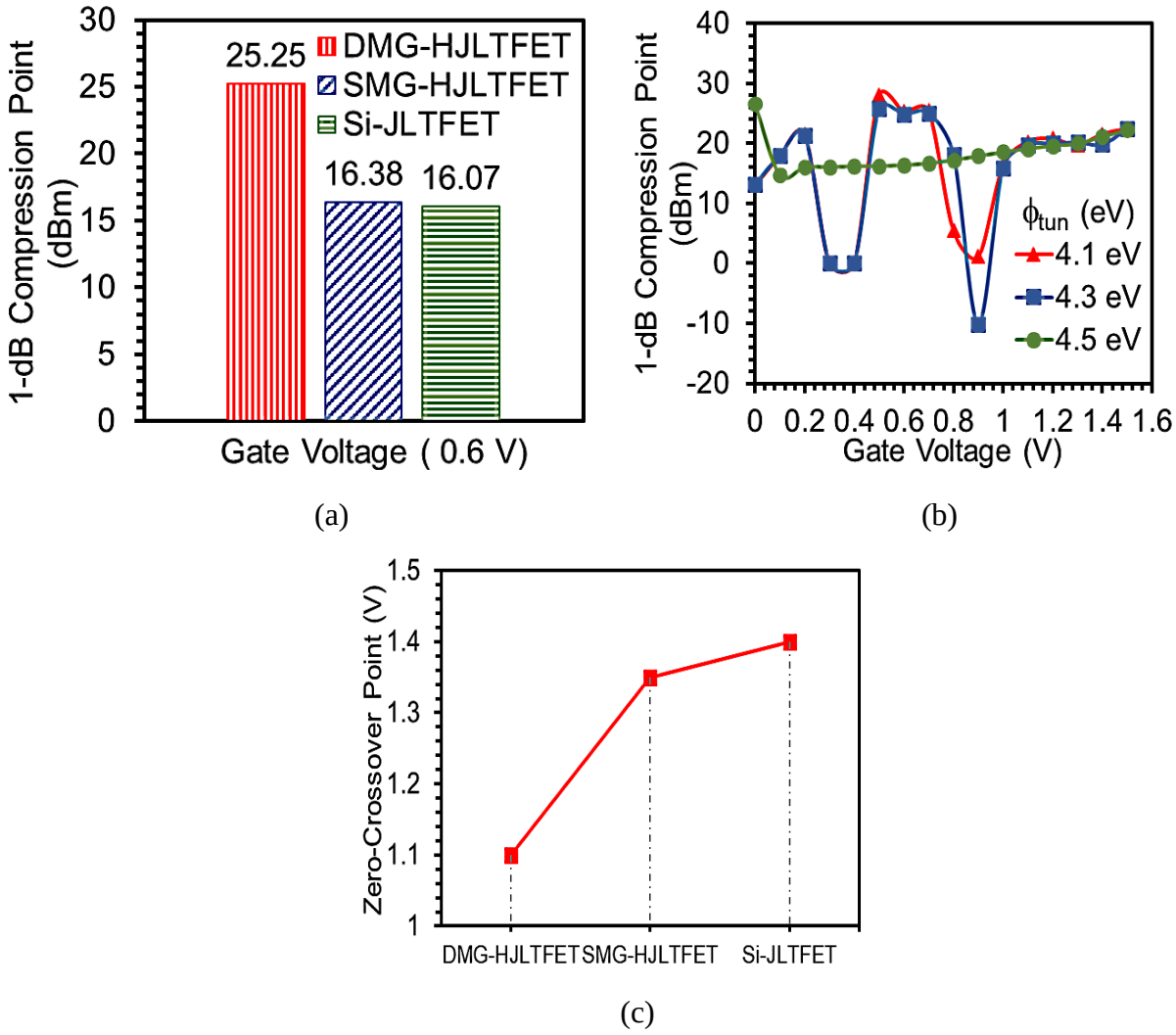


Fig. 2.21. Plot of 1-dB compression point as a function of gate bias for (a) DMG-HJLTFET, SMG-HJLTFET, and Si-JLTFET and (b) TG work function variation. (c) Variation of zero-crossover point with gate bias for DMG-HJLTFET, SMG-HJLTFET, and Si-JLTFET [24].

In **Fig. 2.21(a)**, 1-dB value is improved in the case of DMG-HJLTFET than SMG-HJLTFET and Si-JLTFET, due to the reduced signal distortion and higher value of g_m. At lower gate voltage (0.6 V), DMG- HJLTFET exhibits the maximum (25.25 dBm) value of 1dB compression point, whereas SMG-HJLTFET exhibits 16.38 dBm as the maximum 1dB compression point value. Si-JLTFET has the least 1dB compression point value. Out of three devices, DMG-HJLTFET shows 54% improved value of 1dB compression point than SMG-HJLTFET and 57% higher than Si-JLTFET.

Fig. 2.21(b) demonstrates the disparity of 1dB compression point with gate voltage of 1.5 V for TG work function variation of 4.1 eV, 4.3 eV, and 4.5 eV. If we apply the 4.1 eV TG work function, (DMG), the maximum peak value of 1dB compression point shifts towards the lower gate voltage and becomes 8.5% higher than 4.3 eV TG and 75% higher than 4.5 eV TG work function. The maximum value of 1dB compression point is still observed at higher gate bias on changing of TG work function to 4.5 eV. Thus, the optimized value of TG work function is 4.1 eV. **Fig. 2.21(c)** depicts the disparity of zero-crossover point for DMG-HJLTFET, SMG-HJLTFET, and Si-JLTFET. The choice of optimum gate bias point can help in suppressing the non-linearity in terms of g_{m3}, which can be determined through the zero-crossover point of g_{m3}. It is observed from **Fig. 2.21(c)** that in DMG-HJLTFET, the zero-crossover point gets shifted towards lower gate bias as compared to SMG-HJTFET and Si-JLTFET, due to the application of DMG.

Moreover, the bandgap and DMG engineering incorporated in DMG-HJLTFET leads to improved intermodulation distortion figure of merits (FOMs) such as VIP2, VIP3, IIP3, IMD3, and 1dB compression point, making the transistor level linearization more efficient and less time consuming than the expensive experimental efforts and optimization through device fabrication. These improved parameters maintain the linearity of the wireless communication systems even when receiving a weak signal, making the device highly suitable for wireless applications such as low noise amplifiers (LNA) for cellular transceivers, space communications and radio astronomy [40]. Moreover, the other improved performance parameters such as I_{ON}, I_{ON}/I_{OFF}, I_{OFF}, steeper SS, and $g_m$of DMG-HJLTFET as compared to its counter devices makes it desirable for fast switching performance and analog applications.

2.8 CONCLUSION

In this chapter, the potential of DMG-HJLTFET is explored in terms of analog, RF/microwave, linearity performance metrics and intermodulation distortion parameters by optimizing the suitable tunnel gate work function and length in the DMG engineered HJLTFET designed with InAs/GaAs compound semiconducting hetero-materials through extensive 2-D simulations. The dual-material gate engineering showed the improved electrostatic characteristics in the form of high I_{ON} and I_{ON}/I_{OFF} in DMG-HJLTFET as compared to SMG-HJLTFET and Si-JLTFET. This study has established a significant band bending at the hetero-material tunneling interface of DMG-HJLTFET leading to narrower barrier width by the application of DMG engineering. The SS value of DMG-HJLTFET is 52.4% and 88.8% reduced in comparison with SMG-HJLTFET and Si-JLTFET due to the energy-band profile modulation obtained by dual-material gate technology and III-V compound semiconducting materials. The optimum RF FOMs have been obtained in the form of f_{max}, GBP, h_{12}, UPG, Gma reflecting its promising applications in high frequency and microwave regime. whereas, the conventional homo-material Si based device have shown the degraded performance in comparison. The h_{12} (UPG) of DMG-HJLTFET is 3.35% and 26.8% (1.63% and 31.4%) higher than SMG-HJLTFET and Si-JLTFET. Besides all the advantages of the proposed device, the improvement in the small signal admittance (Y) parameters on the amalgamation of DMG and band-gap engineering techniques makes the device suitable for future high-speed switching systems. Moreover, DMG-HJLTFET is found to have better g_{m3}, VIP2, VIP3, IIP3, IMD3 and 1dB compression point in comparison with SMG-HJLTFET and Si-JLTFET. The 1dB compression point of DMG-HJLTFET is 55% superior to SMG-HJLTFET and 57% superior to Si-JLTFET. Therefore, DMG-HJLTFET can be considered an alternative in the modern wireless and distortion-less communication systems.

However, the use of conventional low-k material (SiO_2, mono-dielectric) in the oxide region under the control gate nearby the source side and drain side lowers the ON current by producing the

ambipolar conduction in the device. Also, high-k dielectric materials (mono-dielectric) enhance the leakage current. Therefore, a heterogeneous gate dielectric engineering is executed in the next chapter by developing a heterogeneous gate dielectric stack having high-k and low-k material in the oxide region under CG nearby the source and drain regions, respectively.

2.9 REFERENCES

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CHAPTER-3

HIGH SWITCHING PERFORMANCE OF NOVEL HETEROGENEOUS GATE DIELECTRIC – HETERO-MATERIAL BASED JUNCTIONLESS-TFET

This chapter reports the effect of heterogeneous gate dielectric stack in a III-V compound semiconducting material based hetero-structure junctionless tunnel field effect transistor (reported in **chapter 2**), HD-HJLTFET for analog analysis. In this proposed device, low bandgap material, InAs is used in the source region and higher bandgap material, GaAs is used in the channel and drain region to implement the bandgap engineering at the source to channel interface. Further, a heterogenous gate dielectric has been introduced by replacing the conventional gate oxide under the control gate by high-k gate oxide and low-k gate oxide at the source and drain side, respectively. The selection of an appropriate high-k oxide for the hetero dielectric and length of the high-k oxide in proposed device has been optimized using different dielectric materials in the high-k region. The results of hetero-dielectric HJLTFET (HD-HJLTFET) are also compared with Mono-dielectric HJLTFET for Low-k HJLTFET (only SiO_2 at Control Gate) and High-k HJLTFET (only HfO_2 at Control Gate). The proposed device shows enhanced performance in terms of I_{ON} (~304% and ~15% higher), I_{OFF} (~9% and ~13% lower), I_{ON}/I_{OFF} (~348% and ~36% higher), device efficiency (480% and ~195% higher), g_m (~302% and ~14% higher), g_{m3} (~309% and ~12% lower), and Subthreshold swing (~16% and ~10% reduced) as compared to mono-dielectric devices, Low-k HJLTFET and High-k HJLTFET, respectively.

3.1 INTRODUCTION

A conventional MOSFET faces a difficulty in attaining a low-thermal budget because of the necessity of complex fabrication and large doping-concentration gradient due to the existence of two source/channel and channel/drain junctions. Scaling down the MOSFET dimensions in accordance with the International Technology Roadmap for Semiconductors (ITRS) guidelines becomes very challenging due to the doping junctions present between the source/channel and channel/drain boundaries beyond 32-nm nodes technology [1]-[3]. In order to withstand the downscaling issues with time various novel structures have been evolved by the researchers. In past few years junctionless field effect transistors (JLFET) have attracted the interest of many researchers due to the absence of doping junctions [4]-[5]. Unlike MOSFET, the doping concentration of JLFET is the same all over the source, channel, and drain regions. Owing to the absence of concentration gradient in the lateral direction of the channel, this device is quite easier to fabricate along with improved electrical performance and better uniformity than MOSFET. The junctionless concept have been explored in many devices such as TFETs [6], FinFETs [7], Negative capacitance FETs [8], Nanowire FETs [9]. TFETs are the most promising candidates in present technology over MOSFETs owing to its steeper sub-threshold swing (SS) (< 60 mV/decade) and lower leakage current (I_{OFF}), [10-15], as discussed in the introduction part of **chapter 2**. The Tunnel FETs work on the fundamental mechanism of band to band tunneling [16]-[17]. By applying the junctionless technology, the result characteristics of a TFET can be enhanced in the form of higher ON current (I_{ON}), steeper SS along with fast current switching ratio (I_{ON}/I_{OFF} ratio). Along with junctionless technology, the direct bandgap III-V compound semiconducting materials also aid to accomplish higher I_{ON} by incorporating lower bandgap and higher bandgap materials in the Source and channel region [18]-[20]. Further, enhancement in I_{ON} and SS can be achieved by High-k gate oxide; however, it increases the leakage

current and the ambipolar current in TFETs. So hetero-gate dielectric is better option in comparison to high-k dielectrics [21].

In this chapter, a hetero-gate-dielectric hetero-junctionless TFET (HD-HJLTFET) has been designed using III-V compound semiconducting materials. The InAs (lower bandgap) and GaAs (higher bandgap) are used in the source and channel regions, respectively giving rise to a hetero-junctionless device, which provides better results as compared to Si based TFET because of the higher energy bandgap and hence wider tunneling barrier in case of Si material-based devices as discussed in the **chapter 2**. A heterogeneous gate dielectric engineering (HDE) is executed in the proposed device, HD-HJLTFET by locating high-k and low-k material (SiO_2) in the oxide region under the control gate (CG) nearby the source side and drain side, respectively. The results are obtained for the optimization of the high-k stack material and stack length by using different dielectric materials in the stack. A comparison of HD-HJLTFET is made with two conventional configurations namely Low-k HJLTFET (which uses only SiO_2 as the gate oxide under the control gate) and High-k HJLTFET (which uses only a high-k oxide under the control gate) is investigated in this chapter for analog applications.

3.2 DEVICE STRUCTURE

Fig. 3.1(a)-(c) represents the graphic outlook of entire device design framework [(a) HD-HJLTFET, (b) Low- k HJLTFET, and (c) High-HJLTFET]. The device design parameters have been mentioned in **Table 2.2** of **chapter 2**. The results are evaluated after optimizing the high-k material as HfO_2 with optimized high-k stack length of 7nm. The biasing conditions of the device are $V_{GS} = 1.5\ V$ and $V_{DS} = 1.5\ V$ for the ON state and $V_{GS} = 0.0\ V$ and $V_{DS} = 1.5\ V$ for the OFF state.

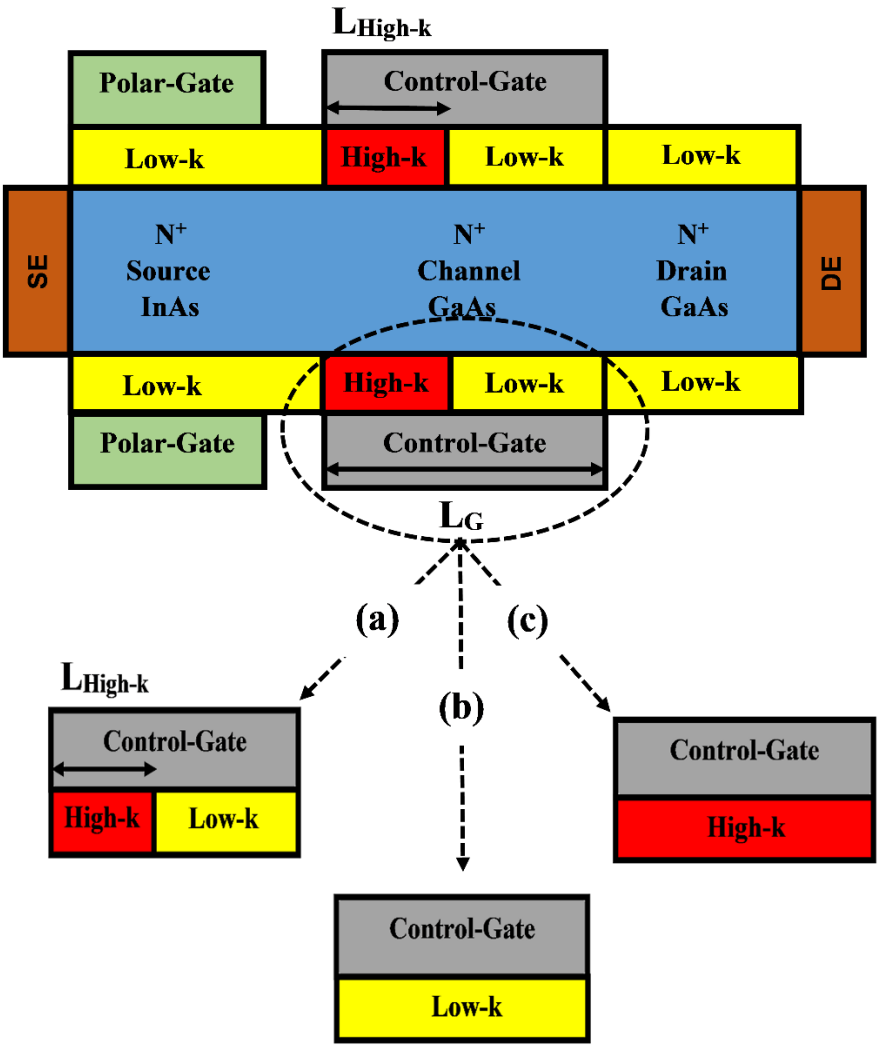

Fig. 3.1. Device architecture of (a) HD-HJLTFET, (b) Low-k HJLTFET, and (c) High-k HJLTFET [22].

3.3 RESULTS AND DISCUSSION

The energy band diagrams of HD-HJLTFET and Low-k HJLTFET are represented in **Fig. 3.2(a)** for the OFF state, ($V_{GS} = 0.0\ V, V_{DS} = 1.5\ V$). The implementation of hetero-material InAs in the source and GaAs in the channel and drain, the bandgap difference between the two materials leads to a wider barrier width at the source to channel interface as evident from the figure. This results in minor flow of carriers due to the P-i-N diode leakage. As revealed in **Fig. 3.2(b)**, when the device is turned on,

($V_{GS} = 1.5\ V, V_{DS} = 1.5\ V$) by applying the gate biasing of 1.5 V at the control gate, due to the hetero-materials present at the source and channel, a local minimum is induced in the conduction band at the source to channel (S/C), boundary.

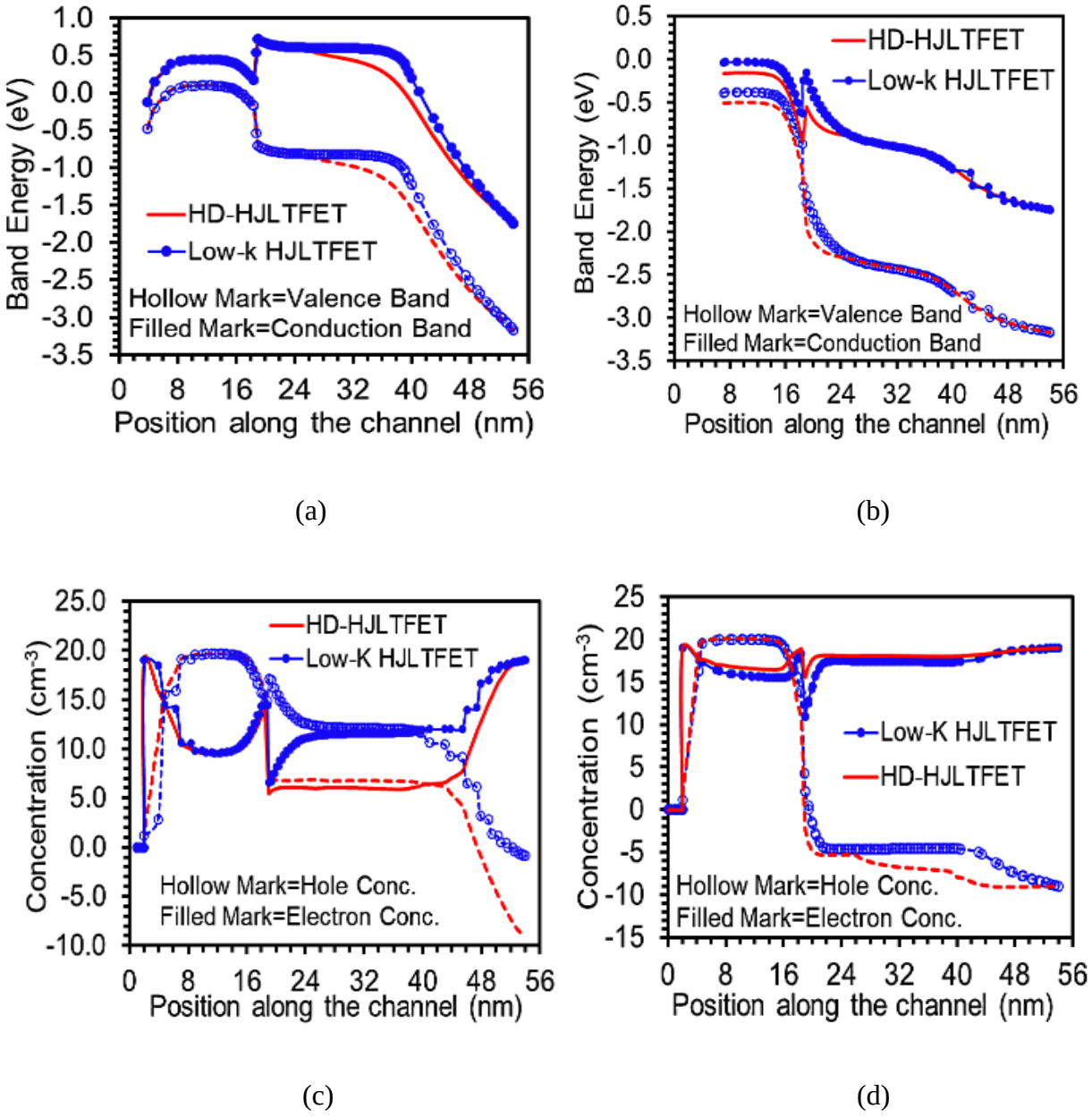

Fig. 3.2. (a) OFF state energy band diagram, (b) ON state energy band diagram, (c) OFF state carrier concentration and (d) ON state carrier concentration of HD-HJLTFET and Low-k HJLTFET [22].

Due to the application of high-k oxide towards the source, gate to channel coupling is strengthened and this local minimum induced in the conduction band edge bends further and overlaps the valence band edge of the source. This process elevates the tunneling probability of the carriers from the source to the channel because of the narrower tunneling barrier width at the S/C boundary as compared to the low-k oxide.

Fig. 3.2(c) illustrates the electron and hole concentration of HD-HJLTFET and Low-k HJLTFET, when no gate biasing is applied. This reveals that the devices attain the P-i-N doped configuration deprived of any physical doping being implanted. In the ON state, as shown in **Fig. 3.2(d)**, When gate biasing is applied to CG, the electron concentration profile of the HD-HJLTFET increases under the control gate due to the high-k stack towards the source region. It gives rise to an n doped pocket region beneath the spacer region between CG and PG. Hereafter the barrier width gets shortened and causes to shift in the tunneling of the carriers towards the left of the junction. This fact is further supported by the results revealed by the non-local band-to-band electron tunneling rate of HD-HJLTFET Compared with Low-k HJLTFET as shown in **Fig. 3.3(a)**.

As depicted from the **Fig. 3.3(a)**, on the application of high-k oxide close to the source, overlapping of conduction band local minimum edge and the valence band of the source leads to narrower barrier width as explained before. The electrons tunnel through the barrier with a higher tunneling rate in HD-HJLTFET as the electric field of CG is greater at the S/C boundary as compared to Low-k HJLTFET, as revealed in **Fig. 3.3(b)**, providing higher mobility to the carriers to tunnel through the junction whereas, low-k dielectric material diminishes the mobility of carriers due to lower gate to channel coupling. This improves the flow of the electrons across the hetero- junction and hence electrons start early tunneling at a higher rate as compared to Low-k HJLTFET. Amongst three devices as revealed in **Fig. 3.3(b)**, HD-HJLTFET and High-k HJLTFET show almost similar trend of electric field at the S/C intersection in contrary to Low-k HJLTFET. Whereas, the electric field of

High-k HJLTFET is risen at the D/C interface as compared to other two devices as an outcome of high-k oxide at the drain side, which rises the drain to channel coupling.

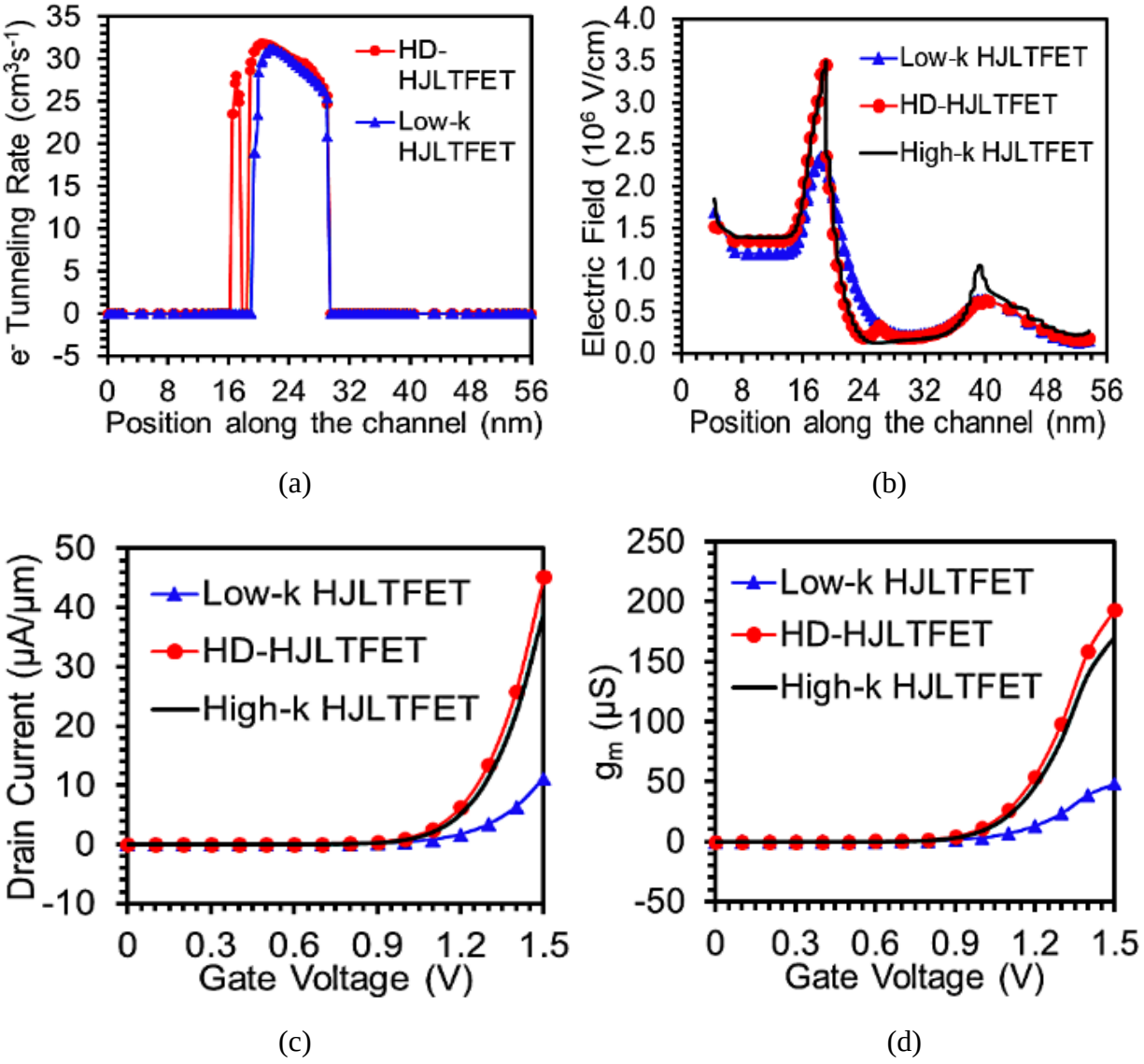

Fig. 3.3. (a) Non-local BTBT electron tunneling rate and (b) ON state Electric field along the channel direction. (c) Transfer characteristics and (d) Transconductance, g_m of HD-HJLTFET compared with Low-k HJLTFET and High-k HJLTFET [22].

In **Fig. 3.3(c)**, a comparison of the transfer characteristics of HD-HJLTFET is displayed with Low-k HJLTFET and High-k HJLTFET. The ON current of HD-HJLTFET is 1.2 orders higher in magnitude than High-k HJLTFET and 4.04 orders higher in magnitude than Low-k HJLTFET. This increment in ON current is due to the channel modulation leading to larger tunneling probability of the electrons

across the junction on the application of heterogeneous gate dielectric stack under CG. Another crucial parameter that determines the current driving efficacy of the device at a constant drain bias is the transconductance, g_m. To attain higher gain, the device should exhibit higher value of g_m. From **Fig. 3.3(d)**, it is observed that HD- HJLTFET shows superiority in terms of g_m in comparison to Low-k HJLTFET and High-k HJLTFET attributed to the enhanced driving current on the application of heterogeneous gate dielectric under CG.

Fig. 3.4(a) it can be observed that the higher order transconductance coefficient, g_{m3} attains lowest value for HD-HJLTFET, which is 11.96% and 309.4% lower as compared to High-k HJLTFET and Low-k HJLTFET, respectively. The aforementioned reduction in g_{m3} for HD-HJLTFET supports improved linearity performance of the device because of lower amplitude. **Fig. 3.4(b)** displays the comparison of device efficiency as a function of gate voltage, which is the ratio of transconductance to current. It is noticeable from the **Fig. 3.4(b)** that hetero-dielectric device attains the highest device efficiency as compared to Low-k HJLTFET and High-k HJLTFET. The peak of device efficiency in HD-HJLTFET and Low-k HJLTFET is also attained at lower gate voltage than High-k HJLTFET. Device efficiency of the proposed device is 194.5% and 480% higher than High-K HJLTFET and Low-k HJLTFET, respectively. In **Fig. 3.4(c)**, it is worth observing that a minimal leakage current (OFF current) is produced in HD-HJLTFET, which is 12.7% and 9.03% lower than High-k HJLTFET and Low-k HJLTFET, respectively. This is resulted because of the larger tunneling barrier width at the S/C interface when the device is in the OFF state. The High-k HJLTFET shows the highest value of leakage current in comparison to the other two devices, which is the result of higher electric field and drain to channel coupling at the D/C junction.

Fig. 3.4(d) illustrates the comparison plot of current switching ratio, I_{ON}/I_{OFF} of HD-HJLTFET, Low-k HJLTFET, and High-k HJLTFET. As clearly expressed by the **Fig. 3.4(d)**, HD-HJLTFET exhibits the highest I_{ON}/I_{OFF} ratio, which is 1.36 and 4.5 orders higher in magnitude than High-k HJLTFET and Low-k HJLTFET, respectively.

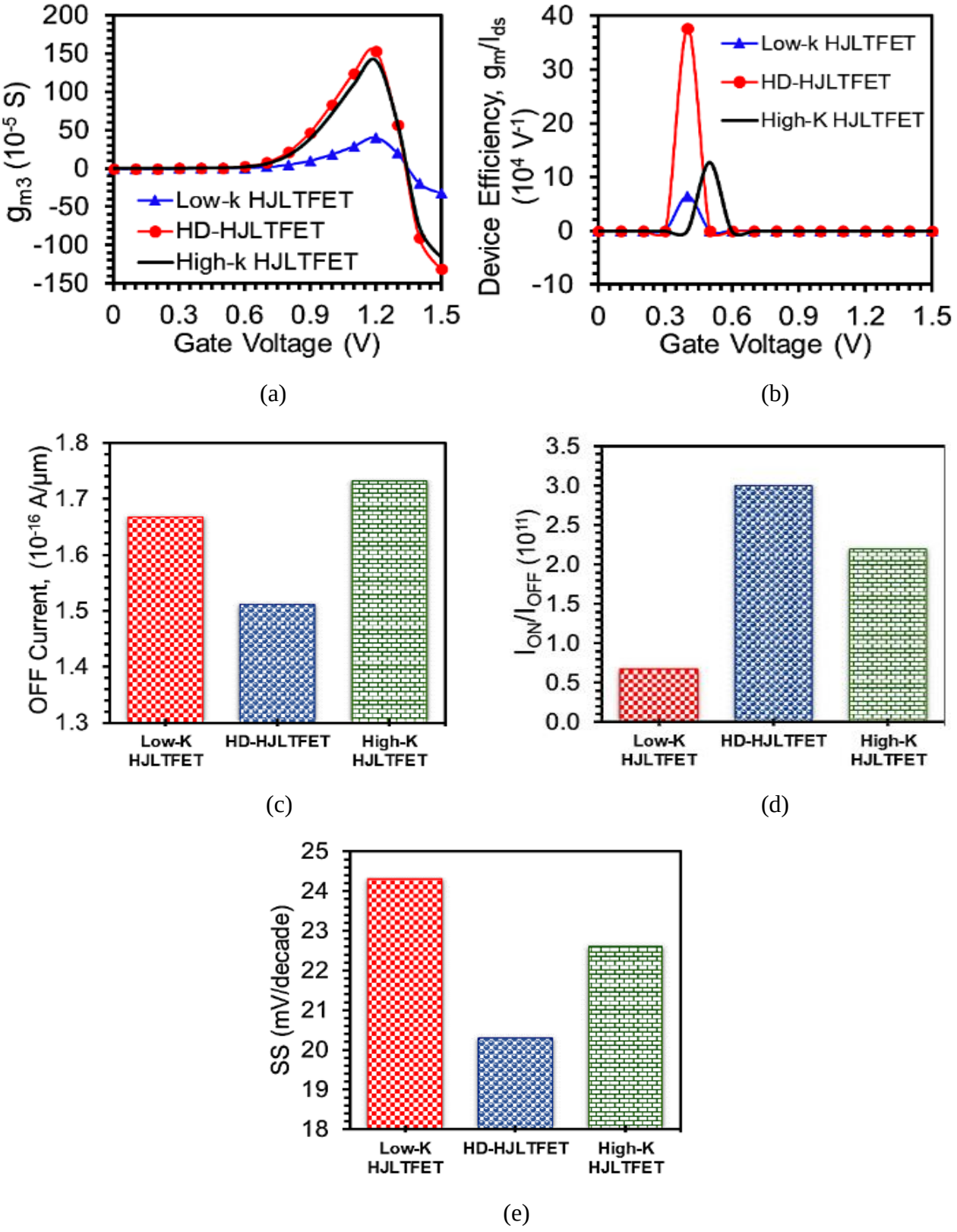

Fig. 3.4. Comparative plot of (a) g_{m3}, (b) Device efficiency, (c) OFF current, (d) Current switching ratio, I_{ON}/I_{OFF}, and (e) SS of HD-HJLTFET compared with Low-k HJLTFET and High-k HJLTFET [22].

In **Fig. 3.4(e)**, HD- HJLTFET shows ~10% and ~16% smaller value of SS as compared to High-k HJLTFET and Low-k HJLTFET, respectively, which is a significant parameter for analog applications of TFET. The optimization of dielectric material for the proposed device is investigated by employing different insulating materials i.e., HfO_2 (k = 25), ZrO_2 (k = 22), Al_2O_3 (k = 9), Si_3N_4 (k = 7), and SiO_2 (k = 3.9), in the high-k region.

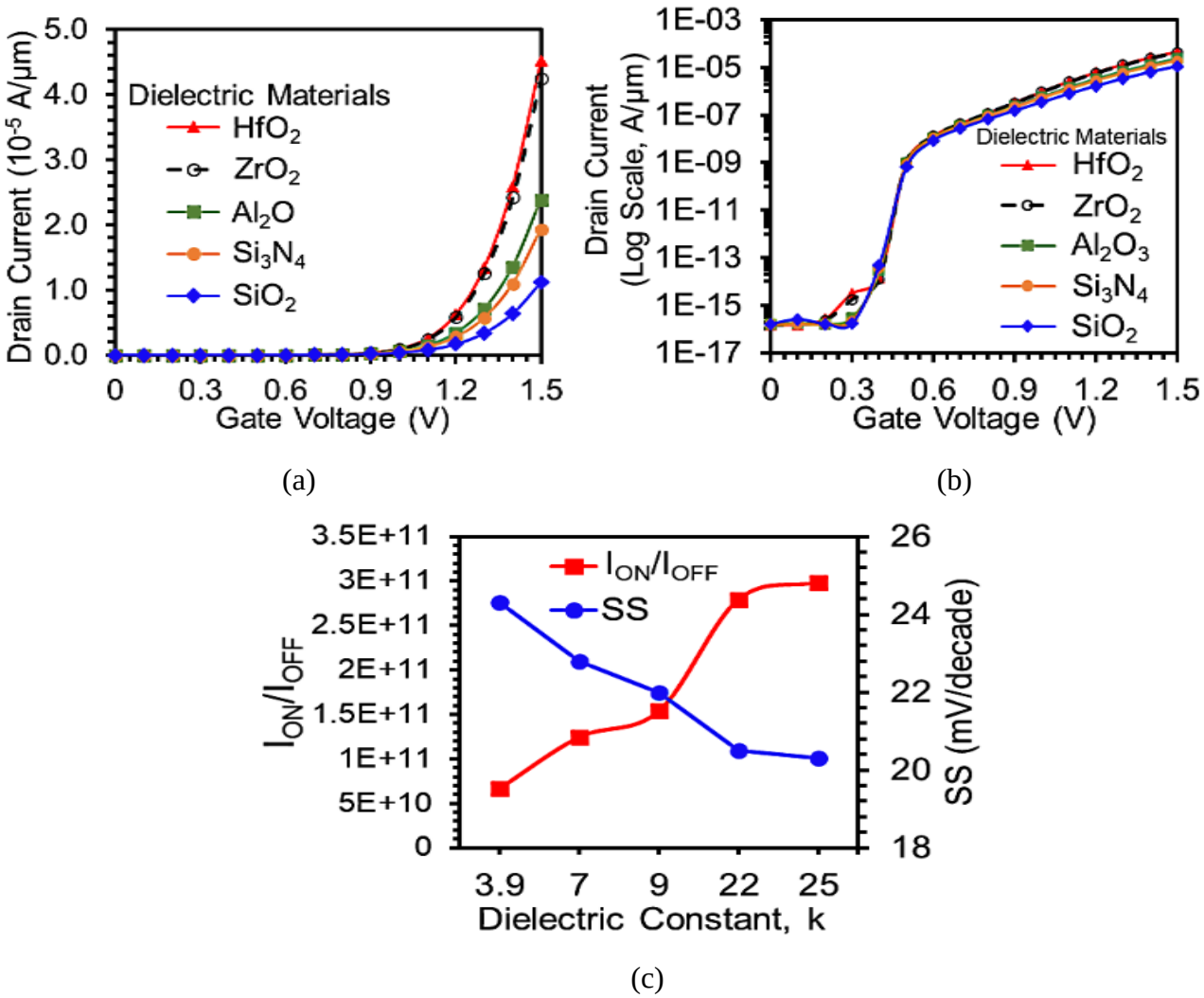

Fig. 3.5. Comparison of Transfer characteristics in (a) Linear scale, (b) Log scale for different dielectric materials, and (c) current switching ratio and SS variation for dielectric materials constants [22].

In **Fig. 3.5(a) and (b)**, the transfer characteristics of HD-HJLTFET for different dielectric materials are illustrated. The results show a marked improvement in the form of ON current on increasing the

dielectric constant of the high-k. HD-HJLTFET with HfO_2 (k = 25) shows the highest value of the ON current which is due to the higher gate coupling provided by the higher dielectric constant material. The physical oxide thickness is kept constant as 2nm throughout the simulations for all the dielectric materials. **Fig. 3.5(c)** displays the comparison plot of current switching ratio and SS as a function of different dielectric materials in the high-k region as mentioned before. For Low-k HJLTFET device (SiO_2, k = 3.9), the I_{ON}/I_{OFF} is least amongst the chosen dielectric materials and on increasing the dielectric constant, k of the high-k region; the I_{ON}/I_{OFF} exhibits positive gradient for HD-HJLTFET. The reason behind such a trend is the increment in the electric field at the S/C intersection below CG owing to the existence of high-k region. The maximum I_{ON}/I_{OFF} is attained for HfO_2 in the range of 3×10^{11}, while I_{ON}/I_{OFF} of SiO_2, k = 3.9 (Low-k HJLTFET), shows the least value of 0.6×10^{11}. So, the optimized dielectric material for the high-k region is HfO_2. In order to optimize HD-HJLTFET, the length of the high-k region, $L_{High\text{-}k}$ has been optimized for high-k dielectric material HfO_2.

Fig. 3.6(a) expresses the transfer characteristics of HD-HJLTFET as a function of gate voltage by varying the length of the high-k region, $L_{High\text{-}k}$. It can be observed that the ON current shows an increasing pattern on reducing the $L_{High\text{-}k}$ from 20 nm to 7 nm, whereas the ON current again decreases for $L_{High\text{-}k}$ = 5 nm. The $L_{High\text{-}k}$ = 20 nm corresponds to High-k HJLTFET, where HfO_2 is located over the whole channel region. **Fig. 3.6(b)** displays the OFF state current variation of HD-HJLTFET as a function of $L_{High\text{-}k}$. The OFF state current starts reducing as the $L_{High\text{-}k}$ is decreased from 20 nm to 10 nm and starts increasing for further reduction in $L_{High\text{-}k}$. The variation of current switching ratio, I_{ON}/I_{OFF} of HD-HJLTFET is presented as a function of $L_{High\text{-}k}$ in **Fig. 3.6(c)**, which shows an upsurging trend of I_{ON}/I_{OFF} ratio with an increment of ~36% on decreasing the $L_{High\text{-}k}$ from 20 nm to 7 nm. The I_{ON}/I_{OFF} ratio starts decreasing as the $L_{High\text{-}k}$ is further reduced to 5 nm.

Fig. 3.6(d) displays the comparison of SS of HD-HJLTFET as a function of $L_{High\text{-}k}$. It is clear from the **Fig. 3.6(d)** that the optimized $L_{High\text{-}k}$ is 7 nm, at which the SS is smallest. The optimization of

$L_{High\text{-}k}$ depends upon the local minimum induced at the conduction band edge of the S/C interface. On reducing $L_{High\text{-}k}$, the conduction band well gets shallower resulting into minor tunneling of electrons. On the contrary, the increment in $L_{High\text{-}k}$ widens the conduction band well leading to poor transition between ON and OFF states. On comparing the results of current switching ratio and SS for $L_{High\text{-}k}$, the length of the high-k stack is optimized to 7 nm.

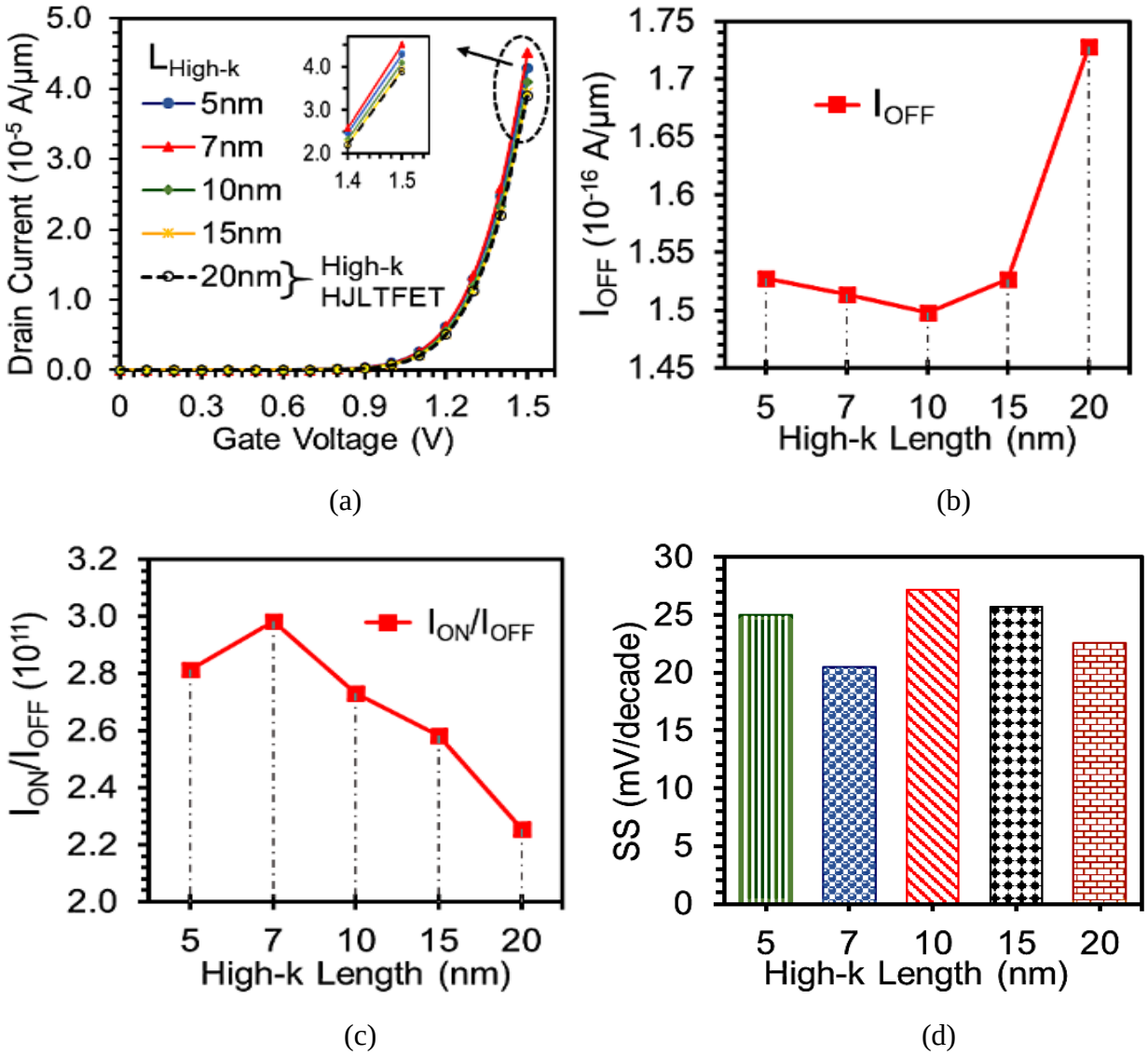

Fig. 3.6. Comparison of (a) Transfer characteristics (b) OFF current, (c) Current switching ratio, I_{ON}/I_{OFF}, and (d) SS of HD-HJLTFET for different high-k gate stack lengths, L_{Stack} [22].

The comparison of result characteristics of HD-HJLTFET with Low-k HJLTFET and high-k HJLTFET is displayed in **Table 3.1**. The HD-HJLTFET attains superior performance in terms of I_{ON}, I_{ON}/I_{OFF} ratio, and SS with comparison to the other two aforementioned devices.

TABLE 3.1

RESULT CHARACTERISTICS OF HD-HJLTFET, LOW-K HJLTFET AND, HIGH-K HJLTFET [22]

	HD-HJLTFET	**Low-k HJLTFET**	**High-k HJLTFET**
I_{ON} (µA/µm)	45.2	11.2	39
I_{OFF} (A/µm)	1.5×10^{-16}	1.6×10^{-16}	1.7×10^{-16}
I_{ON}/I_{OFF}	3×10^{11}	0.6×10^{11}	2.2×10^{11}
SS (mV/decade)	20	24	22

3.4 CONCLUSION

In this chapter, a junctionless TFET with III-V compound semiconducting hetero-materials has been explored using a hetero-gate dielectric having a combination of high-k oxide at the source side and low-k oxide at the drain side. The proposed HD-HJLTFET shows marked improvement as compared to mono-dielectric HJLTFET – High-k HJLTFET and Low-k HJLTFET in terms of I_{ON}, I_{ON}/I_{OFF}, device efficiency, and SS. So, the combination of hetero-dielectric used in the proposed device tends to advance the analog performance of the device, which makes it an appropriate alternative for low power and fast switching applications.

However, developing a hetero-structure TFET using the combination of InAs (binary)-AlGaSb (ternary, in place of GaAs-binary) III-V compound semiconducting materials provides a tunable

bandgap at the S/C interface, where the energy bandgap of ternary material, $Al_xGa_{1-x}Sb$ depends on the Al-mole fraction value (x.composition). The properties of $Al_xGa_{1-x}Sb$ can be modified by changing the x-composition, therefore the device structure can be optimized for best outcomes by using this material in the channel and drain region. The suitability of lattice matched standard III-V growth and processing techniques are the prime reason for choosing these materials [23], which has been discussed in the next chapter.

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CHAPTER-4

PERFORMANCE ENHANCEMENT IN A NOVEL AMALGAMATION OF ARSENIDE/ANTIMONIDE TUNNELING INTERFACE WITH CHARGE PLASMA JUNCTIONLESS-TFET

In this chapter, the binary channel and drain material, GaAs used in **chapter 2** has been replaced by the ternary (AlGaSb) compound semiconducting material. The material is chosen because of the tunable bandgap property, where the bandgap of AlGaSb can be modified by changing the mole fraction of Al to induce a charge plasma based tunable bandgap arsenide/antimonide tunneling S/C interface. The hetero-material JLTFET (H-JLTFET) depicts superior performance than conventional homo-material Si JLTFET in terms of DC characteristics showing ~128 and ~1.27×10^{8} times higher I_{ON} and I_{ON}/I_{OFF} along with ~10^{-6} times, ~50%, and 88% lower I_{OFF}, V_{th}, and SS. The superior performance is attributed to the conduction band local minimum induced at the channel yielding to narrower tunneling barrier width at an optimized Al-mole fraction (0.15) of AlGaSb. Further, 77 times higher g_m of H-JLTFET led to 5×10^{6} and 205 times higher device efficiency and f_T along with ~66% reduction in the parasitic capacitance making it favorable for high-speed switching applications as compared to Si JLTFET.

4.1 INTRODUCTION

The Junctionless TFET proves to be the most promising architecture among the various TFET engineering schemes to resolve various issues like fabrication complexity owing to the presence of doping junctions, which stipulates a higher thermal budget for complex thermal annealing, random dopant fluctuations, and ion implantation. It consolidates the benefits of a junctionless FET (elevated ON-current, I_{ON}) and a TFET (smaller subthreshold swing, SS). The nonexistence of p-n doping junctions also boosts the immunity of TFET towards the short channel effects [1]-[2].

Another key in determining the electrical performance of TFET is the semiconductor material. The Silicon TFET being an indirect semiconductor with a large energy bandgap based homojunction device diminishes the carrier mobility and band to band tunneling probability, and hence the ON state current degrades [2], [3]-[5]. So, to overcome the drawbacks of homojunction-TFETs, the direct bandgap III-V Compound semiconducting materials have been used in past few years. By using a lower and higher bandgap III-V compound semiconducting material in the source and channel, respectively, a heterostructure based junctionless TFET is formed which results into improved electrical performance as compared to homojunction-TFETs [6]-[9]. The application of high-k materials in combination with semiconducting materials and lattice mismatch between two hetero-materials originates the interface trap charges due to trapping of mobile ionic and immobile charges at the semiconductor/oxide and source/channel (S/C) interface, which deteriorates the device reliability and lifetime [10-11].

The researchers have proposed several n-TFET architectures by incorporating hetero-junction arsenide/antimonide tunneling interfaces in history. Lu *et al*. [12], and Li *et al*. [13], achieved remarkable results beating other TFET designs by forming A “T-shape” vertical architecture using an InAs/AlGaSb hetero-junction. The first demonstration of a self-aligned InAs/Alo.45Gao.55Sb heterojunction TFETs has been reported by Zhou. G. *et al*. [14], using an optical-lithography-only.

The InAs/Al0.05Ga0.95Sb based nanowires have been designed using a virtual TFET technology platform by Baravelli *et al*. [15]-[16]. However, the analysis of InAs/AlGaSb hetero-materials have not been explored for the junctionless TFET architecture to the best of our knowledge.

In this chapter, a novel III-V compound semiconducting hetero-materials, InAs/AlGaSb based junctionless TFET (H-JLTFET) has been proposed. The proposed device involved the careful optimization of many key-elements including the source and channel material parameters, hetero-structure junctionless architecture, doping level, and gate length. The hetero-material engineering is incorporated by using lower bandgap InAs in the source and higher bandgap AlGaSb in the channel and drain sections, respectively. Afterwards bandgap engineering is applied by optimizing the Al mole fraction in ternary compound semiconducting material, AlGaSb on the basis of higher I_{ON}, smaller SS, and higher current switching ratio (I_{ON}/I_{OFF}).

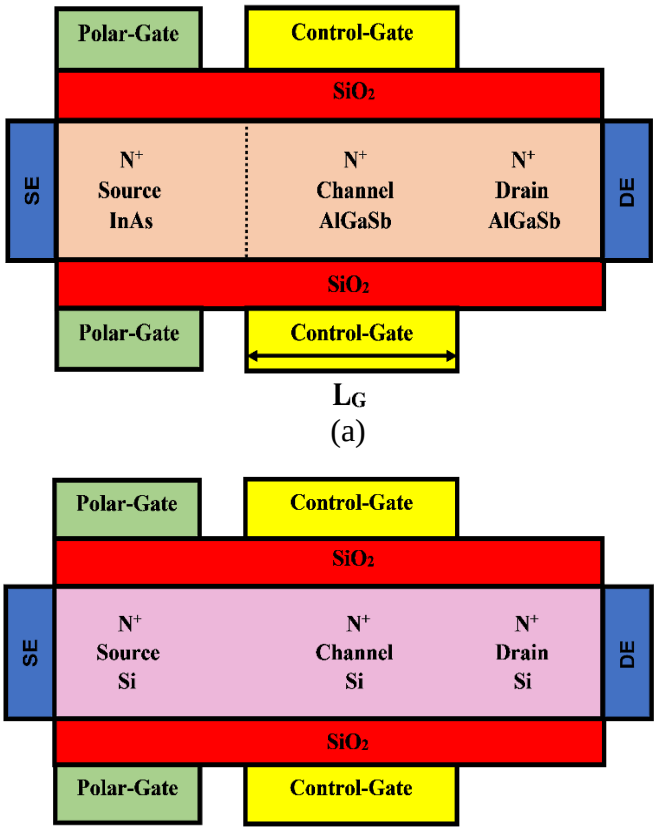


Fig. 4.1. Device architecture of (a) H-JLTFET (InAs-AlGaSb) and (b) JLTFET (Si), [17].

The performance of proposed hetero-material based device, H-JLTFET has been compared with homo-material based JLTFET using Si.

4.2 DEVICE DESIGN

Fig. 4.1 illustrates the architecture of (a) hetero-material (H-JLTFET) and (b) homo-material (JLTFET) junctionless tunnel FETs. The device design parameters are displayed in **Table. 4.1**. The Al mole fraction in AlGaSb is set to 0.15 during the simulations of H-JLTFET device. In both the devices, SiO_2 (k = 3.9), has been used as the dielectric material in the oxide region. The work functions of control gate (CG), polar gate (PG) and other parameters are retained in both devices to make a fair comparison of results. The simulation methodology applied to the device is already discussed in **chapter 2**.

Table 4.1

Device Design Parameters [17]

Parameter	***Symbol***	***Value***
Channel Length	L_G	20nm
Body Thickness	T_{Body}	3nm
Doping Concentration	N_D	$1 \times 10^{19} cm^{-3}$
Oxide thickness	T_{OX}	2nm
Isolation thickness	L_{Gap}	2nm
CG work Function	ϕ_{CG}	4.5eV
PG Work Function	ϕ_{PG}	5.93eV

4.3 RESULTS AND DISCUSSION

In this segment, the impact of III-V compound semiconducting hetero-materials has been examined over the homo-material in junctionless TFET device structure for a supply voltage, V_{GS} = 0.0 V, V_{DS} = 1.5 V for OFF-state, and V_{GS} = 1.5 V and V_{DS} = 1.5 V for ON-state to analyse the analog/RF behaviour of both the devices. The hetero-material incorporated in H-JLTFET gives rise to a tunable bandgap at the source/channel interface (S/C) on applying the band engineering via the use of AlGaSb and InAs material in the channel and source section, respectively. The energy bandgap of ternary material, AlGaSb dependent on the Al-mole fraction (x.comp) is approximated by the function [18], [19]:

$$E_g^{Al_xGa_{1-x}Sb} = \left[x.E_g^{AlSb} + (1-x).E_g^{GaSb} - x.(1-x)C_{Al_xGa_{1-x}Sb}\right], \quad (4.1)$$

Where, $C_{Al_xGa_{1-x}Sb}$ is the bowing factor for energy bandgap for AlGaSb given as below:

$$C_{Al_xGa_{1-x}Sb} = [1.22x - 0.044] \quad (4.2)$$

Fig. 4.2(a) and **(c)** displays the energy diagram of H-JLTFET and JLTFET along the channel direction in the OFF-state and ON-state, respectively. The current conduction in TFET which is controlled by the gate voltage is strongly dependent on the tunneling barrier width; which, further depends on the energy bandgap at the S/C interface. In H-JLTFET, at the hetero-material S/C interface, InAs has the lower energy bandgap as compared to AlGaSb leading to lower tunneling barrier width, which is still higher at the D/C interface due to the presence of homo-material AlGaSb. As shown in **Fig. 4.2(a)**, When no gate biasing is applied (OFF-state), The potential barrier at the S/C interface is elevated enough to restrict the flow of carriers across the junction. In that case, only minor leakage carriers having energy higher than the S/C interface barrier width can tunnel into the channel and get accumulated at the drain node. The magnified view of the **Fig. 4.2(a)** has been added for better clarity of the energy band diagram at the S/C interface for both H-JLTFET and JLTFET.

As shown in **Fig. 4.2(b)**, the conduction band at the drain and valence band at the source are somewhat overlapping each other in the OFF state, however there is no such bands overlapping in case of H-JLTFET. Hence, the tunneling window becomes shorter in case of Si-JLTFET giving rise to higher leakage current. On applying the gate bias (ON-state), the gate electric field modulate the channel so that the conduction band of the channel is pulled down by inducing a local minimum of the conduction band edge at the S/C interface owing to the existence of hetero-material in H-JLTFET, as revealed in **Fig. 4.2(c)**.

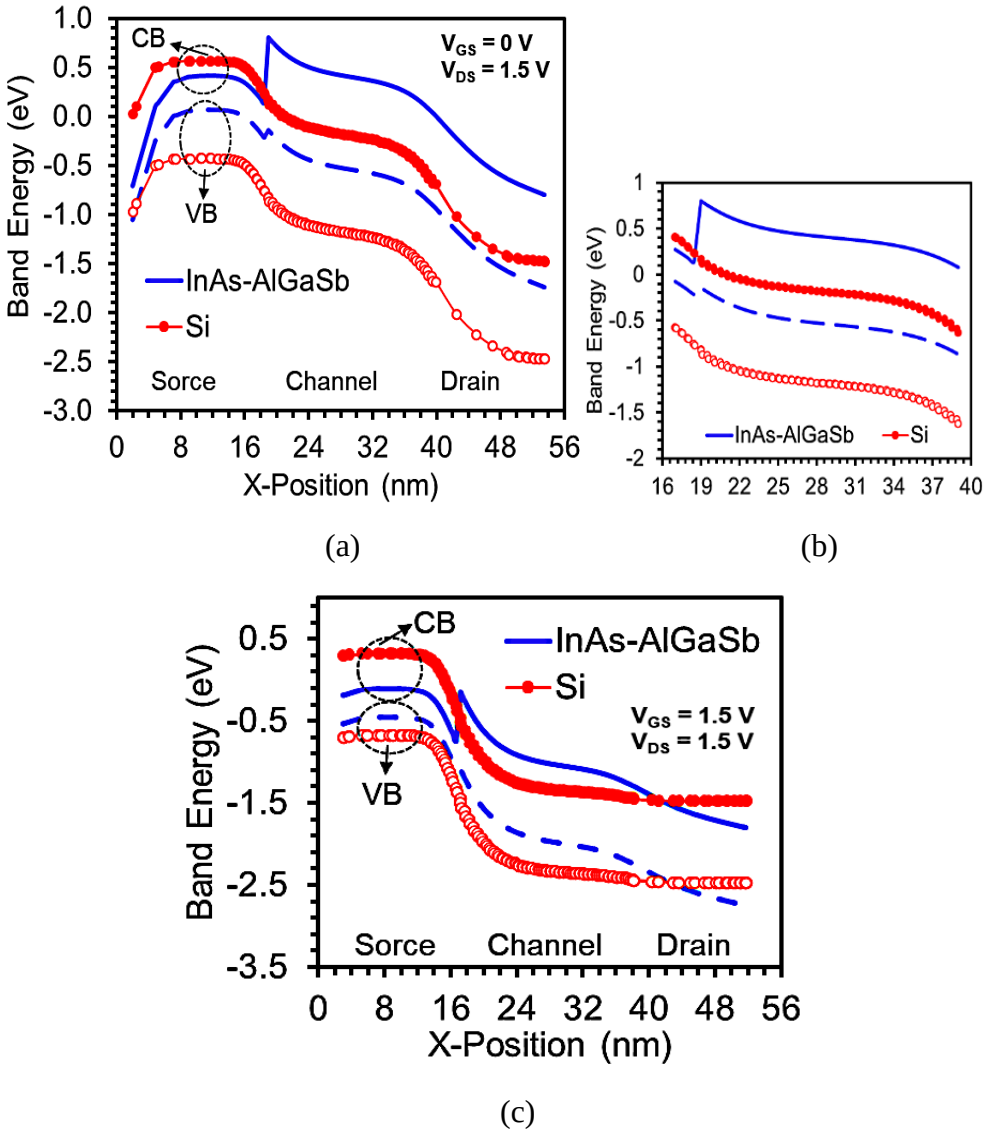
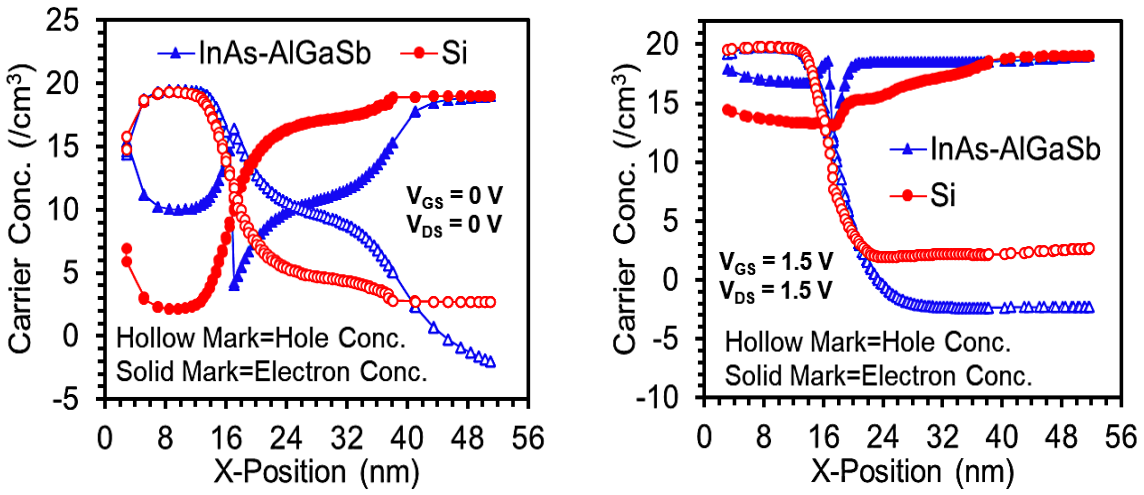


Fig. 4.2. Comparison plots of H-JLTFET and JLTFET for (a) OFF state, (b) magnified view of band bending at the S/C and D/C interface, and (c) ON state energy band diagram [17].

As an outcome, the tunneling barrier width at the S/C interface abruptly diminishes and hence larger number of electrons tunnel through the barrier on account of the dominance of band-to-band tunneling between the local minimum of conduction band of channel and valence band of source. However, the homo-material Si having the higher bandgap at the S/C interface leads to a wider tunneling barrier. As a result, even on applying the gate biasing to JLTFET, lower number of electrons tunnel through the barrier in comparison to H-JLTFET.

When no biasing is applied to the gate and drain, the device is in the thermal equilibrium state. The PG and CG give rise to a p-i-n doped architecture even in the absence of any physical doping in both the device (**Fig. 4.3a**). The higher electron concentration of H-JLTFET as compared to JLTFET at the S/C junction leads to abruptness at the junction. When the gate biasing is applied to CG (**Fig. 4.3b**), the hetero-material S/C junction gives rise to an n-doped pocket region beneath the spacer region between PG and CG in H-JLTFET.



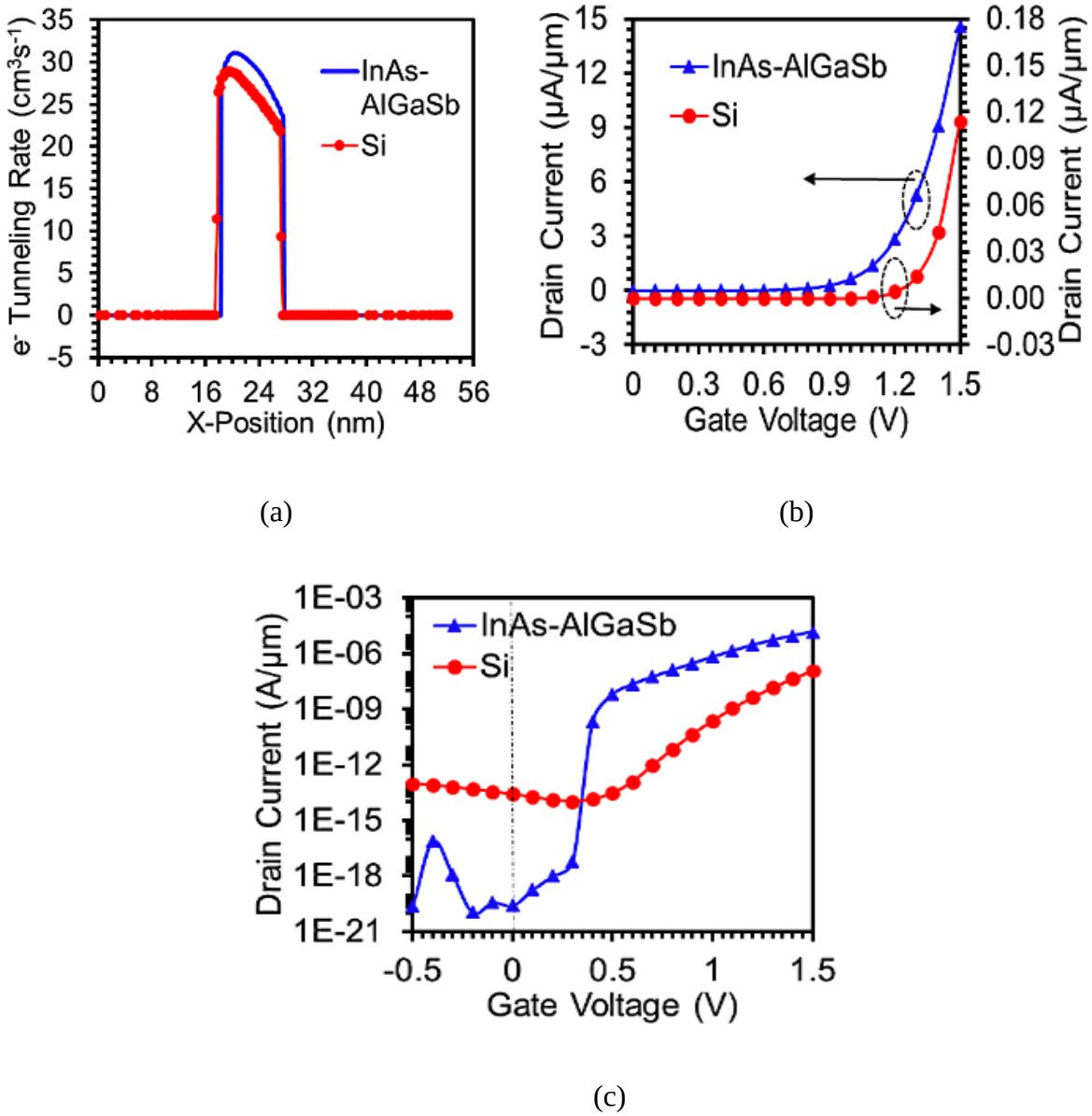
(a) (b)

Fig. 4.3. Comparison plots of H-JLTFET and JLTFET for (a) Thermal equilibrium and (b) ON state carrier concentration [17].

This increment in the electron concentration under the spacer region induces the conduction band local minimum at the S/C interface and hence the tunneling barrier width is narrowed down. The electron concentration in the channel is abrupt in H-JLTFET, while JLTFET has gradual increment in the electron concentration in the channel section.

In **Fig. 4.4(a)**, the abrupt band bending and hence narrow tunneling barrier thickness of H-JLTFET leads to BTBT electron tunneling rate of 7.6% higher than JLTFET. **Fig. 4.4(b)** correlates the linear scale transfer characteristics of the aforementioned devices. As evident from the figure, I_{ON} of H-JLTFET shows higher value than JLTFET. The enhanced I_{ON} of H-JLTFET resulted from the steeper band bending, inducing the conduction band local minimum at the hetero-material S/C interface; whereas low I_{ON} in JLTFET is due to the wider barrier width of the Si homo- material S/C interface that hinders the tunneling rate of electrons. The I_{ON} of hetero-material InAs-AlGaSb (H-JLTFET) device is ~128 orders higher in magnitude than homo-material Si device (JLTFET).

Fig. 4.4(c) compares the transfer characteristics of H-JLTFET and JLTFET in log scale, depicting the comparison of I_{ON}, I_{OFF}, and I_{AMB}. As evident from the characteristics, the I_{OFF} of the proposed hetero-material S/C interface H-JLTFET reduces from an order of 10^{-14} to 10^{-20} as compared to homo-material JLTFET. In OFF state, the CG voltage is at zero and due to the drain biasing, the source/gate electronic potential (ϕ_{CG}) reduces and the drain/gate electronic potential ($\phi_{CG}+V_{DD}$) rises. This leads to the overlapping between the energy bands of the channel and drain. The higher electric field at the D/C junction of JLTFET as compared to H-JLTFET triggers the higher tunneling rate of electrons across the D/C junction leading to higher leakage current. The ambipolar behaviour is also determined at the D/C junction of the TFET as a function of negative gate bias. The ambipolar current of H-JLTFET is also suppressed as compared to JLTFET as a consequence of the wider D/C. The I_{AMB} of H-JLTFET is 2.46×10^{-20} A/µm, whereas JLTFET exhibits I_{AMB} of the order of 9.7×10^{-14} A/µm (**Fig. 4.4c**).



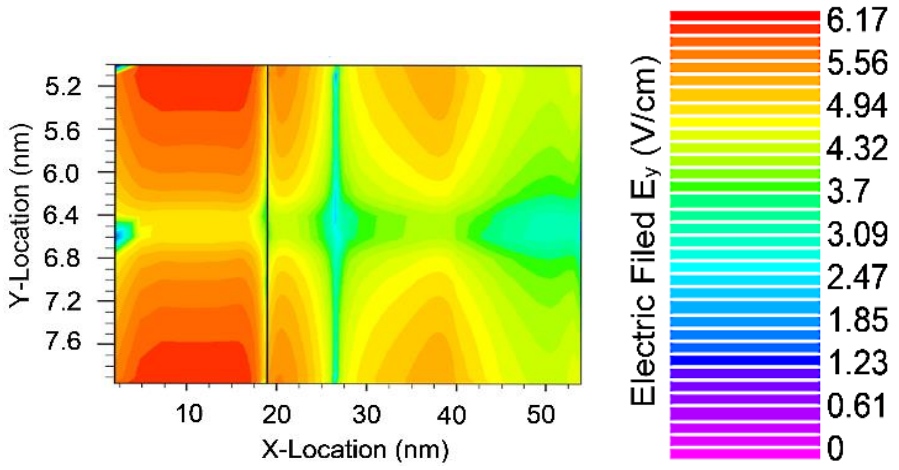
(a) (b)

(c)

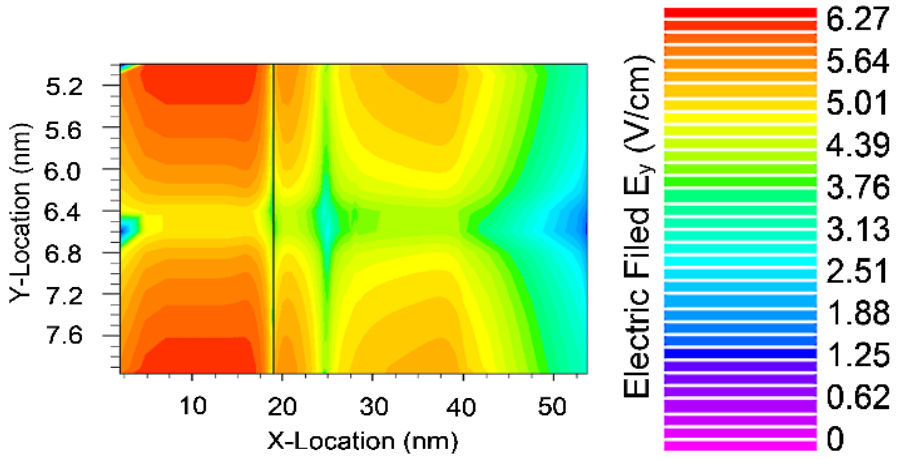
Fig. 4.4. (a) Band to band electron tunneling rate, (b) Transfer characteristics in linear scale, and (c) Transfer characteristics in log scale of H-JLTFET and JLTFET [17].

Fig. 4.5(a) and **(b)** shows the level curve of the normal component of electric field, E_y for H-JLTFET and JLTFET. The higher value of E_y at the interface can limit the performance of the device by increasing the reliability issues such as the gate leakage current and interface trap generation [20]-[21]. However, n-pocket region induced beneath the spacer region by the hetero-material S/C interface in H-JLTFET reduces the peak E_y to ~1.6% as compared to Si JLTFET making H-JLTFET more immune to interface traps and leakage current. The threshold voltage is a crucial parameter

determining the capability of the device to get turned on at the lowest gate voltage possible. The threshold voltage in this work is retrieved by means of V_{GS} @ I_{DS} =10^{-7} A, the constant current method.



(a)



(b)

Fig. 4.5. Normal electric field, E_y contour plot of (a) H-JLTFET and (b) JLTFET along the device length in log scale at V_{GS}=1.5 V, V_{DS}=1.5 V [17].

Fig. 4.6(a) clearly indicates the achievement of lower threshold voltage in H-JLTFET as compared to JLTFET. The threshold voltage of H-JLTFET is about 0.76 V, whereas JLTFET is still in the OFF state at this voltage. The V_{th} of JLTFET is 1.48 V, which is the gate voltage at which the H-JLTFET attains the peak tunneling current. Another essential parameter of determining the device efficiency to shift from the OFF to ON state, is the current switching ratio, I_{ON}/I_{OFF}. Along with I_{ON}/I_{OFF}, SS is a significant factor which defines the capability of the device to shift from OFF to ON state.

Fig. 4.6(b) represents the comparison plot of I_{ON}/I_{OFF} and SS for both the aforementioned devices, where the optimized hetero-materials combination InAs-AlGaSb along with junctionless technology (H-JLTFET) leads to ~1.3 $\times 10^8$ times higher I_{ON}/I_{OFF} and ~88% smaller SS as compared to homo-material Si based device (JLTFET) showing its superiority over JLTFET in making abrupt transition and fast switching speed applications.

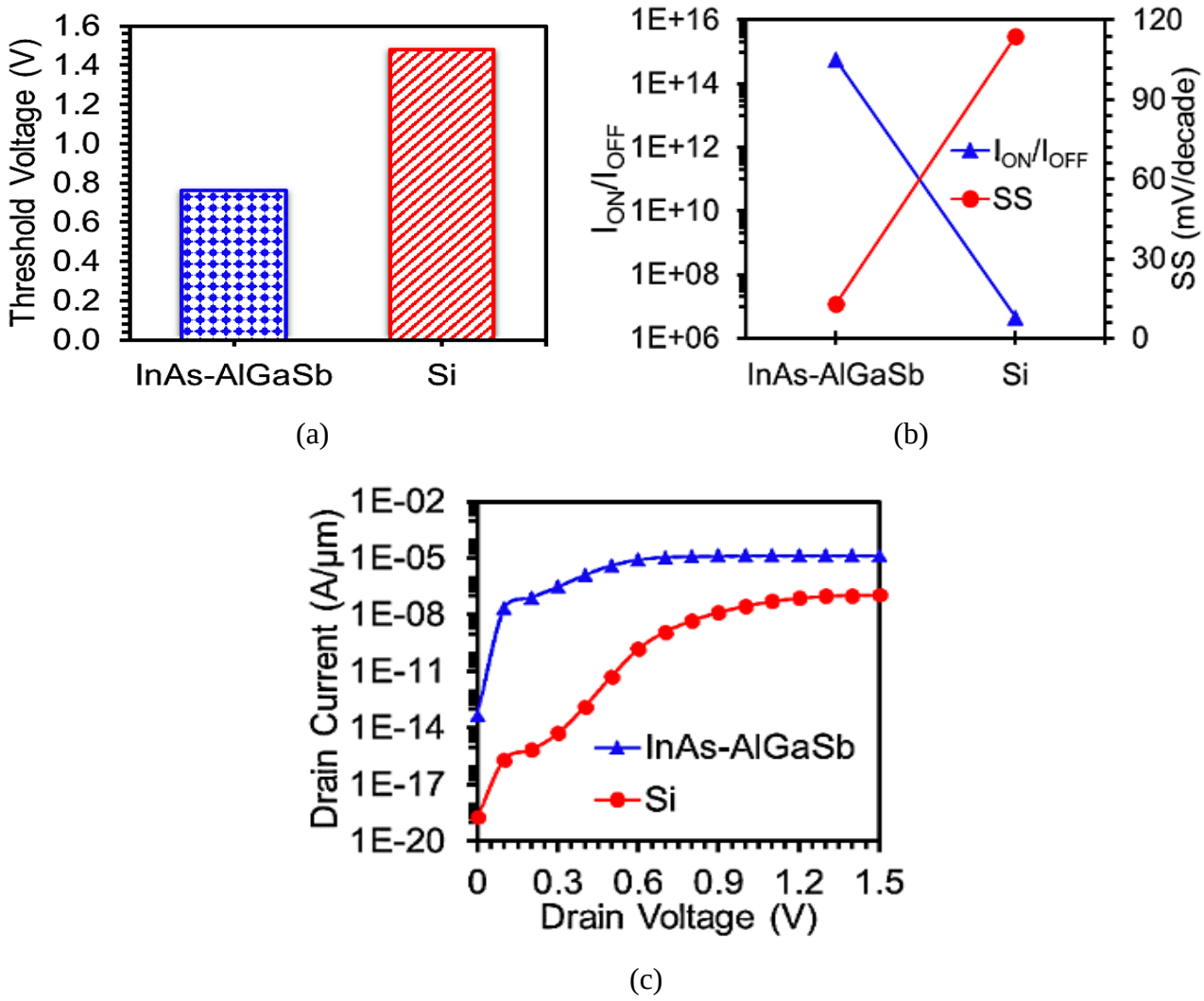
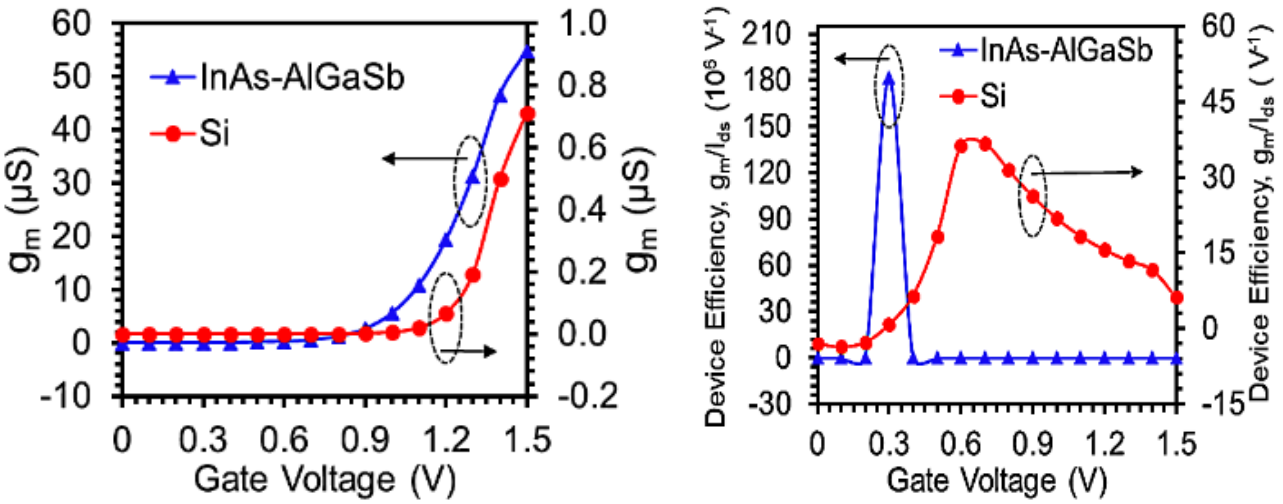


Fig. 4.6. (a) Threshold voltage, (b) I_{ON}/I_{OFF} and SS, and (d) Output characteristics of H-JLTFET and JLTFET [17].

The consequences of wider tunneling barrier and hence inferior tunneling rate of electrons in Si JLTFET results into poor V_{th}, I_{ON}/I_{OFF}, and SS results. The output characteristics of the aforementioned devices for $V_{GS} = 1.5\ V$ are displayed in **Fig. 4.6(c)**. The drain current of H-JLTFET

starts rising for lower value of V_{DS} and after a certain limit, the drain current becomes independent of V_{DS} and finally saturates. The higher tunnel coupling offered by H-JLTFET attributes to an earlier saturation point with higher drain current whereas, JLTFET exhibits lower drain current and later saturation at a higher drain voltage.

In TFETs, the drain current is regulated by the gate voltage, therefore the transconductance, g_m becomes the most crucial factor to determine the analog performance of TFET. It is the ratio of output current to input voltage at constant drain bias, which measures the amplification capability of the device. **Fig. 4.7(a)** displays the disparity of g_m with respect to gate voltage at $V_{DS} = 1.5\ V$ for the aforementioned devices. The g_m variation of H-JLTFET shows significant improvement at lower gate voltage, whereas JLTFET achieves the peak vale of g_m at a larger gate voltage. The g_m peak value of H-JLTFET is ~77 times higher as that of JLTFET implying a better voltage to current conversion rate. The hetero-material (InAs-AlGaSb) S/C interface applied in H-JLTFET initiates the abrupt upsurge in the output current at lower input voltage, which leads to a higher g_m and hence higher gain. For high-frequency RF applications, the parasitic capacitances associated with the device should be minimum in order to minimize its effect on the power dissipation and switching speed of the device. The increment in parasitic capacitances influence the signal distortion and circuit oscillations by creating a path between the input and output nodes of the device. Further, **Fig. 4.7(b)** displays the comparison plot of device efficiency also called as transconductance generation factor (TGF) of two aforementioned devices as a function of gate voltage. TGF is the ratio of transconductance to drain current, which measures the efficiency of converting DC parameter (I_d) into AC parameters (g_m). The H-JLTFET achieves a significantly higher device efficiency of 181 MV^{-1} at a lower gate voltage of 0.3 V, whereas, JLTFET achieves maximum of 36 V^{-1} at 0.6 V. The additional increase in gate voltage results into a fall in TGF due to the dominance of drain current over g_m.



(a) (b)

Fig. 4.7. (a) Transconductance, g_m and (b) Device efficiency of H-JLTFET and JLTFET at constant drain bias V_{DS} = 1.5 V [17].

Fig. 4.8(a) and **(b)** represents the comparison plot of H-JLTFET and JLTFET for parasitic capacitances, C_{gs} (gate to source) and C_{gd} (gate to drain capacitance) at V_{DS}=1.5 V. A small signal AC analysis is performed at a frequency of 1THz to obtain the parasitic capacitances. In **Fig. 4.8(a)**, C_{gs} of both devices initially decreases with an increment in V_{GS} upto 0.4 V and then upsurges as soon as V_{GS} rises above 0.4 V. The upsurging trend of both devices is because of the inter-gate capacitance delivered by PG over the source region. However, H-JLTFET achieves a lower value of C_{gs} upto a certain gate voltage and then, it marginally increases at higher gate voltage. By virtue of widening of inversion layer from drain to source, the coupling between source and gate is reduced. Since the inversion layer is formed from the drain to the source, so the C_{gd} shows a dominating trend over C_{gs} with an increasing gate voltage (**Fig. 4.8b**). Due to the reverse biased S/C junction in TFETs, the potential drop across this junction is quite larger than the D/C junction. Thus, the C_{gd} is much higher than C_{gs} as a result of charge decoupling at the source due to larger potential drop at S/C junction. The H-JLTFET attains much lower value of C_{gd} in comparison to JLTFET as revealed in **Fig. 4.8(b)** owing to the wider potential barrier at the D/C junction. The C_{gd} of H-JLTFET is approximately 66%

smaller as compared to JLTFET for V_{GS} = 1.5 V. Another important parameter determining the switching speed of the device is cut off frequency f_T at which the current gain becomes **unity (Fig. 4.8c**).

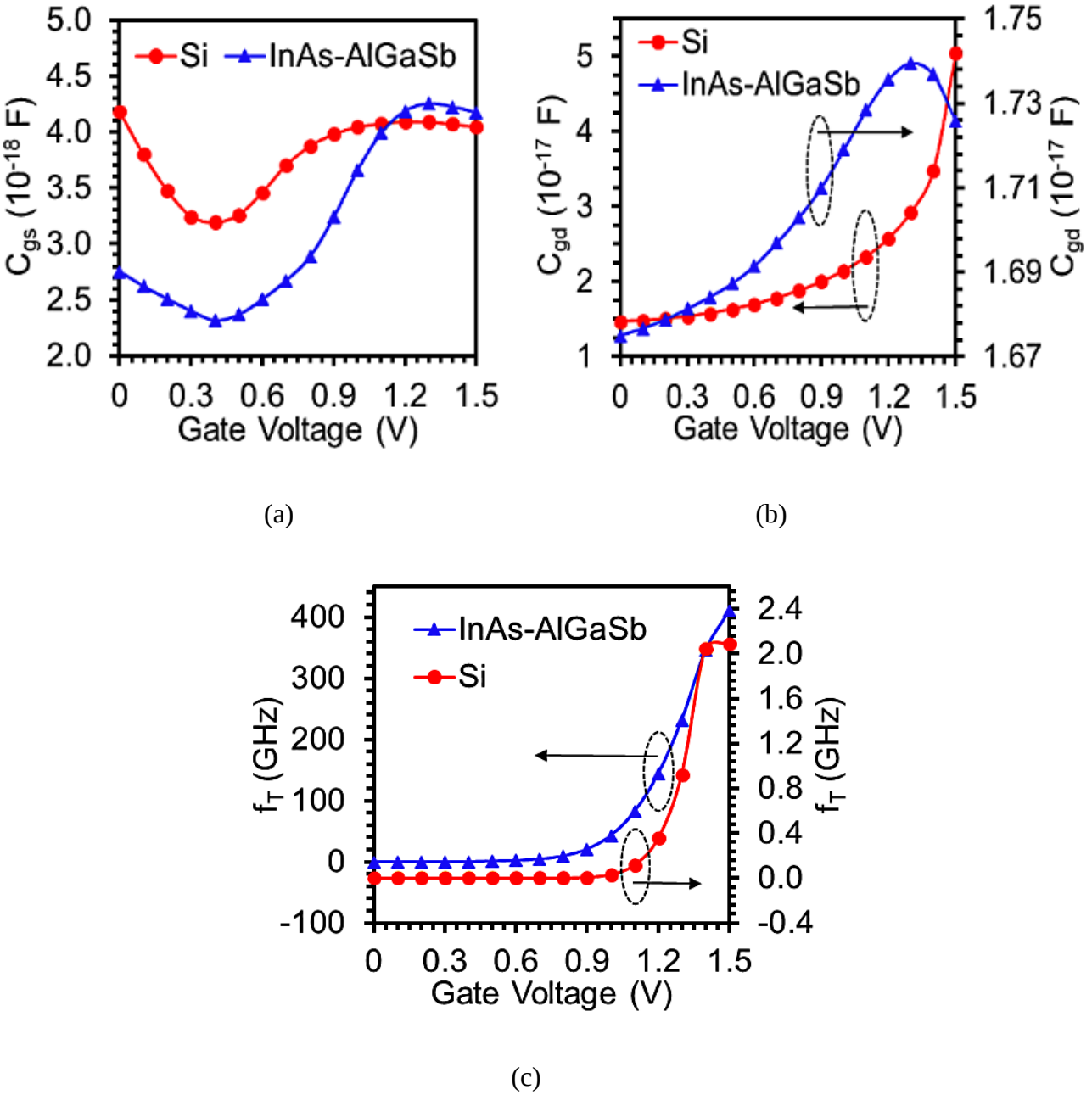


Fig. 4.8. Comparative plot of (a) C_{gs}, (b) C_{gd}, and (c) f_T as a function of gate voltage for H-JLTFET and JLTFET at constant drain bias V_{DS} = 1.5 V [17].

It is directly proportional to g_m and inversely to the parasitic capacitances [22], as given by **eqn (2.1) in chapter 2**. Hence, it is inferred that f_T is degraded by the higher parasitic capacitances. The peak value of f_T is 410 GHz and 2 GHz for H-JLTFET and JLTFET, respectively as shown in **Fig. 4.8(c)**. The 205 times elevated value of f_T due to the amalgamation of hetero-materials at the S/C interface in H-JLTFET makes it clear that f_T is dominated by g_m indicating the negligible dependence on parasitic capacitances.

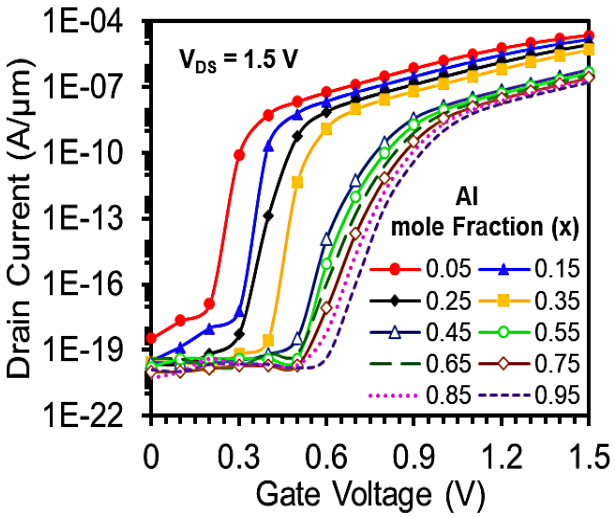


Fig. 4.9. Turn-on characteristics of H-JLTFET for different Al-mole fraction (x-component) in $Al_xGa_{1-x}Sb$ as channel [17].

In **Fig. 4.9**, the impact of Al-mole fraction in $Al_xGa_{1-x}Sb$ has been illustrated in the form of transfer characteristics of H-JLTFET by varying the Al-mole fraction from 0.05 to 0.95. For an optimized device response, the Al-mole fraction in the channel and drain region plays a vital role. It is apparent from the figure that with a rise in the x-comp. of Al, the I_{ON} of H-JLTFET starts decreasing along with an increment in I_{OFF} due to the enlarged bandgap at hetero-S/C interface, which degrades the current switching ratio and SS of H-JLTFET. The x-comp. of 0.15 gives the best outcomes in terms of I_{ON}/I_{OFF} and SS making it suitable for high-speed switching applications. The result characteristics (I_{ON}/I_{OFF} ratio and SS) have been extracted by scaling down the channel length of H-JLTFET from 20 nm 10 nm to analyse the impact of channel length scaling on device performance as shown in

Fig.4.10. The scaling of channel length in H-JLTFET from 20 nm to 10 nm leads to reduction in the tunneling barrier width at the S/C interface and hence the OFF state current increases from the order of 10^{-20} to 10^{-11} A/µm. Hence, the H-JLTFET shows performance degradation on scaling down the channel length from 20 nm to 10 nm, however, the current switching ratio and SS shows negligible change for channel length scaling from 20 nm to 15 nm.

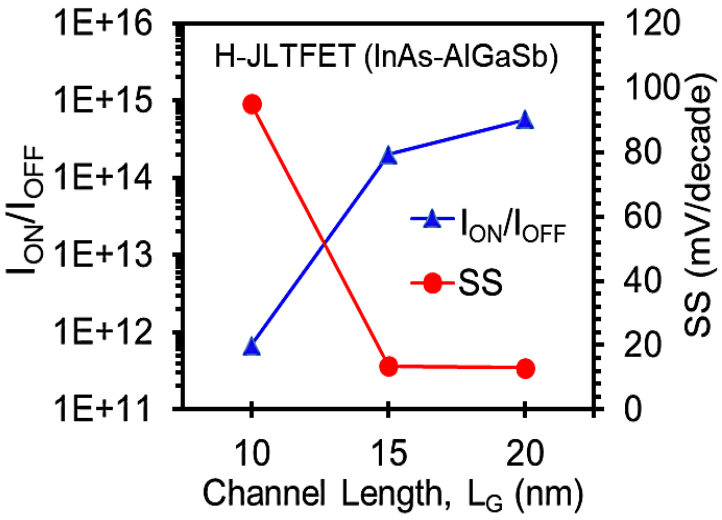
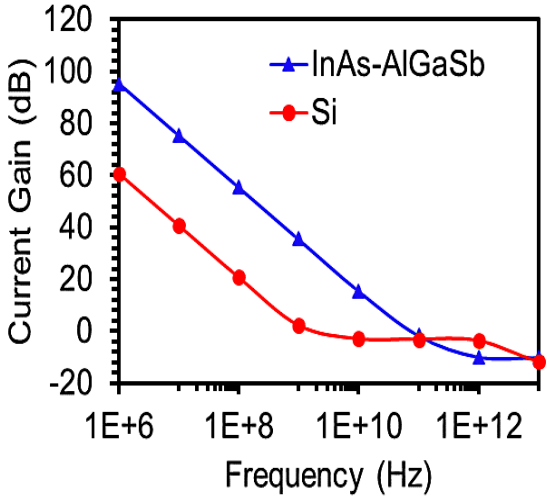
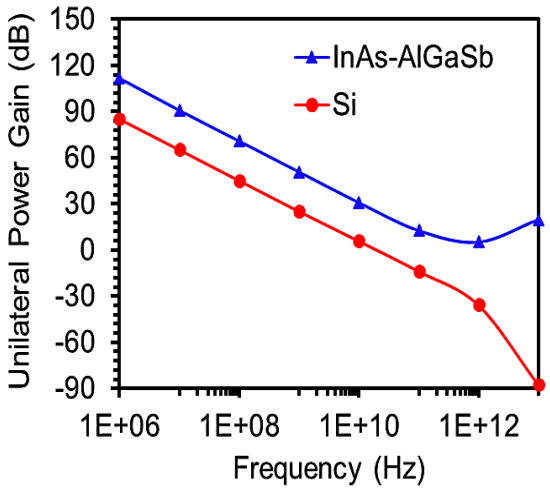


Fig. 4.10. Impact of channel length scaling on Current switching ratio, I_{ON}/I_{OFF} and SS of H-JLTFET [17].

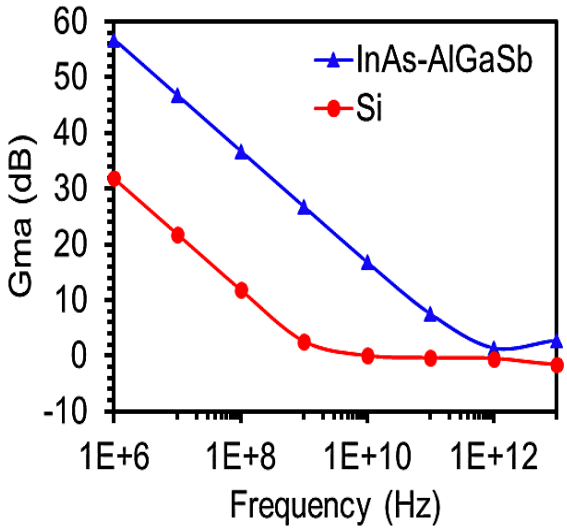
To study the feasibility of HJLTFET over JLTFET in high frequency applications, the variation of current gain, unilateral power gain, and maximum available power gain (Gma) have been displayed in **Fig. 4.11(a-c)**. The application of hetero-material InAs-AlGaSb leads to higher current gain and unilateral power gain than homo-material Si (**Fig. 4.11a-b**). The higher current gain and unilateral power gain in HJLTFET is attributed to the higher I_{ON} and I_{ON}/I_{OFF}. The HJLTFET attains 1.6 (1.8) times higher current gain (unilateral power gain) than JLTFET. In **Fig. 4.11(c)**, the HJLTFET attains 1.3 times higher Gma as compared to JLTFET signifying the application of HJLTFET in designing of low noise amplifiers over conventional JLTFET.



(a)



(b)



(c)

Fig. 4.11. (a) Current gain, (b) Unilateral power gain, and (c) Maximum available power gain (Gma) of HJLTFET and JLTFET [17].

In small signal equivalent circuit, the study of small signal parameters (addmitance parameters) becomes necessary as the MOSFET can be replaced by Y-parameters - Y_{11}, Y_{12}, Y_{21}, and Y_{22}. In non-quasi static approach, all the information regarding the RF FOMs can be extracted directly from the real and imaginary components of Y parameters [22]. **Fig. 4.12(a-d)** demonstrates the variation of

real and imginary components of the Y parameters with respect to frequency. In **Fig. 4.12(a)** and **4.12(d)**, the Y_{11} and Y_{22} attain smaller values at smaller frequency and increases steadily as the frequency rises. Moreover, the variation of Y_{11} and Y_{22} in HJLTFET is lower in magnitude as compared to JLTFET.

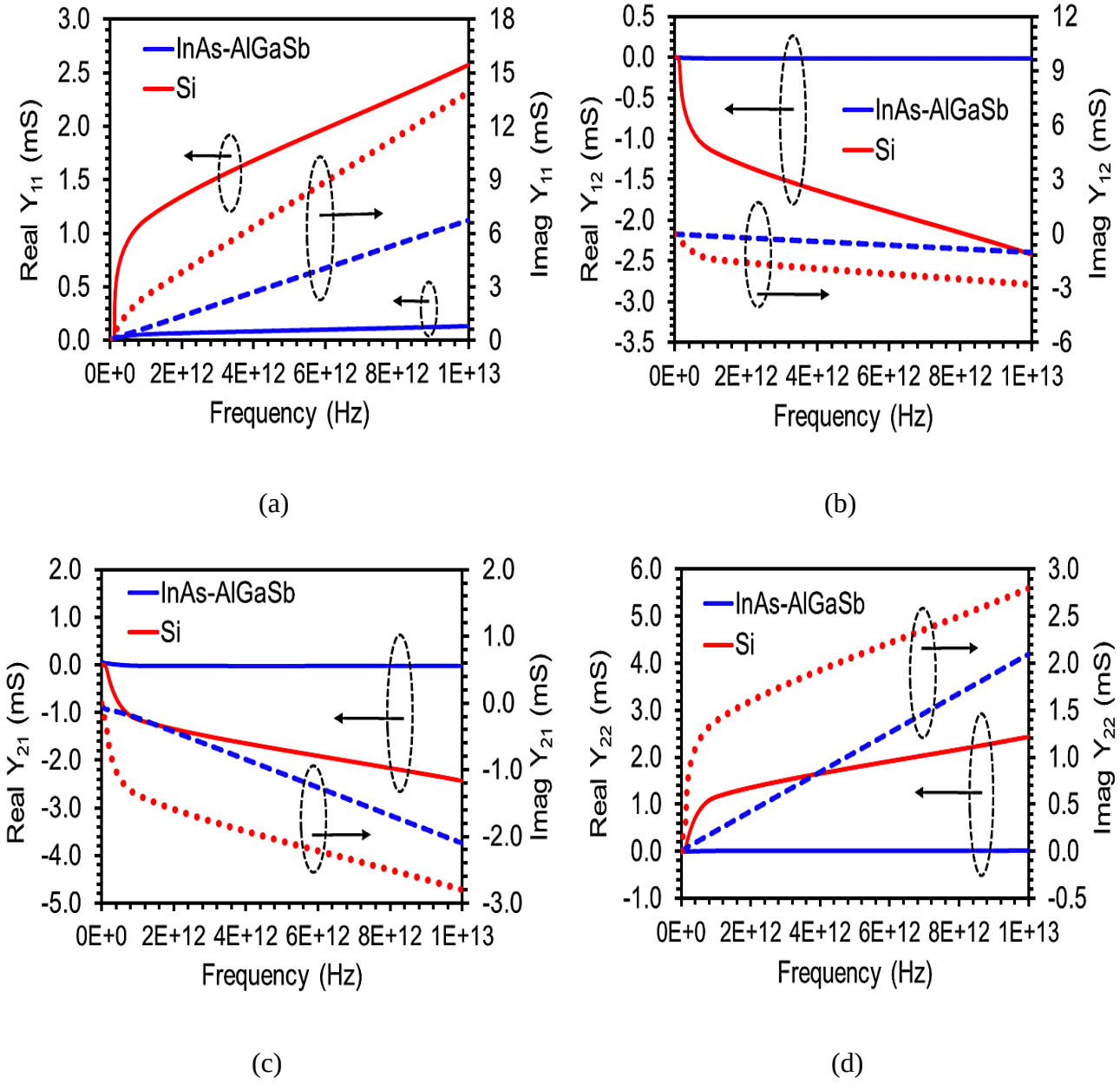


Fig. 4.12. The Variation of real and imaginary components of the admittance (Y) parameters: (a) Y_{11}, (b) Y_{12}, (c) Y_{21}, and (d) Y_{22} as a function of frequency for HJLTFET and JLTFET [17].

In **Fig. 4.12(b)** and **4.12(c)**, the Y_{12} and Y_{21} attains greater values at smaller frequency and declines steadily with rise in frequency for both HJLTFET and JLTFET. However, the magnitude of variation is higher in case of JLTFET as compared to HJLTFET showing better reliability of HJLTFET in terms of small signal parameters and RF applications as compared to JLTFET. The proposed device, H-JLTFET shows appreciable improvement in the form of analog FOMs in comparison to conventional Si-JLTFET and recently published junctionless TFET designs in the literature as mentioned in **Table 4.2**.

Table 4.2

Comparison of Result Characteristics of present work with previously published TFET designs [17]

	DG-HJ-JLTFET [14]	**H-JLTFET [23]**	**H-JLTFET (Present work)**	**Conv. Si-JLTFET (Present work)**
I_{ON} (µA/µm)	~ 1.0	6.0	14.5	0.11
I_{OFF} (A/µm)	$\sim 1.0 \times 10^{-11}$	1.72×10^{-18}	2.57×10^{-20}	2.56×10^{-14}
I_{ON}/I_{OFF}	1.0×10^{5}	2.3×10^{12}	5.67×10^{14}	4.41×10^{6}
SS (mV/decade)	42	> 60	13.2	114.3
g_m (µS)	-	5.5	54	0.71
f_T (GHz)	-	-	410	2.09

4.4 CONCLUSION

In this chapter, for the first time a hetero-material combination of a binary and ternary compound semiconducting material, InAs-$Al_{0.15}Ga_{0.85}Sb$ has been reported for a charge plasma based double gate junctionless TFET by incorporating tunable bandgap engineering at the S/C interface. The analog FOMs revealed that H-JLTFET is a better candidate in comparison to conventional Si based JLTFET. As an outcome of the narrower barrier width at the S/C interface, H-JLTFET achieves the highest I_{ON} and I_{ON}/I_{OFF} as ~14 µA/µm and $\sim 10^{14}$, which is ~128 and $\sim 1.27 \times 10^{8}$ orders higher in magnitude than

JLTFET, respectively. The III-V group hetero-material S/C interface reduces the V_{th} and SS by ~50% and ~88% as compared to JLTFET, respectively. Further, the wider potential barrier at D/C interface of H-JLTFET suppresses the I_{OFF} and I_{AMB} from an order of 10^{-14} to 10^{-20}. Additionally, the InAs-AlGaSb hetero-material interface reduces the parasitic capacitance to ~66% as compared to Si homo-material JLTFET. Also, f_T of H-JLTFET is enhanced to 205 times as that of Si JLTFET. The small signal parameters extraction in terms of Y-parameters and power gains show improved results on the implementation of hetero-material InAs/AlGaSb in HJLTFET as compared to JLTFET. Thus, hetero-material InAs-AlGaSb junctionless TFET can be considered as an appropriate replacement of conventional homo-material Si JLTFET for RF communications and high frequency applications.

Various factors like pressure, temperature, and other transient stresses are considered to be the key factors affecting the reliability of the electronic devices over the lifetime. However, the interface trap charges (ITCs) at the semiconductor/oxide interface originating during the fabrication process of electronic device plays an important role in reliability issues. In real environment, a higher number of positive and negative ITCs develop at the Si-SiO_2 interface while fabricating the device. These ITCs strongly affect the reliability of the device. Therefore, the impact of ITCs polarity and density has been examined in next chapter to study the reliability of HJLTFET in terms of analog/RF and linearity parameters.

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CHAPTER-5

INTERFACIAL CHARGE ASSOCIATED RELIABILITY IMPROVEMENT IN ARSENIDE/ANTIMONIDE TUNNELING INTERFACED-JUNCTIONLESS TFET.

This chapter investigates the reliability improvement in the arsenide/antimonide tunable bandgap tunnelling interface based junctionless TFET device (HD-HJLTFET) by the introduction of positive (donor) and negative (acceptor) localized interfacial trap charges at the semiconductor/oxide (S/O) and semiconductor/semiconductor (S/S) interfaces. In this chapter, the hetero dielectric engineering has been implemented in device discussed in **chapter 4** to improve its immunity in terms of performance variation with different ITCs polarity compared to low-k dielectric device (HJLTFET). The high-k dielectric towards source to channel (S/C) interface and low-k dielectric towards drain to channel (D/C) interface enhances performance of HD-HJLTFET in terms of ON current (~162% ↑), transconductance (~90% ↑), intrinsic gain (~13% ↑), cut-off frequency (~98% ↑), g_{m2} (~28% ↓), and g_{m3} (~1022% ↓) as compared to HJLTFET. The linearity parameters of HD-HJLTFET (VIP2, VIP3, IIP3, 1dB compression point, and IMD3) also showed marked improvement with negligible variation against different ITC polarity than its counter device, making it more reliable for low power microwave and distortion-free wireless communication systems.

5.1 INTRODUCTION

The interface trap charges (ITCs) are originated during the fabrication of nanoscale devices due to trapping of mobile ionic and immobile charges at the semiconductor/oxide (S/O) interface. The damages induced by the fabrication process, stress, and radiation originate these ITCs, which deteriorates the device reliability and lifetime [1]-[5]. The ITCs are generally of donor and acceptor type. The donor traps position exists over the valence band, whereas acceptor traps exist beneath the conduction band. In TFETs, a stronger transverse electric field at the tunneling interface plays a vital role in lowering the tunneling barrier thickness; however, it also leads to the generation of ITCs, which weakens the electric field in the channel region According to the relation: BTBT rate $\propto \exp(-A/E_y)^6$, this weak electric field degrades BTBT rate and hence, affecting the tunneling current at the source/channel (S/C) tunneling interface, which dampens the device performance. Apart from higher electric field, other aggravating elements in ITCs generation are stress induced due to hot carriers and positive bias temperature instability [6].

In hetero-TFET proposed by Sant et al. [7], the ITCs degrade the SS due to weak gate and drain coupling. The effect of ITCs on suppression of ambipolarity of nanowire TFET has been studied to a limited extent by Beneventi et al. [8]. Jaya et al. [9] investigated the cylindrical PNIN-GAA-TFET reliability issues on the application of ITCs. Gupta et al. [10] studied the impact of ITCs on Si-based junctionless TFET. Although several InAs/AlGaSb based hetero-junction TFET structures like "T-shape" vertical TFET [11]-[12], self-aligned InAs/AlGaSb hetero-junction TFETs [13], and InAs/AlGaSb based nanowires [14]-[15] have been fabricated in the recent years, however, the impact of ITCs has not been explored for InAs/AlGaSb hetero-material based charge plasma junctionless TFET architecture.

In this chapter, for the first time, a novel amalgamation of charge plasma junctionless TFET and compound semiconducting hetero-material InAs/AlGaSb along with heterogeneous gate dielectric

has been explored to examine the consequences of ITCs on the reliability of heterogeneous gate dielectric-hetero-material junctionless TFET (HD-HJLTFET). The heterogeneous dielectric has been added to strengthen the device's immunity against ITCs, and results are compared with low-k dielectric based hetero-material junctionless TFET (HJLTFET) in the form of DC, analog/RF, and linearity.

5.2 DEVICE DESIGN AND SIMULATION

The simulation architecture of HD-HJLTFET is displayed in **Fig. 5.1(a)**. The architecture of both devices (HJLTFET and HD-HJLTFET) is a lateral n-type junctionless TFET with doping concentration fixed at 1×10^{19} cm^{-3}. It consists of a control gate (CG) and polarity gate (PG) with a work function of 4.5 eV and 5.93 eV to induce intrinsic channel and p^+ source. The isolation thickness between CG and PG is kept at 2 nm. The existence of this isolation gap between PG and CG to isolate two gates from each other limits the tunnel barrier narrowing at the S/C interface in JLTFET. The reduction of isolation gap leads to enhancement of ON current and SS, however the parasitic capacitances increase due to the increased vicinity of two gate electrodes. This gives rise to the power dissipation [16]. Therefore, optimum isolation thickness is required for performance improvement of JLTFET devices. This issue can be resolved by incorporating compound semiconducting hetero-material bandgap engineering at the S/C interface of JLTFET. The tunable bandgap leads to tunnel barrier lowering at the S/C interface and hence the tunnelling probability of the carriers increases leading to higher ON current [17]. The channel length, oxide thickness, and body thickness are taken as 20 nm, 2 nm, and 3 nm, respectively (discussed in **chapter 5**). The oxide region in HD-HJLTFET consists of two parts – HfO_2 (ε_2 = 24) near the source and SiO_2 (ε_1 = 3.9) near the drain, whereas HJLTFET comprises of only one oxide region i.e., SiO_2 ($\varepsilon_1 = \varepsilon_2$ = 3.9).

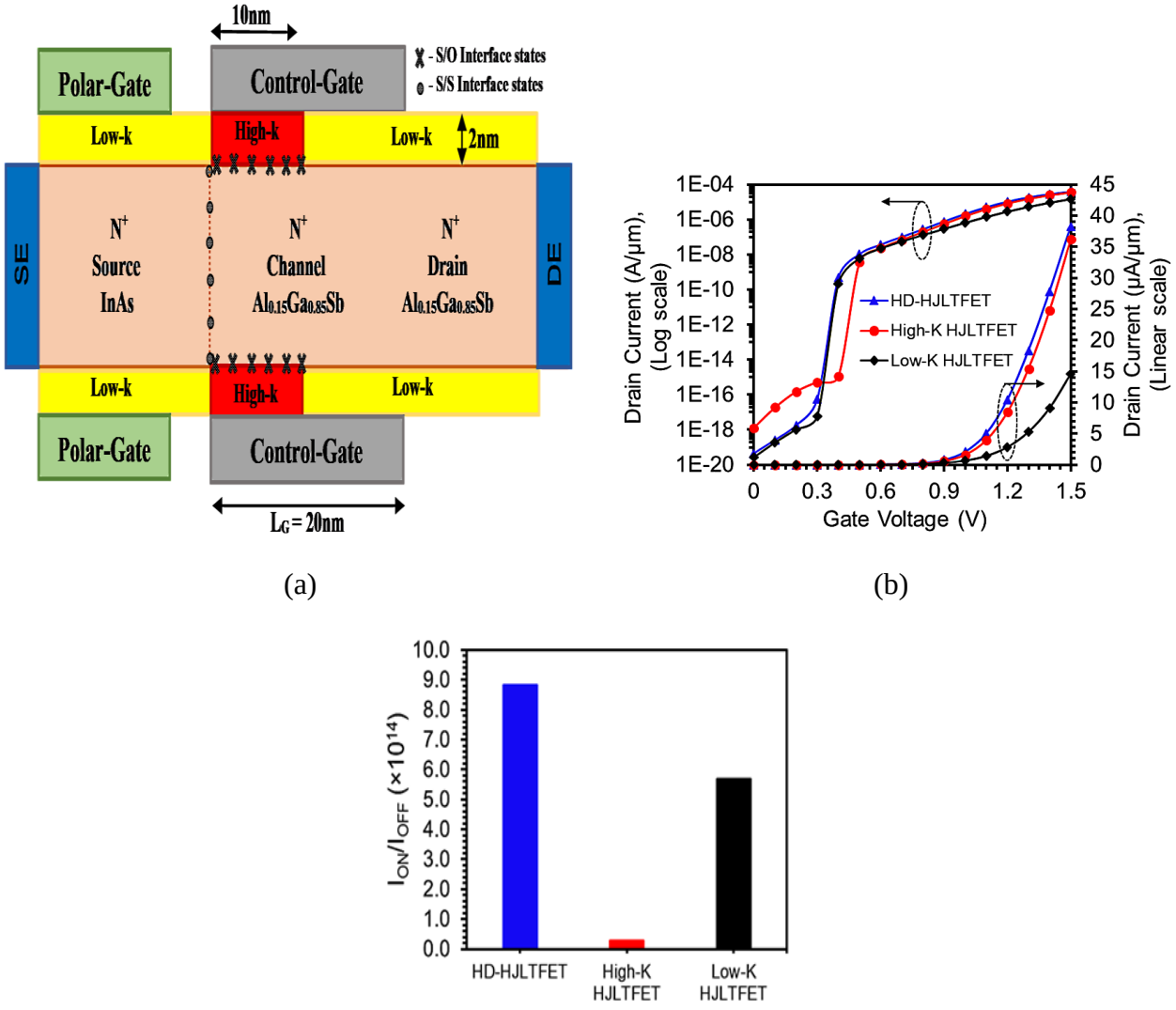


Fig. 5.1. Device architecture of (a) HD-HJLTFET (InAs-AlGaSb) (b) Transfer characteristsics, and (c) Current switching ratio of HD-HJLTFET, High-K HJLTFET and Low-K HJLTFET.

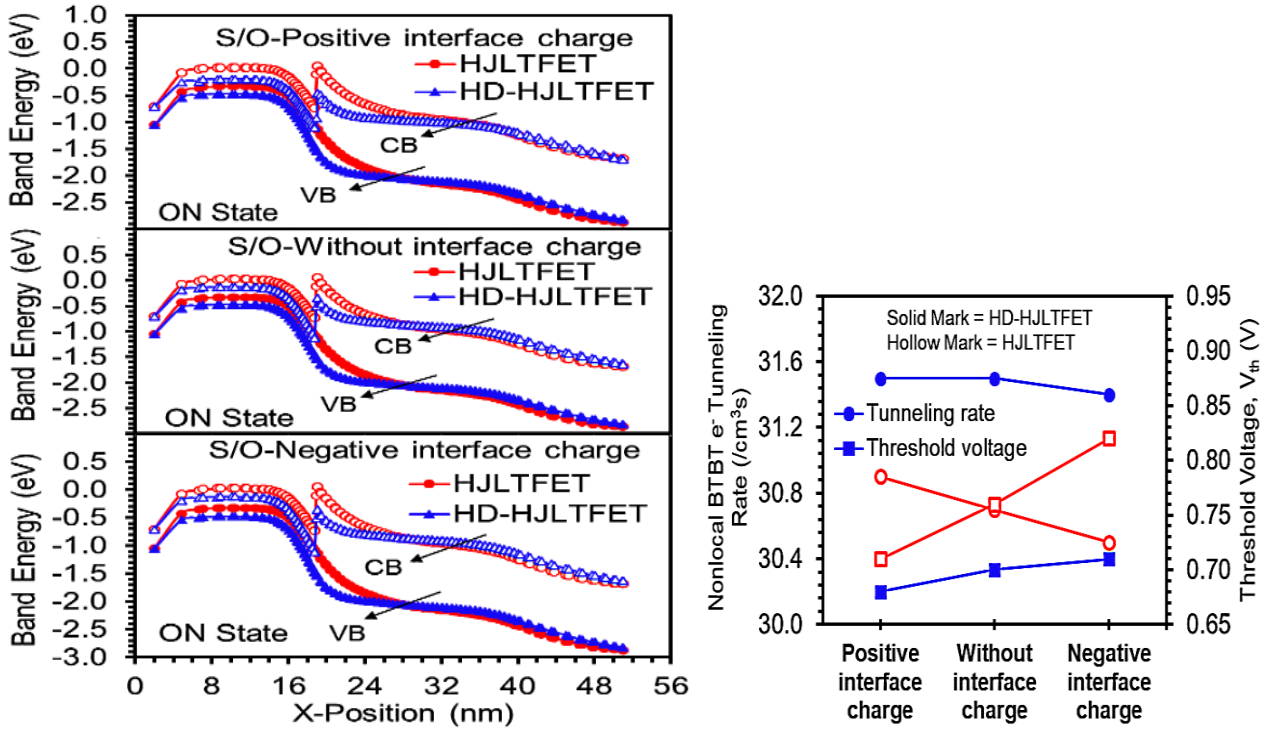
Since the hetero-material (InAs/AlGaSb) used in this chapter introduces a semiconductor/semiconductor (S/S) interface at S/C tunneling interface. Therefore, the impact of ITCs at the S/S interface has also been considered in the simulations. HD-HJLTFET and HJLTFET have been compared to study the impact of ITCs at the semiconductor/oxide (S/O) interface on device reliability and performance. The positive (acceptor) and negative (donor) charges with equal density have been considered at the AlGaSb/HfO_2 interface alongside the source for 7 nm, owing to the higher transverse electric field at the S/C tunneling interface. Due to the hetero-material architecture, the

impact of ITCs at the S/S (InAs/AlGaSb) interface is also considered. The interface charge density (N_f) has been chosen based on formerly reported simulation and experimental data, which involves the hot carrier/radiation/process damages resulting in trap density of 10^{11}-10^{13} $cm^{-2}eV^{-1}$ [18]-[19]. In these simulations, the interface charges are uniformly distributed with trap charge density fixed at N_f = 0, $\pm1\times10^{12}$ cm^{-2} in both the cases (S/O and S/S interface) to analyse the minimum performance variation of both devices. The polarity and position of interface charges are specified using the INTERFACE statement from [20]. This chapter is limited only to the study of ITCs at the S/O and S/S interfaces. The influence of ITCs at HfO_2/SiO_2 has been neglected, because in TFET S/O interface charges at S/C tunneling interface plays a vital role in device performance [9].

A few abbreviations used in this chapter are PIC - positive interface charge, WIC - without (neutral) interface charge, NIC - negative interface charge, S/O - interface charge, NIC - negative interface charge, S/O - semiconductor/Oxide interface, and S/S - semiconductor/semiconductor interface. This chapter is focussed on studying the impact of interface trap charges polarity at the semiconductor/oxide (S/O) interface of HD-HJLTFET and Low-K HJLTFET to see which one is more immune and reliable to ITCs. **Fig. 1.5(b-c)** illustrates the comparison of all three cases - hetero-gate dielectric, high-K gate dielectric, and low-K gate dielectric-based devices (HD-HJLTFET, High-K HJLTFET, and Low-K HJLTFET) for transfer characteristics (**Fig. 1.5b**) and Current switching ratio (I_{ON}/I_{OFF}) (**Fig. 1.5c**). On the basis of improved current switching ratio of HD-HJLTFET and Low-K HJLTFET in comparison to High-K HJLTFET (**Fig 1.5c**), these two cases have been chosen to be compared for ITCs polarity analysis.

5.3 RESULTS AND DISCUSSION

5.3.1 INFLUENCE OF S/O – ITCS ON ANALOG AND RF/MICROWAVE CHARACTERISTICS



(a) (b)

Fig. 5.2. (a) Energy band diagram (ON state) and (b) Non-local BTBT electron tunneling rate and threshold voltage of HD-HJLTFET and HJLTFET for different ITC polarity.

In this segment, the impact of ITC polarity (positive (donor type), negative (acceptor type), and neutral) at the S/O interface is examined to study the analog and RF/microwave performance for both the devices (HD-HJLTFET and HJLTFET). In **Fig. 5.2(a)**, the energy barrier width of the proposed HD-HJLTFET at S/C tunneling interface is lower than HJLTFET for all ITC polarity, due to the enforcement of high-k dielectric material (HfO_2) in the direction of the source, which results in more band bending and enhanced BTBT tunneling rate of electrons from the valence band of the source to the conduction band of the channel (**Fig. 5.2b**). In the presence of NICs, the BTBT electron tunneling

rate is reduced in both the devices; the PICs, however, increase the electron tunneling rate. Also, there is a minor variation in the BTBT tunneling rate for HD-HJLTFET than HJLTFET in terms of ITC polarity. This is due to the higher oxide capacitance of the high-k region in HD-HJLTFET, following the reduction in flat band voltage change, ΔV_{fb} ($\Delta V_{fb} = q.N_f/C_{ox}$, where ΔV_{fb} is the change in flat band voltage, C_{ox} is the oxide capacitance, N_f is the charge density, and q is the electronic charge) [9]. The variation in the threshold voltage (V_{th}) concerning all ITCs is also tiny in the case of HD-HJLTFET, whereas the V_{th} for PIC (NIC) is reduced (increased) to 6.5% (7.8%) in HJLTFET (**Fig. 5.2b**).

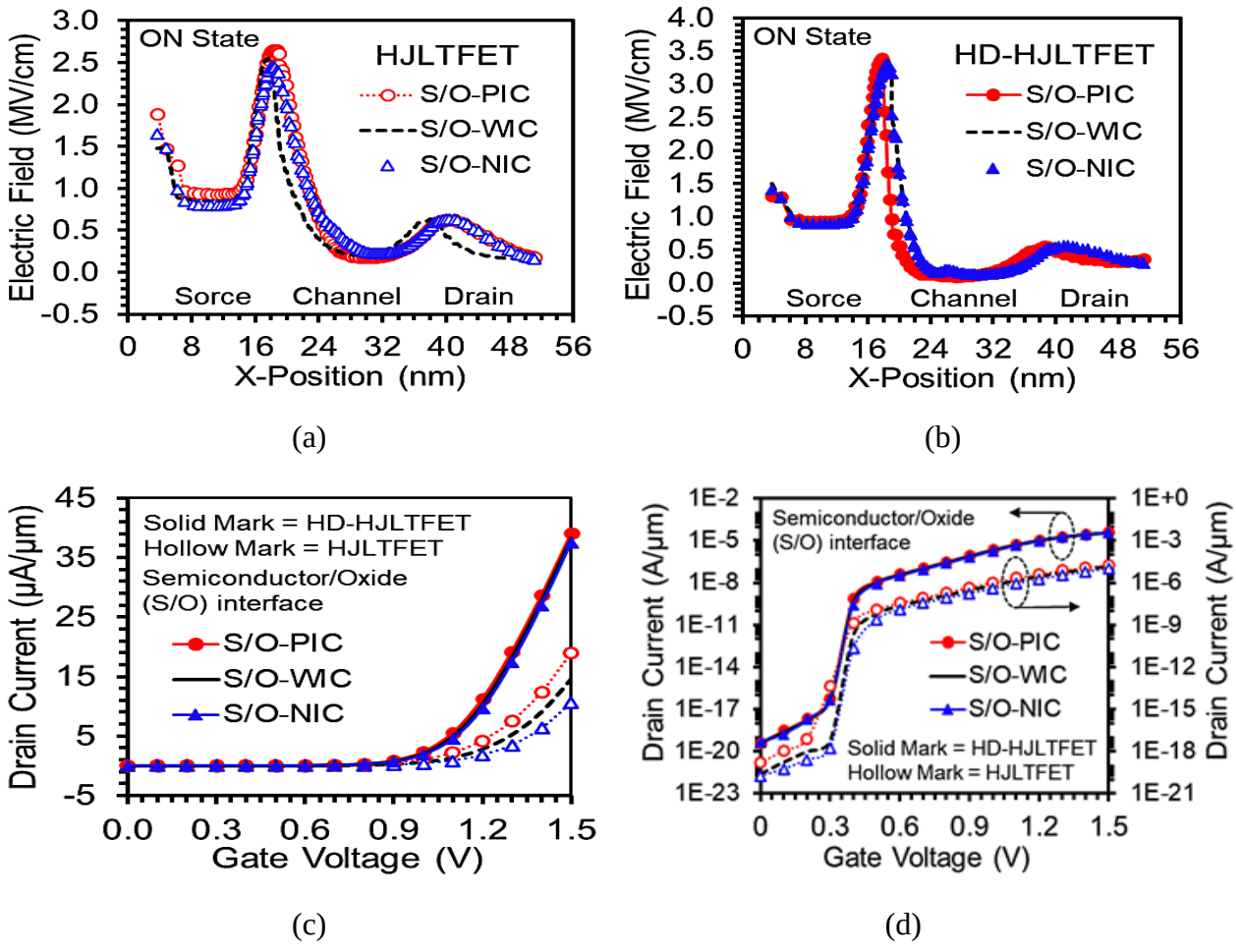
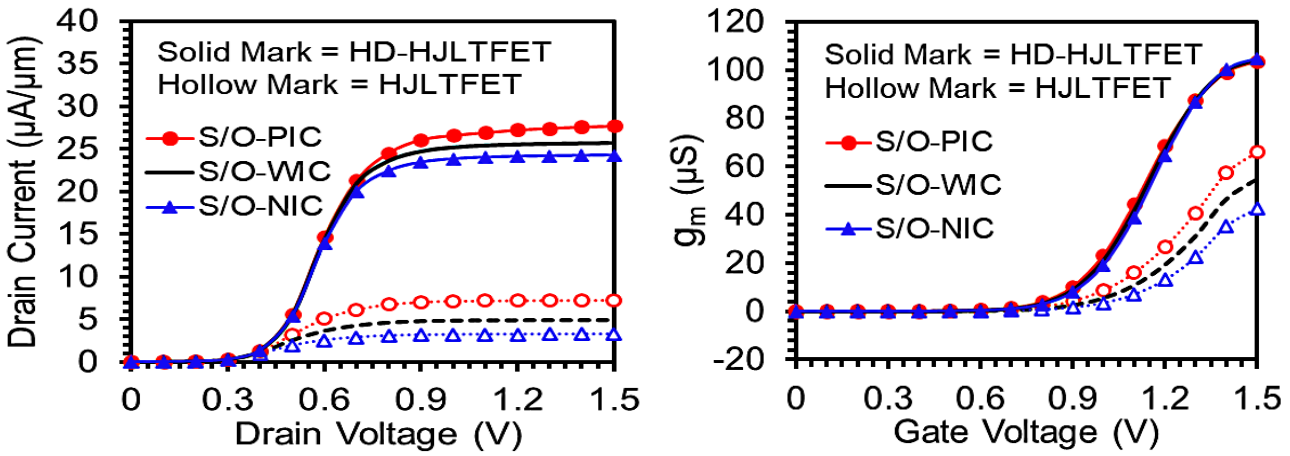


Fig. 5.3 Effect of ITC polarity on (a)-(b) Electric field of HJLTFET and HD-HJLTFET, (c) Transfer characteristics in linear scale, and (d) log scale of HJLTFET and HD-JLTFET.

The incorporation of heterogeneous dielectric in HD-HJLTFET raises the electric field at the S/C tunneling interface and reduces the electric field at the drain/channel (D/C) interface due to amalgamation of high-k dielectric towards the source and low-k dielectric towards the drain (**Figs. 5.3a-b**). The electric field at the S/C and D/C interfaces of HD-HJLTFET attains almost the same values for all ITCs polarity (PIC, WIC, and NIC) (**Fig. 5.3b**); however, in HJLTFET, the electric field near the S/C interface is increased (decreased) due to higher (lower) tunneling rate for PIC (NIC). The electric field at the D/C interface is approximately the same for PIC and NIC (**Fig. 5.3a**).



(a) (b)

Fig. 5.4. Effect of ITC polarity on (a) Output characteristics and (b) Transconductance of HD-JLTFET and HJLTFET.

Figs. (5.3c-d) illustrates the influence of different ITCs on the transfer characteristics of both aforementioned devices in linear and log scale. By attaining the high-k dielectric material in the direction of the source, the gate to channel coupling is improved, and hence the steeper band bending at the S/C interface gives rise to higher tunneling probability, which elevates the ON current of HD-HJLTFET. The PIC (NIC) increases (decreases) the ON current by 2.1% (2.34%) and 30% (27%) in HD-HJLTFET and HJLTFET, respectively. The leakage current of HD-HJLTFET attains approximately the same value for all ITCs, whereas the leakage current of PIC (NIC) increases(decreases) to 499% (34.6%) in HJLTFET (**Fig. 5.3d**), which shows that the transfer

characteristics of HD-HJLTFET are less affected by ITCs, making it more reliable in contrast to HJLTFET.

Figs. 5.4(a-b) depicts variation of output characteristics and transconductance g_m of the two devices for different ITC polarity in terms of gate bias, which determines the current driving proficiency of the device. The figure clarifies that g_m increases (decreases) to 20.4% (22%) due to the presence of PIC (NIC), leading to more considerable variation in the result parameters for the ITCs at the S/O boundary of HJLTFET, whereas, the g_m of HD-HJLTFET is affected negligibly (increases (decreases) to 0.4% (1.1%) for PIC (NIC)), thereby improving its reliability significantly.

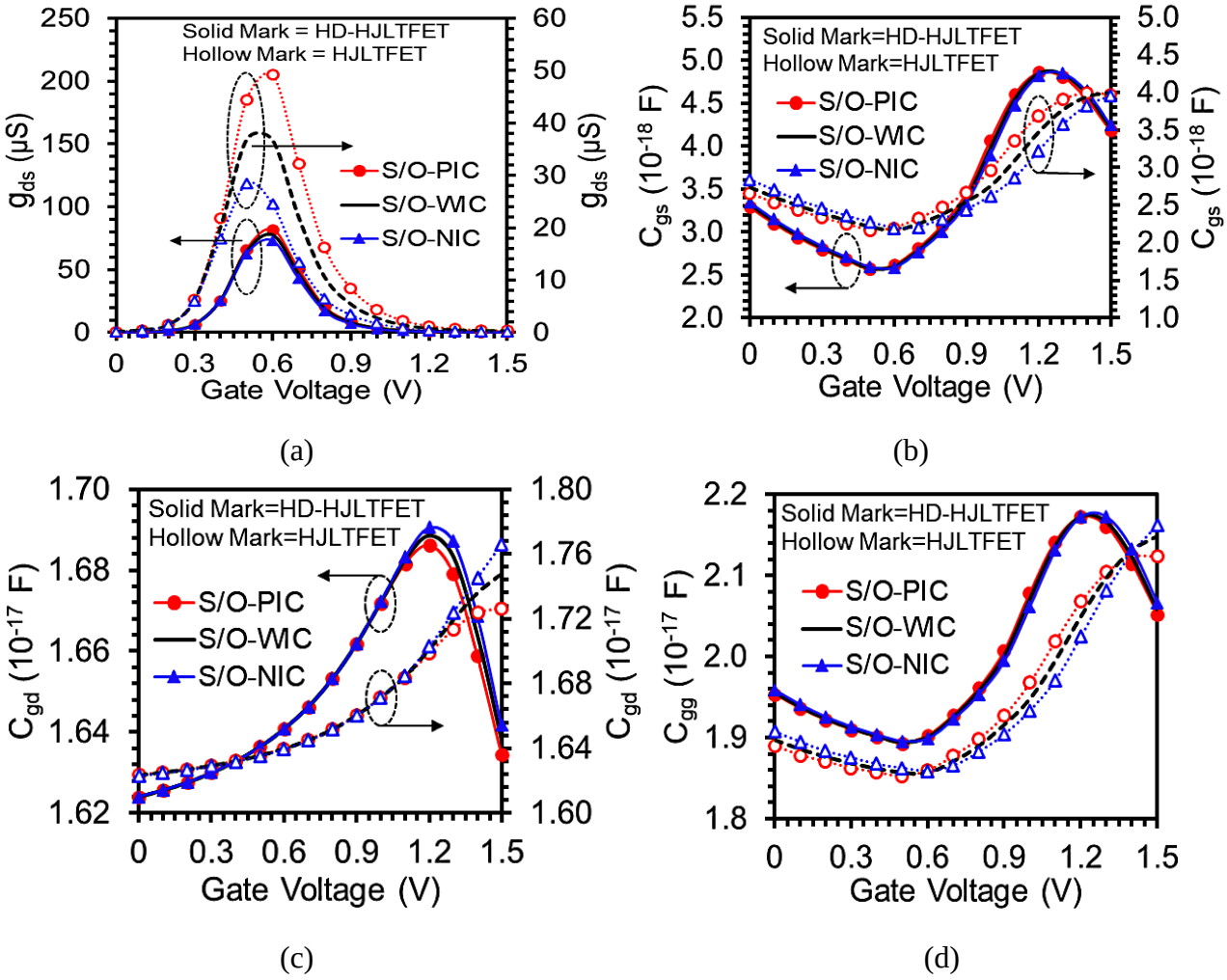


Fig. 5.5 Effect of ITC polarity on (a) Output conductance, Parasitic capacitances (b) C_{gs}, (c) C_{gd}, and (d) C_{gg} of HJLTFET and HD-HJLTFET, respectively.

Owning to the implementation of heterogeneous gate dielectric in HD-HJLTFET, the influence of ITCs on output conductance (g_{ds}) is almost negligible (**Fig. 5.5a**). As shown in **Fig. 5.5(a)**, g_{ds} of HD-HJLTFET is almost two times higher than HJLTFET; however, the introduction of PIC (NIC) in HJLTFET increases (decreases) the g_{ds} peak by ~1.3 times (~0.6 times) than WIC. It is essential to investigate the bias dependent parasitic capacitances of a TFET due to its different switching mechanisms and dependence of functioning pace on the parasitic capacitance. A small-signal AC analysis has been performed by ramping the DC voltage from 0-1.5V at a constant frequency of 1 THz to evaluate the intrinsic capacitances between the respective pair of electrodes (source, gate, and drain).

In **Fig. 5.5(b)**, for both devices, C_{gs} for starts decreasing as the gate voltage is ramped up from 0V to 0.6V and then starts surging with further increase in V_{gs} above 0.6V. This rising tendency of C_{gs} is initiated by the inter-gate capacitance offered by the polar gate over the source region. However, the impact of ITC polarity is negligible in HD-HJLTFET and the HJLTFET suffers from larger variation in C_{gs} with the introduction of different ITC polarity (**Fig. 5.5b**). As reported in [16] and [22], the inversion layer is set up from the drain to the source so that at higher gate voltage, C_{gg} is dominated mainly by C_{gd}. Due to lower electric field and higher gate to drain coupling at D/C junction, C_{gd} and hence C_{gg} shows more immunity against ITC polarity in HD-HJLTFET than HJLTFET (**Figs. 5.5c-d**). It is observed that in HD-HJLTFET, the presence of PIC (NIC) reduces (increases) the C_{gd} and C_{gg} to 0.4% (0.1%) and 0.4% (0.4%), respectively at V_{gs} = 1.5 V, whereas the presence of interface charges does not affect C_{gd} and C_{gg} at V_{gs} = 0 V. In HJLTFET, C_{gd} and C_{gg} reduces (increases) to 0.8% (1.7%) and 1.4% (0.4%), respectively, at V_{gs} = 1.5 V and the PIC (NIC) reduces (increases) C_{gg} by 1.4% (0.4%) at V_{gs} = 0 V.

Fig. 5.6(a) illustrates other crucial parameters cut-off frequency (f_T)-maximum oscillation frequency (f_{max}) with respect to gate voltage. HD-HJLTFET shows a negligible impact of ITC polarity on f_T as compared to its counterpart. The peak value of f_T is increased (decreased) by 21.9% (22.4%) on the

introduction of PIC (NIC) at the S/O interface of HJLTFET. This higher variation in f_T is due to the larger impact of ITC polarity on g_m of HJLTFET (**Fig. 5.4b**), this happens because f_T is directly dependent on g_m [16].

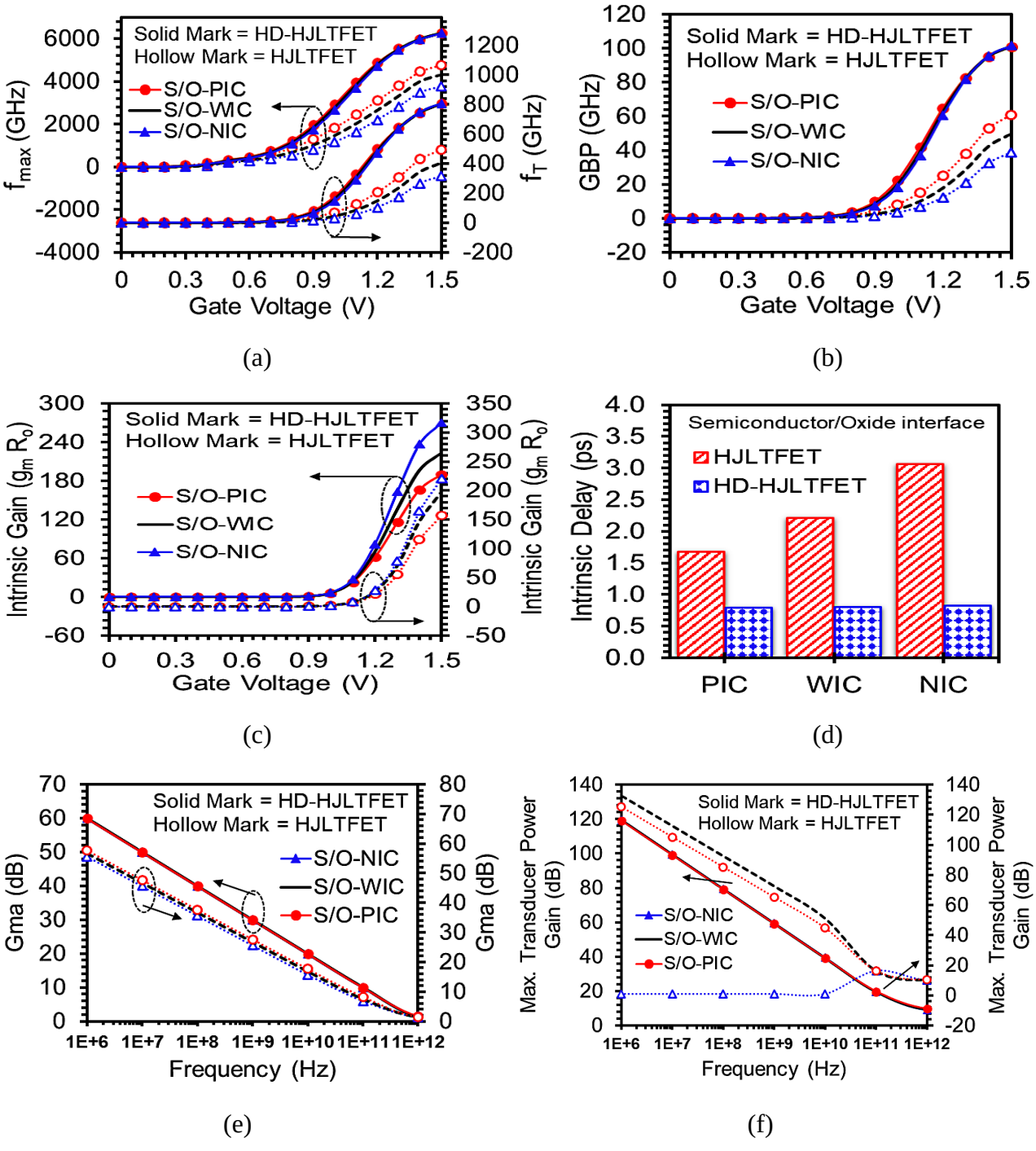


Fig. 5.6 Impact of ITC polarity on (a) Cut-off frequency/Maximum oscillation frequency, (b) Gain bandwidth product, (c) Intrinsic gain, (d) Intrinsic delay, (e) Maximum transducer power gain, and (f) Gma of HJLTFET and HD-HJLTFET, respectively.

However, HD-HJLTFET is immune to the impact of ITC polarity on f_T due to the immunity of g_m and C_{gg} from ITC polarity at the S/O interface of HD-HJLTFET. Along with attaining ~1.5 times higher peak of f_{max} the proposed device also shows a negligible variation (0.003%) in f_{max} for ITCs polarity at the S/O interface. However, the PIC (NIC) increases (decreases) the peak value of f_{max} by 11% (12.4%) in HJLTFET (**Fig. 5.6a**). In RF applications, gain bandwidth product (GBP) is another vital factor directly proportional to g_m and inversely proportional to C_{gd}. The impact of ITC polarity on GBP is insignificant in HD-HJLTFET (**Fig. 5.6b**). Moreover, the large variation of g_m and C_{gd} in HJLTFET gives rise to even larger impact of ITC polarity on GBP so that the PIC (NIC) increases (decreases) the peak value of GBP by 22% (22.8%). **Fig. 5.6(c)** displays the comparison plot of ITC influence on intrinsic gain ($A_v = g_m/g_{ds}$) of both devices. The higher A_v is desirable for better analog performance. HD-HJLTFET attains 13% higher A_v than HJLTFET. However, the impact of ITCs at the S/O interface of both the devices is approximately similar due to the higher g_m (higher g_{ds}) in HD-HJLTFET and lower g_{ds} (lower g_m) in HJLTFET, which counterbalances the impact of ITC polarity in both devices.

Fig. 5.6(d) compares the intrinsic delay for ITC polarity (PIC, WIC and, NIC) at the S/O interface of the two devices. The intrinsic delay for HJLTFET is 2, 2.8, and 3.8 times higher than HD-HJLTFET for PIC, WIC, and NIC, respectively. The application of HD engineering in HD- HJLTFET leads to an insignificant variation in intrinsic delay for different ITCs polarity at the S/O interface. Moreover, the enhancement in ON current in HD-HJLTFET reduces the intrinsic delay by 68% compared to HJLTFET. While designing low noise amplifiers, Maximum available power gain (Gma) needs to be considered, which measures the theoretical maximum power gain offered by a device. The higher the Gma of a device, the higher will be the power gains offered by the device as an actual amplifier. In HD-HJLTFET, there is negligible variation in the Gma for interface trap charges introduced at the S/O interface as compared to HJLTFET for a range of radio spectrum frequencies from 10^5 to 10^{12} Hz (**Fig. 5.6e**). Also, the Gma of HD-HJLTFET is higher than HJLTFET due to higher ON current

and transconductance. The effect of ITCs is investigated for maximum transducer power gain (G_{MT}) in **Fig. 5.6(f)**. The introduction of ITCs in HJLTFET produces higher variation in terms of G_{MT}, whereas no such variation is observed in case of HD-HJLTFET. Which shows more immunity towards interface trap charges in HD-HJLTFET.

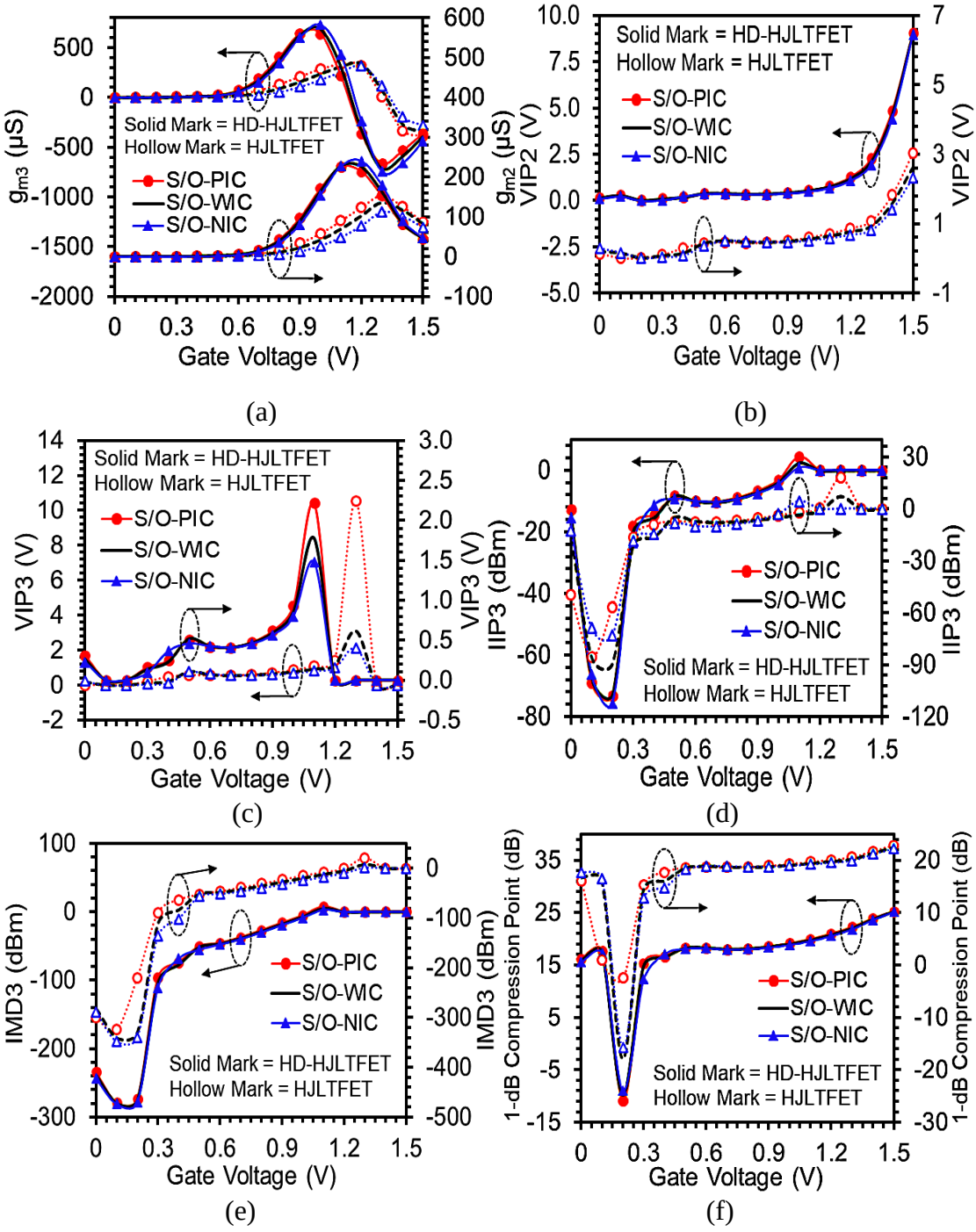


Fig. 5.7. Impact of ITC polarity on (a) g_{m2}-g_{m3}, (b) VIP2, (c) VIP3, (d) IIP3, (e) IMD3, and (f) 1-dB compression point of HJLTFET and HD-HJLTFET.

5.3.2 INFLUENCE OF S/O – ITCS ON LINEARITY AND HARMONIC DISTORTION PERFORMANCE

The desired quality of the signals in modern communication systems can be attained by assuring improved linearity and minimal signal distortion. If the device is unable to maintain linearity, then the nonlinear output may distort the desired signals. To address the nonlinearity issue, the influence of S/O-ITCs polarity on the linearity and distortion figure of merits such as g_{m2}, g_{m3}, VIP2, VIP3, IIP3, IMD3, 1-dB compression point, and zero-crossover point for HD-HJLTFET and HJLTFET has been studied. To attain better linearity and minimum distortion; VIP2, VIP3, IIP3, and 1-dB compression point should be high, whereas g_{m2}, g_{m3}, and IMD3 should be as low as possible [23]. All of these terms are discussed in detail in **chapter 2**. **Fig. 5.7(a)** shows the disparity between second/third-order derivative of transconductance (g_{m2}/g_{m3}) for different S/O-ITCs polarity of the two devices. The high-k dielectric incorporated towards the tunneling junction in proposed device shifts the peaks of both g_{m2} and g_{m3} towards lower gate bias than HJLTFET. Also, g_{m2} and g_{m3} of HD-HJLTFET is reduced to ~28% and 1022% of HJLTFET at V_{gs} = 1.4 V and 1.3 V, respectively. Further, a variation of g_{m2} and g_{m3} against ITCs polarity is also negligible in HD-HJLTFET, whereas the presence of PIC (NIC) at the S/O interface of HJLTFET increases (decreases) the g_{m2} and g_{m3} peak values relating to WIC.

Fig. 5.7(b) shows that high-k dielectric used near the S/C interface of HD-HJLTFET enhances g_m such that the amplitude of VIP2 was 3.5 orders higher than low-k dielectric used in HJLTFET. Also, the presence of PIC (NIC) increases (decreases) the amplitude of VIP2 to 0.1% (0.9%) in case of HD-HJLTFET. However, for HJLTFET, the increment (decrement) in VIP2 is 15% (11%) in the presence of PIC (NIC) in terms of WIC. In **Fig. 5.7(c)**, VIP3 peak is shifted towards the lower gate voltage revealing that better linearity can be accomplished at lower gate voltage by applying high-k dielectric at the tunneling interface. Moreover, the VIP3 peak is increased (decreased) to 240% (32%) due to

the existence of PIC (NIC) with respect to WIC in HJLTFET, whereas, the PIC (NIC) increases (decreases) the peak of VIP3 by 24% (17%) in HD-HJLTFET. Third-order intercept input power (IIP3) and third-order intermodulation distortion power (IMD3) are other crucial parameters of linearity in wireless communication systems. **Figs. 5.7(d-e)** displays the amplitude variance of IIP3 and IMD3 for ITCs polarity at S/O interface of HD-HJLTFET and HJLTFET. The variation of IIP3 and IMD3 due to the existence of S/O-ITCs polarity in HD-HJLTFET is nearly unaffected compared to HJLTFET. Also, the IIP3 of HD-HJLTFET is much higher than the IMD3 due to enhanced g_m and reduced g_{m3} on the amalgamation of high-k dielectric at the tunneling interface, that enhances the device power by minimizing the hot-carrier effect. The reduced signal distortion and enhanced g_m of HD-HJLTFET give rise to higher 1dB compression point with peak shifted towards lower gate bias than HJLTFET (**Fig. 5.7f**).

Table 5.1.

Comparison of result features of HJLTFET, conventional HD JL-TFET [10], and proposed HD-HJLTFET for various ITCs polarity (PIC and NIC) with respect to WIC.

Parameters	***HJLTFET (conv.)***	***Conv. HD JL-TFET [10]***	***HD-HJLTFET (prop.)***
S/O-Interface Trap Charges	***Positive (Negative)***	***Positive (Negative)***	***Positive (Negative)***
Transfer Characteristics	30% ↑ (27% ↓)	13% ↑ (12.6% ↓)	2.1% ↑ (2.3% ↓)
Output characteristics	47.7% ↑ (33.2% ↓)	13.3% ↑ (12% ↓)	7.7% ↑ (5.4% ↓)
Transconductance	20.4% ↑ (22% ↓)	69.4% ↑ (44.1% ↓)	0.4% ↑ (1.2% ↓)
Output Conductance	32% ↑ (32.4% ↓)	14% ↑ (13.4% ↓)	5% ↑ (6.4% ↓)
Gate to source Capacitance	6.3% ↑ (7.2% ↓)	2.76% ↑ (2% ↓)	0.4% ↑ (0.4% ↓)
Gate to drain Capacitance	0.8% ↑ (1.7% ↓)	12.4% ↑ (8% ↓)	0.4% ↑ (0.12% ↓)
Cut-off Frequency	22% ↑ (22.4% ↓)	-	0.1% ↑ (0.24% ↓)
Maximum Oscillation Frequency	11% ↑ (12.4% ↓)	-	0.003% ↑ (0.003% ↓)

Moreover, there is an increase (decrease) of 0.3% (0.08%) in 1dB compression point on the existence of PIC (NIC) in HD-HJLTFET, which is negligible in comparison to an increase (decrease) of 1.3% (1.3%) for PIC (NIC) in HJLTFET.

As displayed in **Table 5.1**, the proposed device has shown many orders lower or negligible variation in the analog, RF, linearity and distortion performance in terms of ITCs polarity at the S/O interface in comparison to HJLTFET (conventional) and published conventional device HD JL-TFET [6].

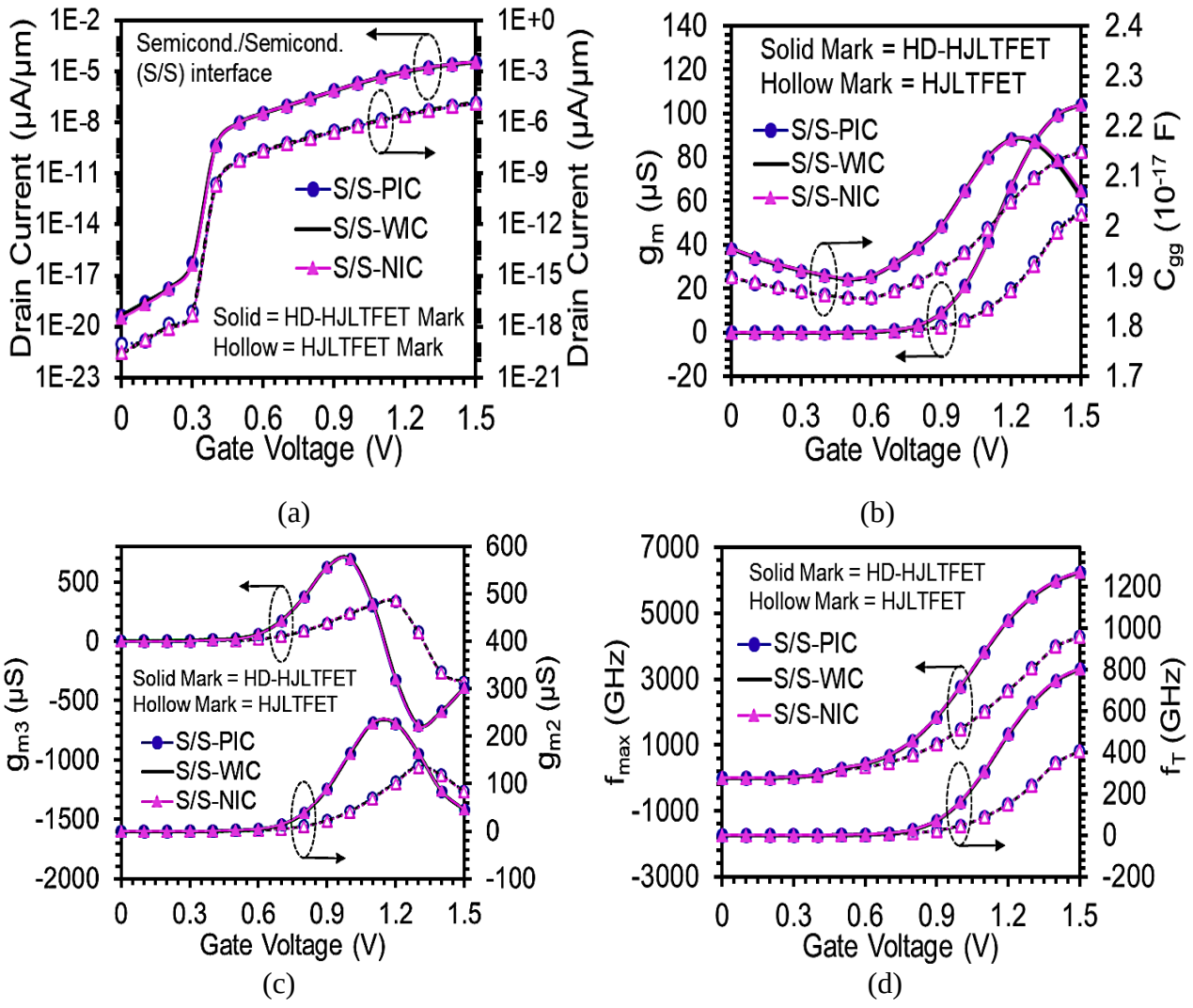


Fig. 5.8. Impact of S/S-ITC polarity on (a) Transfer characteristics, (b) g_m /C_{gg}, (c) g_{m2}/g_{m3}, and (d) f_T/f_{max} of HD-JLTFET and HJLTFET.

5.3.3 INFLUENCE OF S/S – ITCS ON PERFORMANCE OF HD-HJLTFET AND HJLTFET

The effect of S/O interface trap charges polarity on the performance of both devices has been discussed in the preceding sections. Since the fundamental architecture of both devices is based on the amalgamation of two semiconducting hetero-materials at the S/C junction, therefore the impact of S/S interface trap charges polarity (PIC, WIC, and NIC) has also been investigated with same charge density (N_f = 0, $\pm 1\times10^{12}$ cm^{-2}) on the analog/RF performance of the two devices. **Figs. 5.8(a-b)** demonstrates the impact of S/S-ITCs polarity on the transfer characteristics and transconductance in terms of gate voltage for HD-HJLTFET and HJLTFET. The two devices exhibited no influence of ITC polarity i.e., PIC and NIC, on the transfer characteristics and g_m and gave same result as that for absence of ITC (WIC) at the S/S interface. Similarly, other result parameters like C_{gg}, g_{m2}, g_{m3}, f_T, and f_{max} showed no influence of the S/S-ITCs polarity on HD-HJLTFET and HJLTFET (**Figs. 5.8b-d**). The donor (PIC) and acceptor (NIC) ITCs showed the same result characteristics as that for the absence of ITCs (WIC) at the S/S interface of the two devices. Thus, it is inferred from the above results that both the devices are immune to S/S-ITCs polarity.

5.4 CONCLUSION

This chapter presented a comprehensive investigation showing the influence of ITCs polarity on the RF/microwave, linearity, and distortion parameters of heterogeneous dielectric engineering imposed hetero-material based junctionless TFET device (HD-HJLTFET). All result characteristics are compared with no interface charges case. The incorporation of HD technique in charge plasma-based device leads to the enhancement of band bending at the S/C interface, making the tunneling barrier narrower. The process improves the transconductance, and the device attains superior performance

in terms of A_v, f_T, f_{max}, VIP2, VIP3, IIP3, IMD3, and 1-dB compression point. The average variation of result elements in HD-HJLTFET (HJLTFET) in terms of transfer characteristics is: - ~2% (~28.5%), g_m - ~0.8% (~21.2%), g_{ds} - ~5.7% (~32%), C_{gs} - ~0.4% (~6.8%), C_{gd} - ~0.2% (~1.3%), f_T - ~0.17% (~22%), and f_{max} - ~0.003% (~12%), showing more immunity against S/O-ITCs polarity (PIC and NIC) than HJLTFET. Further, both devices showed negligible performance variation against the presence of ITCs polarity at the hetero-material (InAs/AlGaSb) S/S interface. The optimization of a reliable and efficient device must consider the influence of ITCs on efficiency degradation since these ITCs are usually present in a real device, which may affect the result outcomes.

Till now only PG and CG are considered responsible for the retention of hole plasma and electron plasma in JLTFET. However, the retention of the hole plasma in the p^+ prompted source is highly influenced by the choice of source electrode metal work function, which has been given due attention in the next chapter. This may lead to the formation of Schottky or ohmic contact formation at the source electrode metal/source interface. This may change the performance metrics of JLTFET, which has been overlooked before.

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CHAPTER-6

INFLUENCE OF SOURCE ELECTRODE METAL WORK FUNCTION ON POLAR GATE PROMPTED SOURCE HOLE PLASMA IN ARSENIDE/ANTIMONIDE TUNNELING INTERFACED JUNCTIONLESS TFET.

Numerous studies have explored the impact of control gate and polar gate on the retention of hole and electron charge plasma to induce the source and channel region polarity in junctionless tunnel field effect transistor (JLTFET). However, polar gate is not the only one responsible for the retention of hole plasma in the p^+ prompted source but the hole plasma near the interface of source electrode metal and p^+ prompted source (SEM/S) is influenced by the choice of source electrode metal work function too. This chapter features a comprehensive investigation of the mutual significance of PG and SEM work function on p^+ prompted source to study key analog characteristics of arsenide/antimonide tunneling interfaced hetero-material JLTFET (HJLTFET), which is unexplored in the literature otherwise. Three metals – W (4.55 eV), Mo (4.65 eV), and Pd (5.3 eV) has been considered as the source electrodes in HJLTFET. For source electrode metal work function lesser than p^+ prompted source (W and Mo), the Schottky contact is formed by the depletion of hole plasma near source electrode metal and p^+ prompted source interface. This results in the immediate current inhibition at source to channel interface caused by an undesired movement of electrons en route to the Schottky interface. The Schottky tunneling phenomenon is considered by implementing the Universal Schottky Tunneling model to study the underestimated drain current of HJLTFET. However, the Universal Schottky Tunneling model becomes inconsequential for source electrode

metal work function higher than p^+ prompted source (Pd) as hole plasma is preserved by the ohmic contact formation.

6.1 INTRODUCTION

The fast-growing need of next generation devices in artificial intelligence, cloud computing, low power and high-speed modern communication systems, and internet of things has led the research community to explore new innovative ideas at the sub 20 nm technology node like never before. The high operation speed, improved functionality and enhanced packing density are the results of continuous downscaling of CMOS technology. However, it results in various critical challenges like high leakage current, high static power dissipation and short channel effects [1-7]. Other modern electronic devices like MOSFET, HEMT, HBT, and negative capacitance filed effect transistors (FETs) show degraded performance at sub 20 nm technology node despite being widely used in modern communication systems. The alternative to such issues can be the device having steeper swing and lower leakage current. Tunnel field effect transistor (TFET) is amongst the most promising devices to fill these gaps along with improved performance pertaining to steeper swing and lower leakage current. However, inferior ON current (I_{ON}) is still a snag for the TFET devices. Moreover, the development of extremely thin doping junctions using highly doped source and drain region is one of the major obstacles owing to the increased thermal expenses for hybrid thermal annealing and ion implantation [8-9]. Along with that, random dopant fluctuations are also generated due to the highly doped source and drain regions [10]. Therefore, to eradicate the junction constraint and simplify the fabrication complexity, junctionless FETs were introduced based on charge plasma concept. Thus, junctionless TFETs have given a new outlook to the electronic industry by merging the advantages of TFET (steeper swing) and JLFET (high I_{ON}) [11-17].

Many researchers have paid attention to analyse the performance characteristics of JLTFET by exploring the impact of control gate (CG) and polar gate (PG) work functions. However, the depletion of hole plasma by the work function of source electrode metal (SEM) at the interface of SEM and p^+ prompted source region (SEM/S) has not been given due importance [11-16, 18-20]. The depletion

of hole plasma gives rise to a Schottky interface at the SEM/S interface, which is implemented through the universal Schottky tunneling mechanism (UST) at the SEM/S interface. The ignorance of UST at the SEM/S interface leads to underrated performance of the device. In this work, due attention has been given to the UST at the SEM/S interface by selecting appropriate source electrode metal work function. To take into account the Schottky tunneling at the SEM/S interface, an in-depth attention has been laid upon incorporating the Universal Schottky Tunneling model (UST) in this chapter, which has been overlooked by many researchers before [8-9, 11, 17]. **Fig. 6.1** represents the grid sites near the Schottky contact, which signifies the localized tunneling generation rates of electrons. In UST mechanism, the tunneling current is calculated across these grid sites within a specified distance of the electrode. **Eq. 6.1** describe the calculation of tunneling current component as follows [18-19, 21]:

$$J_T = \frac{A^* T_L}{K} \int_E^{\infty} I(E') \ln\left[\frac{1+f_s(E')}{1+f_m(E')}\right] dE' \tag{6.1}$$

$$G_T = \frac{1}{q} \nabla J_T \tag{6.2}$$

Where, J_T is the tunneling current density, A^* is the effective Richardson's coefficient, T_L is the lattice temperature, $I(E')$ is the tunneling probability, $f_s(E')$ and $f_m(E')$ are the Maxwell-Boltzmann distribution functions in the semiconductor and metal and E' is the carrier energy. G_T is the localized tunnelling rate. The total current density across the Schottky barrier is the sum of thermionic emission component and tunnelling component as shown in **Fig. 6.1**. **Eq. 6.3** represents the mathematical expression for total current density across the Schottky barrier:

$$J_{TOT} = J_T + J_{TH} \tag{6.3}$$

Where J_{TOT} is the total current density and J_{TH} is the thermionic emission component. For lower Schottky barrier height, the thermionic emission of the carriers over the barrier increases leading to

enhancement in the thermionic emission component of current. In that case the tunnelling current density is reduced. However, the tunnelling current comes into play only if the tunnelling width is lower than 10 nm [18].

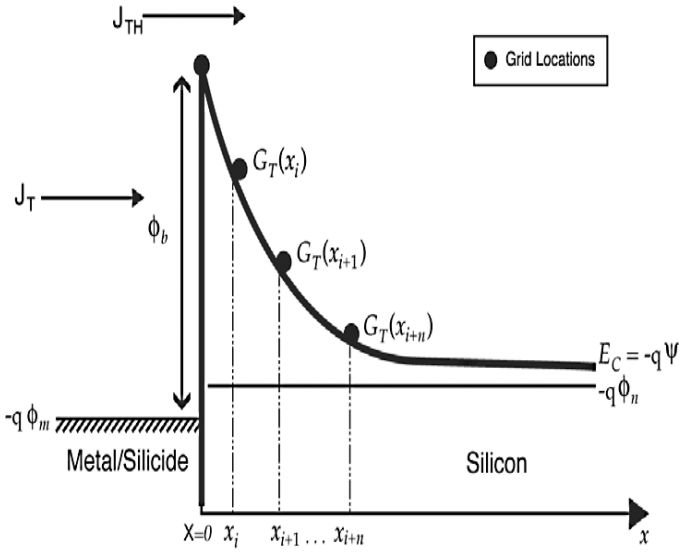


Fig. 6.1. The universal Schottky tunnelling mechanism representing the local tunnelling generation rate at the metal/semiconductor interface [21].

In this chapter, for the first time, metals with different work functions as the source electrode have been implemented to study the significance of SE metals on the analog characteristics of HJLTFET. The presented work may be helpful to study various underrated physical effects of JLTFETs in regards to ohmic and schottky contacts. It may put the research of junctionless devices in the right direction owing to the hole plasma depletion consideration at the SEM/S interface, which has been overlooked before.

6.2 DEVICE DESIGN AND SIMULATION

The schematic device architecture of proposed device HJLTFET is presented in **Fig. 6.1(a)**. The

device dimensions and parameters are the same as of **chapter 4**. To study the impact of metal work function in the source electrode, three metals viz. tungsten (W, 4.55 eV), Molybdenum (Mo, 4.75 eV), and palladium (Pd, 5.3 eV) have been implemented [20]. The ON state and OFF state corresponds to V_{GS} = 1.5 V, V_{DS} = 1.5 V and V_{GS} = 0.0 V, V_{DS} = 1.5 V, respectively.

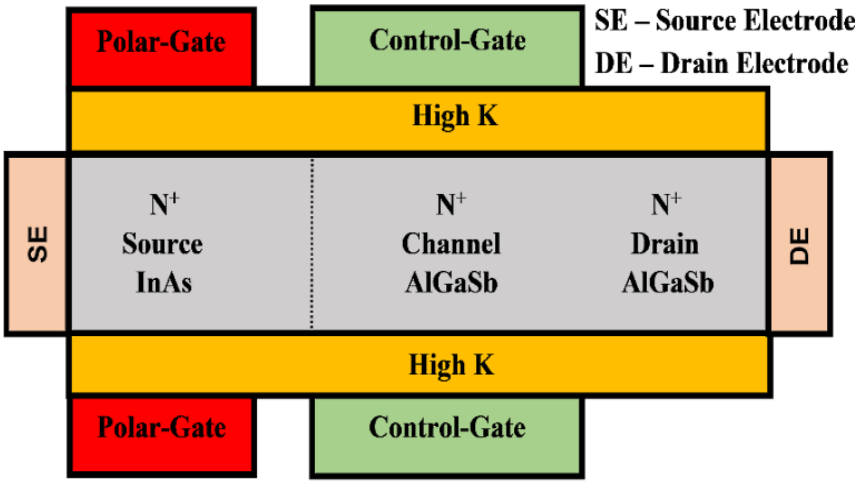


Fig. 6.2. Device schematic architecture of HJLTFET [22].

6.2 SIMULATION METHODOLOGY

To consider the quantum mechanical effects of thin body semiconductor, the drift-diffusion mode-space method (DD_MS) has been implemented. This model solves the 1D transport equations in each sub-band and quasi-fermi levels are extracted. The currents and bulk carrier densities are calculated by summating over all sub-bands. It captures quantum effects in transverse direction along with other models for band-to-band tunnelling, mobility and recombination. The other models used in simulation are already mentioned in **chapter 2**. To inculcate the impact of interface trap charges and band tailing, the interface charges are uniformly distributed with trap charge density fixed at $N_f = 1\times10^{12}$ cm^{-2} for semiconductor/semiconductor and semiconductor/oxide interfaces (S/S and S/O interface) based on earlier reported simulation and experimental data involving the hot carrier/radiation/process damages

[21]. The polarity and position of interface charge is specified using the INTERFACE statement [23]. The prime focus of the chapter is to include the impact of SE metal work function on the device performance. For that purpose, the UST model has been evoked while designing the HJLTFET having SE metal work function lower than the p^+ (hole plasma) prompted source region. Moreover, the results obtained are also compared with HJLTFET after the exclusion of UST model, to study the variation of result characteristics with the inclusion and exclusion of UST model. The SE metal work function lower than p^+ prompted source region gives rise to the Schottky tunneling at the SEM/S interface, which is taken into account by the implementation of UST model. Such aspect of HJLTFET devices have not been considered in former studies to the best of our knowledge.

6.3 RESULTS AND DISCUSSION

In this section, a thorough investigation of the impact of three SE metal work functions on the analog characteristics of InAs/AlGaSb based HJLTFET has been carried out.

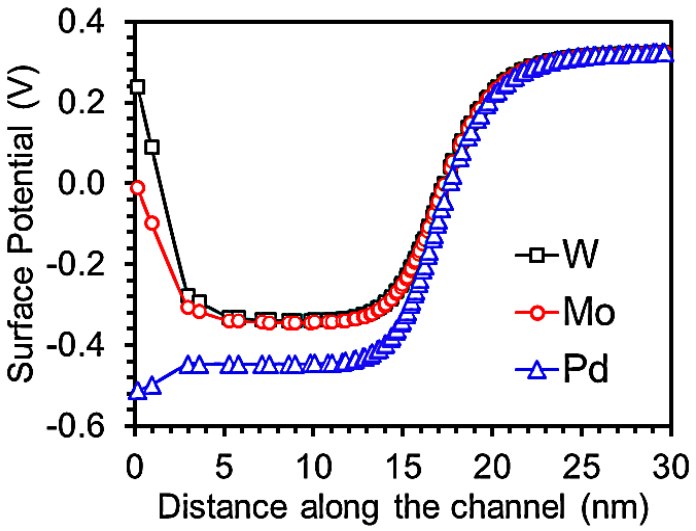


Fig. 6.3. Surface potential variation along the channel direction for three SE metals at thermal equilibrium state [22].

Fig. 6.3 illustrates the variation of surface potential along the channel direction for no biasing condition (thermal equilibrium state, V_{GS} = 0.0 V, V_{DS} = 0.0 V) for three SE metal work functions. For SEMs, W and Mo having work function lesser than p^+ prompted source, the hole plasma induced by the PG nearby the SEM/S interface gets depleted by the surface potential. However, for the larger work function metal Pd, the hole plasma at the SEM/S interface is retained by the PG (**Fig. 6.3**). Such variation of surface potential with respect to the different SE metal work function shows synchronization with the already existing theories [24].

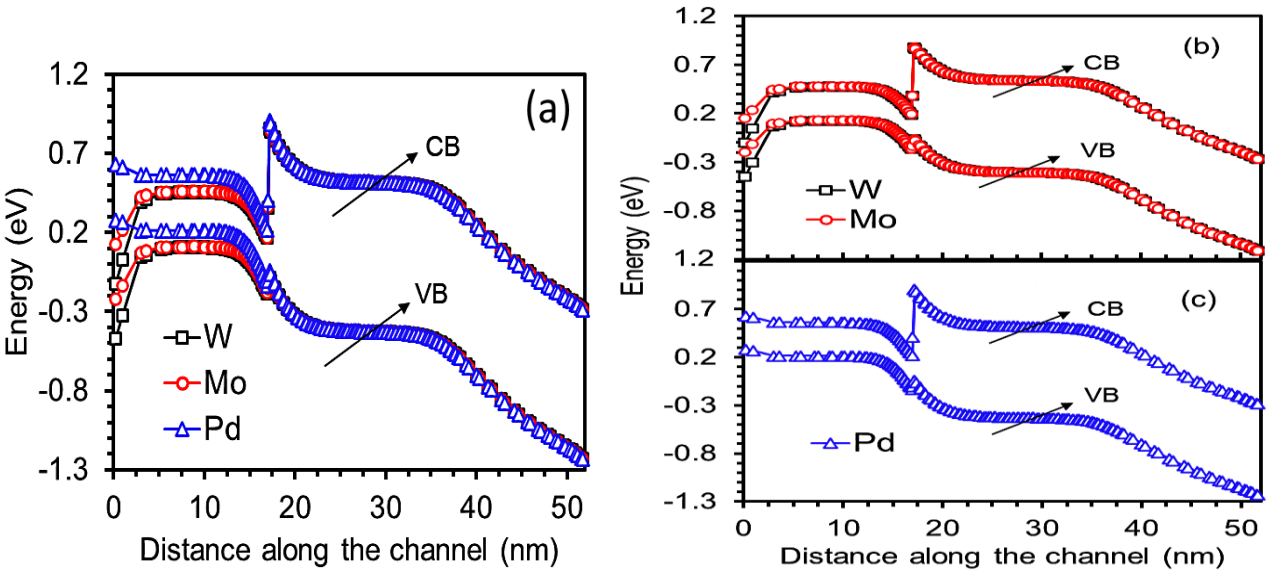


Fig. 6.4. (a) Energy band profile of HJLTFET for three SE metals at thermal equilibrium state, (b) Formation of Schottky interface at W and Mo SE/Source interface, and (c) Formation of ohmic contact for Pd SE [22].

Fig. 6.4 (a-c) displays the disparity of energy band profile along the channel direction at thermal equilibrium for three SE metal work functions. The energy band profile of HJLTFET has been calculated by considering the cutline across the whole channel length (along the x-direction) 1 nm below the channel surface. In **Fig. 6.4(a)**, the depletion of hole plasma near the SEM/S interface for W and Mo gives rise to Schottky contact due to the SEM work function lesser than p^+ prompted source. Whereas the higher work function SE metal, Pd gives rise to ohmic contact owing to the

preservation of hole plasma. In **Fig. 6.4(b)**, for W and Mo SEs, the source region is no longer p^+ type at the SEM/S interface.

The depletion of hole plasma leads to reduction of effective carrier conduction as the electrons attain higher probability to move towards the SE. Thus, the electrons available for tunneling across the S/C interface reduces (**Fig. 6.4b**). However, the hole plasma is preserved for SEM work function higher than p^+ prompted source (for Pd), maintaining the electron movement only towards the S/C interface. Thus, the effective carrier conduction remains unaltered for Pd SE metal (**Fig. 6.4c**). It confirms that along with PG, the choice of SEM work function is equally responsible for the induction of hole plasma in the source region of HJLTFET. A detailed theory regarding the transformation of metal contact from ohmic to Schottky by choosing appropriate work functions has been developed in [20]. However, the transformation of metal contacts from ohmic to Schottky for hetero-material junctionless TFETs leads to new aspects for the research community and mobile industry.

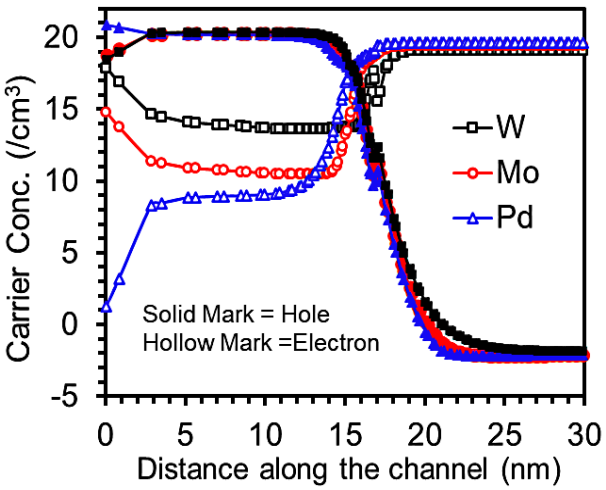
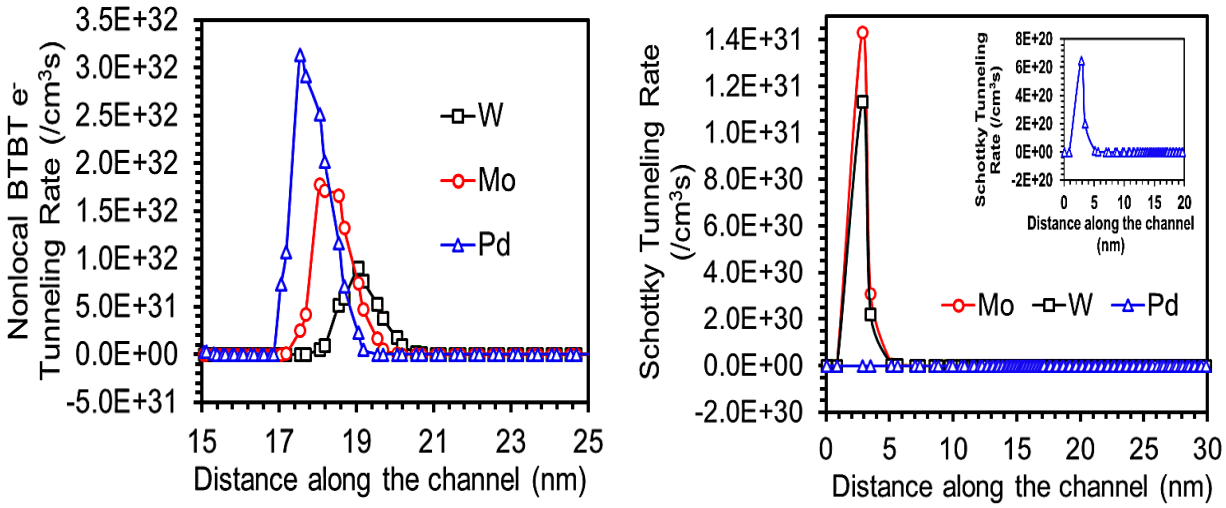


Fig. 6.5. ON state electron and hole concentration along the channel direction for three SE metals [22].

Fig. 6.5 illustrates the electron/hole concentration of carriers along the channel length for three SE metals. As stated before, in **Fig. 6.4(a-b)** regarding the electrons moving towards the SE region for W and Mo SE metals, a similar phenomenon has been observed regarding the carrier concentration

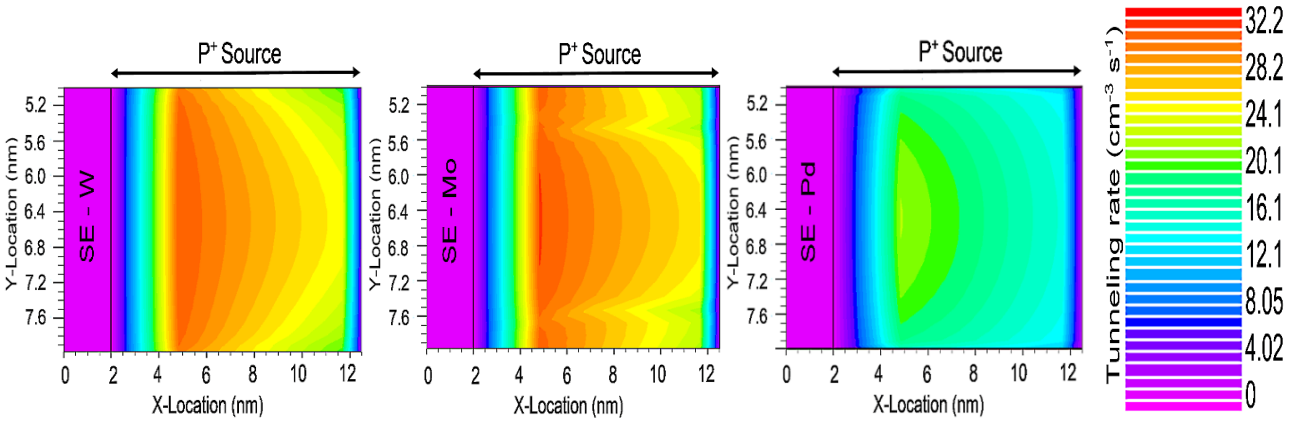
in **Fig. 6.5**. The electron concertation increases greatly as compared to the hole concentration near the SE region for W and Mo metals confirming the movability of electrons in the direction of SE. This declines the tunneling of electrons across the S/C interface and hence the BTBT rate of HJLTFET is diminished for W and Mo SE metals (**Fig. 6.6a**). Therefore, the overall conduction of HJLTFET is also hampered owing to the lowered BTBT rate. Since number of electrons available for tunneling across the S/C interface has declined, the drain current of HJLTFET also reduces for W and Mo SEs. For Pd SE, the absence of Schottky interface at the SEM/S interface leads to the highest electron BTBT rate. There is only one way movability of electrons from source to channel region through S/C interface leading to numerous electrons available for effective conduction of HJLTFET (**Fig. 6.6a**). As mentioned before, the W and Mo SEs exhibit the Schottky tunneling at the SEM/S interface. Therefore, the UST model need to be implemented to emulate the accurate device physics regarding the tunneling phenomenon at the SEM/S interface. **Fig. 6.6(b)** displays the Schottky tunneling rate of electrons at the SEM/S interface for all three metal SEs – W, Mo, and Pd.



(a) (b)

Fig. 6.6. (a) Band to band tunneling rate at S/C interface and (b) Schottky tunneling rate at SEM/S interface for different SE metals [22].

The comparison of contour plot of Schottky tunneling is also illustrated in **Fig. 6.7.** The Schottky tunneling for W is lower than Mo. The reason behind lower Schottky tunneling of W is the larger Schottky potential barrier, whereas Mo SE attains lower Schottky potential barrier height (**Fig. 6.3**) and width leading to enhanced Schottky tunneling rate (**Fig. 6.6b**). The Schottky tunneling rate for Pd SE is almost negligible owing to higher SE work function than p^+ prompted source. This is because of the non-existence of Schottky interface at the SEM/S interface of Pd SE. Therefore, the UST model has no influence on the performance of Pd SE. The contour plots of the three aforementioned SE metals show similar variation in **Fig. 6.7**. Here, the Mo SE (**Fig. 6.7b**) leads to significantly higher Schottky tunneling rate than W SE (**Fig. 6.7a**) at the SEM/S interface, whereas the Schottky tunneling rate of Pd SE is diminished (**Fig. 6.7c**).

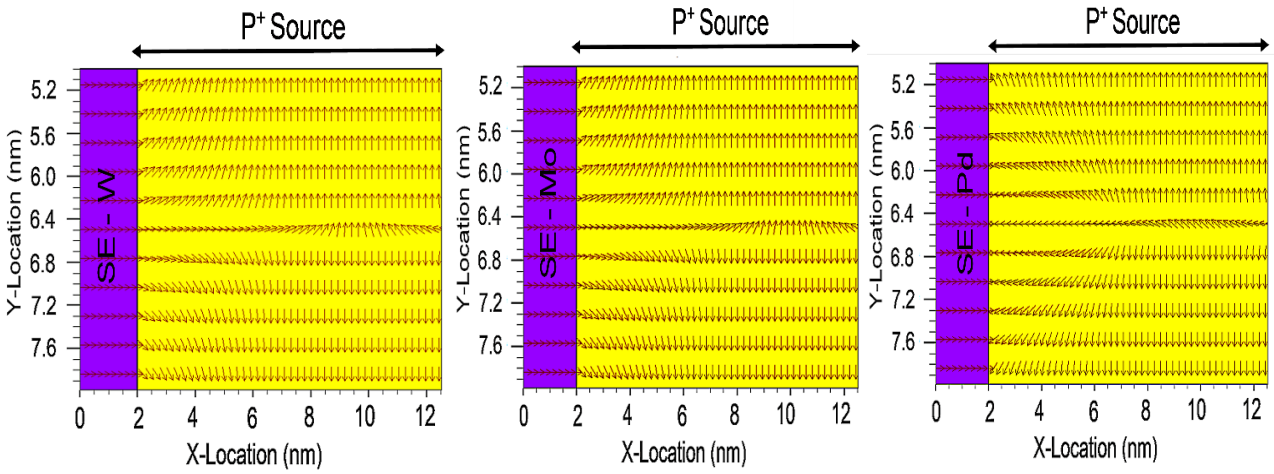


(a) (b) (c)

Fig. 6.7. ON state level curve (contour) of Schottky tunneling rate (log scale) of HJLTFET for (a) W, (b) Mo, and (c) Pd [22].

Fig. 6.8(a-b) illustrates the vector representation of the electric field direction of HJLTFET for three SE metal work functions under the ON state. It has displayed the electric field vector representation in the hole plasma depleted region near the SEM/S interface. Since the direction of electric field is opposite to the direction of flow of electrons, therefore the movability of electrons from source to channel is defined by the electric field vector. It helps to outline the impact of SEM work function on

the formation of Schottky tunneling interface at the SEM/S interface of HJLTFET. For W and Mo SEs, the movability of electrons is more in the direction of SE forming the Schottky interface (**Fig. 6.8a-b**). This is due to the hole plasma depletion at the SEM/S interface and hence the current conduction is abstained in the channel region (**Fig. 6.8a-b**), whereas, the electric filed vector shows only one way movability of electrons from source to channel vanishing the Schottky contact formation at the SEM/S interface of Pd SE. Hence, the current conduction remains immune for Pd SE, due to ohmic contact formation at SEM/S interface (**Fig. 6.8c**).



(a) (b) (c)

Fig. 6.8. ON State electric field vector illustration of HJLTFET for (a) W, (b) Mo, and (c) Pd [22].

To illustrate the impact of inclusion and exclusion of UST model in the SE-HJLTFET device physics, the transfer characteristics of HJLTFET have been plotted for three aforementioned SE metal work functions (W, Mo, and Pd) in **Fig. 6.9(a)**. For the both inclusion and exclusion of UST model, the results show major variation for SEM work functions lesser than the p^+ prompted source region (W and Mo). On the implementation of UST model, the Schottky tunneling is taken into account due to the depleted hole plasma at the SEM/S interface. This Schottky tunneling gives precise calculations of the drain current, which is overlooked without the implementation of UST model. There is no

variation of transfer characteristics in Pd SE with or without the UST model. The reason behind this is the formation of ohmic contact by Pd SE with the p^+ prompted source and hence the hole plasma is preserved by the PG. Therefore, role of UST becomes meaningless for Pd SE so the drain current remains unchanged with or without UST model application. Also, the maximum drain current is obtained for Pd SE, which justifies the above discussion of ohmic contact formation at the Pd SEM/S interface. The result is supported by the highest BTBT rate of electrons at the S/C interface in Pd SE shown in **Fig. 6.6(a)**. It is inferred that along with BTBT (S/C interface) the Schottky tunneling (SEM/S interface) is equally significant in defining the conduction of HJLTFET. The drain current for W (Mo) is almost 2.44% (1.56%) enhanced on the inclusion of UST model. The significance of SEM work function comes into play only for the ON state. When no gate bias is applied, the wider hetero-material tunneling barrier restricts the flow of electrons across the S/C interface, such that the effect of SE metal diminishes. For the whole simulation process and result parameters extraction, the work function of CG is kept fixed. So, it is primarily the impact of SE metal work function on the results variation, which describes the role of UST model in formation of Schottky and ohmic contacts.

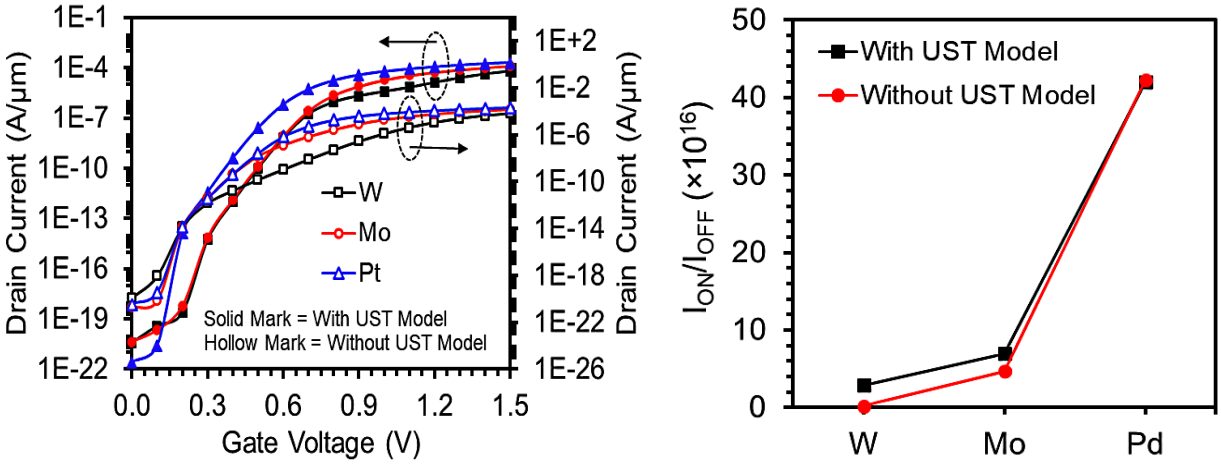


Fig. 6.9. (a) Transfer characteristics and (b) current switching ratio (I_{ON}/I_{OFF}) of HJLTFET for three SE metals [22].

Further, the impact of UST model has been studied for current switching ratio (I_{ON}/I_{OFF}) of HJLTFET for three SE metals W, Mo, and Pd (**Fig. 6.9b**). For SEM work function lesser than p^+ prompted source (W and Mo) there is a noticeable variation of I_{ON}/I_{OFF} with or without UST model. However, for Pd SE having higher work function than p^+ prompted source, there is a negligible variation of I_{ON}/I_{OFF} for both cases. This signifies the importance of the role of SE metal work function being played in the conduction of HJLTFET. The I_{ON}/I_{OFF} ratio of HJLTFET for W (Mo) SE becomes 16 (1.5) times higher on the inclusion of UST model as compared to without UST model case.

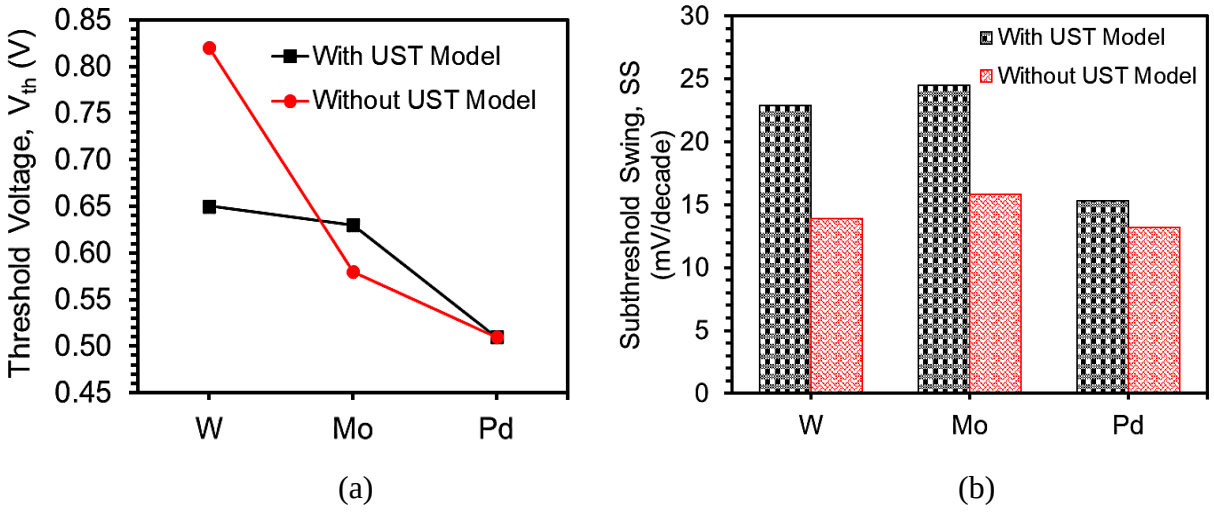


Fig. 6.10. Impact of SE metal work function on (a) Threshold voltage and (b) SS of HJLTFET [22].

Fig. 6.10(a) displays the significance of UST model on the variation of threshold voltage (V_{th}) of HJLTFET for three SE metal work functions. The V_{th} of HJLTFET reduces by 0.79/1.08 times for W/Mo SE with UST model implementation than without the UST model case. This shows the undervalued drain current of HJLTFET (W and Mo) without UST model implementation, whereas, Pd SE preserve the hole plasma in the source region and hence the ohmic contact formed at Pd SEM/S interface shows improved V_{th} in comparison to other two metal SEs. Thus, the comparison of with

and without UST model for Pd SE shows no variation of V_{th}. **Fig. 6.10(b)** shows the comparison of SS for all three SE metal work functions with and without UST model implementation. The variation of SS for Pd SE is marginally increased, whereas the variation is larger in case of other two metal SEs.

6.4 CONCLUSION

This chapter gives the detailed analysis of the influence of different SE metal work functions in the formation of Schottky and ohmic contacts by including the most important UST model in proposed hetero-material InAs/AlGaSb based HJLTFET. The role of different SE metal work functions was evaluated with respect to the polarity gate prompted source region of HJLTFET (p^+ source) for analog performance parameters. It is found that the total current conduction of HJLTFET gets hampered with SEM work function lesser than p^+ prompted source as the hole plasma gets depleted near the SEM/S interface. This results in the formation of Schottky contact leading to the undesired electrons' movement towards the SE. The electrons available for BTBT through S/C interface gets reduced in number, hence hampering the effective conduction of HJLTFET (drain current). Thus, inspite of efficient BTBT of electrons at S/C interface, the formation of Schottky contact abstain the current conduction of HJLTFET (for W and Mo SE work functions). This signifies the requirement of ohmic contact formation at the SEM/S interface in addition to the sufficient band to band tunneling across the S/C interface. Therefore, the SE work function must be higher than the p^+ prompted source forming the ohmic contact at the SEM/S interface to facilitate the effective current conduction in the n-type HJLTFET. Moreover, the UST model must be implemented during the simulations to include the device physics of the Schottky tunneling at the SEM/S interface, which is overlooked otherwise. However, for the fabrication of HJLTFET, the SE with higher work function than the p^+ prompted source must be preferred to ensure effective device functioning.

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CHAPTER-7

SUMMARY AND FUTURE SCOPE

This chapter recapitulates the complete summary of the work carried out in this thesis. The future scope of the work is also presented to extend the research.

7.1 SUMMARY

This thesis comprehends the latest approach of utilizing the tunnel field effect transistor (TFET) instead of the conventional MOSFET owing to its fundamental working principle of quantum band to band tunnelling (BTBT) through the potential barrier rather than thermionic emission of carriers over the barrier (MOSFET). To reduce the fabrication complexity of doping junctions, a junctionless TFET architecture has been implemented along with hetero-material source to channel (S/C) tunnelling interface (HJLTFET) by utilising III-V compound semiconducting binary/binary and binary/ternary materials. Moreover, to improve the performance of HJLTFET, various engineering schemes have been incorporated. A dual metal gate, hetero-material tunneling interfaced junction-less TFET, (DMG-HJLTFET) has been developed by utilizing InAs (low band-gap source material)/GaAs (higher band-gap channel and drain material) in **Chapter 2** based on the band-gap and dual material gate engineering. The 2-D TCAD simulations have been executed to explore the impact of Tunnel gate process variations - work function and length on DC and analog figure of merits (FOMs) of DMG-HJLTFET. The extracted result parameters have also been compared to SMG-HJLTFET and conventional Si-JLTFET. The DMG-HJLTFET attains improved ON current in the range of 88.5×10^{-6} A/µm and OFF current remains as low as 2.89×10^{-16} A/µm. It exhibits a high current switching ratio of 3.1×10^{11} as compared to SMG-HJLTFET ($I_{ON} = 24 \times 10^{-6}$ A/µm and $I_{ON}/I_{OFF} = 1.4 \times 10^{11}$) and Si-JLTFET ($I_{ON} = 7 \times 10^{-6}$ A/µm and $I_{ON}/I_{OFF} = 1.8 \times 10^{6}$). The SS value of DMG-HJLTFET is 52.4% and 88.8% reduced in comparison with SMG-HJLTFET and Si-JLTFET due to the energy-band profile modulation obtained by dual-material gate technology and III-V compound semiconducting materials. The optimum RF FOMs have been obtained in the form of f_{max}, GBP, h_{12}, UPG, Gma reflecting its promising applications in high frequency and microwave regime. whereas, the conventional homo-material Si based device have shown the degraded performance in comparison. Moreover, DMG-HJLTFET is found to have better g_{m3}, VIP2, VIP3, IIP3, IMD3 and 1dB compression point in comparison with SMG-HJLTFET and

Si-JLTFET. Therefore, DMG-HJLTFET can be considered an alternative in the modern wireless and distortion-less communication systems as discussed in **Chapter 2**.

However, the use of conventional low-k material (SiO_2, mono-dielectric) in the oxide region under the control gate nearby the source side and drain side lowers the ON current by producing the ambipolar conduction in the device. Also, high-k dielectric materials (mono-dielectric) enhance the leakage current. Therefore, a heterogeneous gate dielectric engineering is executed in the **Chapter 3** by developing a heterogeneous gate dielectric stack having high-k and low-k material in the oxide region under CG nearby the source and drain regions, respectively. The performance of HD-HJLTFET has been compared with mono-dielectric high-k HJLTFET and low-k HJLTFET. The selection of an appropriate high-k oxide for the hetero dielectric and length of the high-k oxide in HD-HJLTFET has been optimized using different dielectric materials - HfO_2 (k = 25), ZrO_2 (k = 22), Al_2O_3 (k = 9), Si_3N_4 (k = 7), and SiO_2 (k = 3.9) in the high-k region. This study indicated the HD-HJLTFET to be an alternate to conventional mono-dielectric devices for high switching applications.

Further, to induce a tunable bandgap tunnelling interface at the S/C interface of H-JLTFET, GaAs used in **Chapter 2** has been replaced by the ternary (AlGaSb) compound semiconducting material in **Chapter 4**. The material is chosen because of the tunable bandgap property, where the bandgap of AlGaSb can be modified by changing the mole fraction of Al to induce a charge plasma based tunable bandgap arsenide/antimonide tunneling S/C interface. The superior performance is attributed to the conduction band local minima induced at the channel yielding to narrower tunneling barrier width at an optimized Al-mole fraction (0.15) of AlGaSb. 77 times higher g_m of H-JLTFET led to 5×10^6 and 205 times higher device efficiency and f_T along with ~66% reduction in the parasitic capacitance making it favorable for high-speed switching applications as compared to Si JLTFET.

The interface trap charges (ITCs) at the semiconductor/oxide interface originating during the fabrication process of electronic device plays an important role in reliability issues. The device

characteristics should be analysed in the presence of these ITCs to ensure the reliability. In **Chapter 5**, the impact of semiconductor/oxide ITCs density and polarity – positive ITCs (donor) and negative ITCs (acceptor) has been examined for analog/RF FOMs. In this chapter, the hetero dielectric engineering has been implemented in HJLTFET discussed in **chapter 4** to improve its immunity in terms of performance variation with different ITCs polarity compared to low-k dielectric device (HJLTFET). The high-k dielectric towards S/C interface and low-k dielectric towards D/C interface in HD-HJLTFET results in enhanced performance with negligible variation against different ITC polarity than its counter device.

To analyse the importance of Schottky and ohmic contacts **Chapter 6** features a comprehensive investigation of the mutual significance of polar gate (PG) and source electrode metal (SEM) work function on the retention of hole plasma in the p^+ prompted source to study the key analog characteristics of HJLTFET developed in **Chapter 4**. For that purpose, three metals – W (4.55 eV), Mo (4.65 eV), and Pd (5.3 eV) have been considered for simulation of HJLTFET. It is found that the total current conduction of HJLTFET gets hampered with SEM work function lesser than p^+ prompted source as the hole plasma gets depleted near the SEM/S interface. This results in the formation of Schottky contact leading to the undesired electrons' movement towards the SE. The electrons available for BTBT through S/C interface gets reduced in number, hence hampering the effective conduction of HJLTFET (drain current). Thus, inspite of efficient BTBT of electrons at S/C interface, the formation of Schottky contact abstain the current conduction of HJLTFET (for W and Mo SE work functions). This signifies the requirement of ohmic contact formation at the SEM/S interface in addition to the sufficient band to band tunneling across the S/C interface. Therefore, the SE work function must be higher than the p^+ prompted source forming the ohmic contact at the SEM/S interface to facilitate the effective current conduction in the n-type HJLTFET. However, for the fabrication of HJLTFET, the SE with higher work function than the p^+ prompted source must be preferred to ensure effective device functioning.

7.2 FUTURE SCOPE

The prime objective of this thesis is to design a TFET device which can overcome the limitations of conventional TFET architecture and fabrication complexity by introducing various device and material engineering techniques. The immunity of proposed device against various interface trap charges polarity and density has also been investigated to ensure the reliability of the device. The importance of choice of source electrode metal work function has also been studied to analyse the ohmic and Schottky contacts formation at the source electrode metal/p^+ prompted source. However, there are a few objectives which can be explored as the future aspects as follows

1. Temperature analysis can be performed to study the application of the HJLTFET for a wide range of temperature.
2. Circuit analysis of HJLTFET can be done to investigate the possibility of HJLTFET for digital circuit applications like RAM, gated logic designs, and CMOS inverters.
3. HJLTFET can be implemented in sensing applications as a biochemical sensor, which can sense both bio-molecules such as glucose, DNA, proteins, cancer and harmful gases.
4. To study the impact of mobile charges at the Semiconductor/oxide interface of HJLTFET for reliability issues.
5. Noise analysis can be performed on HJLTFET, to study the noise FOMs such as Noise Figure, Cross-Correlation, and Auto- Correlation for the designing of Low-Noise Amplifiers.

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ORIGINAL ARTICLE

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Impact of tunnel gate process variations on analog/radio frequency (microwave) and small signal parameters of hetero-material tunneling interfaced charge plasma junctionless tunnel field effect transistor

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Abstract

This paper proposes a dual metal gate, hetero-material tunneling interfaced junctionless tunnel field effect transistor (TFET), (DMG-HJLTFET), utilizing III–V compound semiconducting materials, InAs (low band-gap source material)/GaAs (higher band-gap channel and drain material) by applying the band-gap and dual material gate engineering. The 2-D TCAD simulations have been executed to explore the impact of tunnel gate process variations—work function and length on DC and analog figure of merits (FOMs) of DMG-HJLTFET. The extracted result parameters have also been compared to SMG (single metal gate)-HJLTFET and conventional Si-JLTFET. The DMG-HJLTFET attains improved ON current in the range of 88.5×10^{-6} A/μm and OFF current remains as low as 2.89×10^{-16} A/μm. It exhibits a high current switching ratio of 3.1×10^{11} as compared to SMG-HJLTFET ($I_{ON} = 24 \times 10^{-6}$ A/μm and $I_{ON}/I_{OFF} = 1.4 \times 10^{11}$) and Si-JLTFET ($I_{ON} = 7 \times 10^{-6}$ A/μm and $I_{ON}/I_{OFF} = 1.8 \times 10^{6}$). Further, the radio frequency/microwave (RF) parameters such as power gains (h_{12}, UPG, and Gma), f_{max}, and GBP have been compared for all three aforementioned devices. Moreover, the small signal admittance (Y) parameters have been examined to explore the possible scope of DMG-HJLTFET for future internet of everything communications and fast switching applications.

KEYWORDS

band to band tunneling, dual material gate, gallium arsenide, junctionless tunnel FET, radio frequency

1 | INTRODUCTION

Tunnel field effect transistors (TFETs) have attracted considerable interest in being energy-efficient devices and have been used in low power applications as compared to MOSFETs because of low leakage current along with steeper subthreshold slope (SS). The SS of conventional MOSFETs is limited to a value greater than 60 mV/decade at 300 K. The performance degradation of MOSFET is due to its fundamental mechanism of thermionic emission of the carriers over the potential barrier, whereas TFET works on the principle of quantum tunneling of carriers through the potential

barrier.[1–3] MOSFET suffers from various unwanted issues like SCEs, high leakage current, DIBL, and SS > 60 mv/decade.[4–6] TFET is immune to these severe issues except the problem of low ON-current (I_{ON}),[7,8] ambipolar conduction, and inadequate high-frequency response.[9] However, lower value of I_{ON} is an eminent issue, which need to be resolved along with keeping its leakage current and SS unelevated. The prime reason for low I_{ON} is the large bandgap of Si (∼1.1 eV),[10,11] which brings on an inadequate quantum band-to-band tunneling through the barrier. This hitch can be solved by employing low bandgap semiconducting materials or III–V compound semiconducting materials like $InAs, GaAs, InP, SiGe$[12–16]; however, it becomes challenging to use III–V compound semiconducting materials for making selective oxide formation due to the problem of lattice incongruity.

In the downscaling approach, fabrication of doping junctions in TFETs becomes a tedious and expensive task. One of the alternative devices proposed in past few years is JLFET based on the principle of Lilienfeld's architecture of first transistor.[17] Owing to the absence of doping junction, it makes the fabrication process very smooth and effortless. TFET constitutes efficient electrical parameters than MOSFET, however, suffers from the problem of large SS just like MOSFET.[18–20] Recently, many research papers have addressed the proposal of a new architecture named junctionless TFET (JLTFET), which consolidates the benefits of a JLFET (elevated I_{ON}) and a TFET (low SS).[21] A JLTFET is a uniformly doped junctionless TFET, whose fundamental mechanism of carrier polarity induction is charge plasma. The basic idea of charge plasma concept is to convert a highly doped $n^+ - n^+ - n^+$ substrate into the conventional $p^+ - i - n^+$ substrate by using two different work function gates as the polar gate (PG) and a control gate (CG).[11,16] By using charge plasma concept, the involuted fabrication processes, arbitrary doping fluctuations, and scalability issues can be reduced adequately.

In this paper, we have introduced a novel amalgamation of III–V compound semiconducting materials, InAs (lower bandgap,[22]) and GaAs (higher bandgap,[14]) as the source and channel materials in a hetero-material tunneling interfaced single metal gate (SMG) junctionless device (SMG-HJLTFET). The prime reason of using an amalgamation of InAs and GaAs is the larger energy bandgap and higher carrier mobility obtained at the source/channel (S/C) interface of the hetero-material structure in comparison to Si-JLTFET, which represents the homo-material based JLTFET device, whose parameters are similar to Han et al.[23] The energy bandgap of InAs and GaAs is 0.35 and 1.42 eV, respectively.[24] Furthermore, in order to enhance the result characteristics of SMG-HJLTFET, we incorporated the dual material gate (DMG) engineering by dividing the CG of SMG-HJLTFET into a tunnel gate (TG) and a supplementary gate (SG). The prime utility of TG is to improve the excavation of the carriers at the S/C interface; accordingly, the position of TG is optimized toward the S/C interface. The SG is used to increase the barrier height by placing it toward the channel/drain (DC) interface. The TG and SG work-functions are optimized to embellish the DC and analog/RF characteristics of the device. The improvement of the result characteristics is also examined against SMG-HJLTFET and conventional Si-JLTFET.

2 | DEVICE STRUCTURE

This work is based on an n-type DMG-HJLTFET presented in Figure 1A. We also compared our proposed device with SMG-HJLTFET and Si-JLTFET having the same parameters as shown in Table 1. The dimensions of the proposed device have been considered within the range prescribed by the ITRS roadmap.[25] We used a double gate technology to increase the gate controllability over the channel. We employed two isolated gates as the PG and CG in SMG-HJLTFET and Si-JLTFET, which have different work functions to achieve the required carrier concentration in the source and channel region, respectively. The drain region is reserved at the same doping concentration. The PG is utilized to induce p^+ source region and CG is used to make the channel intrinsic. Further, a dual material technique is used in CG, where the overall CG length ($L_{CG} = L_{tun} + L_{sup}$), is distributed into TG ($L_{tun} = 4$ nm) and SG ($L_{sup} = 16$ nm). The ON state corresponds to $V_{GS} = 1.5$V, $V_{DS} = 1.5$V, and OFF state corresponds to $V_{GS} = 0.0$V, $V_{DS} = 1.5$V.

3 | MODEL VALIDATION

3.1 | Simulation methodology

The entire device simulations were executed through a 2-D device simulator, Silvaco-ATLAS.[24] We applied the nonlocal BTBT model to evaluate the band-to-band electron tunneling rate along the S/C interface. The band gap

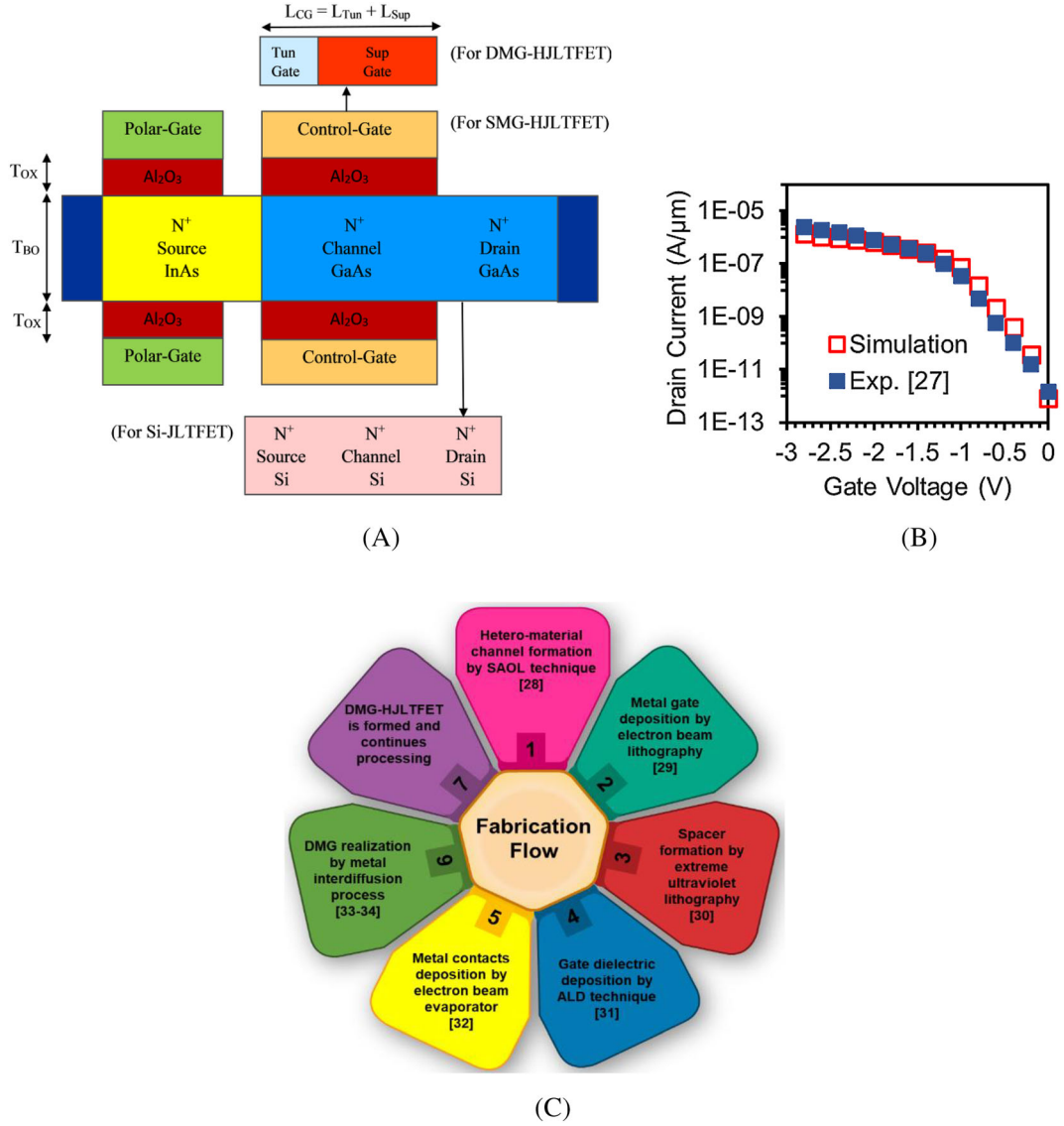

FIGURE 1 (A) Device schematic structure, (B) calibration plot, and (C) fabrication process flow of proposed dual metal gate, hetero-material tunneling interfaced junctionless tunnel field effect transistor (DMG-HJLTFET) [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 1 Device design parameters

Parameters	Si JLTFET	SMG HJLTFET	DMG HJLTFET	Units
Gate length (L_{CH})	20[23]	20	20	nm
Oxide thickness (T_{OX})	2	2	2	nm
Isolation thickness (T_{ISO})	2	2	2	nm
Body thickness (T_{BO})	3[23]	3	3	nm
Polar gate length (L_{PG})	15	15	15	nm
control gate length (L_{CG})	20	20	20	nm
PG Work function (ϕ_{PG})	5.93	5.93	5.93	eV
CG Work function (ϕ_{CG})	4.3	4.5	—	eV
TG Work function (ϕ_{tun})	—	—	4.1	eV
SG Work function (ϕ_{Sup})	—	—	4.5	eV

narrowing model (BGN) and Auger recombination model are also enabled for estimating the channel region doping concentration. We also invoked the CVT model (Lombardi) to comprehend the consequences of mobility dependent on concentration, parallel-perpendicular electric field, and temperature. The SRH recombination model and Fermi Dirac statistics are implemented to perform the calculations of intrinsic carrier concentration. For further accuracy, the quantum confinement (QC) model given by Hansch[26] is also applied.

3.2 | Calibration

Due to the lack of experimental data available for InAs/GaAs based TFET, we calibrated the simulation models of our proposed device with the information extracted from a fabrication-based research work,[27] in order to authenticate the model parameters and the device measurements. We deliberated all the device parameters and biasing conditions of our device exactly the same as that of the published results reported in Zhao et al.,[27] for the calibration purpose. Figure 1B illustrates the comparison of the I_dV_g characteristics obtained from the extracted data of the experimental work[27] and our simulations. It validates all the model parameters due to the close propinquity of the compared results. Figure 1C illustrates the step-by-step fabrication process flow of the proposed device. The hetero-material source/channel interface is formed using the self-aligned optical lithography technique reported in Zhou et al.[28] Thereafter, the electron beam lithography and ultraviolet lithography are used to deposit the metal gates and spacer region.[29,30] Then, the dielectric layer is deposited using atomic layer deposition[31] and metal contacts are formed using electron beam evaporation.[32] Furthermore, the DMG engineering architecture can be implemented by two ways—the tilt angle evaporation technique[33] and metal interdiffusion process.[34] Thus, the DMG-HJLTFET can be fabricated using the above device design outlines, in which the significance of hetero-material S/C interface and GME engineering scheme have been united with JLTFET for achieving improved characteristics.

4 | RESULTS AND DISCUSSION

4.1 | Comparative performance analysis of basic device characteristics

This subsection presents the impact of InAs/GaAs hetero-material based S/C tunneling interface and the DMG application on the electrical characteristics of DMG-HJLTFET in the form of energy band diagram, carrier concentration, band-to-band electron tunneling rate, transfer characteristics and transconductance (g_m), and compared the same with SMG-HJLTFET and Si-JLTFET devices. Figure 2A,B represents the enhancement of DMG-HJLTFET characteristics over SMG-HJLTFET and Si-JLTFET in terms of energy diagram for the OFF and ON state, respectively, at a depth of

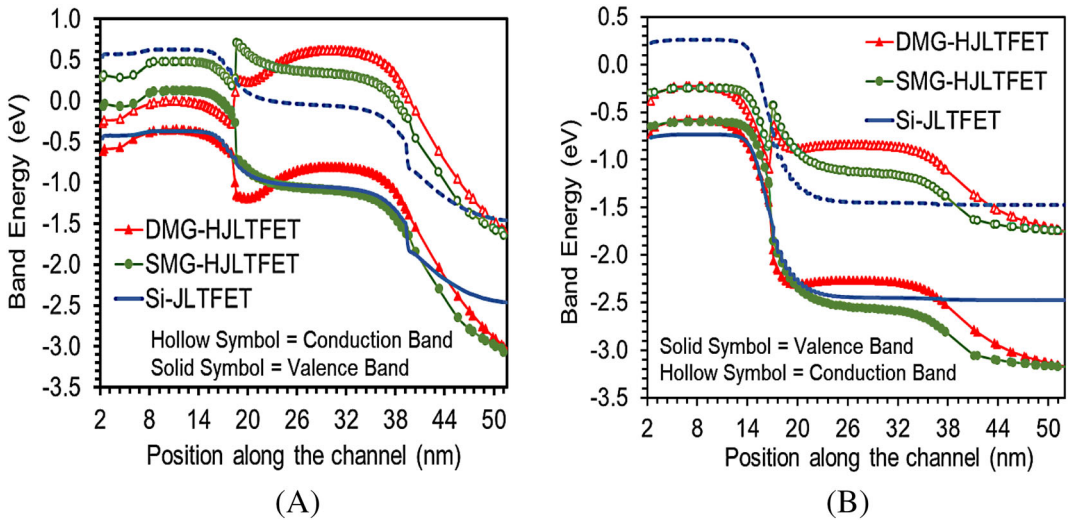

FIGURE 2 (A) OFF state and (B) ON state energy diagram along *x* direction [Colour figure can be viewed at wileyonlinelibrary.com]

1 nm below the channel surface. The TG work function (ϕ_{tun}) is kept smaller than SG work function (ϕ_{sup}). When we do not apply any bias (OFF state), the conduction band of the channel is fetched up. The tunneling barrier thickness at the S/C boundary becomes much wider and thus prevents the overlapping of the bands. As an outcome, the electrons' tunneling probability from source to channel is negligible, which yields merely an inconsequential leakage current. Hence, the BTBT rate is reduced, and the I_{ON}/I_{OFF} ratio is improved for DMG-HJLTFET in comparison with SMG-HJLTFET and Si-JLTFET. In the ON state, with the gradual increment in the gate voltage, the low band gap *InAs* source and ϕ_{tun} dragged down the conduction band to the left of the S/C boundary. The tunneling barrier becomes narrow and the electrons can easily excavate through the S/C interface, in DMG- HJLTFET.

The I_{ON} surges exponentially with a fall in the tunneling barrier wideness. The high-k oxide material is accustomed to improve the I_{ON} parameter. However, Si-JLTFET leads to wider tunneling barrier due to its higher energy band gap, and hence, the I_{ON} degrades in comparison to the other two devices (Figure 2B). Figure 3A,B represents the electron-hole concentration in the OFF and ON state for the three aforementioned devices at a depth of 1 nm below the channel surface. By using appropriate CG and PG work functions (ϕ_{CG} and ϕ_{PG}) in the channel and source region, respectively, the device attains conventional $p^+ - i - n^+$ doped conformation without any physical doping (Figure 3A,B).

The HJLTFETs being quantum mechanical devices conduct the current through a different mechanism called band-to-band tunneling of carriers across the S/C interface, which is associated to the barrier thickness. Figure 4A represents the BTBT electron tunneling rate alongside the channel direction, which depends upon the gate voltage and gate dielectric material as well. On the application of lower work function metal as TG, the excavation of charge carriers gets shifted toward the left of the interface. Thus, improves the I_{ON} of the device as compared to the other two. Figure 4B indicates the deviation of drain current and g_m with gate voltage, which vindicates the prominent electrostatic reliability of DMG-HJLTFET over SMG-HJLTFET and Si-JLTFET. The g_m is an imperative factor providing the gain of the device as a function of V_{GS} for analog circuit designs. In order to achieve high frequency and analog characteristics, the g_m should be upraised. In Figure 4B, the g_m of DMG-HJLTFET is highest and Si-JLTFET has the least value of g_m among the three devices. In DMG-HJLTFET, the I_{ON}, and hence the switching ratio, I_{ON}/I_{OFF}, is also improved using the dual metal gate configuration, which is quite low SMG-HJLTFET and Si-JLTFET.

Figure 4C shows the comparison of intrinsic gain, ($A_v = g_m * R_o$) of the three aforementioned devices, where A_v of DMG-HJLTFET increases with rise in gate voltage and attains ~17 orders higher value of A_v in comparison to SMG-HJLTFET and ~157 orders higher value of A_v than Si-JLTFET. The higher A_v is desirable for improved analog performance. Such an escalation in A_v is the result of increase in g_m of DMG-HJLTFET, because of the direct dependence of A_v on g_m (shown in Figure 2C). The output characteristics of the aforementioned devices for $V_{GS} = 1.5\ V$ are displayed in Figure 4D (both log and linear scale). The drain current of DMG-HJLTFET starts rising for lower value of V_{DS} and after a certain limit, the drain current becomes independent of V_{DS} and finally saturates. The higher tunnel coupling offered by DMG-HJLTFET attributes to an earlier saturation point with higher drain current, whereas the other two devices exhibit lower drain current and delayed saturation at a higher drain voltage.

Figures 5 and 6 demonstrate the 2-D level curves of Si-JLTFET, SMG-HJLTFET, and DMG-HJLTFET, respectively, revealing the electric field and BTBT electron tunneling rate curves along the device length. In the ON state, the level

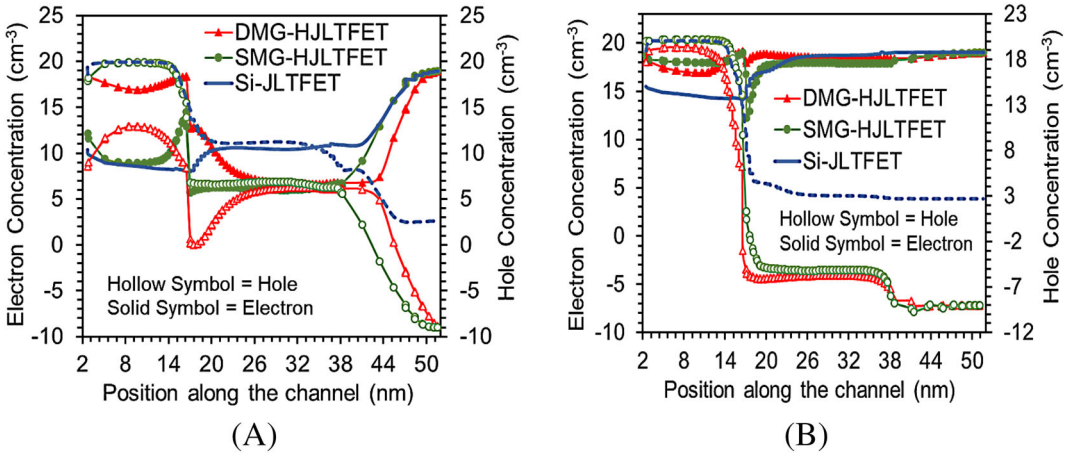

FIGURE 3 (A) OFF state and (B) ON state electron and hole concentration along *x* direction [Colour figure can be viewed at wileyonlinelibrary.com]

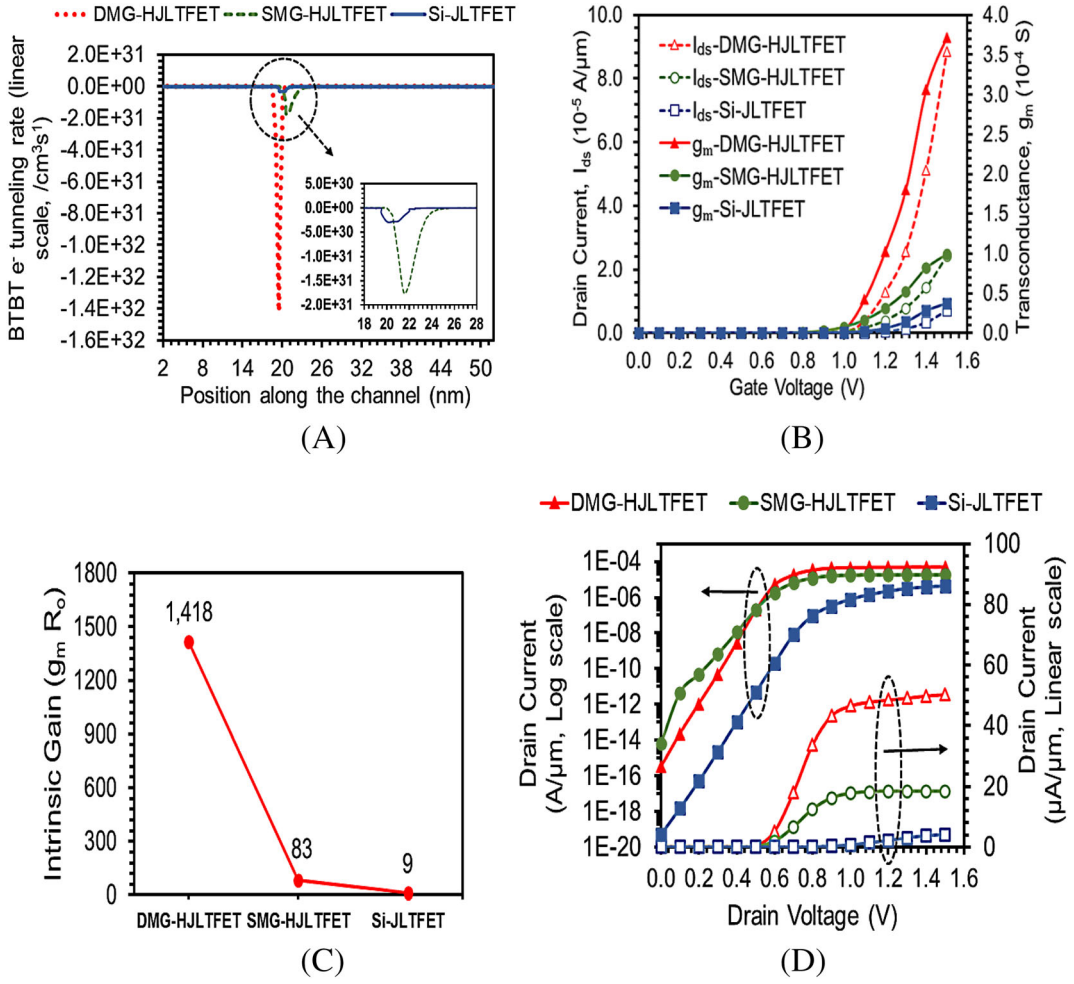

FIGURE 4 (A) Electron tunneling rate alongside the channel, (B) disparity of drain current and transconductance, (C) intrinsic gain, and (D) output characteristics of dual metal gate, hetero-material tunneling interfaced junctionless tunnel field effect transistor (DMG-HJLTFET), single metal gate (SMG)-HJLTFET, and Si-JLTFET at $V_{GS} = 1.5\,V, V_{DS} = 1.5\,V$ [Colour figure can be viewed at wileyonlinelibrary.com]

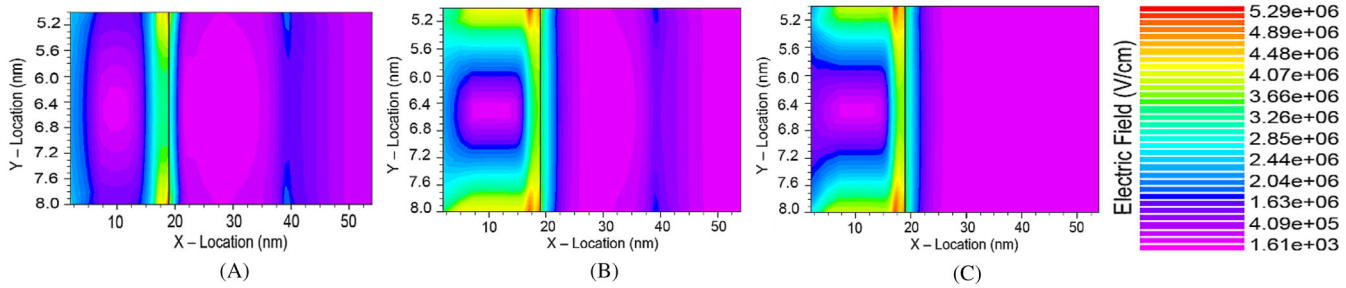

FIGURE 5 Level curve of electric field of (A) dual metal gate, hetero-material tunneling interfaced junctionless tunnel field effect transistor (DMG-HJLTFET), (B) single metal gate (SMG)-HJLTFET, and (C) Si-JLTFET along device length at $V_{GS} = 1.5\,V, V_{DS} = 1.5\,V$ [Colour figure can be viewed at wileyonlinelibrary.com]

curve of electric field varying along the body length specifies a positive extreme value at the S/C interface. Figure 6 displays the level curve of the BTBT electron tunneling rate along the device length, where we observe that the electron tunneling gets shifted toward the left of the interface under the source to channel spacer region in case of DMG-HJLTFET due to the presence of lower ϕ_{tun}, giving rise to the tunneling current at the S/C interface, for all three devices.

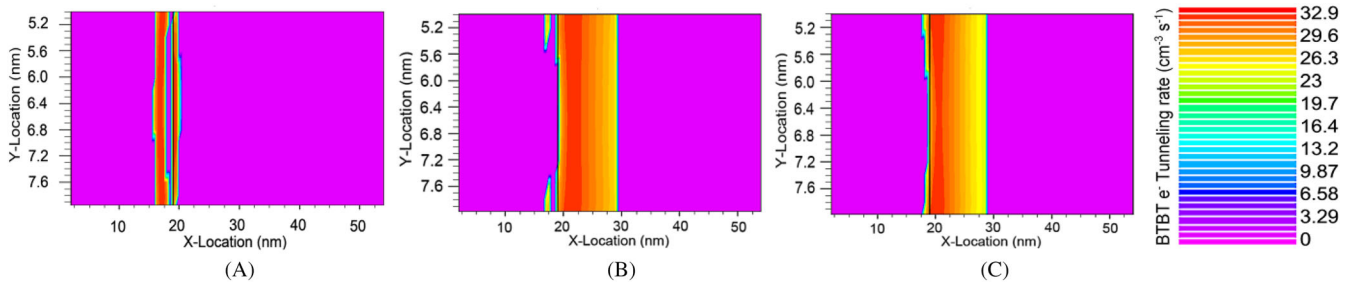

FIGURE 6 Level curve of BTBT e^- tunneling rate of (A) dual metal gate, hetero-material tunneling interfaced junctionless tunnel field effect transistor (DMG-HJLTFET), (B) single metal gate (SMG)-HJLTFET, and (C) Si-JLTFET along device length at $V_{GS} = 1.5\,V, V_{DS} = 1.5\,V$ [Colour figure can be viewed at wileyonlinelibrary.com]

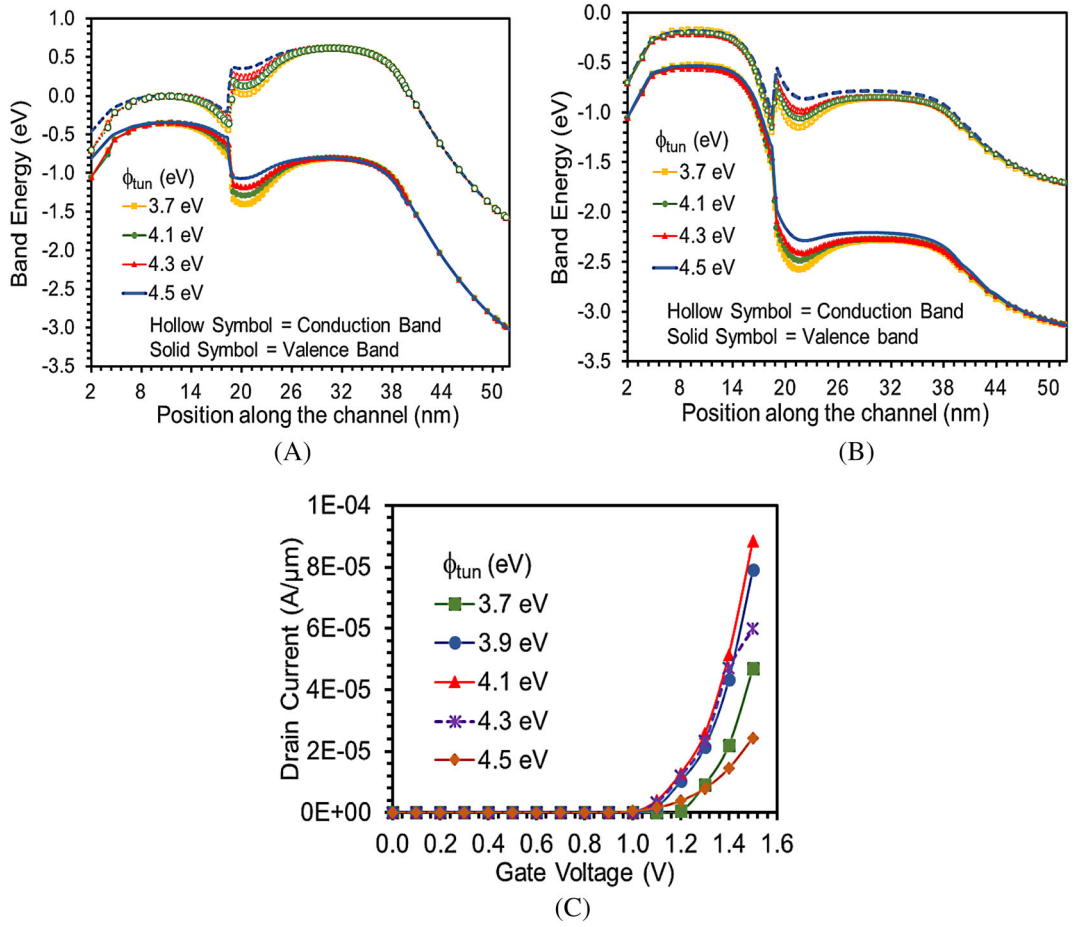

FIGURE 7 (A) OFF state, (B) ON state energy diagram, and (C) Transfer characteristics of dual metal gate, hetero-material tunneling interfaced junctionless tunnel field effect transistor (DMG-HJLTFET) for tunnel gate (TG) work function variation from 3.7 to 4.5 eV at $V_{GS} = 1.5\,V, V_{DS} = 1.5\,V$ [Colour figure can be viewed at wileyonlinelibrary.com]

4.2 | Impact of ϕ_{tun} variation on performance characteristics of DMG-HJLTFET

This subsection describes the optimization and impact of ϕ_{tun} variation from 3.7 to 4.5 eV on DMG-HJLTFET performance. In Figure 7A,B, we examined the relevance of ϕ_{tun} on the energy band profile of DMG-HJLTFET while the ϕ_{sup} is fixed to 4.5 eV. It represents the significance of ϕ_{tun} variation from 3.7 to 4.5 eV in the OFF-ON state, respectively. In the OFF-state on decreasing the ϕ_{tun} from 4.5 to 3.7 eV, there is an escalation in the tunnel barrier width at the S/C

intersection. Hence, the significant overlapping between the conduction band/valence band of the channel/source regions declines. It diminishes the flow of charge carriers through the interface, and hence, the BTBT rate is reduced. In the ON state, the decrement in ϕ_{tun} leads to band bending of conduction band/valence band of the channel/source regions at the S/C interface (Figure 7B). The band bending shifts to the left of S/C interface, promoting higher tunneling rate due to the reduced tunneling barrier width. Hence, I_{ON} rises significantly.

In Figure 7C, the electrical transfer characteristics of DMG-HJLTFET are displayed by varying the ϕ_{tun} from 4.5 to 3.7 eV, keeping the ϕ_{sup} fixed at 4.5 eV. The maximum drain current is achieved for $\phi_{tun} = 4.1$ eV, where the I_{ON} increases by 3.6 orders in magnitude than $\phi_{tun} = 4.1$ eV and 1.8 orders in magnitude than $\phi_{tun} = 3.7$ eV (Figure 7C). The leakage current, I_{OFF} remains almost unaltered (2.89×10^{-16} A/μm to 1.72×10^{-16} for $\phi_{tun} = 4.1$ eV to $\phi_{tun} = 4.5$ eV).

Figure 8A illustrates the I_{ON} and I_{OFF} by varying the ϕ_{tun} from 3.7 to 4.5 eV. The I_{ON} starts increasing as we vary the ϕ_{tun} from 3.7 eV and becomes maximum at 4.1 eV. On further varying the work function value up to 4.5 eV, the I_{ON} again decreases. The I_{OFF} decreases with the variation of ϕ_{tun} (3.7–4.5 eV). The current switching ratio of DMG-HJLTFET is changing with respect to ϕ_{tun} disparity (3.7–4.5 eV, Figure 8B). The simulated results reveal that when we increase the work function mismatch of the CG from 0 to 0.4 eV, the channel conduction band bends downwards and overlaps with the source valence band at the S/C interface. This leads to a higher I_{ON} and steeper SS. The further mismatch of the ϕ_{CG} leads to decrement in the current switching ratio. The optimized results are obtained at 0.4 eV work function difference. The I_{ON} of DMG-HJLTFET is about 3.6 orders higher in magnitude, and the SS value is 52.4% less than SMG-HJLTFET, and the I_{ON} is about 12.6 orders higher in magnitude and the SS value is 88.8% less than Si-JLTFET.

Figure 9A shows the transfer characteristics of single metal gate HJLTFET having ϕ_{CG} 4.1 eV, 4.5 eV, and dual metal gate HJLTFET (CG is divided into TG and SG, ($L_{CG} = L_{tun}$, 4 nm + L_{sup}, 16 nm)) having $\phi_{tun} = 4.1$ eV and $\phi_{sup} = 4.5$ eV. The I_{ON} for 4.1 CG-HJLTFET rises to 128 μA/μm, and the I_{OFF} is 1.89×10^{-10} A/μm, so the I_{ON}/I_{OFF} is 6.7×10^{5}, which is very poor as compared to DMG-HJLTFET and SMG-HJLTFET (4.5 CG) as discussed earlier. The SS of DMG-HJLTFET-4.1 TG + 4.5 SG (13.8 mV/decade) is also smaller as compared to SMG-HJLTFET-4.5 CG (29.03 mV/decade) and SMG-HJLTFET-4.1 CG (123.5 mV/decade) as shown in Figure 9B, reflecting its effectiveness in low leakage-improved performance application. The inset of Figure 9B illustrates the comparison plot of SS of three devices.

4.3 | Impact of L_{tun} variation on performance characteristics of DMG-HJLTFET

This subsection describes the optimization of L_{tun} in DMG-HJLTFET by varying the L_{tun} from 4 to 10 nm. Figure 10A displays the OFF-state energy diagram demonstrating position of bands in DMG-HJLTFET alongside the channel

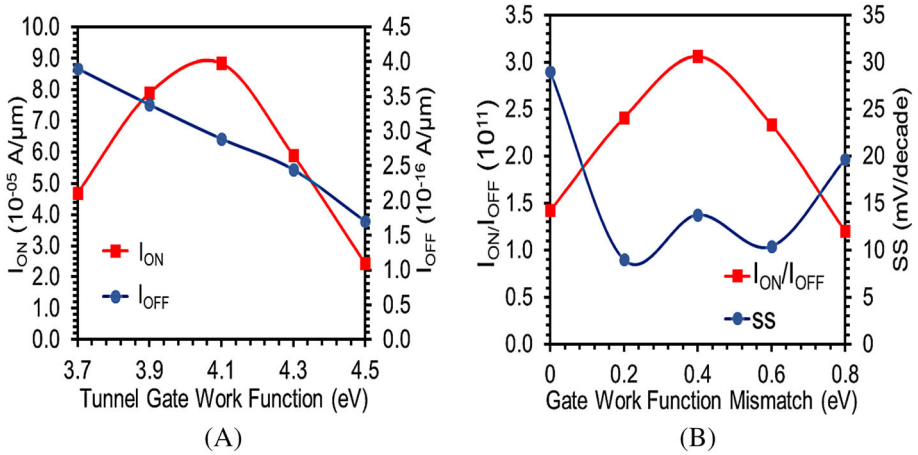

FIGURE 8 (A) ON current and current switching ratio (I_{ON}/I_{OFF}) with the tunnel gate work function (ϕ_{tun}) variation. (B) dual metal gate, hetero-material tunneling interfaced junctionless tunnel field effect transistor (DMG-HJLTFET) current switching ratio and subthreshold slope (SS) variation with gate work function disparity [Colour figure can be viewed at wileyonlinelibrary.com]

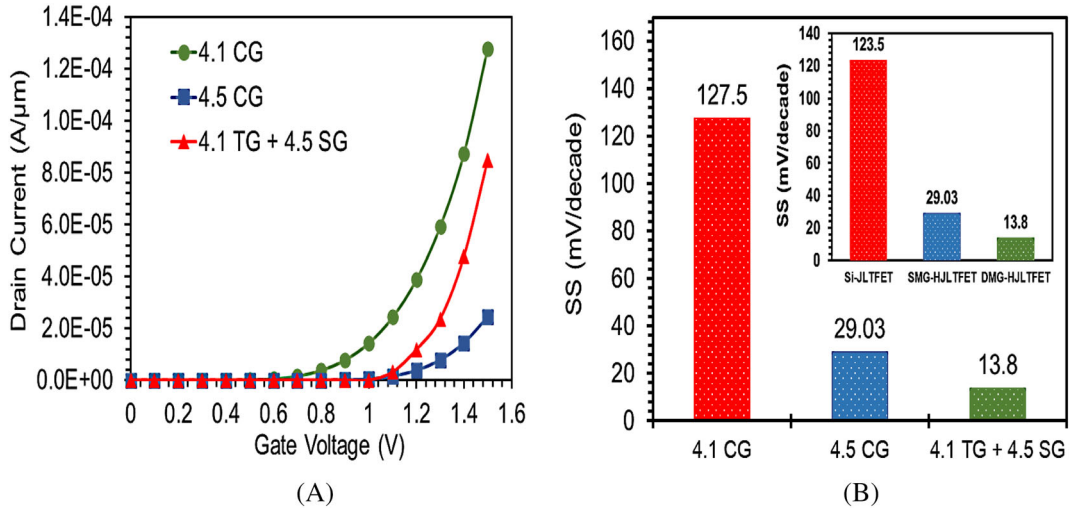

FIGURE 9 (A) Transfer characteristics and (B) sub-threshold slope (SS) of dual metal gate, hetero-material tunneling interfaced junctionless tunnel field effect transistor (DMG-HJLTFET) (4.1 TG + 4.5 SG), single metal gate (SMG)-HJLTFET (4.5 CG and 4.1 CG). (Inset) SS of three aforementioned devices [Colour figure can be viewed at wileyonlinelibrary.com]

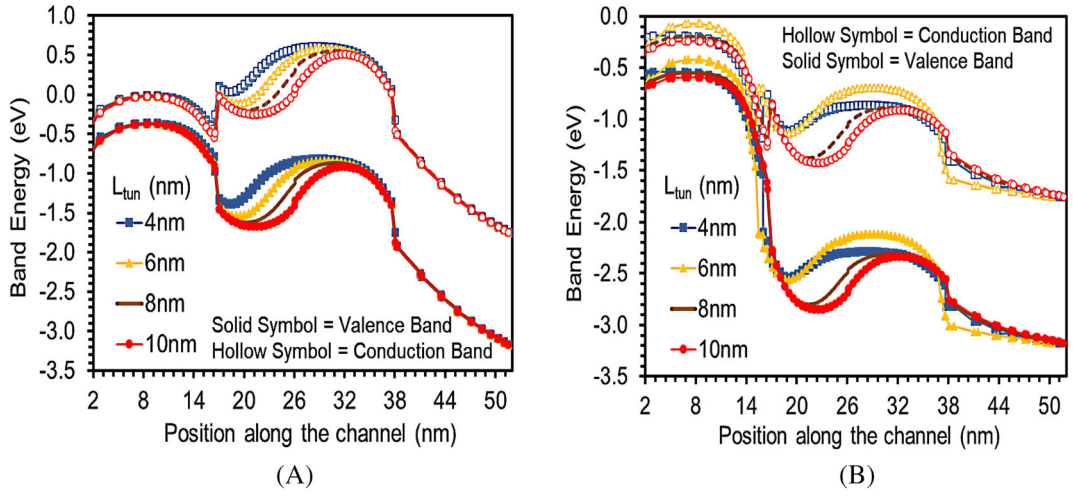

FIGURE 10 (A) OFF state and (B) ON state energy diagram of dual metal gate, hetero-material tunneling interfaced junctionless tunnel field effect transistor (DMG-HJLTFET) with tunnel gate length varying from 4 to 10 nm [Colour figure can be viewed at wileyonlinelibrary.com]

direction on shifting L_{tun} from 4 to 10 nm. When we increase L_{tun} beyond 4 nm, the channel conduction band and the source valence band start bending downwards. The barrier width becomes narrow, leading to the tunneling of minority carriers across the interface, and hence, leakage current rises. In Figure 10B, when the device is turned on, the distance between the bands across the S/C interface is swayed directly by L_{tun}. The conduction/valence band at the channel/source region starts overlapping. The potential barrier becomes very narrow, contributing to the significant flow of electrons across the interface. The suitable L_{tun} is optimized at 4 nm.

In Figure 11A, the contrast between the I_{ON}/I_{OFF} and I_{ON} of DMG-HJLTFET is displayed with respect to the disparity of L_{tun}. The L_{tun} is increased from 0 to 10 nm, managing the entire CG length unchanged ($L_{CG} = L_{tun} + L_{sup}$). At 0.0 nm L_{tun} (SMG-HJLTFET), the I_{ON} is 24.3 μA/μm and the I_{ON}/I_{OFF} is 1.4×10^{11}. When the L_{tun} starts increasing, the I_{ON} starts rising to 88.5 μA/μm at 4 nm and the I_{ON}/I_{OFF} is 3.1×10^{11}. Once it reaches 8 nm, the I_{ON} falls down (54 μA/μm) and the I_{ON}/I_{OFF} decreases to 1.8×10^{11}. At 10 nm, the I_{ON} rises to 96.9 μA/μm and I_{OFF} escalate sharply to 2.9×10^{-15} A/μm, resulting into lower value of the I_{ON}/I_{OFF} of 5.79×10^{9}. So, the optimized results are obtained at 4 nm L_{tun}. Figure 11B signifies the variation of SS of DMG-HJLTFET by modifying L_{tun} from 0 to 10 nm. At 0 nm L_{tun},

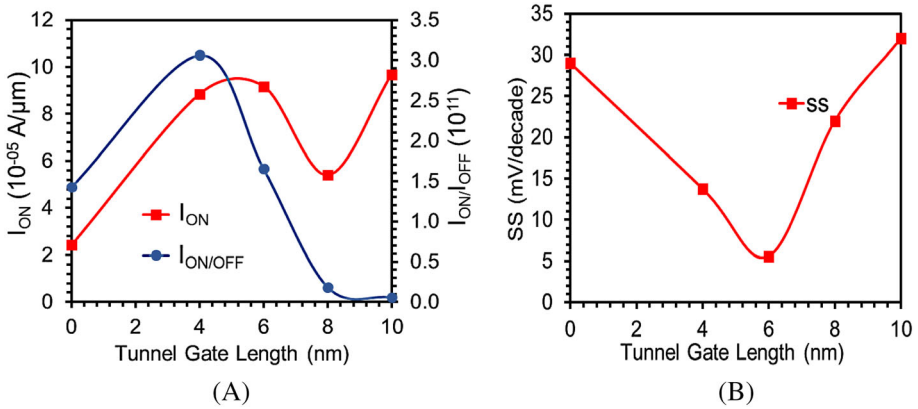

FIGURE 11 (A) Comparison of current switching ratio (I_{ON}/I_{OFF}), ON current (I_{ON}), and (B) sub-threshold slope (SS) for tunnel gate length variation in dual metal gate, hetero-material tunneling interfaced junctionless tunnel field effect transistor (DMG-HJLTFET) [Colour figure can be viewed at wileyonlinelibrary.com]

the SS value is 29.03 mV/decade, which is the value for SMG-HJLTFET; at 10 nm, the SS value is 32 mV/decade. The variation in the SS value is due to the band profile modulation as described before. The optimized value of SS is 13.8 mV/decade at 4 nm L_{tun} due to the better I_{ON}/I_{OFF} and I_{ON}.

4.4 | Comparative Analog/RF Performance Analysis

This section presents the detailed analysis of analog/RF characteristics of the aforementioned three devices. For the designing of TFET based high switching speed circuits, the parasitic capacitances play a vital role. Therefore, the reliance of parasitic capacitances of the aforementioned devices with respect to gate bias has been investigated in this section. Due to the different inversion charge distribution in TFET, the drain bias has lesser impact at the gate/source (G/S) interface and therefore lesser is the impact of C_{gs} (gate source capacitance) on C_{gg} (total gate capacitance, $C_{gg} = C_{gd} + C_{gs}$) in comparison with C_{gd} (gate drain capacitance). As the gate bias is increased, the inversion layer shifts from the drain to the source and hence C_{gd} increases. As there is minor influence of C_{gs} on C_{gg}, therefore, the variation of C_{gg} resembles C_{gd} for DMG-HJLTFET, SMG-HJLTFET, and Si-JLTFET as expressed in Figure 12A,B. Figure 12C illustrates the variation of current gain (h_{21}) of three aforementioned devices with frequency at constant $V_{GS} = 1.5V$ and $V_{DS} = 1.5V$. For the most commonly used cellular communication frequency of the order of 10^6 Hz (1 MHz), the DMG-HJLTFET attains 3.35% and 26.8% higher h_{12} than SMG-HJLTFET and Si-JLTFET, which indicates a substantial enhancement in h_{12} by the application of DMG engineering. This enhancement is attributed to the enhanced I_{ON} and current switching of DMG-HJLTFET as compared to the other two.

Similar pattern is observed with unilateral power gain (UPG) of DMG-HJLTFET as compared to the other two, where DMG-HJLTFET attains 1.63% and 31.4% higher UPG than SMG-HJLTFET and Si-JLTFET for the entire range of frequencies under consideration (Figure 12D). It specifies the comparison of the activity and passivity of two port system and measures the highest achievable power. Hence, DMG and SMG systems are more active than Si-JLTFET for the entire frequency range under consideration. Figure 12E shows the improvement of another important RF parameter, maximum available power gain (Gma) of three aforementioned devices. It is the maximum power gain accessible to the device, which cannot be exceeded. Hence, it is desirable to propose devices with higher Gma. The improved tunneling of carriers and hence higher I_{ON} of DMG-HJLTFET leads to higher Gma (3.6% ↑ and 41.4%↑) as compared to SMG-HJLTFET and Si-JLTFET (Figure 12E).

Figure 13A–C illustrates the disparity of cut off frequency (f_T), maximum oscillation frequency (f_{max}), and gain bandwidth product (GBP) with gate bias for aforementioned devices. The frequency at which the current gain turns to unity (0 dB) is f_T. The value of f_T is considered by extracting g_m, C_{gs}, and C_{gd} using the AC small-signal analysis at an operating frequency of the order of 1 THz along with DC voltage ramped from 0 to 1.5 V. The enhancement in f_T with gate bias for DMG-HJLTFET is due to the enhancement in g_m by the application of DMG engineering (Equation (1)).[28] However, the SMG-HJLTFET attains lower f_T due to the rise in transit time of electrons and degraded parasitic capacitances than Si-JLTFET. Quantitatively, DMG-HJLTFET leads to 3.7 and 1.26 times higher f_T against SMG-HJLTFET

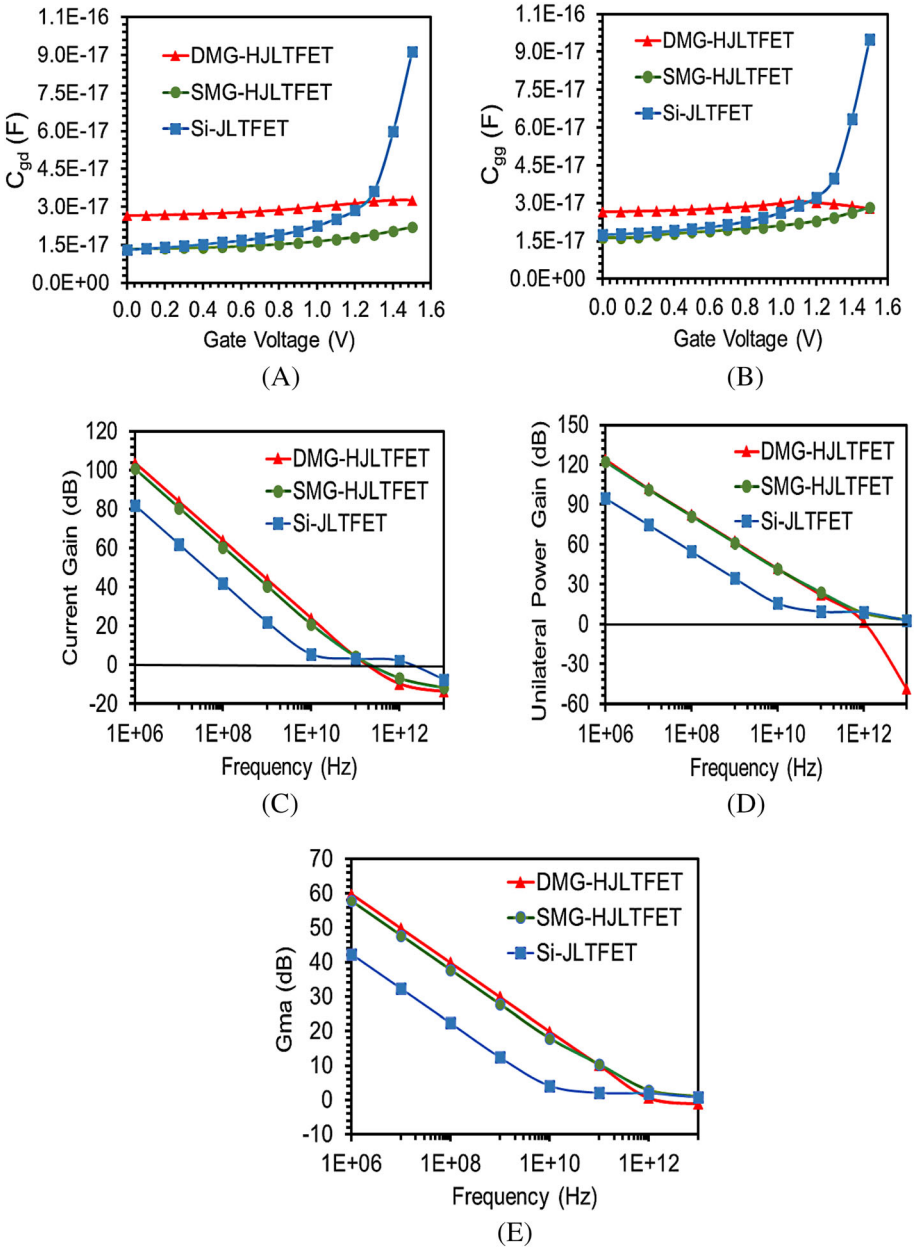

FIGURE 12 Parasitic capacitances (A) C_{gd}, (B) C_{gg}, (C) current gain, (D) unilateral power gain, and (E) maximum available power gain (Gma) [Colour figure can be viewed at wileyonlinelibrary.com]

and Si-JLTFET resulting in highest switching speed among the three (Figure 13A). The Equation (2) illustrates the mathematical expression of f_{max}. It is the frequency at which the maximum unilateral power gain turns to unity (0 dB). The value of f_{max} is calculated by extracting f_T, R_{gd}, and C_{gd} in the same way as done for calculating f_T with DC voltage ramped from 0 to 1.5 V. From Equations (2) and (3),[28] it is clear that f_{max} and GBP depends on g_m and parasitic capacitances, so the variation of both follows almost the same fashion. The GBP represents the product of the bandwidth and gain of an amplifier. The peak value of GBP signifies the frequency at which the device attains maximum gain. In Figure 13B,C, the f_{max} and GBP shows increment with rise in gate bias. The DMG-HJLTFET, SMG-HJLTFET, and Si-JLTFET attain 7.2(0.18) THz, 4.5(0.07) THz, and 3.8(0.006) THz peak value of f_{max} (GBP), respectively at 1.5 V gate bias.

The comparison of the result characteristics of all three devices is shown in Table 2, showing superiority of DMG-HJLTFET among the three devices in terms of analog/RF parameters. Moreover, we have compared the result characteristics of DMG-HJLTFET for $V_{DS} = 0.5$ and 1.5 V in Table 3. From the Table 3, it is clear that the current gain and

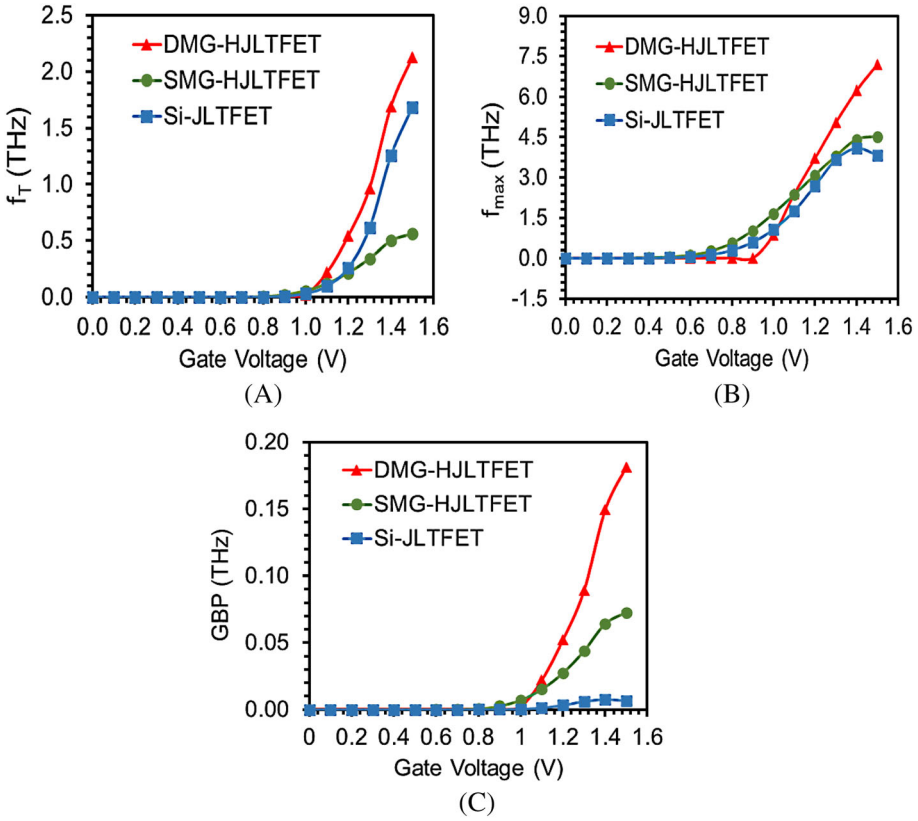

FIGURE 13 Variation of (A) cut-off frequency (f_T), (B) maximum oscillation frequency (f_{max}), and (C) gain bandwidth product (GBP) as a function of gate voltage for dual metal gate, hetero-material tunneling interfaced junctionless tunnel field effect transistor (DMG-HJLTFET), single metal gate (SMG)-HJLTFET, and Si-JLTFET [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 2 Result characteristics of Si-JLTFET, SMG-HJLTFET, and DMG-HJLTFET

	Si-JLTFET	SMG-HJLTFET	DMG-HJLTFET
I_{ON} (μA/μm)	7	24.3	88.5
I_{OFF} (A/μm)	3.87×10^{-12}	1.72×10^{-16}	2.89×10^{-16}
I_{ON}/I_{OFF}	1.8×10^{6}	1.4×10^{11}	3.1×10^{11}
SS (mV/decade)	123.5	29.03	13.8
g_m (S)	0.37×10^{-4}	0.99×10^{-4}	3.7×10^{-4}
f_{max} (THz)	3.8	4.5	7.2
GBP (THz)	0.006	0.07	0.18

TABLE 3 Comparison of result characteristics of DMG-HJLTFET for $V_{DS} = 0.5$V and $V_{DS} = 1.5$V

	$V_{DS} = 0.5$V	$V_{DS} = 1.5$V
I_{ON} (μA/μm)	0.2	88.5
g_m (S)	0.54×10^{-6}	3.7×10^{-4}
Current gain (dB)	33.6	103.9
Gma (dB)	42.5	60

Gma decreases by 209% and 29%, respectively by decreasing the V_{DS} from 1.5 to 0.5 V. Such a substantial decrement in the current gain and Gma may limit the ability of the device to measures the highest achievable power. Also, various other result characteristics (I_{ON} and g_m) show an inferior performance on decreasing the supply voltage. Thus, we have optimized the gate and drain bias to 1.5 V so as to achieve superior RF/analog characteristics.

In RF communication systems, the mathematical modeling and study of the admittance (Y) parameters along with the parasitic capacitances for the small signal equivalent circuits is essential. Such investigation has not been given due attention in charge plasma based junctionless TFET devices. In RF communication systems, modeling the parasitic capacitances in the power area scaling has become very crucial as reported in the 2017 edition of IRDS.[35] As shown in Equations (4) and (5),[25] there is a direct reliance of parasitic capacitances on these Y parameters and frequency. Y_{11}, Y_{22}, Y_{12}, and Y_{21} are the short circuit input admittance, output admittance, forward transfer admittance, and reverse transfer admittance, respectively.

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \tag{1}$$

$$f_{max} = \sqrt{\frac{f_T}{8\pi(R_{gd}C_{gd})}} \tag{2}$$

$$GBP = \frac{g_m}{20\pi(C_{gd})} \tag{3}$$

$$C_{gs} = \frac{Im(Y_{11})+Im(Y_{12})}{\omega} \tag{4}$$

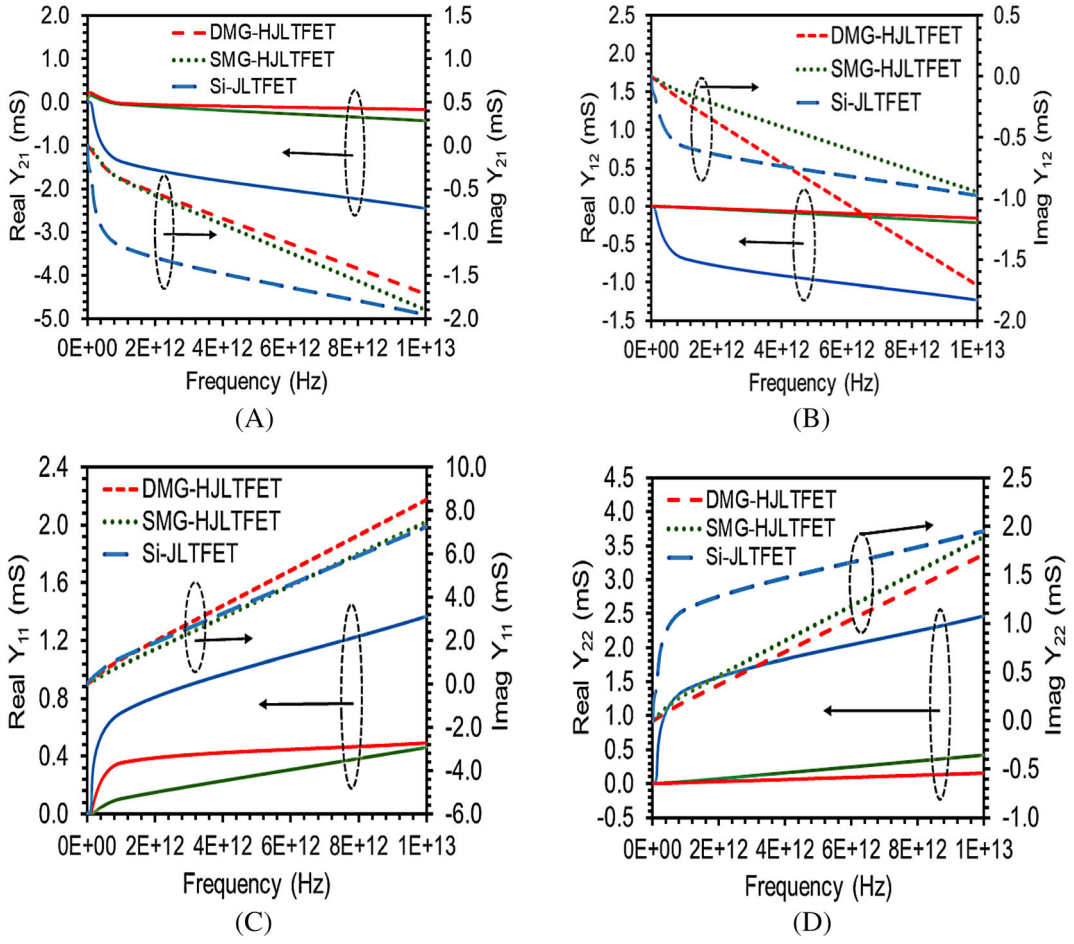

FIGURE 14 The variation of real and imaginary components of the admittance (Y) parameters: (A) Y_{21}, (B) Y_{12}, (C) Y_{11}, and (D) Y_{22} as a function of frequency for dual metal gate, hetero-material tunneling interfaced junctionless tunnel field effect transistor (DMG-HJLTFET), single metal gate (SMG)-HJLTFET, and Si-JLTFET [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 4 Comparison of RF FOMs of DMG-HJLTFET with previously published devices

	DMMG-HJLTFET[15]	HJ-HD-DLTFET[36]	DMG-HJLTFET (present)
C_{gd} (F)	3.6×10^{-15}	8.0×10^{-15}	3.26×10^{-17}
C_{gg} (F)	3.7×10^{-15}	–	2.82×10^{-17}
f_T (GHz)	9.17	107	2120
GBP (GHz)	0.17	16.3	180

$$C_{gd} = \frac{-Im(Y_{12})}{\omega} \tag{5}$$

Figure 14A–D illustrates the comparison of real and imaginary components of Y-parameters of three devices. The Y_{11} and Y_{22} show similar variation of gradual increment with increment in frequency for all three devices; however, the variation of real and imaginary components of Y_{11} and Y_{22} is lower in DMG-HJLTFET and SMG-HJLTFET than Si-JLTFET. The Y_{12} and Y_{21} are gradually decreasing with rise in frequency; however, the magnitude of variation is lower in DMG-HJLTFET and SMG-HJLTFET than Si-JLTFET.

Table 4 presents the comparison of present DMG-HJLTFET device with the recently designed TFET devices,[15,36] showing the superior RF performance of DMG-HJLTFET.

5 | CONCLUSION

This paper has emphasized on the analysis of analog and RF/microwave parameters of our proposed device by optimizing the suitable TG work function and length in the DMG engineered HJLTFET designed with InAs/GaAs compound semiconducting hetero-materials through extensive 2-D simulations. The dual-material gate engineering showed the improved electrostatic characteristics in the form of high I_{ON} and I_{ON}/I_{OFF} in DMG-HJLTFET as compared to SMG-HJLTFET and Si-JLTFET. This study has established a significant band bending at the hetero-material tunneling interface of DMG-HJLTFET leading to narrower barrier width by the application of DMG engineering. The SS value of DMG-HJLTFET is 52.4% and 88.8% reduced in comparison with SMG-HJLTFET and Si-JLTFET due to the energy-band profile modulation obtained by dual-material gate technology and III–V compound semiconducting materials. The optimum RF FOMs have been obtained in the form of f_{max}, GBP, h_{12}, UPG, and Gma reflecting its promising applications in high frequency and microwave regime, whereas the conventional homo-material Si based device has shown the degraded performance in comparison. The h_{12} (UPG) of DMG-HJLTFET is 3.35% and 26.8% (1.63% and 31.4%) higher than SMG-HJLTFET and Si-JLTFET. Besides all the advantages of the proposed device, the improvement in the small signal admittance (Y) parameters on the amalgamation of DMG and band-gap engineering techniques makes the device suitable for future high-speed switching and IOE communication systems.

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CONFLICT OF INTEREST
The authors declare no conflicts of interest.

AUTHOR CONTRIBUTION
Samriti Sharma: Conceptualization, methodology, software, data curation, writing–original draft preparation. **Rishu Chaujar**: Supervision, reviewing and editing.

DATA AVAILABILITY STATEMENT
Data sharing is not applicable to this article as no datasets were generated or analyzed during the current study.

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PAPER

Influence of source electrode metal work function on polar gate prompted source hole plasma in arsenide/antimonide tunneling interfaced junctionless TFET

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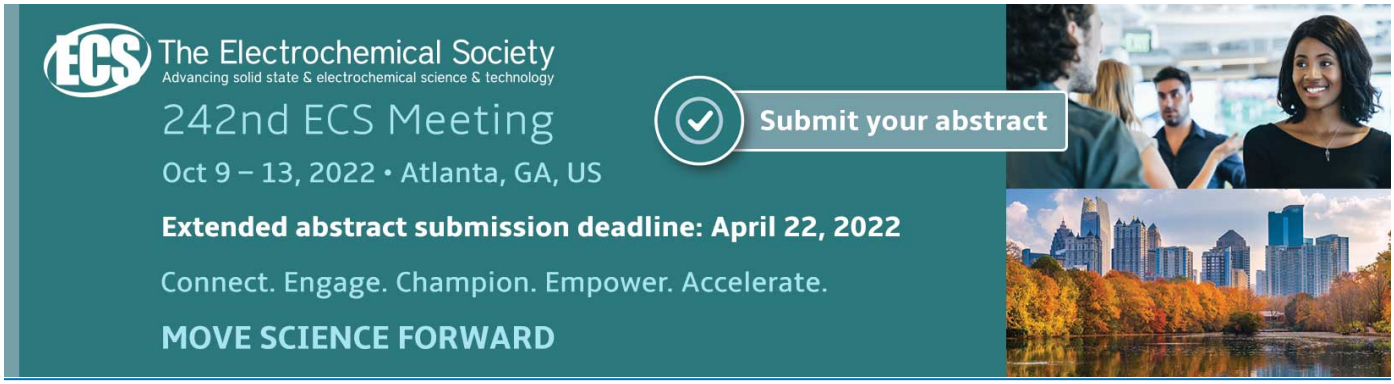

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Influence of source electrode metal work function on polar gate prompted source hole plasma in arsenide/antimonide tunneling interfaced junctionless TFET

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Abstract

Numerous studies have explored the impact of control gate and polar gate (PG) on the retention of hole and electron charge plasma to induce the source and channel region polarity in junctionless tunnel field effect transistor (JLTFET). However, PG is not the only one responsible for the retention of hole plasma in the p^+ prompted source but the hole plasma near the interface of source electrode metal (SEM) and p^+ prompted source (SEM/S) is influenced by the choice of SEM work function too. This paper features a comprehensive investigation of the mutual significance of PG and SEM work function on p^+ prompted source to study key analog characteristics of arsenide/antimonide tunneling interfaced hetero-material JLTFET (HJLTFET), which is unexplored in the literature otherwise. We have considered three metals—W (4.55 eV), Mo (4.65 eV), and Pd (5.3 eV) as the source electrodes in HJLTFET. For SEM work function lesser than p^+ prompted source (W and Mo), the Schottky contact is formed by the depletion of hole plasma near SEM and p^+ prompted source interface. This results in the immediate current inhibition at source to channel interface caused by an undesired movement of electrons en route to the Schottky interface. The Schottky tunneling phenomenon is considered by implementing the universal Schottky tunneling (UST) model to study the underestimated drain current of HJLTFET. However, the UST model becomes inconsequential for SEM work function higher than p^+ prompted source (Pd) as hole plasma is preserved by the ohmic contact formation.

Keywords: arsenide, hole plasma, junctionless TFET, source electrode metal, universal Schottky tunneling

(Some figures may appear in colour only in the online journal)

1. Introduction

The fast-growing need of next generation devices in artificial intelligence, cloud computing, low power and high-speed modern communication systems, and internet of things has led the research community to explore new innovative ideas at the sub 20 nm technology node like never before. The high operation speed, improved functionality and enhanced packing density are the results of continuous downscaling of complementary metal oxide semiconductor (CMOS) technology. However, it results in various critical challenges like high leakage current, high static power dissipation and short channel effects [1–7]. Other modern electronic devices like metal-oxide semiconductor field-effect transistor (MOSFET), high electron mobility transistor (HEMT), heterojunction bipolar transistor (HBT) and negative capacitance field effect transistors (FETs) show degraded performance at sub 20 nm technology node despite being widely used in modern communication systems. The alternative to such issues can be the

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device having steeper swing and lower leakage current. Tunnel field effect transistor (TFET) is amongst the most promising devices to fill these gaps along with improved performance pertaining to steeper swing and lower leakage current. It overcomes the prime issue of thermionic limit of 60 mV decade^{-1} (MOSFET) owing to the band-to-band tunneling (BTBT) of carriers rather than thermionic emission in MOSFET [4–8]. However, inferior ON current (I_{ON}) is still a snag for the TFET devices. Moreover, the development of extremely thin doping junctions using highly doped source and drain region is one of the major obstacles owing to the increased thermal expenses for hybrid thermal annealing and ion implantation [8, 9]. Along with that, random dopant fluctuations are also generated due to the highly doped source and drain regions [10]. Therefore, to eradicate the junction constraint and simplify the fabrication complexity, junctionless FETs were introduced based on charge plasma concept. The fundamental basis of charge plasma is to utilize gates having different work functions to induce the source and channel region polarity [8]. Thus, junctionless TFETs have given a new outlook to the electronic industry by merging the advantages of TFET (steeper swing) and junctionless field effect transistor (JLFET) (high I_{ON}) [11–17].

Many researchers have paid attention to analyze the performance characteristics of junctionless tunnel field effect transistor (JLTFET) by exploring the impact of control gate (CG) and polar gate (PG) work functions. However, the depletion of hole plasma by the work function of source electrode metal (SEM) at the interface of SEM and p^+ prompted source region (SEM/S) has not been given due importance [11–16, 18–20]. The depletion of hole plasma gives rise to a Schottky interface at the SEM/S interface, which is implemented through the universal Schottky tunneling (UST) mechanism at the SEM/S interface. The ignorance of UST at the SEM/S interface leads to underrated performance of the device. In this work, we have given due attention to the UST at the SEM/S interface by selecting appropriate SEM work function. To take into account the Schottky tunneling at the SEM/S interface, an in-depth attention has been laid upon incorporating the UST model in our present work, which has been overlooked by many researchers before [8, 9, 11, 16]. Figure 1 represents the grid sites near the Schottky contact, which signifies the localized tunneling generation rates of electrons. In UST mechanism, the tunneling current is calculated across these grid sites within a specified distance of the electrode. Equation (1) describe the calculation of tunneling current component as follows [18, 19, 21]:

$$J_{\mathrm{T}} = \frac{A^* T_{\mathrm{L}}}{K} \int_{E}^{\infty} (E) \ln \left[\frac{1 + f_{\mathrm{s}}(E)}{1 + f_{\mathrm{m}}(E)} \right] \mathrm{d}E \tag{1}$$

$$G_T = \frac{1}{q} \nabla J_T \tag{2}$$

where J_{T} is the tunneling current density, A^* is the effective Richardson's coefficient, T_{L} is the lattice temperature, $I(E')$ is the tunneling probability, $f_{\mathrm{s}}(E')$ and $f_{\mathrm{m}}(E')$ are the Maxwell-Boltzmann distribution functions in the semiconductor and metal and E' is the carrier energy. G_{T} is the localized tunneling rate.

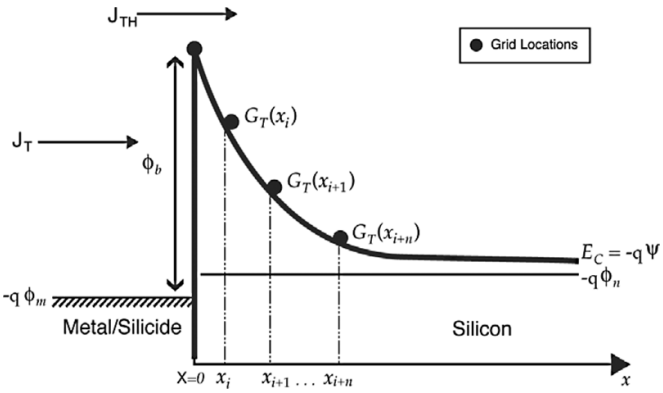

Figure 1. The universal Schottky tunneling mechanism representing the local tunneling generation rate at the metal/semiconductor interface. Reproduced with permission from [21] ATLAS User's Guide, SILVACO Int., Santa Clara, CA, USA, Version 5.26.1.R, 2018.

The total current density across the Schottky barrier is the sum of thermionic emission component and tunneling component as shown in figure 1. Equation (3) represents the mathematical expression for total current density across the Schottky barrier:

$$J_{\mathrm{TOT}} = J_{\mathrm{T}} + J_{\mathrm{TH}} \tag{3}$$

where J_{TOT} is the total current density and J_{TH} is the thermionic emission component. For lower Schottky barrier height, the thermionic emission of the carriers over the barrier increases leading to enhancement in the thermionic emission component of current. In that case the tunneling current density is reduced. However, the tunneling current comes into play only if the tunneling width is lower than 10 nm [18].

We utilized the binary/ternary compound semiconducting hetero-material based hetero-junctionless TFET (HJLTFET) using InAs/AlGaSb with Al mole fraction of 0.15 (our previously published work [17]). In present work, for the first time, metals with different work functions as the source electrode have been implemented to study the significance of source electrode (SE) metals on the analog characteristics of HJLTFET. The presented work may be helpful to study various underrated physical effects of JLTFETs in regards to ohmic and Schottky contacts. It may put the research of junctionless devices in the right direction owing to the hole plasma depletion consideration at the SEM/S interface, which has been overlooked before. Our article is framed into five parts. First part presents the details of literature review and the introduction of the presented work. Second part describes the details of device structure, parametric details and device material information. Third part explains the simulation models, methodology, calibration and the fabrication process flow of our device. The results and detailed discussion are presented in part four. The summary of the presented work is concluded in part five of the paper.

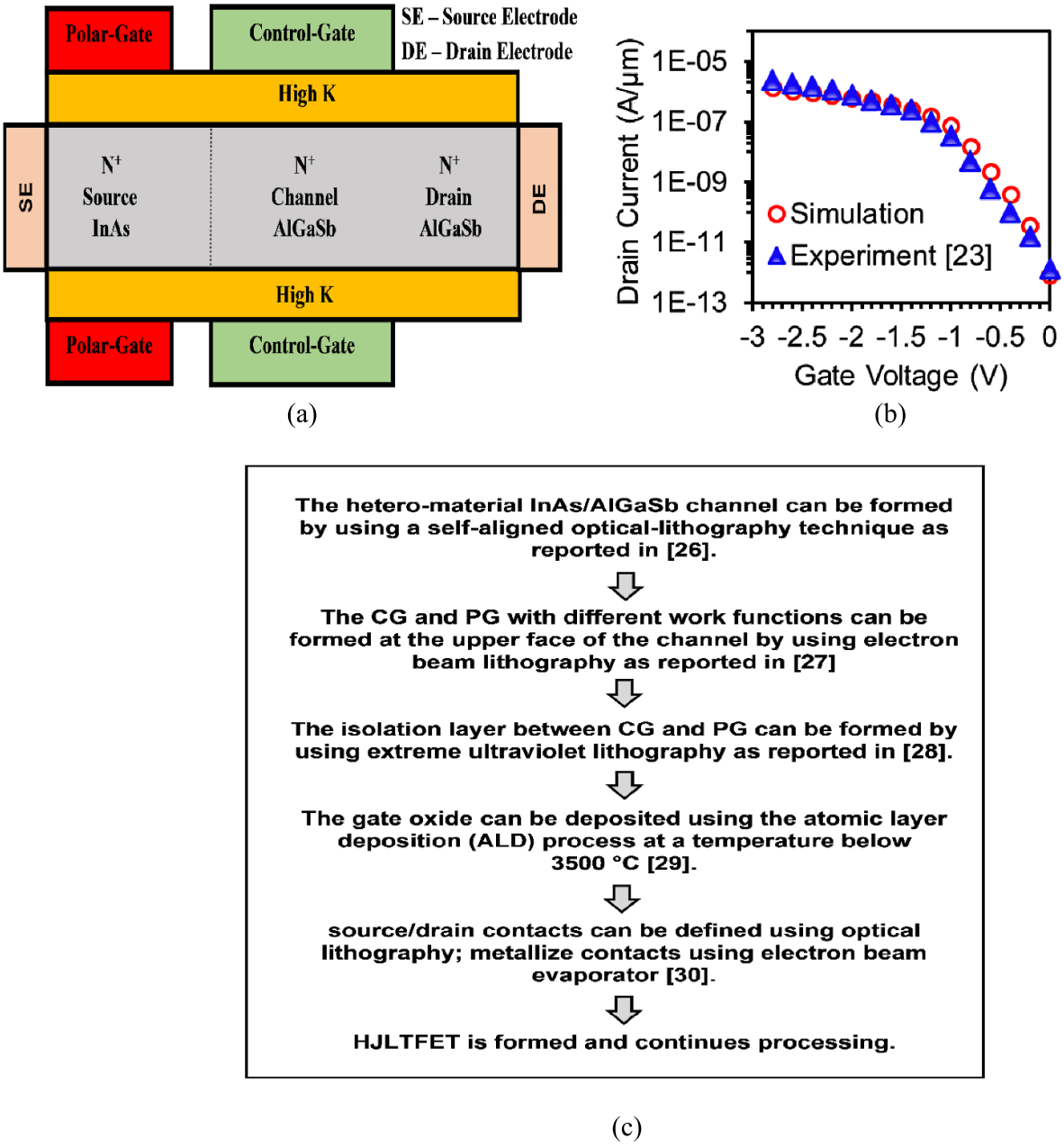

Figure 2. (a) Device schematic architecture of HJLTFET, (b) calibration plot, and (c) fabrication process flow of proposed HJLTFET.

2. Device structure

The schematic device architecture of our proposed device HJLTFET is presented in figure 2(a). The optimization of Al mole fraction in AlGaSb used in channel region is already presented in [17]. The doping concentration of the source and channel region is kept uniform at 1×10^{19} cm^{-3}. The thickness of the semiconductor body is 3 nm. The other device design parameters are framed in table 1. A polarity gate PG with work function 5.93 eV is implemented over the source region to prompt the (hole plasma) p^+ source. The CG with work function of 4.5 eV is implemented over the channel region to prompt the electron plasma. The 2 nm thick high k dielectric material (HfO_2) is applied to insulate the gate electrodes from the source and channel semiconductor material. To study the impact of metal work function in the source electrode, we employed three metals viz. tungsten (W, 4.55 eV), molybdenum (Mo, 4.75 eV), and palladium (Pd, 5.3 eV) [20]. The ON state and OFF state corresponds to $V_{GS} = 1.5$ V, $V_{DS} = 1.5$ V and $V_{GS} = 0.0$ V, $V_{DS} = 1.5$ V, respectively.

3. Simulation methodology

The simulation modeling and physics based numerical calculations are performed using Silvaco-ATLAS TCAD tool [21]. To implement the device physics, various physical models

Table 1. Device parameters.

Parameter	Symbol	Value
Channel length	L_G	20 nm
Doping concentration	N_D	1×10^{19} cm^{-3}
Oxide thickness	T_{OX}	2 nm
Isolation thickness	L_{Gap}	2 nm
CG work function	ϕ_{CG}	4.5 eV
PG work function	ϕ_{PG}	5.93 eV
Spacer length	L_{Spr}	2 nm

have been applied like Fermi Dirac statistics, band gap narrowing model, CVT model (Lombardi) to understand the significance of concentration, electric field, and temperature associated mobility, and Hansch quantum confinement model [22]. To emulate the physics related to the electron density, hole density, and trapped electron density in the conduction band, valence band, and forbidden gap, respectively, we have incorporated Shockley–Read–Hall (SRH) (trap assisted recombination) and Auger recombination models in our device to include minority recombination effects with carrier lifetime (TAUP0 $= 1 \times 10^{-7}$ s^{-1}). The trap assisted tunneling dominates the SRH recombination process and reduces the carrier lifetimes near the strong electric field regions, which affects the leakage current of the device. Therefore, we have applied the TAT model in our device.

To inculcate the source/channel (S/C) arsenide/antimonide interface tunneling and to define the electric field along the whole tunneling area, non-local BTBT model is used by generating a quantum tunneling meshing around the S/C interface. The calibration of the simulation models and parameters being used in our device has been validated with the information extracted from a fabrication-based research work [23] by maintaining the device biasing settings precisely the same as that of the published results stated in [23]. Figure 2(b) illustrates the calibration of the transfer characteristics obtained from the extracted data of the experimental work and our simulations. It validates all the model parameters due to the close propinquity of the compared results. To account for the gate leakage impact on subthreshold swing (SS) in HJLTFET, we have implemented the Fowler-Nordheim (FN) model in our simulations. The FN model calculates the tunneling current due to the tunneling of electrons from the semiconductor Fermi level into the oxide conduction band. This is caused by the high electric field across the oxide. Each electrode-oxide and oxide-semiconductor interface is divided into discrete segments and for each oxide-semiconductor segment, the FN current is calculated. Which is further added to the electrode-oxide boundary. Table 2 represents the model parameters for HJLTFET simulations. To consider the quantum mechanical effects of thin body semiconductor, we have invoked the drift-diffusion mode-space method. This model solves the 1D transport equations in each sub-band and quasi-Fermi levels are extracted.

The currents and bulk carrier densities are calculated by summating over all sub-bands. It captures quantum effects in transverse direction along with other models for BTBT, mobility and recombination. To inculcate the impact of interface trap

Table 2. FN model parameters [21].

Parameter	Value
A_{FN}	1.82×10^{-7}
B_{FN}	1.90×10^{8}
A_{FH}	1.82×10^{-7}
B_{FH}	1.90×10^{8}

charges and band tailing in our device, the interface charges are uniformly distributed with trap charge density fixed at $N_f = 1 \times 10^{12}$ cm^{-2} for semiconductor/semiconductor and semiconductor/oxide interfaces (S/S and S/O interface) based on earlier reported simulation and experimental data involving the hot carrier/radiation/process damages [24, 25]. The polarity and position of interface charge is specified using the INTERFACE statement [21]. The prime focus of the work is to include the impact of SE metal work function on the device performance. For that purpose, we evoked the UST model in case of designing the HJLTFET having SE metal work function lower than the p$^+$ (hole plasma) prompted source region. Moreover, the results obtained are also compared with HJLTFET after the exclusion of UST model, to study the variation of result characteristics with the inclusion and exclusion of UST model. The SE metal work function lower than p$^+$ prompted source region gives rise to the Schottky tunneling at the SEM/S interface, which is taken into account by the implementation of UST model. Such aspect of HJLTFET devices have not been considered in former studies to the best of our knowledge. Figure 2(c) illustrates the fabrication process flow chart of the proposed HJLTFET.

4. Results and discussion

In this section, a thorough investigation of the impact of three SE metal work functions on the analog characteristics of InAs/AlGaSb based HJLTFET has been carried out.

Figure 3 illustrates the variation of surface potential along the channel direction for no biasing condition (thermal equilibrium state, $V_{GS} = 0.0$ V, $V_{DS} = 0.0$ V) for three SE metal work functions. For SEMs, W and Mo having work function lesser than p$^+$ prompted source, the hole plasma induced by the PG nearby the SEM/S interface gets depleted by the surface potential. However, for the larger work function metal Pd, the hole plasma at the SEM/S interface is retained by the PG (figure 3). Such variation of surface potential with respect to the different SE metal work function shows synchronization with the already existing theories [26]. Figures 4(a)–(c) display the disparity of energy band profile along the channel direction at thermal equilibrium for three SE metal work functions. We have calculated the energy band profile of HJLTFET by considering the cutline across the whole channel length (along the x-direction) 1 nm below the channel surface. In figure 4(a), the depletion of hole plasma near the SEM/S interface for W and Mo gives rise to Schottky contact due to the SEM work function lesser than p$^+$ prompted source. Whereas the higher work function SE metal, Pd gives rise to ohmic contact owing to the

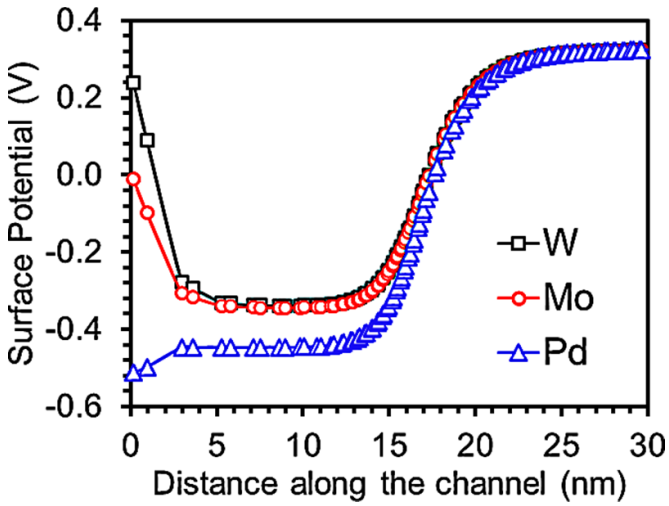

Figure 3. Surface potential variation along the channel direction for three SE metals at thermal equilibrium state.

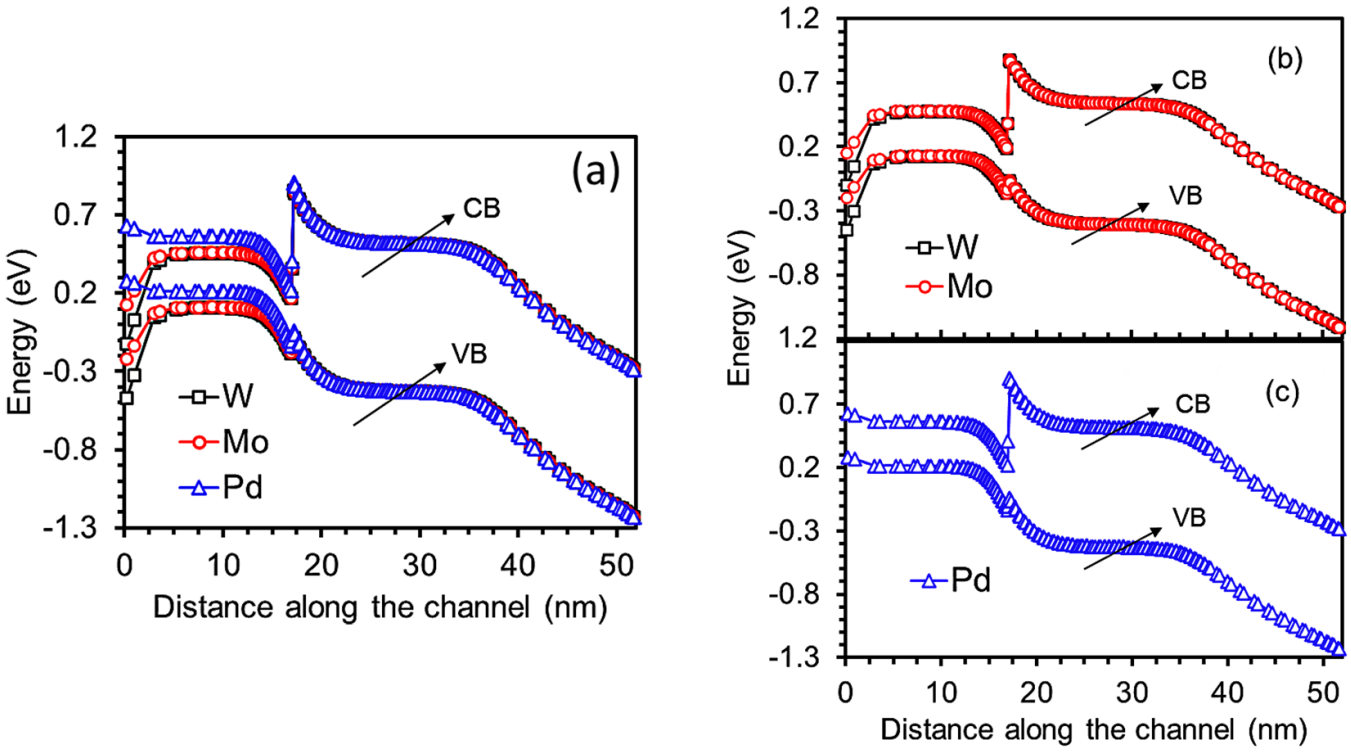

Figure 4. (a) Energy band profile of HJLTFET for three SE metals at thermal equilibrium state, (b) formation of Schottky interface at W and Mo SE/source interface, and (c) formation of ohmic contact for Pd SE.

preservation of hole plasma. In figure 4(b), for W and Mo SEs, the source region is no longer p^+ type at the SEM/S interface.

The depletion of hole plasma leads to reduction of effective carrier conduction as the electrons attain higher probability to move towards the SE. Thus, the electrons available for tunneling across the S/C interface reduces (figure 4(b)). However, the hole plasma is preserved for SEM work function higher than p^+ prompted source (for Pd), maintaining the electron movement only towards the S/C interface. Thus, the effective carrier conduction remains unaltered for Pd SE metal (figure 4(c)). It confirms that along with PG, the choice of SEM work function is equally responsible for the induction of hole plasma in the source region of HJLTFET. A detailed theory regarding the transformation of metal contact from ohmic to Schottky by choosing appropriate work functions has been developed in [20]. However, the transformation of metal contacts from ohmic to Schottky for HJLTFETs leads to new aspects for the research community and mobile industry.

Figure 5 illustrates the electron/hole concentration of carriers along the channel length for three SE metals. As stated

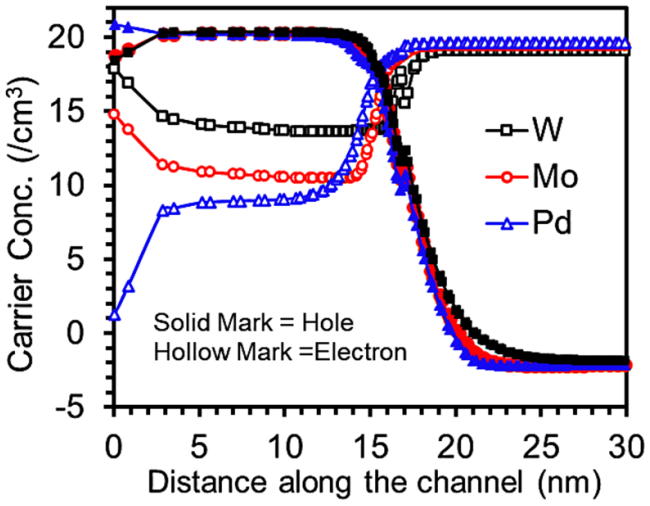

Figure 5. ON state electron and hole concentration along the channel direction for three SE metals.

before, in figures 4(a) and (b) regarding the electrons moving towards the SE region for W and Mo SE metals, a similar phenomenon has been observed regarding the carrier concentration in figure 5. The electron concentration increases greatly as compared to the hole concentration near the SE region for W and Mo metals confirming the movability of electrons in the direction of SE. This declines the tunneling of electrons across the S/C interface and hence the BTBT rate of HJLTFET is diminished for W and Mo SE metals (figure 6(a)). Therefore, the overall conduction of HJLTFET is also hampered owing to the lowered BTBT rate. Since number of electrons available for tunneling across the S/C interface has declined, the drain current of HJLTFET also reduces for W and Mo SEs. For Pd SE, the absence of Schottky interface at the SEM/S interface leads to the highest electron BTBT rate. There is only one way movability of electrons from source to channel region through S/C interface leading to numerous electrons available for effective conduction of HJLTFET (figure 6(a)). As mentioned before, the W and Mo SEs exhibit the Schottky tunneling at the SEM/S interface. Therefore, the UST model need to be implemented to emulate the accurate device physics regarding the tunneling phenomenon at the SEM/S interface.

Figure 6(b) displays the Schottky tunneling rate of electrons at the SEM/S interface for all three metal SEs—W, Mo, and Pd. The comparison of contour plot of Schottky tunneling is also illustrated in figure 7. The Schottky tunneling for W is lower than Mo. The reason behind lower Schottky tunneling of W is the larger Schottky potential barrier, whereas Mo SE attains lower Schottky potential barrier height (figure 3) and width leading to enhanced Schottky tunneling rate (figure 6(b)). The Schottky tunneling rate for Pd SE is almost negligible owing to higher SE work function than p^+ prompted source. This is because of the non-existence of Schottky interface at the SEM/S interface of Pd SE. Therefore, the UST model has no influence on the performance of Pd SE. The contour plots of the three aforementioned SE metals show similar variation in figure 7. Here, the Mo SE (figure 7(b)) leads to significantly higher Schottky tunneling rate than W SE (figure 7(a)) at the SEM/S interface, whereas the Schottky tunneling rate of Pd SE is diminished (figure 7(c)).

Figures 8(a) and (b) illustrate the vector representation of the electric field direction of HJLTFET for three SE metal work functions under the ON state. We have displayed the electric field vector representation in the hole plasma depleted region near the SEM/S interface. Since the direction of electric field is opposite to the direction of flow of electrons, therefore the movability of electrons from source to channel is defined by the electric field vector. It helps to outline the impact of SEM work function on the formation of Schottky tunneling interface at the SEM/S interface of HJLTFET. For W and Mo SEs, the movability of electrons is more in the direction of SE forming the Schottky interface (figures 8(a) and (b). This is due to the hole plasma depletion at the SEM/S interface and hence the current conduction is abstained in the channel region (figures 8(a) and (b)), whereas, the electric filed vector shows only one way movability of electrons from source to channel vanishing the Schottky contact formation at the SEM/S interface of Pd SE. Hence, the current conduction remains immune for Pd SE, due to ohmic contact formation at SEM/S interface (figure 8(c)).

To illustrate the impact of inclusion and exclusion of UST model in the SE-HJLTFET device physics, we have plotted the transfer characteristics of HJLTFET for three aforementioned SE metal work functions (W, Mo, and Pd) in figure 9(a). For the both inclusion and exclusion of UST model, the results show major variation for SEM work functions lesser than the p^+ prompted source region (W and Mo). On the implementation of UST model, the Schottky tunneling is taken into account due to the depleted hole plasma at the SEM/S interface. This Schottky tunneling gives precise calculations of the drain current, which is overlooked without the implementation of UST model. There is no variation of transfer characteristics in Pd SE with or without the UST model. The reason behind this is the formation of ohmic contact by Pd SE with the p^+ prompted source and hence the hole plasma is preserved by the PG. Therefore, role of UST becomes meaningless for Pd SE so the drain current remains unchanged with or without UST model application. Also, the maximum drain current is obtained for Pd SE, which justifies the above discussion of ohmic contact formation at the Pd SEM/S interface. The result is supported by the highest BTBT rate of electrons at the S/C interface in Pd SE shown in figure 6(a). It is inferred that along with BTBT (S/C interface) the Schottky tunneling (SEM/S interface) is equally significant in defining the conduction of HJLTFET. The drain current for W (Mo) is almost 2.44% (1.56%) enhanced on the inclusion of UST model. The significance of SEM work function comes into play only for the ON state. When no gate bias is applied, the wider hetero-material tunneling barrier restricts the flow of electrons across the S/C interface, such that the effect of

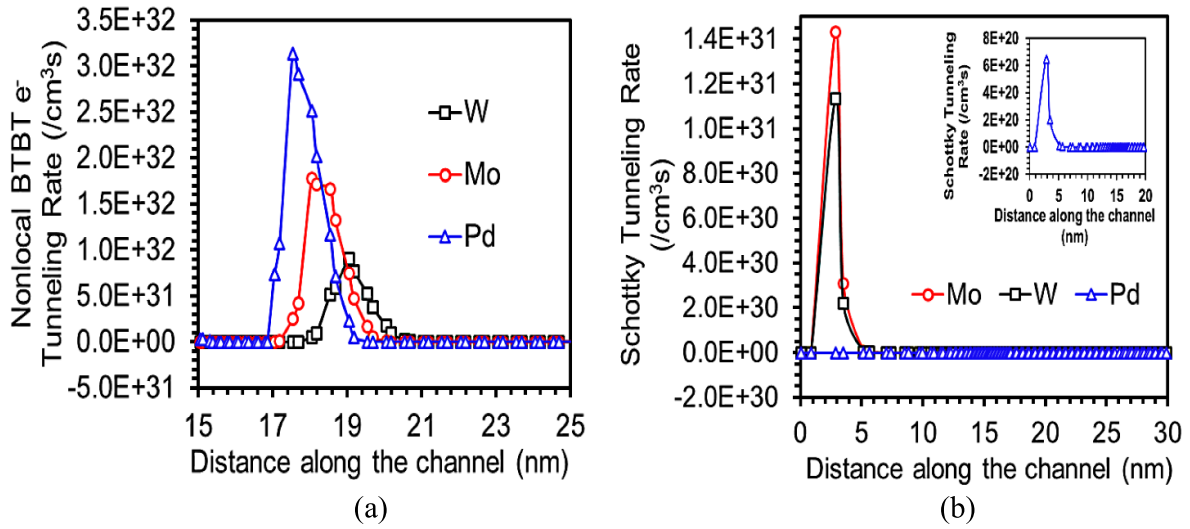

Figure 6. (a) Band to band tunneling rate at S/C interface and (b) Schottky tunneling rate at SEM/S interface for different SE metals.

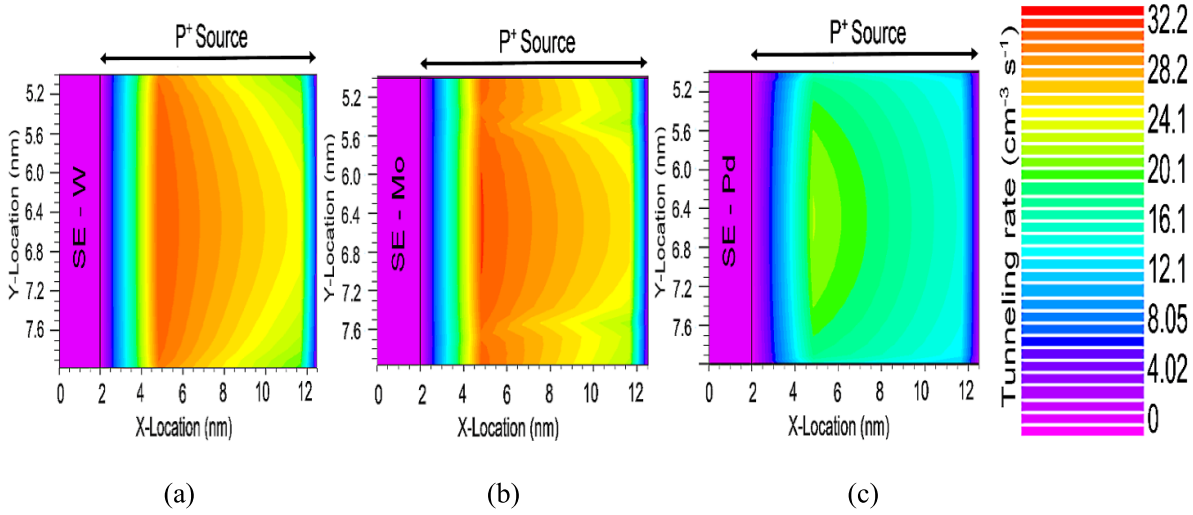

Figure 7. ON state level curve (contour) of Schottky tunneling rate (log scale) of HJLTFET for (a) W, (b) Mo, and (c) Pd.

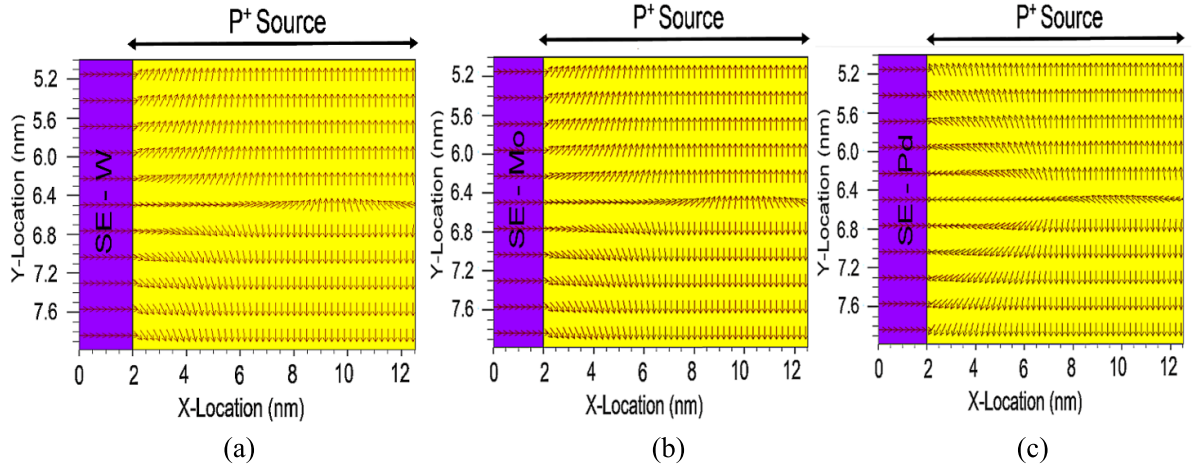

Figure 8. ON state electric field vector illustration of HJLTFET for (a) W, (b) Mo, and (c) Pd.

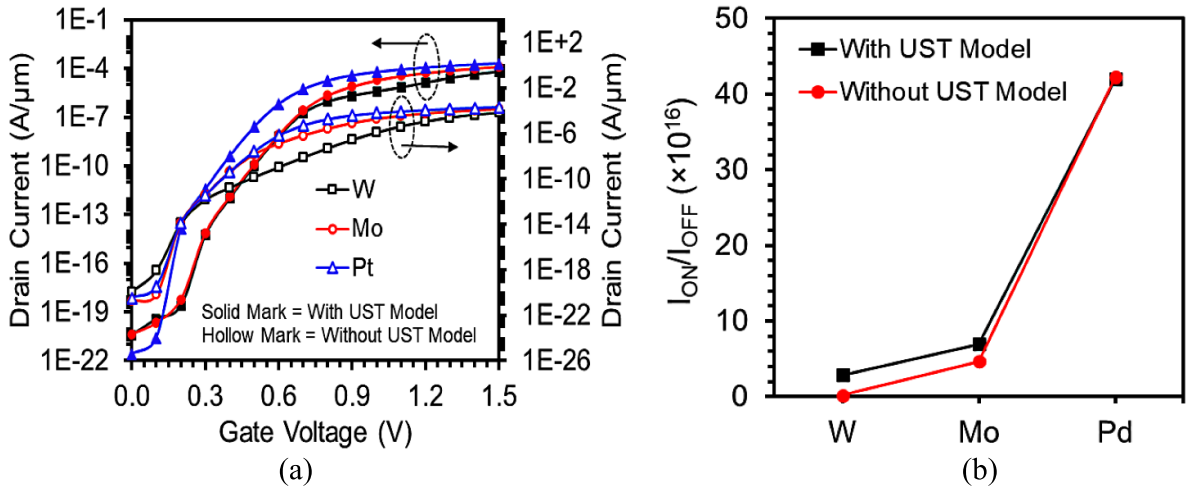

Figure 9. (a) Transfer characteristics and (b) current switching ratio (I_{ON}/I_{OFF}) of HJLTFET for three SE metals.

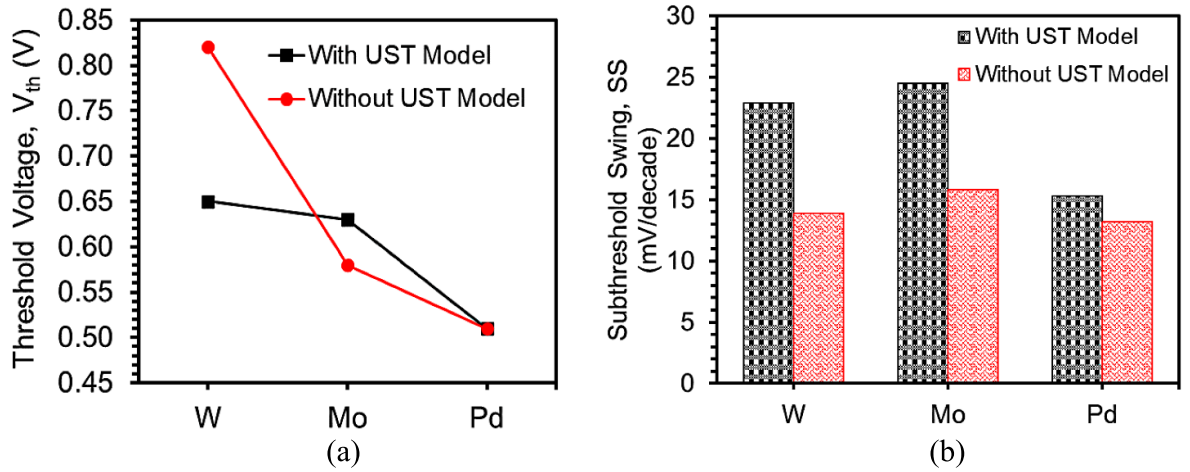

Figure 10. Impact of SE metal work function on (a) threshold voltage and (b) SS of HJLTFET.

SE metal diminishes. For the whole simulation process and result parameters extraction, we have kept the work function of CG at a fixed value. So, it is primarily the impact of SE metal work function on the results variation, which describes the role of UST model in formation of Schottky and ohmic contacts.

Further, the impact of UST model has been studied for current switching ratio (I_{ON}/I_{OFF}) of HJLTFET for three SE metals W, Mo, and Pd (figure 9(b)). For SEM work function lesser than p^+ prompted source (W and Mo) there is a noticeable variation of I_{ON}/I_{OFF} with or without UST model. However, for Pd SE having higher work function than p^+ prompted source, there is a negligible variation of I_{ON}/I_{OFF} for both cases. This signifies the importance of the role of SE metal work function being played in the conduction of HJLTFET. The I_{ON}/I_{OFF} ratio of HJLTFET for W (Mo) SE becomes 16 (1.5) times higher on the inclusion of UST model as compared to without UST model case. Figure 10(a) displays the significance of UST model on the variation of threshold voltage (V_{th}) of HJLTFET for three SE metal work functions. The V_{th} of HJLTFET reduces by 0.79/1.08 times for W/Mo SE with UST model implementation than without the UST model case. This shows the undervalued drain current of HJLTFET (W and Mo) without UST model implementation, whereas, Pd SE preserve the hole plasma in the source region and hence the ohmic contact formed at Pd SEM/S interface shows improved V_{th} in comparison to other two metal SEs. Thus, the comparison of with and without UST model for Pd SE shows no variation of V_{th}. Figure 10(b) shows the comparison of SS for all three SE metal work functions with and without UST model implementation. The variation of SS for Pd SE is marginally increased, whereas the variation is larger in case of other two metal SEs. Figure 11 illustrates the significance of inclusion and exclusion of FN model on the SS value for three SE metals (W, Mo, and Pd). The variation of SS shows no significant change on the application of FN model. So, there is a negligible effect of gate leakage in HJLTFET.

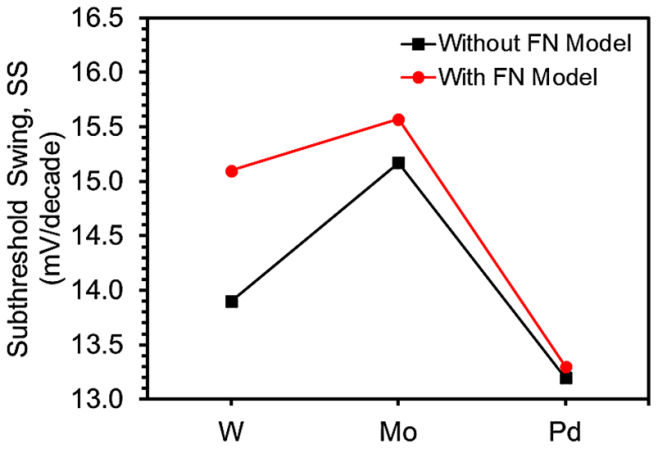

Figure 11. Impact of inclusion and exclusion of FN model on SS of HJLTFET.

5. Conclusion

This research gives the detailed analysis of the influence of different SE metal work functions in the formation of Schottky and ohmic contacts by including the most important UST model in our proposed hetero-material InAs/AlGaSb based HJLTFET. The role of different SE metal work functions was evaluated with respect to the polarity gate prompted source region of HJLTFET (p^+ source) for analog performance parameters. It is found that the total current conduction of HJLTFET gets hampered with SEM work function lesser than p^+ prompted source as the hole plasma gets depleted near the SEM/S interface. This results in the formation of Schottky contact leading to the undesired electrons' movement towards the SE. The electrons available for BTBT through S/C interface gets reduced in number, hence hampering the effective conduction of HJLTFET (drain current). Thus, in spite of efficient BTBT of electrons at S/C interface, the formation of Schottky contact abstain the current conduction of HJLTFET (for W and Mo SE work functions). This signifies the requirement of ohmic contact formation at the SEM/S interface in addition to the sufficient band to band tunneling across the S/C interface. Therefore, the SE work function must be higher than the p^+ prompted source forming the ohmic contact at the SEM/S interface to facilitate the effective current conduction in the n-type HJLTFET. Moreover, the UST model must be implemented during the simulations to include the device physics of the Schottky tunneling at the SEM/S interface, which is overlooked otherwise. However, for the fabrication of HJLTFET, the SE with higher work function than the p^+ prompted source must be preferred to ensure effective device functioning.

Data availability statement

No new data were created or analyzed in this study.

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TECHNICAL PAPER

RF, linearity and intermodulation distortion analysis with small-signal parameters extraction of tunable bandgap arsenide/antimonide tunneling interfaced JLTFET

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Abstract
This paper presents a charge plasma junctionless tunnel field effect transistor (JLTFET) based on a novel blend of an arsenide/antimonide tunable bandgap source to channel (S/C) tunneling interface by incorporating binary/ternary compound semiconducting materials (InAs/AlGaSb) in the source and channel regions to investigate the radio frequency (RF), linearity and intermodulation distortion performance. The proposed hetero-material JLTFET (H-JLTFET) is compared with a conventional homo-material (silicon) based JLTFET to explore the possible scope of HJLTFET for RFIC and wireless applications. The simulation study reveals that the HJLTFET achieves an improved performance in consideration of RF, Linearity and intermodulation distortion FOMs as parasitic capacitance (C_{gg}, 60.7% ↓), maximum oscillation frequency (f_{max}, 2292% ↑), gain bandwidth product (225 times ↑), Intrinsic gain (A_v, 708% ↑), peak transconductance (g_m, 79 times ↑), and various signal performance metrics such as VIP2 (97.9% ↑), VIP3 (326% ↑), IIP3 (237.9% ↑), and 1-dB compression point (11.6% ↑) in comparison to JLTFET. Moreover, HJLTFET shows better reliability in terms of power gains and small signal admittance (Y) parameters variation with high frequency as compared to JLTFET. Therefore, HJLTFET appears to be an efficient alternative for high frequency and low power operations required in future RFIC designs and wireless communication systems.

1 Introduction

The aggressive device size downscaling in conventional metal–oxide–semiconductor-field-effect transistors (MOSFETs) has resulted in various issues of short channel effects, random dopant fluctuations, drain induced barrier lowering, increased leakage current (I_{OFF}), and high-power dissipation (Hamedi-Hagh and Bindal 2008; Bangsaruntip et al. 2010; Jin et al. 2006; Dixit et al. 2005; Kranti and Armstrong 2007). Also, the thermionic emission mechanism in MOSFET leads to a theoretical limitation of subthreshold swing (SS) to 60 mV/dec at room temperature. Hence, devices having another mode of carrier transport are needed to achieve a smaller SS. The tunnel FETs (TFETs) are the devices being preferred over MOSFETs due to the band-to-band tunnelling mechanism of carriers, which results in steeper SS, low I_{OFF}, and lower standby power (Kumar and Janardhanan 2013; Boucart and Ionescu 2007; Pal and Dutta 2016; Seabaugh and Zhang 2010). However, TFETs suffer from the issue of lower ON current (I_{ON}). To enhance the I_{ON} of TFETs, the conventional large energy band gap silicon material has been replaced with III–V compound semiconducting materials to induce hetero-material source/channel (S/C) interface with lower energy bandgap source and larger energy bandgap channel regions. This leads to narrowing of the tunneling barrier width and hence the tunneling probability of the carriers improves (Sharma and Chaujar 2021a, 2022; Aghandeh and Ziabari 2017; Patel et al. 2019).

The junctionless tunnel field effect transistors (JLTFETs) have gained huge attention of researchers due to the unification of JLFET (higher I_{ON}) and TFET (steeper SS) architectural benefits (Colinge et al. 2010; Lee et al. 2009). It utilizes the concept of charge plasma by inducing the conventional p^+-i-n^+ substrate from the n-doped substrate with the application of two gates with diverse work

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functions at the source and channel regions, respectively (Sharma and Chaujar 2021a, 2022; Aghandeh and Ziabari 2017). TFETs being the steeper SS devices, can be chosen as the building blocks in the wireless communication systems (Gupta et al. 2019). Highly competent and economical RF systems are required to manage the poor signals and meet the standards of modern communication systems. To accomplish an effective communication system, the higher order harmonics and intermodulation distortion should be as low as possible (Vanlalawmpuia and Bhowmick 2019; Gupta and Chaujar 2016). To substantiate negligible intermodulation distortion and higher order harmonics, the linearity aspect of the devices becomes essential to study (Madan et al. 2017). To improve the linearity behaviour of the devices, the researchers have implemented various techniques. However, there are still many nonlinearity factors, which lead to noise in the RF wireless systems (Kumar et al. 2018; Paliwoda and Misra 2011; Saha et al. 2020). Maintaining high linearity at the system level becomes extremely difficult due to the power consumption by the complex circuits. Therefore, to enhance the device reliability in low power applications, the transistor level linearity is preferred.

In the present manuscript, we have incorporated the junctionless TFET architecture along with III–V compound semiconducting hetero-material (InAs/AlGaSb) as an alternative for the conventional homo-material (silicon). The purpose of this is to induce a hetero-material tunable bandgap S/C tunnelling interface, which leads to energy bandgap modification at the barrier and facilitates higher carrier mobility. On applying the gate bias, the tunnelling barrier width gets narrow down and hereafter numerous majority carriers pass through the barrier leading to higher I_{ON}. The InAs and AlGaSb is utilized as the source and channel material. The InAs and AlGaSb based devices are most appropriate for fabricating smaller conductive structures in comparison to other materials. It has the applications in various semiconductor micro- and nano-electromechanical systems (MEMS/NEMS) such as high frequency signal processing apparatuses, high resolution actuators, sensors, and medical diagnostic devices (Yamaguchi et al. 2002; Yadav et al. 2017; Nirmal et al. 2015; Alvi 2017). The projected device named as hetero-material junctionless TFET (HJLTFET) is investigated for RF and linearity FOMs as intrinsic gain, parasitic capacitance, transconductance, maximum oscillation frequency, transconductance frequency product, gain bandwidth product, intrinsic delay, higher order harmonics, VIP2, VIP3, IIP3, IMD3, and 1-dB compression point. Moreover, the power gains and small signal admittance parameters are also studied. The result characteristics of HJLTFET are compared with conventional silicon based JLTFET.

2 Device designing

Figure 1a illustrates the schematic device architecture of HJLTFET. Initially, we designed a conventional Si (homo-material) based junctionless TFET (JLTFET) and then incorporated the novel amalgamation of binary (InAs) and ternary ($Al_xGa_{1-x}Sb$) compound semiconducting materials at the S/C interface. The mole fraction of Al (x. comp) in $Al_xGa_{1-x}Sb$ is fixed at 0.15 in HJLTFET. The optimization of Al mole fraction for HJLTFET is explained in our previous work (Sharma and Chaujar 2021b).

The channel length and body thickness in both devices is 20 nm and 3 nm, respectively. We have implemented SiO_2 as the dielectric material in both the aforementioned devices. The oxide thickness between two gates is 2 nm. We employed two isolated gates as the (polar gate) PG and (control gate) CG in HJLTFET and JLTFET, which have different work functions in order to achieve the required carrier concentration in the source and channel region, respectively. The CG and PG have work function of 4.5 eV and 5.93 eV, respectively. Also, the spacer thickness is retained at 2 nm between the PG and CG to isolate the two gates. The doping concentration of both devices is kept same (1×10^{19} cm^{-3}). The doping concentration is chosen to be uniform so that the required polarity of source, channel, and drain regions can be attained through the charge plasma concept (Sharma and Chaujar 2021a, 2022; Aghandeh and Ziabari 2017). All the device parameters are kept same as that of Sharma and Chaujar (2021b). The ON state corresponds to V_{GS} = 1.5 V, V_{DS} = 1.5 V and OFF state corresponds to V_{GS} = 0.0 V, V_{DS} = 1.5 V.

3 Simulation methodology and calibration

We have performed the entire device simulations through a 2-D device simulator, Silvaco-ATLAS (ATLAS User's Guide, SILVACO Int. 2018). The models applied throughout the simulations are the non-local BTBT model (to account for the tunneling of electrons at the S/C interface), Band gap narrowing model (BGN), Auger recombination model (for considering the highly doped channel region), SRH recombination model (to elucidate generation and recombination effects), Fermi Dirac statistics, and the CVT model (Lombardi) (to calculate the mobility dependent on concentration, electric field, and temperature). Moreover, the quantum confinement (QC) effects are acknowledged by making use of the model given by Hänsch et al. (1989). To substantiate the models employed in our device, we calibrated the simulation models by extracting the data of published results while maintaining the parameters and dimensions of the device exactly the

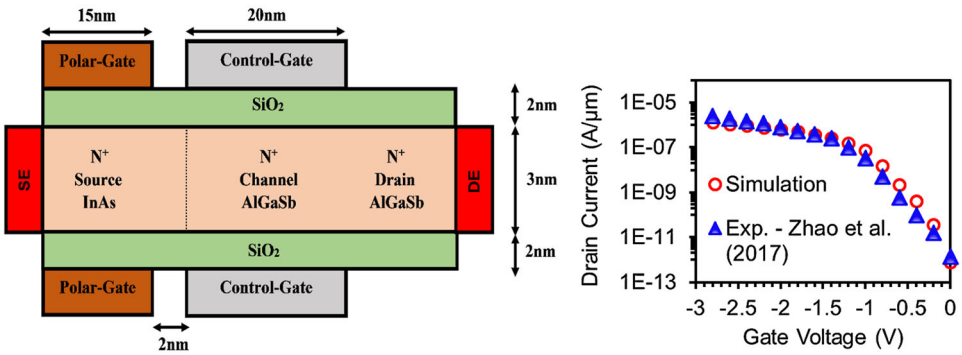

Fig. 1 Graphic structure of **a** HJLTFET and **b** Calibration plot

same as that of Zhao et al. (2017). Figure 1b shows the calibration of transfer characteristics by showing the close agreement between the experimental work and our simulation.

4 Results and discussion

4.1 Analog/radio frequency analysis

Figure 2a presents the transfer characteristics variation of HJLTFET and JLTFET. When no gate bias is applied, the incorporation of bandgap engineering by using hetero material InAs/AlGaSb in the source/channel regions leads to wider tunnelling barrier thickness at the S/C interface.

Therefore, only a few minority carriers can tunnel through the barrier leading to very low I_{OFF}. However, on applying the gate voltage, the overlapping of the bands at the S/C interface happens by narrowing of the tunnel barrier width. Now, larger number of carriers attain sufficient energy to tunnel through the S/C interface and hence the I_{ON} rises (Fig. 2a). As a result, the current switching ratio of HJLTFET reaches to 10^8 orders higher as compared to JLTFET. The transconductance (g_m) is one of the most important parameters in modern RF/wireless applications. It is responsible for the smooth amplification and better efficiency of the system. It is defined in Eq. 1 (Verma and Gupta 2021),

$$g_m = \partial I_{DS}/\partial V_{GS}. \quad (1)$$

For higher current conversion rate of the device, g_m should be higher. Figure 2b shows the comparison plot of peak g_m of HJLTFET and JLTFET, where the peak g_m of HJLTFET is $\sim$ 79 times higher than the JLTFET device. The higher value of g_m of HJLTFET attributes to the rise in I_{ON} of the device due to the hetero-material S/C tunneling interface. Whereas, the Si material having larger band gap leads to poor carriers tunneling across the S/C interface and hence poor I_{ON} results in poor g_m (Fig. 2b). Figure 2c displays the contrast of intrinsic gain, A_v of the two devices, where A_v of HJLTFET increases with rise in gate voltage and attains 8.2 orders higher value in comparison to JLTFET. Such a rise in A_v is the result of rise in g_m of HJLTFET, due to the direct dependence of A_v on g_m (Eq. 2) (Verma and Gupta 2021).

$$A_v = g_m \times R_{gd}. \quad (2)$$

Figure 3a displays the contrast of total parasitic capacitance, C_{gg} of HJLTFET and JLTFET. The parasitic capacitances should be as low as possible for efficient operation of the device in RF applications. The JLTFET

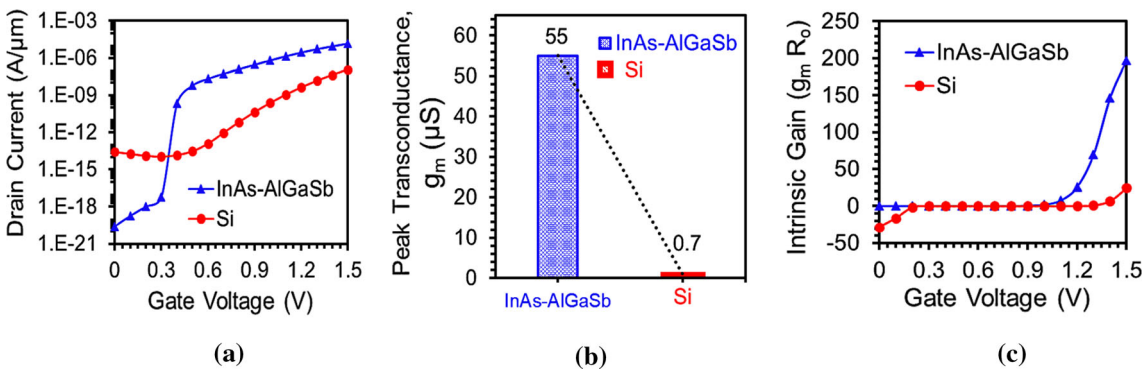

Fig. 2 **a** Transfer characteristics, **b** Peak transconductance, and **c** Intrinsic gain of HJLTFET and JLTFET

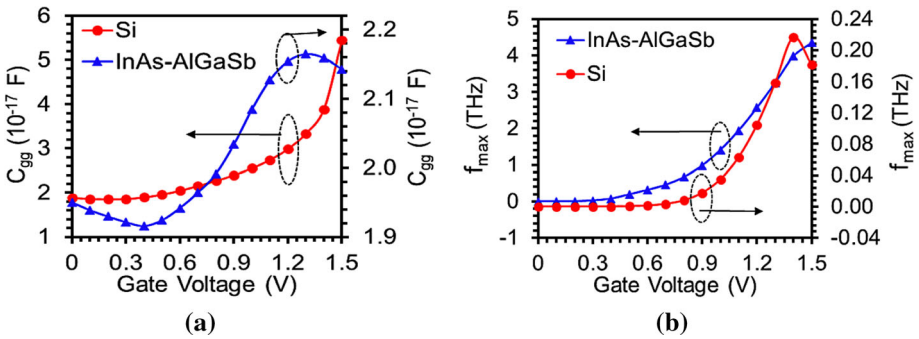

Fig. 3 **a** Total parasitic capacitance (C_{gg}) and **b** Maximum oscillation frequency (f_{max}) of HJLTFET and JLTFET

shows degradation of C_{gg} in comparison to HJLTFET in Fig. 3a. At higher gate voltage, the C_{gg} starts decreasing in HJLTFET, whereas it keeps on rising for the whole gate bias range in JLTFET. Another important parameter in RF analysis is the maximum oscillation frequency, f_{max}. It is the frequency whereupon the power gain turns to unity. It is clear from Fig. 3b that the f_{max} is much higher in case of HJLTFET, due to the direct dependence on cutoff frequency and hence on g_m [Eq. 3 (Verma and Gupta 2021)]. The f_{max} of HJLTFET is 4 THz, whereas it is 0.18 THz for JLTFET.

$$f_{\max} = \sqrt{\frac{f_T}{8\pi\left(R_{gd}C_{gd}\right)}}. \tag{3}$$

Figure 4a shows the comparison of gain bandwidth product, GBP expressed mathematically in Eq. (4) (Verma and Gupta 2021). It is the product of gain and bandwidth of the amplifier.

It is the frequency whereupon the maximum gain is acquired by the device. The HJLTFET achieves a higher peak value of GBP as 50.6 GHz, than JLTFET (0.22 GHz), owing to the significant enhancement in g_m.

$$\mathrm{GBP} = \frac{g_m}{20\pi\left(C_{gd}\right)}. \tag{4}$$

Another parameter of RF FOMs is the transconductance frequency product—product of f_T and device efficiency (Eq. 5) (Verma and Gupta 2021). In Fig. 4b, Due to the enhancement in the g_m and C_{gg}, the peak value of TFP of HJLTFET (1627 GHz) is attained at 0.3 V of gate voltage, whereas JLTFET attains 0.023 GHz peak value of TFP at 1.4 V gate voltage.

$$\mathrm{TFP} = \frac{g_m}{I_{DS}} \times f_T. \tag{5}$$

For the evaluation of speed of transistors, intrinsic delay needs to be taken into account. It is mathematically expressed by Eq. (6) (Verma and Gupta 2021).

$$\tau = \frac{C_{gg} \times V_{dd}}{I_{\mathrm{ON}}}. \tag{6}$$

Figure 5 displays the comparison of intrinsic delay of HJLTFET and JLTFET. Here the intrinsic delay reduces intensively for HJLTFET owing to the enhancement in I_{ON} and C_{gg}. This significant reduction of intrinsic delay leads to fast switching speed of the device as $f_i = 1/\tau$. The intrinsic delay of HJLTFET is 99.6% lower than JLTFET.

4.2 Linearity and intermodulation distortion analysis

This segment presents the detailed study of intermodulation distortion and linearity performance of the aforementioned devices. To attain better linearity and minimum signal distortion for modern wireless communication system, the FOMs need to be examined are the higher order transconductance coefficient (gm_3), second-order voltage

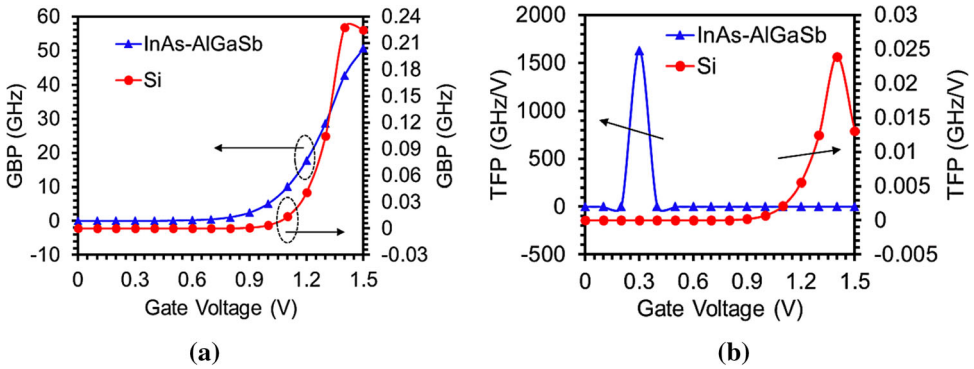

Fig. 4 **a** Gain bandwidth product (GBP) and **b** Transconductance frequency product (TFP) of HJLTFET and JLTFET

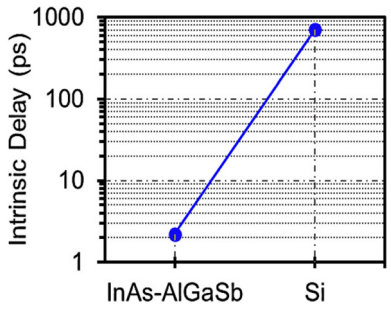

Fig. 5 Comparison plot of Intrinsic delay of HJLTFET and JLTFET

intercept point (VIP2), third-order voltage intercept point (VIP3), third-order input intercept point (IIP3), third-order intermodulation distortion (IMD3), 1-dB compression point. The g_{m3} is the crucial linearity FOM, as it governs the lower limit of distortion in a device. For superior RF and linearity, the g_{m3} of the device should be controlled to a lower limit. This is the dominant parameter for nonlinear behavior of the device. Figure 6 displays the contrast of g_{m3} for HJLTFET and JLTFET, where HJLTFET shows reduction in g_{m3} with the increase in gate voltage. Equation 7 illustrates the mathematical expression for VIP2, which is directly dependent on g_m (Verma and Gupta 2021). Figure 7a shows the comparison of VIP2 with gate voltage for HJLTFET and JLTFET. With the rise in gate voltage, the VIP2 rises in both devices, however, HJLTFET attains higher value of VIP2 due to the enhanced g_m as compared to JLTFET. The HJLTFET attains 2.63 V of VIP2, whereas JLTFET attains only 1.3 V of VIP2 at 1.5 V gate voltage. Thus, HJLTFET exhibits substandard distortion and improved linearity behavior as compared to JLTFET.

$$\mathrm{VIP2} = 4 \times \frac{g_m}{g_{m2}}. \tag{7}$$

Figure 7b displays the disparity of VIP3 with gate voltage. The mathematical formula of VIP3 is defined in Eq. 8, where it is clear that VIP3 is inversely dependent on g_{m3} (the dominant source of nonlinear behavior of a device) (Verma and Gupta 2021). Therefore, VIP3 should

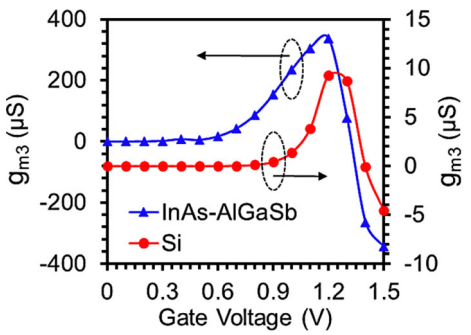

Fig. 6 Comparison plot of g_{m3} of HJLTFET and JLTFET

have the maximum amplitude to suppress the dominance of third order harmonics. From the Fig. 7b, the magnitude of VIP3 seems to be higher in HJLTFET, owing to the enhanced g_m as compared to JLTFET. Thus, HJLTFET proves to be a more linear device giving rise to higher drive current and better efficiency.

$$\mathrm{VIP3} = \sqrt{24 \times \frac{g_m}{g_{m3}}}. \tag{8}$$

Figure 8a illustrates another important FOMs of RF devices, which is IIP3. As defined in Eq. 9, IIP3 depends directly on g_m and inversely on g_{m3} (Verma and Gupta 2021). Here, R_s is presumed as 50 Ω in RF applications. Hence, a system attaining higher g_m and suppressed g_{m3} is desired to achieve a higher value of IIP3. Figure 8a shows the comparison of IIP3 parameter of HJLTFET and JLTFET. As the gate voltage increases, the IIP3 rises for HJLTFET and attains maximum value at 1.3 V of gate voltage, whereas the IIP3 value decreases in case of JLTFET.

$$\mathrm{IIP3} = \frac{2}{3} \times \frac{g_m}{g_{m3} \times R_S}. \tag{9}$$

In order to obtain a linear device, the understanding of IMD3 is essential, as it determines the intermodulation distortion in a device. It can disrupt the information in the nearby channel of the wireless communication systems. Hereafter, to suppress the IMD3, g_{m3} should be reduced (Eq. 10) (Verma and Gupta 2021). Figure 8b demonstrates the disparity of IMD3 for HJLTFET and JLTFET. For lower gate voltage, HJLTFET shows minimum variation of IMD3 as compared to JLTFET causing minimum distortion and better linearity.

$$\mathrm{IMD3} = R_S\left[4.5 \times (\mathrm{VIP3})^3 \times g_{m3}\right]^2. \tag{10}$$

The 1-dB compression point decides the higher limit of the linearity aspect of the device. This is the point up to which the amplifier shows linear behavior and degrades the performance beyond that due to the signal distortions. Hence, the amplifier gain saturation takes place producing a condition called compression. Therefore, the device having higher 1-dB compression point is preferred for lower intermodulation distortion and better linearity performance.

From Fig. 8c, it is inferred that with the rise in gate voltage, the HJLTFET shows rise in 1-dB compression point than JLTFET, due to the higher g_m (Eq. 11), showing better linearity and lower distortion (Verma and Gupta 2021). The HJLTFET attains 11.6% higher value of 1-dB compression point in contrast to JLTFET.

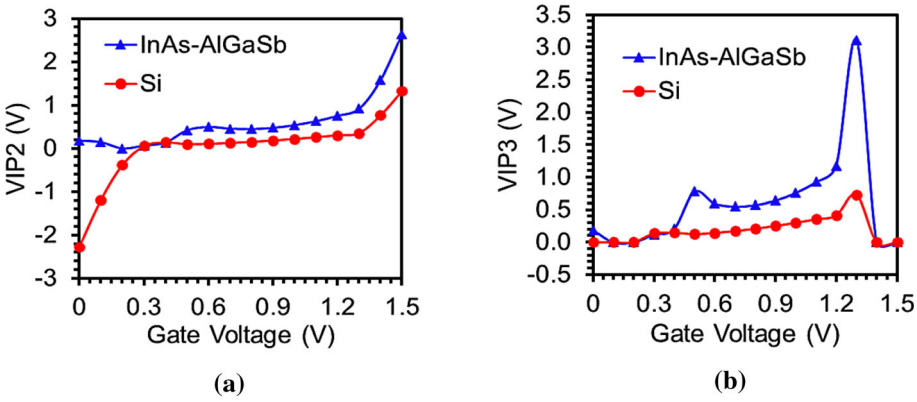

Fig. 7 **a** VIP2 and **b** VIP3 of HJLTFET and JLTFET

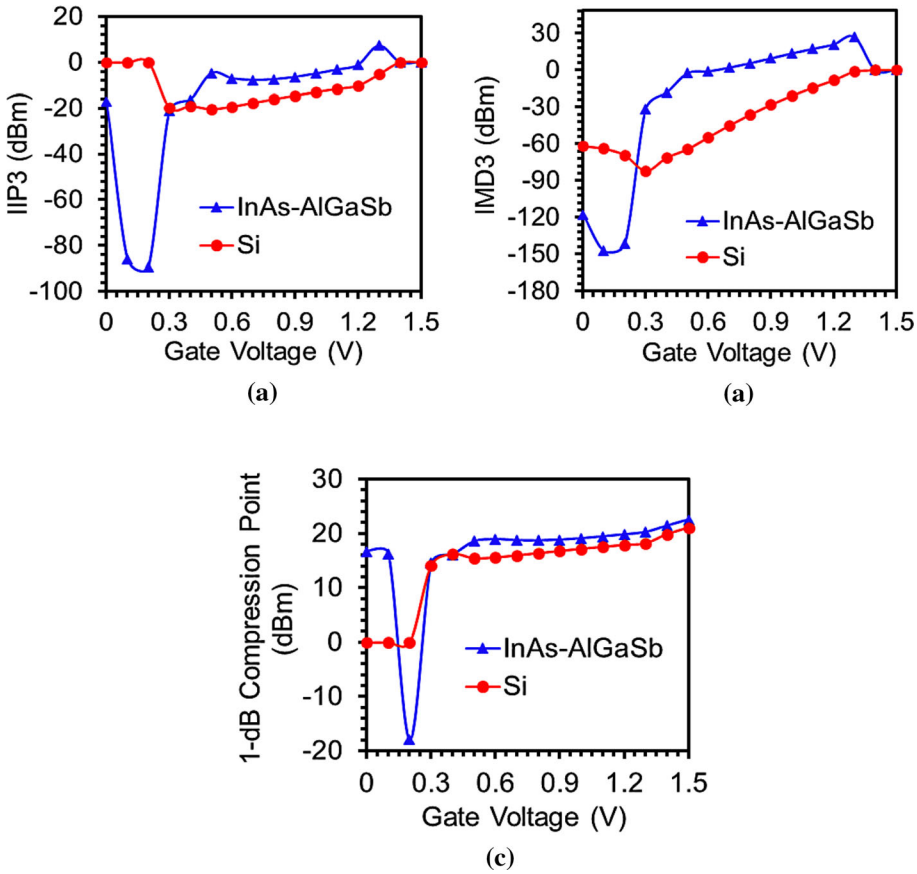

Fig. 8 **a** IIP3, **b** IMD3, and **c** 1-dB compression point of HJLTFET and JLTFET

$$1\text{-dB} = 0.22\sqrt{\frac{g_m}{g_{m2}}}. \tag{11}$$

4.3 Power gains and small signal parameters analysis

To study the feasibility of HJLTFET over JLTFET in high frequency applications, the variation of current gain, unilateral power gain, and maximum available power gain (Gma) have been displayed in Fig. 9a–c. The application of hetero-material InAs-AlGaSb leads to higher current gain and unilateral power gain than homo-material Si (Fig. 9a, b). The higher current gain and unilateral power gain in HJLTFET is attributed to the higher I_{ON} and I_{ON}/I_{OFF}. The HJLTFET attains 1.6 (1.8) times higher current gain (unilateral power gain) than JLTFET. In Fig. 9c, the HJLTFET attains 1.3 times higher Gma as compared to JLTFET signifying the application of HJLTFET in designing of low noise amplifiers over conventional JLTFET.

In small signal equivalent circuit, the study of small signal parameters (addmitance parameters) becomes necessary as the MOSFET can be replaced by Y-parameters—Y_{11}, Y_{12}, Y_{21}, and Y_{22}. In non-quasi static approach, all the

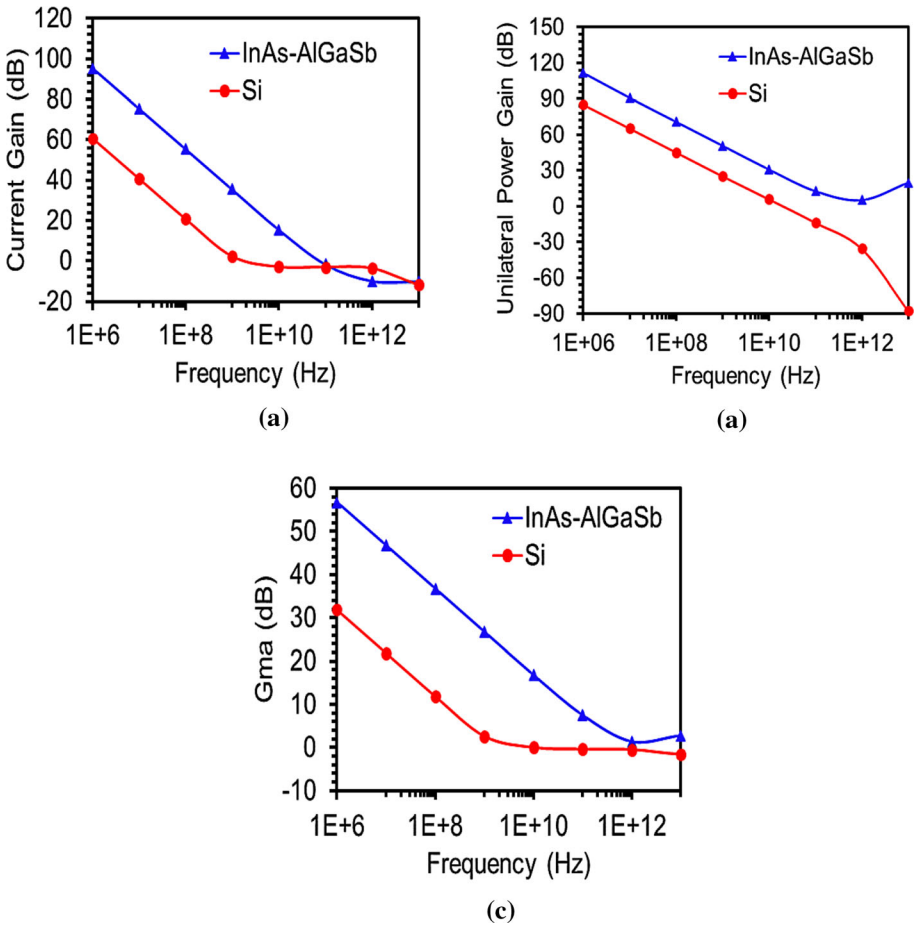

Fig. 9 **a** Current gain, **b** Unilateral power gain, and **c** Maximum available power gain (Gma) of HJLTFET and JLTFET

information regarding the RF FOMs can be extracted directly from the real and imaginary components of Y parameters (Cho et al. 2011). Figure 10a–d demonstrates the variation of real and imginary components of the Y parameters with respect to frequency. In Fig. 10a and d, the Y_{11} and Y_{22} attain smaller values at smaller frequency and increases steadily as the frequency rises. Moreover, the variation of Y_{11} and Y_{22} in HJLTFET is lower in magnitude as compared to JLTFET. In Fig. 10b and c, the Y_{12} and Y_{21} attains greater values at smaller frequency and declines steadily with rise in frequency for both HJLTFET and JLTFET. However, the magnitude of variation is higher in case of JLTFET as compared to HJLTFET showing better reliability of HJLTFET in terms of small signal parameters and RF applications as compared to JLTFET. Table 1 presents the comparison of our proposed device HJLTFET, conventional Si based JLTFET, and recently published TFET design in the literature to show the superiority of HJLTFET over other two devices in the table.

5 Conclusion

In this article, we projected a hetero-material InAs/AlGaSb (x = 0.15) tunneling interfaced JLTFET (HJLTFET) and compared it with conventional silicon material based JLTFET for analog/RF, linearity and intermodulation distortion performance. Owing to the tunnel barrier lowering at the arsenide/antimonide S/C tunneling interface in HJLTFET, the I_{ON} and g_m gets elevated and mitigates the parasitic capacitance. The HJLTFET shows improved intrinsic gain, f_{max}, GBP, and TFP as compared to JLTFET, making the device feasible for RFIC designs. Moreover, the HJLTFET appears to be comparatively linear with lower intermodulation distortion than JLTFET in terms of g_{m3}, VIP2, VIP3, IIP3, IMD3, and 1-dB compression point, showing its suitability for wireless communication systems. The small signal parameters extraction in terms of Y-parameters and power gains show improved results on the implementation of hetero-material InAs/AlGaSb in HJLTFET as compared to JLTFET. Thus, HJLTFET appears to be the superior candidate than JLTFET for RF communication and high frequency applications.

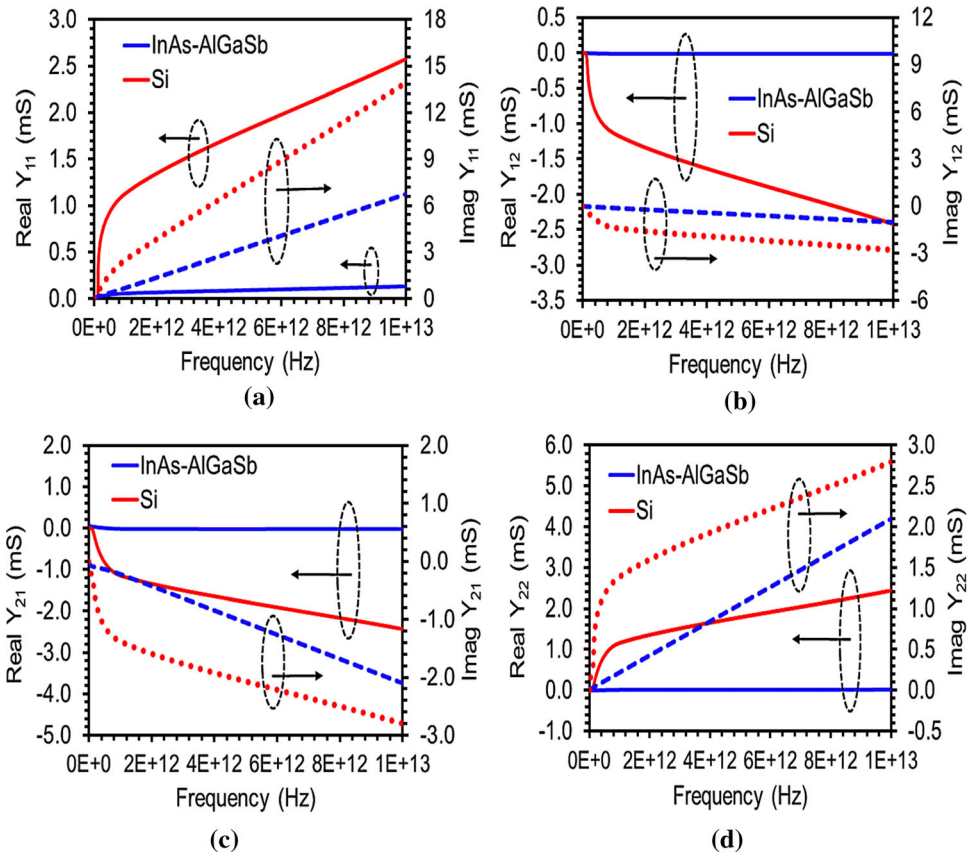

Fig. 10 The Variation of real and imaginary components of the admittance (Y) parameters: **a** Y11, **b** Y12, **c** Y21, and **d** Y22 as a function of frequency for HJLTFET and JLTFET

Table 1 Comparison of device performance with latest TFET design

	I_{ON}/I_{OFF}	Peak g_m (μS)	C_{gg} (F)	TFP (GHz)	GBP (GHz)
H-JLTFET Paras and Chauhan (2019)	10^{12}	7.3	3.5×10^{-15}	2.5	0.35
HJLTFET (Present work)	10^{14}	55	2.1×10^{-17}	1627	50.6
Conv. Si-JLTFET (Present work)	10^{6}	0.7	5.5×10^{-17}	0.023	0.22

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Declarations

Conflict of interests The authors have no competing interests to declare that are relevant to the content of this article.

Compliance with Ethical Standards All the ethical standards have been seen by the authors and will supposed to follow them in future as well.

Consent for publication Not applicable.

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Regular paper

Performance enhancement in a novel amalgamation of arsenide/antimonide tunneling interface with charge plasma junctionless-TFET

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ABSTRACT

In this article, a novel combination of an arsenide/antimonide tunneling interface using binary (InAs) and ternary (AlGaSb) compound semiconducting materials and junctionless tunnel field effect transistor (JLFET) has been explored to induce a charge-plasma based tunable bandgap source/channel (S/C) interface. The hetero-material JLTFET (H-JLTFET) depicts superior performance than conventional homo-material Si JLTFET in terms of DC characteristics showing ~128 and ~1.27×10^8 times higher I_{ON} and I_{ON}/I_{OFF} along with ~10^{-6} times, ~50%, and 88% lower I_{OFF}, V_{th}, and SS. The superior performance is attributed to the conduction band local minimum induced at the channel yielding to narrower tunneling barrier width at an optimized Al-mole fraction (0.15) of AlGaSb. Furthermore, 77 times higher g_m of H-JLTFET led to 5×10^6 and 205 times higher device efficiency and f_T along with ~66% reduction in the parasitic capacitance making it favorable for high-speed switching applications as compared to Si JLTFET.

1. Introduction

The tunnel field effect transistor (TFET) has arisen as a potential candidate in modern communications systems by overcoming MOSFETs' prime issue related to the subthreshold swing (SS) being greater than 60 mV/decade [1,2]. However, TFET faces an issue of inferior ON state current and ambipolar conduction. Moreover, the fabrication complexity increases due to doping junctions, which stipulates a higher thermal budget for complex thermal annealing, random dopant fluctuations, and ion-implantation. Therefore, all the attention has been shifted towards an endurable and economical solution of junction restraint. Inspired by Lilienfeld' junctionless transistor design [3], many junctionless FETs have been proposed and fabricated [4–6]. The Junctionless TFET is proved to be the most promising architecture among the various TFET engineering schemes to resolve the above-said issues by consolidating the benefits of a junctionless FET (elevated ON current) and a TFET (steeper SS). The nonexistence of p-n doping junctions also boosts the immunity of TFET towards short channel effects [7,8].

Another key in determining the electrical performance of TFET is the semiconductor material. The Silicon TFET being an indirect semiconductor with a large energy bandgap based homojunction device diminishes the carrier mobility and band-to-band tunneling probability, and hence the ON state current degrades [2,9–11]. To overcome the drawbacks of homojunction-TFETs, the direct bandgap III-V compound semiconducting materials have been used in the past few years. Using a lower and higher bandgap III-V compound semiconducting material in the source and channel, respectively, a heterostructure-based junctionless TFET is formed, which results in improved electrical performance compared to homojunction-TFETs [12–15]. The application of high-k materials in combination with semiconducting materials and lattice mismatch between two hetero-materials originates the interface trap charges due to trapping of mobile ionic and immobile charges at the semiconductor/oxide and source/channel (S/C) interface, which deteriorates the device reliability and lifetime [16–17].

The researchers have proposed several nTFET architectures by incorporating hetero-junction arsenide/antimonide tunneling interfaces in history. Lu et al. [18], and Li et al. [19], achieved remarkable results beating other TFET designs by forming A "T-shape" vertical architecture using an InAs/AlGaSb hetero-junction. Zhou et al. [20] has reported the first demonstration of a self-aligned InAs/Alo.45Gao.55Sb hetero-junction TFET, using an optical-lithography-only. The InAs/Al0.05 Ga0.95Sb based nanowires have been designed using a virtual TFET technology platform by Baravelli et al. [21,22]. However, the analysis of InAs/AlGaSb hetero-materials has not been explored for the junctionless TFET architecture to the best of our knowledge.

In this work, we propose a novel III-V compound semiconducting

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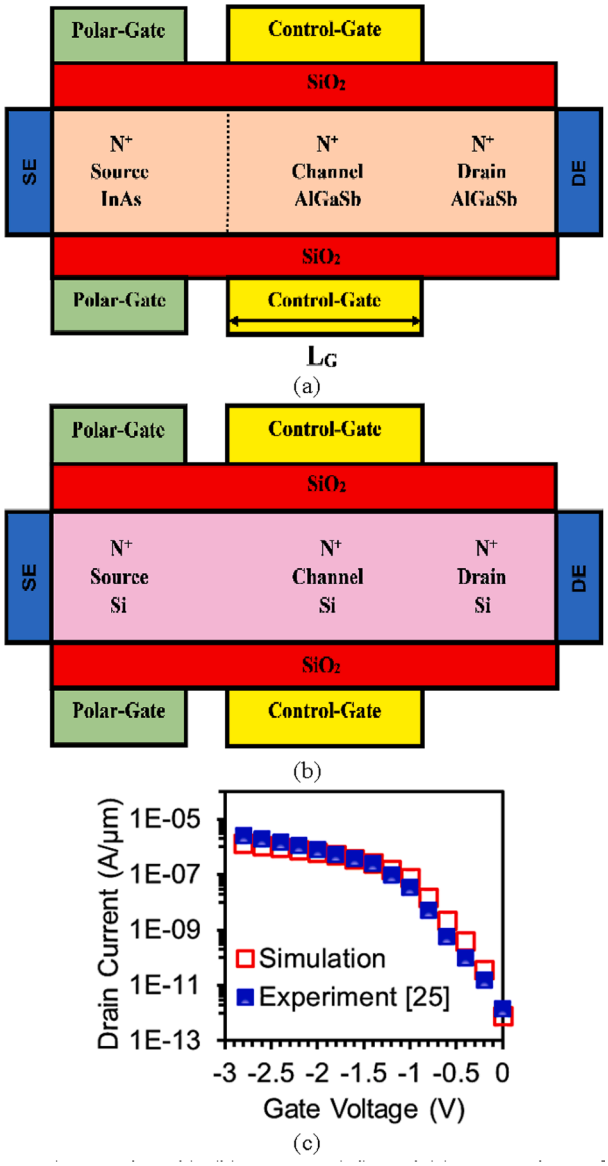

Fig. 1. Device architecture of (a) H-JLTFET (InAs-AlGaSb), (b) JLTFET (Si), and (c) Comparison of experimental [25] and simulated transfer characteristics of TFET.

hetero-materials, InAs/AlGaSb based junctionless TFET (H-JLTFET). Its fundamental mechanism is based on the induction of charge carriers by the charge plasma concept to transform a highly doped $n^+ - n^+ - n^+$ substrate into the conventional $p^+ - i - n^+$ substrate by using two different work function gates over the source and channel regions [8,12,15]. The proposed device involves the careful optimization of many key elements, including the source and channel material parameters, heterostructure junctionless architecture, doping level, and gate length. The hetero-material engineering is incorporated by using lower bandgap InAs in the source and higher bandgap AlGaSb in the channel and drain sections. Thereafter, bandgap engineering is applied by optimizing the Al mole fraction in a ternary compound semiconducting material, AlGaSb based on higher ON state current, steeper SS, and higher current switching ratio. The suitability of lattice-matched standard III-V growth and processing techniques is the prime reason for choosing these materials [1]. The performance of our hetero-material-based device, H-JLTFET has been compared with homo-material-based JLTFET using Si.

Table 1
Device design parameters.

Parameter	Symbol	Value
Channel Length	L_G	20 nm
Body Thickness	T_{Body}	3 nm
Doping Concentration	N_D	1×10^{19} cm^{-3}
Oxide thickness	T_{OX}	2 nm
Isolation thickness	L_{Gap}	2 nm
CG work Function	ϕ_{CG}	4.5 eV
PG Work Function	ϕ_{PG}	5.93 eV

2. Device design and simulation

Fig. 1 illustrates the architecture of (a) hetero-material (H-JLTFET) and (b) homo-material (JLTFET) junctionless tunnel FETs. The device design parameters are displayed in Table 1. The Al mole fraction in AlGaSb is set at 0.15 during the simulations of H-JLTFET device. SiO_2 (k = 3.9) has been used as the dielectric material in the oxide region in both devices. The work functions of control gate (CG), polar gate (PG) and other parameters are retained in both devices to compare results. All the simulations of H-JLTFET and JLTFET are carried out in Silvaco-ATLAS simulator [23]. The most important model used in our simulations is the non-local band-to-band tunneling model. In TFETs, the band-to-band tunneling current depends on the band edge profile at the S/C junction and it strongly impacts the potential and band energies at and around the junction. However, as a result of this strong coupling, the issues of convergence appear in few situations. In such cases, other standard tunneling models can also be implemented along with non-local band-to-band tunneling model.

The other models invoked in the simulations are the Shockley-Read-Hall (SRH) recombination model, the band gap narrowing model, Auger recombination model, and Fermi Dirac Statistics. To include the effects of mobility due to parallel- perpendicular electric field, temperature, and concentration, the CVT (Lombardi) model is applied. To include the quantum effects, we implemented the Hansch's quantum confinement model [24]. Before simulating our proposed device, we have validated the simulation set up with the experimental data extracted from the fabrication based published work [25]. Fig. 1(c) illustrates the endorsement of simulation set up with the experimental data in terms of transfer characteristics. Due to the lack of experimental data availability for InAs-AlGaSb based planar TFET, we performed the model calibration for Si-SiGe TFET, keeping the device parameters and the biasing conditions exactly as that of the work reported in [25]. The close proximity of the simulation and experimental results authorizes the model deliberations of the simulation set up.

In the proposed device's fabrication process, the hetero-material InAs/AlGaSb channel can be formed by using a self-aligned optical-lithography technique as reported in [20]. The CG and PG with different work functions can be formed at the upper face of the channel by using electron beam lithography, whereas the isolation layer between CG and PG can be formed by using various modern techniques such as extreme ultraviolet lithography, X-ray lithography, and ion projection lithography) as reported in [26,27]. The oxide region and the source and drain contacts can be deposited using the atomic layer deposition (ALD) process at a temperature below 3500 °C [28].

3. Results and discussion

In this segment, the impact of III-V compound semiconducting hetero-materials has been examined over the homo-material in junctionless TFET device structure for a supply voltage, $V_{GS} = 0.0\ V$, $V_{DS} = 1.5\ V$ for OFF state, and $V_{GS} = 1.5\ V$ and $V_{DS} = 1.5\ V$ for ON state to analyze the analog behavior of both the devices. The hetero-material incorporated in H-JLTFET gives rise to a tunable bandgap at the source/channel interface (S/C) on applying the band engineering via

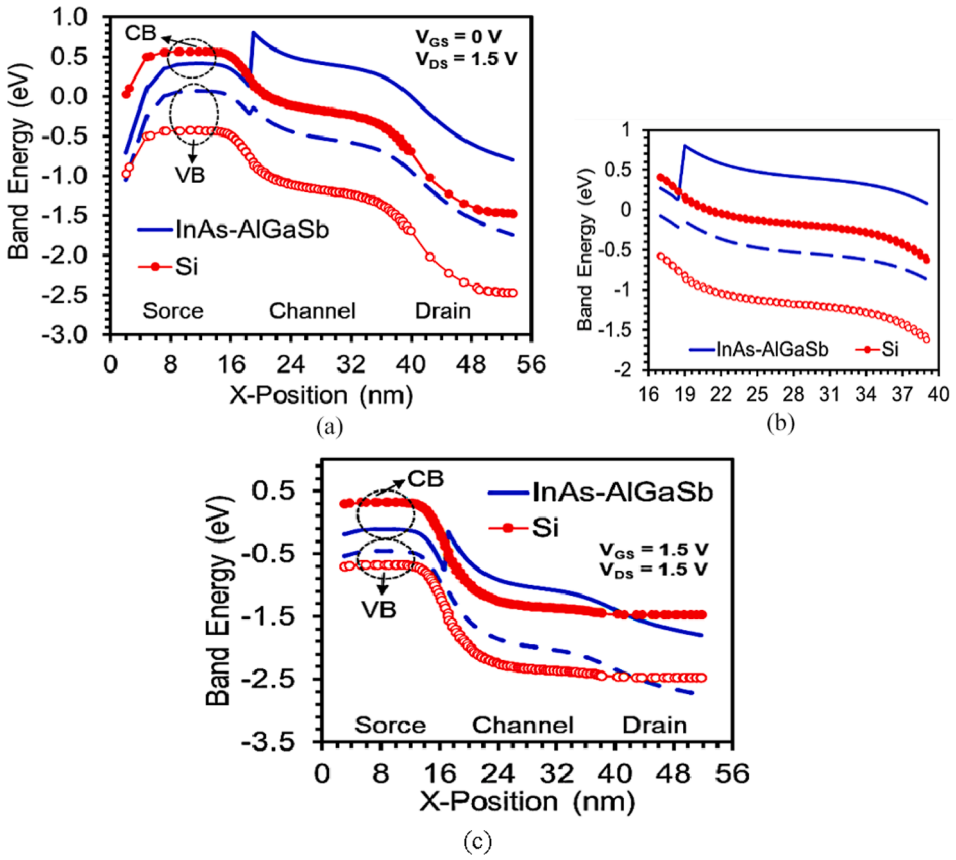

Fig. 2. Comparison plots of H-JLTFET and JLTFET for (a) OFF state, (b) magnified view of band bending at the S/C and D/C interface, and (c) ON state energy band diagram.

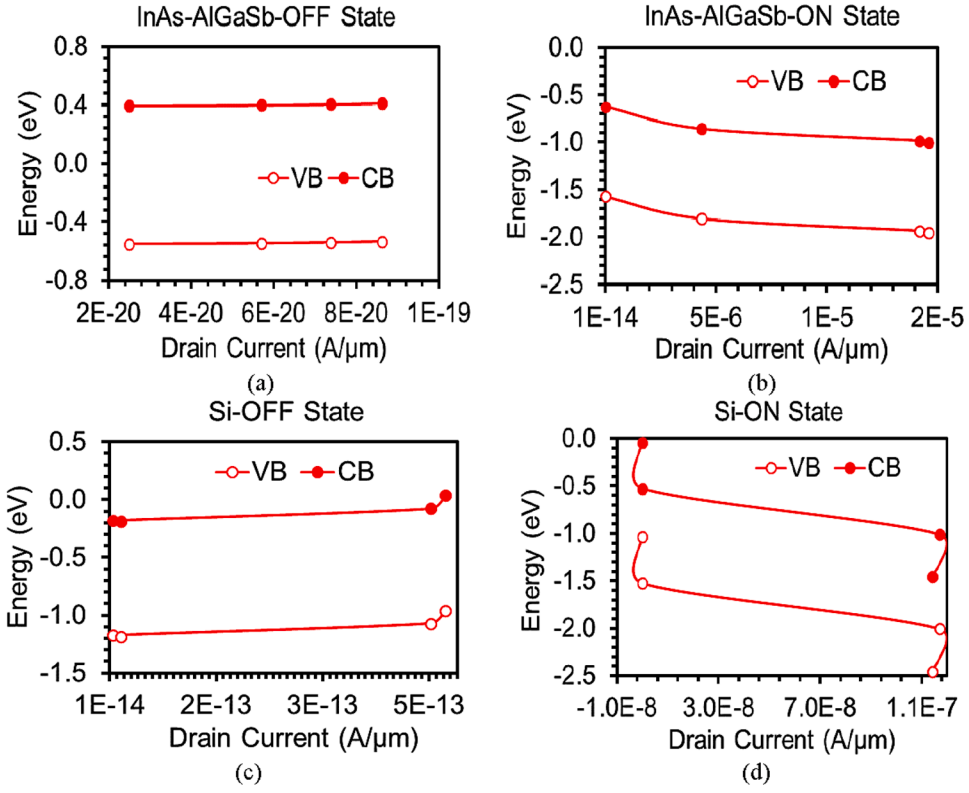

Fig. 3. Energy as a function of drain current for (a) H-JLTFET OFF state, (b) H-JLTFET ON state, (c) JLTFET OFF state, and (d) JLTFET ON state.

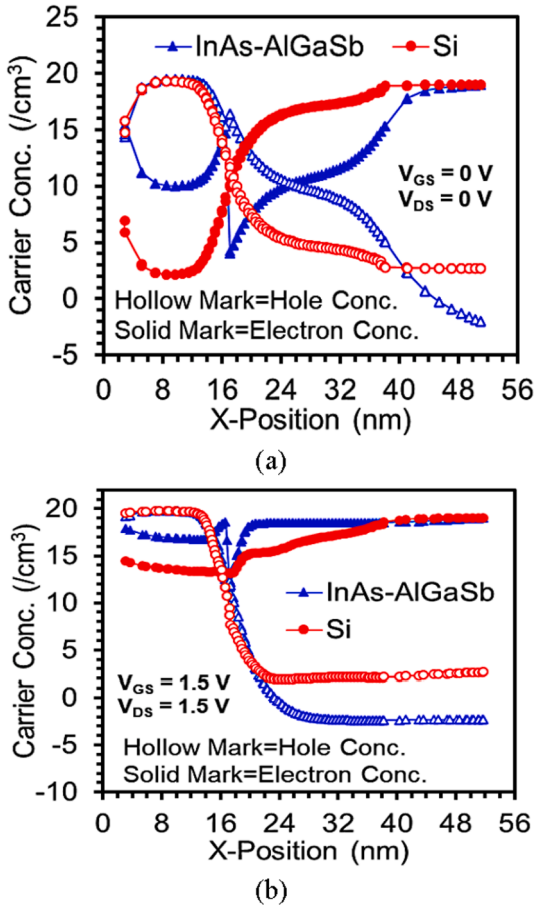

Fig. 4. Comparison plots of H-JLTFET and JLTFET for (a) Thermal equilibrium and (b) ON state carrier concentration.

AlGaSb and InAs material in the channel and source section, respectively. The energy bandgap of ternary material, AlGaSb dependent on the Al-mole fraction (x.comp) is approximated by the function [23,29]:

$$E_g^{Al_xGa_{1-x}Sb} = \left[x.E_g^{AlSb} + (1-x).E_g^{GaSb} - x.(1-x)C_{Al_xGa_{1-x}Sb}\right], \quad (1)$$

where, $C_{Al_xGa_{1-x}Sb}$ is the bowing factor for energy bandgap for AlGaSb given as below:

$$C_{Al_xGa_{1-x}Sb} = [1.22x - 0.044] \quad (2)$$

Fig. 2(a) and (c) display the energy diagram of H-JLTFET and JLTFET along the channel direction in the OFF state and ON state, respectively. The current conduction in TFET controlled by the gate voltage, is strongly dependent on the tunneling barrier width, which, further depends on the energy bandgap at the S/C interface. In H-JLTFET, at the hetero-material S/C interface, InAs has the lower energy bandgap than AlGaSb; thereby, leading to lower tunneling barrier width, which is still higher at the D/C interface due to the presence of homo-material AlGaSb. As shown in Fig. 2(a), when no gate biasing is applied (OFF state), the potential barrier at the S/C interface is elevated enough to restrict carriers' flow across the junction. In that case, only minor leakage carriers having energy higher than the S/C interface barrier width can tunnel into the channel and get accumulated at the drain node. We have added the magnified view of Fig. 2(a) to better clarify the energy band diagram at the S/C interface for both H-JLTFET and JLTFET. As shown in Fig. 2(b), the conduction band at the drain and valence band at the source are somewhat overlapping in the OFF state; however, there is no such overlapping in case of H-JLTFET. Hence, the tunneling window becomes shorter in case of Si-JLTFET, giving rise to

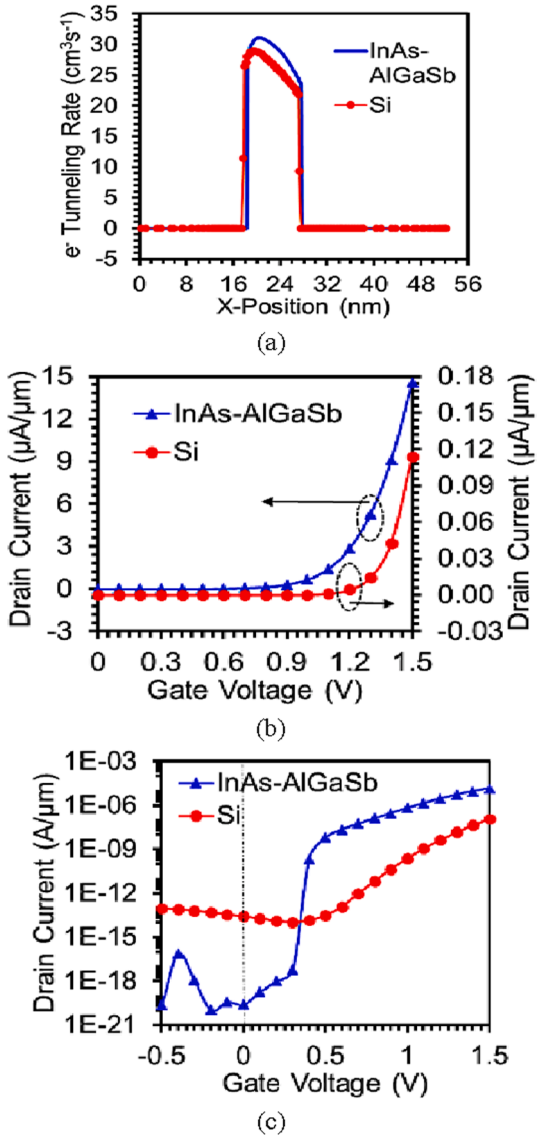

Fig. 5. (a) Band to band electron tunneling rate, (b) Transfer characteristics in linear scale, and (c) Transfer characteristics in log scale of H-JLTFET and JLTFET.

higher leakage current. On applying the gate bias (ON state), the gate electric field modulates the channel so that the conduction band of the channel is pulled down by inducing a local minimum of the conduction band edge at the S/C interface owing to the existence of hetero-material in H-JLTFET, as revealed in Fig. 2(c). As an outcome, the tunneling barrier width at the S/C interface abruptly diminishes, and hence, larger number of electrons tunnel through the barrier on account of the dominance of band-to-band tunneling between the local minimum of the conduction band of channel and valence band of the source. However, the homo-material Si having the higher bandgap at the S/C interface leads to a wider tunneling barrier. As a result, even on applying the gate biasing to JLTFET, lower number of electrons tunnel through the barrier than H-JLTFET.

Fig. 3(a)–(d) reflect the relation of band bending behaviour and drain current of both devices in the OFF state and ON state. If we see the OFF state Fig. 3(a) and (c), the energy gap between the conduction band and valence band of InAs-AlGaSb HJLTFET is larger than that of Si JLTFET. The leakage current variation is in the range of $\sim 10^{-20}$ A/μm for H-JLTFET, whereas it varies from 10^{-14} to 10^{-13} A/μm for JLTFET. In the ON state, both H-JLTFET and JLTFET attain I_{ON} current in the

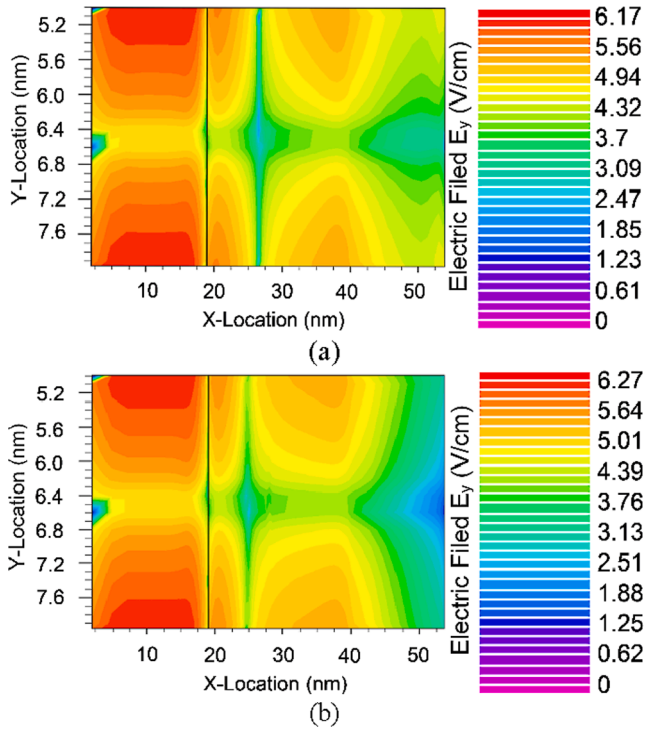

Fig. 6. Normal electric field, E_y contour plot of (a) H-JLTFET and (b) JLTFET along the device length in log scale at $V_{GS} = 1.5$ V, $V_{DS} = 1.5$ V.

range of $\sim 10^{-5}$ A/μm and $\sim 10^{-7}$ A/μm(Fig. 3(b) and (d)).

When no biasing is applied to the gate and drain, the device is in the thermal equilibrium state. The PG and CG give rise to a P-i-N doped architecture even in the absence of any physical doping in both the devices (see Fig. 4(a)). The higher electron concentration of H-JLTFET than JLTFET at the S/C junction leads to abruptness at the junction. When the gate biasing is applied to CG (Fig. 4(b)), the hetero-material S/C junction gives rise to an n-doped pocket region beneath the spacer region between PG and CG in H-JLTFET. This increment in the electron concentration under the spacer region induces the conduction band local minimum at the S/C interface and hence the tunneling barrier width gets narrowed. The electron concentration in the channel is abrupt in H-JLTFET, while JLTFET has a gradual increment in the channel section's electron concentration.

In Fig. 5(a), the abrupt band bending and narrow tunneling barrier thickness of H-JLTFET leads to the BTBT electron tunneling rate of 7.6% higher than JLTFET. Fig. 5(b) correlates the linear scale transfer characteristics of the aforementioned devices. As evident from the figure, the ON current, I_{ON} of H-JLTFET shows a higher value than JLTFET. The enhanced I_{ON} of H-JLTFET resulted from the steeper band bending, induces the conduction band local minimum at the hetero-material S/C interface. Whereas low I_{ON} in JLTFET is due to the wider barrier width of the Si homo- material S/C interface that hinders electrons' tunneling rate. The I_{ON} of hetero-material InAs-AlGaSb (H-JLTFET) device is ~128 orders higher in magnitude than homo-material Si device (JLTFET). Fig. 5(c) compares the transfer characteristics of H-JLTFET and JLTFET in log scale, depicting the comparison of I_{ON}, I_{OFF}, and I_{AMB}. As evident from the characteristics, the I_{OFF} of the proposed hetero-material S/C interface H-JLTFET reduces from 10^{-14} to 10^{-20} as compared to homo-material JLTFET. In the OFF state, the CG voltage is at zero and due to the drain biasing, the source/gate electronic potential (ϕ_{CG}) reduces and the drain/gate electronic potential ($\phi_{CG} + V_{DD}$) rises. This leads to the overlapping between the energy bands of the channel and drain. The higher electric field at the D/C junction of JLTFET as compared to H-JLTFET triggers the higher tunneling rate of electrons across the D/C junction leading to a higher leakage current. The ambipolar behavior is

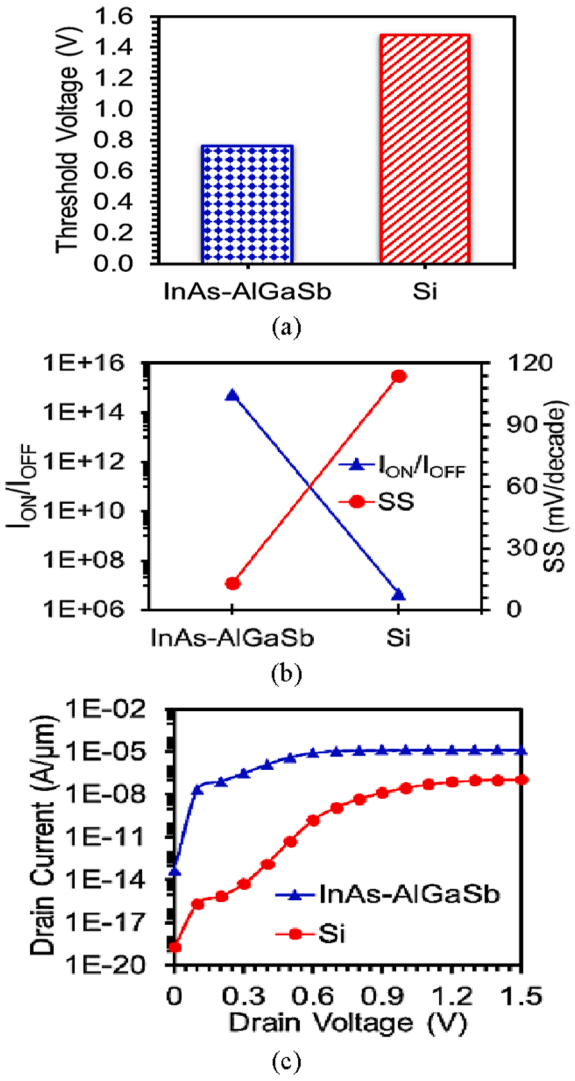

Fig. 7. (a) Threshold voltage, (b) Current switching ratio, I_{ON}/I_{OFF} and SS, and (d) Output characteristics of H-JLTFET and JLTFET.

also determined at the D/C junction of the TFET as a function of negative gate bias. The ambipolar current of H-JLTFET is also suppressed compared to JLTFET as a consequence of the wider D/C. The I_{AMB} of H-JLTFET is 2.46×10^{-20} A/μm, whereas JLTFET exhibits I_{AMB} of the order of 9.7×10^{-14} A/μm (see Fig. 5(c)).

Fig. 6(a) and (b) show the level curve of the normal component of electric field, E_y for H-JLTFET and JLTFET. The higher value of E_y at the interface can limit the performance of the device by increasing the reliability issues such as the gate leakage current and interface trap generation [30,31]. However, the n-pocket region induced beneath the spacer region by the hetero-material S/C interface in H-JLTFET reduces the peak E_y to ~1.6% compared to Si JLTFET making H-JLTFET more immune to interface traps and leakage current.

The threshold voltage is a crucial parameter determining the device's capability to get turned on at the lowest gate voltage possible. The threshold voltage in this work is retrieved through the constant current method and is found to be V_{GS} @ $I_{DS} = 10^{-7}$ A. Fig. 7(a) indicates the achievement of lower threshold voltage in H-JLTFET than JLTFET. The threshold voltage of H-JLTFET is about 0.76 V, whereas JLTFET is still in the OFF state at this voltage. The V_{th} of JLTFET is 1.48 V, the gate voltage at which the H-JLTFET attains the peak tunneling current. Another essential parameter for determining the device efficiency to shift from the OFF to ON state is the current switching ratio, I_{ON}/I_{OFF}.

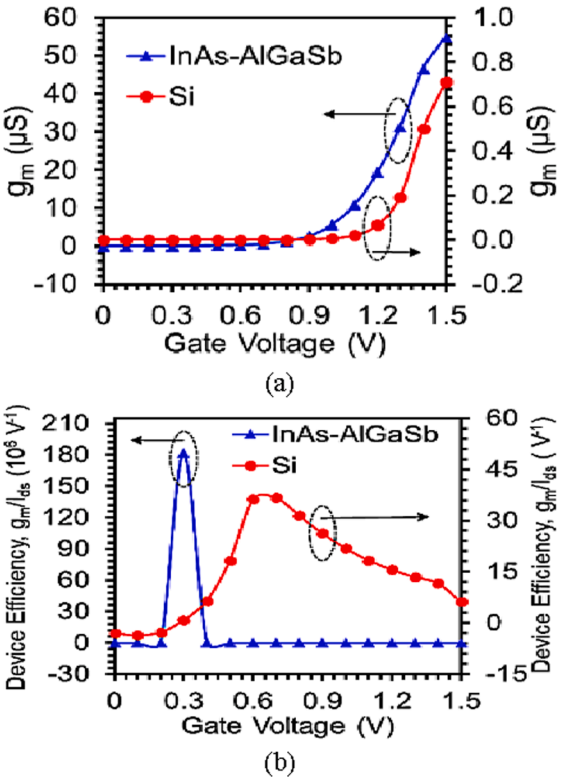

Fig. 8. (a) Transconductance, g_m and (b) Device efficiency of H-JLTFET and JLTFET at constant drain bias V_{DS} = 1.5 V.

Along with I_{ON}/I_{OFF}, the SS is a significant factor that defines the device's capability to shift from OFF to ON state. Fig. 7(b) represents the comparison plot of I_{ON}/I_{OFF} and SS for the two aforementioned devices, where the optimized hetero-materials combination, InAs-AlGaSb along with junctionless technology (H-JLTFET) leads to ~1.3×10^8 times higher I_{ON}/I_{OFF} and ~88% smaller SS as compared to homo-material Si-based device (JLTFET) showing its superiority over JLTFET in making abrupt transition and fast switching speed applications. The consequences of the wider tunneling barrier and the inferior tunneling rate of electrons in Si JLTFET are poor V_{th}, I_{ON}/I_{OFF}, and SS results.

The aforementioned devices' output characteristics for $V_{GS} = 1.5$ V are displayed in Fig. 7(c). The drain current of H-JLTFET starts rising for lower V_{DS} value, and after a certain limit, the drain current becomes independent of V_{DS} and finally saturates. The higher tunnel coupling offered by H-JLTFET attributes to an earlier saturation point with higher drain current whereas, JLTFET exhibits lower drain current and later saturation at a higher drain voltage.

In TFETs, the drain current is regulated by the gate voltage; therefore the transconductance, g_m becomes the most crucial factor in determining the analog performance of TFET. It is the ratio of output current to input voltage at constant drain bias, which measures the device's amplification capability. Fig. 8(a) displays the disparity of g_m with respect to gate voltage at $V_{DS} = 1.5$ V for the aforementioned devices. The g_m variation of H-JLTFET shows significant improvement at lower gate voltage, whereas JLTFET achieves the peak vale of g_m at a larger gate voltage. The g_m peak value of H-JLTFET is ~77 times higher than that of JLTFET, implying a better voltage to current conversion rate. The hetero-material (InAs-AlGaSb) S/C interface applied in H-JLTFET initiates the abrupt upsurge in the output current at lower input voltage, which leads to a higher g_m and hence higher gain. For high-frequency RF applications, the parasitic capacitances associated with the device should be lowest to minimize its effect on the power dissipation and switching speed of the device. The increment in parasitic capacitances influences the signal distortion and circuit oscillations by creating a path

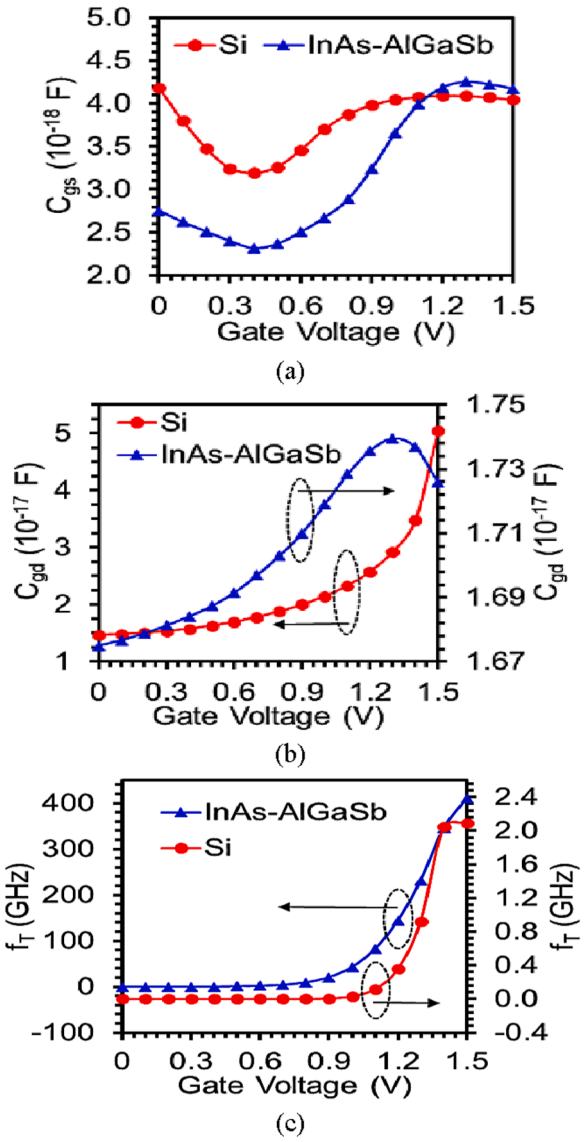

Fig. 9. Comparative plot of (a) C_{gs}, (b) C_{gd}, and (c) f_T as a function of gate voltage for H-JLTFET and JLTFET at constant drain bias V_{DS} = 1.5 V.

between the device's input and output nodes. Further, Fig. 8(b) displays the comparison plot of device efficiency, called transconductance generation factor (TGF) of two aforementioned devices, as a function of gate voltage. TGF is the ratio of transconductance to drain current, which measures the efficiency of converting DC parameter (I_d) into AC parameters (g_m). The H-JLTFET achieves a significantly higher device efficiency of 181 MV^{-1} at a lower gate voltage of 0.3 V, whereas JLTFET achieves a maximum of 36 V^{-1} at 0.6 V. The additional increase in gate voltage results in a fall in TGF due to the dominance of drain current over g_m.

Fig. 9(a) and (b) represents the comparison plot of H-JLTFET and JLTFET for parasitic capacitances, C_{gs} (gate to source), and C_{gd} (gate to drain capacitance) at V_{DS} = 1.5 V. A small-signal AC analysis is performed at a frequency of 1THz to obtain the parasitic capacitances. In Fig. 9(a), C_{gs} of both devices initially decreases with an increment in V_{GS} upto 0.4 V and then upsurges as soon as V_{GS} rises above 0.4 V. The upsurging trend of both devices is because of the inter-gate capacitance delivered by PG over the source region. However, H-JLTFET achieves a lower value of C_{gs} upto a certain gate voltage and then, it marginally increases at a higher gate voltage. The coupling between source and gate is reduced by widening of inversion layer from drain to source. The

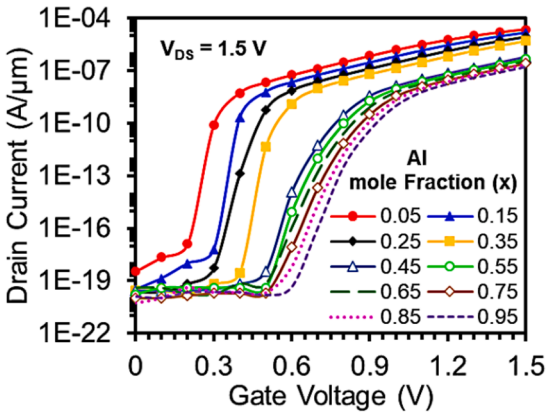

Fig. 10. Turn-on characteristics of H-JLTFET for different Al-mole fraction (x-component) in $Al_xGa_{1-x}Sb$ as channel.

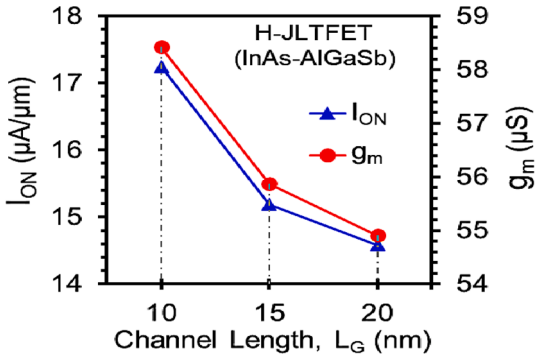

Fig. 11. Impact of channel length scaling on ON current, I_{ON} and transconductance, g_m of H-JLTFET.

inversion layer is formed from the drain to the source, so that C_{gd} shows a dominating trend over C_{gs} with an increasing gate voltage (Fig. 9(b)). Due to the reverse-biased S/C junction in TFETs, the potential drop across this junction is quite larger than the D/C junction. Thus, the C_{gd} is much higher than C_{gs} as a result of charge decoupling at the source due to a larger potential drop at S/C junction. The H-JLTFET attains a much lower value of C_{gd} in comparison to JLTFET as revealed in Fig. 9(b) owing to the wider potential barrier at the D/C junction. The C_{gd} of H-JLTFET is approximately 66% smaller than JLTFET for $V_{GS} = 1.5$ V. Another important parameter determining the switching speed of the device is cut-off frequency f_T at which the current gain becomes unity (see Fig. 9(c)). It is directly proportional to g_m and inversely to the parasitic capacitances [32], as given by Eq. (3)

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{3}$$

Hence, Eq. (3) infers that f_T is degraded by the higher parasitic capacitances. The peak value of f_T is 410 GHz and 2 GHz for H-JLTFET and JLTFET, respectively, as shown in Fig. 9(c). The 205 times elevated value of f_T due to the amalgamation of hetero-materials at the S/C interface in H-JLTFET makes it clear that f_T is dominated by g_m, indicating the negligible dependence on parasitic capacitances.

In Fig. 10, the impact of Al-mole fraction in $Al_xGa_{1-x}Sb$ has been illustrated in the form of transfer characteristics of H-JLTFET by varying the Al-mole fraction from 0.05 to 0.95. For an optimized device response, the Al-mole fraction in the channel and drain region plays a vital role. It is apparent from the figure that as we increase the x-component of Al, the I_{ON} of H-JLTFET starts decreasing along with an increment in I_{OFF} due to the enlarged bandgap at hetero-S/C interface, which degrades the current switching ratio and SS of H-JLTFET. The x-component of 0.15 gives the best outcomes in terms of I_{ON}/I_{OFF} and SS, making it suitable for high-speed switching applications. We have extracted the result characteristics, the ON current, I_{ON} and transconductance, g_m of our proposed device by scaling down the channel length from 20 nm 10 nm to analyse the impact of channel length scaling on device performance as shown in Fig. 11. The oxide thickness and isolation between PG and CG is kept the same. The scaling of channel length in H-JLTFET from 20 nm to 10 nm leads to the reduction in the effective channel length. The wider band-gap drain becomes closed to the S/C interface and hence the tunneling distance becomes narrow. In the ON state, the tunneling probability of charge carriers is increased due to the abrupt band bending at the S/C interface for the shorter channel length. Therefore, as shown in Fig. 11, the ON current increases by 18% as we scale down the channel length from 20 nm to 10 nm. Also, g_m shows an improvement of 6.4% on scaling down the channel length from 20 nm to 10 nm in H-JLTFET. The enhanced tunneling of charge carriers at the S/C interface improves the current driving capability of the device and hence g_m is increased with shorter channel length. Therefore, H-JLTFET has demonstrated significant potential in channel length scaling. Our proposed device, H-JLTFET, shows appreciable improvement in the form of analog figure of merits (FOMs) in comparison to conventional Si-JLTFET and recently published junctionless TFET designs in the literature, as mentioned in Table 2.

Table 2
Comparison of result characteristics of present work with previously published TFET designs.

	DG-HJ-JLTFET [14]	H-JLTFET [33]	H-JLTFET (Present work)	Conv. Si-JLTFET (Present work)
I_{ON} (μA/μm)	1.0	6.0	14.5	0.11
I_{OFF} (A/μm)	1.0×10^{-11}	1.72×10^{-18}	2.57×10^{-20}	2.56×10^{-14}
I_{ON}/I_{OFF}	1.0×10^{5}	2.3×10^{12}	5.67×10^{14}	4.41×10^{6}
SS (mV/decade)	42	> 60	13.2	114.3
g_m (μS)	–	5.5	54.9	0.71
f_T (GHz)	–	–	410	2.09

4. Conclusion

For the first time, in the present piece of work, a hetero-material combination of a binary and ternary compound semiconducting material, InAs-$Al_{0.15}Ga_{0.85}Sb$, has been reported for a charge plasma based double gate junctionless TFET by incorporating tunable bandgap engineering at the S/C interface. The analog FOMs revealed that our proposed device, H-JLTFET is a better candidate in comparison to conventional Si based JLTFET. As an outcome of the narrower barrier width at the S/C interface, H-JLTFET achieves the highest I_{ON} and I_{ON}/I_{OFF} as ~14 μA/μm and ~10^{14}, which is ~128 and ~1.27×10^{8} orders higher in magnitude than JLTFET, respectively. The III-V group hetero-material S/C interface reduces the V_{th} and SS by ~50% and ~88% as compared to JLTFET, respectively. Further, the wider potential barrier at D/C interface of H-JLTFET suppresses the I_{OFF} and I_{AMB} from an order of 10^{-14} to 10^{-20}. Additionally, the InAs-AlGaSb hetero-material interface reduces the parasitic capacitance to ~66% as compared to Si homo-material JLTFET. Moreover, f_T of H-JLTFET is enhanced to 205 times as that of Si JLTFET. Thus, hetero-material InAs-AlGaSb junctionless TFET can be considered as an appropriate replacement of conventional homo-material Si JLTFET for high-speed switching applications.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence

the work reported in this paper.

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Appendix A. Supplementary material

Supplementary data to this article can be found online at https://doi.org/10.1016/j.aeue.2021.153669.

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Band gap and gate metal engineering of novel hetero-material InAs/GaAs-based JLTFET for improved wireless applications

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ABSTRACT

This paper investigates the reliability of a dual metal gate-hetero-material junctionless tunnel FET (DMG-HJLTFET), by using a novel combination of III–V compound semiconducting materials, InAs (lower bandgap) in the source region and GaAs (higher bandgap) in the channel and drain regions. We applied bandgap engineering and dual material gate engineering to improve the linearity metrics and distortion parameters by optimizing an appropriate lower work function tunnel gate toward the source and higher work function supplementary gate toward the drain and compared all the results with SMG (single metal gate)-HJLTFET and Si-JLTFET. The DMG-HJLTFET showed marked improvements in terms of I_{ON}, I_{ON}/I_{OFF}, SS, g_m, g_{m3}, VIP2, VIP3, and 1-dB compression point. The input power, IIP3 of DMG-HJLTFET, is 158% greater than SMG-HJLTFET and is 154.7% greater than Si-JLTFET. The distortion power, IMD3 of DMG-HJLTFET, is 171.8% and 20.5% lower than SMG-HJLTFET and Si-JLTFET, respectively, thereby making it suitable for low-power distortion-free wireless communication systems.

1 Introduction

The expansion of modern wireless technology has increased the urge to downscale the dimensions of the modern communication systems. To effectuate higher speed operations and faster calculations in mobile communication industry, the present technology necessitates innovations and high-performance communication systems. For advanced systems, the progress stipulates cost-effective and highly efficient radio frequency (RF) and linearity circuit designs, which can handle weak signals. To ameliorate the signal-to-noise ratio and improve the quality of weak signals, high-power and low-noise amplifiers are the two main contenders. However, due to the higher-order harmonics in the non-linear circuits, loss of information may occur because of the cross-modulation [1–3].

For linearity and RF applications, intermodulation distortion and device linearity demand proper attention. The most critical issue in wireless application devices is power dissipation. One of the ways to

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control power dissipation is the scaling down of supply voltage and the other way is to design transistors, which have a low subthreshold slope (SS). On downscaling the threshold voltage, the off current increases dramatically, which is theoretically related to the fact that the SS of metal oxide semiconductor field effect transistor (MOSFET) cannot be lower than 60 mV/decade [4, 5]. The MOSFET suffers from many other serious issues like static power dissipation, high leakage current, and short channel effects [6]. The Tunnel Field Effect Transistors (TFETs) are considered as a potential candidate to deal with issues related to MOSFETs due to the fundamental technique of current switching, which makes a TFET more efficient than MOSFET. A MOSFET works on the mechanism of the thermionic emission of carriers over the potential barrier, while TFET inhibits the quantum band-to-band tunneling of carriers through the barrier [7]. Therefore, a TFET proves to be the better alternative to MOSFET, attaining lower SS and low OFF current; however, lower ON current is still an issue with TFET. To resolve the aforementioned issue, a new more promising architecture named junctionless TFET (JLTFET) has been explored in previous research, which unites the benefits of a junctionless FET (higher ON current) and a TFET (steeper SS) [8, 9]. Moreover, JLTFET also enhances the immunity toward the short channel effects due to non-existence of p–n doping junctions [10, 11].

The primary mechanism of JLTFET is the charge plasma method to convert a highly doped $n^+ - n^+ - n^+$ substrate into the conventional $p^+ - i - n^+$ substrate by using two gates (polar gate and control gate) with different work functions over the source and channel region and thus reducing the fabrication complexity, scalability issues, and random doping fluctuations [11–13]. Another factor responsible for low ON current in conventional TFET is the semiconducting material. The silicon (Si) is an indirect semiconducting material with large energy bandgap, which degrades the carrier mobility and band-to-band tunneling probability. Thus, the Si-based homojunction TFET attains a lower ON current [14–16]. Many researchers have recently explored the III–V compound semiconducting materials-based heterostructure TFETs by using a lower energy gap material than Si in the source region to increase the tunneling of carriers across the junction [12, 13, 17, 18].

Against this backdrop, this work focuses on the linearity performance assessment of our proposed device, dual metal gate-hetero-material-junctionless TFET (DMG-HJLTFET), having dual metal gate engineering (DMG) applied on a junctionless TFET. We used a novel combination of III–V compound semiconducting materials Indium Arsenide (InAs)/Gallium Arsenide (GaAs) to incorporate the hetero-material bandgap engineering benefits along with junctionless configuration; this is facilitated by the direct bandgap nature and very high electron and hole mobility of InAs/GaAs at the tunneling interface. The InAs [17] with a lower work function than Si is used as the source region material and GaAs [19] with greater work function than Si is employed as the channel and drain material. The material properties of InAs and GaAs employed in our simulation framework are displayed in Table 1. Before applying the DMG, we proposed single metal gate-hetero-material-junctionless TFET (SMG-HJLTFET) device using the same materials and dimensions. We then added the DMG to study the effect of dual metal work functions on the device linearity metrics. The control gate (CG) is divided into a tunnel gate (TG) and a supplementary gate (SG) with the work function of TG being smaller than SG. In this device, TG is located near the source/channel (S/C) interface and SG is located near the channel/drain (C/D) interface. A polar gate (PG) with fixed work function is used over the source region to induce the p-type polarity. The linearity and distortion characteristics of DMG-HJLTFET are also compared with the SMG-HJLTFET and the conventional Si-JLTFET (homo-material).

Table 1 Material properties of InAs and GaAs used in our simulation [22, 24]

Material parameters	InAs	GaAs
Relative permittivity	14.6	13.2
Energy bandgap (eV)	0.35	1.42
Electron mobility (cm^2/Vs)	$\leq 4 \times 10^4$	1200
Hole mobility (cm^2/Vs)	$\leq 5 \times 10^2$	61
Electron affinity (eV)	4.9	4.07

2 Device structure

Figure 1a, b show the schematic cross-sectional view of the simulation structure of DMG-HJLTFET and SMG-HJLTFET, respectively. First, we designed the Si-JLTFET (conventional), which has the same design and channel material parameters (bandgap, lattice constant, and electron affinity) as in [20]. We then incorporated the novel amalgamation of III–V compound semiconducting hetero-materials (InAs/GaAs) and DMG to compare homo-material Si-JLTFET and hetero-material JLTFETs (SMG-HJLTFET and DMG-HJLTFET) for various result characteristics. We used a lateral n-type JLTFET with the same type of doping incorporated at the source, channel, and drain regions so that a junction is induced between two semiconductor materials at S/C interface, instead of formation of doping junctions as in regular TFET devices. Since the configuration is junctionless, the charge plasma concept is used to induce the relative carrier concentration in the source and channel regions with the help of PG and CG [13]. The doping of the body is kept uniform with concentration of $1 \times 10^{19}\text{cm}^{-3}$ and the thickness of the body (T_{BO}) is 3 nm. The length of the channel (L_{CG}) is 20 nm, while the source and the drain are kept at 15 nm length each and we kept the isolation (L_{ISO}) between PG and CG at 2 nm. The work function of PG is 5.93 eV, and the work function of CG is 4.5 eV. A high-k dielectric material Al_2O_3 with dielectric thickness (T_{OX}) of 2 nm is used. The work functions of TG (TG ($\phi_{TG} = 4.1$ eV)) and SG (SG ($\phi_{SG} = 4.5$ eV)) are chosen by tuning them for optimized linearity performance. The length of TG (L_{TG}) and SG (L_{SG}) is kept at 4 nm and 16 nm, respectively, so that the total CG length ($L_{CG} = L_{TG} + L_{SG}$) remains constant.

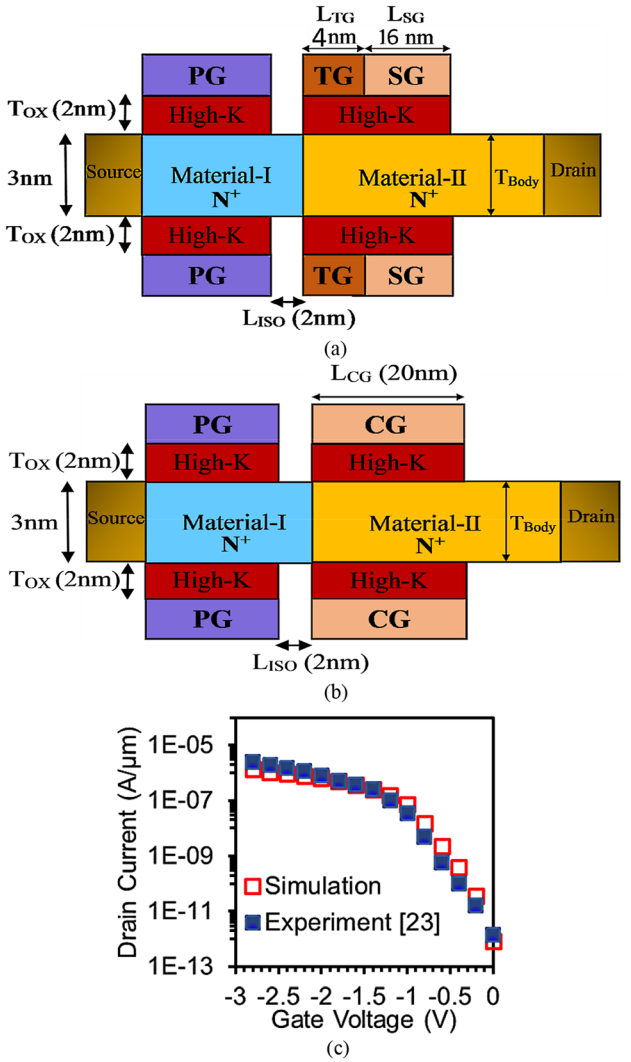

Fig. 1 Schematic structure of **a** Dual metal gate-heterojunctionless TFET (DMG-HJLTFET) and **b** Single metal gate-heterojunctionless TFET (SMG-HJLTFET). **c** Calibration of device with the published results

3 Model validation

3.1 Simulation methodology

To employ the effects of electron tunneling from valence band of the source to conduction band of the channel at S/C interface, the non-local band-to-band tunneling (BTBT) model is applied. We have also implemented the quantum tunneling meshing in the tunneling region to administer the generation rate and tunneling rate of carriers at each mesh node of the S/C interface. To include the effect of traps between the top of the valence band and the bottom of the conduction band, a trap-assisted tunneling model is applied. For simulation accuracy, the quantum confinement model given by Hansch [21] is also invoked. The bandgap narrowing model, the Shockley–Read–Hall recombination model, and the Auger recombination model are also enabled. The Fermi Dirac statistics is also invoked during the simulation. The CVT model (Lombardi) is also enabled to include concentration-dependent mobility and mobility due to parallel and perpendicular electric field and temperature. To perform all the mathematical carrier transport equations, we have employed the Gummel and Newton's numerical

method in our simulations. All the models are incorporated in the simulation setup using a TCAD simulator, Silvaco-ATLAS [22].

3.2 Calibration

As InAs/GaAs hetero-material combination has not been applied in TFET so far, we first calibrated the simulation models, specifically the most important non-local band-to-band tunneling model, with previously reported experimental work based on hetero-material SiGe, Ge, and Si for HS-TFET [23] by keeping all the device parameters and biasing conditions precisely as same as in [23] (Fig. 1c). We extracted the transfer characteristics of the experimental work reported in [23] and performed the simulation in Silvaco-ATLAS TCAD software; the two sets of results are depicted in Fig. 1c, which validate the model parameters due to a close proximity between the two set of results. After developing the calibrated simulation models, we executed them on our proposed device (SMG-HJLTFET and DMG-HJLTFET) by fine-tuning the hetero-material properties of InAs and GaAs (shown in Table 1) in the simulation models.

4 Results and discussion

Figure 2a illustrates the electrical transfer characteristics as a function of gate bias, ($V_{GS} = 1.5\text{V} \text{and} V_{DS} = 1.5\text{V}$) of our proposed device (DMG-HJLTFET) in comparison with SMG-HJLTFET and Si-JLTFET. The ON current of DMG-HJLTFET attains the highest value due to the utilization of InAs, which has the energy band gap of 0.34 eV as the source material and lower work function TG toward the S/C interface. The valence band of the source overlaps with the conduction band of the channel, which reduces the potential barrier width and hence larger electrons tunnel through the barrier ensues. It results in an exponential rise in the ON current so that DMG-HJLTFET achieves ON current 268% higher as compared to SMG-HJLTFET and 1164% higher than Si-JLTFET. The SS of three devices, DMG-HJLTFET, SMG-HJLTFET, and Si-JLTFET, is displayed in Fig. 2b, which shows a steeper SS value of DMG-HJLTFET than the Si-JLTFET due to the application of lower bandgap material toward the source and DMG. Figure 2c illustrates the comparison of ON current peak value for hetero-material tunnel FET having the CG work function equal to 4.1 eV and 4.5 eV for V_{GS} = 1.5 V and V_{DS} = 1.5 V. The results are also compared with DMG hetero-material tunnel FET which comprises of TG with work function of 4.1 eV and SG with work function of 4.5 eV.

Figure 2d, e also depict the contrast between set of results, expressed in the form of OFF current and current switching ratio (I_{ON}/I_{OFF}) for CG work function 4.1 eV and 4.5 eV, and DMG which has TG of 4.1 eV and SG of 4.5 eV. The CG with 4.1 eV work function appears to attain the highest ON current of 1.3×10^{-04} A/μm, while the CG with work function 4.5 eV attains the least ON current of 2.4×10^{-05} A/μm. When we set the CG work function to 4.1 eV, the leakage current of SMG design rises to 1.9×10^{-10} A/μm; in contrast, when the DMG design is invoked, the leakage current reduces to 2.9×10^{-16} A/μm. The DMG device (4.1 TG + 4.5 SG), appears to attain the maximum current switching ratio (3.1×10^{11}) which is 4.6×10^{5} higher than 4.1 CG SMG design and 2.2 orders higher than 4.5 CG SMG design. The reason behind the maximum current switching ratio and the lower leakage current flow in the DMG configuration is the application of a low work function TG toward the source and a high work function SG toward the drain. When we applied the gate bias of 1.5 V, the TG increases the electric field at the S/C intersection and decreases the tunneling barrier thickness and hence helps pulling down the conduction band. The valence band at the source overlaps with the conduction band at the channel. The electrons can tunnel very quickly through the junction thereby leading to higher ON current. At the no bias state, the broader energy gap material GaAs toward the channel side leads to higher tunneling barrier potential and reduction in tunneling of electrons diminishes so that low leakage current ensues.

It is critical to study the linearity parameters of a device to analyze its behavior in the high-frequency regime. The modern communication system must achieve minimum signal distortion and better linearity along with high speed. To improve the linearity of the system, there should be a uniformity of transconductance, g_m as a function of applied gate voltage. However, g_m of MOSFET and TFET is dependent on the applied gate voltage, signifying the non-linear properties of the two devices. Here, we examine the significance of using the III–V

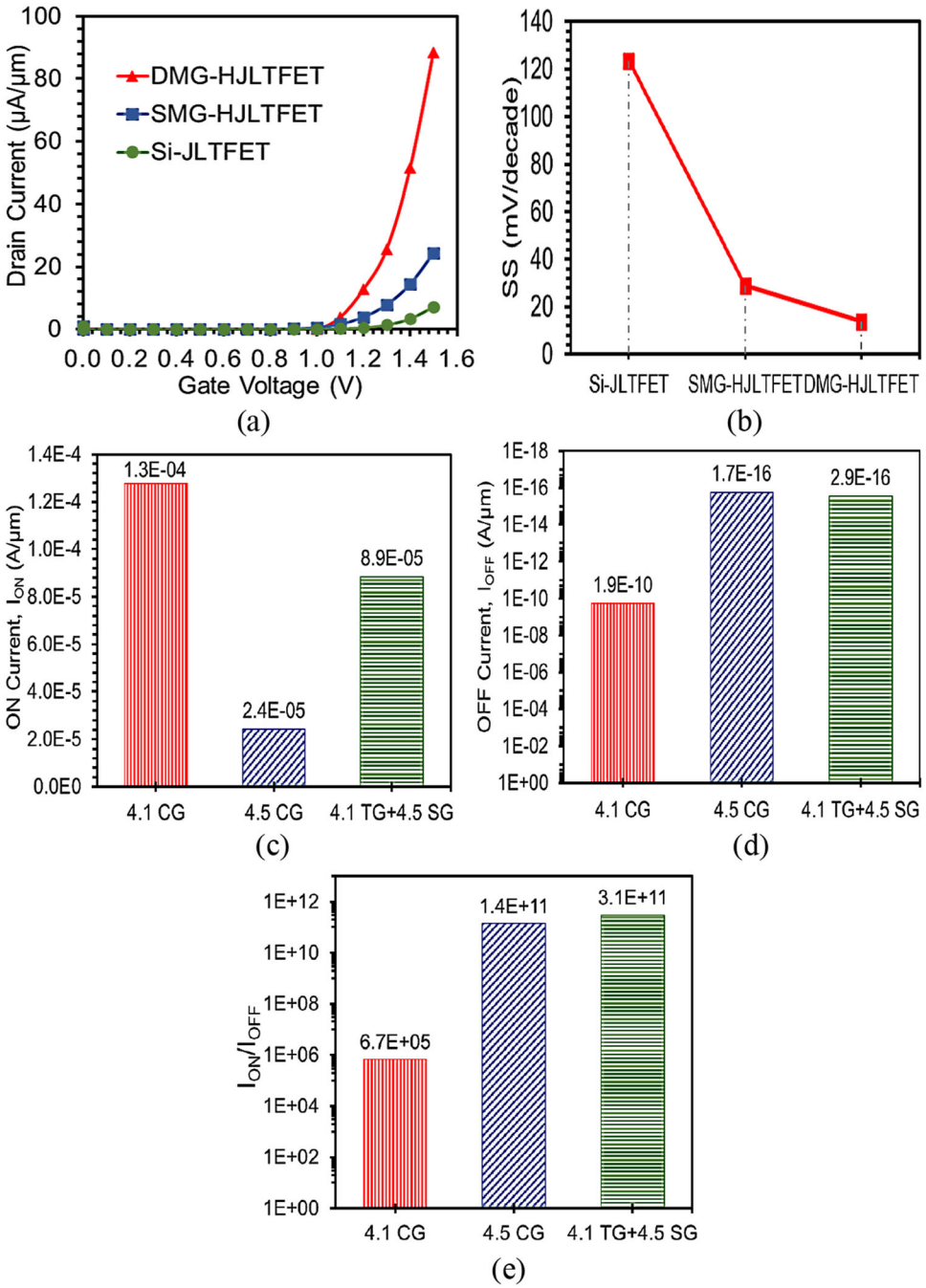

Fig. 2 **a** Transfer characteristics and **b** SS of DMG-HJLTFET, SMG-HJLTFET, and Si-JLTFET for $V_{GS} = 1.5V, V_{DS} = 1.5V$; peak value of **c** ON current, **d** OFF current, and **e** Current switching ratio (I_{ON}/I_{OFF}) for single metal gate configuration with 4.1 eV and 4.5 eV control gate work function and dual metal gate configuration consisting of 4.1 eV tunnel gate and 4.5 eV supplementary gate

compound semiconducting materials (InAs/GaAs) and DMG engineering on the linearity performance and intermodulation distortion in the form of VIP2, VIP3, IIP3, IMD3, 1-dB compression point, g_m, and g_{m3} as below:

$$g_{mn} = \frac{1}{n!}\frac{d^n I_{DS}}{dV_{GS}^n}, \quad \text{where } n = 1, 2, 3 \tag{1}$$

$$\text{VIP2} = 4 \times \frac{g_{m1}}{g_{m2}} \tag{2}$$

$$\text{VIP3} = \sqrt{24 \times \frac{g_{m1}}{g_{m3}}} \tag{3}$$

$$\text{IIP3} = \frac{2}{3} \times \frac{g_{m1}}{g_{m3} \times R_S} \tag{4}$$

$$\mathrm{IMD3} = R_S[4.5 \times (\mathrm{VIP3})^3 \times g_{m3}]^2 \quad (5)$$

$$1-\mathrm{dB} = 0.22\sqrt{\frac{g_{m1}}{g_{m2}}} \quad (6)$$

In Eq. (4), $R_S = 50$ is imputed owing to its practical applications in RF systems. The VIP2 is extrapolated input voltage at which first- and second-order harmonic voltages are equal and the VIP3 is extrapolated input voltage at which first- and third-order harmonic voltages are equal [25]. For high linearity, VIP2 and VIP3 must be high. The third-order intercept input power (IIP3) is defined as extrapolated input power at which the first- and third-order harmonic powers are equal. The third-order intermodulation distortion power (IMD3) is defined as the third-order intermodulation distortion corresponding to extrapolated intermodulation power at which the first- and third-order intermodulation harmonic powers are equal [25]. In Eq. (3–5), the third-order transconductance coefficient g_{m3} determines the lower limits on the distortion, and hence the amplitude of g_{m3} must be low for better linearity and low distortion applications. Equation (6) defines the 1 dB compression point which is the input power due to which the gain drops by 1 dB.

Figure 3a represents the comparison between g_m of DMG-HJLTFET, SMG-HJLTFET, and Si-JLTFET as a function of gate voltage $V_{GS} = 1.5$V. The transconductance (g_m) is an important parameter for wireless device applications, which provides the gain of the device as a function of V_{GS} and its value must be high to achieve high frequency and linearity characteristics of the device. In Fig. 3a, we found that the g_m of DMG-HJLTFET is approximately 274% higher than SMG-HJLTFET and 902% higher than Si-JLTFET with Si-JLTFET having the lowest value of g_m among the three devices. Due to the DMG configuration employed in the DMG-HJLTFET, TG comprising of the lower work function metal gives rise to the tunneling of charge carriers at the S/C intersection. It improves the current driving capability of the device, and hence the g_m increases, which also helps to decide the optimum gate bias for the device mechanism. For wireless applications, the third-order transconductance parameter is more dominant than the second-order transconductance because it leads to non-linearity due to the frequency interference and is responsible for output signal distortions. Figure 3b illustrates the variation of g_{m3} with V_{GS}. Among the three devices, DMG-HJLTFET has the lowest g_{m3} at $V_{GS} = 1.5$V and its amplitude is 9 times lower than SMG-HJLTFET and 20.6 times lower than Si-JLTFET. However, above a certain gate bias, there is a considerable variation in g_{m3} with gate voltage for DMG-HJLTFET in comparison with other devices. The large variation of g_{m3} with gate voltage in DMG-HJLTFET represents the non-linear behavior of g_{m3} due to the harmonic distortion. The increment in gate voltage beyond a certain point gives rise to harmonic distortion generated by g_{m3}, which results in reduced

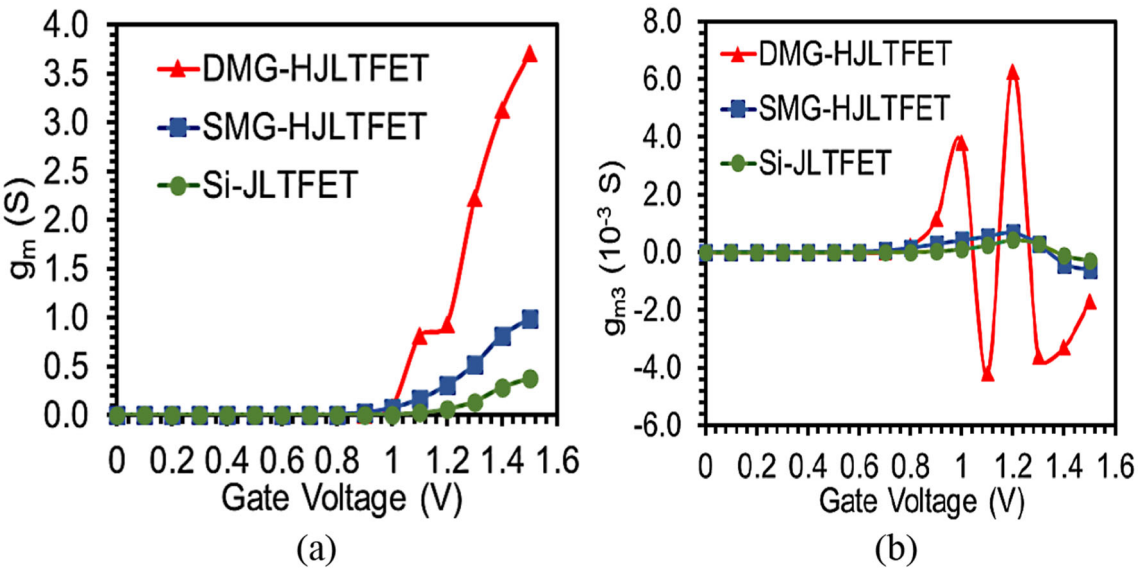

Fig. 3 **a** g_m and **b** g_{m3} of DMG-HJLTFET, SMG-HJLTFET, and Si-JLTFET

gate control over the channel; this, however, can be avoided by setting the gate bias close to g_{m3} zero-crossover point (mentioned in Fig. 7c). Because of almost symmetrical variation of g_{m3} around the zero crossover point (Fig. 3b), the harmonic distortion generated from it can be nullified for a small signal [26].

In Fig. 4a, b, DMG-HJLTFET attains maximum peak value of VIP2 and VIP3 at very low V_{GS}, which signifies that in order to preserve high linearity, low driving voltage is required. Si-JLTFET has the lowest value of the VIP3 peak among three devices. The DMG and the lower bandgap compound semiconducting material in the source and higher bandgap material in the channel and drain in our proposed device fosters higher current driving proficiency and hence leads to higher VIP2 and VIP3 peak values toward the lower gate voltage side. DMG-HJLTFET attains 220 times higher value of VIP2 than SMG-HJLTFET and 276 times higher value than Si-JLTFET and it also achieves 19.3 times higher value of VIP3 than SMG-HJLTFET and 21.9 times higher value than Si-JLTFET. Figure 5a, b signifies the disparity of VIP2 and VIP3 as a function of gate voltage for TG work function variation. The maximum peak value of VIP2 and VIP3 gets shifted toward the lower gate voltage for DMG configuration by using TG of 4.1 eV work function toward the source region, whereas when the TG work function increases to 4.3 eV, the peak values of VIP2 and VIP3 decrease. The 4.5 eV TG work function attains the lowest VIP2 and VIP3, shifting the peaks toward the higher gate voltage.

Figure 6a illustrates the IIP3 peak value of DMG-HJLTFET, SMG-HJLTFET, and Si-JLTFET at $V_{GS} = 0.6$V. IIP3 of DMG-HJLTFET is 158.4% higher than SMG-HJLTFET and 154.7% higher than Si-JLTFET. Si-JLTFET has the lowest value (− 17.33 dBm) among the three devices, which indicates the potential of DMG-HJLTFET for high linearity applications. The difference between the IIP3 peak values of DMG-HJLTFET and SMG-HJLTFET is the consequence of DMG design, as discussed before. It aids in attaining the maximum peak value of IIP3 at lower gate voltage, indicating its higher linearity attributes at low gate bias. We observe the same in Fig. 6b, where the disparity of IIP3 as a function of gate voltage is shown by varying the TG work function. On applying lower work function TG of 4.1 eV toward the source and higher work function SG of 4.5 eV toward the drain, the maximum peak value of IIP3 can be achieved at just 0.6 V gate bias. For better linearity and distortion-free operations, IIP3 needs to be high and IMD3 needs to be low. IIP3 shows approximately similar variation for TG work function 4.1 eV and 4.3 eV and when we increase the work function to 4.5 eV, the peak value is attained at 1.3 V gate voltage, which is not favorable when compared with lower work function values. It implies that the optimized value of the TG work function is 4.1 eV.

Figure 6c illustrates the disparity of IMD3 for DMG-HJLTFET, SMG-HJLTFET, and Si-JLTFET as a function of gate bias. DMG-HJLTFET exhibits the lowest value of IMD3 as − 212.9 dBm, whereas SMG-HJLTFET attains 1.24 dBm and Si-JLTFET attains 10.4

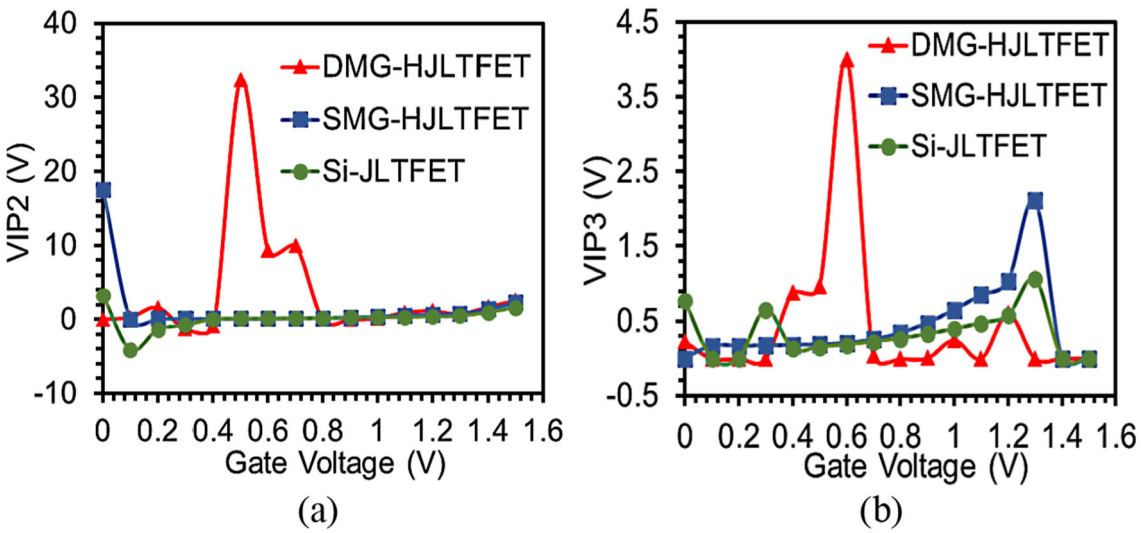

Fig. 4 Disparity of **a** VIP2 and **b** VIP3 as a function of gate voltage for DMG-HJLTFET, SMG-HJLTFET, and Si-JLTFET

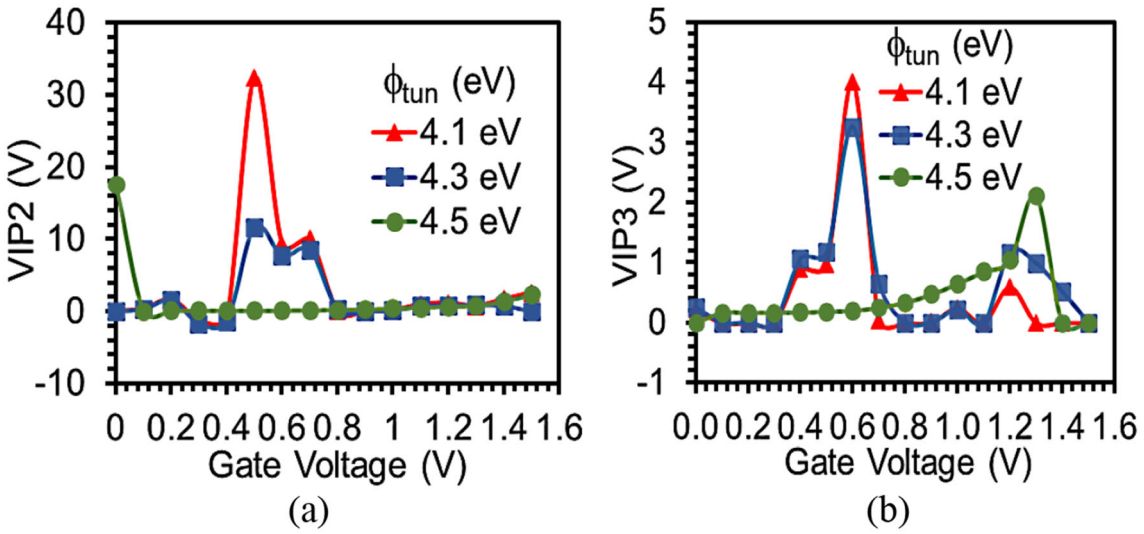

Fig. 5 Plot of **a** VIP2 and **b** VIP3 as a function of gate voltage for TG work function variation

dBm with IMD3 of DMG-HJLTFET being 171.8 orders lower than SMG-HJLTFET and 20.5 orders lower than Si-JLTFET, which is essential for a distortionless communication system. Figure 6d clarifies that the hetero-material JLTFET with 4.1 eV TG work function exhibits lowest value of IMD3 as compared to 4.3 eV and 4.5 eV TG work function. The 4.1 eV TG work function gives IMD3 approximately 16.4% lower than 4.3 eV TG and 225.8% lower than 4.5 eV TG work function. Thus, the optimized TG work function value of 4.1 eV reduces the amplitude distortion at low gate bias.

In Fig. 7a, 1-dB value is improved in the case of DMG-HJLTFET than SMG-HJLTFET and Si-JLTFET, due to the reduced signal distortion and higher value of g_m. At lower gate voltage (0.6 V), DMG-HJLTFET exhibits the maximum (25.25 dBm) value of 1 dB compression point, whereas SMG-HJLTFET exhibits 16.38 dBm as the maximum 1 dB compression point value. Si-JLTFET has the least 1 dB compression point value. Out of three devices, DMG-HJLTFET shows 54% improved value of 1 dB compression point than SMG-HJLTFET and 57% higher than Si-JLTFET. Figure 7b demonstrates the disparity of 1 dB compression point with gate voltage of 1.5 V for TG work function variation of 4.1 eV, 4.3 eV, and 4.5 eV. If we apply the 4.1 eV TG work function, (DMG), the maximum peak value of 1 dB compression point shifts toward the lower gate voltage and becomes 8.5% higher than 4.3 eV TG and 75% higher than 4.5 eV TG work function. The maximum value of 1 dB compression point is still observed at higher gate bias on changing of TG work function to 4.5 eV. Thus, the optimized value of TG work function is 4.1 eV. Figure 7c depicts the disparity of zero-crossover point for DMG-HJLTFET, SMG-HJLTFET, and Si-JLTFET. The choice of optimum gate bias point can help in suppressing the non-linearity in terms of g_{m3}, which can be determined through the zero-crossover point of g_{m3}. It is observed from Fig. 7c that in DMG-HJLTFET, the zero-crossover point gets shifted toward lower gate bias as compared to SMG-HJTFET and Si-JLTFET, due to the application of DMG. Table 2 displays the comparison of result characteristics of our proposed device with previously published hetero-material-junctionless structures based on different materials in the literature, where our proposed device appears to have promising result characteristics in terms of I_{ON}, SS, and g_m. Moreover, the bandgap and DMG engineering incorporated in DMG-HJLTFET leads to improved intermodulation distortion figure of merits (FOMs) such as VIP2, VIP3, IIP3, IMD3, and 1 dB compression point, making the transistor-level linearization more efficient and less time consuming than the expensive experimental efforts and optimization through device fabrication. These improved parameters maintain the linearity of the wireless communication systems even when receiving a weak signal, making the device highly suitable for wireless applications such as low-noise amplifiers (LNA) for cellular transceivers, space communications, and radio astronomy [27]. Moreover, the other improved performance parameters

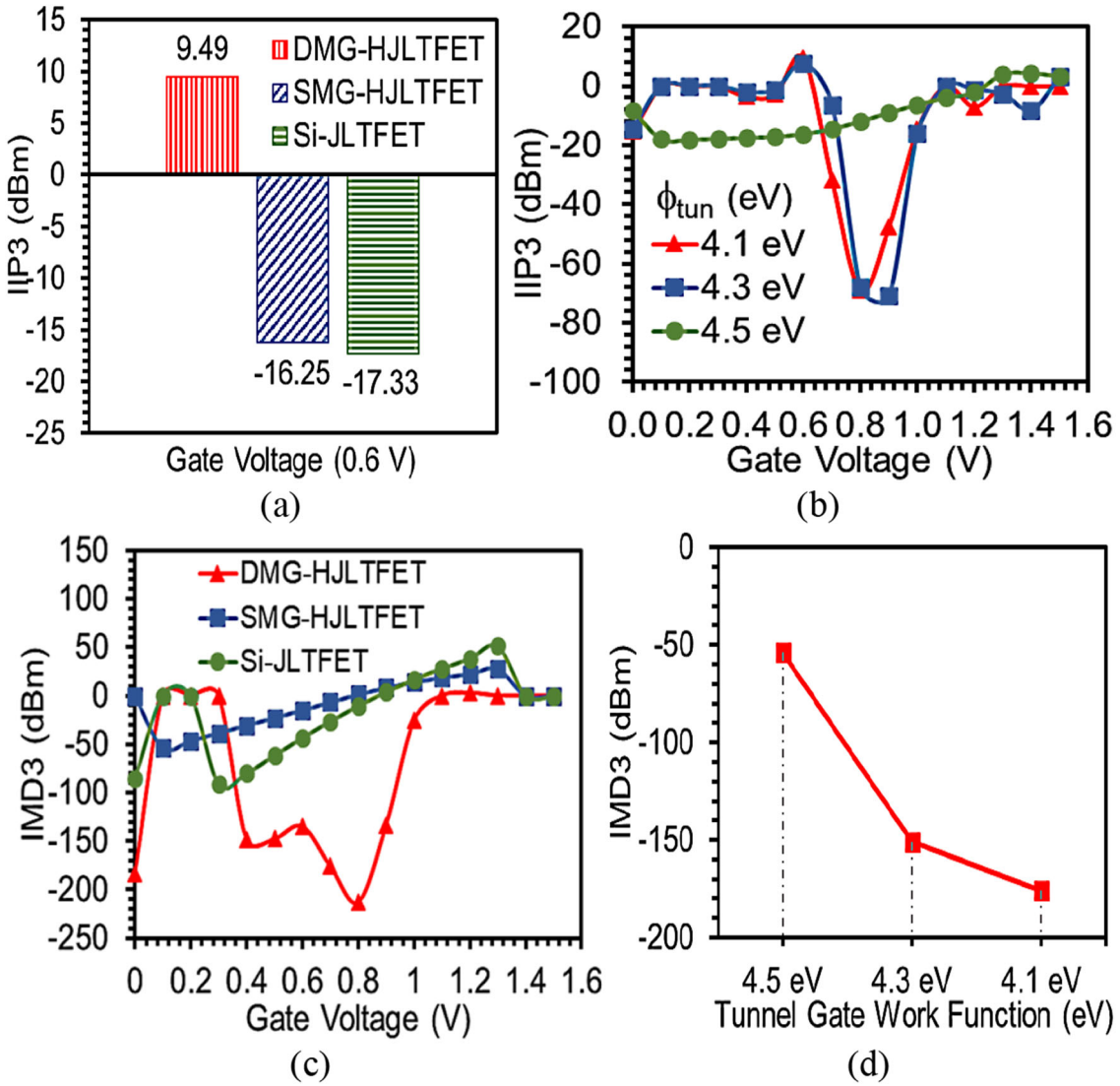

Fig. 6 Disparity of **a** IIP3 and **c** IMD3 as a function of gate bias for DMG-HJLTFET, SMG-HJLTFET, and Si-JLTFET. Disparity of **b** IIP3 and **d** IMD3 as a function of gate bias TG work function variation

such as I_{ON}, I_{ON}/I_{OFF}, I_{OFF}, steeper SS, and g_m of DMG-HJLTFET as compared to its counter devices make it desirable for fast switching performance and analog applications.

5 Conclusion

In this paper, we explored the potential of our recommended device in terms of linearity performance metrics and intermodulation distortion parameters by applying the bandgap engineering using the novel combination of compound semiconducting materials InAs/GaAs. The dual material gate engineering utilized in our proposed device improves the ON current up to 8.9×10^{-05} A/μm, which is 3.7 times higher than SMG-HJLTFET and 12.7 times higher than Si-JLTFET, whereas the current switching ratio rises to 2.2 times higher than SMG-HJLTFET and 1.7×10^5 times higher than Si-JLTFET. The implementation of lower work function TG toward the source region enhances the carrier passage efficiency and transconductance, thereby leading to more significant outcomes in terms of VIP2, VIP3, and IIP3 linearity metrics of DMG-HJLTFET in comparison to SMG-HJLTFET and Si-JLTFET. The transfer characteristics get modified because of the band overlapping at the S/C interface, which reduces the

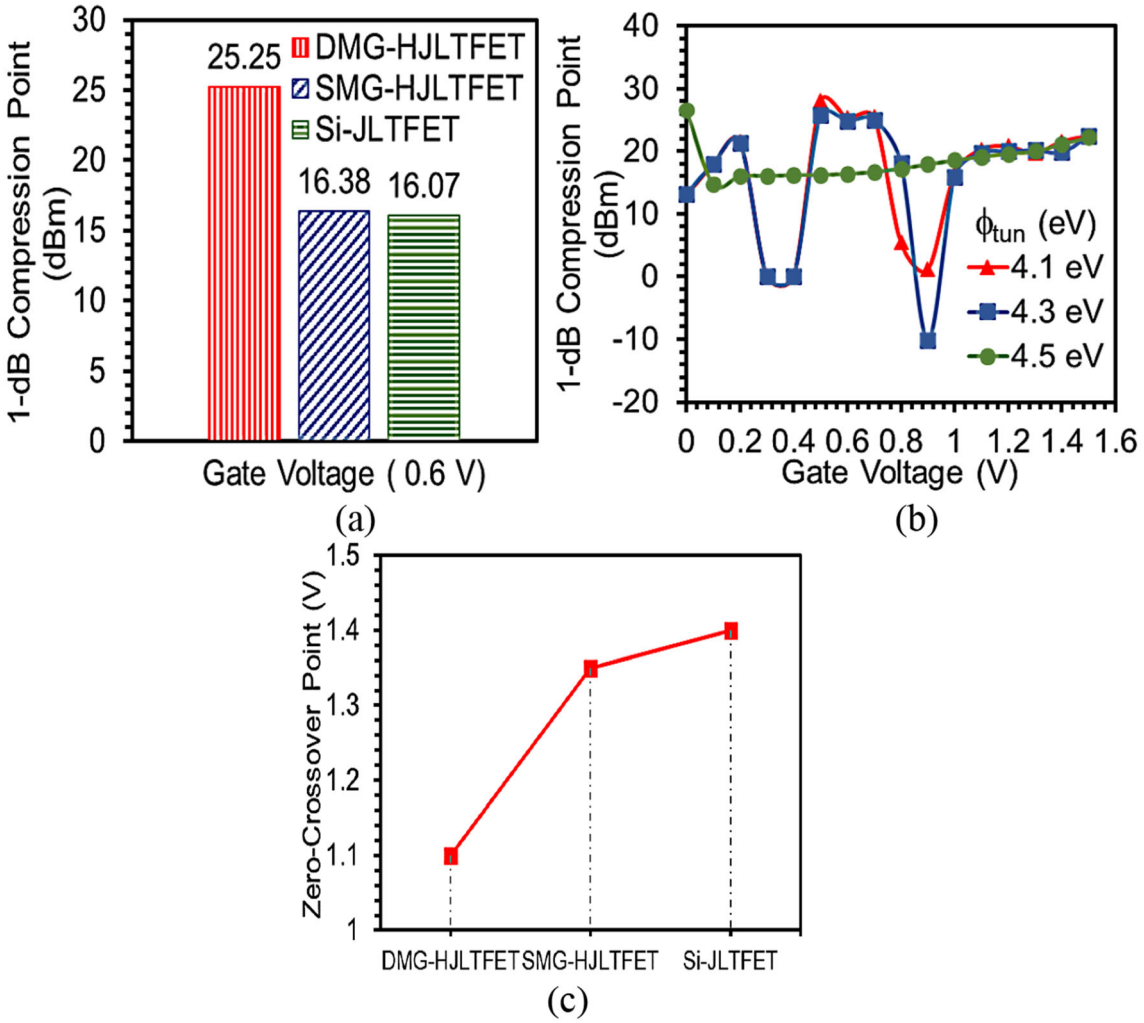

Fig. 7 Plot of 1-dB compression point as a function of gate bias for **a** DMG-HJLTFET, SMG-HJLTFET, and Si-JLTFET and **b** TG work function variation. **c** Variation of zero-crossover point with gate bias for DMG-HJLTFET, SMG-HJLTFET, and Si-JLTFET

Table 2 Comparison of this work with previously published devices

	DMMG-HJLTFET [28]	HJLTFET [20]	DMG-HJLTFET [12]	DMG-HJLTFET (this work)
I_{ON} (A/μm)	10×10^{-6}	6×10^{-6}	10×10^{-4}	88.5×10^{-6}
I_{OFF} (A/μm)	6.5×10^{-19}	1.72×10^{-18}	7.8×10^{-14}	2.89×10^{-16}
I_{ON}/I_{OFF}	1.5×10^{13}	2.3×10^{12}	1.2×10^{10}	3.1×10^{11}
SS (mV/decade	52	> 60	29	13.8
g_m (S)	1.2×10^{-5}	5.5×10^{-6}	2.8×10^{-4}	3.7×10^{-4}

tunneling barrier width and leads to the superior zero-crossover point and 1 dB compression point. The DMG-HJLTFET is found to have better g_m, g_{m3}, VIP2, VIP3, IIP3, IMD3, and 1 dB compression point in comparison with SMG-HJLTFET and Si-JLTFET. The 1 dB compression point of DMG-HJLTFET is 55% superior to SMG-HJLTFET and 57% superior to Si-JLTFET. Therefore, DMG-HJLTFET promises superior performance than SMG-HJLTFET and Si-JLTFET and can be considered an alternative in the modern wireless and distortionless communication systems.

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Compliance with ethical standards

Conflict of interest The authors have no relevant financial or non-financial interests to disclose.

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Performance Analysis of a Novel Hetero-material InAs/GaAs Junctionless TFET

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***Abstract*—In this work, we proposed and investigated the performance features of a hetero-material junctionless tunnel field-effect transistor (HM-JLTFET) by incorporating□□-compound semiconducting materials, InAs having low work function, in the source section and GaAs having higher work function, in the channel and drain sections, respectively. The transfer characteristics, subthreshold slope, leakage current, and current switching ratio of the proposed device are also compared with the conventional TFET device having the same dimensions as that of HM-JLTFET. The simulated results reflect the capability of the proposed device to suppress the performance degradation factors like leakage current and power consumption along with improving the current driving capability and fast switching at low gate voltage.**

Keywords—Hetero-material, Junctionless, TFET, Band-gap, Indium arsenide, Polar gate.

I. INTRODUCTION

Due to the thermionic emission as the fundamental mechanism of MOSFET, the performance of MOSFET degrades comprising of subthreshold slope value larger than 60 mV/decade and high leakage current. Many other conventional devices like CMOS (the combination of nMOS and pMOS), High Electron Mobility Transistor (HEMT), Negative capacitance FET, and Heterojunction Bipolar Transistor (HBT) appear to be promising in one form of challenges while degrades in other technological challenges. The nonstop scaling down of CMOS technology in the past few years has led to many operational enhancements in terms of high speed and packing density; however, it becomes very challenging to fabricate ultra-shallow junctions at such small dimensions [1]-[3]. Various techniques like ion implantation and annealing are required in order to fabricate ultra-shallow junctions with heavy doping, which, however, suffers from random dopant fluctuations [4]-[5].

Along with such issues, the downscaling of MOSFET lead to static power dissipations and high leakage current [6]-[7]. TFETs are the devices, which overcome the issues of higher leakage current and fast switching along with lower subthreshold slope. The underlying mechanism of TFET device is the band to band quantum excavation of electrons through the barrier, which results into high ON current and high I_{ON}/I_{OFF} current switching ratio [8]. In the past few decades, many research papers have highlighted the importance of TFET; however, low ON-current and fabrication of metallurgical junctions has been a complicated task. In order to meet the requirements of modern technology, junctionless TFETs have come into the picture [3]. Junctionless TFETs integrate the advantages of junctionless FETs and TFETs. Junctionless FET shows high ON current and has less variability as compared to MOSFETs as it does not require any metallurgical junction. TFETs show steeper SS, however, suffer from low ON-current [3], [9]. JLTFET works on the principle of inducing source and drain regions through charge plasma [3]. This paper includes the amalgamation of the concept of JLFET and TFET along with ˜ -˜ compound semiconducting materials, where, InAs is used in the source section and GaAs in the channel and drain sections, respectively.

II. DEVICE ARCHITECTURE AND SIMULATION SETUP

Fig. 1(a) illustrates the pictorial outlook of our proposed device double gate hetero-materials junctionless TFET (HM-JLTFET). The configuration of the device is a lateral n-type junctionless TFET consisting of a uniformly doped substrate with concentration of 1×10^{19} cm^{-3}. Our device is based on charge plasma concept using two isolated gates as the Polar gate and Control gate, where the Control gate has lower work function than Polar gate. The primary purpose of these isolated gates is to convert a highly doped $n^+ - n^+ - n^+$ substrate into the conventional $p^+ - i - n^+$structure. The device structure parameters are mentioned in Table I. The work functions of the control gate and polar gate are 4.5 eV and 5.93 eV, respectively.

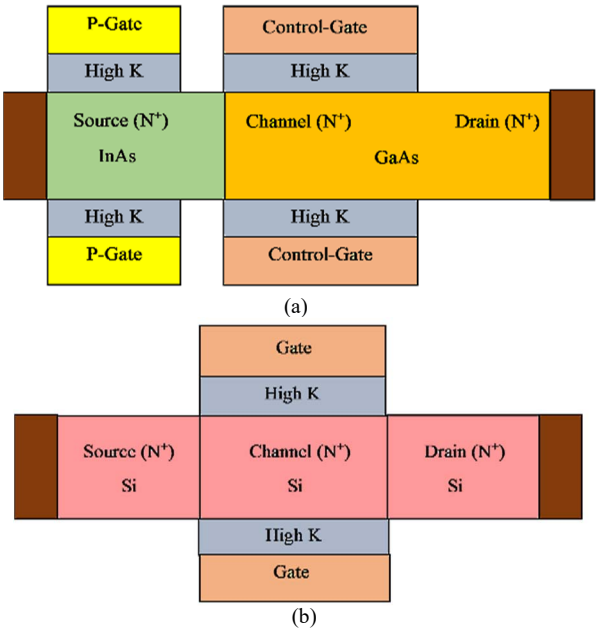

Fig. 1. Pictorial outlook of (a) Hetero-material junctionless TFET (HM-JLTFET) and (b) Conventional TFET

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High Switching Performance of Novel Heterogeneous Gate Dielectric—Hetero-Material Based Junctionless-TFET

Samriti Sharma and Rishu Chaujar

1 Introduction

A conventional MOSFET faces a difficulty in attaining a low-thermal budget because of the necessity of complex fabrication and large doping-concentration gradient due to the existence of two source/channel and channel/drain junctions. Scaling down the MOSFET dimensions in accordance with the International Technology Roadmap for Semiconductors (ITRS) guidelines becomes very challenging due to the doping junctions present between the source/channel and channel/drain boundaries beyond 32-nm nodes technology [1]. In order to withstand the downscaling issues with time various novel structures have been evolved by the researchers. In past few years junctionless field-effect transistors (JLFET) have attracted the interest of many researchers due to the absence of doping junctions [2, 3]. Unlike MOSFET, the doping concentration of JLFET is the same all over the source, channel, and drain regions. Owing to the absence of concentration gradient in the lateral direction of the channel, this device is quite easier to fabricate along with improved electrical performance and better uniformity than MOSFET. The junctionless concept has been explored in many devices such as TFETs [4], FinFETs [5], Negative capacitance FETs [6], Nanowire FETs [7]. TFETs are the most promising candidates in present technology over MOSFETs owing to its steeper sub-threshold swing (<60 mV/decade) and lower leakage current, [8–10]. The Tunnel FETs work on the fundamental mechanism of band-to-band tunnelling [11, 12]. By applying the junctionless technology, the result characteristics of a TFET can be enhanced in the form of higher ON current, steeper sub-threshold swing along with fast current switching ratio [13]. Along with junctionless technology, the direct bandgap III-V compound semiconducting materials also aid to accomplish higher ON state current by incorporating lower bandgap and higher bandgap materials in the Source and channel region [14–16]. Further, enhancement

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