STATIC LOW-POWER VERIFICATION OF SYSTEM-ON-CHIP (SoC)

A DISSERTATION
SUBMITTED IN PARTIAL FULFILLMENT FOR THE AWARD
OF

MASTER OF TECHNOLOGY
IN
VLSI DESIGN AND EMBEDDED SYSTEMS

Submitted by

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I, Kumar Suryanshu 2K20/VLS/08, student of M.tech (VLSI Design and Embedded system), hereby declare that the Project Dissertation titled "**STATIC LOW-POWER VERIFICATION OF SYSTEM-ON-CHIP (SoC)**" which is submitted by me to the department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associate ship, fellowship or other similar title or recognition

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CERTIFICATE

I hereby certify that the dissertation titled "**STATIC LOW-POWER VERIFICATION OF SYSTEM-ON-CHIP (SoC)**" which is submitted by KUMAR SURYANSHU Roll No. 2K20/VLS/08 to the department of Electronics and Communication Engineering, Delhi Technological University, Delhi in the fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ABSTRACT

As technology nodes shrink to nanometers, the semiconductor sector is drastically scaling down. Processors are decreasing in size while increasing in performance and decreasing in delay. Power, performance, and area are the three primary considerations in the digital design of any processor or System-On-Chip. A good design is typically characterized by high performance and low power consumption, requiring less silicon area on the chip. All three criteria are interrelated, so if one improves, the other two will suffer as well. All throughout the world, scientists and engineers are attempting to improve all three elements simultaneously, which is pretty difficult.

Today's integrated frameworks require low power architecture. The low power architecture is also essential for battery-powered applications, such as mobile phones, portable computers, pocket calculators, wrist watches and PDAs. Therefore, the necessity for low-power design and verification is urgent. Power management has risen to prominence in recent years especially in lower node technologies as static power dissipation is greater compared to dynamic power. In nanoscale technology, power dissipation will increase as the technological node decreases and the performance speed, number of transistors, and leakage current rise.

Static power dissipation plays a vital role as the size of a technological node shrinks; therefore, this dissipation should be minimized in the design. Consequently, various Low power methods are presented in this report. Specialized power management cells that are UPF-compliant are also examined in depth.

In this project, low power checks of SoC have been verified. Verification and debugging of low power checks has been performed through Low power verification tool which generates log files and report files. These files give error and warning messages in our

design and help us to debug our design through graphical user interface mode to verify and eliminate errors. When Netlist, Unified Power format (UPF) and constraint files are given to a low power verification tool it generates log and report files. UPF is relatively a new concept which has been introduced in 2007, later it became IEEE 1801 Low Power Standards. While Netlist contains all information about functionality of design, UPF specify all power intent information in the design. This report comprises simulation results and reports of low power checks, which include all errors, warnings or violations, in order to comprehend all phases and procedures of static low power verification of SoC.

Keyword and phrases: Low Power Verification, Unified Power Format, System-On-Chip, Hardware Description Language, Power Management Unit, Power-Aware Design.

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LIST OF ABBREVIATIONS

UPF	Unified Power Format
IC	Integrated Circuit
GUI	Graphical User Interface
PG	Power/Ground
ELS	Enable Level Shifter
LS	Level Shifter
AON	Always-ON
PNR	Placement and Route
GUI	Graphical User Interface
RTL	Register Transfer Level
LEC	Logical Equivalence Checks
LVS	Layout versus Schematics
DRC	Design Rule Checks
HDL	Hardware Decription Language
TCL	Tool Command language
PMU	Power Management Unit
SCMR	Standard Cell Main Rail
STA	Static Timing Analysis

CHAPTER 1

INTRODUCTION

1.1 Prologue

In today's world, technology advances at a breakneck pace, and the technology node of semiconductor devices is shrinking every year. According to American industrialist Gordon Moore, the co-founder of Intel, the number of transistors on a computer chip doubles every 18 to 24 months, and the size of ICs is dropping as well. The compact size of an IC has several advantages, but as its power density rises, other difficulties arise. Not only does an integrated circuit with a high-power density heat the product, but it also becomes unstable quickly. Due to this issue, the IEEE 1801 low-power standards have been developed to make ICs more reliable, resilient, and standardized, which would alleviate these issues. Once an IC is built, it must be verified by ensuring that its functionality and behaviour are correct and that it adheres to the IEEE 1801 low power standard, commonly known as the UPF [1]. This IEEE standard includes design flow, analysis, and verification implementation flow, as well as portable, low-power specifications that can be used in electronic products [2, 3].

Huge demand for portability, and dependability drives the current consumer electronics business. In addition to faster time-to-market and product quality, additional functionality, performance, and bandwidth are crucial for optimizing sales of semiconductors [4]. The proliferation of applications, such as mobile phones, computers, laptops, PDAs and portable systems, has been accompanied by an exponential increase in battery-powered systems [3].

1.2 VLSI Design Flow

The semiconductor industry's chip manufacturing process necessitates a specific flow for proper chip operation and high yield [5]. Below is a diagram of the VLSI design flow, which practically every industry in the world uses to improve their semiconductor products. This is shown in below Fig. 1.1.

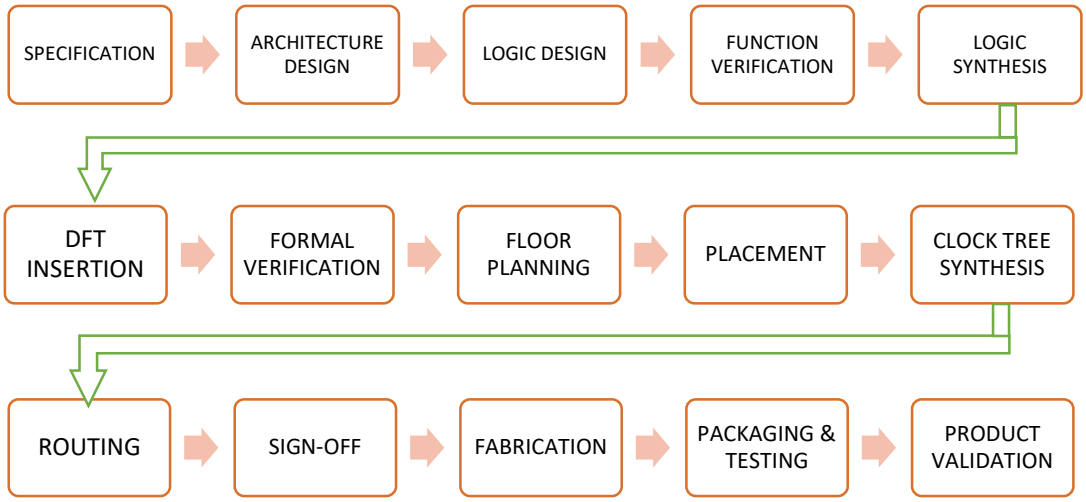

Fig. 1.1 VLSI Design Flow

As shown in Fig. 1.2, Sign-off in advanced desinging of SoC is vital stage as its result is given straightforwardly to semiconductor foundry for manufacturing [6]. Principally five checks are perfomed here. Logical Equivalence Checks (LEC) guarantees useful check among Netlist and RTL. In Layout versus Schematics (LVS) stage, extracted layout netlist from GDSII document is contrasted with netlist of a similar stage with LVS rule checker. Design Rule Checks (DRC) guarantee legitimate physical connectionn and reports infringement if any [7, 8]. In Post Layout STA all timing checks are performed again utilizing the genuine parasitic removed after the directing of plan. Power checks includs IR drop checks and low power checks. Emphasis will be given to low power checks [9].

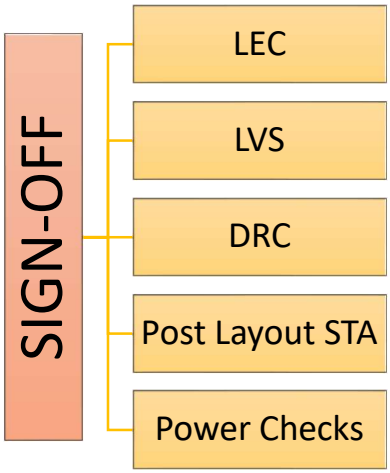

Fig 1.2 Sign-off stages

1.3 Types of Power consumption in CMOS based design

There are primarily two components of power dissipation in a CMOS circuit:

1. Dynamic power consumption 2. Static power consumption

1.3.1 Dynamic Power consumption

Internal power and switching power constitute dynamic power. It is the energy expended during state transition. External capacitor charging and discharging consumes switching power. It is proportional to both clock frequency and switching activity. Internal power is due to short circuit current that flows through Pull Up to Pull Down Logic, when both PMOS and NMOS are ON. Low threshold voltage and slow transition produce greater internal power usage [9, 10]. It is the power consumed when the device is operational and the signal values are changing. At a given output node it is given by:

$$P_{dynamic} = \alpha * C_L * V_{dd}^2 * f_{Clock} \quad (1.1)$$

where, α = node transition activity factor, C_L = total output load capacitance,

V_{dd} = supply voltage and f_{Clock} = clock frequency

1.3.2 Static Power consumption

As a result of leakage current, CMOS devices have a low static power consumption. This power consumption occurs when all inputs are held at a valid logic level and the circuit is not in charging states. At higher technology nodes, CMOS devices have low static power consumption, however at lower technology nodes, such as below 90nm, static power consumption is rather significant. A little amount of current still seeps through gate of MOSFET even when it is OFF, and this heat is dissipated. CMOS chip designs feature smaller leakage currents than far earlier bipolar designs, although scaling has made it more difficult to keep leakage current at a reasonable level. This is because when technology nodes shrink, leakage current rises. Leakage currents constitute the majority of dissipated static power. [11].

$$P_{static} = V_{cc} * I_{cc} \quad (1.2)$$

Where, V_{cc} = supply voltage, I_{cc} = device current (sum of leakage current)

Total Power dissipation in a CMOS circuit is given by:

$$P_{total} = P_{dynamic} + P_{static} \quad (1.3)$$

1.4 Low Power Verification Checks Flow

Figure 1.3 depicts a low power check where the first step is to check RTL block using UPF consistency and signal corruption check, Synthesis design block can be checked using signal corruption, structural and functional check, and power/ground connected block can be checked using signal corruption, structural and functional check as well as PG check [3]. At RTL Block, low power verification aids in finding power intent issues in UPF early in the design life cycle, resulting in a UPF that is clean prior to initiating the design flow [12].

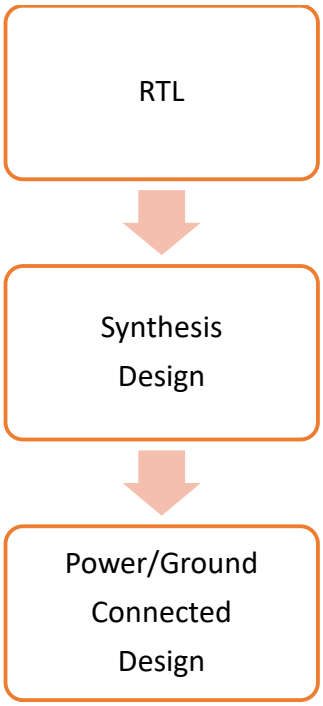

Fig. 1.3 Low power check flow

Low power verification requires RTL like Verilog, VHDL or SVD file , UPF file as well as the design's PG Netlist or post-layout netlist. Low power verification needs standard Liberty (Library) files (.db file). Low power verification reads the Liberty

DB file for timing information, annotating power connections, describing the design, and validating particular cells for the Gate level netlist.

It will require the power intent contained in UPF. Low power verification tool generates log files, error and warning reports for static rule violations defined in design. TCL is a common programming language for executing and debugging low power checks/violations. Low power verification tool also assists with GUI debugging as shown in Fig. 1.4 [13].

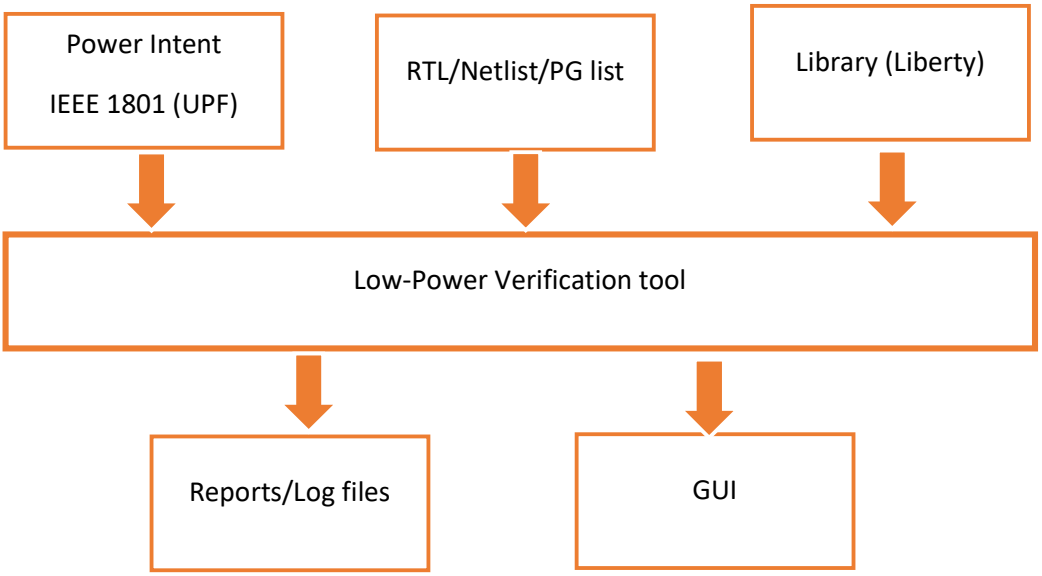

Fig. 1.4 Low power verification checks

UPF and Netlist are examined in accordance with fig. 1.3 and fig. 1.4 and following checks are performed on them:

1.4.1 Signal Corruption Checks

It detects power architecture violations at the gate-level netlist. This check will return an error if a signal is connected to a constant instead of a port or a net.

1.4.2 Power Intent Consistency Checks

Performs syntax and semantic tests on the UPF in order to approve its consistency before starting execution.

1.4.3 Structural Checks

Validates the inclusion and connection of cells used in low power design, including isolation cells, level shifters, power switches, always-on cells and retention registers, all across the implementation process.

1.4.4 Functional Checks

This checks and verifies the correct functionality of design along with different special power management cells.

1.4.5 Power and Ground (PG) Checks

Compares the PG to the UPF routing specification for power networks on physical netlists.

1.5 UPF Flow

UPF syntax and semantics are based on Tcl and can be combined with non-UPF Tcl commands. This file defines the design's power management architecture and is used to generate specific reports regarding the design's power intent. In UPF, standard commands are specified that tool understands and responds to accordingly. UPF flow can be seen in Fig. 1.5. It can be seen that for power intent design, UPF is integrated with RTL in design stage only [14]. Traditionally, only RTL was utilized for design implementation. However, due to the necessity for power-aware designs in recent years, UPF is being employed to implement designs. Synthesis, Placement & Route will happen in accordance with RTL along with UPF.

1.6 Low Power Techniques

Low power techniques are utilized to decrease the total power consumption of a system. By reducing capacitive load and activity factor, which in turn reduces the switching activity and thus reduces dynamic power consumption. There are numerous strategies to reduce static power consumption, some of which are described below. Some of low power techniques are:

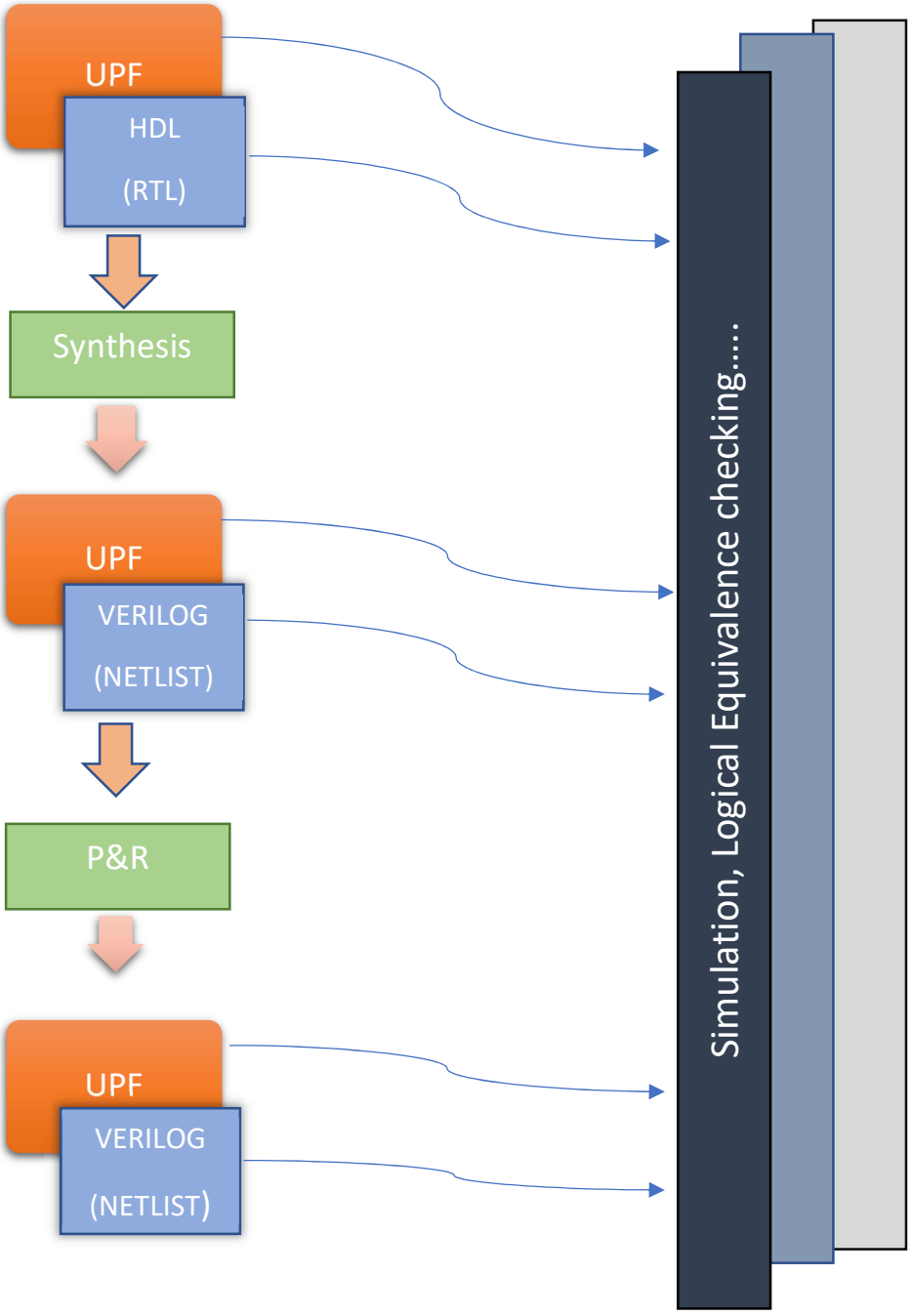

Fig. 1.5 UPF flow

1.6.1 Clock gating

It is utilized to decrease the dynamic power of the design. When the design clock is not required, it is easy to disable it without affecting the design's functionality [4]. By lowering the switching frequency, clock gating decreases the dynamic power dissipation of the circuit. Following Fig. 1.6 shows clock gating phenomenon:

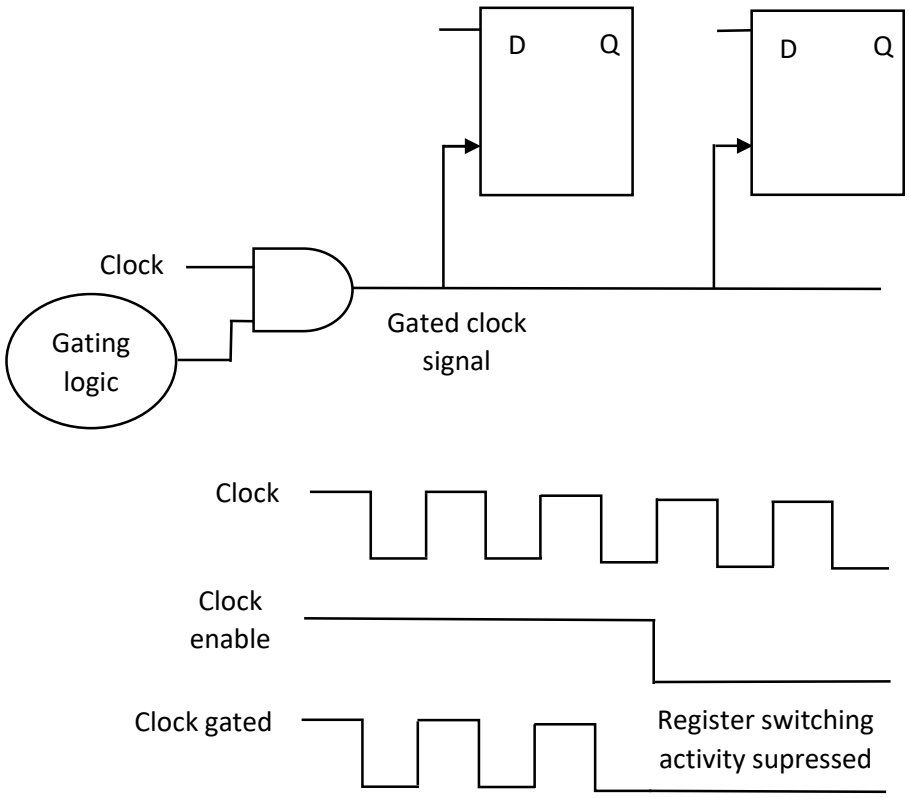

Fig. 1.6 Clock gating demonstration

1.6.2 Dynamic Voltage and Frequency Scaling

By adjusting the frequency and voltage, energy usage can be decreased . When a high working frequency is required, the supply voltage is increased to achieve it. For example, Graphics Processing unit on SoC operates at higher frequency than rest of processor so a higher voltage is required for this task. Similarly a lower voltage is required when a component of processor is working on lower frequency

1.6.3 Multi V_{dd}

By including multiple voltages into the design, both static and dynamic energy is conserved. The chip is fabricated using many supply voltages [15]. Various functional blocks operate at different voltages, and power loss can be reduced by lowering the supply voltage as shown in Fig. 1.7.

1.6.4 Multi Thresold Voltage(V_{th})

Using two or three kinds of cells, such as low V_{th}, High V_{th}, and Standard V_{th} cell, the multi threshold voltage techniques has become a standard method for minimizing leakage voltage .

Low V_{th} cell: It switches quickly, has a minimal clock interval, uses less dynamic power, and has a low delay

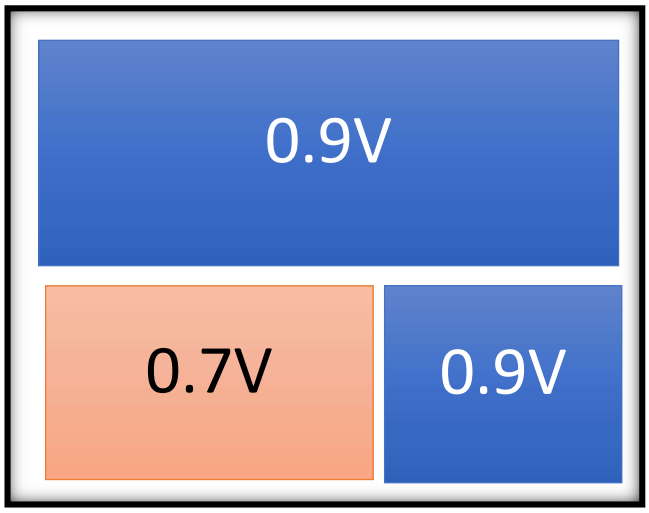

Fig 1.7 Multi V_{dd} design of SoC

High V_{th} cell: It generates less leakage power, greater dynamic power, and greater delay.

Standard V_{th} cell: It has a medium leakage current and delay.

1.6.5 Power gating

Power gating is used to minimize power usage by turning off the current in blocks that are not in use. This transitory closure time can likewise called as "low power mode" . Yet again when circuit blocks are expected for activity they are actuated to "active mode".Thus, it conserves overall chip power. Power Gating is successful for lessening leakage power.

1.7 Special Power Management Cells

Power management cells are specialized cells used to manage power distribution in a design using a UPF file. These strategies utilize power management cells, which are specialized cells. Power management commands specify the properties of instances of power management cells used to implement and validate the power intent of the design. These power management cells eliminate the Voltage error, the Voltage crossover, and the power domain error. Power management cells with two sets of rails are also known as Dual power rail Supply Cells. Dual power rail

provides both primary and secondary power rail to these cells. The PMU repeatedly controls power on and off. Using a power switch, it regulates the signal by toggling it according to the power domain. It helps to reduce current by shutting off the majority of unnecessary design components. Several cell types are described.

These cells are Isolation Cell, Level Shifter Cell, Retention Cell, Power Switch Cell, Always-On Cell, Enable Level Shifter and Bi-directional Level Shifter

1.7.1 Isolation Cell

Isolation cells often referred to as clamp cells. These are the unique cells utilized in low power designs as shown in Fig. 1.8. The synthesis tool inserts it to isolate the wires and buses passing from the power-gated domain to the always-on domain. Isolation cells are utilized to lower the design's power dissipation. The Power domain that is turned off will not drive any outputs, hence these outputs will act as floating nodes, which might cause issues for active power domains that receive floating node inputs [16]. It would result in a crowbar current that exceeds the specified limit, impairing the functionality of the power up domain. "AND" gate and "OR" gate are the types of clamp cells employed when isolation cells pass unknown signal “X”, resulting in power leakage. To pass a Signal “HIGH” or “1”, it requires an “OR” gate, and to pass a Signal “LOW” or “0”, it requires an “AND” gate as Isolation cell.

Consider a design with two power domains, PD_1 and PD_2, and the propagation of signal S1 from PD_1 to PD_2. When both power domains are powered on, the signal's value is either 0 or 1. However, when the power domain PD_1 is deactivated and PD_2 is activated. The value of S1 will be unknown. This corrupts the logic for powering up the PD_2 domain. To prevent this, design engineers put isolation cells between the outputs of the powered-down domain and the powered-up domain's input.

Normal operating conditions see the isolation cell functioning as a buffer. When PD_1 is shut down, the isolation cells restrict its output to either 0 or 1. The isolation cell features an isolation enable signal that specifies whether the isolation cell should function as a buffer or offer isolation.

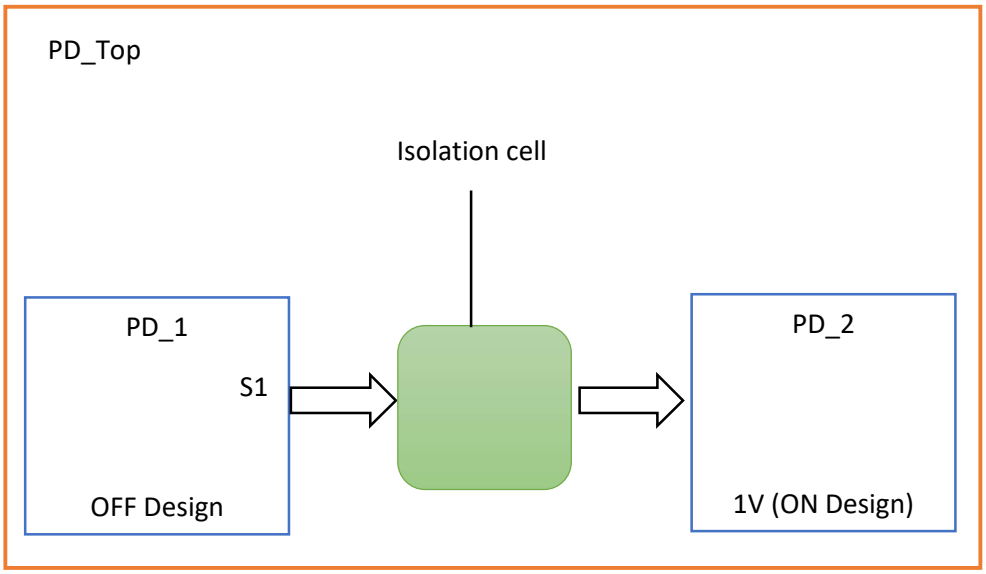

Fig. 1.8 Isolation cell Block diagram

Without an isolation cell, power will leak when the MOSFET gate receives an unknown signal (X). When to pass '0', the AND gate shown in fig. 1.9 is used, and when to pass '1', the OR gate shown in fig. 1.10 is used .

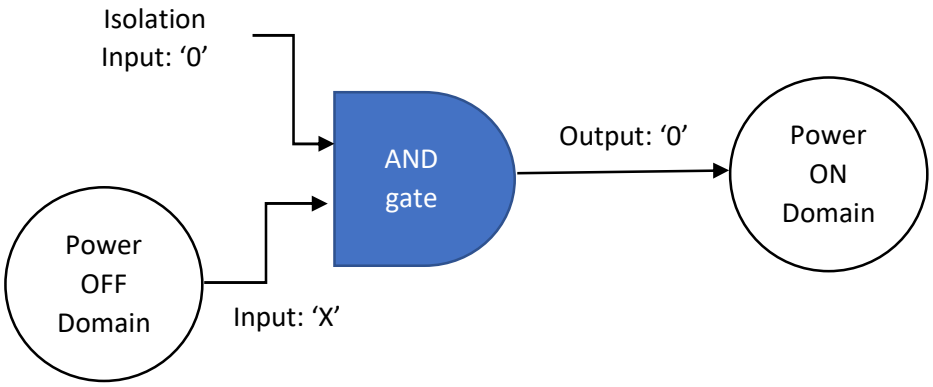

Fig. 1.9 Type 'LOW' signal transmission utilizing 'AND' gate as an isolation cell.

Table 1.1 Truth Table for isolation cell using AND GATE retaining or clamp '0'

Isolation Input	Input	Output
0	X	0
1	X	X
X	1	X
X	0	0

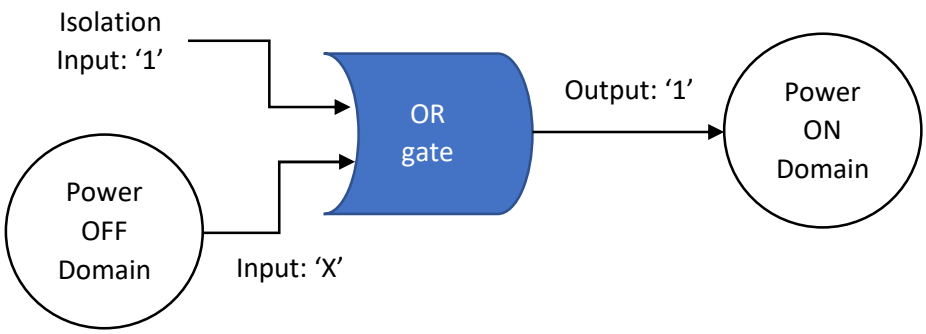

Fig. 1.10 Type 'HIGH' signal transmission utilizing 'OR' gate as an isolation cell.

Table 1.2 Truth Table for isolation cell using OR GATE retaining or clamp '1'

Isolation Input	Input	Output
0	X	X
1	X	1
X	1	1
X	0	X

1.7.2 Level Shifter Cell

The Level Shifter Cell transforms one voltage level into another. These are the standard cells utilized in multivoltage designs as hown in Fig. 1.11 and 1.12. The level shifter is added using the synthesis tool.

Level Shifters transform voltage to three different modes:

1. High to Low Level Shifter: It converts voltage from High to Low.
2. Low to High Level Shifter: It converts voltage from Low to High.
3. Bidirectional Level Shifter: It converts both from L to H and H to L.

Consider a design with two power domains, PD_3 and PD_4, and the propagation of signal S2 from PD_3 to PD_4. When both power Domains are powered and the voltage differential is smaller than the threshold value (which can be determined using a simulator), there are no design flaws. Nevertheless, if the voltage differential exceeds the threshold value a ssuming PD_4 operates at a greater voltage level than PD_3, it can be inferred that a logic 1 at PD_3 corresponds to a logic 0 at PD_4. This results in improper data transmission. To overcome this problem, the designer inserts level-shifting cells between the power domains [17].

These cells convert high voltage to low voltage and vice versa. This allows for the accurate transmission of data between two distinct power domains. The level shifter enable signal regulates whether or not the level shifter cell should transform the voltage level or function as a buffer.

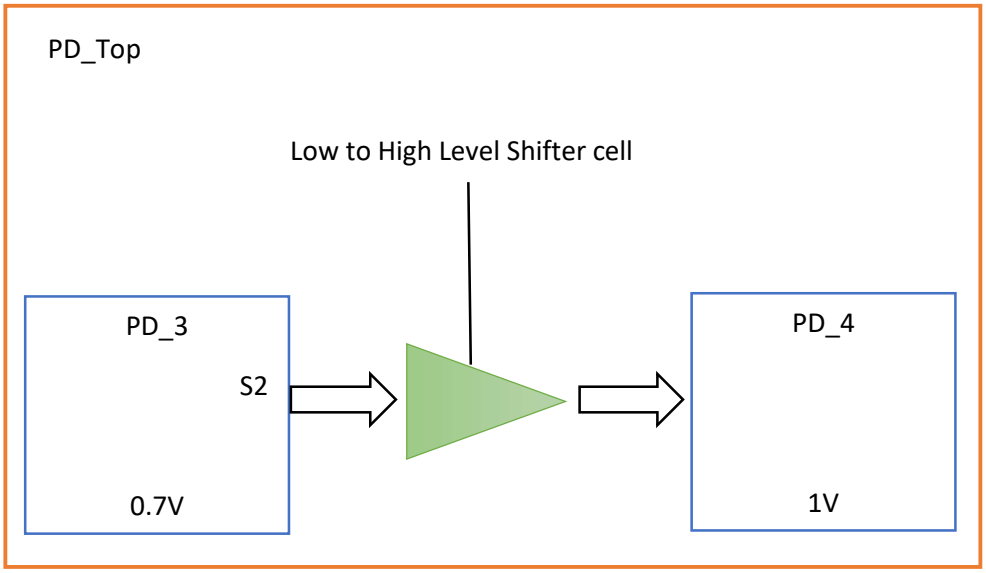

Fig. 1.11 LOW to HIGH level shifter cell

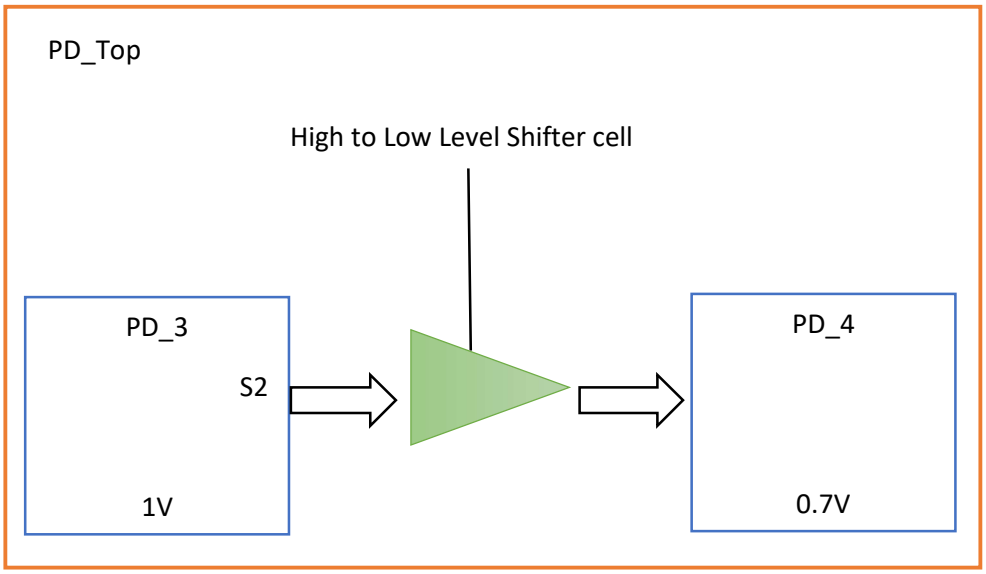

Fig. 1.12 HIGH to LOW level shifter cell

1.7.3 Retention Cell

Retention cells are unique cells that are used to store information in binary format, shown in Fig. 1.13. Before powering down, it can store its internal state and data in a register also known as a shadow register. When the primary power supply is disconnected, the device is able to keep its condition when power is restored. Master-Slave live Flip flop is the best illustration of a retention cell. It consists of a Master latch and a Slave latch whose output is dependent on negative or positive clock. In the retention operation, when the primary power is turned off, the Slave latch stores the data. The primary source of power for the latch is the main power rail of the "ALWAYS-ON" cell. State-saving latches are implemented with high-threshold transistors to reduce power consumption, allowing them to remain operational even in power-down mode [18]. The operation of the retention cell is controlled by the "SLEEP" signal. When a power domain's power supply is disconnected, the register's states should remain intact. Retention cells are always ON, therefore they continuously consume power. It has generally low leakage. Low Threshold cells are high-performance cells that receive their power from a standard supply, they can be latch/Flip Flop.

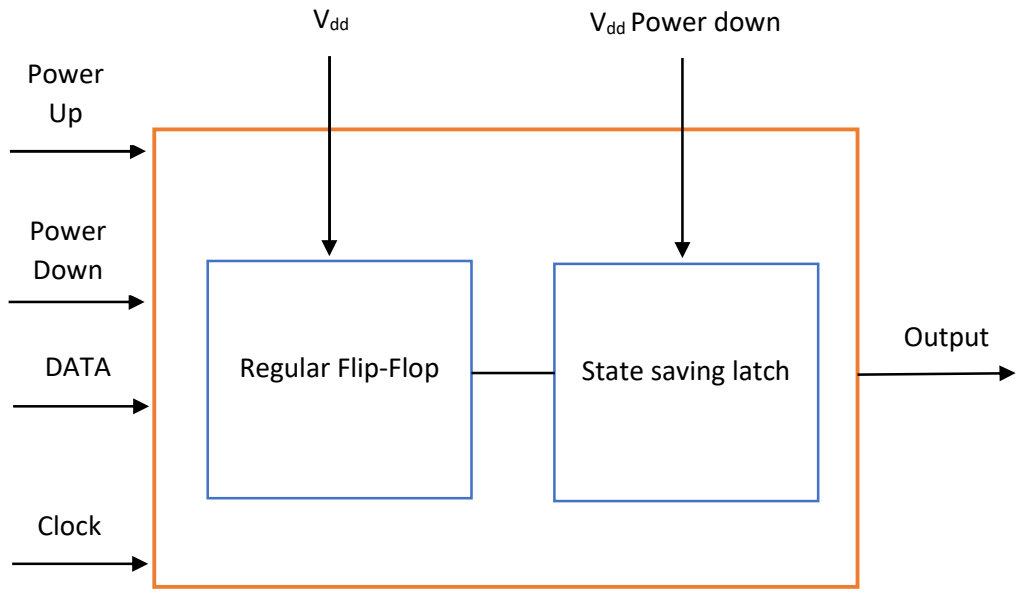

Fig. 1.13 Retention cell block diagram

In 'normal mode', the State saving latch is not activated. Before powering down the regular flip-flop, the value of the regular flip-flop will be transferred to the state

latch. The regular flip-flop is powered down, while the state-saving register is powered up for state retention.

1.7.4 Power Switch

In the design, power Switch cells are employed for power Gating by powering off a component of the design, shown in Fig. 1.14. When a subblock is no longer required or in use, it can be turned off using the power switch cell, and the scope command is used to turn off the voltage domain. As a power Switch, a Header (PMOS) and Footer (NMOS) transistor of fixed size is utilized. In order to activate the power switch of the PMOS transistor, the sleep signal is set to 'LOW' when the power switch is needed. The power switch is installed in both column and ring fashion [19].

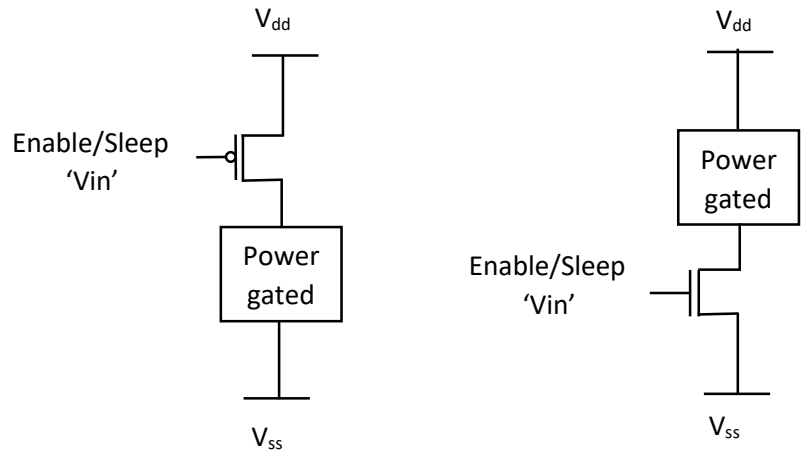

Fig. 1.14 MTCMOS Power Switch used for Power Gating.

Consider PMOS with MTCMOS power switch at drain that controls power gating by turning off the MOSFET using power gated logic. This Multi Threshold CMOS comes in two varieties:

1. Low Voltage Threshold
2. High Voltage Threshold

Low Voltage Threshold can reduce short circuit power during normal mode, while High Voltage Threshold can reduce leakage power during off mode.

1.7.5 Always-ON Cells

An always-on cell phone cannot be turned off. As always-on cells, buffers and inverters are typically employed. Logic cells should be powered on regardless of whether the power domain is ON or OFF. The power domain that can be turned off is referred to as the power down domain. While the Source and Sink domains are in the "ON" state, the logic inside the cell is employed to transport signals in the off domain [13, 19].

Always on cell are of two types:

- Single Rail Power cells
- Dual Rail Power cells

1.7.5.1 Single Rail Power cells: Only single-power inverters and buffers from standard cell libraries are used.

1.7.5.2 Dual Rail Power cells: These unique cells, such as inverter and buffer, are found in the target library. It has two power supply rails: a primary supply rail and a secondary supply rail, where the primary supply rail is connected to a power off supply and the secondary supply rail is always on as shown in Fig. 1.16.

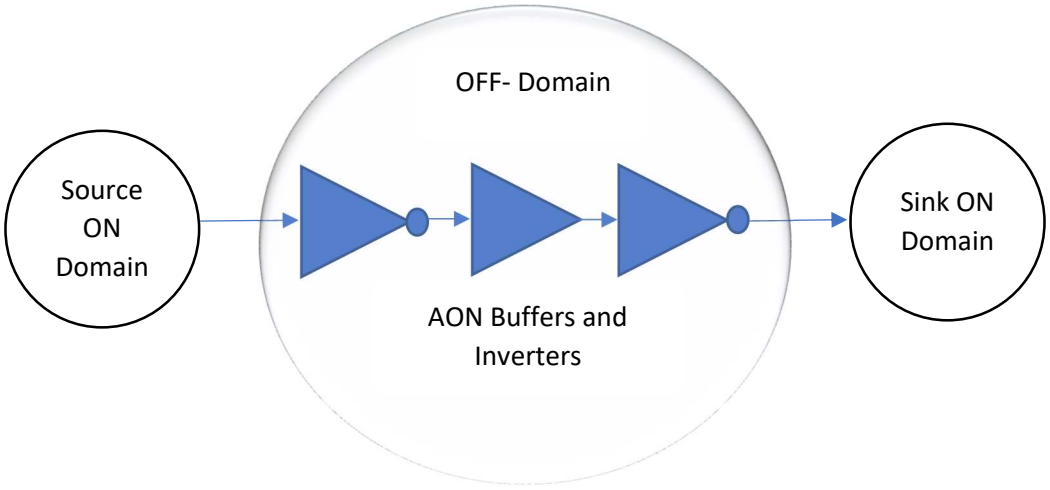

Fig. 1.15 AON Buffers & Inverters in OFF domain

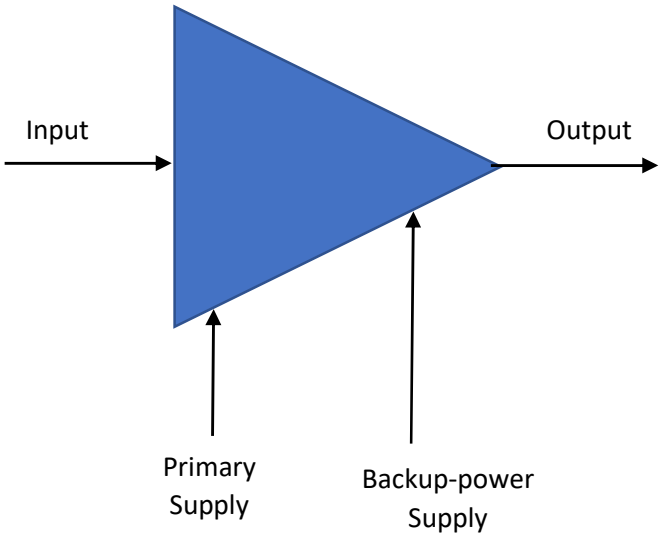

Fig. 1.16 Dual Power Rail Supply AON Cell

There are two types of power in a dual power rail supply: primary and secondary. According to RTL Engineer, primary power is always on, whereas secondary power can be turned on and off. In contrast, a single power rail supply solely provides primary power.

1.7.6 Enable Level shifter

Enable Level Shifter cells are also referred to as ELS cells, this is shown below in Fig. 1.17. It can operate both as a Level Shifter cell and an Isolation cell. Its benefit is the reduction of chip area. It is capable of changing voltage from low to high and high to low, as well as performing isolation from the Off domain to the On domain. If there is a crossing between two power domains from the OFF domain to the ON domain, an isolation cell with a perfect control signal and a clamp cell is required [10, 21]. If there is a voltage imbalance between the two domains, a level shifter is necessary. It is probable that both situations exist, thus Enable Level Shifter is required in this instance. For the OFF domain, the voltage is "High," while for the ON domain, it is "Low."

1.7.7 Bi-directional Level Shifters

The bidirectional level shifter can change voltage from high to low as well as from low to high.

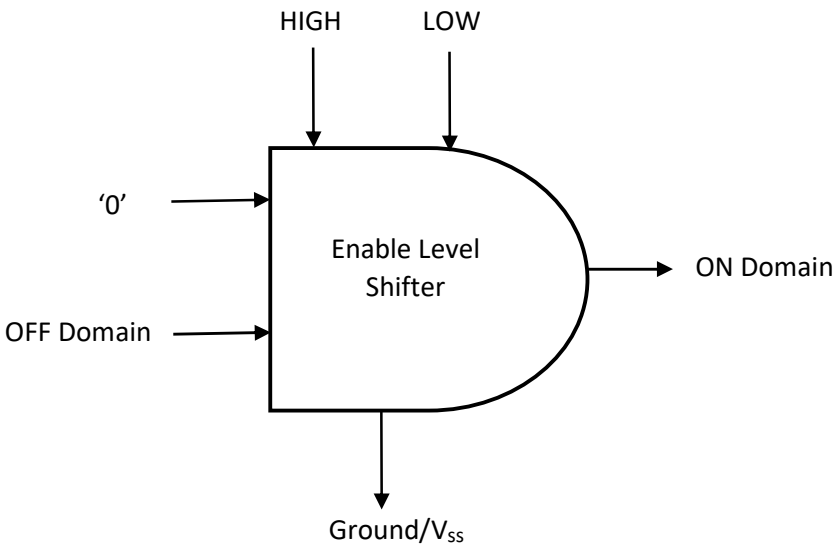

Fig. 1.17 Enable Level Shifter

If the voltage between Source and Sink varies over time due to dynamic voltage and frequency scaling, a bidirectional level shifter is employed to convert the voltage in both directions as shown in Fig. 1.18

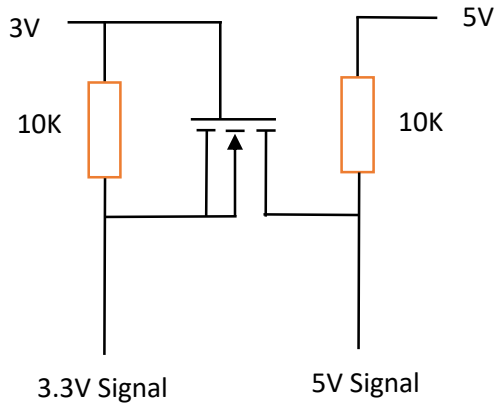

Fig. 1.18 Bi-directional Level Shifters

Here, the voltage is converted from 3.3V to 5V and vice versa. Therefore, it is known as a bidirectional level shifter.

Special power management cells discussed in section 1.8 are summarized below in Table 1.3. Table depicts which cells are used in a which particular design condition [7].

Table 1.3 Multiple voltage special cell requirement

Working & Function	**Isolation cell**	**Level Shifter Cell**	**Retension Cell**	**Power Switch Cell (MTCMOS)**	**Always-On Cell**
Multi-Volatge Domain	No	Yes	No	No	No
Multi-Supply with shutdown no state retension	Yes	No	No	Yes	No
Multi-Voltage with Shutdown	Yes	Yes	No	Yes	No
Multi-Voltage with Shutdown and State Retension	Yes	Yes	Yes	Yes	Yes

1.8 Conclusions

In this chapter, the fundamentals of low power design are covered. Why low power design and verification are required has been clarified. The motivation and purpose of this dissertation topic have been evaluated. Types of power dissipation, various low power verification checks in a design, UPF flow, and various low power strategies, as well as specific power management cells, have been covered

1.9 Motivation

The growing complexity of designs and shrinking technologies, which allow more functionality to be packed into a smaller area of a chip, have created a new set of hurdles for SoC verification. Hardware-software co-verification has become unavoidable with the introduction of new approaches and sophisticated tools that aid in verifying SoC connectivity, signal integrity, power management, and performance of analog components. To achieve faster results, this necessitates a unified and integrated verification environment with smooth information flow and reuse across domains/levels [4, 5].

Because node technology improves every year and demand is high, power consumption rises as well. For example, in technology nodes over 90 nm, dynamic power dissipation is larger than static power dissipation. Dynamic power usage can be minimized by reducing switching frequency (i.e toggling of output node from HIGH to LOW and vice versa). Static power consumption is more important than dynamic power consumption at technology nodes smaller than 90 nm. The outcome of leakage quiescent current is static power consumption (i.e there is no toggling of output node) [6].

Low power verification tools are next-generation verification system that offer a scalable environment in which advanced tools operate seamlessly together to complete diverse verification tasks by integrating technologies. As a low power solution, low power verification tools are utilized for voltage-aware functional verification. Using a sophisticated low power static-rule checker, all advanced power management operations are covered [3]. Static low power verification signoff tool offers a low-noise report, intelligent process analysis, quick unified debug, support for a unified power format, quick and rapid outputs,

and faster overall checks. Using a GUI to debug the design's violation, it is possible to locate precise faults and violations and perform low-power verification [7, 8].

1.10 Literature Review

1.10.1 Previous work reported

Compact size of an IC has many advantages, but as its power density rises, other difficulties arise. Not only does an integrated circuit with a high-power density heat the product, but it also becomes unstable quickly. Due to this issue, the IEEE 1801 low-power standards have been developed to make ICs more reliable, resilient, and standardized, which would alleviate these issues. The UPF is an IEEE standard that was established by Accellera members in 2007. It aims to simplify the process of describing, simulating, and testing IC designs with many power states and complex design. Once an IC is built, it must be verified by ensuring that its functionality and behaviour are correct and that it adheres to the IEEE 1801 low power standard, commonly known as the UPF. Engineers and researchers throughout the world have begun integrating UPF with Netlist for power-aware design and verification of processors or system on chips.

R. Sharafinejad et al. [2] have presented a methodology for formally verifying power with power management strategies in current processors in terms of two characteristics of functionality and automatic power management control throughout the verification process. In order to accomplish this, the PMU is extracted from the UPF and GPM and incorporated into the implementation such that low-level control signals for each power domain can be properly modified. The results demonstrate a 13 times reduction in verification time compared to existing methods.

V. Gourisetty et al. [5] represents A low power design flow in view of the UPF standard. This design cycle is implemented using electronic design automation tools from Synopsys and tested on generic 90nm and 32/28nm libraries from Synopsys. The synthesis scripts are formatted in the 'tcl' language, which is compatible with the Synopsys tools.

J. Patel et al. [11] proposes that in state-of-the-art low power IC architectures, designers implement a multitude of distinct power domains. These tools assist

designers in achieving the essential dependable, accurate, and exhaustive verification to create a sturdy design. Increasingly, low power design strategies are employed to prevent leakage and dynamic power consumption. By employing low power design techniques, life of batteries can be extended.

1.10.2 Objective

Following are the primary objectives of this dissertation:

- To perform different types of low-power verification checks like design checks, power ground check, etc. on Netlist and UPF of a particular System on chip design of lower technology node.
- To assess the importance of using special power management cells in design with different low power techniques in compliance with UPF.
- To analyze log files and report files generated by low power verification tool for debugging of errors with help of GUI.
- To analyze numerous types of violations/errors/warning given by low power verification tool and how to fix them.

1.11 Organization of work

This dissertation has been structured as follows:

Chapter 2: Low Power verification flow is discussed in great detail. Different types of low power checks along with UPF structure is mentioned. This chapter elaborates on different stages in debugging of low power checks along with warning and error messages given by tool.

Chapter 3: This chapter shows different types of error/warning/violation thrown by verification tool with generated reports and log files. Degguging of violations and errors through GUI is also shown in this chapter.

Chapter 4: Conclusions of dissertation are discussed in this chapter.

CHAPTER 2
LOW POWER VERIFICATION FLOW & STAGES

2.1 Introduction

In the low power verification design flow procedure, It begins with the design specification, which includes dimensions, power, and performance [4]. RTL block specifies how data is moved from one register to another. During each clock cycle, this data is sent to different registers using a boolean logic expression. This is accomplished using high-level languages such as Verilog and VHDL, and the synthesis tool accepts these files. UPF is added to RTL. It defines the architecture of power. It guarantees that the design will function properly under a PMU with a stated power architecture. The RTL is then transformed into a gate-level netlist. Here, Golden-UPF includes RTL. The UPF file is utilized in a number of low power verification design flow blocks, including synthesis, placement, and route, in conjunction with various low power verification designs and PG checks. Prior to the synthesizing process, the quality of the UPF and its mistakes are evaluated [1]. At this level, low power verification checks are done as shown in Fig 3.1. It is then transferred to the synthesis stage, where the compiler performs low power synthesis.

2.2 Low Power Verification Design Flow

Typically, synthesis converts the RTL to the gate-level netlist. By design compiler, all other low power information is recorded in Supplemental UPF. This combination of Supplemental UPF and Golden UPF is used for "UPF check" and "Design Check" using a low power verification instrument to determine whether or not the insertion of the cell during synthesis is proper. Then, both are sent to “Placement and Route” together with the synthesized netlist, where "UPF/low power checks", "Design Checks", and "PG Checks" are done using the physical netlist and UPF file [14]. Sign-Off, also known as tape out, signifies that design is complete and ready for physical implementation.

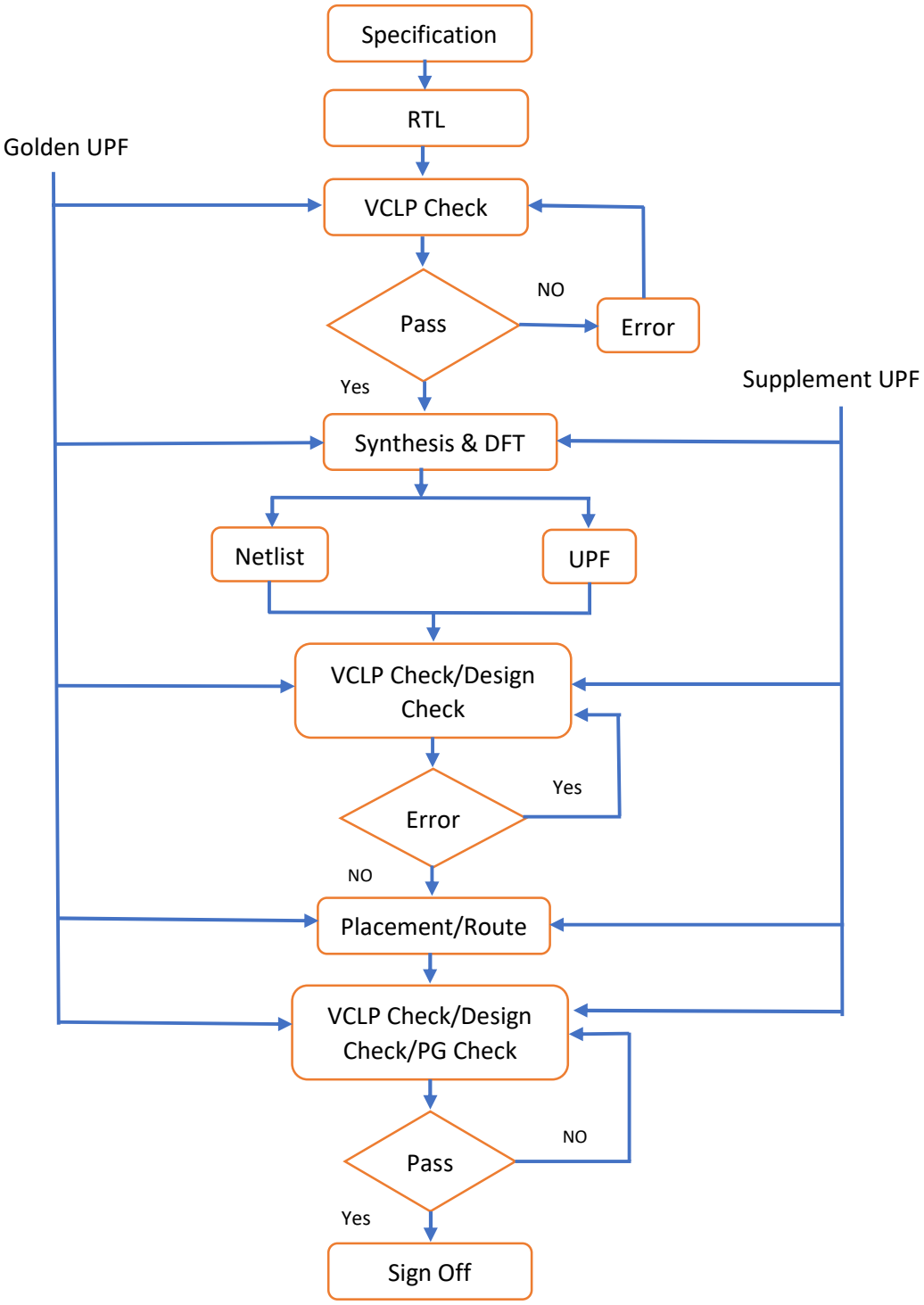

Fig. 2.1 Low power verification flow diagram

This flow is a recursive process, till all errors and warnings doesn't get resolved, Sign-Off will not happen.

2.3 UPF File Structure

The tool saves a UPF file to validate its operation in the .upf file format. It is written in TCL format. It follows a common UPF intent command. The file organization of UPF command are in Table 3.1

Table 2.1 UPF Power management commands

Sl. No.	UPF Power management commands
1	Create_power_domain
2	Set_design_attribute
3	Connect_supply_net
4	Create_supply_net
5	Add_pst_state
6	Create_power_switch
7	Add_power_state
8	Set_isolation
9	Map_power_switch
10	Set_isolation_control
11	Set_level_shifter
12	Map_isolation
13	Set_retention
14	Map_level_shifter

2.4 Important checks in Low Power Verification

The low power verification tool performs numerous tests on the Golden UPF and Netlist. Because of this, significant problems arise that must be resolved. Several of the errors are displayed here [22, 23].

- According to the PST state set specified in the UPF file, isolation protection is required from Source to Sink at the crossover between two power domains. Source and sink of the signal are related with the power condition of the supply set. If an isolation strategy is not specified, an isolation

protection cell will not be incorporated into the design. In the absence of an isolation strategy, energy may be squandered and the system may not operate correctly.

- At the boundary between two power domains, level shifter protection is required from source to sink, as indicated by the PST status set in the UPF file. Source and sink of the signal are related with the power condition of the supply set. If a level shifter approach is not specified, a level shifter protection cell is not incorporated into the design. When level shifter strategy is absent, power can be wasted and it functions wrongly. It can be typed from low to high or high to low.
- The instance's SCMR is not linked to the main primary power supply, indicated as UPF-supply. SCMR pin should be connected to primary power. The main rail of the standard cell determines how the physical connection will be handled in the floor plan block.
- When the supply pin of the Macro is not connected to the supply net, a Macro error occurs.
- PG check is displayed for connection of cell pin or instance pin. This pin should not be connected directly to the main power source or ground. Instead, this should be linked to TIE HIGH or TIE LOW.

2.5 Stages performed in low power verification

There are three phases of low power verification that must be verified and executed.

- Design/UPF development
- Post-Synthesis
- Post-Route

2.5.1 Design/UPF development

At this stage, UPF is generated and written, but it has not yet added low power management special cells such as isolation cell gates, PG connection checks, level shifter cell gates so that this type of problem will not arise in subsequent stages. For instance, the isolation strategy missing error is logged if the object is referenced in UPF but omitted from the design, and if the driver is off and the receiver is on.

2.5.2 Post-Synthesis

At this level, all prior checks have been conducted and UPF is stable, but any changes to the design will generate errors in the new UPF [24]. Consequently, a modification to the UPF is permissible in order to address the issue. At this stage, all cells may be installed, but the power and ground connections have yet to be made. At this step after Synthesis, the electrical accuracy can be examined. For instance, a level shifter is required at the crossover between two domains, but none is present, and the isolation gate is required at the requisite location, but the isolation control assigned to the isolation cell is not defined in the UPF [4].

2.5.3 Post-Route

At this stage, all prior checks are conducted and all low power objects, cells, and power/ground connections are verified; if an issue occurs, it can be resolved by modifying the UPF file and the Synthesis result. On the power/ground connection, all electrical correctness is examined to ensure that it complies with UPF. For instance, a level shifter is present at the crossing, but the input pin is linked to the power supply, but this is not reflected in the UPF file. Consider a scenario in which the power pin of the macro is connected to the supply power net, but the supply connected does not correspond to the supply in the UPF file.

2.6 Warnings in Design Setup

Here, two warnings that happened during the low power Verification tests are described [3, 7].

- Bit-specific Attribute Unsupported
- Input port is driven

2.6.1 Bit-specific Attribute Unsupported

Error:

- Bit-specific Attribute 'clock' on individual bus bit ‘bit_name’ of DBcell ‘cell_name_is_specified’ is not supported. It may lead to incorrect results.

Comments on the error:

- Here it shows that in specific .ldb file name “name of ldb file” of the cell “cell name” has a pin “pin name” has a clock on it.

How to check:

- Check the log file where you will receive error description as given above than go to db_link.log and search for the file and copy its path and open in vnc with .lib extension. Then go for “block name” in the file and in that go for “pin” and look according to error.

2.6.2 Input port is driven

Error:

- In the plan, input port 'input_name' is associated with yield or inout port in other instance 'instance_name'

Comments on the error:

- Here the module name is "model_name" has input port given "primary_power_input" and it is associated as inout or ouput in instance "instance_name"
- Similarly, for “Ground_input”.

How to check:

- Go to the "netlist file" and search for "instance name" to obtain all error-related information.

2.7 Conclusions

This chapter discusses the low power verification flow and its associated stages in detail. Important verification checks for low power have been mentioned. In addition, the UPF file structure and a few instructions are shown. Low power verification on different stages of netlist and UPF are shown in this chapter.

CHAPTER 3

RESULTS AND DISCUSSIONS

In design, child partitions and top partitions are used to perform and process a variety of tasks. To ensure that these partitions function properly, various types of checks are performed, as depicted in Fig. 1.4 low power verification check on UPF and netlist file at different stages as shown in Fig 2.1 Using the load upf command, child partitions are added to the top partition. At this point, the debugging process begins. The low power verification program will generate a very simple report to help the user comprehend the problem with the power distribution design and its associated files. Two input files are required for debugging: the gate level netlist file, which displays the physicality of the power design's connectivity, and the UPF file, which specifies the logical connections [25].

As seen in Section 1.7, distinct cell types execute distinct functions. In the report Management_summary and tree_summary violations help in resolving and minimizing problems in low-power designs. In the partition uncompressed file, the management_summary and tree_summary files are created. This violation summary can be found using the commands listed below, such as read_upf and report_violation. As complexity in design and low power increases rapidly, the design undergoes additional functional signoff checks to satisfy the requirement. By manually checking a large number of reports with TCL, UPF, Design & GUI debugging will be quite slow.

3.1 Output and Simulation results

The low power verification tool reduces debugging time by intelligently grouping violations and revealing the actual root cause, hence saving time. Similar violations in the uncompressed file that can be compressed are displayed in the partition compressed file. In management_summary, violations and errors are displayed using checking stages, whereas in tree_summary, the result is displayed using severity checks. These are shown in following Tables 3.1 and 3.2

Table 3.1 Management summary of design with different family violations

Management Summary				
Stage	**Family**	**Errors**	**Warnings**	**Infos**
UPF	Isolation	1880	151	0
UPF	Level Shifter	40507	0	0
UPF	Upf consistency	6	1	0
Design	Analog	201	0	0
Design	Design Consistency	90	0	0
Design	Isolation	360	3	0
Design	Level Shifter	48	0	0
PG	Power Ground	1	4343	0
Total		**48325**	**4506**	**0**

Table 3.2 Tree summary of design with all low power violations

Tree Summary			
Severity	**Stage**	**Tag**	**Count**
error	UPF	ISO_CONTROL_STATE (2)	2
error	UPF	ISO_STRATEGY_MISSING (1878)	1878
error	UPF	LS_STRATEGY_MISSING (40507)	40507
error	UPF	UPF_SPADRIVER_STATE (3)	3
error	UPF	UPF_SPARECEIVER_STATE (1)	1
error	UPF	UPF_SUPPLY_NOLOAD (1)	1
error	UPF	UPF_SUPPLY_NOSTATE (1)	1
error	Design	ANALOG_NET_INCORRECT (201)	201
error	Design	DESIGN_BACKUP_STATE (90)	90
error	Design	ISO_BUFINV_STATE (1773)	1773
error	Design	ISO_CONTROL_CLAMP (1441)	1441
error	Design	ISO_CONTROL_CONN (41)	41
error	Design	ISO_INST_MISSING (1878)	1878
error	Design	ISO_SINK_STATE (99)	99
error	Design	LS_INST_MISSING (360)	360
error	PG	PG_BIAS_EXCESS (16)	16
error	PG	PG_BIAS_INSUFFICIENT	16
error	PG	PG_BIAS_PATH	16
error	PG	PG_SUPPLY_NOPORT	1
warning	UPF	ISO_MAP_MISSING	75
warning	UPF	ISO_STRATCONTROL_GLITCH	14
warning	UPF	ISO_STRATEGY_IGNORED	62

warning	UPF	UPF_ATTR_OVERRIDE	1
warning	Design	ISO_CONTROL_GLITCH	3
warning	Design	ISO_OUTPUT_UNCONN	8
warning	PG	PG_DATA_SUPPLY	4343
Total			**52831**

The **report_upf** command displays the design top name, which is the primary project. After reading the UPF file, it generates information regarding the power intent. By using the report_upf command, one may determine how many instances of isolation, level shifter, retention, power switch, and multi-rail macros exist in the upf file as shown in Table 4.3. Similarly, the report_design command provides information on the design and library file.

Table 3.3 Power intent information generated by report_upf command

Read UPF	
Design top	TOP
Isolation instances	0
Level shifter instances	6087
Retention instances	0
Power switch instances	0
Multirail macro instances	3
Total instances	493389
Crossovers	88031
Merged power states	13

The **report_read_violation** command is used to obtain a comprehensive report of all SDC, UPF violations, design read as well as GUI violations as shown in Tables 3.4 and 3.5. The low power verification tool displays the source and sink destination in GUI format, making debugging extremely flexible. By executing the report_read_violation command in the low power verification shell, the message can be viewed in its summary form.

Table 3.4 Management summary by report_read_violation command

Management Summary				
Stage	**Family**	**Errors**	**Warnings**	**Infos**
DESIGN_READ	UPF	0	1	79
TCL	SETUP	1	1	3
Sanity	SETUP	0	0	6
Total		**1**	**2**	**88**

Table 3.5 Tree summary by report_read_violation command

Tree Summary			
Severity	**Stage**	**Tag**	**Count**
error	TCL	CMD-013	1
warning	Design read	UPF_ATTR_VALUE_OVERRIDE	1
warning	TCL	COM_OPT009	1
info	Design read	POWER_TOP_SCOPE	1
info	Design read	UPF_FILE_LOADED	2
info	Design read	UPF_FILE_PARSING	1
info	Design read	UPF_ISOLATION_BIAS	75
info	Sanity	NEW_FIELD_DEFINITION	6
info	TCL	CMD-081	2
info	TCL	COM_OPT030	1
Total			**91**

3.2 Debugging through GUI

In Fig. 3.1, GUI representation of the error supply short, the pin with the stated 'instance' is indicated by an arrow, however, in design, many pins of different instances are shorted with one another.

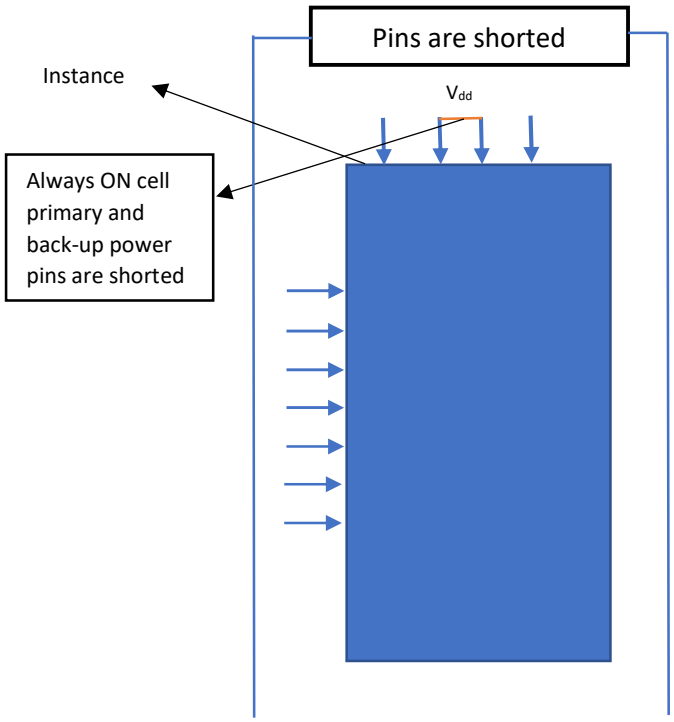

Fig. 3.1 GUI representation of an error "supply short" in tool

A supply short is a severe electrical violation between the power and ground networks [4]. In some instances, several types of power pins (i.e., internal power

pins and power switch cell's power pins) are shorted, along with always-on cell pins such as the primary and backup power pins, which is redundant in the design.

As depicted in Fig. 3.2, Isolation Strategy is ignored in the GUI display by debugging through low power verification. An arrow indicates the pin where Isolation strategy at the crossing of two power domains will be ignored during tests. By colour in GUI, two distinct power domains are represented.

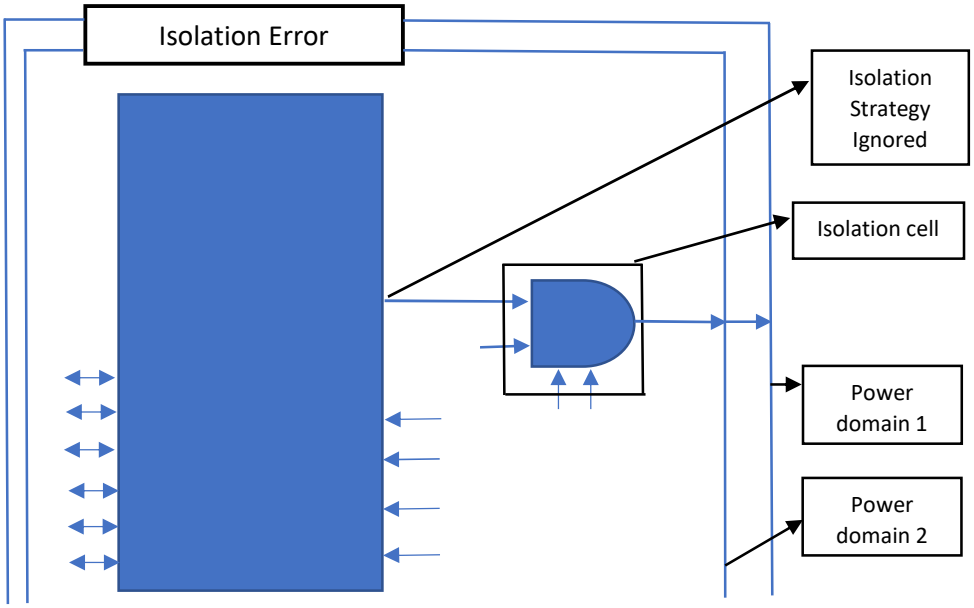

Fig. 3.2 GUI representation of error "Isolation strategy missing"

3.3 Conclusions

Low power verification has been performed on given design of SoC. All reports of violations have been tabulated. GUI view is also shown. Debugging of two errors through GUI is also represented. This verification tool provides feature of GUI which makes easier to debug violation and errors in design.

CHAPTER 4

CONCLUSION

Low power design of System on chip, be it smartphones, wearable devices, or laptops is the need of the hour. Static low power verification of any SoC design ensures that all low power checks are in compliance with UPF. If any error/violations are found, it is reported back to the design engineer for correction. In this project, all low power issues of a particular SoC have been verified and debug and results have been added to this report. Report and log files clearly mention all violations which have to corrected in Netlist and UPF files. GUI helps in debugging of violations with ease. If all errors and warnings got resolved, then this Netlist and UPF is given to Tape-out through which it will be given to foundry for manufacturing of devices. The low power verification tool enables us to find and report low-power issues and provide a design free of bugs. Increasing chip density and operation speed may result in a chip design with a high clock frequency and complexity. As a result, the requirement for static low power verification of SoC will only expand in the future, as the semiconductor industry continues to rapidly scale down and daily innovations are introduced. As a future project, this can be developed in a way to verifying multicore processors.

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