STUDY AND DESIGN OF SECOND GENERATION VOLTAGE CONVEYER BASED ANALOG CIRCUITS

A DISSERTATION

SUBMITTED IN THE PARTIAL FULFILLMENT OF THE REQUIREMENT FOR THE AWARD OF THE DEGREE

OF

Master of Technology

In

VLSI Design & Embedded Systems

Submitted by:

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MAY 2022

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CANDIDATE'S DECLARATION

I, ABHINAV ANAND, student of MTech (VLSI Design and Embedded Systems), hereby declare that the project Dissertation titled "STUDY AND DESIGN OF SECOND GENERATION VOLTAGE CONVEYER BASED ANALOG CIRCUITS" which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

Date: 25/05/2022 **ABHINAV ANAND**

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CERTIFICATE

This is to certify that the work contained in the project titled "**Study and design of second generation voltage conveyer based analog circuits",** submitted by **Abhinav Anand, Roll no. 2K20/VLS/01,** in the partial fulfillment of the requirement for the award of Master of Technology in VLSI & Embedded Systems to the Electronics & Communication Engineering Department, Delhi Technological University, Delhi, is a bona fide work of the students carried out under my supervision.

Date: 25/05/2022

Place: Delhi

Submitted to:

Prof. Rajeshwari Pandey

SUPERVISOR

Abstract

Second generation voltage controlled conveyers is an active block that is being widely explored in the field of analog electronics. Many exciting and wide range applications are being realized using second generation voltage conveyers. The applications such as sensor read out circuits, amplifiers, instrumentation amplifiers, multivibrators, etc. The properties of VCII can be used to implement applications like current follower, voltage follower, voltage to current converter, current to voltage converter, voltage differentiator, voltage integrator, etc. The work done during the course of this project helps in realizing analog circuits based on second generation voltage conveyer circuit. The analog circuits which have been implemented using VCII in this project are voltage buffer, current buffer, current to voltage converter, voltage to current converter, voltage differentiator, voltage integrator, Schmitt trigger, and Pulse Width Modulator.

The Schmitt Trigger and Pulse Width Modulator circuits that have been designed using VCII presents a novel approach to realizing such non linear applications using active blocks. The circuits of Schmitt Trigger and Pulse Width Modulator have been designed using CMOS technology of 180 nm. The operation of both the circuits have been critically analyzed through mathematical computations and the feasibility of the circuits have been validated using SPICE simulations.

ACKNOWLEDGEMENT

The successful completion of this project would not have been possible without the guidance and supportive mentorship of Prof. Rajeshwari Pandey. The constant motivation and support of my mentor was the major driving force behind all the hard work put into the completion of this work, brainstorming of ideas, all the learnings acquired during the course of this project and successful implementation of all the ideas

A special thanks to my cohorts and peers for always helping out with my queries during the course of this project. Despite the odds, they have always motivated and inspired to work hard.

I would like to thank my family members for all the support and guidance, to cope up with all the hardships and adversities, and keeping consistent focus for successful completion of this project.

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NOMENCLATURE

Abbreviations

NMOS	N- channel Metal oxide semiconductor
PMOS	P- channel Metal oxide semiconductor
CMOS	Complementary Metal oxide semiconductor
VCII	Second generation voltage conveyer
mW	Milli Watts
nW	Nano Watts
pJ	Pico Joules
V	Volts
F	Farads
nm	Nano meters
V to I	Voltage to current
I to V	Current to voltage
G	Transconductance gain
R	Impedance gain
α	Intrinsic voltage gain
β	Intrinsic current gain
AC	Alternating current
dB	Decibels
Vref	Reference voltage
Vin	Input voltage
Vout	Output voltage

Chapter 1
Introduction to VCII

1.1 Introduction:

Implementation of analog circuits using active blocks is being enormously explored. The concept of active blocks in realizing analog circuits is the high controllability it offers over passive components. One such active block, a second generation current conveyors [1]-[2] has also created feasible opportunities in realizing amplifiers [3]-[4], simulated ground inductors [5]-[7], sensor read-out circuits [8]-[9], instrumentation amplifiers [6] [7] etc. The second generation current conveyers are functionally active blocks. The major advantages offered by the second generation current conveyers are high linearity, high frequency range and a wide sense of dynamic range. Current conveyers are being used in a wide range of applications.

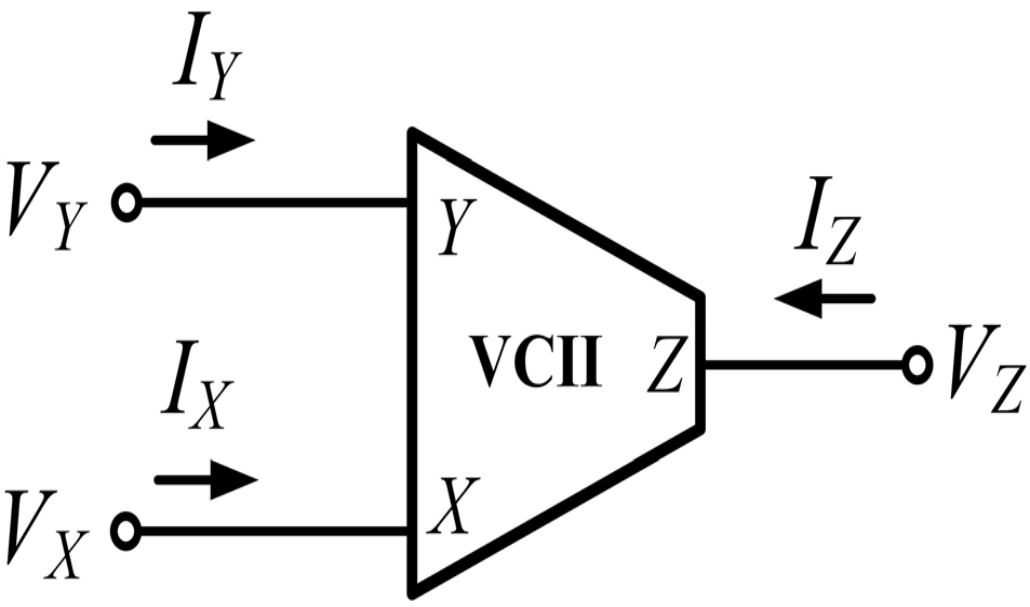

Fig. 1.1: Basic block signifying second generation voltage conveyer [10]

The second generation voltage conveyers can also be a useful active building block to realize analog functions. The analog functions can be implemented using both current mode and voltage mode approach. The basic difference between a current controlled conveyer and a voltage controlled conveyer active blocks is the driving port signal. In current controlled conveyers, the current signal on the input port is conveyed to the output port. In voltage controlled conveyers, the voltage at the input port is transferred to the output port.

1.2 Motivation:

Second generation voltage conveyers (VCII) are being potentially explored to implement variety of applications in the analog domain. The applications include voltage buffers, current buffers, voltage to current converters, current to voltage converters, analog filters, etc. The research prospects of second-generation voltage conveyers have encouraged the researchers to explore various applications using second voltage conveyers and its design. [3][4]

Various applications have been explored in this project and the properties and performance parameters associated with each application has been studied and analyzed. Different designs of VCII have also been studied. [2]

The most sought-after application of the second-generation voltage conveyer that is being researched is the novel oscillator. The next course of work will be based on the design and implementation of the novel oscillator circuit using VCII.

1.3 Mathematics of second-generation voltage conveyers (VCII)

A Second-generation voltage conveyer is a three-port block. The three ports/terminals of the block are namely X, Y and Z terminals. According to (1.1), the output at all three ports are mentioned with respect to values of parasitic component within the device, the values of voltage and current across all the three ports i.e. X, Y and Z ports. The equation (1.1) is applicable at low frequencies for the calculation of output signals at the X, Y and Z ports It is seen that a VCII block consists of a current buffer between Y and X terminals and a voltage buffer between X and Z terminals.

$$\begin{bmatrix} Ix \\ Vy \\ Vz \end{bmatrix} = \begin{bmatrix} \left(\frac{1}{Rx}\right) + sCx & \pm\beta & 0 \\ 0 & Ry + sLy & 0 \\ \alpha & 0 & Rx + sLz \end{bmatrix} \begin{bmatrix} Vx \\ Iy \\ Iz \end{bmatrix} \qquad (1.1)$$

The operation of the voltage conveyer active block can be demonstrated in (1.1). The input current, which is supplied to the Y terminal of the VCII block, is transferred to the X terminal, according to the operation of the conveyer. This transfer of current takes place through a current buffer network, which is present between the X and Y terminals. Thereafter, the voltage produced at the x terminal will generate output voltage at the low impedance Z terminal. This generation of voltage takes place through a voltage buffer network between X and Z terminals of VCII.

1.4 Applications of voltage conveyer circuit (VCII)

- Voltage to current converter

A typically ideal V to I converter employs high output impedance characteristics. The circuit diagram of V to I converter implemented by using VCII is illustrated in Fig. 1.2.

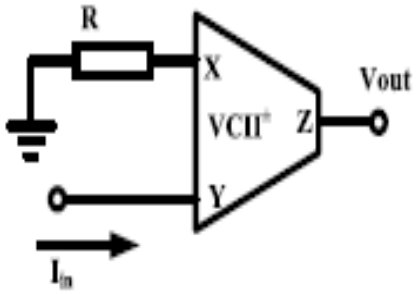

Fig. 1.2: Voltage to current converter [2]

- Current to voltage converter

A typically ideal I to V converter employs low output impedance characteristics. The circuit diagram of I to V converter implemented by using VCII is illustrated in Fig. 1.2.

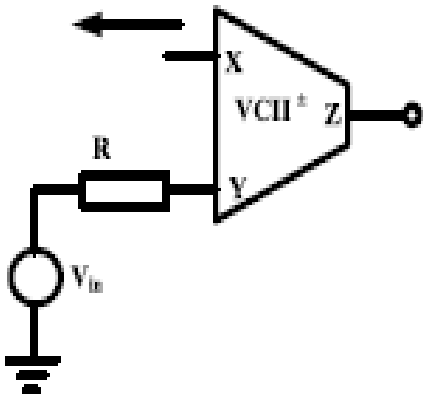

Fig. 1.3: Current to voltage converter [2]

- Voltage Buffer

The voltage buffer circuit is implemented using the unity voltage gain of second generation voltage conveyer. The circuit diagram of the VCII based voltage buffer is given in Fig 1.5.

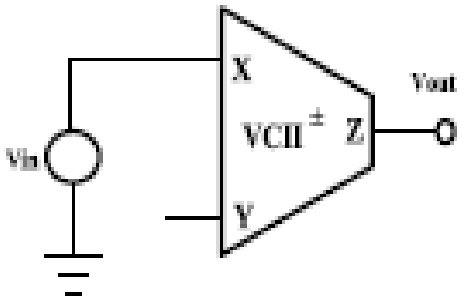

Fig. 1.4: Voltage buffer [2]

- Current buffer

The unity current gain of the second generation voltage conveyer enables the implementation of a current buffer using VCII. The circuit diagram of the current buffer circuit is given in Fig 1.6.

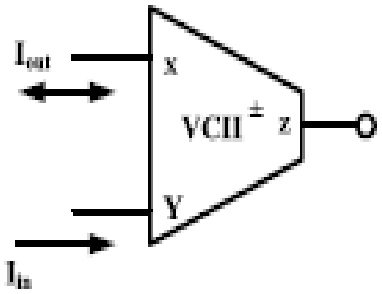

Fig. 1.5 : Current buffer [2]

- Voltage Differentiator

The circuit diagram for implementation of a voltage differentiator circuit using VCII is given in Fig. 1.6. The output response and the gain bandwidth curve is plotted to analyze it's performance.

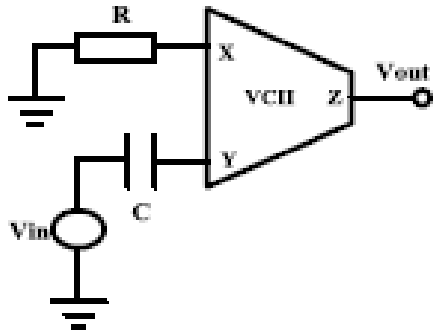

Fig. 1.6: Voltage differentiator [2]

The values of resistance and capacitance determine the mid band gain and the output level of the circuit.

- Voltage Integrator

The circuit diagram for implementation of a voltage integrator circuit using VCII is given in Fig 1.8. The output response and the gain bandwidth curve is plotted to analyze it's performance.

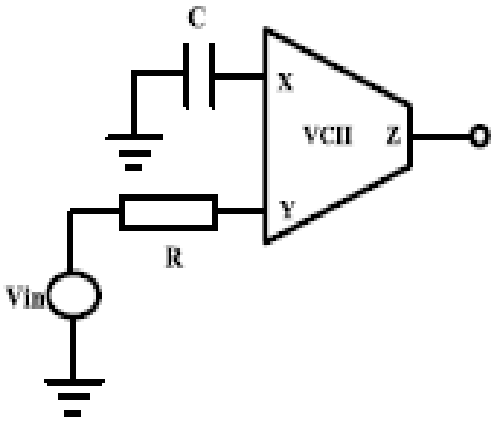

Fig. 1.7: Voltage integrator [2]

The mid band gain and the output level of the circuit is dependent on the values of passive components present in the circuit. The operations of these circuits have been discussed and validated in chapter 2 and chapter 3.

Chapter 2

Schematic design of VCII circuit

In this chapter, a second-generation voltage conveyer (VCII) circuit has been discussed and various design constraints and parameters have been discussed. Schematic design of the circuit has been done on software LT Spice. Operation of the second generation voltage conveyer circuit has also been discussed and role of different circuit components constituting the circuit has been explained.

2.1 Circuit Design of VCII+ and VCII-

Circuit diagram of VCII+ and VCII- have been illustrated in Fig 2.1 and Fig. 2.2. The schematic has been designed on LT Spice using 180-nm CMOS technology and supply voltage of ± 0.90 V. The device sizing and dimensions are mentioned in Table 2.1.

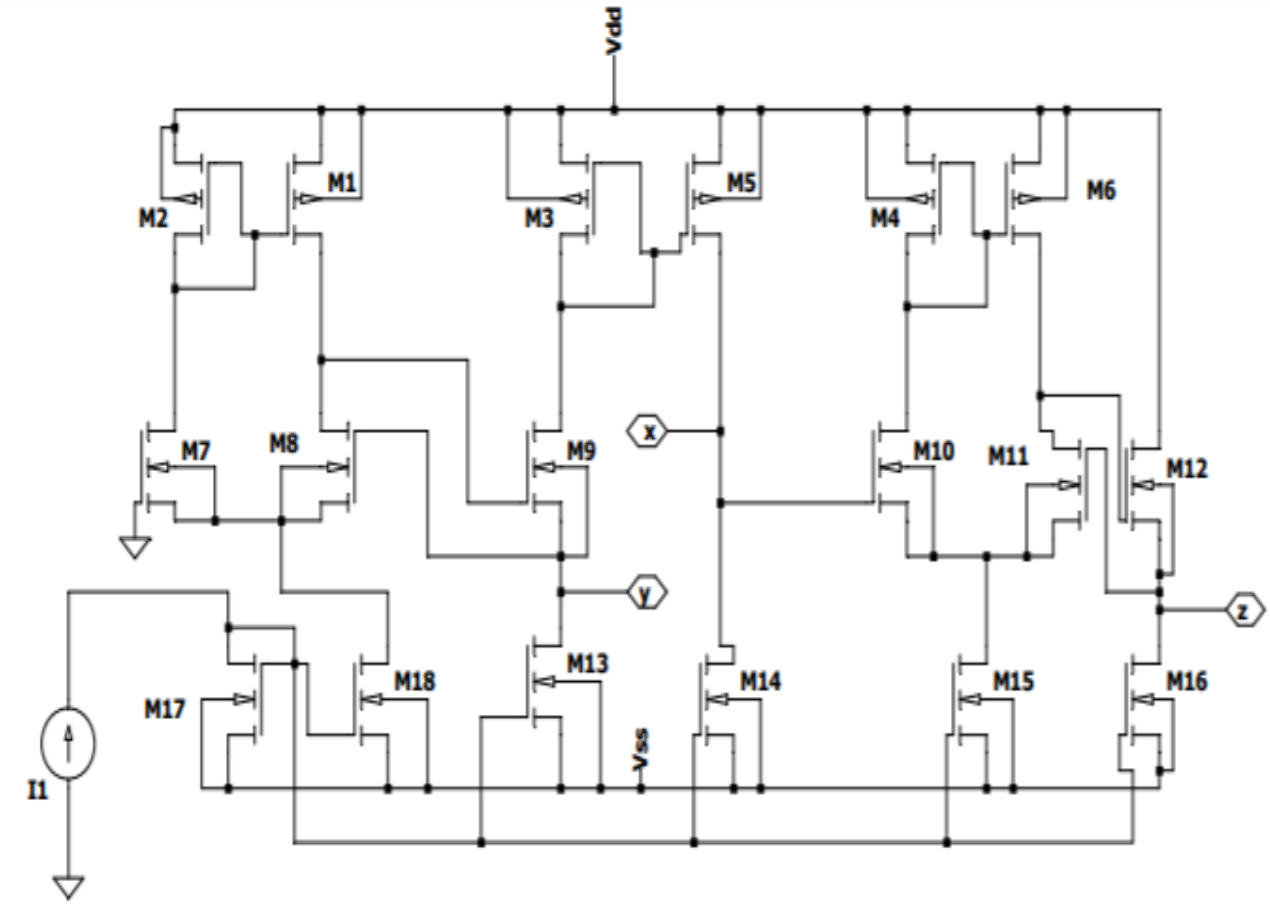

Fig 2.1: Circuit diagram of VCII+

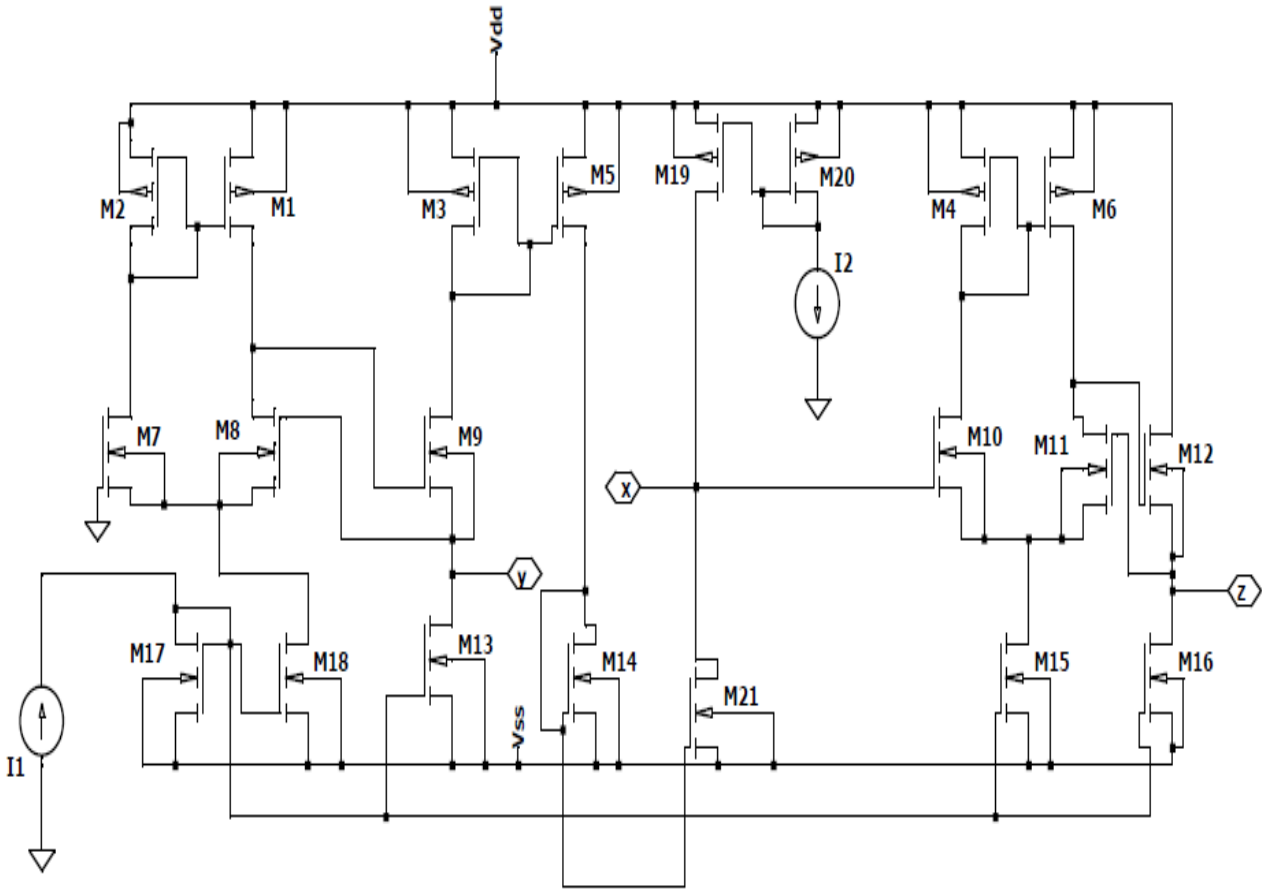

Fig. 2.2. Circuit diagram of VCII-

2.2 Explanation and role of different components

The above schematics, in Fig. 2.1 and Fig. 2.2, uses independent current sources, to feed the circuit with a constant current. A VCII circuit configuration is constituted of two basic circuits. One voltage buffer network is established between the X and Z terminals of the circuit. A current buffer network is established between the Y and X terminals of the circuit.

The implementation of VCII, as seen in Fig. 2.1, takes place through a series connection of current buffer formed with MOS transistors M1, M2, M3, M5, M7, M8 and M9 and voltage buffer is made of MOS transistors M4, M6, M10, M11 and M12. A sperate negative feedback is established in the current buffer network which is constituted with MOS transistors M1, M2, M7 and M8 are used to provide low impedance at the Y terminal. From Fig. 2.1, it can be inferred that a simple current mirror, which is constituted between MOS transistors M3 and M5 enables input current, which is fed at the Y terminal, according to the conveyer action is transferred to the X terminal. A voltage buffer network is constituted and established between MOS transistors M4, M6, M10, M11 and M12. The voltage conveyer action will enable the voltage produced at

the X terminal to be transferred to the Z terminal.

The low impedance generated at the Z terminal is employed by negative feedback loop established between MOS transistors M10, M4 and M6. Finally, MOS transistors M13 to M18 are used for the biasing.

2.3 Creation of VCII block using hierarchy

Use the create symbol option in LT SPICE to create symbol for the above voltage conveyer circuit. The instance name given to this block to be used in the implementation of various application is VCII block. The block has 3 bidirectional nodes namely x, y and z nodes. These nodes are used as input and output nodes in circuits implemented using VCII block. The supply voltage is a constant ±0.90 V.

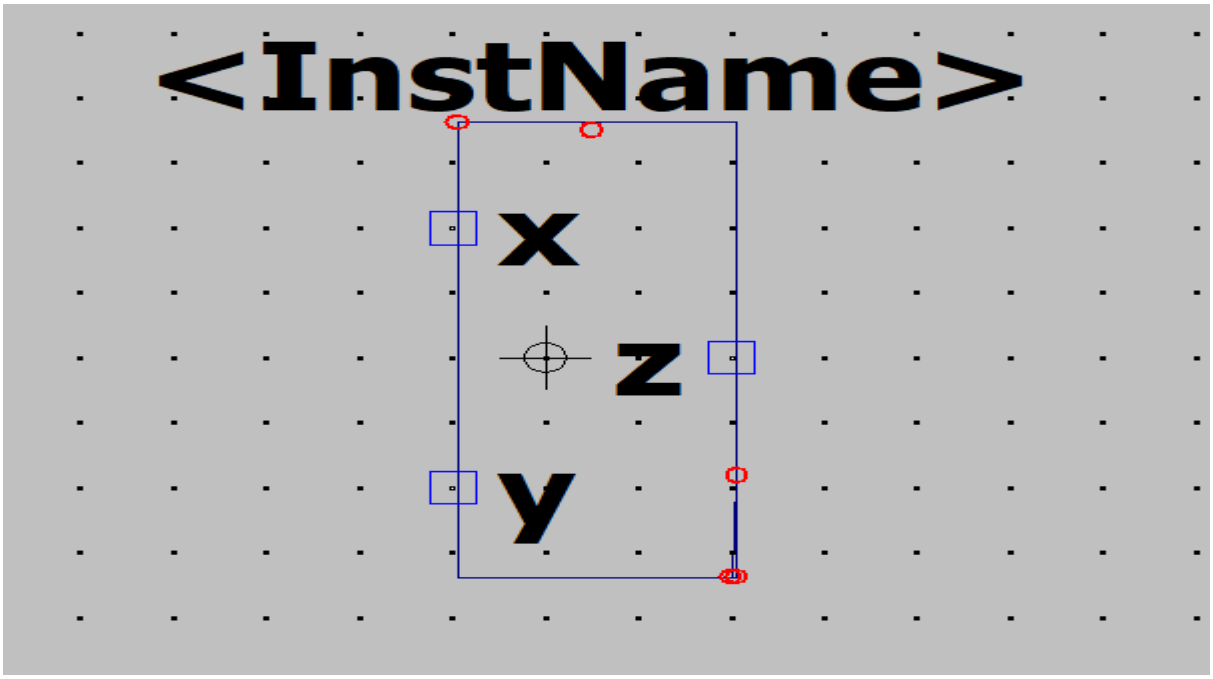

Fig 2.3: Symbol for VCII block

Chapter 3

VCII based Analog circuits

In this chapter, various applications related to second generation voltage conveyer (VCII) have been discussed and implemented using schematic simulation tool LT Spice with 180-nm CMOS technology. The supply voltage is a constant ± 0.90 V. The performance parameters of each circuit have been critically and comprehensively analyzed. The circuit of second generation voltage conveyer used in implementing the circuits is taken from Fig.2.2, chapter 2.

The applications that have been implemented and discussed in this chapter are V to I converter, I to V converter, Voltage buffer, Current buffer, Voltage differentiator and Voltage integrator. The functional feasibility of all circuits has been verified using transient response with input signal as a sinusoidal waveform and step response.

3.1 Voltage to current converter (V to I converter)

- Circuit Diagram is given in Fig 3.1. The voltage conveyer block used in the circuit is the circuit taken from Fig 2.1 in chapter 2. The aspect ratio of all the PMOS transistors and NMOS transistors in the VCII+ circuit, are (40.5 μm/0.54 μm) and (13.5 μm/0.54 μm) respectively. The supply voltage given to the circuit is ±0.90 V. To plot the sinusoidal response, a sine waveform having frequency 1 kHz and amplitude of 20 mV peak to peak is given as input to the circuit. To plot the step response, a step waveform of 10 mV is given as input to the circuit.

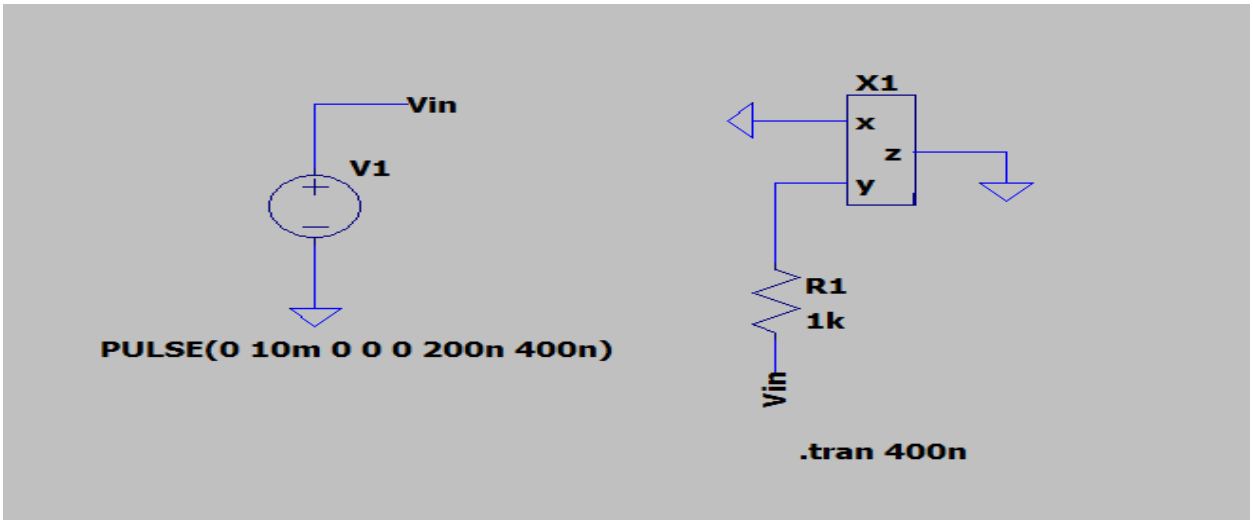

Fig. 3.1: Voltage to current converter

The input voltage is provided to terminal Y of the VCII block and output current is taken from the nodal current of X node of VCII block.

- Transient or the sinusoidal response of the V to I circuit can be observed in Fig. 3.2.

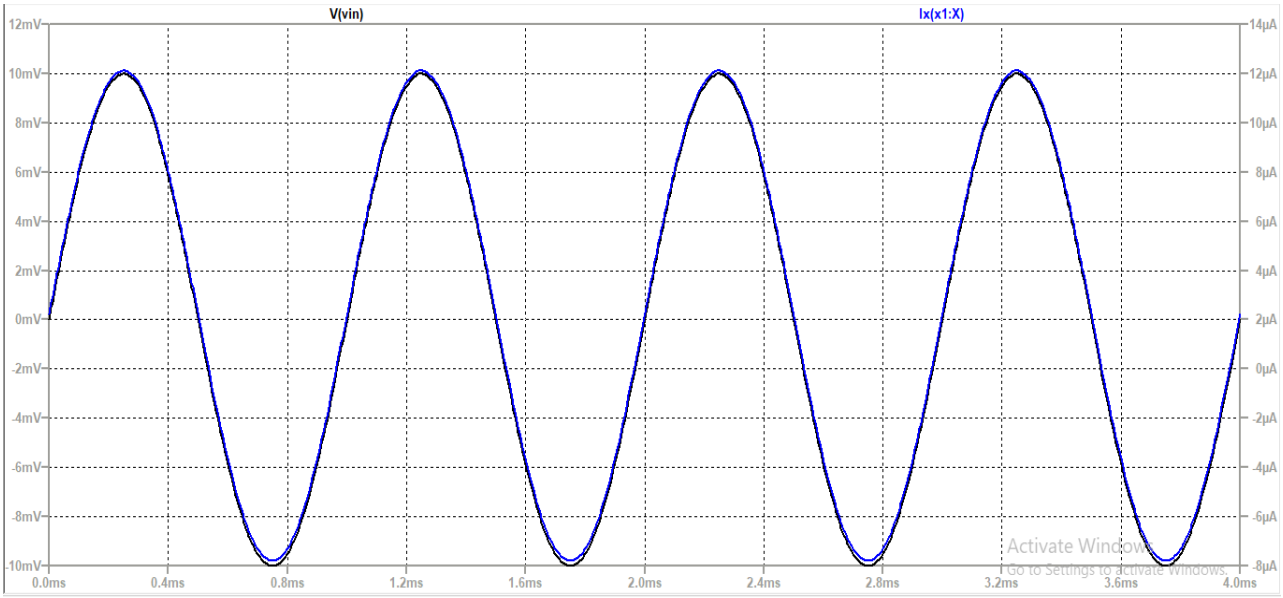

Fig. 3.2: Sinusoidal response of V to I circuit

- The step response of the V to I circuit can be observed in Fig. 3.3.

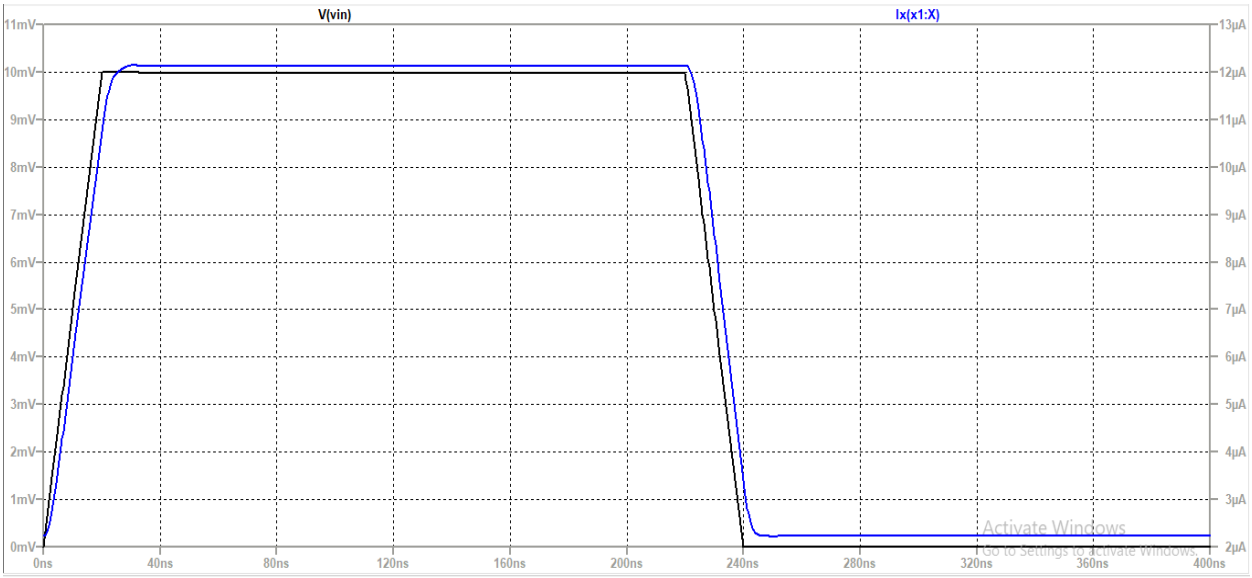

Fig. 3.3: Step response of V to I converter

- Calculation of the transconductance gain of V to I converter from the above step response.

The transconductance gain of the circuit is calculated as :

Transconductance gain(G) = Ix(x1:x)/V(Vin)

G = 12uA/10mV= 1.2mS.

3.2 Current to voltage converter (I to V converter)

- Circuit Diagram is given in Fig 3.4. The voltage conveyer block used in the circuit is the circuit taken from Fig 2.1 in chapter 2. The aspect ratio of all the PMOS transistors and NMOS transistors in the VCII+ circuit, are (40.5 µm/0.54 µm) and (13.5 µm/0.54 µm) respectively. The supply voltage given to the circuit is ±0.90 V. To plot the sinusoidal response, a sine waveform having frequency of 1 KHz and amplitude of 20 µA peak to peak is given as input to the circuit. To plot the step response, a step waveform of 10 µA is given as input to the circuit.

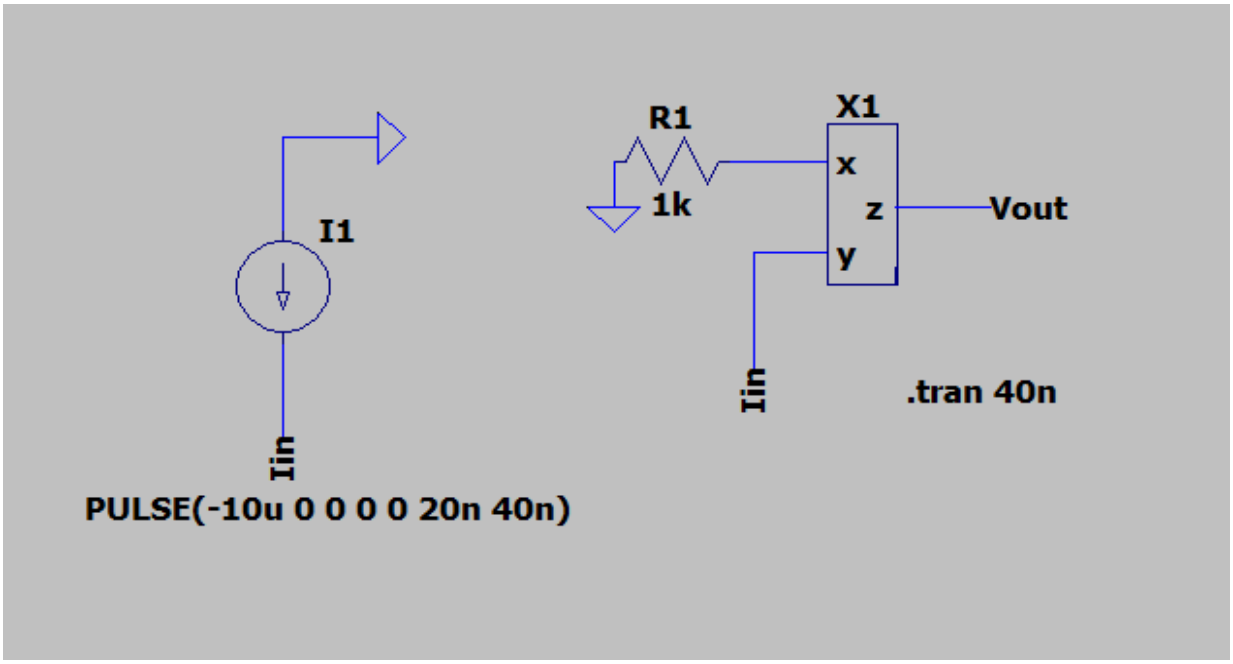

Fig. 3.4: I to V convereter

The input current is provided to terminal Y of the VCII block and output voltage is taken from Z node of VCII block. The voltage conveyer action enables the current at y terminal to be reflected on the x terminal of the circuit. The corresponding voltage which is produced at the X terminal is transferred to the z terminal of the circuit.

- Transient or the sinusoidal response of the I to V circuit can be observed in Fig. 3.5.

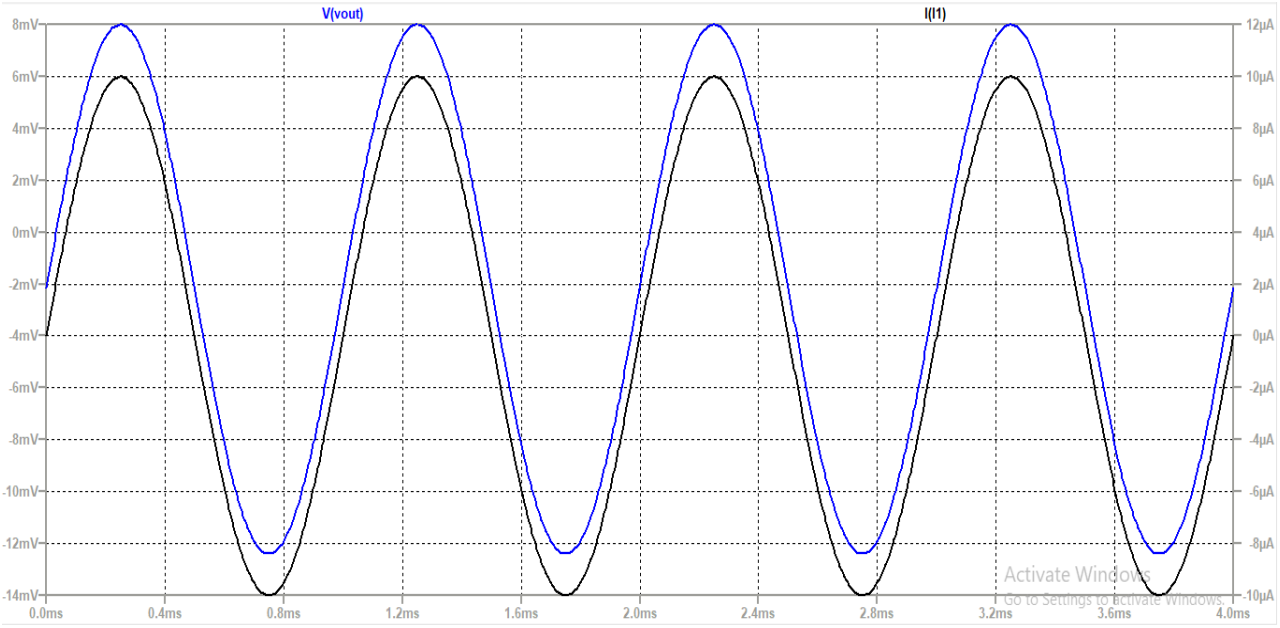

Fig. 3.5: Sinusoidal response of I to V circuit

- The step response of the I to V circuit can be observed in Fig. 3.6.

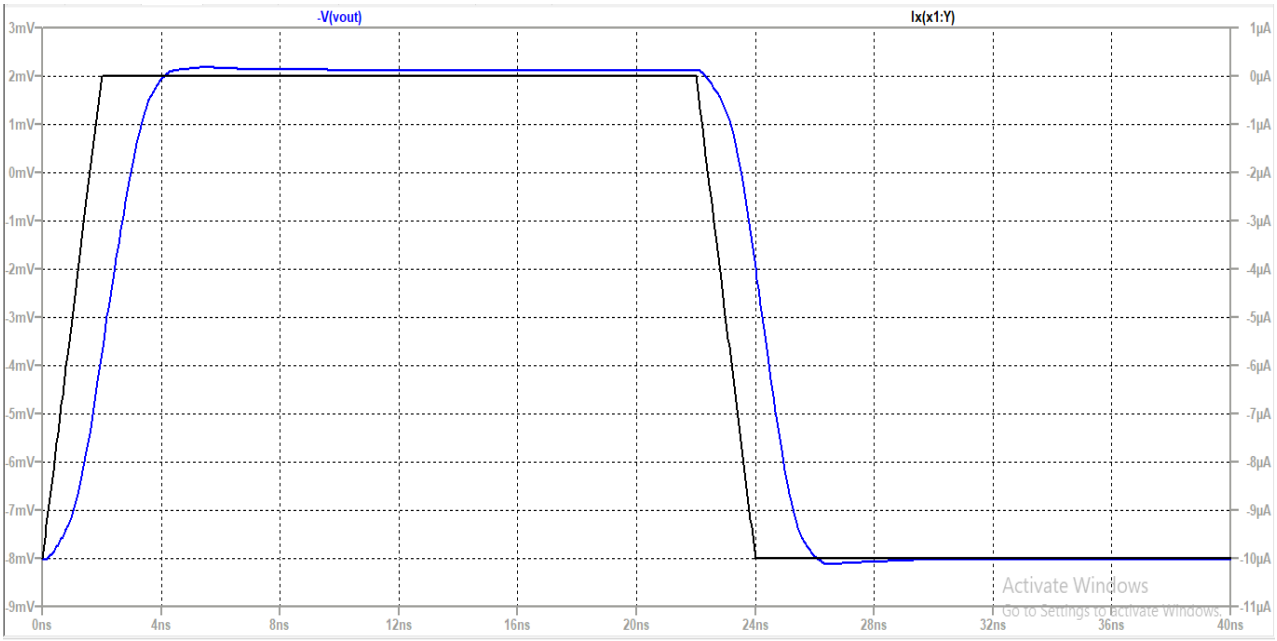

Fig. 3.6: Step response of I to V converter

- Calculation of the impedance gain of I to V converter from the above step response.

Impedance gain(R) = V(Vout)/Ix(x1:Y)

R = 8mV/10uA = 0.8kohms .

3.3 Voltage Buffer

- Circuit Diagram of the voltage buffer circuit implemented by using VCII is given in Fig. 3.7. The voltage conveyer block used in the circuit is the circuit taken from Fig. 2.1 in chapter 2. The aspect ratio of all the PMOS transistors and NMOS transistors in the VCII+ circuit, are (40.5 μm/0.54 μm) and (13.5 μm/0.54 μm) respectively. The supply voltage given to the circuit is ±0.90 V. To plot the sinusoidal response, a sine waveform having frequency of 1 kHz and amplitude of 200 mV peak to peak is given as input to the circuit. To plot the frequency response, the gain is plotted as a function of frequency using logarithmic scale.

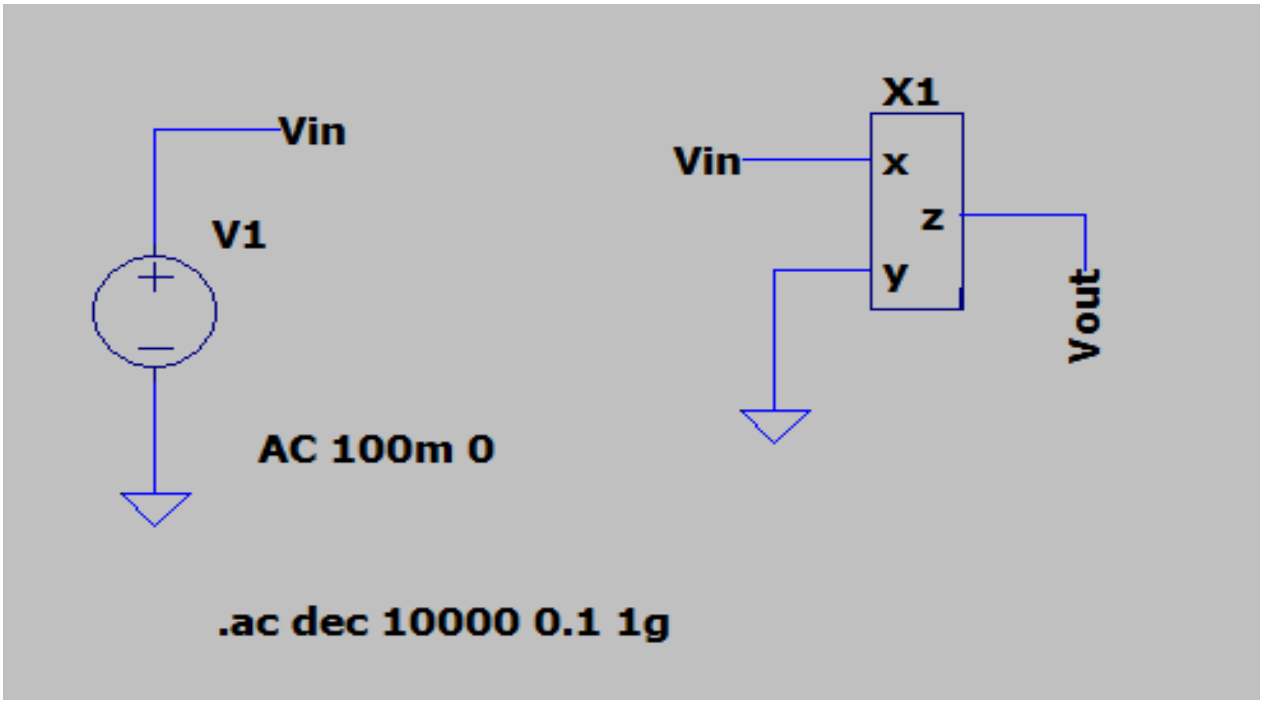

Fig. 3.7: Voltage Buffer circuit

The input voltage is provided to terminal X of the VCII block and output voltage is taken from the Z node of VCII block. The functionality of the voltage conveyer circuit enables the voltage at the x node to reflect at z node. The corresponding current at the x terminal will be transferred to the y terminal according to the voltage conveyer action.

- Transient or the sinusoidal response of the V to I circuit can be observed in Fig. 3.8.

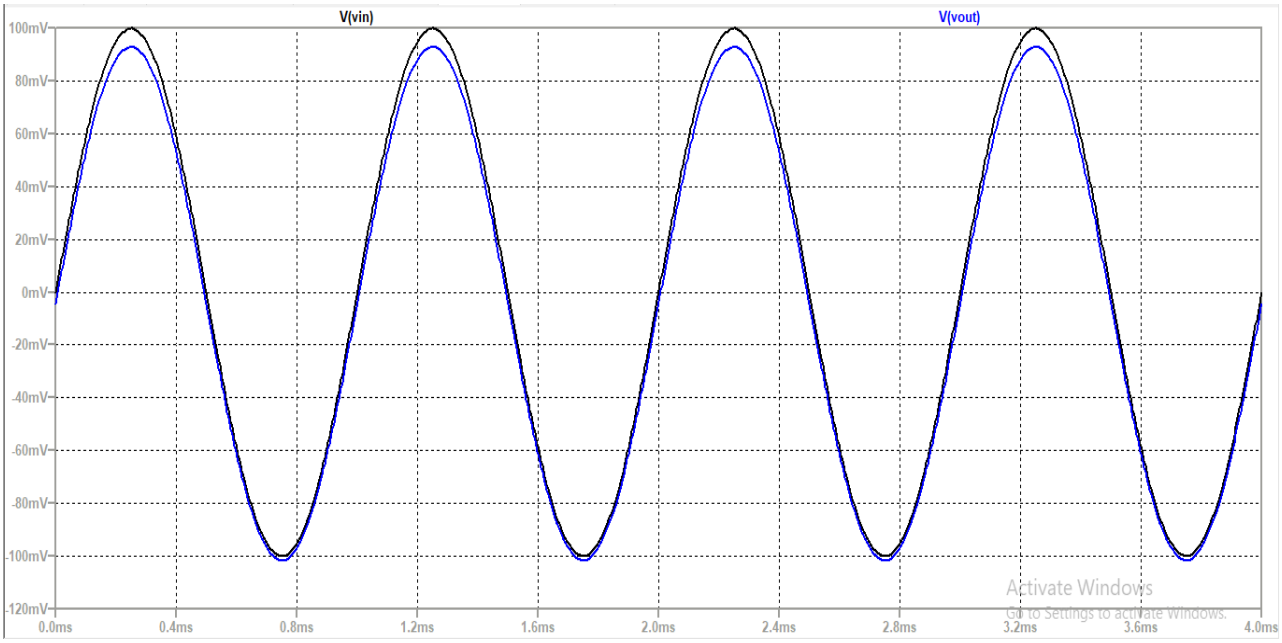

Fig. 3.8: Sinusoidal response of Voltage buffer circuit

- The frequency response of the Voltage buffer circuit can be observed in Fig. 3.9.

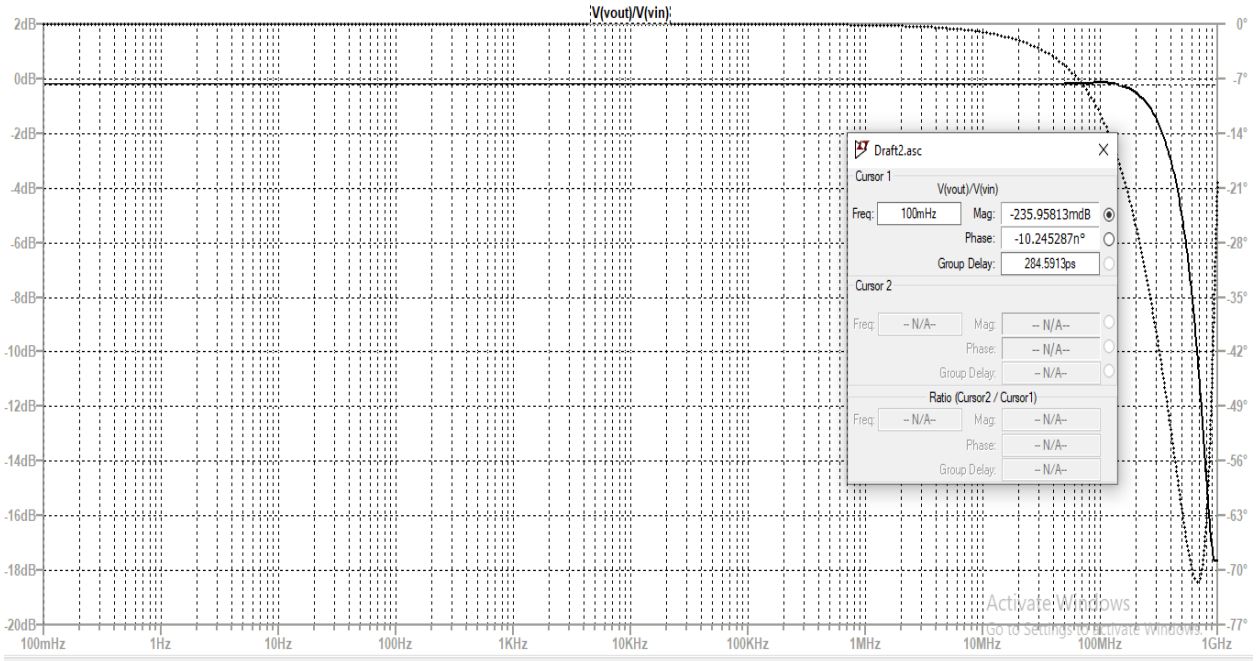

Fig. 3.9: Frequency response of Voltage buffer

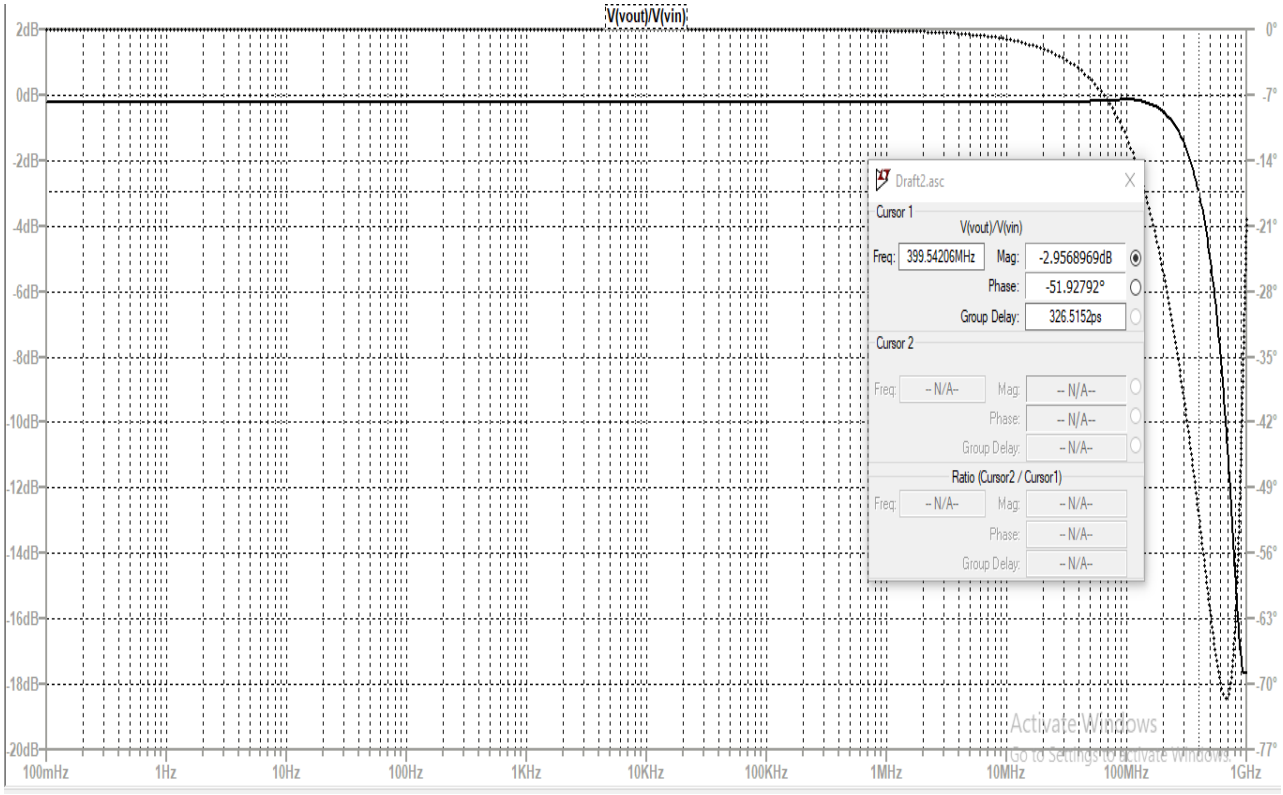

Fig. 3.10: -3 dB Bandwidth of Voltage buffer frequency response

- Calculation of the intrinsic voltage gain of voltage buffer circuit and the -3 dB bandwidth from the above frequency response.

Intrinsic voltage gain(α) = Vout/Vin = -235.95 mdB = 0.9726.

-3 dB bandwidth = 399.54 MHz.

3.4 Current Buffer

- Circuit Diagram of the current buffer circuit implemented by using VCII is given in Fig 3.11. The voltage conveyer block used in the circuit is the circuit taken from Fig 2.1 in chapter 2. The aspect ratio of all the PMOS transistors and NMOS transistors in the VCII+ circuit, are (40.5 µm/0.54 µm) and (13.5 µm/0.54 µm) respectively. The supply voltage given to the circuit is ±0.90 V. To plot the sinusoidal response, a sine waveform having frequency of 1 KHz and amplitude of 20 µA peak to peak is given as input to the circuit. To plot the frequency response, the gain is plotted as a function of frequency using logarithmic scale.

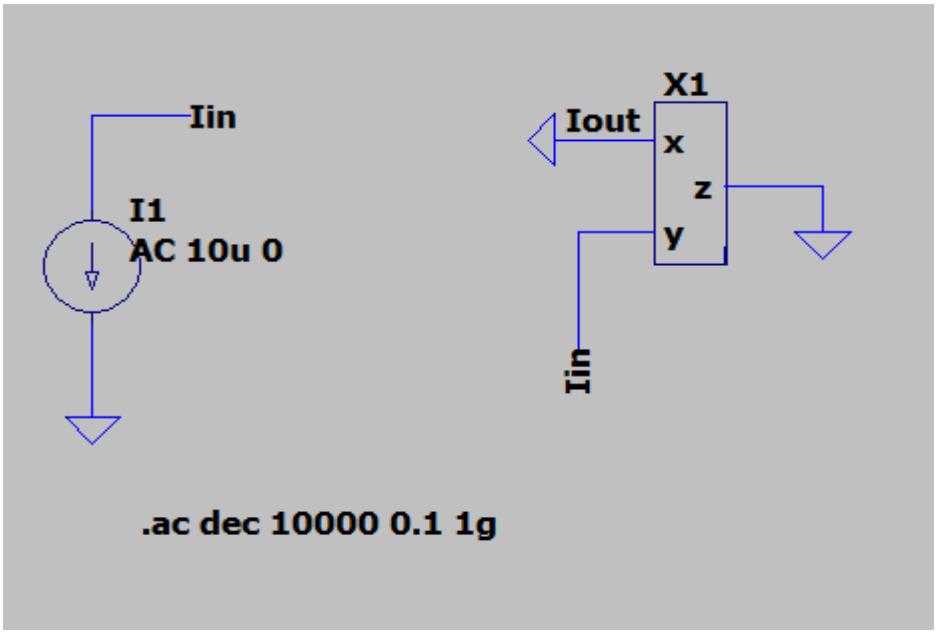

Fig. 3.11: Current Buffer circuit

The input current is provided to terminal Y of the VCII block and output current is taken from the nodal current of X node of VCII block.

- Transient or the sinusoidal response of the V to I circuit can be observed in Fig. 3.12.

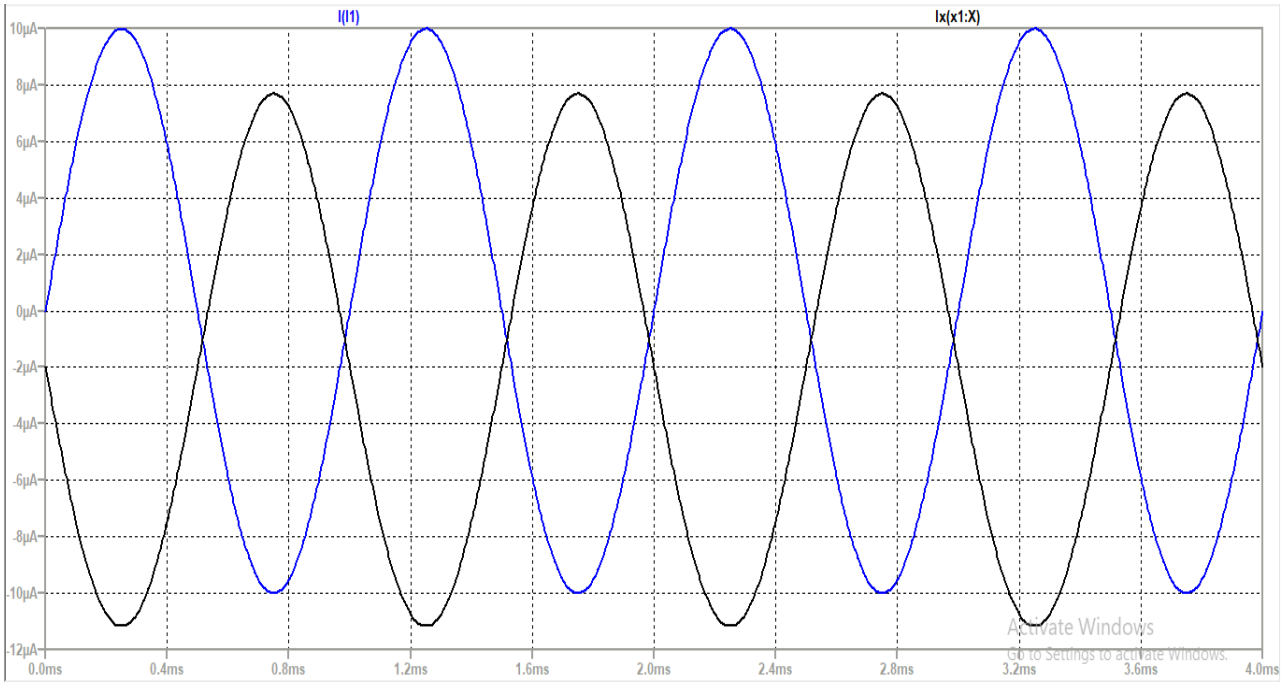

Fig. 3.12: Sinusoidal response of current buffer circuit

- The frequency response of the Voltage buffer circuit can be observed in Fig 3.13.

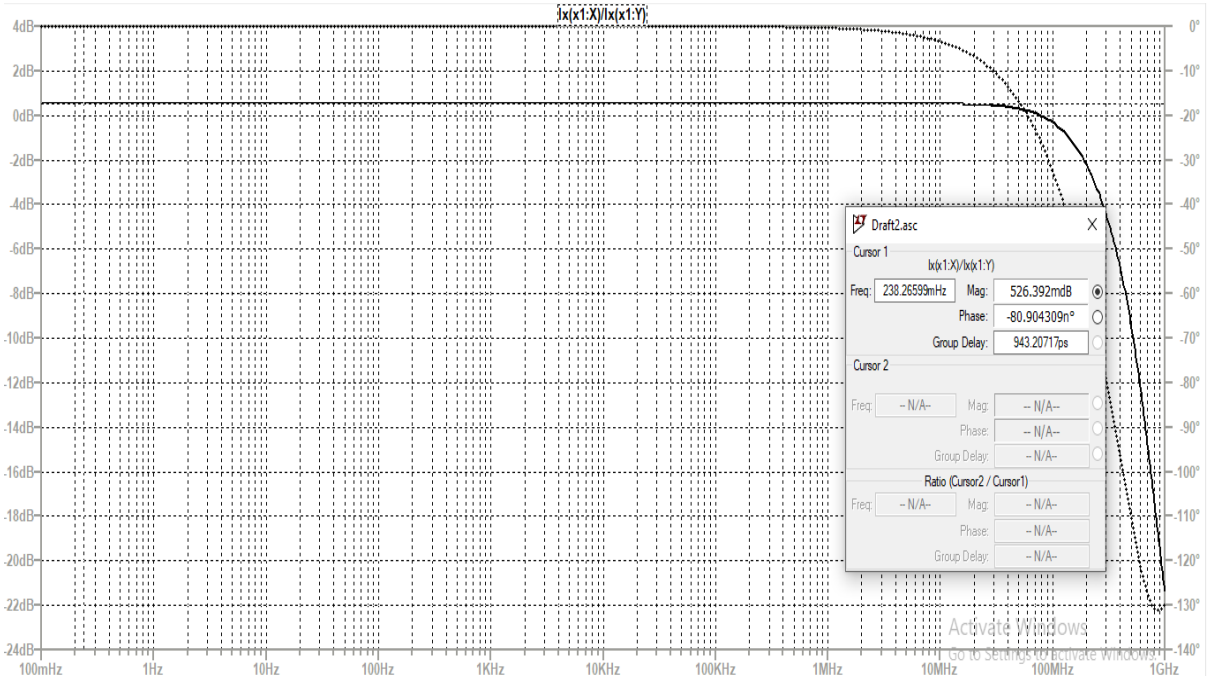

Fig. 3.13: Frequency response of Current buffer

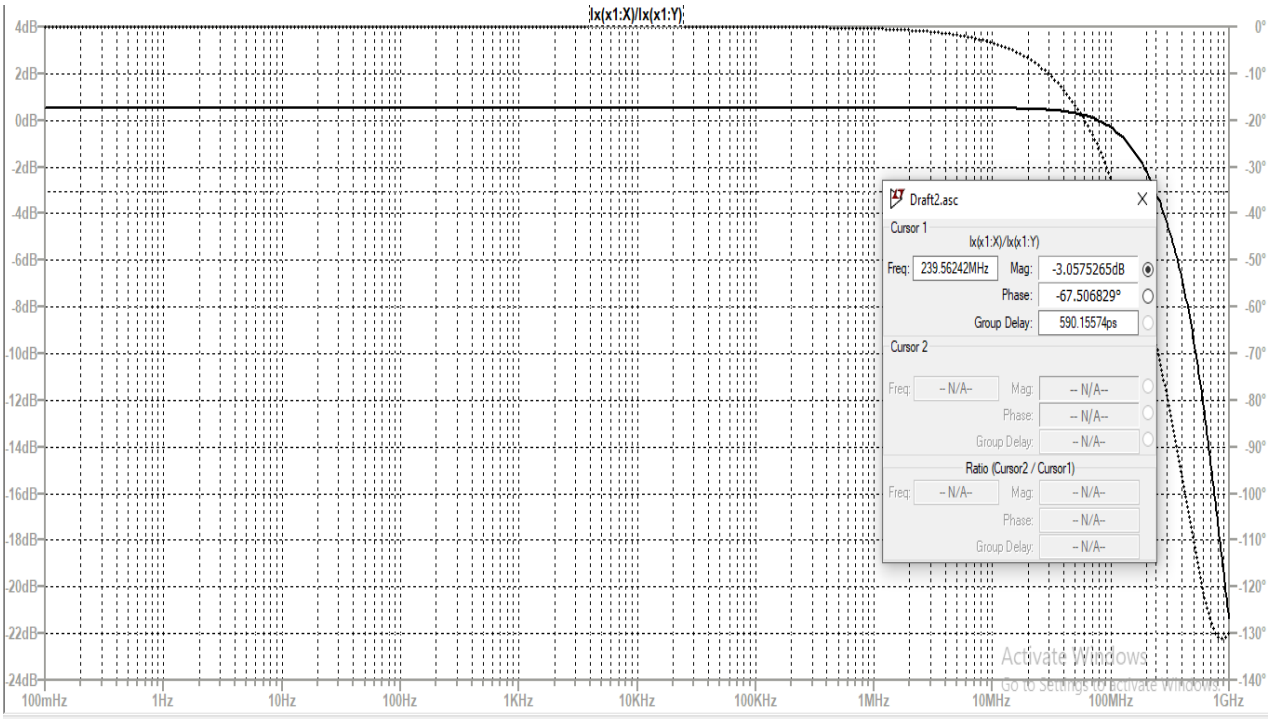

Fig. 3.14: -3 dB Bandwidth of Current buffer frequency response

- Calculation of the intrinsic voltage gain of voltage buffer circuit and the -3 dB bandwidth from the above frequency response.

Intrinsic current gain(β) = Iout/Iin = 526.392 mdB = 1.034.

-3 dB bandwidth = 239.56 MHz.

3.5 Summarized results

The intrinsic parameters calculated from the above applications can be summarized in the table 3.1.

Table 3.1: Intrinsic parameters calculation

Parameters	Values
Impedance gain	0.8 kΩ
Transconductance gain	1.2 mS
Intrinsic voltage gain (-3 dB Bandwidth)	0.9726(399.54 MHz)
Intrinsic current gain (-3 dB Bandwidth)	1.034(239.56 MHz)

Chapter 4

Applications of VCII : Voltage Differentiator and Voltage Integrator

The applications of VCII discussed in Chapter 3, such as voltage buffer, current buffer, etc. are all linear analog circuits implemented through second generation voltage conveyer block. The application of VCII in implementing analog circuits in linear domain can be further extended to voltage differentiator and voltage integrator.

The output of a voltage differentiator circuit is essentially a derivative of the input signal waveform, which is spread over a frequency range. The bandwidth of its operation is dependent on the values of passive components such as resistor, capacitor and inductor. Typically, the frequency response of a first order voltage differentiator circuit is a high pass response. The voltage differentiator circuit is implemented by using a number of techniques such as using passive components as a network of resistor and capacitor, active blocks such as OPAMP, OTRA, CCII, etc.

A voltage integrator circuit outputs time integral of the input signal over a frequency range. The bandwidth of its operation is dependent on the values of passive components such as resistors, capacitors and inductors. Typically, the frequency response of a first order integrator circuit is a low pass response. The voltage integrator circuit is implemented by using a number of techniques such as using passive components as a network of resistor and capacitor, active blocks such as OPAMP, OTRA, CCII, etc.

In this chapter, voltage differentiator circuit and voltage integrator circuit based on second generation voltage conveyer (VCII) have been discussed and implemented using schematic simulation tool LT Spice with 0.18-μm CMOS technology. The circuit of VCII block is the same as illustrated in Fig. 2.1, chapter 2. The supply voltage is a constant ±0.90 V.

The performance parameters of each circuit have been critically and comprehensively analyzed. The mid band gain and bandwidth of the circuit have been calculated from the frequency response and the characteristics of frequency response has been validated.

The functionality of both differentiator and integrator circuit have also been validated using input waveforms in form of pulsed waveform. The input waveform to the differentiator circuit is a pulsed waveform having time period of 8 us, rise time and fall time of 1 us and 1 us respectively and amplitude of 425 mV. The input waveform to integrator circuit is a pulsed waveform having time period of 100 ns, with negligible rise time and fall time and amplitude of 425 mV. The entity X1 used in all the circuit diagrams represents VCII+ circuit, as illustrated in Fig. 2.1, chapter 2.

4.1 Voltage differentiator

- Circuit diagram of VCII based voltage differentiator circuit is given in Fig. 4.1.

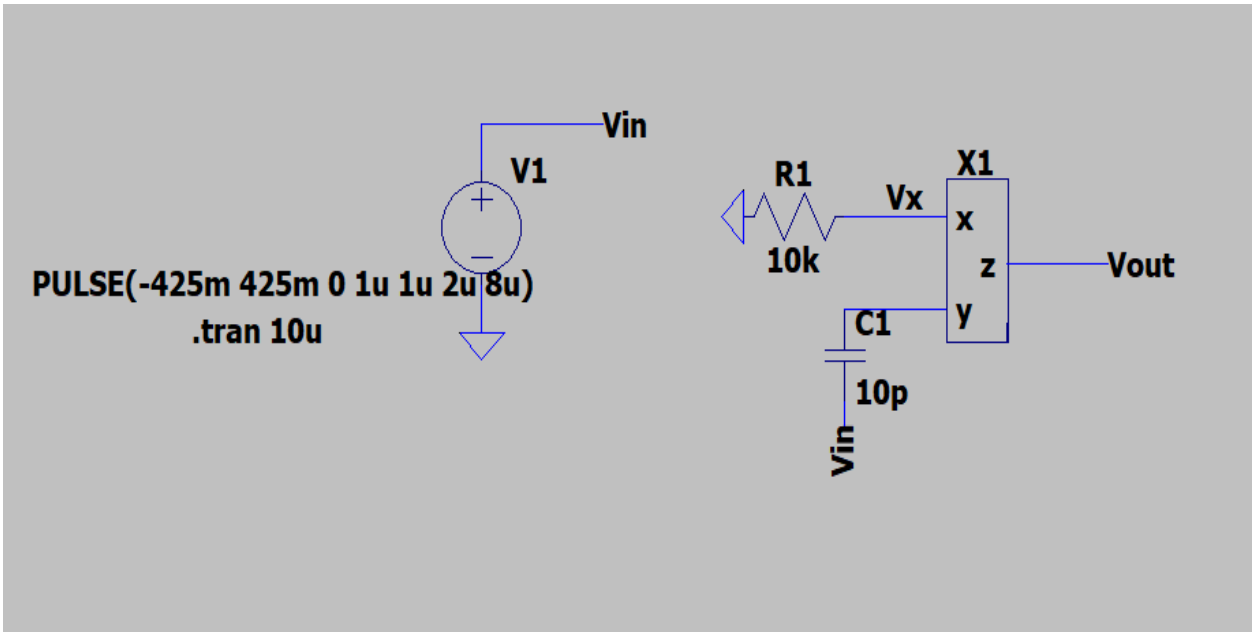

Fig. 4.1: Voltage differentiator circuit

- The output waveform of the VCII based voltage differentiator circuit is given in Fig. 4.2.

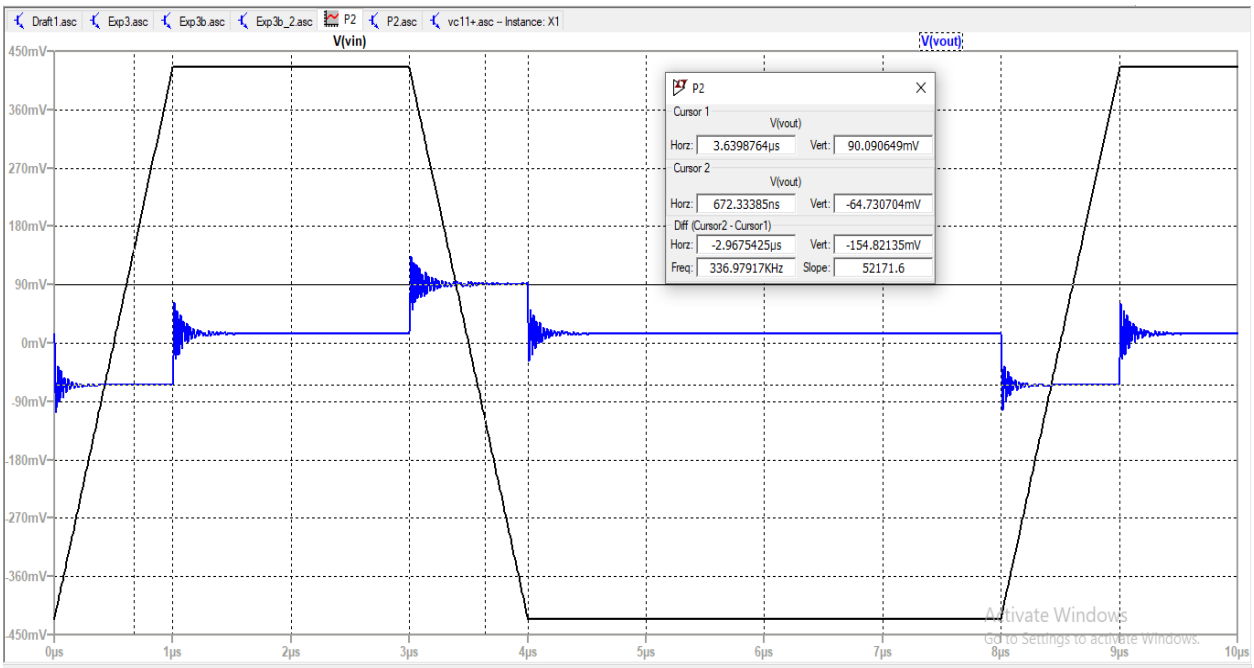

Fig. 4.2: Output waveform of voltage differentiator

- The frequency response of the voltage differentiator circuit is given in Fig. 4.3.

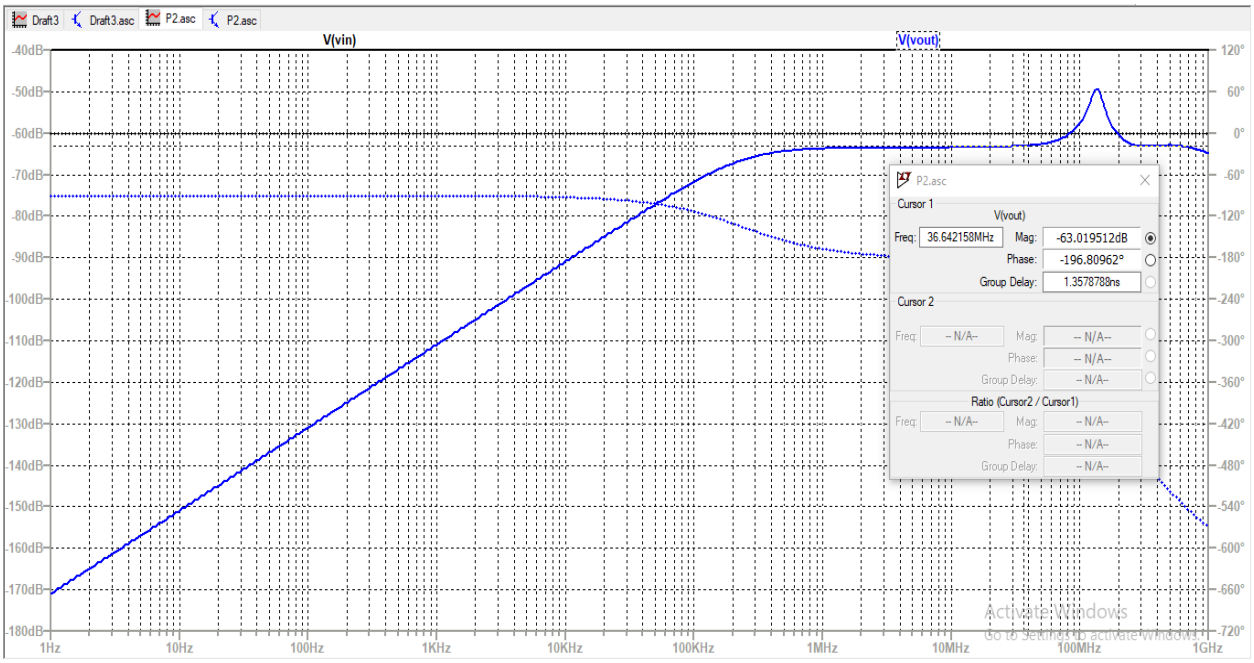

Fig. 4.3: Frequency response of voltage differentiator

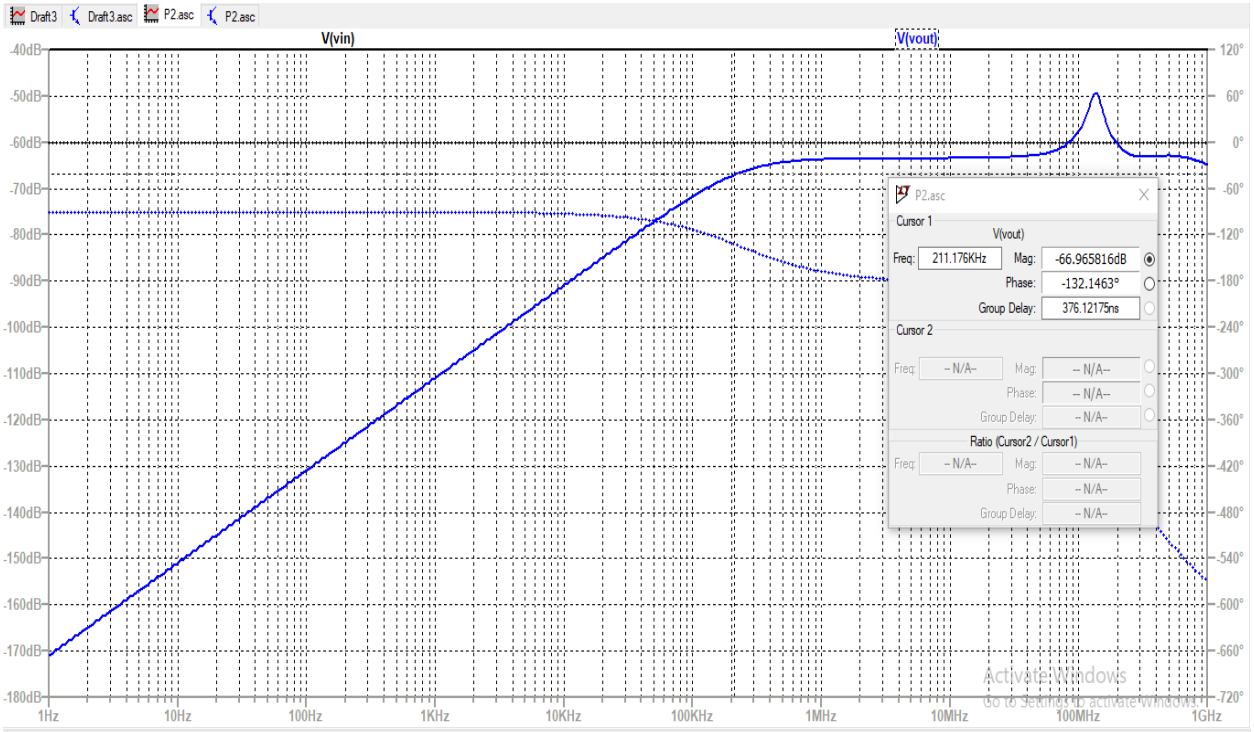

Fig. 4.4: Cut off frequency of voltage differentiator

Mid band voltage gain = -63.44 dB

Cut off frequency = 211.17 KHz.

4.2 Voltage integrator

- Circuit diagram of the voltage integrator circuit implemented using VCII is given in Fig. 4.5.

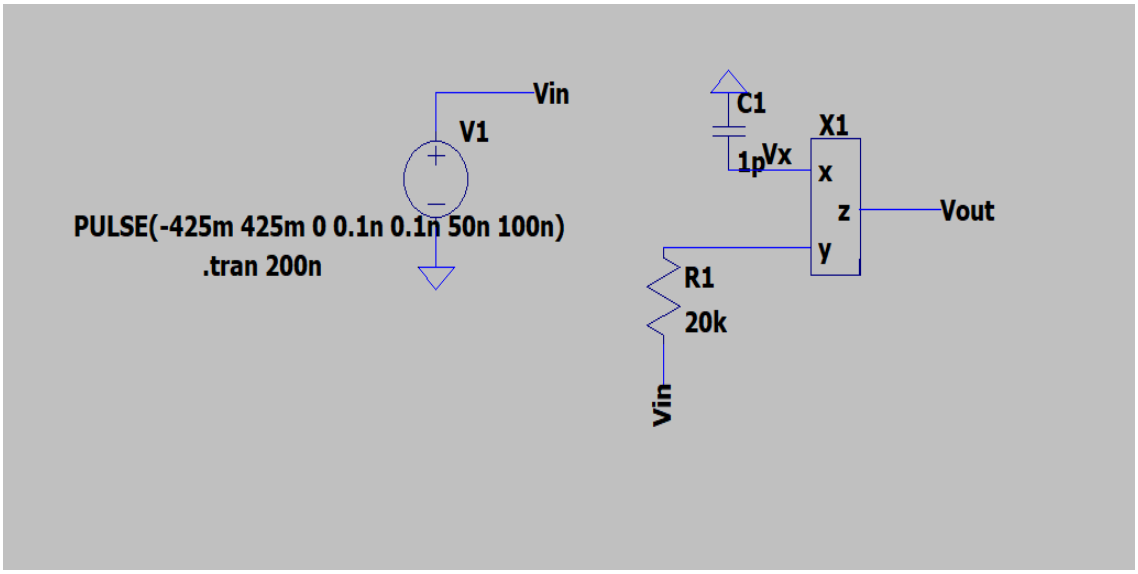

Fig. 4.5: Voltage integrator circuit

- The output waveform of the voltage integrator is given in Fig. 4.6.

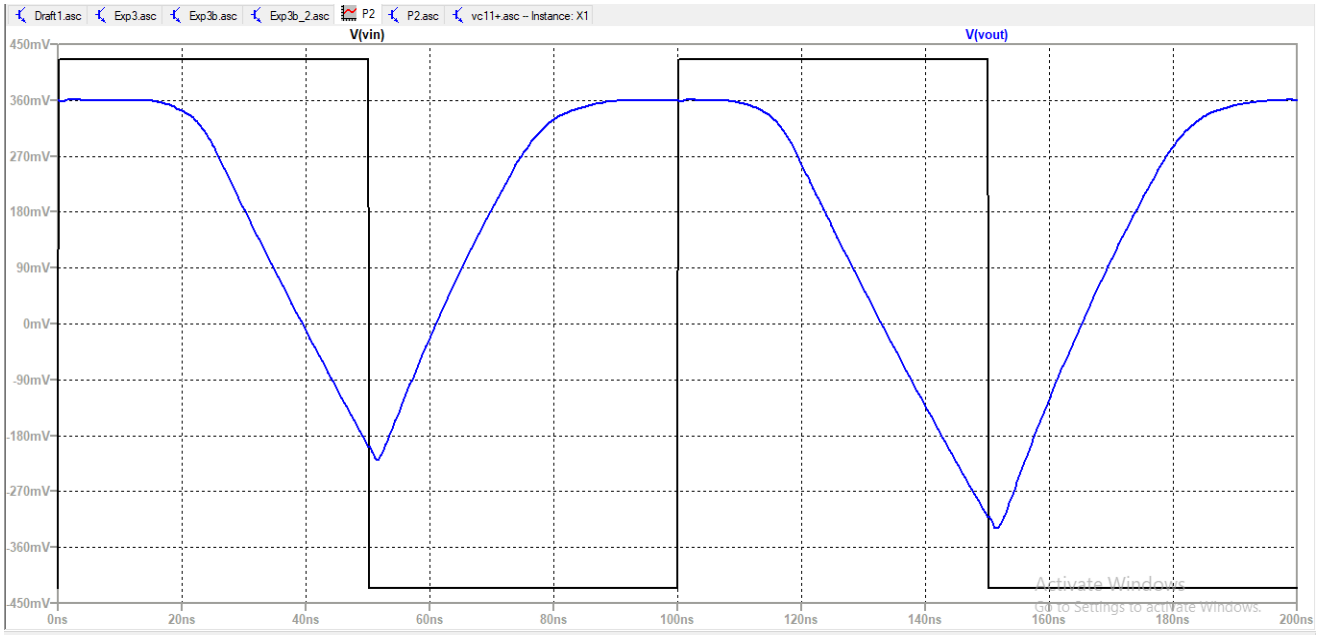

Fig. 4.6: Output waveform of voltage integrator

- The frequency response of the voltage integrator circuit is given in Fig. 4.7.

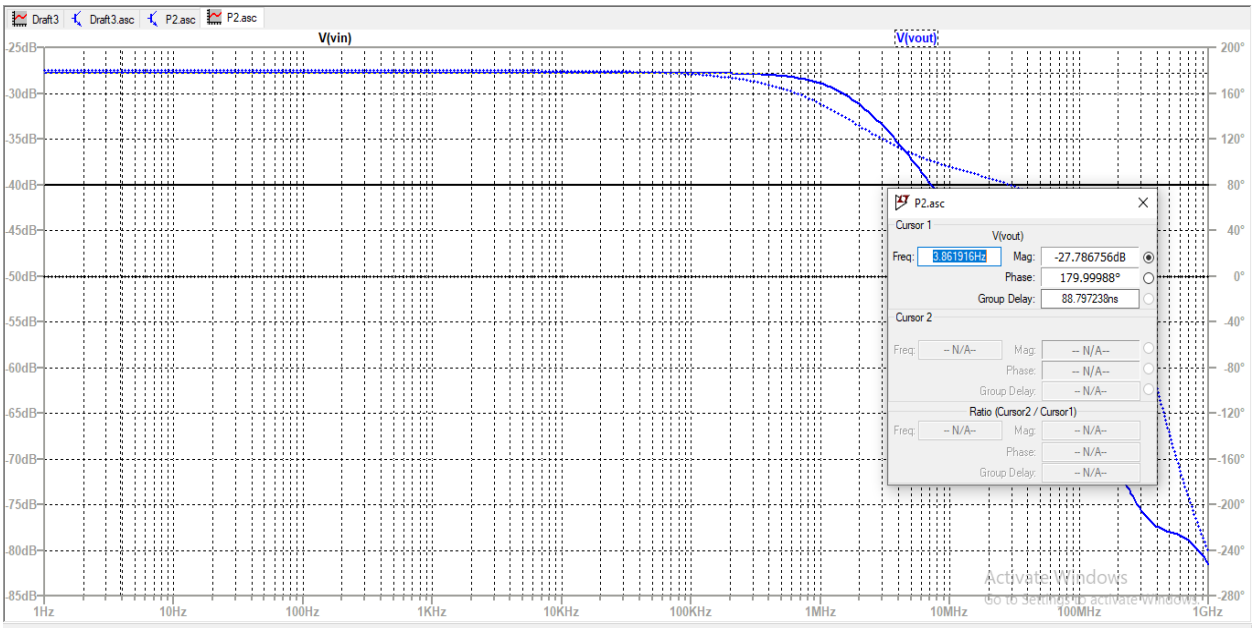

Fig. 4.7: Frequency response of voltage integrator

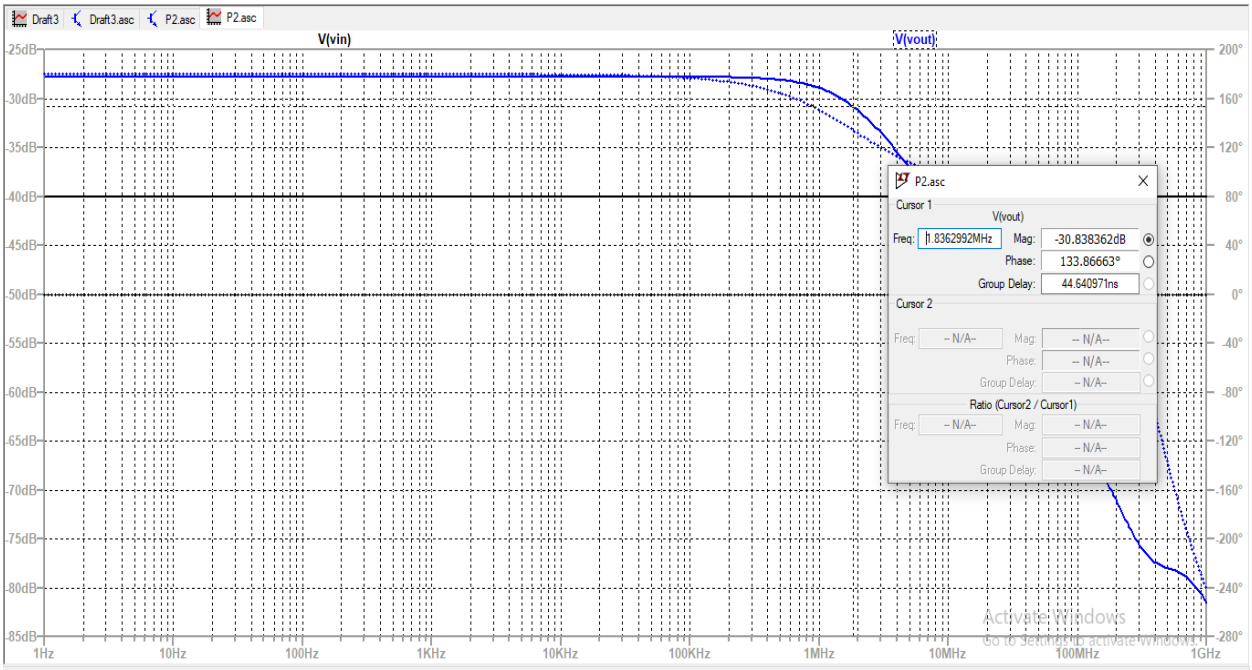

Fig. 4.8: Cut off frequency of voltage integrator

Mid band voltage gain = -27.63 dB.

Cut off frequency = 1.136 MHz.

Chapter 5
Application of VCII : Schmitt Trigger

Schmitt triggers are one of a kind of comparator circuits which find wide range usage in signal conditioning applications. It is a kind of a hysteresis comparator in which a positive feedback is established between the output port and the non inverting input port of the comparator . [1][2] The Schmitt trigger is a special analog circuit that converts analog input signal to a digital output signal. A triggering action enables the output signal to change, this trigger comes in the form of threshold values in the input signal. Output signal of the circuit changes only when the triggering condition occurs, until then it remains constant. The output is low when the input is below a separate (lower) selected threshold, and it preserves its value when the input is between the two thresholds. Hysteresis refers to the Schmitt trigger's dual threshold action, which implies that it has memory. The duty cycle of the output pulsed waveform is dependent on the triggering operation of the Schmitt trigger. This triggering operation of Schmitt trigger is used to implement many signal conditioning modules and techniques.

5.1 Implementation of Comparator using VCII

A prospective comparator circuit has been designed using second generation voltage conveyer circuit and this circuit can also find application as a zero crossing detector for any input waveform. The circuit diagram of the proposed comparator using second generation voltage conveyer block is illustrated in Fig. 5.1. Comparators are used to compare to voltage levels and generates an output of pulsed depending on the logic at which it operated. A basic comparator has two terminals, a positive terminal and negative terminal.

A dual input positive logic comparator compares both the inputs and if the input voltage level at the positive terminal is higher than the input voltage level at the negative terminal, it gives output as logic high, and vice versa. The comparator circuit using a second-generation voltage conveyer is designed using two blocks, one of the VCII+ and the other of VCII-. The blocks are connected using a series of feedback networks to establish a positive or negative feedback establishing a comparator operation. The output of the comparator circuit will be pulse in nature and maximum rate of change in the output voltage is required for comparison. This parameter also has a direct influence on the switching time of the logic. The comparator executed using voltage conveyer has substantially shorter switching time than the comparator executed using operational amplifiers.

5.2 **Circuit Diagram of Comparator**

In the comparator circuit illustrated in Fig.4, the input voltage supply is given as a sinusoidal wave having amplitude of 500 mV and frequency of 1 kHz. The passive components used in the circuit are three resistors, the values of resistors R1, R2, and R3 is 12 kΩ, 15 kΩ, and 15 kΩ. The active building blocks of the comparator are VCII- and VCII+. The operation of the circuit will enable the z terminal of VCII- to give non inverted square waveform as output having the same frequency as the sinusoidal input waveform. The z terminal of the VCII+ block will give a square waveform with inverted logic as output.

The operation of this comparator can also be further extended using different input waveforms. A triangular waveform having frequency of 1 kHz is given as input to the Y terminal of VCII-.

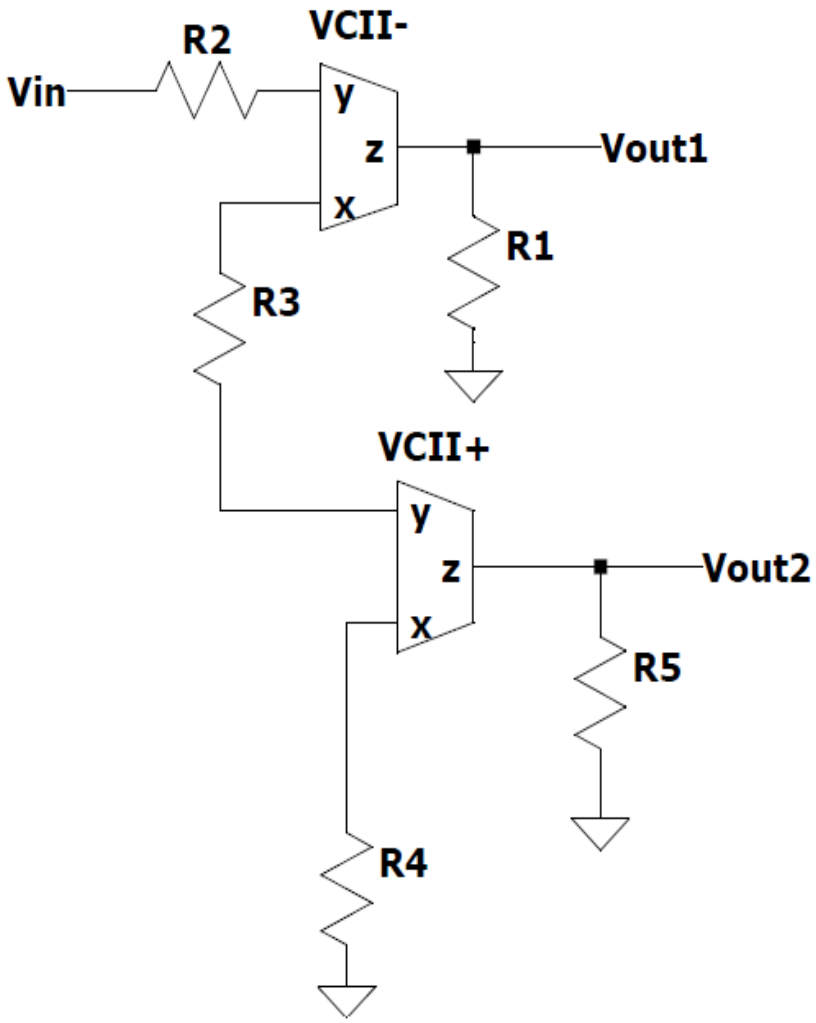

Fig. 5.1: Circuit diagram of VCII based comparator

The advantage of the comparator implemented by using second generation voltage conveyers is a better switching performance over comparator implemented using operational amplifier.

The functional advantage of implementing comparator using voltage conveyers is that both inverted and non inverted configurations of the output can be obtained using a single circuit without employing an inverter.

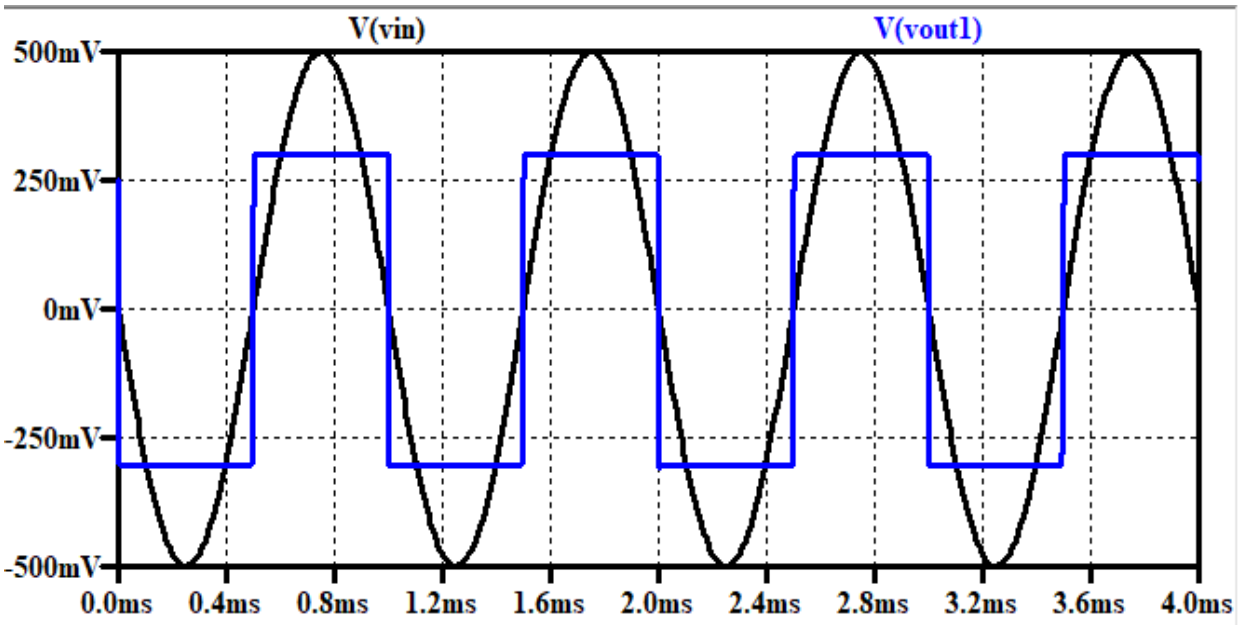

Fig. 5.2: Sinusoidal input and non inverted output waveform of the proposed comparator

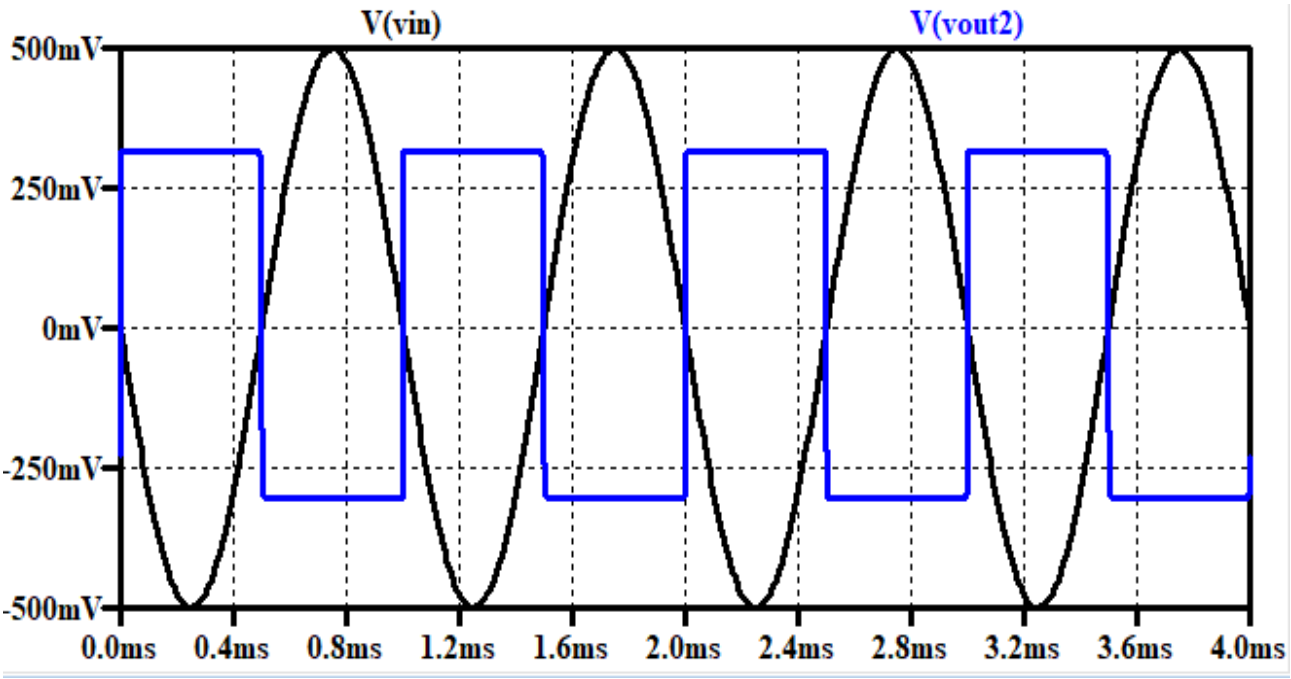

Fig. 5.3: Sinusoidal input and inverted output waveform of the proposed comparator

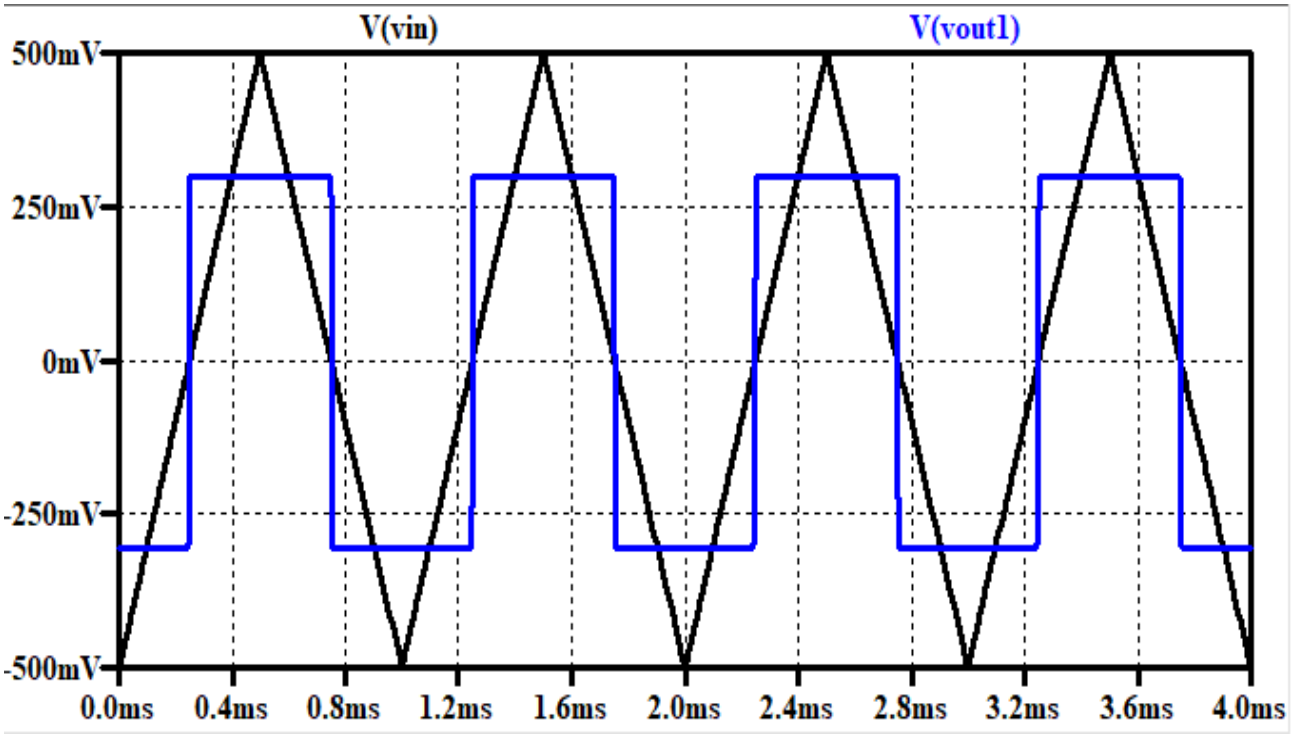

Fig. 5.4: Triangular input and non inverted output waveform of the proposed comparator

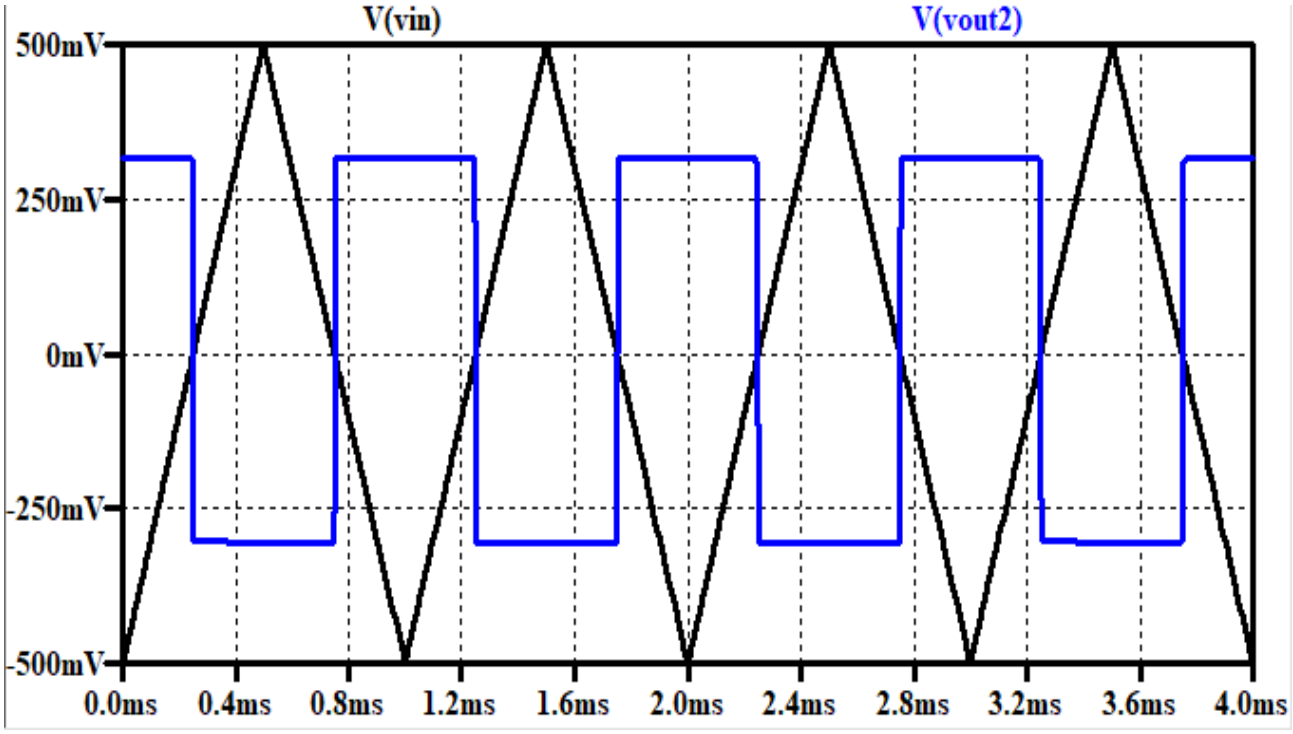

Fig. 5.5: Triangular input and inverted output waveform of the proposed comparator

A major advantage of implementing comparators using voltage conveyers is low power consumption and operating the comparator at low voltage supply. The switching performance is summarized in Table 5.1. The switching performance of the comparator has been analyzed over transitions in both the outputs i.e Vout1 and Vout2.

Table 5.1. Switching performance of the proposed comparator

Switching performance	**Transition in Vout1**	**Transition in Vout2**
Average transition delay (μs)	2.65	2.64
Average power consumption (μW)	328	365

The advantage of the comparator implemented by using second generation voltage conveyers is a better switching performance over comparator implemented using operational amplifier.

The functional advantage of implementing comparator using voltage conveyers is that both inverted and non inverted configurations of the output can be obtained using a single circuit without employing an inverter.

5.3 Implementation of Schmitt Trigger using VCII

The proposed Schmitt trigger using a second-generation voltage conveyer is designed using two blocks, one of the VCII+ and the other of VCII-. The blocks are connected using a series of feedback networks to establish a positive or a negative feedback establishing a comparator operation. The feedback loop is established via the output terminal of the VCII- block in order to initiate positive feedback.

It is important that the parasitic components should also be considered in the operation of Schmitt trigger as it will propagate non ideality within the device thus causing variations in the operation of the circuit. Consider the parasitic resistance and parasitic capacitance at the X terminal of VCII- block to be Rx and Cx respectively. Consider the parasitic resistances at Y terminal and Z terminal of VCII- block to be Ry and Rz respectively. The effects of parasitics can be observed in transient characteristics as well as in transfer characteristics of the Schmitt trigger circuit. The mathematical analysis also gives deep insight into effect of parasitics on operation of the circuit. Thus it is important to design the circuit keeping in consideration the factors contributing to non ideality within the circuit.

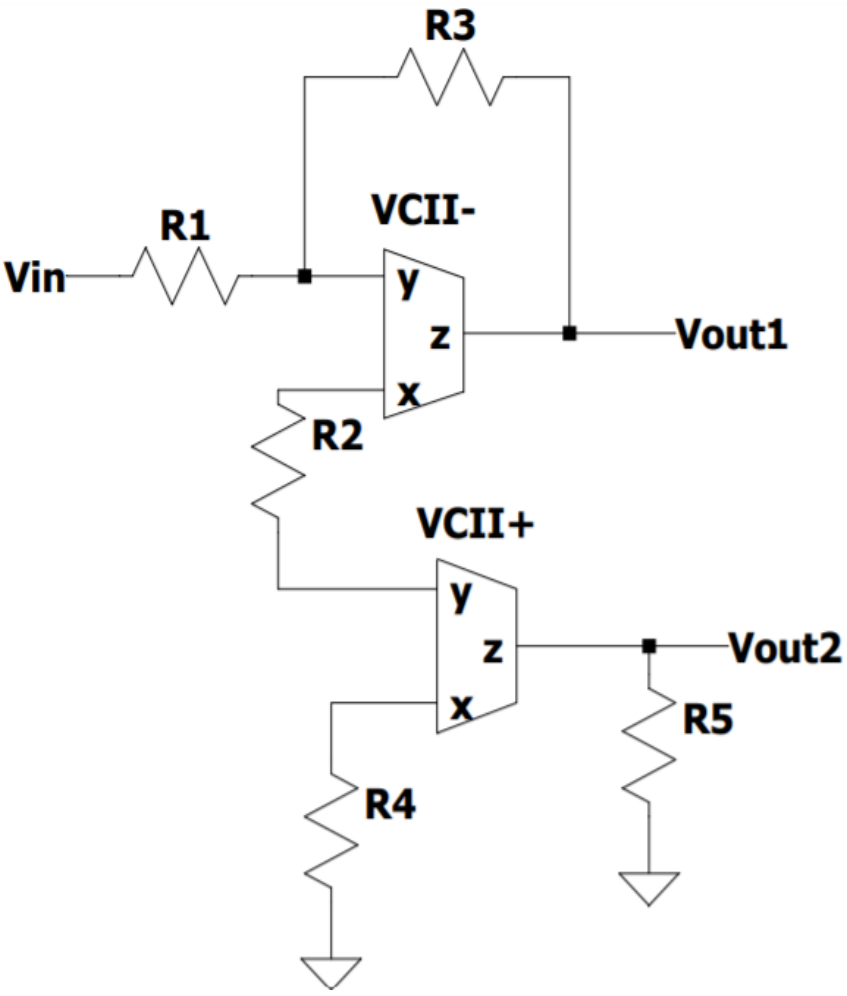

Fig 5.6: VCII based Schmitt trigger circuit

As seen in Fig.9, a feedback loop is established between output of the VCII- block and the y terminal of the VCII- block. Kirchhoff's current law can be used to determine current flowing through the Y terminal of VCII-. As the parasitic resistance across the Z terminal is very low, the voltage drop across the z terminal that occurs due to parasitic resistance Rz is very less.

$$\frac{(Vout1-IyRy)}{R3} - \frac{(Vin-IyRy)}{R1} = \text{Iy} \qquad (5.1)$$

$$\text{Iy} = \frac{\left(\frac{Vout1}{R3} - \frac{Vin}{R1}\right)}{\left(1+\frac{Ry}{R1}-\frac{Ry}{R3}\right)} \qquad (5.2)$$

The current generated at the y terminal will be transferred to the x terminal of VCII- block. This will generate a voltage at the x terminal across resistance R2.

$$Ix = -\beta Iy \qquad (5.3)$$

$$Ix = -\beta \frac{\left(\frac{Vout1}{R3} - \frac{Vin}{R1}\right)}{\left(1+\frac{Ry}{R1}-\frac{Ry}{R3}\right)} \qquad (5.4)$$

$$Vx = -\beta \left\{\frac{\left(\frac{Vout11}{R3} - \frac{Vin}{R1}\right)}{\left(1+\frac{Ry}{R1}-\frac{Ry}{R3}\right)}\right\}\left\{\frac{R2\left(\frac{1}{sCx+\frac{1}{Rx}}\right)}{\left(R2+\frac{1}{sCx+\frac{1}{Rx}}\right)}\right\} \qquad (5.5)$$

The voltage produced at the X terminal of the VCII- block will be transferred to the Z terminal of the VCII+ block through the voltage conveyer action.

$$Vz = -\alpha\beta \left\{\frac{\left(\frac{Vout1}{R3} - \frac{Vin}{R1}\right)}{\left(1+\frac{Ry}{R1}-\frac{Ry}{R3}\right)}\right\}\left\{\frac{R2\left(\frac{1}{sCx+\frac{1}{Rx}}\right)}{\left(R2+\frac{1}{sCx+\frac{1}{Rx}}\right)}\right\} \qquad (5.6)$$

The saturation voltage for both the positive and negative cycle is calculated in (5.7).

$$Vz = \alpha\beta \left\{\frac{\left(\pm\frac{Vout1}{R3} + \frac{Vin}{R1}\right)}{\left(1+\frac{Ry}{R1}-\frac{Ry}{R3}\right)}\right\}\left\{\frac{R2\left(\frac{1}{sCx+\frac{1}{Rx}}\right)}{\left(R2+\frac{1}{sCx+\frac{1}{Rx}}\right)}\right\} \qquad (5.7)$$

Consider the output voltage of VCII- block Vout1, can acquire the values $+V_{sat}$ for the positive cycle and $-V_{sat}$ for the negative cycle. The ± sign indicates output saturation voltage for negative and positive cycle respectively. The values of resistances will determine the value of saturation voltage and the threshold voltages for both positive and negative cycle.

$$Vout1 = \alpha\beta \left\{\frac{\left(\pm\frac{R1}{R3}Vsat + Vin\right)}{\left(1+\frac{Ry}{R1}-\frac{Ry}{R3}\right)}\right\} R1 \left\{\frac{R2\left(\frac{1}{sCx+\frac{1}{Rx}}\right)}{\left(R2+\frac{1}{sCx+\frac{1}{Rx}}\right)}\right\} \qquad (5.8)$$

The operation of the proposed Schmitt trigger can be determined through (5.8). The term V_{sat} can be simplified as in (5.9).

$$Vout1 = k\,(Vin \pm cV_{sat}) \qquad (5.9)$$

This will initiate a triggering action in the device and the saturation voltage is governed by the factors k and c whereas the hysteresis voltage is governed by the factor c, where k= $\alpha\beta R1 \left\{ \frac{R2\left(\frac{1}{sCx+\frac{1}{Rx}}\right)}{\left(R2+\frac{1}{sCx+\frac{1}{Rx}}\right)} \right\} \left\{ \frac{1}{\left(1+\frac{Ry}{R1}-\frac{Ry}{R3}\right)} \right\}$ and c = $\frac{R1}{R3}$.

The ± sign indicates positive and negative threshold voltages respectively. Let $+V_p$ be the positive threshold voltage and $-V_n$ be the negative threshold voltage of the proposed Schmitt trigger. The hysteresis voltage V_h can be computed as given in (13).

$$+V_p = +kcV_{sat} \quad (5.10)$$

$$-V_n = -kcV_{sat} \quad (5.11)$$

$$V_h = +V_p - (-V_n) = 2kcV_{sat} \quad (5.12)$$

The outputs of VCII- and VCII+ blocks will be mutually complementary in nature. The current at the X terminal of VCII- block will be transferred to the Y terminal of VCII+ block. The voltage generated at the X terminal of VCII+ block will be transferred to the output terminal i.e. Z terminal of the VCII+ block. The hysteresis voltage will be the same for the outputs of both VCII- and VCII+ blocks. A negative hysteresis is generated at the output terminal of VCII- block. The output terminal of VCII+ block will generate a positive hysteresis.

In the circuit illustrated in Fig.5, the input voltage is a sinusoidal waveform having frequency of 1 kHz and amplitude of 1V. The operation of Schmitt trigger is simulated over fixed values of passive components used in the circuit. The resistances used in the circuit R1, R2, R3, R4 and R5 have values 15 kΩ, 75 kΩ, 7.5 kΩ, 75 kΩ and 15 kΩ respectively. The output waveforms are generated over a time frame of 4 ms.

As seen in Fig.10 and Fig.11, the outputs of VCII- and VCII+ blocks are complementary in nature. The output at the z terminal of VCII- block produces a negative hysteresis and the output at the z terminal of VCII+ block produces a positive hysteresis.

The hysteresis curve has also been generated over a range of values for R1. The hysteresis voltage will change in accordance to the equation of hysteresis voltage illustrated in (5.12). However, the value of saturation voltage remains constant as it's dependency on R1 is negligible.

The impact of parasitic components in VCII blocks can be seen in the hysteresis curve wherein the parasitic impedance at the x terminal will impact the charging and discharging of the output voltage to the saturation point.

The impact of resistance R3 on hysteresis voltage can be summarized in Table 5.2. The hysteresis voltage V_h can be controlled through resistance R1 as illustrated in (5.12).

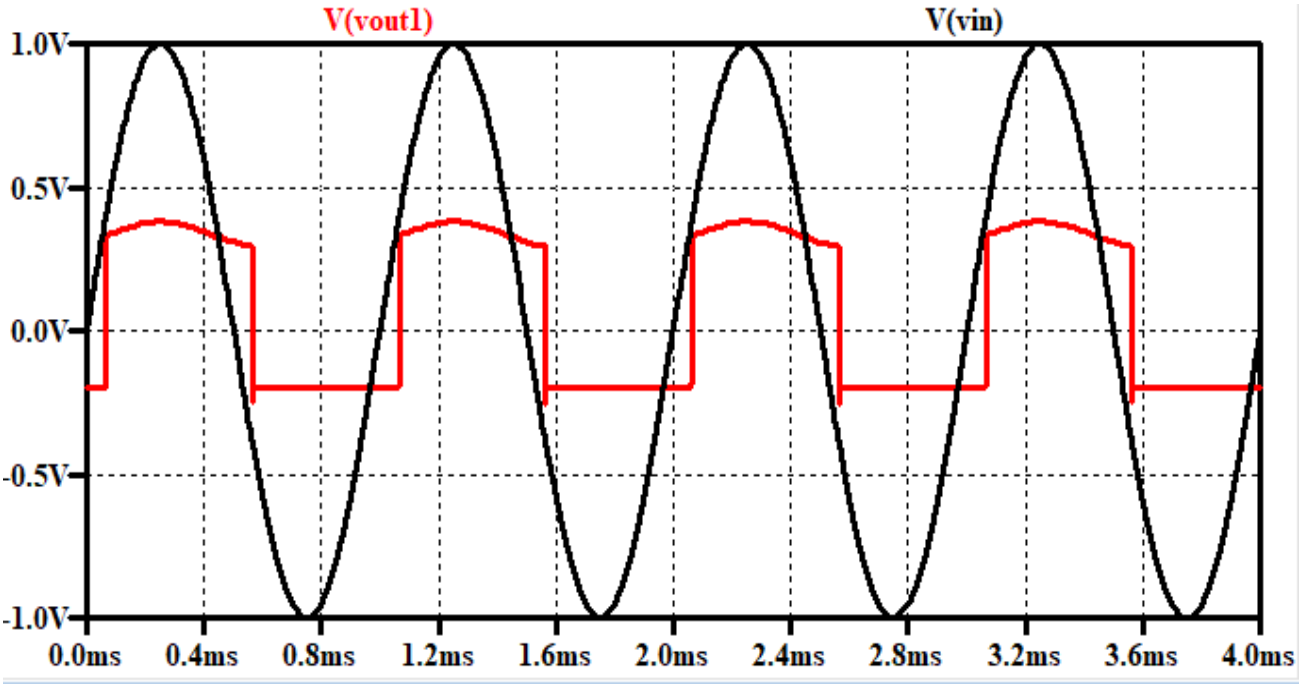

Fig. 5.7: Input and output waveform of the proposed Schmitt trigger having negative hysteresis

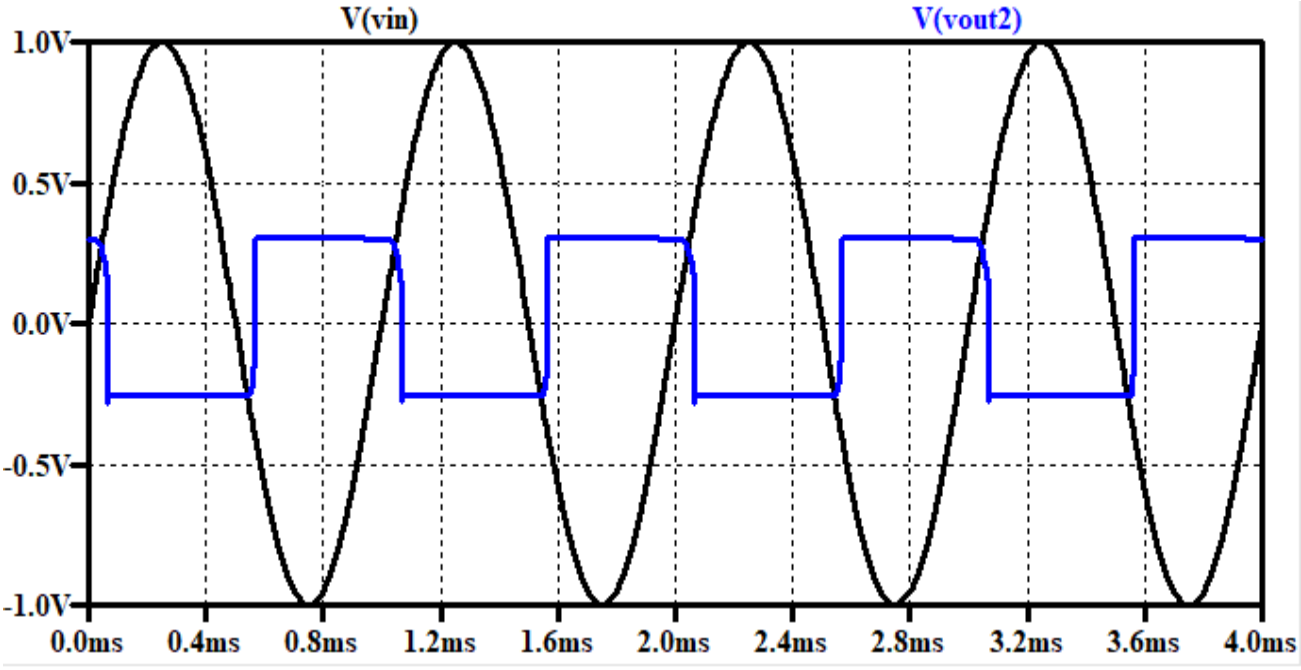

Fig. 5.8: Input and output waveform of the proposed Schmitt trigger having positive hysteresis

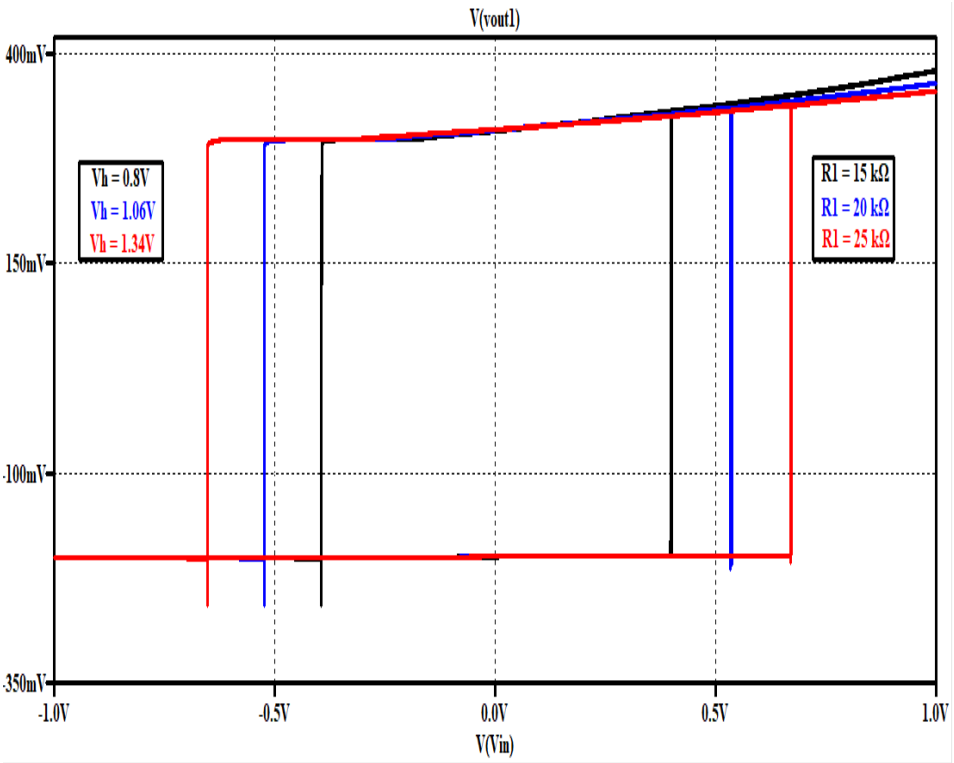

Fig. 5.9: Negative hysteresis curve

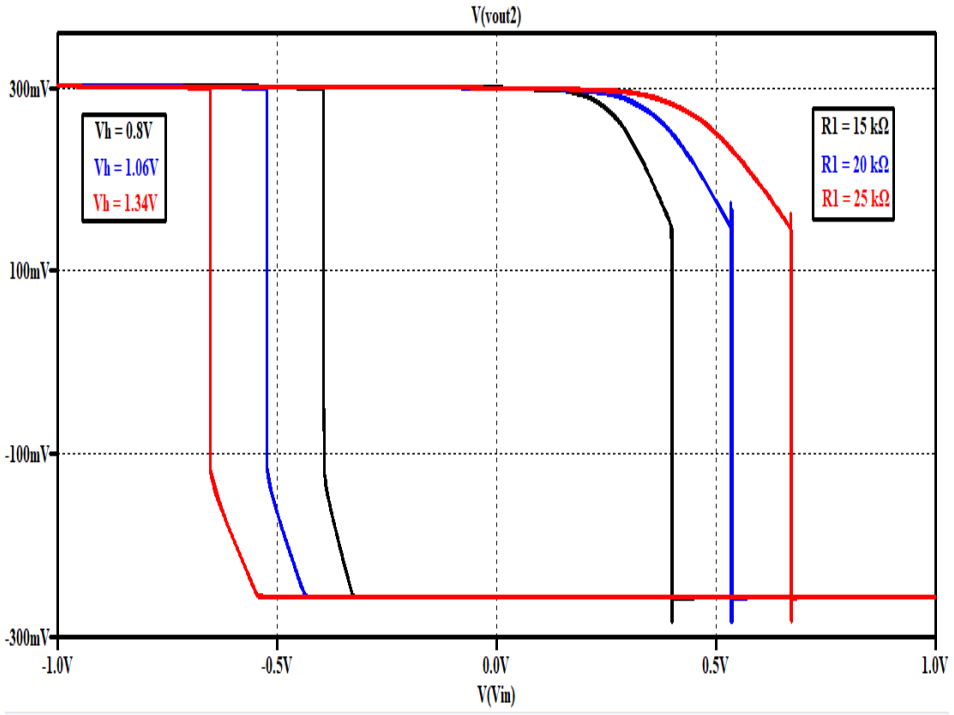

Fig. 5.10: Positive hysteresis curve

Table 5.2. Impact of resistance R1 on hysteresis voltage V_h

Resistance (R1)	**Hysteresis voltage (V_h)**
15 kΩ	0.8 V
20 kΩ	1.06 V
25 kΩ	1.34 V

Chapter 6

Application of VCII : Pulse Width Modulator

Pulse Width Modulators are frequently used in communication systems, DC motor speed control, instrumentation, etc. The internal circuitry involved in PWM generators available in Integrated Circuits (IC) form has high complexity and employs a number of different components such as flip flop, current sources, analog switches, etc. The PWM generator proposed through VCII has advantage of less complexity in circuit and lesser number of active components.

A pulse width modulator is implemented by using a carrier waveform which is used to break the modulating waveform into discrete parts. In this project, pulse width modulation has been implemented using a comparator to chop the modulating signal into discrete components. The modulating waveform is fed as input to the positive port of the comparator and the carrier waveform is fed to the negative port of the comparator. The output of the comparator is a pulse width modulated wave having time period same as that of the carrier wave. The duty cycle of the wave depends on the operation of comparator.

A generalized scheme of a pulse width modulator is depicted in Fig. 6.1. The carrier waveform and modulating signal are firstly summed up and then pulse width modulated signal is generated using the logic of dual port comparator.

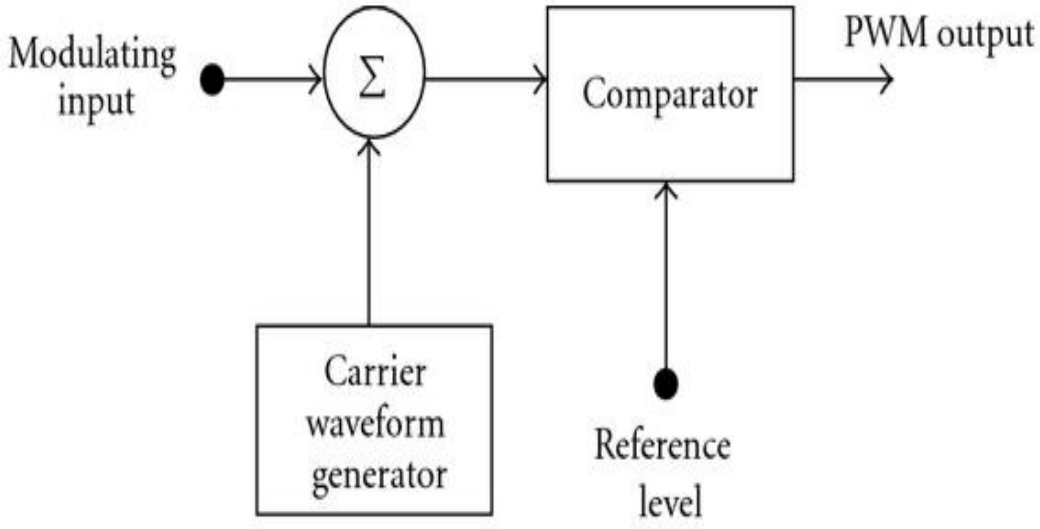

Fig.6.1: Scheme of PWM [11]

The proposed circuit can be analyzed as input voltage, Vin, being fed to the positive port of the comparator and negative reference voltage being fed to the negative port of the comparator, as illustrated in Fig. 6.2.

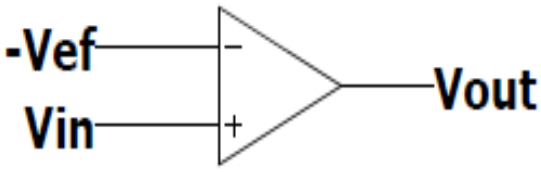

Fig.6.2: Dual Port Comparator

6.1 VCII based dual port comparator

The circuit diagram of the dual port comparator is illustrated in Fig. 6.3.

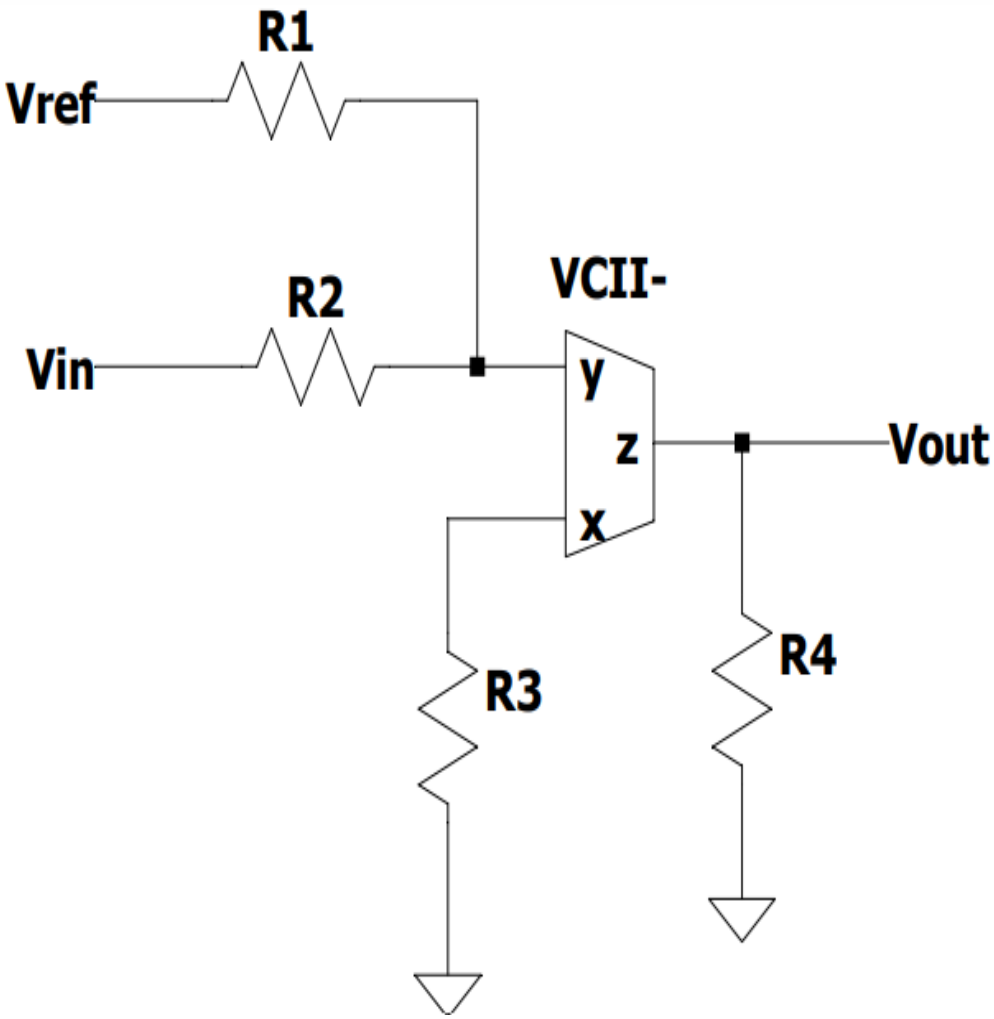

Fig..6.3: Circuit diagram of comparator implemented using VCII-

The operation of the comparator has been analyzed assuming that the parasitic components have negligible impact on the functionality of the circuit. The current across y terminal can be calculated by applying Kirchhoff's current law across y terminal node.

$$\frac{(Vref-IyRy)}{R2} - \frac{(Vin-IyRy)}{R1} = \text{Iy} \qquad (6.1)$$

$$\text{Iy} = \frac{\left(\frac{Vref}{R2} - \frac{Vin}{R1}\right)}{\left(1+\frac{Ry}{R2}-\frac{Ry}{R1}\right)} \qquad (6.2)$$

As the parasitic components have negligible effect on the operation of the circuit, Ry can be ignored in (6.2). The current generated at the y terminal will be transferred to the x terminal of VCII- block. This will generate a voltage at the x terminal across resistance R3.

$$Ix = -\beta Iy \qquad (6.3)$$

$$Ix = -\beta\left(\frac{Vref}{R2} - \frac{Vin}{R1}\right) \qquad (6.4)$$

$$Vx = -\beta \left\{\frac{Vref}{R2} - \frac{Vin}{R1}\right\} \left\{\frac{R3\left(\frac{1}{sCx+\frac{1}{Rx}}\right)}{\left(R3+\frac{1}{sCx+\frac{1}{Rx}}\right)}\right\} R3 \qquad (6.5)$$

The voltage produced at the X terminal of the VCII- block will be transferred to the Z terminal of the block through the voltage conveyer action. The parasitic components across the x terminals can be ignored in (6).

$$Vz = -\alpha\beta \left\{\frac{Vref}{R2} - \frac{Vin}{R1}\right\} R3 \qquad (6.6)$$

$$Vz = \pm\, \alpha\beta \left\{\frac{Vin}{R1} - \frac{Vref}{R2}\right\} R3 \qquad (6.7)$$

Considering the output voltage of VCII- block as Vout, it can acquire the values +Vsat for the positive cycle and -Vsat for the negative cycle. The ± sign, in (8), indicates output saturation voltage for positive and negative cycle respectively. The comparator will compare Vin with -Vref as it's logical operation.

The logic of the comparator is such that if the input voltage, Vin, is greater than the reference voltage, -Vref, the output of the comparator is +Vsat. If the input voltage, Vin, is less than the reference voltage, -Vref, the output of the comparator is -Vsat. The duty cycle of the pulsed waveform generated at the z terminal of VCII- block will depend upon the operation of the comparator and reference voltage level, Vref.

The operation of the comparator can be used to implement pulse width modulation using VCII block, as illustrated in *Fig.4* and *Fig.5*. The input voltage is the modulating signal, Vin, and the reference voltage is the carrier waveform, Vref.

6.2 Simulation Results and Analysis

The feasibility of the theoretical analysis of the proposed pulse width modulator circuit using VCII- block has been validated by spice simulations using 180-nm CMOS technology and ± 0.90 V supply voltage. The aspect ratio of all the PMOS transistors and NMOS transistors in the VCII- circuit, illustrated in Fig.2.2, chapter 2, are (40.5 μm/0.54 μm) and (13.5 μm/0.54 μm) respectively.

In the comparator circuit illustrated in Fig. 6.3, a sinusoidal wave having amplitude of 1V and frequency of 100 kHz is used as Vin. The value of resistors R1, R2, R3 and R4 is chosen as 1 kΩ, 1 kΩ, 15 kΩ and 15 kΩ respectively. The output voltage of the comparator has been represented as Vout1. The comparator output waveform for Vref of values -1.5V, -0.5V, 0V and 0.5V are depicted in Figs. 6.4 -6.7 respectively. In simulation results the reference voltage (Vref), has been signified as -Vref.

In Table 6.1, the variations in duty cycle with respect to change in reference voltage have been enlisted. It may be observed from the Table 6.1 that the simulated values of duty cycle are slightly different from the theoretically computed values.

The non ideality in observed duty cycle has been presented in Fig. 6.8. The variation in simulated and theoretical values may be attributed to due to the presence of parasitics in VCII- and the passive component tolerances.

The operation of this comparator is further extended to implement pulse width modulator by applying modulation signal and carrier wave at Vin and Vref respectively. For implementing the PWM scheme, a modulating sinusoidal signal is applied. Amplitude of the sinusoidal modulating signal is 1V and the frequency is 25 kHz. A triangular waveform having amplitude of 2V and frequency of 200 kHz is used as a carrier wave. The modulating signal, carrier wave and the modulated output waveforms are shown Fig. 6.9. The frequency spectrum of the modulating signal and the pulse width modulated waveform has been captured in Fig. 6.10 and Fig. 6.11 respectively. The peak of the frequency spectrum for the pulse width modulated wave is at 200 KHz, same as the frequency of the carrier waveform thus validating the PWM operation.

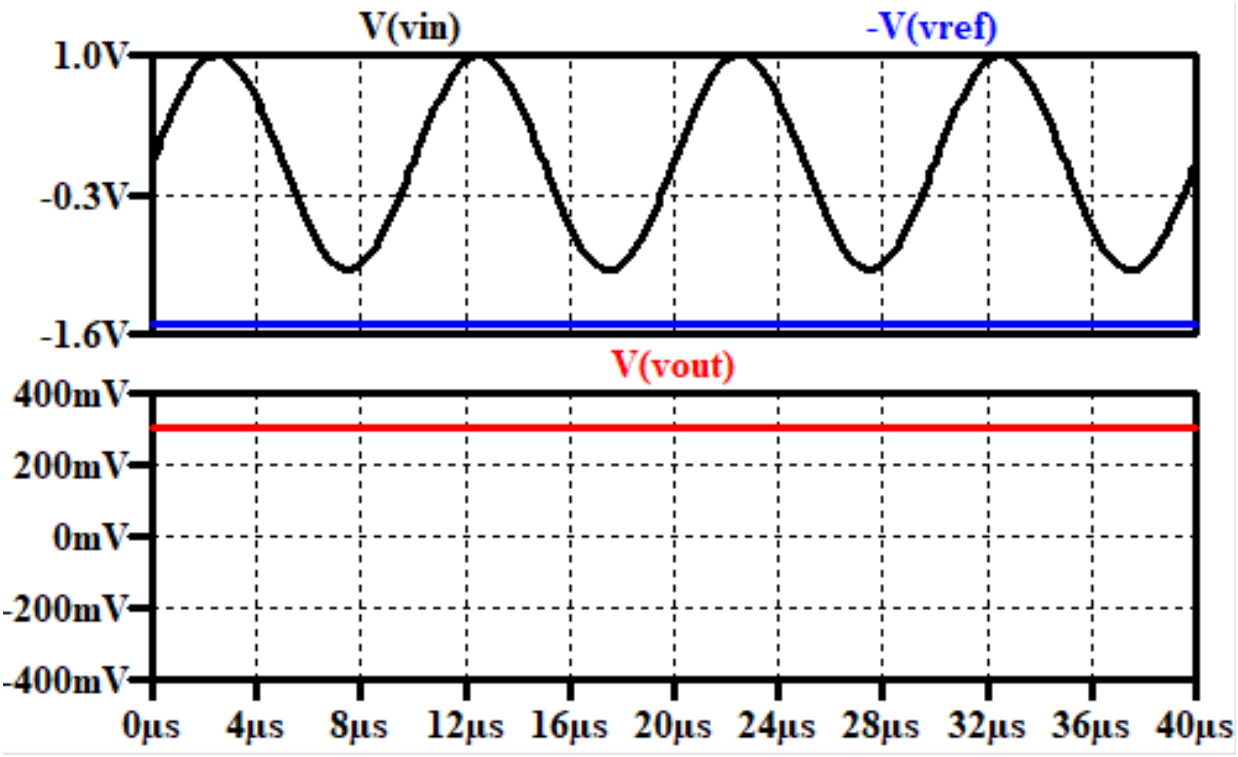

Fig.6.4 : Output waveform having 100% duty cycle

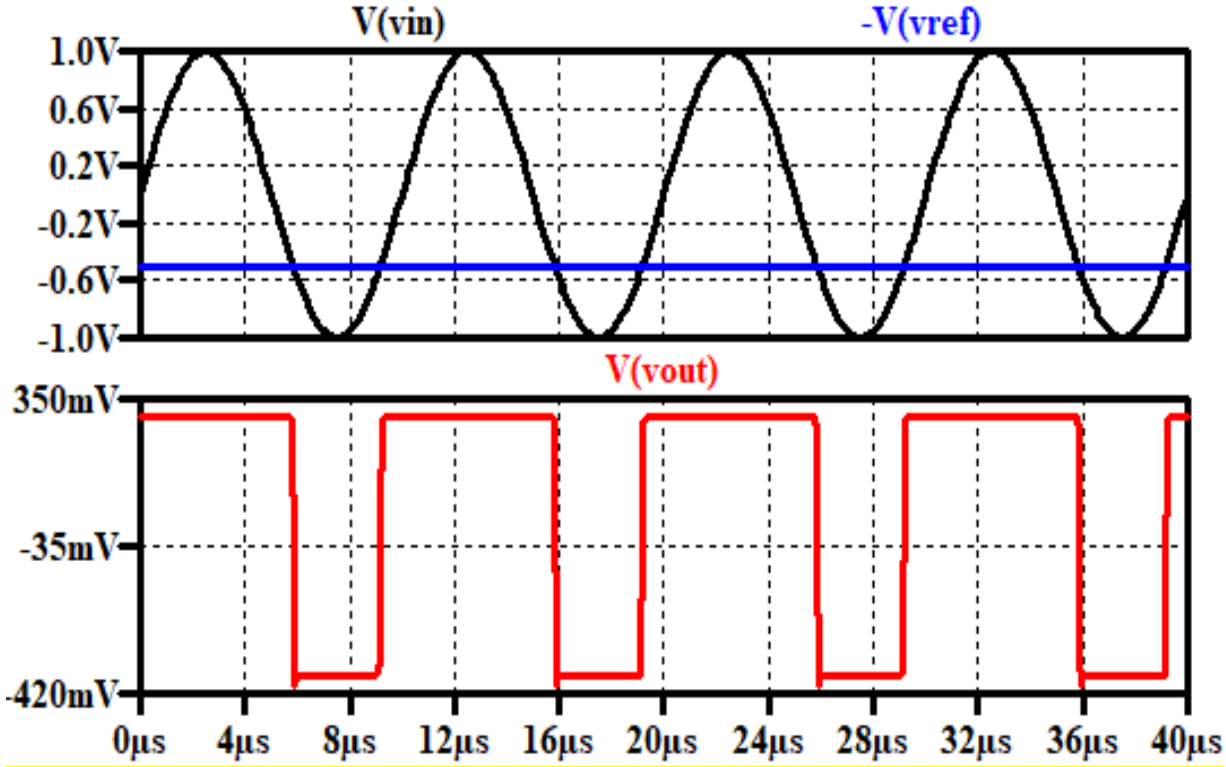

Fig.6.5 : Output waveform having 75% duty cycle

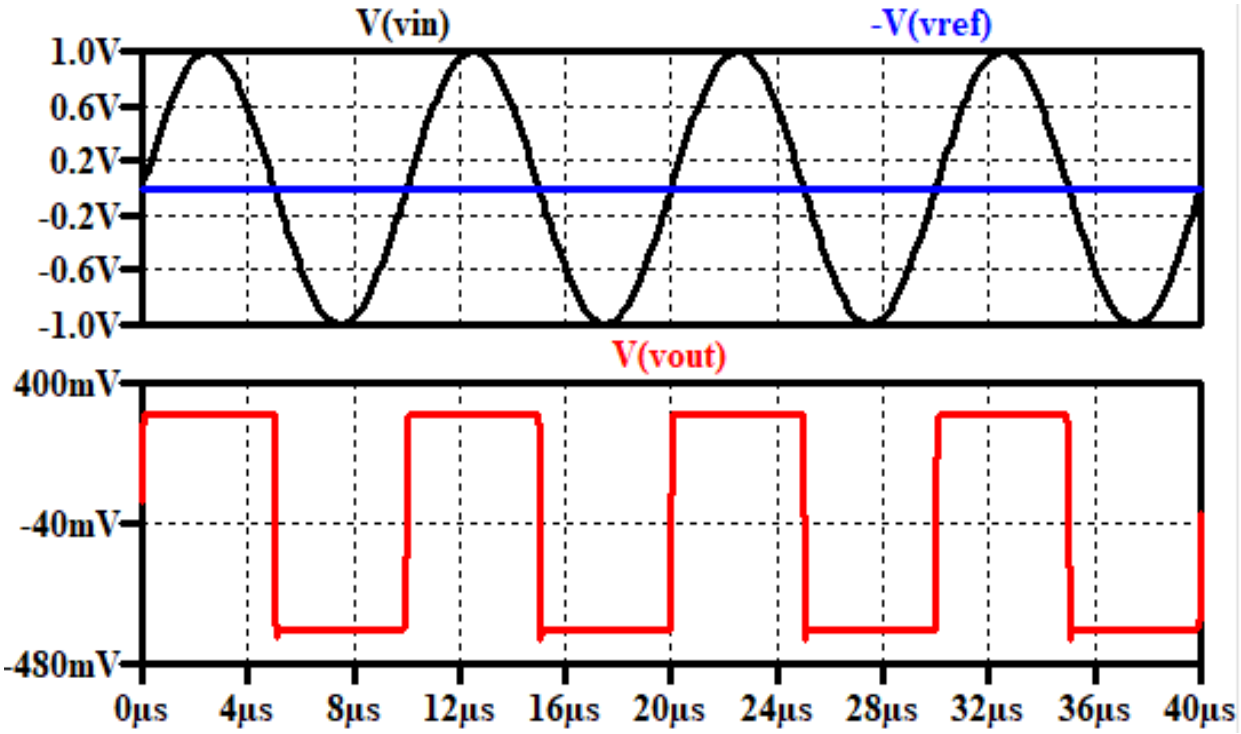

Fig.6.6 : Output waveform having 50% duty cycle

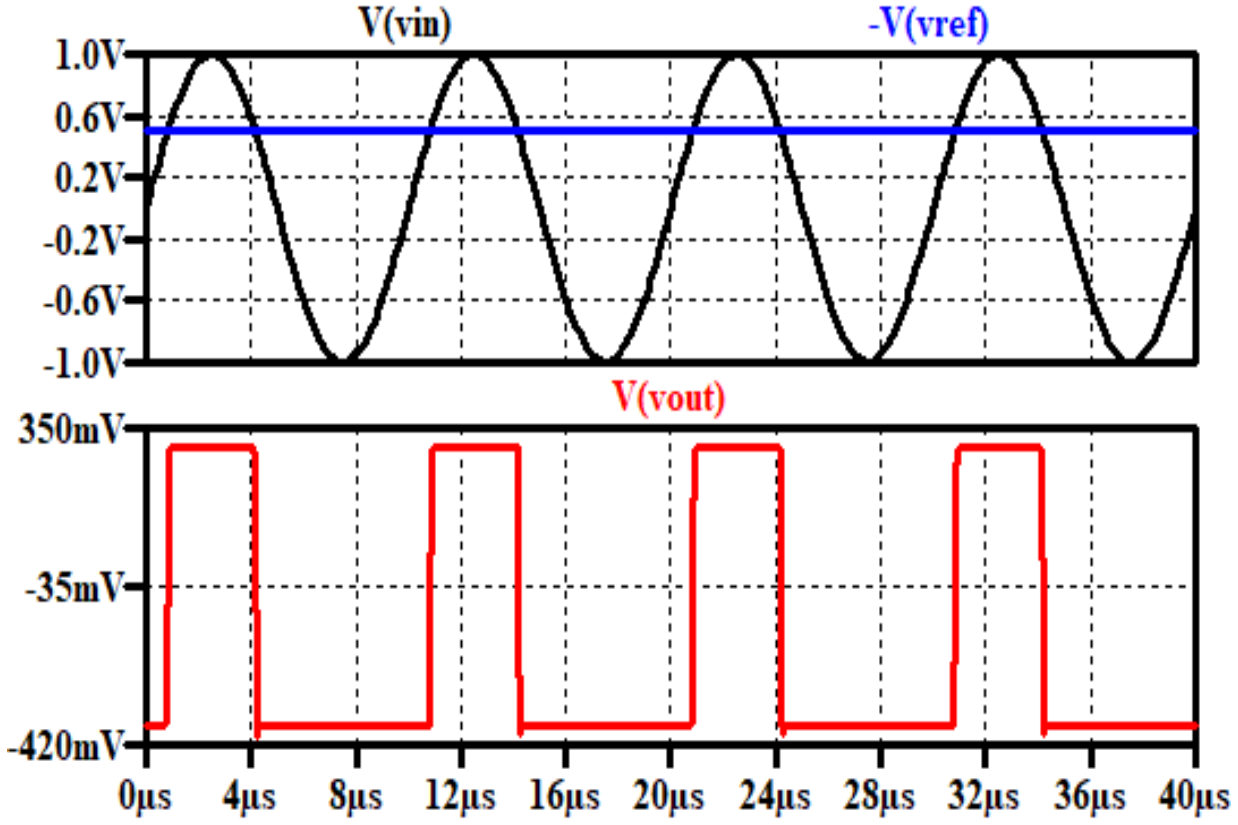

Fig.6.7 : Output waveform having 25% duty cycle

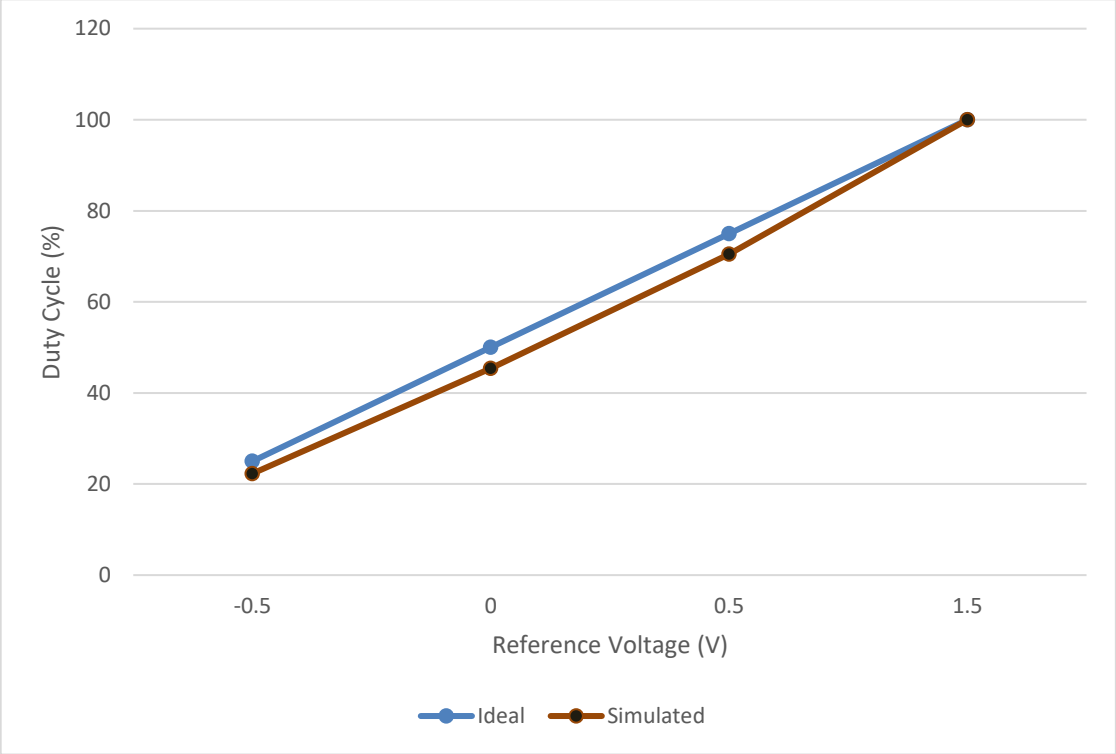

Fig.6.8 : Non ideality in the proposed PWM

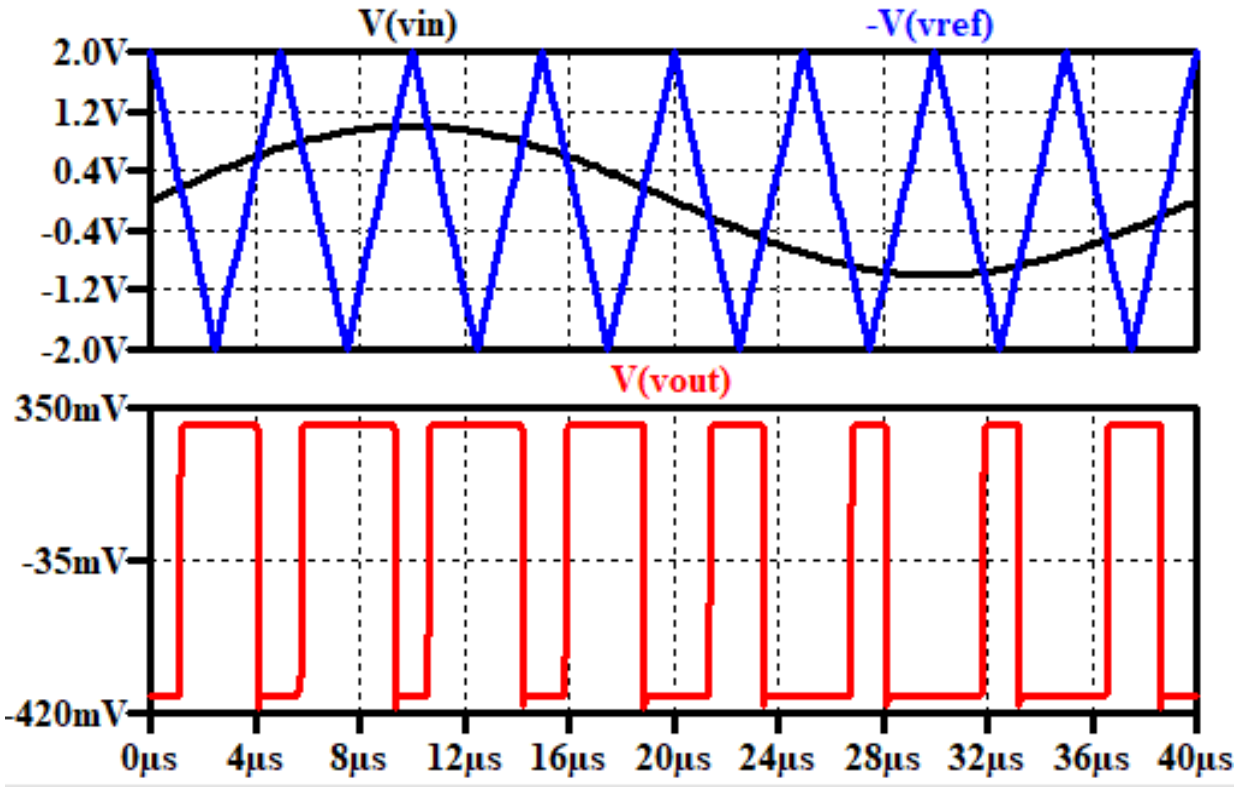

Fig.6.9 : Output waveform of pulse width modulator

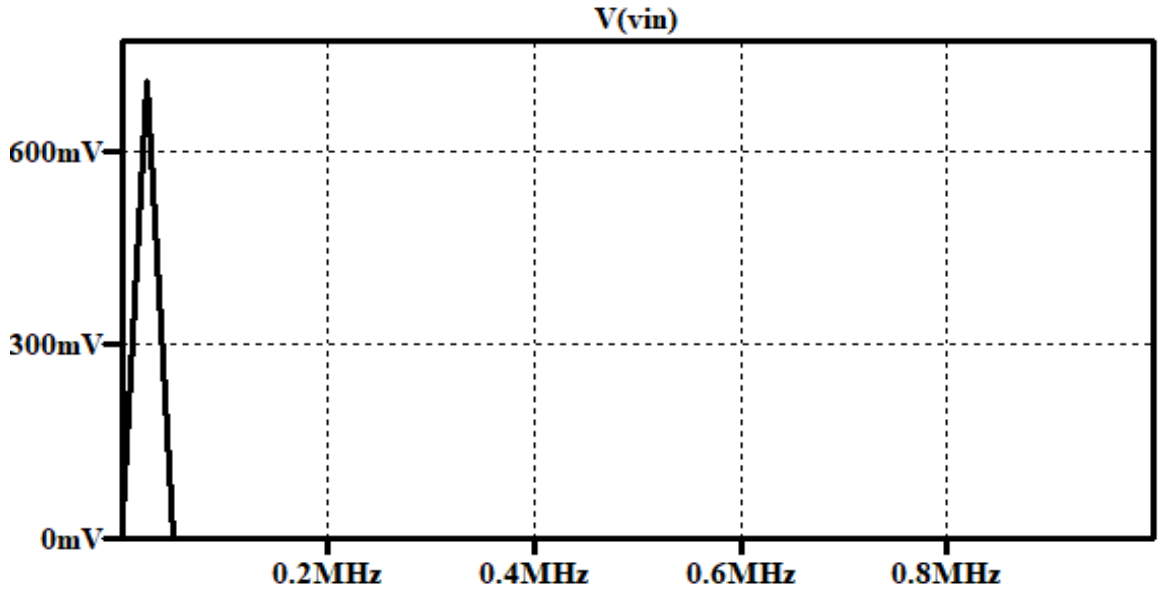

Fig.6.10 : Frequency spectrum of sinusoidal modulating signal

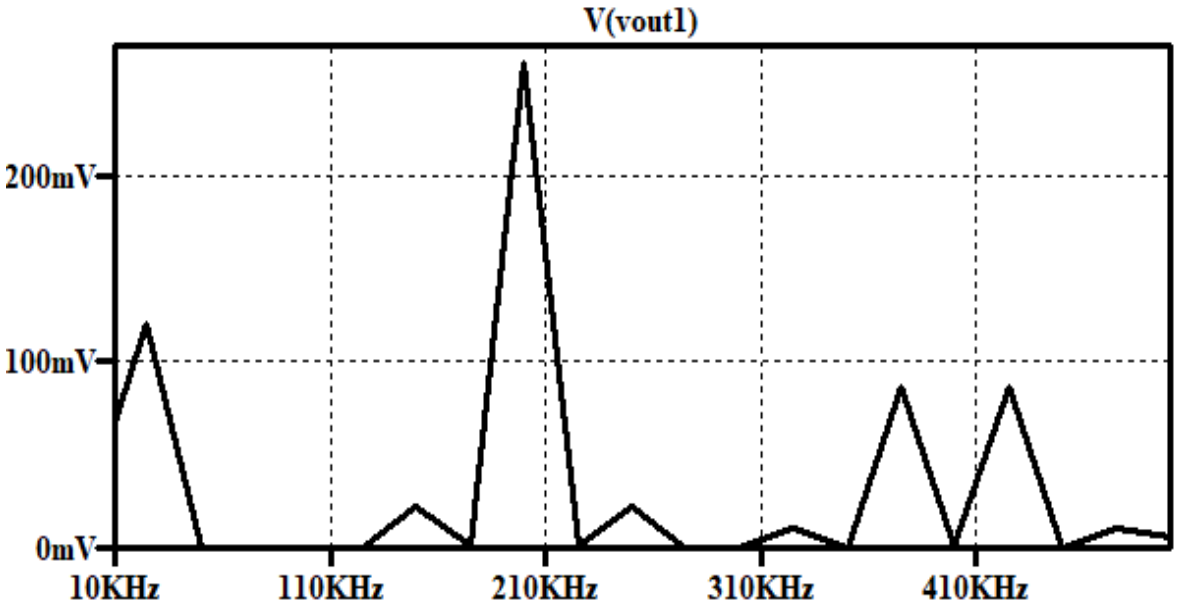

Fig.6.11 : Frequency spectrum of PWM wave

TABLE 6.1. Duty Cycle of The Output Waveform

Reference Voltage	Duty Cycle (ideal)	Duty Cycle (observed)	% Relative Error
1.5	100%	100%	0
0.5	75%	70.5%	0.060
0	50%	45.4%	0.092
-0.5	25%	22.3%	0.108

- **Comparative Analysis**

A comparative study of the proposed VCII based PWM circuit has also been done with the already presented analog PWM circuits using other active blocks. According to Table 6.2, it is observed that in topologies of PWM circuits implemented in [11]-[14], improvements can be seen in the proposed PWM topology using VCII- block. The proposed PWM circuit using VCII- performs better as compared to the one implemented using OP-AMP in [12] in terms of better high frequency performance due to higher slew rate. As compared to PWM generator using OTRA in [11], the proposed PWM generator circuit performs better in terms of accuracy at lower frequencies, as in [11], since it employs exponential waveform as carrier wave. The only trade off is the extra circuitry which is required to generate triangular/sawtooth waveform across the input of dual port comparator. Table 6.2 demonstrates comparative study in implementation of PWM generators using different active blocks.

TABLE 6.2. Comparative Study

Reference	No. of active components	No. of passive components
[11]	1 OTRA	1 Capacitor, 3 Resistors
[12]	1 OP-AMP	1 Capacitor, 3 Resistors
[13]	2 OTAs, 1 inverter, 1 MOS switch	1 Capacitor, 1 Resistor
[14]	3 OTAs	1 Capacitor, 1 Resistor
Proposed	1 VCII	4 Resistors

Chapter 7

Conclusion and Future Scope

In this project work , the second-generation voltage conveyer was comprehensively studied for its properties and design implementations. The basic applications related to the VCII circuit have also been explored and the performance of each application have been closely analyzed and compared. The VCII based applications have also been noted to have low power characteristics which can enable its use in low power applications. Various applications such as Voltage and current buffers, V to I converter, voltage differentiator, etc. have been implemented and their performances have been critically analyzed.

Furthermore, interesting applications such as a Schmitt trigger circuit and pulse width modulator have been implemented using second-generation voltage conveyer circuit, The results of these work illustrate a great deal of potential associated with VCII in implementation of analog circuits. The characteristics of each circuit have been plotted to validate the feasibility of operation and performance of the designed circuits have been critically analyzed using features of the software simulation tool. These applications implemented using

Many applications of great potential can also be explored such as simulated ground inductor, multivibrators, biquad filters, etc using second generation voltage conveyers.

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