Implementation of Analog Signal Processing/Generation Circuits Using Modern Active Building Blocks

A Thesis Submitted to the
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by

Ajishek Raj
(2K16/Ph.D/EE/09)

Under the Supervision of
Prof. Pragati Kumar & Prof. Data Ram Bhaskar

Department of Electrical Engineering
Delhi Technological University
Delhi-110042, India

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Certificate

This is to certify that the thesis entitled **"Implementation of Analog Signal Processing/Generation Circuits Using Modern Active Building Blocks**" being submitted by **Mr. Ajishek Raj (2K16/Ph.D/EE/09)** for the award of degree of **Doctor of Philosophy** in the Department of Electrical Engineering, Delhi Technological University, Delhi, is the record of students own work carried out by him under our supervision.The contents of this research work have not been submitted in part or fully to any other institute or university for the award of any degree.

Date: 26 July 2021

Prof. Pragati Kumar
Department of Electrical Engineering
Delhi Technological University
Delhi-110042, India

Prof. Data Ram Bhaskar
Department of Electrical Engineering
Delhi Technological University
Delhi-110042, India

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Ajishek Raj

AJISHEK RAJ

(2K16/PHD/EE/09)

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List of Symbols

g_m	Transconductance
R	Resistor
C	Capacitor
I_{Bias}	Bias Current
ω	Pole Frequency
Q	Quality Factor
BW	Bandwidth
H	Voltage Gain
S	Sensitivity
Ω	Ohm
$\mho$	Mho
g_p	Parasitic Transconductance
R_p	Parasitic Resistance
C_p	Parasitic Capacitance
r_o	Output Resistance
C_o	Output Capacitance
ϕ	Phase
S^F	Stability Factor

I_D	Drain Current
V_{DS}	Drain to Source Voltage
V_{GS}	Gate to Source Voltage
V_{TH}	Threshold Voltage
μ_n	Surface Mobility
C_{ox}	Gate Oxide Capacitance per Unit Area
W	Width
L	Length

List of Abbreviations

ABB	Active Building Block
IC	Integrated Circuit
Op-Amp	Operational Amplifier
OTA	Operational Transconductance Amplifier
CC	Current Conveyor
CCII	Second Generation Current Conveyor
MCCCII	Multiple Outputs Current Controlled Conveyor
DO-CCCII	Dual Output Current Controlled Current Conveyor
DDCC	Differential Difference Current Conveyor
FDCCII	Fully Differential Current Conveyor
DVCC	Differential Voltage Current Conveyor
CFOA	Current Feedback Operational Amplifier
FTFN	Four Terminal Floating Nullors
VDTA	Voltage Differencing Transconductance Amplifier
CDTA	Current Differencing Transconductance Amplifier
CCCCTA	Current Controlled Current Conveyor Transconductance Amplifier
DVCCTA	Differential Voltage Current Conveyor Transconductance Amplifier
CFTA	Current Follower Transconductance Amplifier

CDCTA	Current Differencing Cascaded Transconductance Amplifier
MCCTA	Modified Current Conveyor Transconductance Amplifier
MISO	Multiple-Input Single-Output
A/D	Analog to Digital Converter
D/A	Digital to Analog Converter
VM	Voltage Mode
CM	Current Mode
TRM	Transresistance Mode
TCM	Transconductance Mode
TOQSO	Third Order Quadrature Sinusoidal Oscillator
BJT	Bipolar Junction Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
GC	Grounded Capacitor
LPF	Low Pass Filter
APF	High Pass Filter
BPF	Band Pass Filter
BRF	Band Reject Filter
APF	All Pass Filter
TOQSO	Third Order Quadrature Sinusoidal Oscillator
CO	Condition of Oscillation
FO	Frequency of Oscillation

Chapter 1

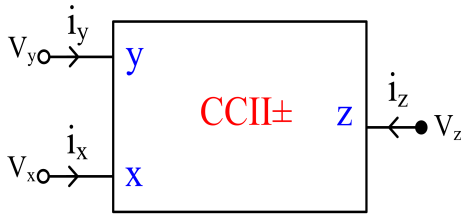
Introduction

This thesis deals with the "Implementation of signal processing/generation circuits using modern active building blocks". Several new analog signal processing circuits, both linear as well as non-linear and signal generation circuits employing operational transconductance amplifiers (OTAs) and current feedback operational amplifiers (CFOAs) have been presented.

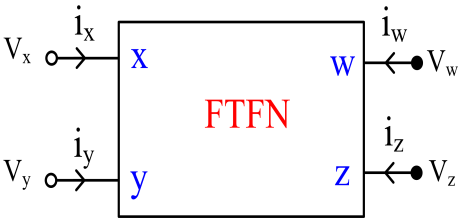
The integrated circuit (IC) op-amp has been the most-widely used analog circuit building block to design analog functions as, during the initial years of development of analog ICs, most of the signal processing was done in the so called "voltage mode". Since, IC op-amp μA741, which was among the most widely produced integrated circuits, was the circuit implementation of a differential voltage controlled voltage source (DVCVS). It was used for different signal processing/generation circuits to implement both linear and non-linear functions. However, in general, the op-amp circuits exhibit: (i) gain bandwidth conflict (except when configured as current controlled voltage source) (ii) limited frequency range of operation (due to finite gain bandwidth product) on one hand and due to the slew-induced distortion (because of finite slew rate of op-amp) on the other hand (iii) requirement of more than the canonic number of passive elements and (iv) requirement of perfect component matching conditions in many cases.

To alleviate the limitations of conventional op-amp circuits and to utilize the advances made in the semiconductor fabrication technologies, both, bipolar as well as CMOS, researchers and circuit designers worldwide have proposed several al-

ternative new analog active building blocks (ABBs) from time to time during the past four decades [1–13]. These building blocks have been used to realize (a) active filters in: (i) voltage mode (VM) [14–29], (ii) current mode (CM) [29–32], (iii) transimepedance mode [30, 33], (iv) mixed mode [34–63], (v) MOS-C [64–69], (vi) frequency agile [70–73], (vii) memristor-based [74–77] (b) oscillators (i) second order harmonic and quadrature sinusoidal oscillators [78–93] (ii) third order sinusoidal oscillators [94–128], and also in non-linear function generator circuits [129–173]. The functional block diagrams and port realtionships of some of the important modern active building blocks are shown below:

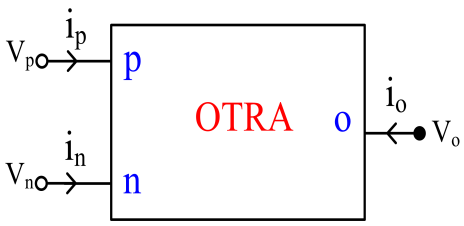


$i_y = 0, V_x = V_y$ and $i_z = \pm\, i_x$



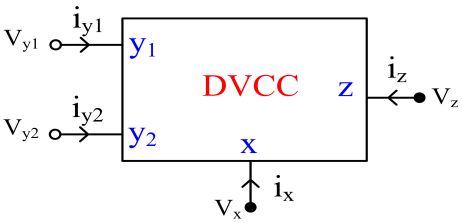
$V_x = V_y = 0,\ i_x = 0, i_y = 0$

$i_w = i_z$ and $V_w, V_z = arbitary$

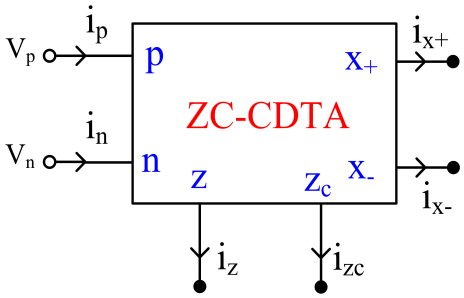


$V_p = 0, V_n = 0\ and$

$V_0 = R_m(i_p - i_n)$

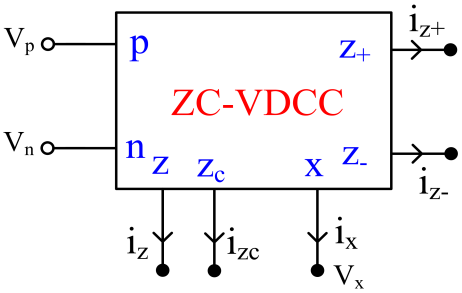


$i_{y1} = i_{y2} = 0, V_x = (V_{y1} - V_{y2}),\ i_{z\pm} = \pm i_x$



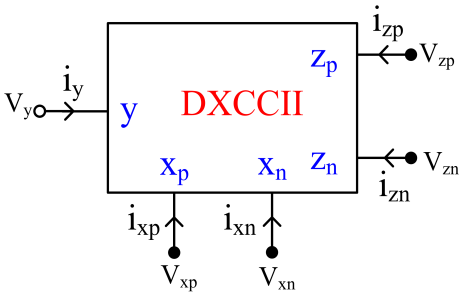
$V_p = 0 = V_n, i_z = i_{zc} = (i_p - i_n)$

$i_{x+} = +\, g_m V_z$ and $i_{x-} = -\, g_m V_z$



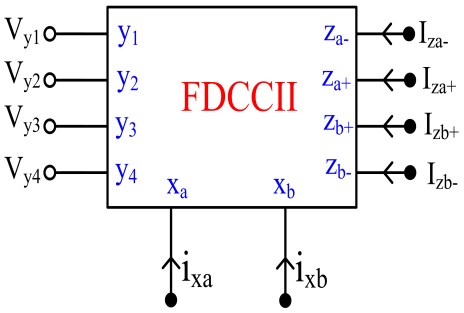
$i_z = g_m(V_p - V_n),\ i_{z\pm} = \pm i_x$ and

$V_x = V_z$



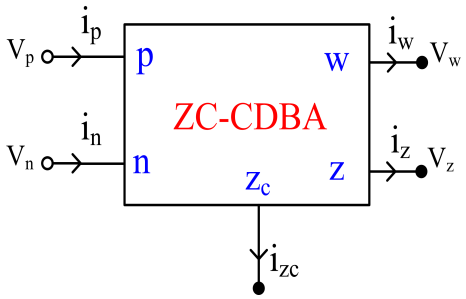
$V_{xp} = V_y, V_{xn} = -V_y, i_y = 0$

$i_{zn} = i_{xn}$ and $i_{zp} = i_{xp}$



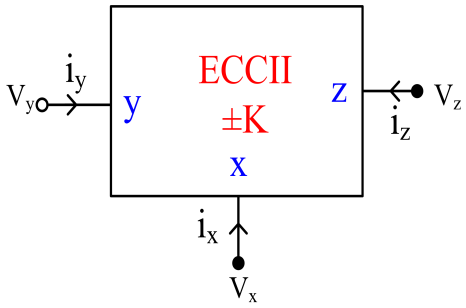
$V_{xa} = V_{y1} - V_{y2} + V_{y3}, V_{xb} = V_{y2} - V_{y1} + V_{y4}$

$i_{za\pm} = \pm i_{xa}$, and $i_{zb\pm} = \pm i_{xb}$



$V_p = V_n = 0, i_z = i_p - i_n$

$i_{zc} = i_z$ and $V_w = V_z$



$i_y = 0, V_x = V_y$ and $i_z = \pm K i_x$

Among the large number of new analog ABBs, only the operational transconductance amplifiers (OTA), current conveyors (CC) and current feedback operational amplifiers (CFOA) have been made available as off-the-shelf ICs [174].

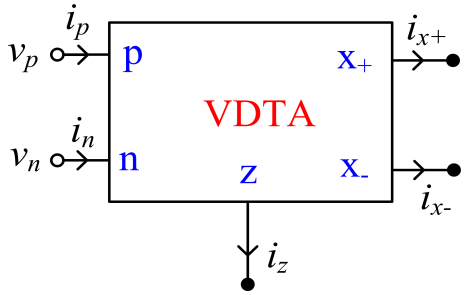
Since the work presented in this thesis deals with a modern active building blocks viz. OTAs and CFOAs, it is worthwhile to present a brief overview of these ABBs.

1.0.1 Operational Transconductance Amplifier

The operational transconductance amplifier, which is the circuit implementation of a differential voltage controlled current source, is a very useful active building block and is available as an off-the-shelf IC from manufacturers e.g. Radio Corporation of America (CA3080), National Semiconductor (LM13700), Maxim (MAX435). Several integrable, both bipolar as well as CMOS implementations of OTA are available in an open literature [175–177]. The most striking feature of an OTA is its very simple architecture (an actively loaded differential pair), and easy programmability of

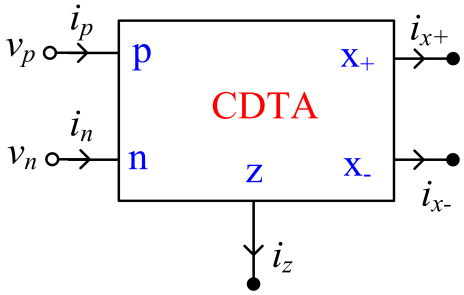
the parameters of the realized circuits acheived by varying its transconductance gain (g_m). Also, the OTA-based circuits can be designed without employing passive resistors! With the emergence of the current-mode techniques in analog circuit design, OTAs have become more relevant as the output of an OTA is a current, which is available at a very high impedance node (ideally infinite) in the circuit (providing ease of cascadability).

OTAs have also been employed as sub-blocks in many of the recently proposed analog active building blocks (ABBs), like voltage differencing transconductance amplifiers (VDTA), current differencing transconductance amplifiers (CDTA), current controlled current conveyor transconductance amplifiers (CCCCTA), differential voltage current conveyor transconductance amplifiers (DVCCTA), current follower transconductance amplifiers (CFTA), current differencing cascaded transconductance amplifiers (CDCTA) etc [1]. The symbolic representation and characteristic equation of the important ABBs employing OTAs are given below.



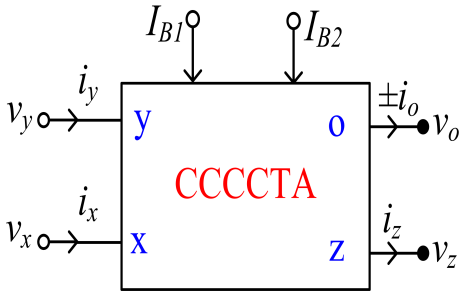
$i_p = 0 = i_n, i_z = g_{m1}(v_p - v_n)$

and $i_{x\pm} = \pm\, g_{m2} v_z$



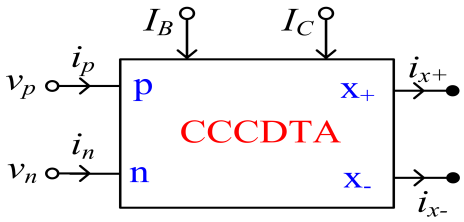
v_p=v_n=0, $i_z = (i_p - i_n)$ and

$i_{x\pm} = \pm\, g_m v_z$



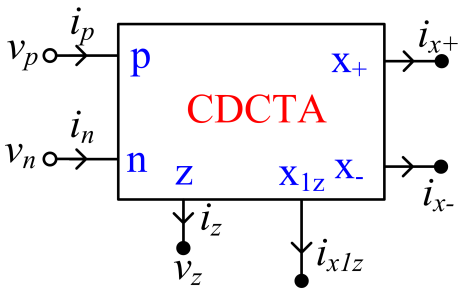
$i_y = 0, v_x = i_x R_x + v_y, i_z = i_x$

and $i_o = g_m v_z$

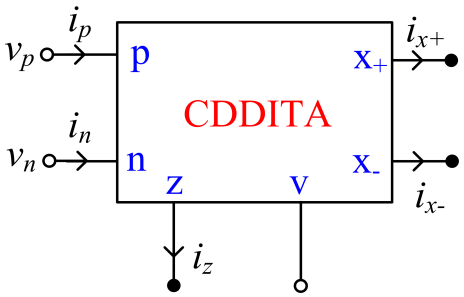


$v_p = R_p i_p,\ v_n = R_n i_n,\ i_z = i_p - i_n$

and $i_x = \pm g_m v_z$

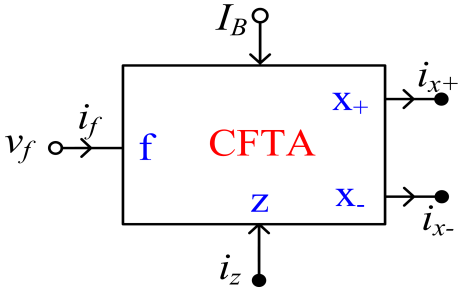


$V_p = V_n = 0$, $I_z = I_p - I_n$, and $I_{x1} = g_{m1} V_z$

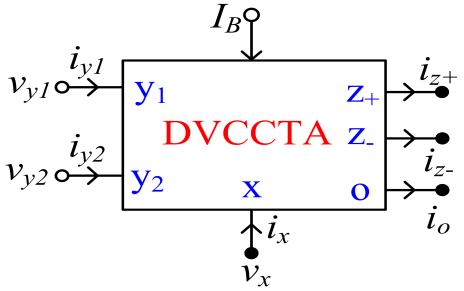


$v_p = v_n = 0$, $i_z = (i_p$ - $i_n)$,

and $i_{x\pm} = \pm\ g_m(v_z - v_v$



$v_f = 0$,$i_z = i_f$ and $i_{x\pm}$=$\pm\ g_m v_{x\pm}$



$i_{y1} = i_{y2} = 0$, $i_{z\pm}$=$\pm i_x$

$v_x = v_{y1} - v_{y2}$, and $i_{0\pm} = g_m v_{z\pm}$

1.0.1.1 Bipolar Implementation of OTA

The bipolar implementation of OTA [175] used in the design of off-the-shelf IC LM13600/LM13700 is shown in Fig. 1.1.

The differential transistor pair Q_4 and Q_5 shown in Fig. 1.1 form a transconductance stage in that the ratio of their collector currents is defined in terms of differential input voltage V_{id} as:

$$V_{id} = (V_+ - V_-) = \frac{kT}{q} ln \frac{I_5}{I_4} \tag{1.1}$$

where $\frac{kT}{q} = V_T =$ thermal voltage, k is the Boltzmann's constant ($1.3806485210^{-23} m^2 kgs^{-2} K^{-1}$), T is temperature in Kelvin and q is the charge on electron (-1.6 x 10^{-19} Coloumb). At room temperature (300K), V_T is equal to 26mV.

Transistors Q_1, Q_2 with diode D_1 form a Wilson current mirror (WCM) which is used to bias the differential pair. For large β_0 transistors, I_{abc} can be approximated

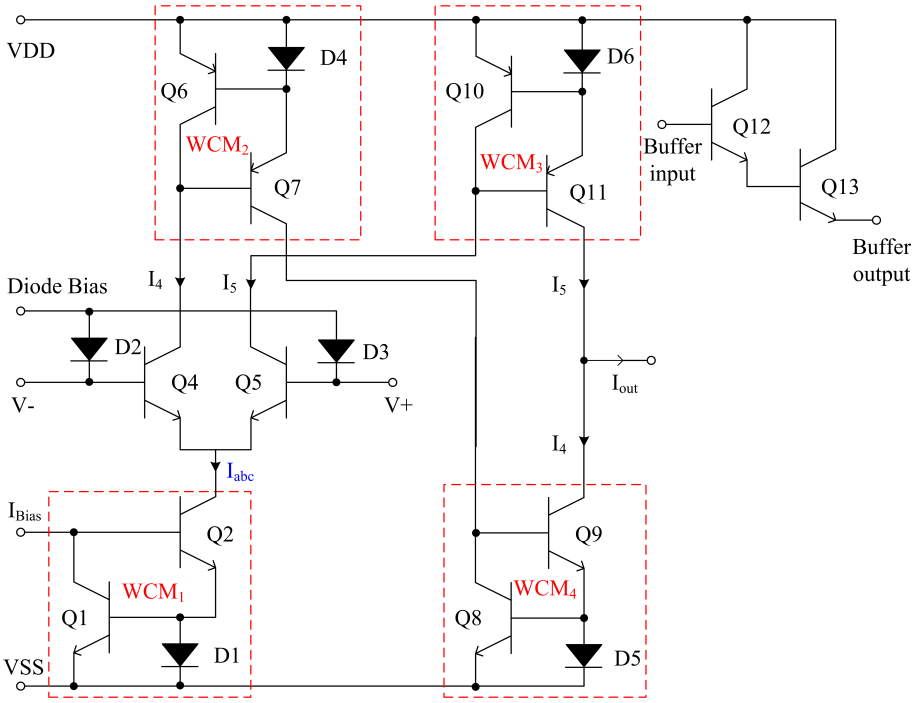


Figure 1.1: Bipolar implementation of one OTA used in LM13600/LM13700 [175]

as:

$$I_{abc} \approx (I_4 + I_5) \tag{1.2}$$

where I_{abc} is the amplifier bias current applied to the gain pin.

The active load for the differential pair is constituted by another WCM, formed by Q_6, Q_7 and D_4. The output current of OTA (I_{out}) is obtained by the current differencing action provided by WCM_3 (Q_{10}, Q_{11} and D_6) and WCM_4 (Q_8, Q_9 and D_5). Therefore, the output current I_{out} becomes:

$$\begin{aligned} I_{out} &= 2\left(\frac{I_{abc}}{4V_T}\right) V_{id} \\ &= \left(\frac{I_{abc}}{2V_T}\right) V_{id} = g_m V_{id} \end{aligned} \tag{1.3}$$

where $g_m = \frac{I_{abc}}{2V_T}$ is the transconductace of OTA.

Diode linearization scheme [177], has been used in LM13700 (D_2 and D_3) to enhance the input linear range, which is otherwise restricted to $\pm$ $2V_T$.

The IC LM13600/LM13700 contains two OTAs and two voltage buffers in the package and its pin diagram is shown in Fig. 1.2.

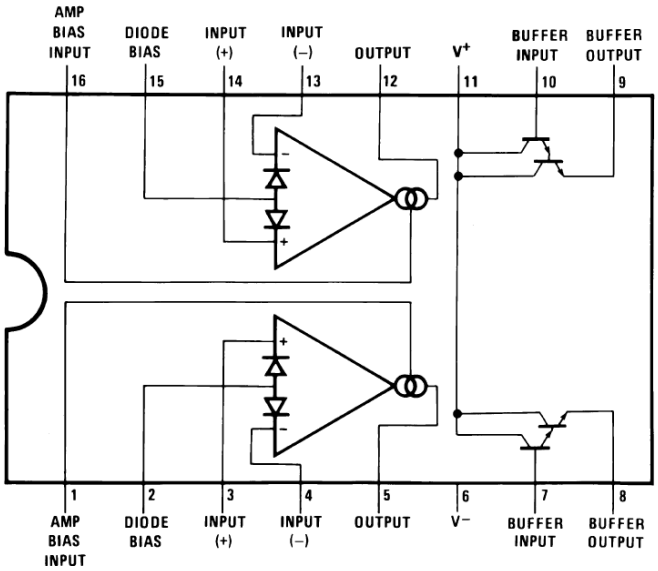


Figure 1.2: Pin diagram of LM13600/LM13700 [175]

1.0.1.2 CMOS Implementation of OTA

In Fig. 1.3, CMOS implementation of OTA [177] has been shown (assuming all MOSFETs are operating in saturation region).

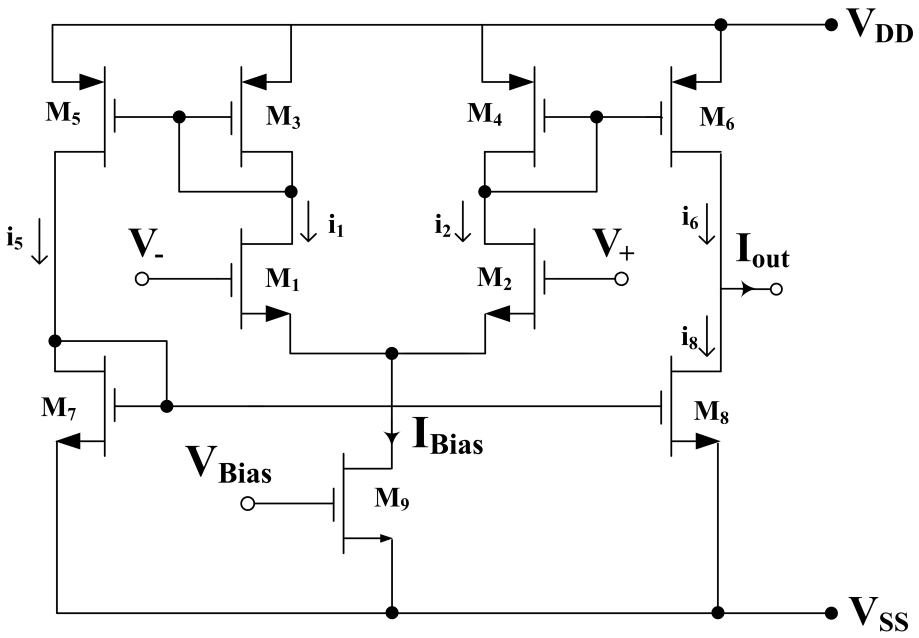


Figure 1.3: CMOS implementation of OTA [177]

From the circuit shown in Fig. 1.3 (negelecting channel length modulation), it is found that:

$$I_{out} = (i_6 - i_8) = (i_2 - i_1) \tag{1.4}$$

as $i_1 = i_5$ (for identical MOSFETs M_1 and M_5), $i_2 = i_6$ (for identical MOSFETs M_4 and M_6, and $i_5 = i_8$ (for matched devices M_7 and M_8. It can be shown that (i_1 - i_2) $\propto$ (V_+ - V_-), then the output current becomes:

$$I_{out} = g_m V_{id} \tag{1.5}$$

where $g_m = \sqrt{\mu_n C_{ox}^{/} (W/L)_n I_{Bias}}$, μ_n is is the surface mobility, $C_{ox}^{/}$ is the gate oxide capacitance per unit area and W/L is the aspect ratio of MOSFETs M_1 and M_2.

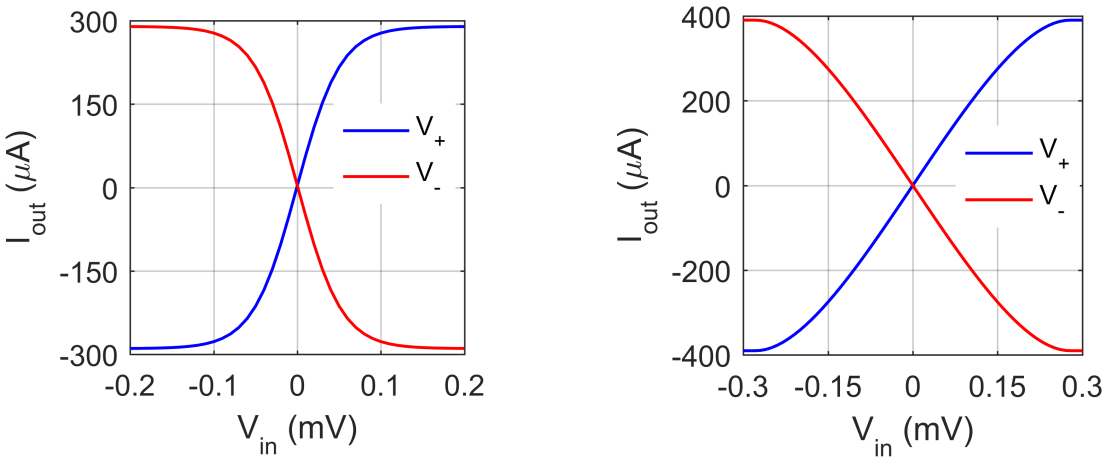
1.0.1.3 DC and Frequency Characteristics of an OTA

The DC transfer characteristics (differential input voltage versus output current) and frequency response of bipolar OTA and CMOS OTA have been displayed in Fig. 1.4 and Fig.1.5 respectively, when one of the input voltage of OTA is at ground (i.e. either V_+ or V_-). The macro model of LM13600/LM13700 has been used for bipolar OTA, whereas, the CMOS OTA has been simulated with 0.18μm CMOS technology parameters. The aspect ratios of different transistors used for Fig. 1.3 are given in Table 1.3.

Table 1.3: Aspect ratios of MOSFETs

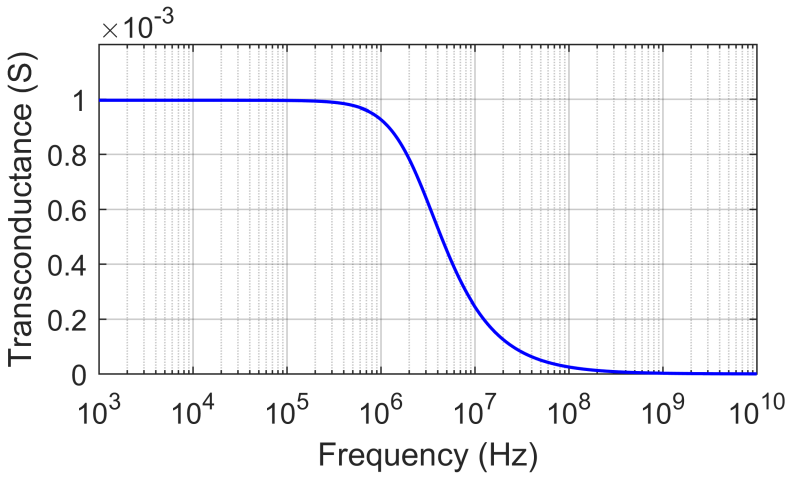
MOSFETs	Aspect Ratio (W/L)
M1, M2	3.6/0.36
M3, M4, M7, M8	1.44/0.36
M5, M6	2.88/0.36
M9	5.4/0.36

The operating range of differential input voltage of an OTA can be obtained from Fig. 1.4 and the maximum bandwidth of the OTA can be determined from Fig. 1.5. The various parameters such as linearity range, bandwidth, DC power dissipation, minimum and maximum values of bias current of bipolar and CMOS OTAs shown in Fig. 1.1 and Fig. 1.3 are given in Table 1.4.

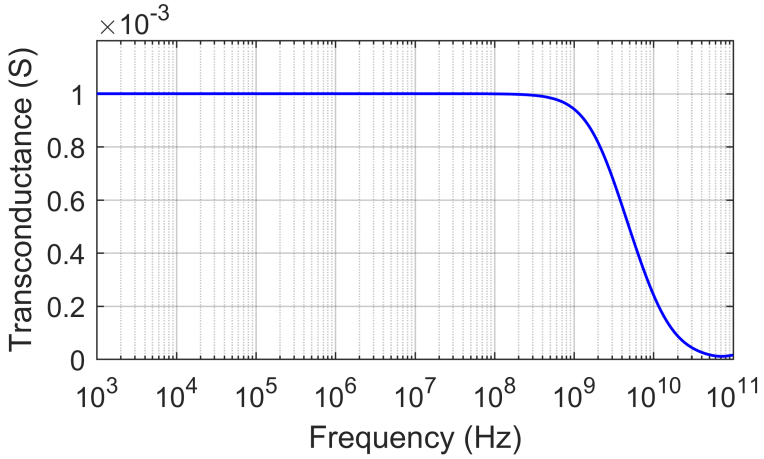


(a) (b)

Figure 1.4: DC transfer characteristics of (a) Bipolar OTA (b) CMOS OTA



(a)



(b)

Figure 1.5: Frequency responses of (a) Bipolar OTA (b) CMOS OTA

Table 1.4: Various parameters of bipolar and CMOS OTAs

Parameters	Bipolar OTA*	CMOS OTA
Linearity range	-50mV to +50mV	-150mV to +150mV
Bandwidth	2 MHz	2.84 GHz
DC power dissipation	570 mW	0.365 mW
Minimum value of I_{Bias}	5.4/0.36	50μA
Maximum value of I_{Bias}	2mA	1.5mA
Supply voltage	$\pm$15V	$\pm$0.9V

*(We have not biased the linearising diodes D_1 and D_2 in our research work)

1.0.2 Current Feedback Operational Amplifier

Current feedback operational amplifiers are also seeking attention of the researchers, in implementation of linear and non-linear signal processing and signal generation circuits, because of better AC performance, high linearity and excellent pulse response. Because of its very high slew rate, of the order of several hundreds to several thousands V/µsec, CFOAs could lead to circuits capable of operating over much wider frequency range than those possible with traditional operational amplifiers.

The CFOAs have been manufactured in IC form by several manufacturers including Analog Devices (AD844) [178] whose bipolar implementation has been shown in Fig. 1.6 [174]and its pin diagram is shown in Fig. 1.7.

In the internal architecture of the CFOA, transistors Q1–Q4 are configured as a mixed translinear cell (MTC) while the collector currents of transistors Q2 and Q3 are sensed by two modified p-n-p and n-p-n Wilson current mirrors consisting of transistors Q5–Q8 and Q9–Q12 respectively to create a replica of current i_X at the terminal - Z thereby yielding $i_Z = i_X$. The two constant current sources, each equal to I_B, force equal emitter currents in transistors Q1 and Q4 thereby forcing input current $i_Y = 0$ when a voltage V_Y is applied at the input terminal -Y. It can be easily shown that with $i_X = 0$, $V_X = V_Y$ and the Z-port current i_Z will be zero [174].

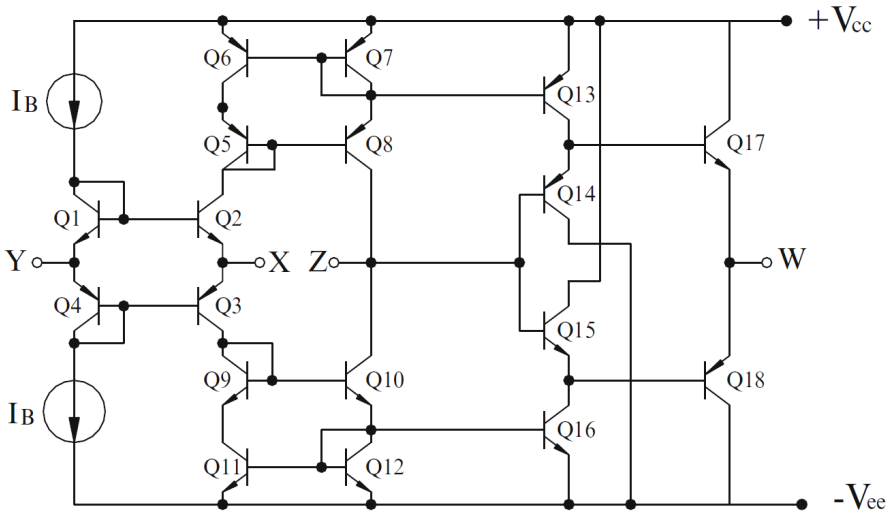


Figure 1.6: Schematic of the CFOA AD844 [174]

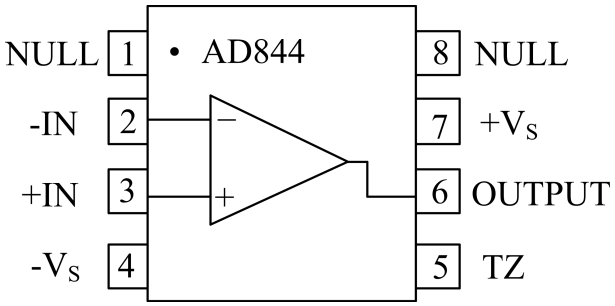


Figure 1.7: Pin diagram of AD844 [178]

However, for the case if $i_X \neq 0$, an exact analysis of the circuit using exponential relations between collector currents and base-emitter voltages for the transistors Q1–Q4 yields:

$$i_Z = i_X = -2I_B Sinh\left(\frac{V_Y - V_X}{V_T}\right) \tag{1.6}$$

An approximate relation between V_X, V_Y and r_X (for $i_X << 2I_B$) can be expressed as:

$$V_X \approx (V_Y + r_X i_X) \tag{1.7}$$

where $r_X = \frac{V_T}{2I_B}$

If terminal - Z is terminated into an external impedance/load Z_L, a voltage V_Z is created which passes through the voltage follower made from another MTC composed of transistors Q13–Q18 for which transistors Q13 and Q16 provide the DC bias currents. The last stage is characterized by an equation similar to (1.7) which

provides $V_W \approx V_Z$.

The defining equations of an ideal CFOA shown in Fig. 1.8 are given in matrix form as:

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \\ v_W \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ v_Z \\ i_W \end{bmatrix} \tag{1.8}$$

The symbolic representation of an ideal CFOA has been presented in Fig. 1.8.

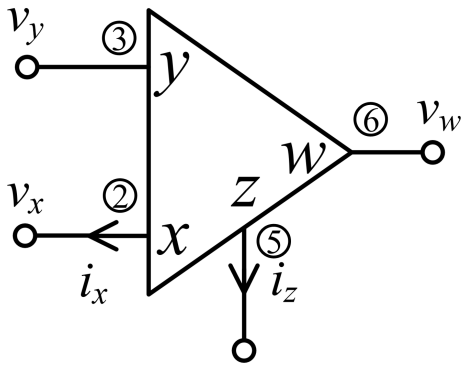


Figure 1.8: Symbolic representation of CFOA

The various parameters of AD844 type CFOA have been provided in Table 1.5

Table 1.5: Parameters of AD844 [178]

Parameters	Bipolar CFOA
Operating range	±18V
Bandwidth	60 MHz
DC power dissipation	1.1 Watt
Input common mode voltage	±18V
Quiescent current	6.5mA
Differential input voltage	6 V
Slew rate	2000 V/μs

1.1 Research Objectives

Though, OTAs have been used to design various types of active filters with different features [3], a careful perusal of the available research work done on the realization of OTA-based filters, it has been observed that compared to other types of universal active filters, relatively less work has been reported on the realization of multiple input single output (MISO) type universal active filters in voltage mode [14–16, 18–28] and MISO type universal active filters in mixed-mode [56–63].

Applications of different ABBs [94–128] including OTAs and CFOAs, in the realization of third order quadrature sinusoidal oscillators, have also been reported by various researchers because of many advantageous features such as lesser harmonic distortions, lower noise, better accuracy and high quality factor, as compared to second order harmonic oscillators. An extensive literature survey on third order sinusoidal oscillators realized with different ABBs, has revealed that only two circuits employing only OTAs [94] and [126] and only one third order sinusoidal oscillator circuit employing CFOAs [128] have been reported in the open literature .

Analog multipliers, dividers and square root circuits [129–145, 147–154, 156–163, 165–170, 172, 173] also play an important role in analog signal processing, telecommunications, and electronic systems, A/D and D/A converters, peak detectors, phase detectors, synthesizers as well as in analog computational systems based on biological 'neural' paradigms [179]. In open literature, various ABBs have been used for the design of voltage mode (VM) analog dividers and square root circuits. CFOAs have also been employed to implement non-linear functions (differential multiplier and divider circuits) [173] uses an excessively large number of components (five CFOAs, six MOSFETs and four identical capacitors).

From a detailed observance of the research works reported above, it has been found that:

(i) There are no circuits available in open literature which can provide all five filter functions in VM based on MISO topology with five or less than five single output OTAs.

(ii) No mixed mode universal active filters have been reported yet, which can provide all five generic filter functions in all four modes with one type of ABBs.

(iii) Though there are a number of third order sinusoidal oscillators available in the open literature, very few OTA-based realizations of third order quadrature sinusoidal oscillator (TOQSO) circuits exist.

(iv) Compared to the available topologies for generation of third order quadrature sinusoidal oscillators with different properties, very few topologies exist in open literature for the generation of TOQSOs.

(v) No third order sinusoidal oscillator circuits are available in open literature which can generate low frequency sinusoidal oscillations.

(vi) Though there are a number of VM divider and square root circuits reported, yet no circuit exists which has single ABB and lesser number of MOSFETs.

(vii) No work has been presented on the realization of single CFOA-based analog multiplier and divider function from the same topology.

Based upon the above discussions, the following research objectives were identified:

Realization of:

(i) OTA-based universal biquad filters with properties and features which were not available in previously reported OTA- based universal filters.

(ii) new OTA-based third order quadrature sinusoidal oscillator circuits.

(iii) new CFOA-based third order sinusoidal oscillator circuits.

(iv) OTA-based non-linear function generation circuits with lesser components count.

(v) CFOA-based non-linear function generation circuit with lesser components count.

1.2 Organisation of Thesis

The work presented in the thesis has been organized in the following manner:

In **Chapter 2**, we have presented three circuits of VM universal biquad filters based

on MISO topology employing OTAs. All five filter functions are realizable from the proposed filter structures by appropriate selection(s) of input voltages. A mixed mode universal active filter configuration using OTAs has also been presented which realizes all five filter functions in all four modes. Macro-model of LM13600/LM13700 and exemplary CMOS OTA have been used to validate the workability of proposed configurations. Sample layout designs have also been included.

Chapter 3 dealt with four new configurations of TOQSOs using three OTAs and three capacitors. All the presented circuits offer independent electronic control of CO and FO. Also, a systematic realization of TOQSO has been presented and based upon this topology, two different TOQSOs employing OTAs and three grounded capacitors have been proposed. Simulation and experimental results have been provided to validate the theory.

In **Chapter 4**, two new topologies for the realization of TOQSO have been presented. Exemplary TOQSOs based on the proposed topology have also been derived. Systematic realization of low frequency third order sinusoidal oscillators using minimal active and passive components have also been presented in this chapter. Validation of the proposed circuits has been confirmed through experimental results.

Chapter 5 presents new configurations of analog divider and square root circuits using single OTA and two MOSFETs. A four quadrant analog multiplier/two quadrant divider circuit using a single CFOA has also been presented.

Chapter 6 of the thesis presents a summary of the research work presented and some suggestions for future work on the ideas explored.

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Chapter 2

Voltage Mode and Mixed Mode Filter Structures Using OTAs

2.1 Introduction

Analog active filters have a wide range of applications in communications, control systems, instrumentation, measurement systems, biomedical signal processing and a host of other related applications [1–21] . In recent years, there has been a growing interest in designing and developing these filters using a variety of active building blocks (ABBs) including current conveyors (CCs) and their different variants, current feedback operational amplifiers (CFOAs), four terminal floating nullors (FTFNs), current controlled current conveyor trans-conductance amplifiers (CCCCTAs), modified current conveyor trans-conductance amplifier (MCCTA), voltage differencing transconductance amplifiers (VDTAs), current difference transconductance amplifiers (CDTA), fully differential difference current conveyor (FDCCII), current differencing buffered amplifier (CDBA), voltage difference current conveyor (VDCC), dual X second generation current conveyor (DXCCII), operational transconductance amplifiers (OTAs) etc. Continuous-time active filters realized with the above mentioned ABBs may be classified into several categories as given below:

- Based on the nature of input and output signals - voltage mode (VM), current mode (CM), transconductance mode (TCM) and transadmittance mode (TAM).

- Based on the order - first order, second order or higher order.

- Based on the number of inputs and number of outputs - single-input single-output (SISO), multiple-inputs single output (MISO), single-input multiple-outputs (SIMO), and multiple-inputs multiple-outputs (MIMO).

- Based on the nature of the elements - fixed structure type, in which the nature of elements do not change for the realization of different filter responses or variable structure type, in which the nature of elements change for the realization of different filter functions.

- Based on the nature of output responses available - universal filter, in which all the five generic filter functions, namely low pass filter (LPF), high pass filter (HPF), band pass filter (BPF), band reject filter (BRF) and all pass filter (APF) are available.

It may be noted that the above mentioned classifications are not mutually exclusive. A particular filter may belong to more than one of the above mentioned classes. Since this chapter deals with voltage mode and mixed mode MISO type universal active filter circuits realised with operational transconductance amplifiers, it is worthwhile to present a comprehensive account of the MISO type active analog filters realized with different ABBs.

2.1.1 MISO Type Mixed Mode Active Analog Filters Realized with ABBs Other than OTAs

In [22], **Soliman** proposed two mixed-mode biquad circuits employing four CCs, four resistors and two grounded capacitors (GCs). One of the circuits (Fig. 2 of [22]) has been shown in Fig. 2.1 in which V_3 is fedback to the summer circuit at

its Y-terminal, whereas, the Y terminal of fourth CCII is connected with V_2. Both the structures presented in [22] can realize LP, BP, HP filter responses in TRM only.

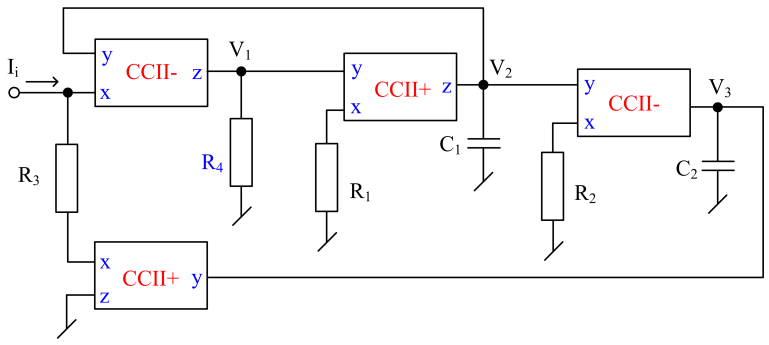


Figure 2.1: Mixed mode biquad circuit reported by Soliman [22].

In 2003, **Abuelma'atti** [23] introduced a mixed-mode biquad using four dual-output second generation current-controlled CCs and two GCs. The reported circuit can realize LP, BP, HP filter functions in VM, CM, TRM, whereas, in TCM, it can provide LP, BP, HP and BR filters. This structure cannot realize AP filter responses. The pole frequency and bandwidth of the reported circuit were independently tunable.

In [24], a mixed-mode biquad circuit employing seven CCs, two GCs and eight resistors was proposed by **Abuelma'atti**, **Bentrica** and **Al-Shahrani** which can provide all the generic filtering functions, namely LPF, HPF, BPF, BRF and APF in all four modes, but the circuit uses inordinately large number of active and passive elements.

In [25], a mixed-mode CCII based active filter employing five CCIIs, two GCs, three grounded resistors and four floating resistors was reported by **Abuelma'atti** and **Bentrica**. Though, the circuit can provide different generic second order filter responses in all the four modes, but employs non-optimal number of resistors.

In [26], **Pandey, Paul, Bhattacharya** and **Jain** introduced a new mixed-mode biquad circuit using three CCIIs, two GCs, three floating resistors and one grounded

resistor. For the realization of filter functions in all four modes, two switches are required and the circuit also requires matching conditions for the realization of BR and AP responses.

In [27], **Siripruchyanun** and **Jaikla** proposed a universal biquad filter in VM and CM. The circuit employs two DO-CCCIIs, one floating capacitor and one GC. The pole frequency and bandwidth of the reported circuit can be tuned electronically through input bias currents.

A mixed-mode universal biquad filter structure using MCCCII [28] was presented in 2009 by **Zhijun**. The circuit employs four MCCCII and two GCs. However, the filter structure can not realize BR and AP responses in all modes of operation.

In [29], **Horng** proposed a current-mode and transimpedance-mode universal biquadratic filter using three multiple output CCIIs, two GCs and five resistors. The circuit realizes all the second order filter functions, namely, LPF, HPF, BPF, BRF and APF. The filter parameters of the realized filter, namely, the pole frequency, and bandwidth can be controlled orthogonally.

In [30], **Pandey** and **Paul** reported a mixed-mode universal biquad filter employing four multiple output current controlled CCs (MOCCCIIs) and two GCs. The circuit can realize all five filter functions in all modes, however, it needs input current scaling for the realization of AP response and also requires matching conditions for the realization of HP, BR and AP responses in CM and TRM.

In [31], **Singh** and **Afzal** proposed a new electronically tunable universal, mixed-mode biquad filter employing five digitally programmable CCIIs, six resistors and two GCs. The structure requires current scaling in CM and TRM for the realization of AP filter and also requires matching conditions for BR filter realization in VM

and TCM.

In [32], **Chang, Lee, Hou, Horng** and **Tu** reported a high-order differential difference current conveyors (DDCCs)-based general mixed-mode universal filter employing (n+1) DDCCs, n GCs and (n+2) grounded resistors. This configuration supports all four modes but to achieve electronic tunability of the filter parameters, additional active devices are required.

In [33], **Lee** presented a fully cascadable mixed-mode universal filter biquad using three DDCCs and all grounded passive components. In this circuit, however, HP, BR, AP responses could not be realized in TRM.

Lee and **Chang** [34], proposed a mixed-mode biquad filter employing one fully differential current conveyor (FDCCII), two GCs, two floating resistors and a grounded resistor. The reported circuit has been shown in Fig. 2.2. However, this circuit cannot realize LP, BR and AP responses in TCM.

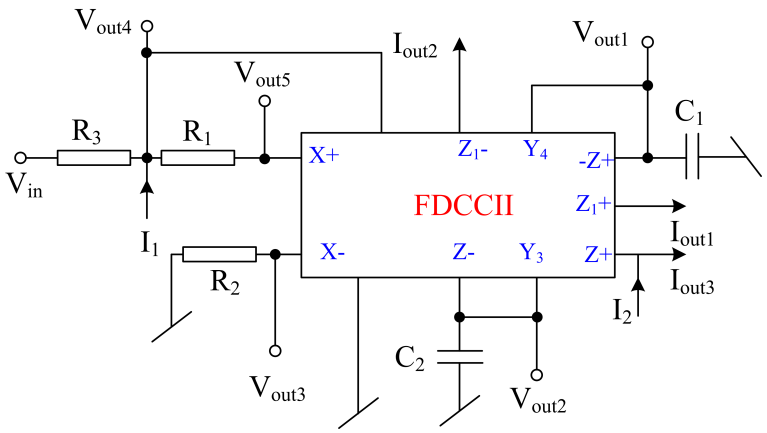


Figure 2.2: Filter configuration reported by Lee and Chang [34].

In 2016, **Lee** proposed a mixed-mode universal biquadratic filter structure employing one FDCCII, one differential voltage current conveyor (DVCC), two GCs, four grounded resistors and two floating resistors [35]. However, to realize AP responses in some of the modes, passive component matching is required.

In 2011, **Soliman** introduced four modified universal biquads employing four DVCCs, four grounded resistors and two GCs [36] . These configurations can realize, at the most, only three filter responses, namely, LPF, HPF, and BPF.

In [37], **Minaei** and **Ibrahim** reported a mixed-mode KHN-biquad using three DVCCs, two GCs and three grounded resistors. The HP and AP responses could not be realized in VM while, HP, BR, AP responses were not realizable in TRM.

In [38], **Lee** reported a mixed-mode universal biquadratic filter employing two plus type fully differential current conveyors (FDCCIIs), two GCs, four grounded resistors and one floating resistor . The circuit can be operated in all four modes. VM and TIM filter functions can be realized directly but in other two modes, different combinations of current and voltage signals are required to realize the filter responses.

In [39], **Yuce** presented a fully integrable, mixed-mode universal biquad using a single specific CFOA (SCFOA), with two floating capacitors and three resistors. This circuit structure is shown in Fig. 2.3. The reported biquad filter offers independent control of resonance frequency and quality factor. The circuit provides filter responses in CM and VM only.
Singh, Maheshwari and **Chauhan** reported another electronically tunable mixed-mode biquad filter employing three MO-CCCCTAs and two GCs in [40]. The HP and AP responses could not be realized in both VM and TRM.

In 2010, **Yuce** and **Sezai**, proposed three mixed-mode filter configurations employing three second generation current conveyors, two floating resistors and two GCs [41]. The presented circuits could realize only LP, BP responses in VM, while all five generic filter functions viz. LP, HP, BP, BR and AP can be obtained in CM.

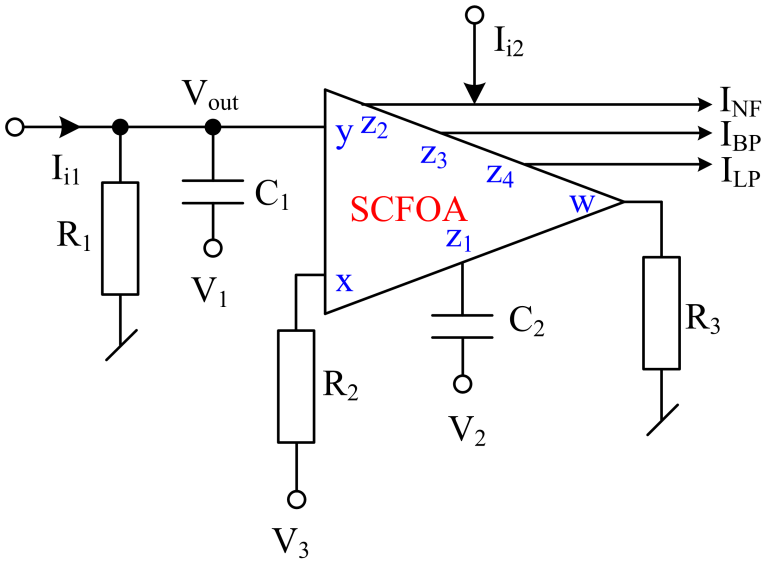


Figure 2.3: SCFOA based mixed mode filter circuit proposed by Yuce [39]

In [42], a mixed-mode universal biquad circuit employing four CFOAs, two GCs, and nine resistors was introduced by **Singh, Singh, Bhaskar** and **Senani**. The proposed structure requires a switch to realise BR and AP responses.

In [43], **Shah** and **Malik** presented a multifunction mixed-mode filter using three FTFNs, one floating capacitor, one GC and three resistors. The circuit could not realise BR and AP responses in CM and VM, HP, BR and AP responses in TRM, and LP, BR, AP responses in TCM.

In [44], **Singh, Maheshwari** and **Chauhan** reported an electronically tunable current/voltage-mode universal biquad filter employing two CCCCTA, one floating capacitor and one GC. However, all five generic filter functions in all four modes could not be realized.

In [45], **Singh** and **Chauhan** proposed a new, electronically tunable, universal mixed-mode biquad filter using MCCTAs, one floating capacitor, one GC and two

resistors. The biquad filter circuit requires passive component matching conditions in TCM for the realization of LP response as well as AP response.

Yesil and **Kacar** [46], introduced two mixed mode biquads using two VDTAs and two GCs. The presented filter circuits could not support current mode and transresistance modes of operations.

2.1.2 MISO type VM and Mixed Mode Analog Active Filters Realized with OTAs

A simple, generalized scheme for the realization of universal filter in VM has been described in [47] by **Khan, Ahmed** and **Minhaj**. Two circuits were reported in which one of the circuit utilizes three OTAs, two floating capacitors and one buffer as shown in Fig. 2.4, whereas, the other circuit was implemented employing three OTAs, two capacitors (one floating and another grounded) and one buffer. The reported filter circuits have electronic tunability of filter parameters. The pole frequency and bandwidth of the realized filters can be controlled independently while, for constant frequency, pole quality factor can also be changed independently.

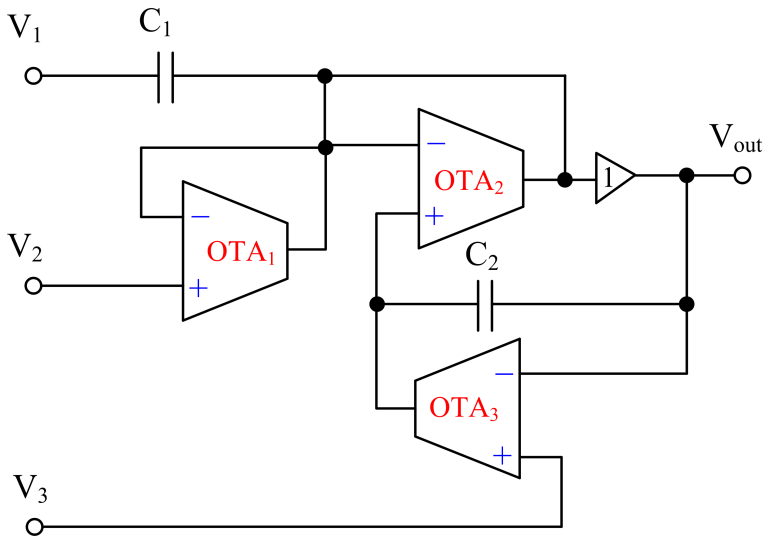


Figure 2.4: Universal biquad filter circuit using OTAs reported by Khan, Ahmed and Minhaj [47].

In [48], **Horng** reported a multifunction filter structure employing a single output OTA, one multiple output OTA and two floating capacitors. With appropriate choice(s) of four input signals, all five filter functions can be realized. The presented circuit has electronic tunable feature of pole frequency for constant pole quality factor.

A six OTAs based biquadratic filter configuration was reported in [49] by **Kumngern** and **Dejhan**. The presented filter circuit is capable of realizing LPF, HPF, BPF, BRF and APF in VM and has independent electronic control of natural frequency and the quality factor.

In yet another proposition [50], **Kumngern, Knobnob** and **Dehjan** reported a six OTAs and two grounded capacitors based universal biquadratic filter topology which provided all generic second order filter functions in VM. The output was available at a high output impedance node .

A VM MISO type universal biquad configuration employing six OTAs and two GCs was reported in [51] by **Psychalinos, Kasimis** and **Khateb** which has been displayed in Fig. 2.5. The presented circuit can provide all five filter functions and also the filter circuit has electronic tunability feature between pole frequency and quality factor.
In [52], **Kumngern** and **Torteanchai** presented a VM biquad filter configuration employing nine OTAs and three capacitors. This structure can realise all standard filter functions with independent electronic control of natural frequency and the quality factor.

Kumngern and **Junnapiya** proposed three OTAs and two capacitors (one floating and other grounded) based VM universal biquadratic filter in [53] where all five fil-

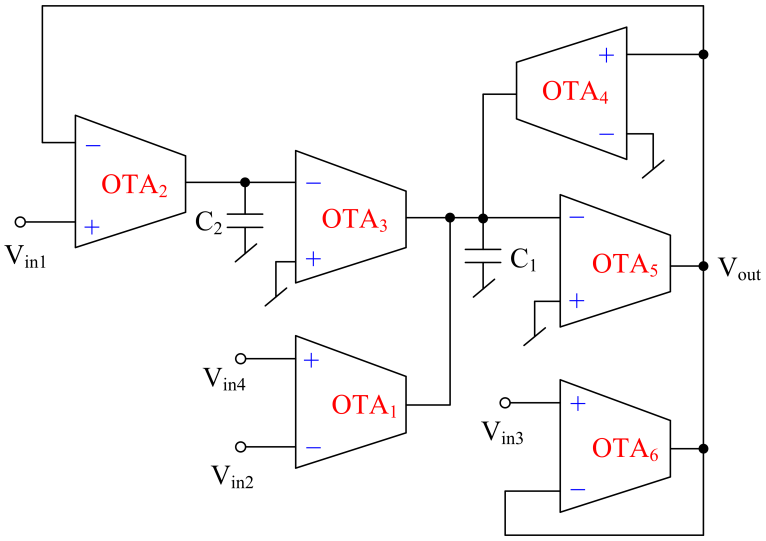


Figure 2.5: Universal biquad filter structure reported by Psychalinos, Kasimis and Khateb [51].

ter functions are available, without any component matching constraints. The pole quality factor of the reported filter circuit can be tuned independently for constant pole frequency.

In [54], two, OTA-C universal biquad structures using four OTAs and two GCs were introduced by **Bhaskar, Singh, Sharma** and **Senani**. One of the reported circuits has been displayed in Fig. 2.6. The circuit can provide CM and TAM outputs only.

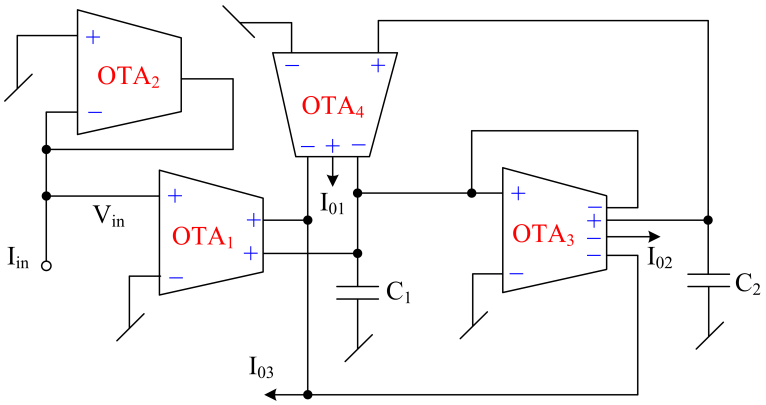


Figure 2.6: OTA-C filter configuration reported by Bhaskar, Singh, Sharma and Senani [54]

In [55], four–input one–output, single ended OTA based circuit in VM has been presented by **Kumngern, Suksaibul** and **Knobnob** which employs six OTAs, two grounded capacitors and two grounded resistors. The presented circuit realizes all five filter functions without any matching constraints. The reported circuit has orthogonal controllability between pole frequency and pole quality factor.

Another MISO type VM universal biquad filter circuit employing five OTAs, two grounded capacitors and one grounded resistor has been presented in [56] by **Wattikornsirikul** and **Kumngern**. The reported circuit yields all five filter functions without any matching conditions.

In [57], **Singh, Bhaskar** and **Prasad** reported two OTAs, two floating capacitors and one buffer based VM filter configuration in which LPF, HPF, BPF, BRF, and APF responses can be obtained by appropriate choice(s) of input voltage signals.

A programmable VM biquad filter topology using minimum number of components was reported by **Bhanja** and **Ray** using two first order filter sections in [58]. The filter circuit employs three OTAs, one floating capacitor, one grounded capacitor, and one grounded resistor to derive all five filter functions. Pole frequency and quality factor of the reported filter can be controlled electronically using the tranconductance of OTAs.

Five–input single–output, VM universal biquad structure employing six OTAs, and two capacitors was proposed in [59] by **Knobnob, Suksaibul** and **Kumngern**. The biquad filter circuit can provide all five standard filter responses without any matching constraints. The pole frequency and quality factor of the proposed filter can be electronically controlled through bias currents of OTAs.

In [60], six single output OTAs, two grounded capacitors and two grounded resistors were used to realize VM universal filter structure by **Kumngern, Suksaibul** and **Khateb** which can realize all five filter functions with electronic control of pole frequency and quality factor.

Wang, Chen, Ku and **Yang** reported five–input single–output, VM filter topology in [61]. This circuit employs five single–output OTAs and two grounded capacitors. This configuration is capable of providing all five filter responses. The filter circuit provides orthogonal electronic control of angular frequency and quality factor.

In 2009, **Chen, Liao** and **Lee** reported a tunable, mixed-mode OTA-C, universal biquad filter [62] employing four single–output OTAs, one dual–output OTA and two GCs. This universal biquad filter can realize all five generic filter responses in VM, CM, TRM but only LP and BP filter responses in TCM. The reported circuit has orthogonal tunability between angular frequency and quality factor. This circuit configuration is reproduced in Fig. 2.7.

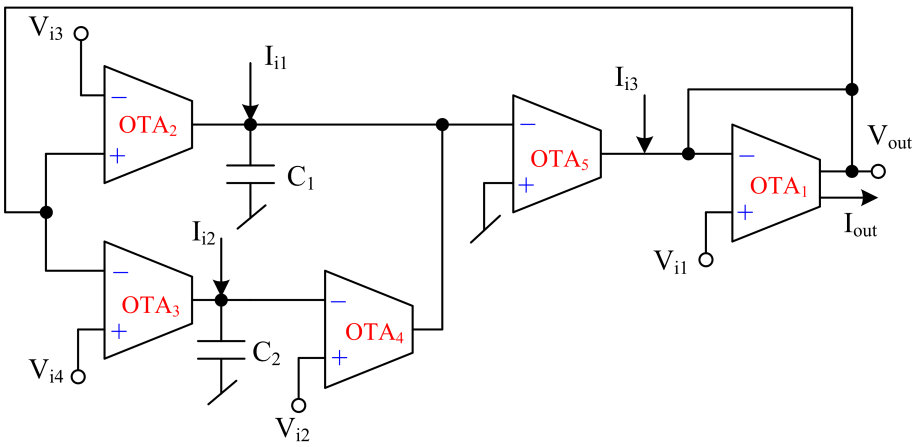


Figure 2.7: Mixed mode biquad filter circuit using OTAs reported by Chen, Liao and Lee [62].

A mixed mode OTA-C universal biquad filter topology [63] was proposed by **Abuelma'atti**, and **Bentrica** using six single–output OTAs, one dual–output OTA and two GCs. The biquad filter circuit can realize all five generic filter responses in all four modes.

The presented circuit requires matching condition for the realization of AP response. Independent electronic tunability of angular frequency and bandwidth is obtainable in the reported circuit.

In [64], **Ibrahim** reported a mixed mode universal filter circuit which employed four dual–output OTAs and two GCs. The presented circuit can not realize BR and AP responses in VM and TRM. The reported circuit enjoys orthogonal tunability of angular frequency and bandwidth.

In [65], a higher-order mixed mode OTA-C universal biquad was proposed by **Lee** and **Chang** which employs (n+1) single–output OTAs, one multi–output OTA and n GCs. As an application example, a sixth order universal filter was designed. However, circuit required voltage inversion and scaling of currents to realize AP filter.

In [66], **Lee** presented two mixed mode filter configurations. One of the structure presented in [66] (Fig. 2), provided all five generic filter functions in all modes (VM, CM, TRM, TCM) but it employed three single–output OTAs, one triple–output OTA, one dual–output OTA and two GCs. Also, the reported circuit had orthogonal tunability between angular frequency and quality factor.

In [67], three OTAs (in which two OTAs have multiple inputs), two capacitors and one voltage buffer based mixed mode universal filter configuration has been reported by **Parvizi**, which can realize all five filter functions in all four modes.

In [68], two higher order multiple mode and trans admittance mode OTA-C filters were introduced by **Lee** employing (n+3)/(n+1) OTAs and n GCs. As an application example, a sixth order filter has been designed which provides orthogonal electronic control of pole frequency and quality factor.

From the above description, it has emerged that a variety of MISO type analog active filters employing different ABBs, including OTAs, have been reported in open literature. The class of MISO type biquads employing OTAs is far from complete from the point of view of

(i) reduction in number of ABBs employed,

(ii) employment of only grounded capacitors,

(iii) employment of optimum number of passive components for achieving a given tunability specification and

(iv) increased the functionality.

Except the work presented in [24–26, 30, 35, 38], no mixed mode biquad filter structure which can operate in all the four modes and can realize the five generic filter responses has been reported so far in open literature.

Therefore, in the following, we present four/five OTAs and two grounded capacitors based MISO type VM universal biquad filter topologies and a mixed mode universal biquad structure which will fill the void in the literature as indicated above.

2.2 VM Universal Biquad Filter Employing Five OTAs[1]

The first proposed universal biquad filter circuit of a MISO type in VM is presented below in Fig. 2.8.

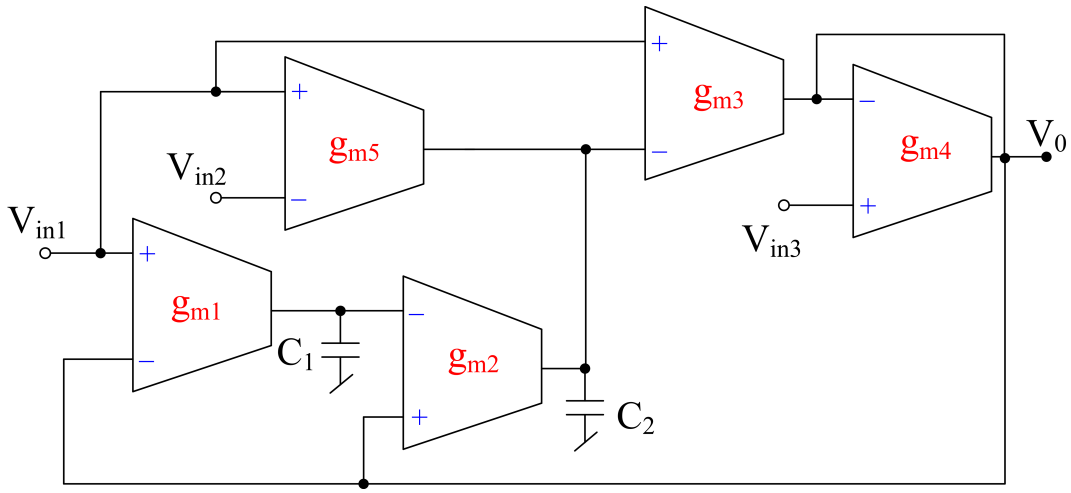


Figure 2.8: First proposed configuration of VM biquad filter

A routine circuit analysis of the circuit, using the ideal terminal relationships of an OTA, yields the following expression for the output voltage in terms of the input voltages:

$$V_0(s) = \frac{AV_{in1}(s) + BV_{in2}(s) + s^2V_{in3}(s)}{s^2 + \left(\frac{g_{m2}g_{m3}}{C_2g_{m4}}\right)s + \left(\frac{g_{m1}g_{m2}g_{m3}}{C_1C_2g_{m4}}\right)} \tag{2.1}$$

where

$$A = \{\left(\frac{g_{m3}}{g_{m4}}\right)s^2 - \left(\frac{g_{m3}g_{m5}}{C_2g_{m4}}\right)s + \left(\frac{g_{m1}g_{m2}g_{m3}}{C_1C_2g_{m4}}\right)\};\ and\ B = \left(\frac{g_{m3}g_{m5}}{C_2g_{m4}}\right)s$$

The various second-order filter functions can now be derived from equation (2.1) by proper selection of input voltages as follows:

[1]The material presented in this section has been published in: Ajishek Raj, D. R. Bhaskar, and Pragati Kumar, "Multiple-Input Single-Output Universal Biquad Filter Using Single Output OTAs" In 2nd IEEE International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), pp. 1237-1240, 2018, New Delhi.

(i) LPF: if $V_{in1} = V_{in2} = -V_{in3} = V_{in}$ (input voltage signal), and $g_{m3} = g_{m4}$

$$\frac{V_0(s)}{V_{in}(s)} = \frac{\left(\frac{g_{m1}g_{m2}g_{m3}}{C_1C_2g_{m4}}\right)}{D(s)}$$

(ii) HPF: if $V_{in1} = V_{in2} = 0$ and $V_{in3} = V_{in}$

$$\frac{V_0(s)}{V_{in}(s)} = \frac{s^2}{D(s)}$$

(iii) BPF: if $V_{in1} = V_{in3} = 0$ and $V_{in2} = V_{in}$

$$\frac{V_0(s)}{V_{in}(s)} = \frac{\left(\frac{g_{m3}g_{m5}}{C_2g_{m4}}\right)s}{D(s)}$$

(iv) BRF: if $V_{in3} = 0$, $V_{in1} = V_{in2} = V_{in}$, and $g_{m3} = g_{m4}$

$$\frac{V_0(s)}{V_{in}(s)} = \frac{\left(s^2 + \frac{g_{m1}g_{m2}g_{m3}}{C_1C_2g_{m4}}\right)}{D(s)}$$

(v) APF: if $V_{in1} = V_{in}$, $V_{in2} = V_{in3} = 0$, $g_{m2} = g_{m5}$ and $g_{m3} = g_{m4}$

$$\frac{V_0(s)}{V_{in}(s)} = \frac{s^2 - \left(\frac{g_{m2}g_{m3}}{C_2g_{m4}}\right)s + \left(\frac{g_{m1}g_{m2}}{C_1C_2}\right)}{D(s)}$$

where

$$D(s) = s^2 + \left(\frac{g_{m2}g_{m3}}{C_2g_{m4}}\right)s + \left(\frac{g_{m1}g_{m2}g_{m3}}{C_1C_2g_{m4}}\right) \tag{2.2}$$

Different filter parameters namely, pole frequency (ω_0), bandwidth (BW) and quality factor (Q_0) of the proposed filter configuration can be derived from equation (2.2) and are given by:

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}g_{m3}}{g_{m4}C_1C_2}}, BW = \frac{g_{m2}g_{m3}}{g_{m4}C_2}, and\ Q_0 = \sqrt{\frac{C_2g_{m1}g_{m4}}{g_{m2}g_{m3}C_1}} \tag{2.3}$$

From equation (2.3), it is evident that ω_0 and BW are orthogonally programmable through the transconductance g_{m1} (i.e., after fixing the value of BW, the ω_0 can be

controlled with g_{m1}).

The gain, in all the filter functions shown in Fig. 2.8 are given as:

$$H_{LPF} = H_{HPF} = H_{BRF} = H_{APF} = 1 \;\; and \;\; H_{BPF} = \frac{g_{m5}}{g_{m2}}$$

where H denotes the gain of the filter. From the expression of gain of BPF, it may be noted that the gain of BPF can be independently tuned through transconductor g_{m5}.

2.2.1 Sensitivity Analysis

The sensitivities of ω_0 and Q_0 with respect to $g_{mi}(i \rightarrow 1-5)$ and $C_i(i \rightarrow 1-2)$ have been evaluated and found as:

$$S_{gm1}^{\omega_0} = S_{gm2}^{\omega_0} = S_{gm3}^{\omega_0} = S_{gm1}^{Q_0} = S_{gm4}^{Q_0} = S_{C_2}^{Q_0} = 0.5$$

$$S_{gm4}^{\omega_0} = S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = S_{gm2}^{Q_0} = S_{gm3}^{Q_0} = S_{C_1}^{Q_0} = -0.5$$

Thus, all active and passive sensitivities are small.

2.2.2 Simulation Results

To validate the workability of the filter structure presented in Fig. 2.8, the circuit was simulated using macro model of LM13700 type OTA. To bias the OTAs, symmetrical DC power supplies of ± 15 V were used. The filter circuit was designed for a nominal frequency of 50 kHz and quality factor of 0.707 by taking identical transconductance values of $g_{m1}, g_{m2}, g_{m3}, g_{m4}$, and g_{m5} = 10.5 m℧. The capacitors C_1 =47 nF, and C_2 = 23.4 5 nF were used. The frequency responses of LPF, HPF, BPF, BRF and APF have been depicted in Fig. 2.9, whereas, the magnitude and phase responses of APF have been displayed in Fig. 2.10.

In Fig. 2.11, we have displayed the transient responses of input and output voltages of APF.

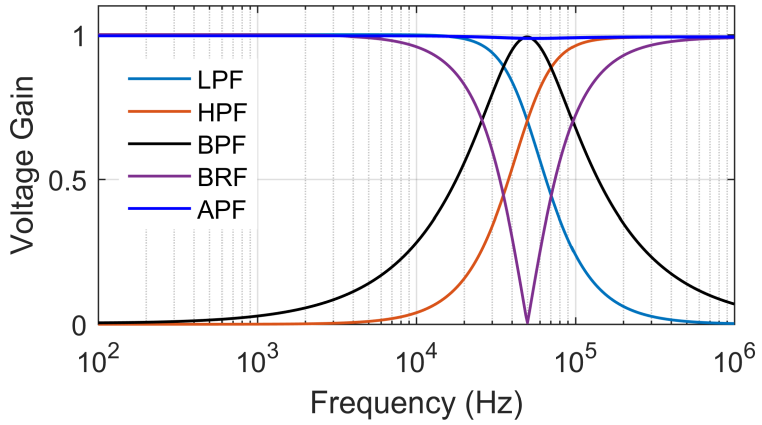


Figure 2.9: Frequency responses of filters of Fig. 2.8

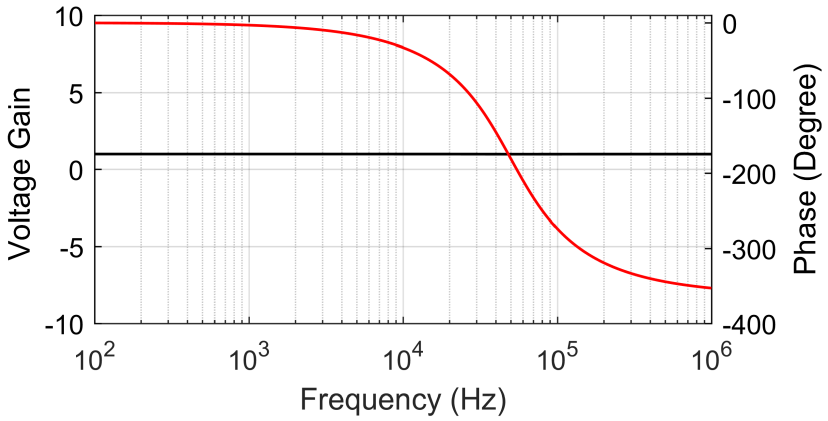


Figure 2.10: Phase responses of APF of Fig. 2.8

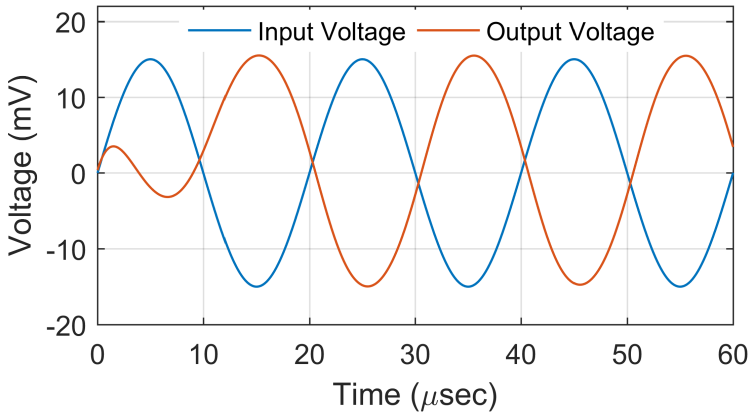


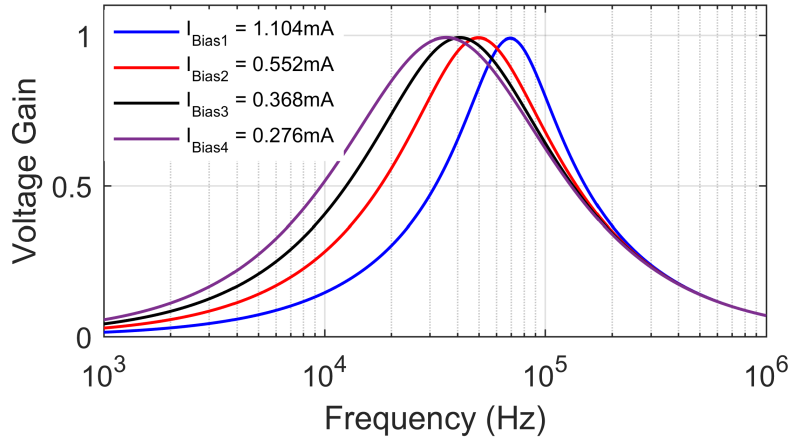
Figure 2.11: Input and output transient responses of APF of Fig. 2.8

2.2.3 Tuning of ω_0 and BW

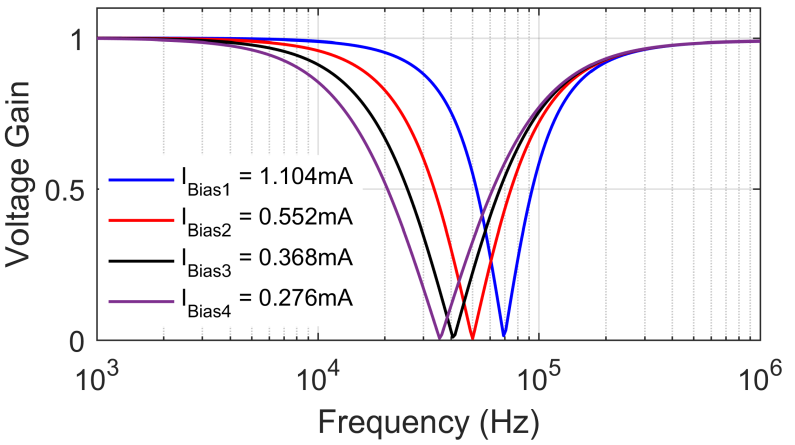
It is observed from equation (2.3) that the BW and ω_0 are orthogonally tunable, i.e., ω_0 can be electronically tuned without changing the BW by varying g_{m1}. To

demonstrate the orthogonal tuning of the pole frequency and the BW, the filter configuration of Fig. 2.8 was designed for the nominal value of the $f_0 = \left(\frac{\omega_0}{2\pi}\right) = 50$ kHz, BW = 71.49 kHz, quality factor = 0.707 and gain = 1 by taking $g_{mi}(i \rightarrow 1-5)$ = 10.5 m℧, $C_1 = 47$ nF and $C_2 = 23.45$ nF. I_{Bias} of 548 μA (for all the OTAs) was used to bias the OTAs.

To confirm the controllability of f_0 without changing the bandwidth, we have used I_{Bias1} = 0.276 mA, 0.368 mA, 0.552 mA and 1.104 mA to get the variations in cut-off frequencies as 36.76 kHz, 41.12 kHz, 50.429 kHz and 69.589 kHz respectively for the BPF and BRF. These results have been shown in Fig. 2.12a and 2.12b for BPF and BRF respectively. It may be noted that the BW remained constant at 71.3 kHz for both BPF and BRF.



(a)



(b)

Figure 2.12: Electronic tunability of ω_0 (a) BPF (b) BRF

2.3 VM Universal Biquad Filters using Four OTAs[2]

The VM universal filter structure presented in Figure 2.8 realizes all the second order filter functions by appropriate selection(s) of input voltages but it has some limitations to realize some of the filter functions i.e, a voltage inversion is needed, which requires an additional circuitry. To overcome the limitations of Fig. 2.8, two different filter configurations have been presented in this section.

Fig. 2.13 shows the new VM universal biquad filter employing four OTAs and two grounded capacitors.

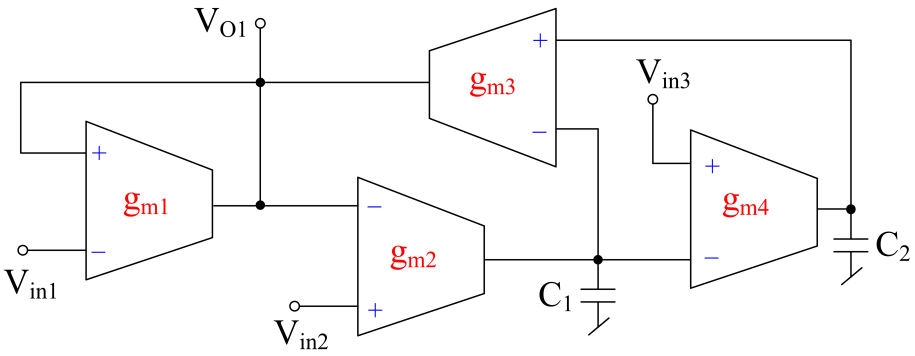


Figure 2.13: Four OTA-based first VM biquad filter structure

Assuming ideal OTAs, a straightforward circuit analysis of the circuit of Fig. 2.13 yields the expression for the output voltage in terms of the three input voltages:

$$V_{O1}(s) = \frac{s^2 V_{in1}(s) - s(\frac{g_{m3}g_{m4}}{C_2 g_{m1}} V_{in3}(s) - \frac{g_{m2}g_{m3}}{C_1 g_{m1}}) V_{in2}(s) + \frac{g_{m2}g_{m3}g_{m4}}{C_1 C_2 g_1} V_{in2}(s)}{D_1(s)} \quad (2.4)$$

where

$$D_1(s) = s^2 + (\frac{g_{m2}g_3 m}{C_1 g_1}) + (\frac{g_{m2}g_{m3}g_{m4}}{C_1 C_2 g_{m1}}) \quad (2.5)$$

From equation (2.4), the various filter responses can be derived as follows:

[2]The material presented in this section has been published in: Ajishek Raj, Pragati Kumar, and D. R. Bhaskar, "Multiple-Input Single-Output Universal Biquad Filters Using Reduced Number of OTAs" In International Symposium on Advanced Electrical and Communication Technologies (ISAECT), pp. 1-4. IEEE, 2019, Rome.

i. HP: if $V_{in2} = V_{in3} = 0$ and $V_{in1} = V_{in}$ (input signal)

$$\frac{V_{O1}(s)}{V_{in}(s)} = \frac{s^2}{D_1(s)}$$

ii. LP: if $V_{in1} = 0$, $V_{in2} = V_{in3} = V_{in}$, $g_{m2} = g_{m4}$ and $C_1 = C_2$

$$\frac{V_{O1}(s)}{V_{in}(s)} = \frac{(\frac{g_{m2}g_{m3}g_{m4}}{C_1C_2g_1})}{D_1(s)}$$

iii. BP: if $V_{in1} = V_{in2} = 0$ and $V_{in3} = V_{in}$

$$\frac{V_{O1}(s)}{V_{in}(s)} = \frac{-s(\frac{g_{m3}g_{m4}}{C_2g_{m1}})}{D_1(s)}$$

iv. BR: if $V_{in1} = V_{in2} = V_{in3} = V_{in}$, $g_{m2} = g_{m4}$ and $C_1 = C_2$

$$\frac{V_{O1}(s)}{V_{in}(s)} = \frac{s^2 + (\frac{g_{m2}g_{m3}g_{m4}}{C_1C_2g_{m1}})}{D_1(s)}$$

v. AP: if $V_{in1} = V_{in2} = 2V_{in3} = V_{in}$, $g_{m2} = g_{m4}$ and $C_1 = C_2$

$$\frac{V_{O1}(s)}{V_{in}(s)} = \frac{s^2 - s(\frac{g_{m2}g_{m3}}{C_1g_{m1}}) + (\frac{g_{m2}g_{m3}g_{m4}}{C_1C_2g_{m1}})}{D_1(s)}$$

The second configuration of four OTAs based VM universal filter is shown in Fig. 2.14. The expression of output voltage for the circuit of Fig. 2.14 (assuming ideal OTAs) is expressed as:

$$V_{O2}(s) = \frac{s^2(\frac{g_{m3}}{g_{m1}})V_{in1}(s) - s\left(\frac{g_{m3}g_{m4}}{C_1g_{m1}}V_{in3}(s) - \frac{g_{m2}}{C_1}V_{in2}(s)\right) + \frac{g_{m2}g_{m3}g_{m4}}{C_1C_2g_{m1}}V_{in2}(s)}{D_2(s)} \quad (2.6)$$

where

$$D_2(s) = s^2 + \left(s\frac{g_{m2}}{C_1}\right) + \left(\frac{g_{m2}g_{m3}g_{m4}}{C_1C_2g_{m1}}\right) \quad (2.7)$$

Equation (2.6) can be used to derive different filter responses as:

i. HP: if $V_{in2} = V_{in3} = 0$ and $V_{in1} = V_{in}$ (input signal)

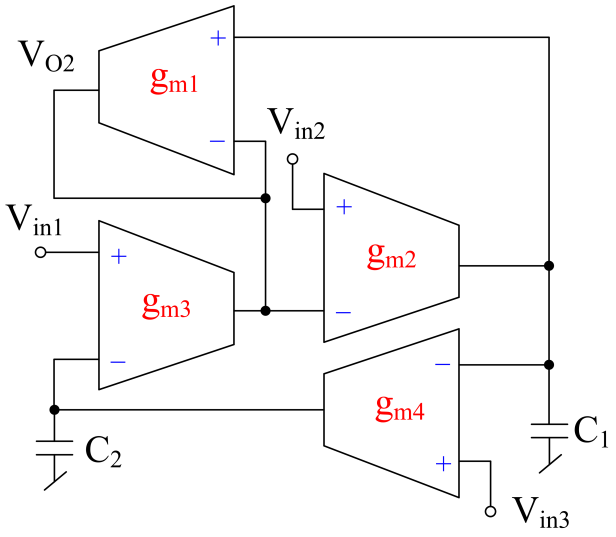


Figure 2.14: Second four OTA-based VM biquad filter topology

$$\frac{V_{O2}(s)}{V_{in}(s)} = \frac{s^2}{D_2(s)}$$

ii. LP: if $V_{in1} = 0$, $V_{in2} = V_{in3} = V_{in}$, $g_{m2} = g_{m4}$ and $C_1 = C_2$

$$\frac{V_{O2}(s)}{V_{in}(s)} = \frac{\left(\frac{g_{m2}g_{m3}g_{m4}}{C_1C_2g_{m1}}\right)}{D_2(s)}; g_{m1} = g_{m3}$$

iii. BP: if $V_{in1} = V_{in2} = 0$ and $V_{in3} = V_{in}$

$$\frac{V_{O2}(s)}{V_{in}(s)} = \frac{-s\left(\frac{g_{m3}g_{m4}}{C_1g_{m1}}\right)}{D_2(s)}$$

iv. BR: if $V_{in1} = V_{in2} = V_{in3} = V_{in}$, $g_{m2} = g_{m4}$ and $C_1 = C_2$

$$\frac{V_{O2}(s)}{V_{in}(s)} = \frac{s^2 + \left(\frac{g_{m2}g_{m3}g_{m4}}{C_1C_2g_{m1}}\right)}{D_2(s)}; g_{m1} = g_{m3}$$

v. AP: if $V_{in1} = V_{in2} = 2V_{in3} = V_{in}$, $g_{m2} = g_{m4}$ and $C_1 = C_2$

$$\frac{V_{O2}(s)}{V_{in}(s)} = \frac{s^2 - s\left(\frac{g_{m2}}{C_2}\right) + \left(\frac{g_{m2}g_{m3}g_{m4}}{C_1C_2g_{m1}}\right)}{D_2(s)}; g_{m1} = g_{m3}$$

The various filter parameters such as ω_0, Q_0, and BW of the circuits presented in Fig. 2.13 and Fig. 2.14 may be derived from equations (2.5) and (2.7) and are

given as:

$$Fig.\ 2.13 \quad \omega_0 = \sqrt{\frac{g_{m2}g_{m3}g_{m4}}{C_1C_2g_{m1}}},\ \ Q_{01} = \sqrt{\frac{C_1g_{m1}g_{m4}}{C_2g_{m2}g_{m3}}},\ \ BW_{01} = \frac{g_{m2}g_{m3}}{C_1g_{m1}} \tag{2.8}$$

$$Fig.\ 2.14 \quad \omega_0 = \sqrt{\frac{g_{m2}g_{m3}g_{m4}}{C_1C_2g_{m1}}},\ \ Q_{02} = \sqrt{\frac{C_2g_{m3}g_{m4}}{C_1g_{m1}g_{m2}}},\ \ BW_{02} = \frac{g_{m2}}{C_1} \tag{2.9}$$

From equation (2.8), it may be noted that, the filter parameters Q_{01} and ω_0 can be tuned orthogonally i.e., for a constant value of ω_0 , Q_{01} may be controlled by varying g_{m1} and g_{m4} simultaneously keeping its ratio (g_{m4}/g_{m1}) constant whereas, from equation (2.9), it may be observed that for Fig. 2.14, for a constant value of ω_0 , Q_{02} may be controlled by varying g_{m1} and g_{m2} simultaneously keeping its ratio (g_{m2}/g_{m1}) constant.

2.3.1 Sensitivity Analysis

The classical formula of sensitivity $S_x^{F(x)} = \frac{x}{F(x)}\frac{\partial F(x)}{\partial x}$ (where F(x) is function and x is a parameter of interest) has been used to evaluate different active and passive sensitivity cofficients of ω_0, Q_{0i} and BW_{0i} (i = 1–2) and are listed below in Table 2.1.

From Table 2.1, it is clear that active and passive sensitivities for both the proposed biquad structures are small.

Table 2.1: Active and passive sensivities of ω_0, Q_{0i} and BW_{0i}

x	g_{m1}	g_{m2}	g_{m3}	g_{m4}	C_1	C_2
$S_X^{\omega_0}$	-0.5	0.5	0.5	0.5	-0.5	-0.5
$S_X^{Q_{01}}$	0.5	-0.5	-0.5	0.5	0.5	-0.5
$S_X^{BW_{01}}$	-1	1	1	0	1	0
$S_X^{Q_{02}}$	-0.5	-0.5	0.5	0.5	-0.5	0.5
$S_X^{BW_{02}}$	0	1	0	0	-1	0

2.3.2 Simulation Results

The functionality of analog signal processing/generation circuits employing different AABs such as CCIIs, OTAs and CFOAs realized using CMOS/Bipolar technologies, can be validated either by employing some macro models of the OTA [69, 70], CCII [71, 72] and CFOA [73] or a transistor level implementation simulated in PSPICE. A transistor level realization of CMOS OTA [74] shown in Fig. 2.15 implemented in 0.18μm with TSMC technology parameters was used to simulate the proposed VM filters demonstrated in Fig. 2.13 and Fig. 2.14. These circuits were simulated in PSPICE program.

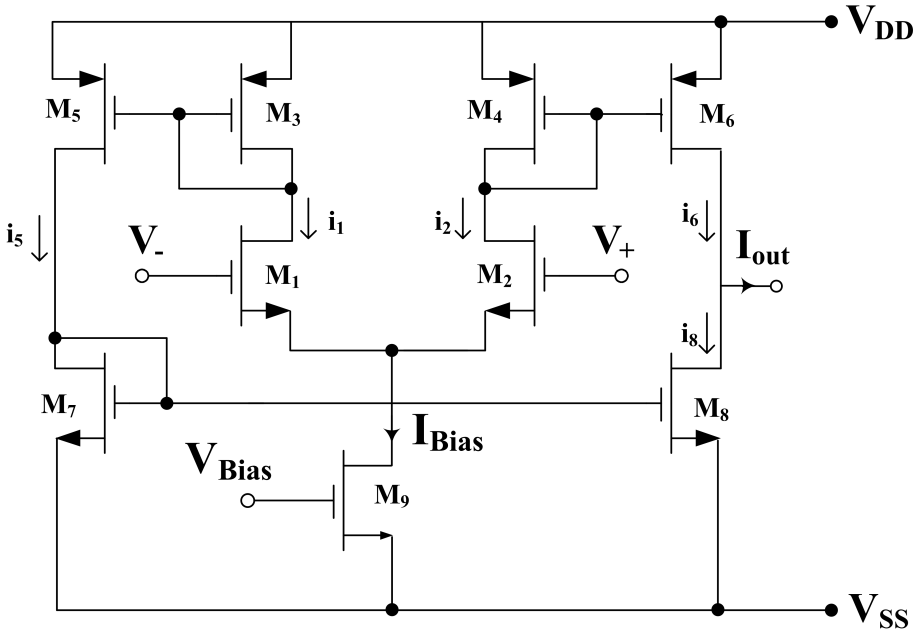


Figure 2.15: Exemplary CMOS implementation of OTA [74]

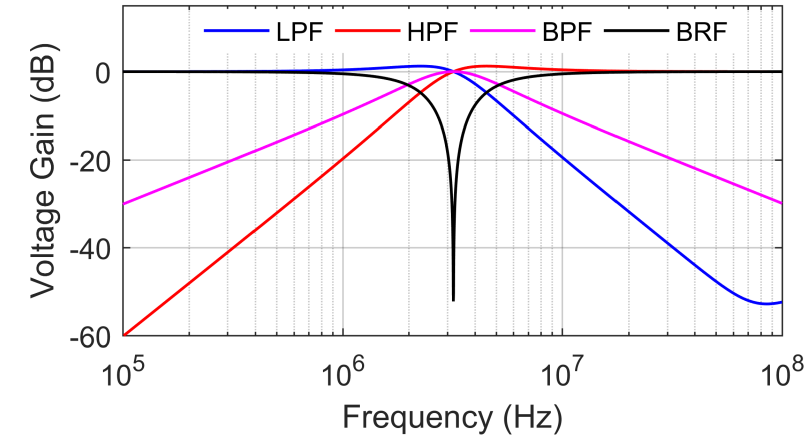
The aspect ratios for Fig. 2.15 are given in Table 2.2.

Table 2.2: Aspect ratio of MOSFETs shown in Fig. 2.15

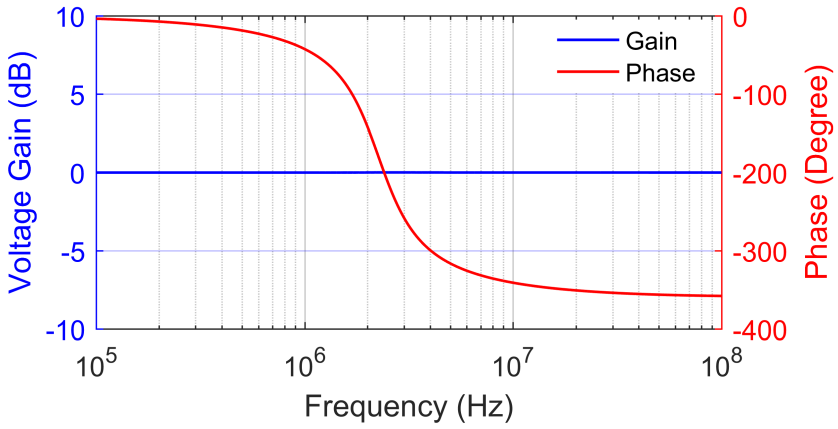
MOSFETs	Aspect Ratio (W/L)
M1, M2	3.6/0.36
M3, M4, M7, M8	1.44/0.36
M5, M6	2.88/0.36
M9	5.4/0.36

The DC power supplies used were ±0.9V and the equal valued transconductances

of 2m℧ for $I_{Bias} = 400\ \mu A$ were used in the simulation. The presented filters were simulated for a nominal designed frequency of $f_0 = 3.49$ MHz and $Q_0 = 1$ by selecting $g_{m1} = g_{m2} = g_{m3} = g_{m4} = 2$m℧, and $C_1 = C_2 = 100$pF for LPF, HPF, BPF and BRF. For the realization of APF, the values of capacitors were taken as $C_1 = 200$pF and $C_2 = 100$pF. Fig. 2.16 and Fig. 2.17 display the frequency responses of the proposed universal biquad filters of Fig. 2.13 and Fig. 2.14 respectively. Fig. 2.18 presents the tunability of Q_0 and gain with ω_0 of Fig. 2.14.

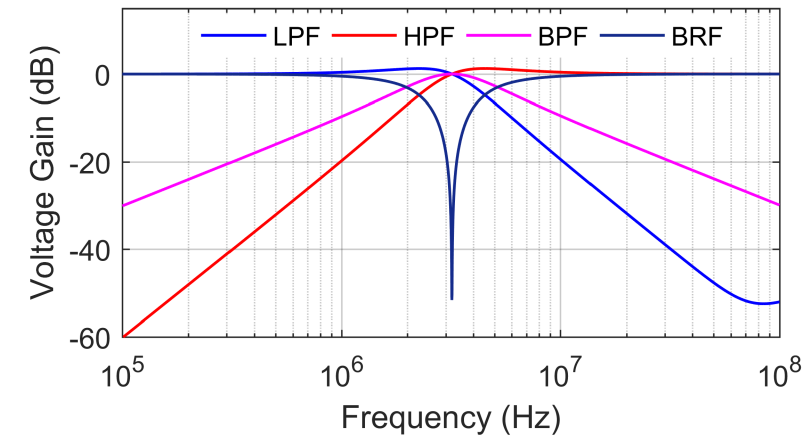


(a)

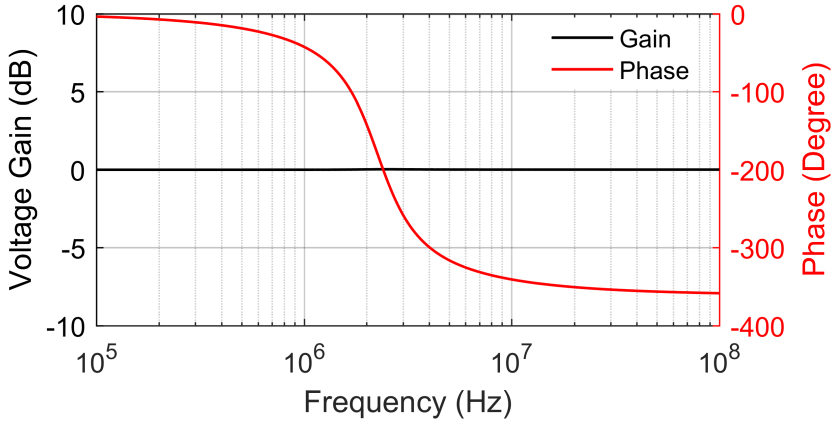


(b)

Figure 2.16: (a) Frequency responses of LPF, HPF, BPF, BRF (b) Frequency and phase responses of APF of Fig. 2.13



(a)



(b)

Figure 2.17: (a) Frequency responses of LPF, HPF, BPF, BRF (b) Frequency and phase responses of APF of Fig. 2.14

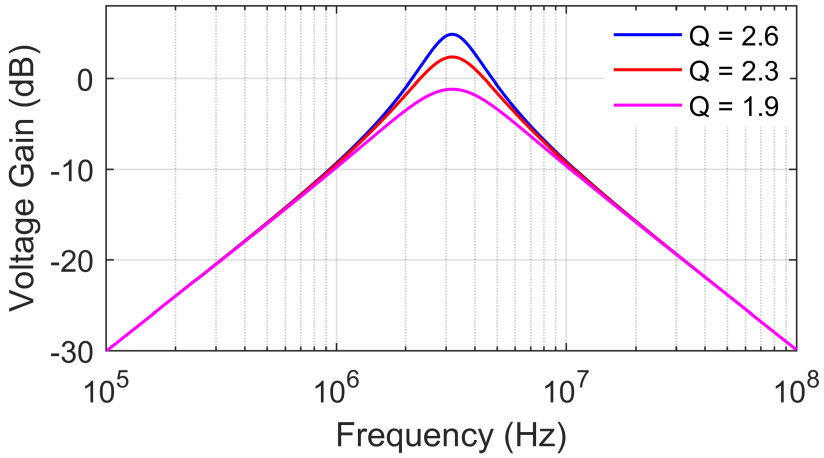


Figure 2.18: Tunability of ω_1 with gain and Q_{01} of proposed biquad filter of Fig. 2.13

2.3.3 Monte-Carlo Simulations

To study the effect of mismatches in the values of the capacitors on the performance of the filter circuit (BPF), Monte-Carlo simulations have been performed by allocating 5% tolerances to the component values $C_1 = C_2 = 100$ pF with 100 runs. Fig. 2.19 shows the histogram of Monte-Carlo simulations for the BPF realized from the proposed configuration of Fig. 2.13. From this statistical result, the deviation in frequency is found to be 13.341kHz. These results, thus, indicate that the mismatch in the component values does not have a significant effect on the realized cut-off frequency of the proposed biquad filter.

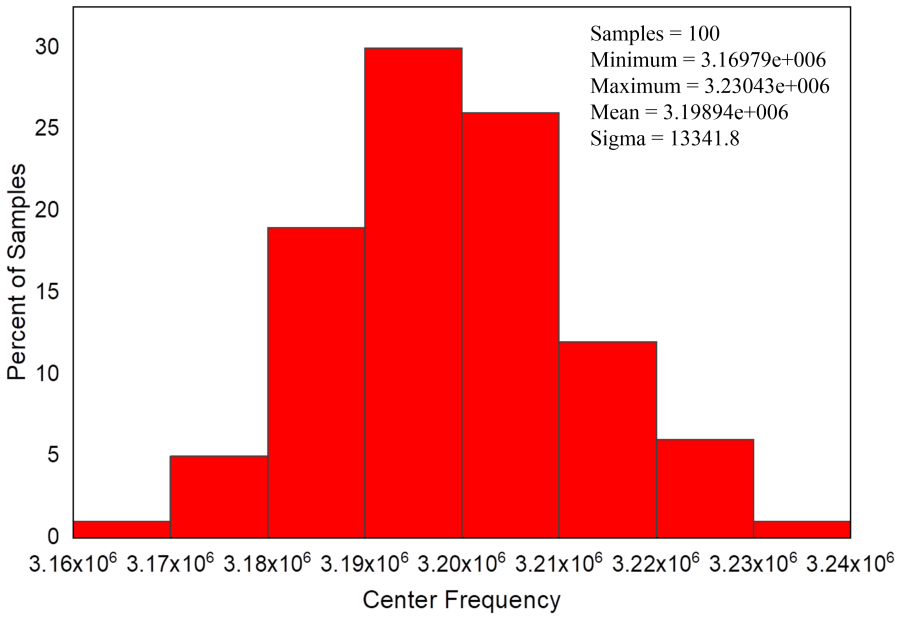


Figure 2.19: Monte-Carlo simulation results of BPF of Fig. 2.13

2.3.4 Noise Analysis

Noise analyses have also been carried out using PSPICE simulations for the proposed biquad filters realized from the circuit given in Fig. 2.13. The output noise in the range of 1 kHz to 5 GHz was found to be below 0.016μV/sqrt(Hz) and 0.018μV/sqrt(Hz) respectively for the circuits of Fig. 2.13 and Fig. 2.14 respectively. These results have been shown in Fig. 2.20

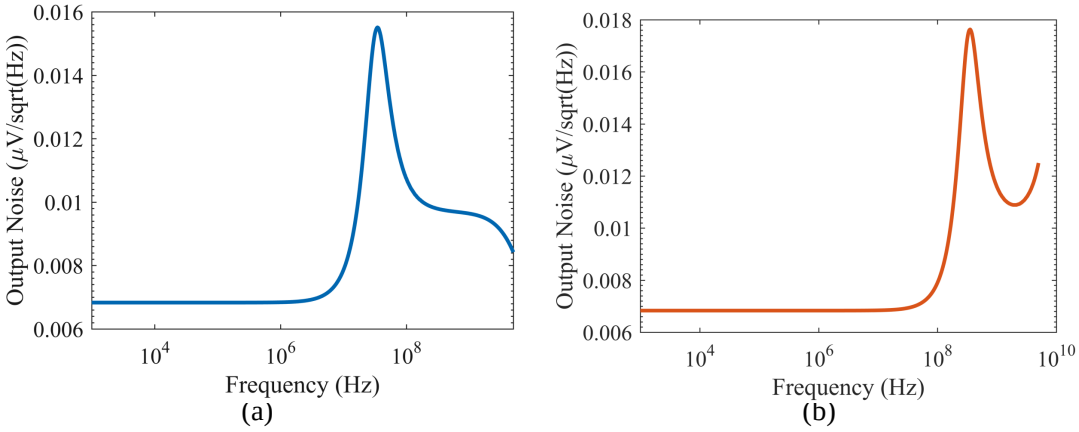


Figure 2.20: Simulation results of output noise for (a) Fig 2.13 (b) Fig 2.14

The power consumption of the biquad filter topologies (measured in PSPICE) was found to be 4.32 mW.

2.3.5 Layout Design of the Proposed Biquad Filter Circuit of Fig. 2.14

We have also made the complete layout of the VM filter derived from the circuit of Fig. 2.14 using Cadence Virtuoso and carried out pre/post layout simulations verifying the design of the filters in integrated circuit form (Fig. 2.21). The total active die area required is 393.484μm^2 (26.32μm x 14.95μm). In the layout simulations, we have used pmoscap of value 100 pF.

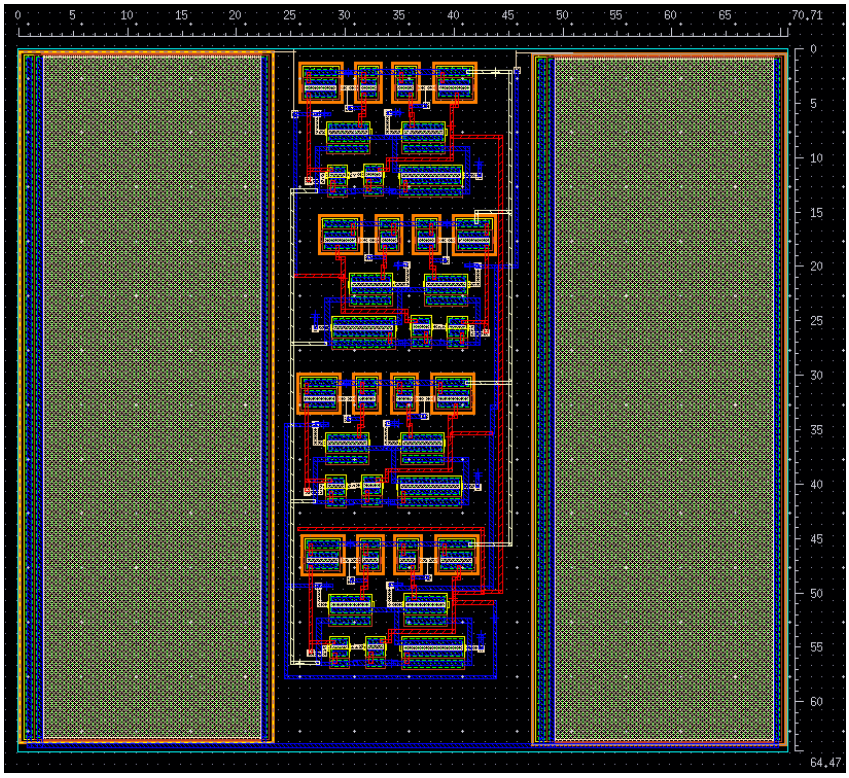


Figure 2.21: Layout design of proposed VM filter configuration of Fig. 2.14

2.4 Mixed Mode Universal Biquad Filter Employing Five OTAs and Two Grounded Capacitors

The biquad filter configurations presented in Fig. 2.8, Fig. 2.13 and Fig. 2.14 can yield universal biquad filters in VM only. In the following, we now present a universal filter structure in which all the generic filter functions are available in all the four modes (VM, CM, TRM, TCM).

2.4.1 Proposed Mixed Mode Filter Configuration[3]

The proposed mixed mode filter structure is shown in Figure 2.22.

Assuming ideal OTAs, a straightforward analysis of the circuit shown in Fig. 2.22 yields the following expressions for the output voltage $V_0(s)$ and output current $I_0(s)$

[3]The material presented in this section has been published in: D. R. Bhaskar, Ajishek Raj, and Pragati Kumar. "Mixed-mode universal biquad filter using OTAs." Journal of Circuits, Systems and Computers, vol. 29, no. 10 (2020): 2050162.

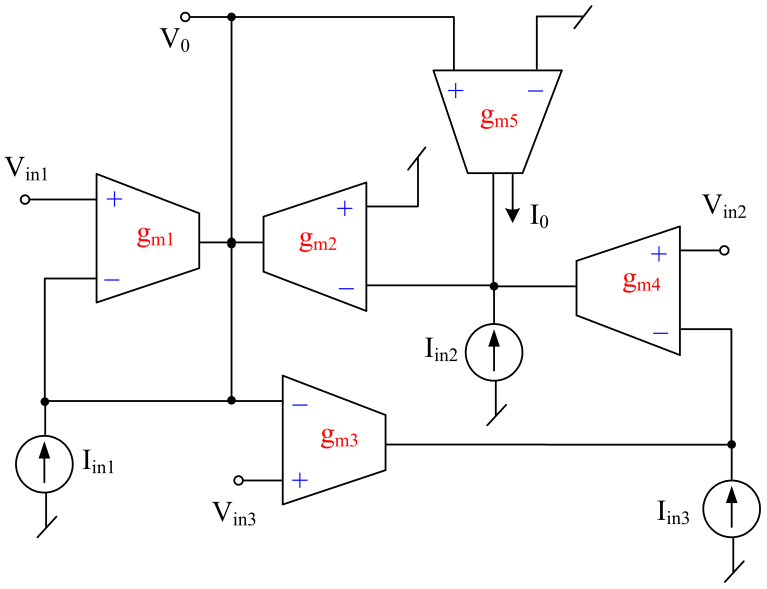


Figure 2.22: Proposed mixed mode OTA-C universal biquad filter configuration

in terms of the three input voltages and three input currents, respectively as:

$$V_0(s) = \left(\frac{N_1(s) + N_2(s)}{D(s)}\right) \tag{2.10}$$

$$I_0(s) = g_{m5} V_0(s) \tag{2.11}$$

where

$$N_1(s) = s^2 V_{in1}(s) - s\left(\frac{g_{m2}g_{m4}}{C_2 g_{m1}}\right) V_{in2}(s) + \left(\frac{g_{m2}g_{m3}g_{m4}}{C_1 C_2 g_{m1}}\right) V_{in3}(s) \tag{2.12}$$

$$N_2(s) = s^2\left(\frac{1}{g_{m1}}\right) I_{in1}(s) - s\left(\frac{g_{m2}}{C_2 g_{m1}}\right) I_{in2}(s) + \left(\frac{g_{m2}g_{m4}}{C_1 C_2 g_{m1}}\right) I_{in3}(s) \tag{2.13}$$

and

$$D(s) = s^2 + s\left(\frac{g_{m2}g_{m5}}{C_2 g_{m1}}\right) + \left(\frac{g_{m2}g_{m3}g_{m4}}{C_1 C_2 g_{m1}}\right) \tag{2.14}$$

From equations (2.10) and (2.11), the various second-order filter responses in all the four modes, can be derived by appropriate choice(s) of input voltage(s) and current(s) as follows.

Case I: If $I_{in1} = I_{in2} = I_{in3}$= 0, the following VM responses, and TCM responses can be obtained:

VM Responses

(i) LPF: if $V_{in1} = V_{in2} = 0$, $V_{in3} = V_{in}$

$$\frac{V_0(s)}{V_{in}(s)} = \frac{\left(\frac{g_{m2}g_{m3}g_{m4}}{C_1C_2g_{m1}}\right)}{D(s)}$$

(ii) HPF: if $V_{in2} = V_{in3} = 0$ and $V_{in1} = V_{in}$

$$\frac{V_0(s)}{V_{in}(s)} = \frac{s^2}{D(s)}$$

(iii) BPF: if $V_{in1} = V_{in3} = 0$ and $V_{in2} = V_{in}$

$$\frac{V_0(s)}{V_{in}(s)} = -\frac{\left(\frac{g_{m2}g_{m4}}{C_2g_{m1}}\right)s}{D(s)}$$

(iv) BRF: if $V_{in2} = 0$, $V_{in1} = V_{in3} = V_{in}$

$$\frac{V_0(s)}{V_{in}(s)} = \frac{\left(s^2 + \frac{g_{m2}g_{m3}g_{m4}}{C_1C_2g_{m1}}\right)}{D(s)}$$

(v) APF: if $V_{in1} = V_{in2} = V_{in3} = V_{in}$, and $g_{m4} = g_{m5}$

$$\frac{V_0(s)}{V_{in}(s)} = \frac{s^2 - \left(\frac{g_{m2}g_{m4}}{C_2g_{m1}}\right)s + \left(\frac{g_{m2}g_{m3}g_{m4}}{C_1C_2g_{m1}}\right)}{D(s)}$$

TCM Responses

(i) LPF: if V_{in1} =V_{in2} = 0, $V_{in3} = V_{in}$

$$\frac{I_0(s)}{V_{in}(s)} = \frac{g_{m5}\left(\frac{g_{m2}g_{m3}g_{m4}}{C_1C_2g_{m1}}\right)}{D(s)}$$

(ii) HPF: if $V_{in2} = V_{in3} = 0$ and $V_{in1} = V_{in}$

$$\frac{I_0(s)}{V_{in}(s)} = \frac{g_{m5}(s^2)}{D(s)}$$

(iii) BPF: if $V_{in1} = V_{in3} = 0$ and $V_{in2} = V_{in}$

$$\frac{I_0(s)}{V_{in}(s)} = -\frac{g_{m5}\left(\frac{g_{m2}g_{m4}}{C_2g_{m1}}\right)s}{D(s)}$$

(iv) BRF: if $V_{in2} = 0$, $V_{in1} = V_{in3} = V_{in}$

$$\frac{I_0(s)}{V_{in}(s)} = \frac{g_{m5}\left(s^2 + \frac{g_{m2}g_{m3}g_{m4}}{C_1C_2g_{m1}}\right)}{D(s)}$$

(v) APF: if $V_{in1} = V_{in2} = V_{in3} = V_{in}$, and $g_{m4} = g_{m5}$

$$\frac{I_0(s)}{V_{in}(s)} = \frac{g_{m5}\left(s^2 - \left(\frac{g_{m2}g_{m4}}{C_2g_{m1}}\right)s + \left(\frac{g_{m2}g_{m3}g_{m4}}{C_1C_2g_{m1}}\right)\right)}{D(s)}$$

Case I: If $V_{in1} = V_{in2} = V_{in3}$= 0, the following CM responses, and TRM responses can be obtained:

CM Responses

(i) LPF: if I_{in1} =1_{in2} = 0, $I_{in3} = I_{in}$

$$\frac{I_0(s)}{I_{in}(s)} = \frac{\left(\frac{g_{m2}g_{m4}g_{m5}}{C_1C_2g_{m1}}\right)}{D(s)}$$

(ii) HPF: if $I_{in2} = I_{in3} = 0$ and $I_{in1} = I_{in}$

$$\frac{I_0(s)}{I_{in}(s)} = \frac{\left(\frac{g_{m5}}{g_{m1}}\right)(s^2)}{D(s)}$$

(iii) BPF: if $I_{in1} = I_{in3} = 0$ and $I_{in2} = I_{in}$

$$\frac{I_0(s)}{I_{in}(s)} = -\frac{\left(\frac{g_{m2}g_{m5}}{C_2 g_{m1}}\right)s}{D(s)}$$

(iv) BRF: if $I_{in2} = 0$, $I_{in1} = I_{in3} = I_{in}$, and $g_{m1} = g_{m3} = g_{m5}$

$$\frac{I_0(s)}{I_{in}(s)} = \frac{\left(\frac{g_{m5}}{g_{m1}}\right)\left(s^2 + \frac{g_{m2}g_{m3}g_{m4}}{C_1 C_2 g_{m1}}\right)}{D(s)}$$

(v) APF: if $I_{in1} = I_{in2} = I_{in3} = I_{in}$, and $g_{m1} = g_{m3} = g_{m5}$

$$\frac{I_0(s)}{I_{in}(s)} = \frac{\left(s^2 - \left(\frac{g_{m2}g_{m5}}{C_2 g_{m1}}\right)s + \left(\frac{g_{m2}g_{m3}g_{m4}}{C_1 C_2 g_{m1}}\right)\right)}{D(s)}$$

TRM Responses

(i) LPF: if $I_{in1} = 1_{in2} = 0$, $I_{in3} = I_{in}$

$$\frac{I_0(s)}{I_{in}(s)} = \frac{\left(\frac{1}{g_{m3}}\right)\left(\frac{g_{m2}g_{m4}g_{m5}}{C_1 C_2 g_{m1}}\right)}{D(s)}$$

(ii) HPF: if $I_{in2} = I_{in3} = 0$ and $I_{in1} = I_{in}$

$$\frac{I_0(s)}{I_{in}(s)} = \frac{\left(\frac{1}{g_{m3}}\right)(s^2)}{D(s)}$$

(iii) BPF: if $I_{in1} = I_{in3} = 0$ and $I_{in2} = I_{in}$

$$\frac{I_0(s)}{I_{in}(s)} = -\frac{\left(\frac{g_{m2}}{C_2 g_{m1}}\right) s}{D(s)}$$

(iv) BRF: if $I_{in2} = 0$, $I_{in1} = I_{in3} = I_{in}$, and $g_{m1} = g_{m3}$

$$\frac{I_0(s)}{I_{in}(s)} = \frac{\left(\frac{1}{g_{m1}}\right)\left(s^2 + \frac{g_{m2}g_{m3}g_{m4}}{C_1 C_2 g_{m1}}\right)}{D(s)}$$

(v) APF: if $I_{in1} = I_{in2} = I_{in3} = I_{in}$

$$\frac{I_0(s)}{I_{in}(s)} = \frac{\left(\frac{1}{g_{m1}}\right)\left(s^2 - \left(\frac{g_{m2}g_{m5}}{C_2 g_{m1}}\right) s + \left(\frac{g_{m2}g_{m3}g_{m4}}{C_1 C_2 g_{m1}}\right)\right)}{D(s)}$$

Thus, it is clear that all second-order filter responses are realizable by proper selection of the input signals. The cut-off frequency ($\omega = 2\pi f_0$), bandwidth (BW) and quality factor (Q_0) for this biquad filter structure are given by:

$$\omega_0 = 2\pi f_0 = \sqrt{\frac{g_{m2}g_{m3}g_{m4}}{C_1 C_2 g_{m1}}} \tag{2.15}$$

$$BW = \frac{g_{m2}g_{m5}}{C_2 g_{m1}} \tag{2.16}$$

$$Q = \frac{1}{g_{m5}}\sqrt{\frac{C_2 g_{m1} g_{m3} g_{m4}}{C_1 g_{m2}}} \tag{2.17}$$

It may be observed from equations (2.15) and (2.16) that, f_0 and BW are orthogonally adjustable; f_0 can be adjusted through the transconductance g_{m3} while the BW is being kept fixed. The expressions of gain for different filter configurations in various modes of operation have also been derived and are given below in Table 2.3.

Table 2.3: Gain of the various filter functions

Functions	VM	CM	TCM	TRM
LPF	1	$\frac{g_{m5}}{g_{m3}}$	g_{m5}	$\frac{1}{g_{m3}}$
HPF	1	$\frac{g_{m5}}{g_{m1}}$	g_{m5}	$\frac{1}{g_{m3}}$
BPF	-$\frac{g_{m4}}{g_{m5}}$	-1	$-g_{m4}$	$-\frac{1}{g_{m5}}$
BRF	1	$\frac{g_{m5}}{g_{m3}}$	g_{m5}	$\frac{1}{g_{m1}}$
APF	1	1	g_{m5}	$\frac{1}{g_{m1}}$

2.4.1.1 Sensitivity Analysis

Using the classical definition of sensitivity, the sensitivities of ω, and BW with respect to g_{mi} $(i \rightarrow 1-5)$ and C_i $(i \rightarrow 1-2)$ can be determined as:

$$S^{\omega}_{gm1} = -0.5, S^{\omega}_{gm2} = S^{\omega}_{gm3} = S^{\omega}_{gm4} = 0.5, S^{\omega}_{gm5} = 0 S^{\omega}_{C_1} = S^{\omega}_{C_2} = -0.5$$

$$S^{BW}_{gm1} = S^{BW}_{C_2} = -1, S^{BW}_{gm2} = S^{BW}_{gm4} = 1, S^{BW}_{gm3} = S^{BW}_{gm5} = S^{BW}_{C_1} = 0$$

Thus, all active and passive sensitivities are small.

2.4.2 Non-Ideal Analysis

The circuit behaviour of a real OTA is different from its ideal model. Several non-ideal models of the OTA have been proposed in open literature from time to time [51, 69, 75]. Fig. 2.23 shows some of the popular non-ideal models of an OTA.

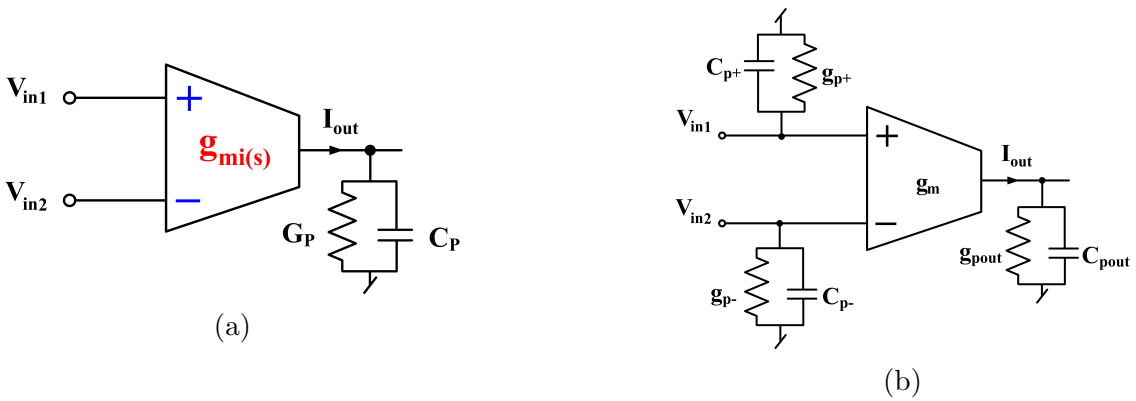


Figure 2.23: Non-ideal models of OTA

It may be noticed from the proposed mixed mode filter circuit of Fig. 2.24 that the parasitic resistances and capacitances present at the non-inverting input terminals of the OTA_1, OTA_3 and OTA_4 will not affect the ideal transfer function while the output parasitic resistances and capacitances of OTA_1 and OTA_2 and input parasitic resistances and capacitances at inverting input terminals of OTA_1, OTA_3 and non-inverting input terminal of OTA_5 can be combined into a single equivalent resistance and single equivalent capacitance. Similarly the output parasitic resistances and capacitances of OTA_4 and OTA_5 are in parallel to the parasitic resistances and capacitances of the inverting input terminal of OTA_2. These three parasitic capacitances can be absorbed by the external capacitance C_2. Also, the parasitic resistance and capacitance at the output terminal of OTA_3 are combined with the parasitic capacitance and resistance at the inverting input terminal of OTA_4. At this node the two parasitic capacitances will be absorbed by the external capacitance C_1.

A routine analysis of the mixed mode universal biquad configuration shown in Fig. 2.24 using the OTA model (shown in Fig. **??**) yields the following non-ideal expressions for the output voltage and output current:

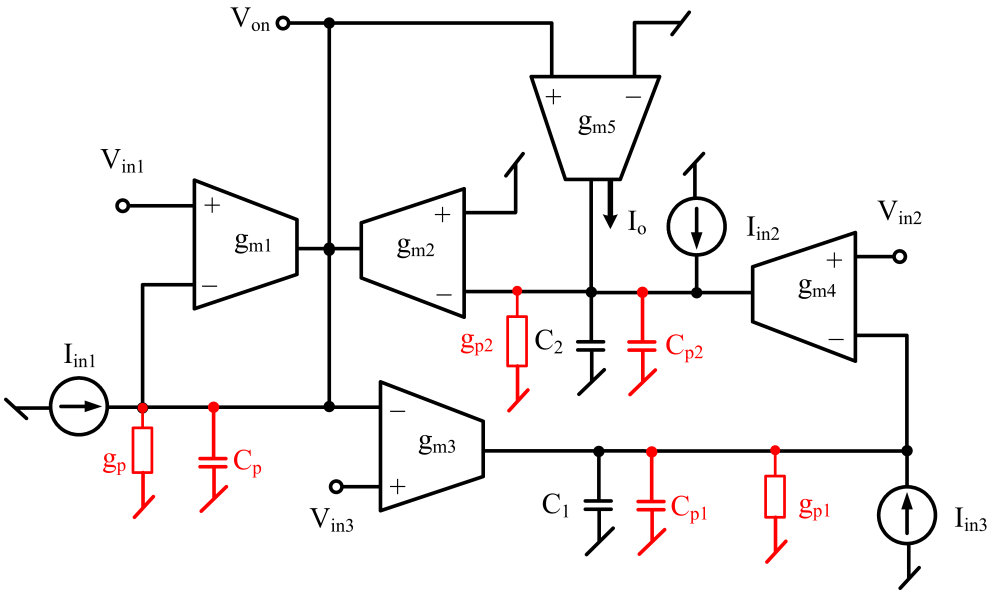


Figure 2.24: Mixed mode filter circuit with parasitic transconductances and capacitances

$$V_{on}(s) = \frac{N_{1n}(s) + N_{2n}(s)}{D_n(s)} \tag{2.18}$$

$$I_{on}(s) = g_{m5}V_{on}(s) \tag{2.19}$$

$$\begin{aligned} N_{1n}(s) = {} & s^2(g_{m1}C_1^pC_2^p)V_{in1} + s\{(g_{m1}C_1^pg_{p2} + g_{m1}C_2^pg_{p1})V_{in1} - (g_{m2}C_1^pg_{m4}V_{in2})\} \\ & + (g_{m1}g_{p1}g_{p2}V_{in1} - g_{m2}g_{m4}g_{p1}V_{in2} + g_{m2}g_{m3}g_{m4}V_{in3}) \end{aligned} \tag{2.20}$$

$$\begin{aligned} N_{2n}(s) = {} & s^2(C_1^pC_2^p)I_{in1} + s\{(C_1^pg_{p2} + C_2^pg_{p1})I_{in1} - (g_{m2}C_1^p)I_{in2}\} \\ & + (g_{p1}g_{p2}I_{in1} - g_{m2}g_{p1}I_{in2} + g_{m2}g_{m4}I_{in3}) \end{aligned} \tag{2.21}$$

$$\begin{aligned} D_n(s) = {} & s^3(C_pC_1^pC_2^p) + s^2\{C_1^pC_2^p(g_{m1}g_p) + C_p(C_1^pg_{p2} + C_2^pg_{p1}\} \\ & + s(g_{m1}g_{p2}C_1^p + g_{m1}g_{p1}C_2^p + g_p(g_{p1}C_2^p + g_pg_{p2}C_1^p + g_{p1}g_{p2}C_p + g_{m2}g_{m5}C_1^p) \\ & + (g_{m1}g_{p1}g_{p2} + g_pg_{p1}g_{p2} + g_{m2}g_{m5}g_{p1} + g_{m2}g_{m3}g_{m4}) \end{aligned} \tag{2.22}$$

where

$$g_p = (g_{p1-} + g_{p3-} + g_{p5+} + g_{pout1} + g_{pout2}), g_{p1} = (g_{p4-} + g_{pout3}), g_{p2} = (g_{p2-} + g_{pout4} + g_{pout5})$$

$$C_p = (C_{p1-} + C_{p3-} + C_{p5+} + C_{pout1} + C_{pout2}), C_1^p = (C_1 + C_{p4-} + C_{pout3})$$

$$C_2^p = (C_2 + C_{p2-} + C_{pout4} + C_{pout5})$$

From the above equations (2.20), (2.21) and (2.22), it may be observed that the values of the input parasitic resistances and input parasitic capacitances of CMOS OTAs are very small, since $sC_p << g_{m1}$; at the signal frequencies of interest and thus, the third order term in equation (2.22) may be neglected. The expressions for cut-off frequency and bandwidth are thus, obtained from the equation (2.22) and are given by:

$$f_0 = \frac{1}{2\pi}\sqrt{\left(\frac{g_{m1}g_{p1}g_{p2} + g_p g_{p1}g_{p2} + g_{m2}g_{m5}g_{p1} + g_{m2}g_{pm3}g_{m4}}{C_1^p C_2^p(g_{m1}g_p) + C_p(C_1^p g_{p2} + C_2^p g_{p1})}\right)}$$

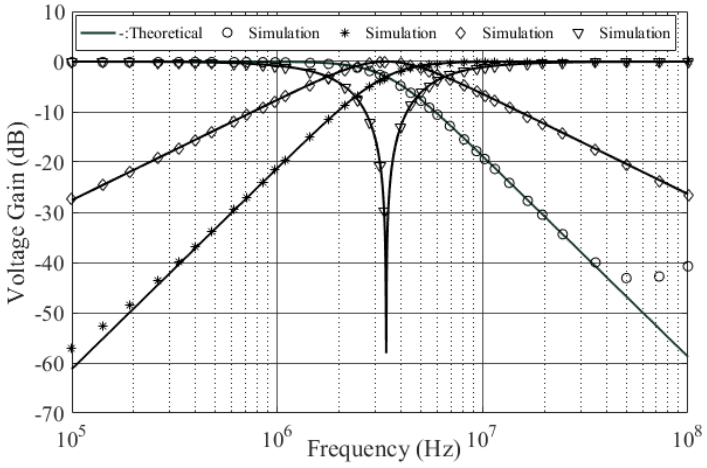
$$BW = \frac{C_1^p(g_{m1}g_{p2} + g_p g_{p2} + g_{m2}g_{m5}) + C_2^p(g_{m1}g_{p1} + g_p g_{p1}) + C_p g_{p1}g_{p2}}{C_1^p C_2^p(g_{m1}g_p) + C_p(C_1^p g_{p2} + C_2^p g_{p1})}$$

As the parasitic conductance $g_{pi\pm}$ (i $\rightarrow$ 1-5) and capacitances $C_{pi\pm}$ (i $\rightarrow$ 1-5) are very small, we have neglected them in calculating the values of these parameters from the non-ideal expressions. Considering other parasitic resistances and capacitances, the cut-off frequency and bandwidth are found to be 3.34 MHz and 30.15 MHz respectively which are very close to theoretically designed values (3.390 MHz and 30.196 MHz respectively).

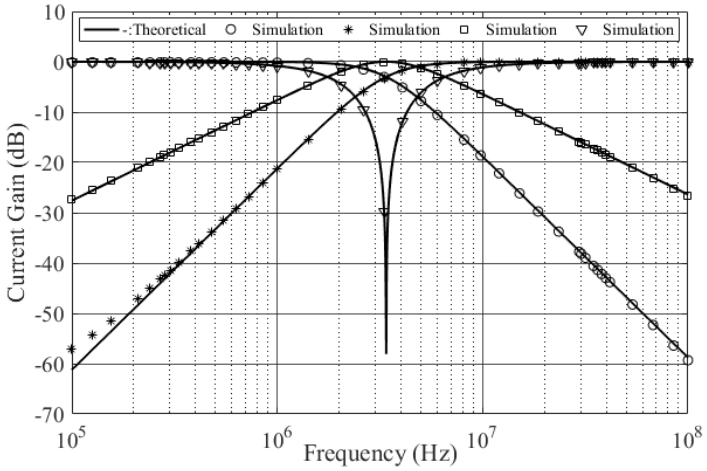
2.4.3 Simulation Results and Layout Design

2.4.3.1 Simulation Results

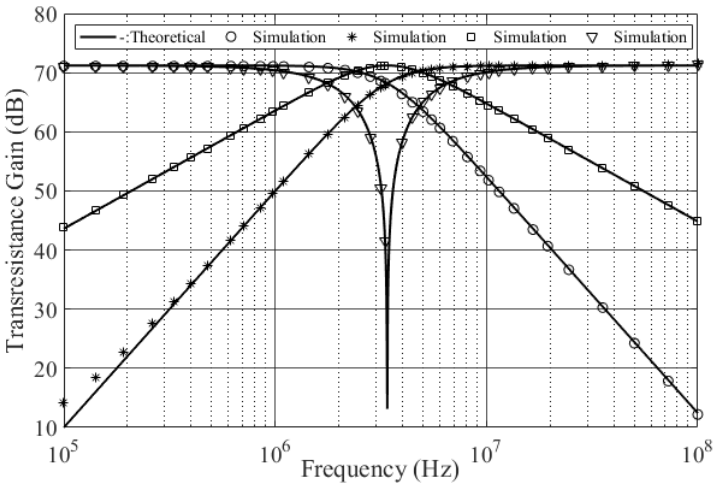
To validate the theoretical propositions of the proposed universal mixed-mode biquad of Fig. 2.22, the circuit was simulated using Cadence Virtuoso Analog Design Environment (ADE) tool at 0.18 μm CMOS technology. The OTA schematic shown in Fig. 2.15 [74] was used for the proposed biquad filter realization. The DC power supplies used were $\pm$ 0.9V, and the bias voltage V_{Bias} was taken as – 0.36 V. The (metal–insulator–metal)MIM capacitors used were of values C_1 = 9.12 pF and C_2 = 18.24 pF for a cut-off frequency of 3.390 MHz and BW of 30.196 MHz. Fig. 2.25 displays the simulated and theoretical frequency responses of VM, CM, TRM, and TCM respectively.


-:Theoretical
Simulation
Simulation
Simulation
Simulation
Voltage Gain (dB)
Frequency (Hz)

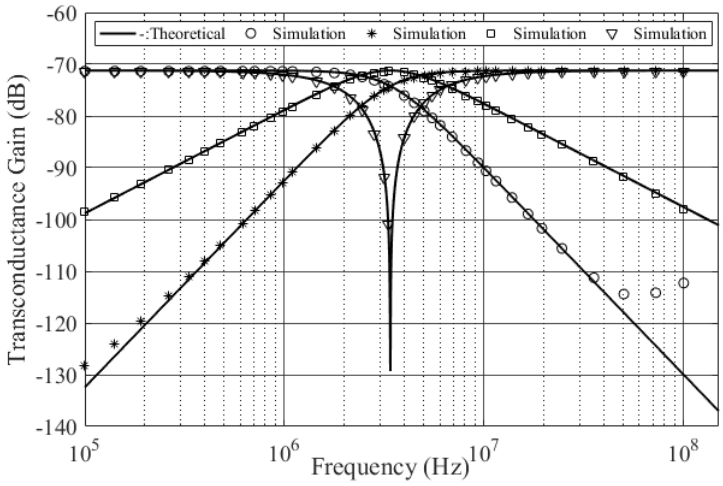
(a)


-:Theoretical
Simulation
Simulation
Simulation
Simulation
Current Gain (dB)
Frequency (Hz)

(b)


-:Theoretical
Simulation
Simulation
Simulation
Simulation
Transresistance Gain (dB)
Frequency (Hz)

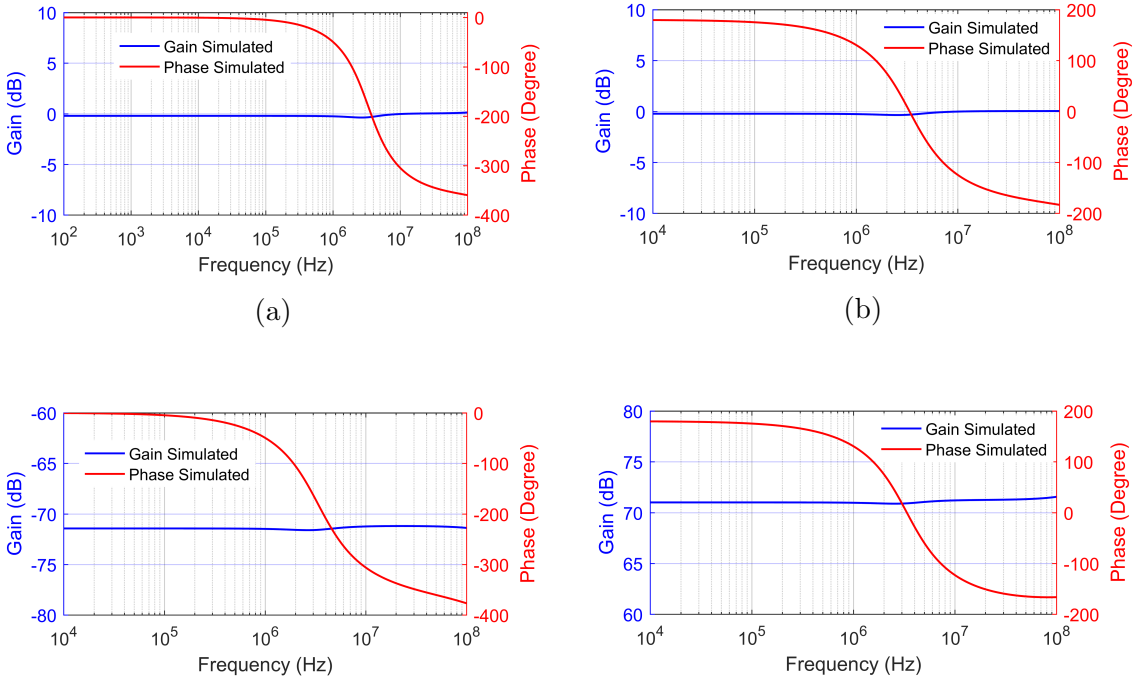
(c)



(d)

Figure 2.25: Frequency responses of (a) VM biquad filter (b) CM biquad filter (c) TRM biquad filter (d) TCM biquad filter

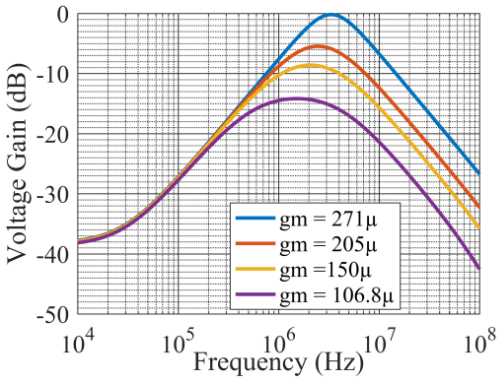
Fig. 2.26 shows the simulated VM, CM, TCM and TRM magnitude and phase responses of AP filter of Fig. 2.22 respectively. The gain variations of different filter responses in various modes are illustrated in Fig. 2.27.



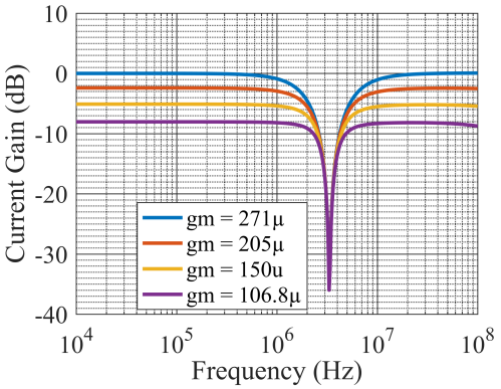
(a) (b)

(c) (d)

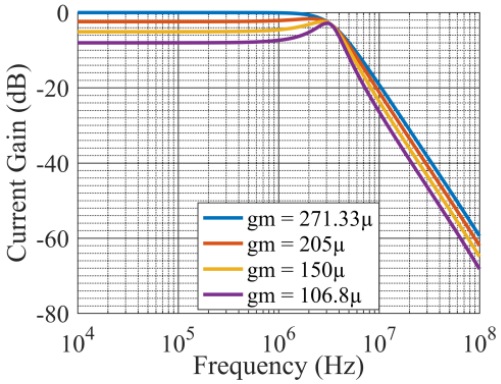
Figure 2.26: Gain and phase responses of APF (a) VM (b) CM (c) TRM (d) TCM


Voltage Gain (dB)
0
-10
-20
-30
-40
-50
10^4
10^5
10^6
10^7
10^8
Frequency (Hz)
gm = 271µ
gm = 205µ
gm =150µ
gm = 106.8µ

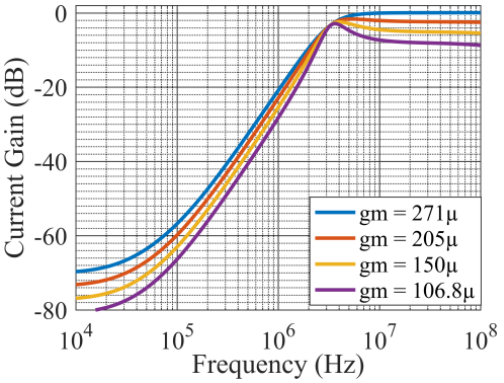
(a)


Current Gain (dB)
10
0
-10
-20
-30
-40
10^4
10^5
10^6
10^7
10^8
Frequency (Hz)
gm = 271µ
gm = 205µ
gm = 150u
gm = 106.8µ

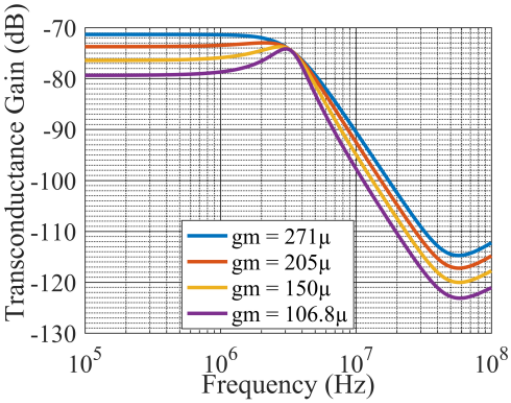
(b)


Current Gain (dB)
0
-20
-40
-60
-80
10^4
10^5
10^6
10^7
10^8
Frequency (Hz)
gm = 271.33µ
gm = 205µ
gm = 150µ
gm = 106.8µ

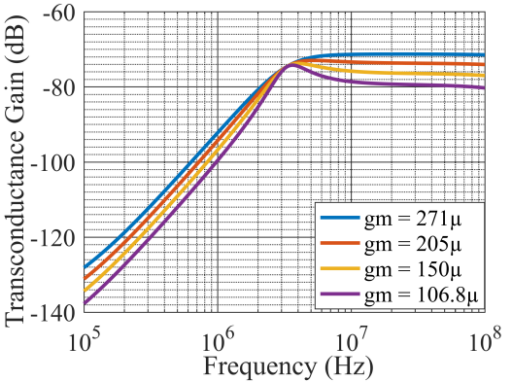
(c)


Current Gain (dB)
0
-20
-40
-60
-80
10^4
10^5
10^6
10^7
10^8
Frequency (Hz)
gm = 271µ
gm = 205µ
gm = 150µ
gm = 106.8µ

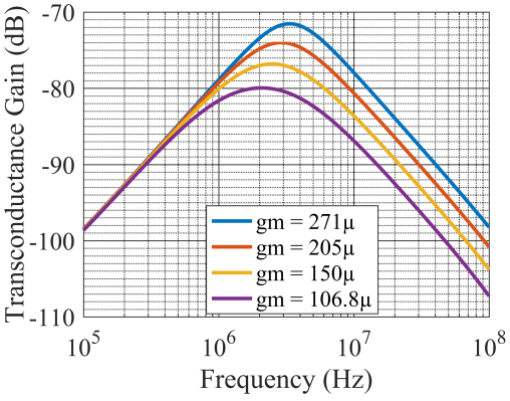
(d)


Transconductance Gain (dB)
-70
-80
-90
-100
-110
-120
-130
10^5
10^6
10^7
10^8
Frequency (Hz)
gm = 271µ
gm = 205µ
gm = 150µ
gm = 106.8µ

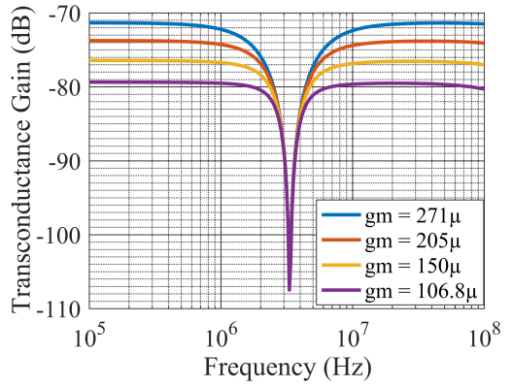
(e)


Transconductance Gain (dB)
-60
-80
-100
-120
-140
10^5
10^6
10^7
10^8
Frequency (Hz)
gm = 271µ
gm = 205µ
gm = 150µ
gm = 106.8µ

(f)


Transconductance Gain (dB)
-70
-80
-90
-100
-110
10^5
10^6
10^7
10^8
Frequency (Hz)
gm = 271µ
gm = 205µ
gm = 150µ
gm = 106.8µ

(g)


Transconductance Gain (dB)
-70
-80
-90
-100
-110
10^5
10^6
10^7
10^8
Frequency (Hz)
gm = 271µ
gm = 205µ
gm = 150µ
gm = 106.8µ

(h)

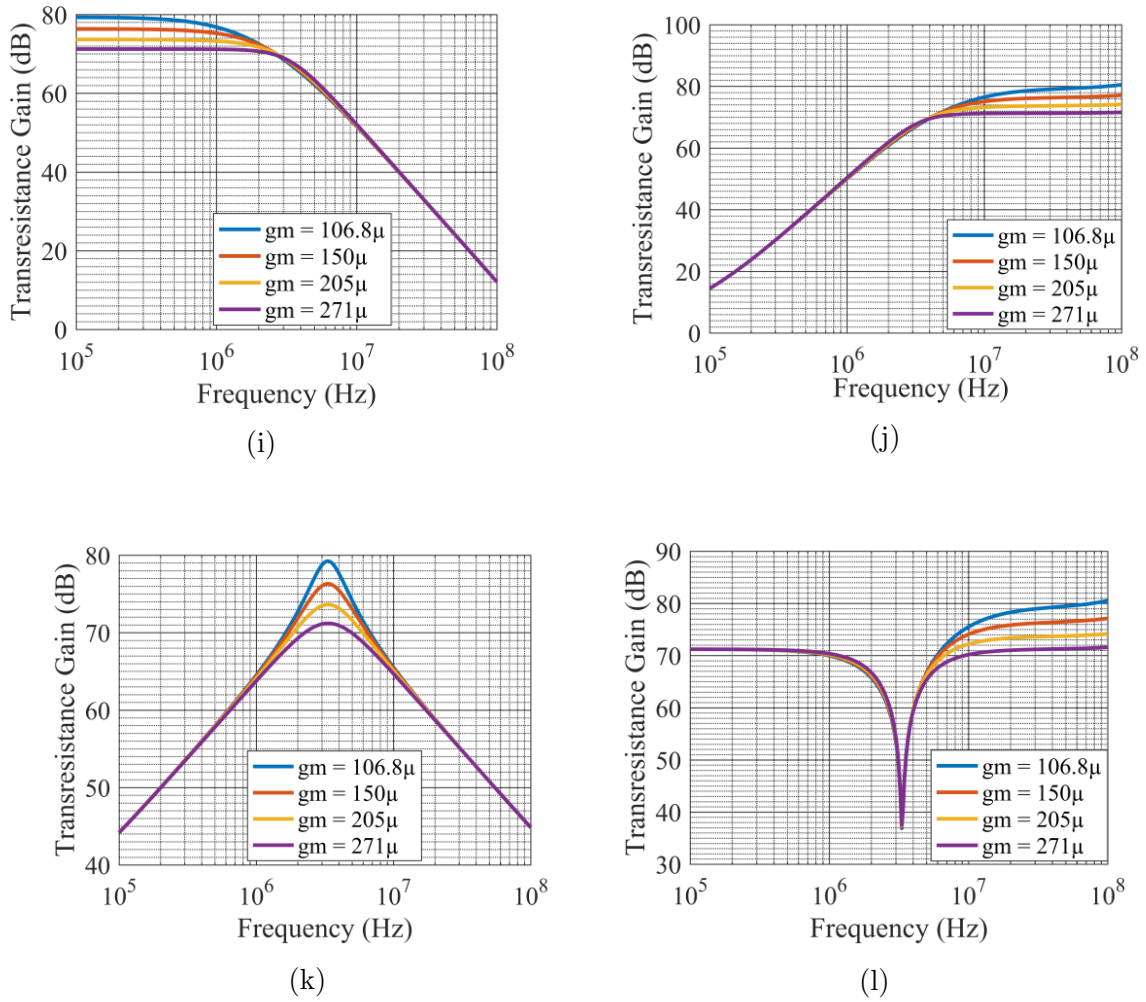
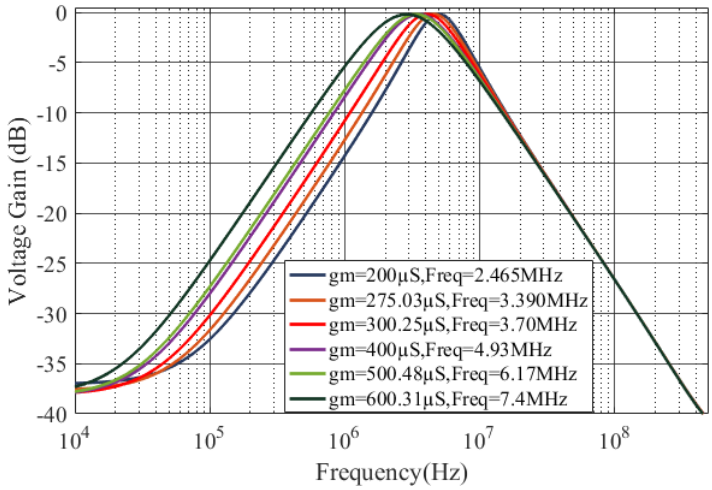
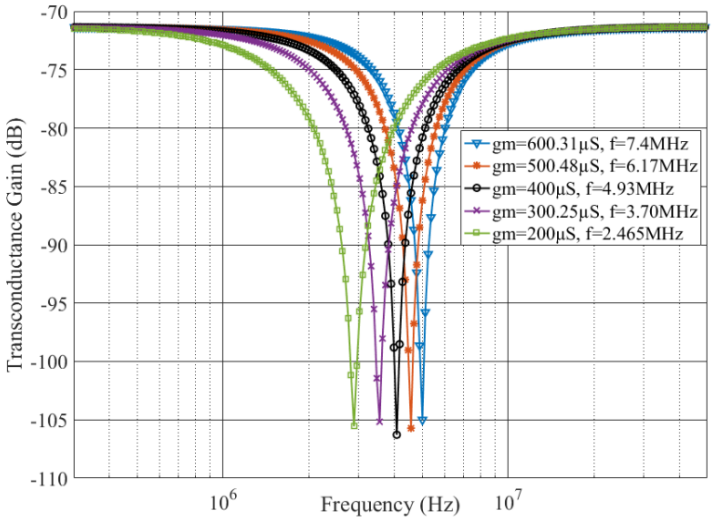


Figure 2.27: Variation of gain with transconductance of various filter responses of Fig. 2.22

To demonstrate the orthogonal tunability of cut-off frequency and BW in VM for the realization of BP filter and in TCM for the realization of BRF, the circuits were simulated to have a BW of 30.196 MHz while the cut-off frequency was varied (by varying g_m) from 2.46 MHz to 7.4 MHz. These simulated results are shown in Fig. 2.28.



(a)



(b)

Figure 2.28: Tunability of cut-off frequency for (a) BPF and (b) BRF of Fig. 2.22

2.4.3.2 Noise Performance Analysis

We have carried out the noise analysis with Cadence Virtuoso simulation tool with respect to variation in V_{bias} of various OTAs in the range of – 0.36V to – 0.9V corresponding to a variation in the transconductance from 2 μA/V to 275 μA/V for the designed frequency of 3.34 MHz. The maximum output noise values for VM, CM, TCM and TRM are 0.12 μV/sqrt(Hz), 28 pA/sqrt(Hz), 0.12 μV/sqrt(Hz) and 28 pA/sqrt(Hz) respectively. Thus, the output noise of the proposed biquad filters in all four modes is found to be low. We have also measured the output noise in

the range of 1 KHz to 1 GHz for all the four modes of operation and the maximum output noise in the chosen frequency range are found to be 1.5 μV/sqrt(Hz), 0.72 nA/sqrt(Hz), 3.2 μV/sqrt(Hz), 0.72 nA/sqrt(Hz) respectively. The variation in output noise with respect to bias voltage (transconductance) and frequency for all the four modes of operation are depicted in Fig. 2.29 and Fig. 2.30 respectively.

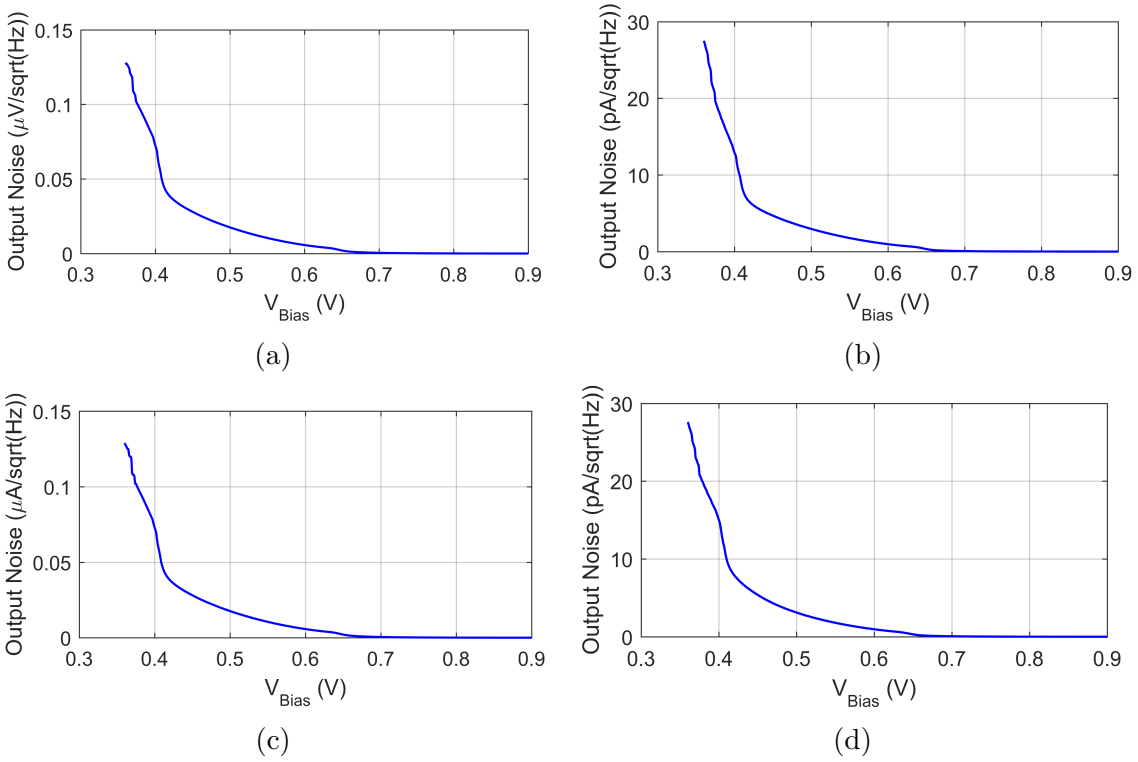
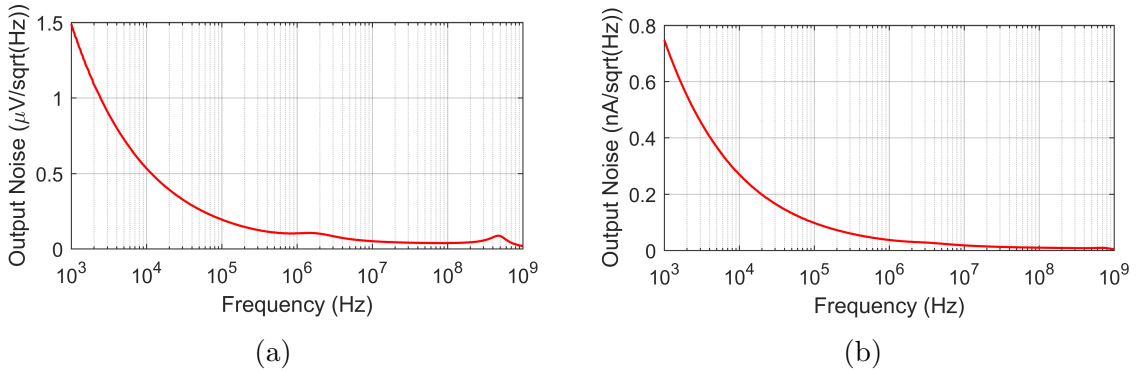
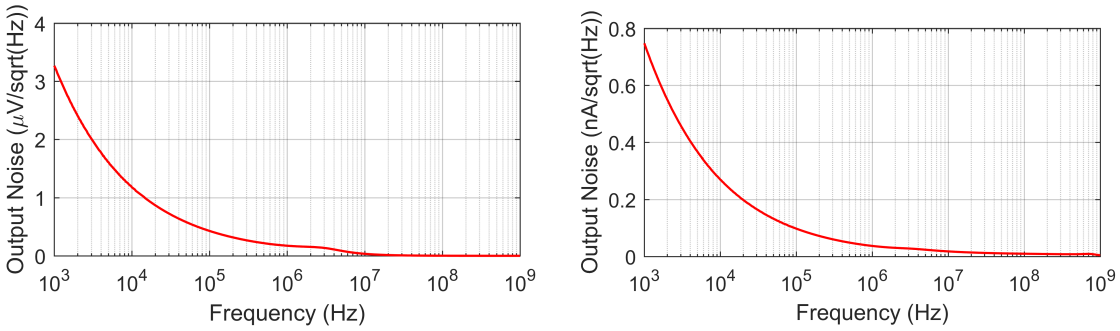


Figure 2.29: Output noise simulation results with V_{Bias} (a) VM biquad (b) CM biquad (c) TRM Biquad (d) TCM biquad of Fig. 2.22



The maximum power consumption of the proposed biquad filters in various modes



(c) (d)

Figure 2.30: Output noise simulation results with frequency (a) VM biquad (b) CM biquad (c) TRM Biquad (d) TCM biquad of Fig. 2.22

using Cadence Virtuoso tools was used and it was found to be 177.3 μW in VM and TRM while in CM and TCM it was 191.7 μW.

2.4.3.3 Layout Design

The layout of proposed mixed mode biquad filter is depicted in Fig. 2.31. All the physical verification checks (Design Rule Check, Layout vs. Schematic check, RC extraction) and post layout simulation results authenticate the layout implementation of the proposed biquad filter configuration. The total active die area required is (228.88 x 157.395) mm^2.

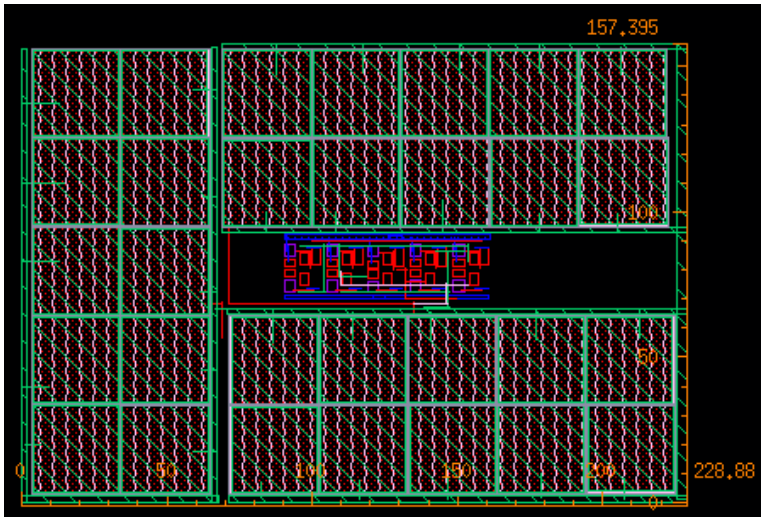


Figure 2.31: Complete physical layout design of the proposed biquad filter in VM of Fig. 2.22

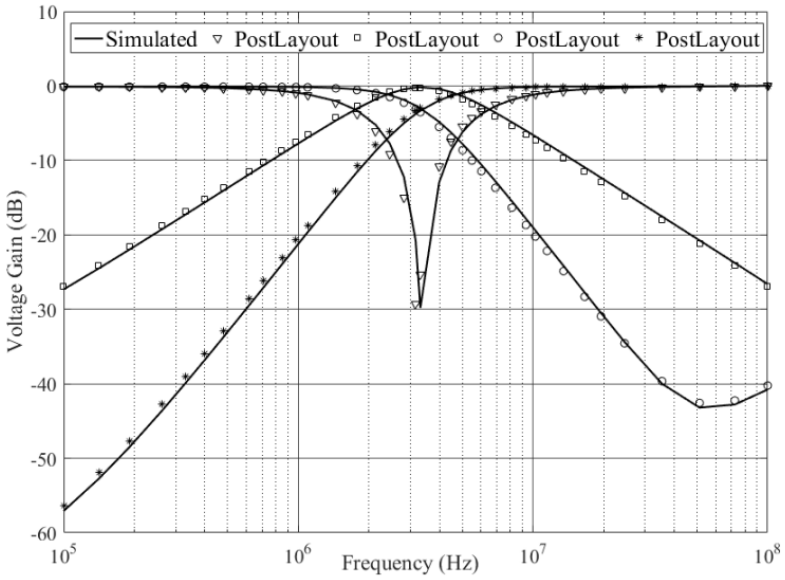


Figure 2.32: Pre-layout and post-layout responses of the proposed biquad in VM Fig. 2.22

Fig. 2.32 shows the pre-layout and post-layout simulation results of LP, HP, BP, and BR filter responses in VM Fig. 2.22.

2.5 Concluding Remarks

In this chapter, we have presented single output OTA–based three MISO type universal biquad structures. The first OTA-C universal biquad filter operates in VM, employs five OTAs and two grounded capacitors and can provide all five generic filter functions by appropriate choice(s) of input voltages. This proposed filter circuit offers electronic orthogonal tunability of pole frequency and BW. Sensitivity of pole frequency with respect to transcondutors and capacitors has also been evaluated and found to be less than half. A macro model of LM13700 type OTA has been used to validate the simulations of the proposed circuit in PSPICE. To obtain the LP filter response, voltage inversion is needed which requires an additional OTA. To alleviate the limitations, we have also proposed two VM universal biquad filter

circuits employing only four single output OTAs with two grounded capacitors. The presented circuits have orthogonal electronic tunability of pole frequency and pole quality factor. An exemplary CMOS OTA, implemented in 180nm TSMC technology parameters, has been used to validate the functionality of proposed biquad filter circuits. Simulation results such as frequency reponses, Monte-Carlo simulations and noise analysis using PSPICE simulation tool have been performed to check the workability of the proposed circuits. We have also made the complete layout design for one of the presented circuits using Cadence Virtuoso simulations tool. Various checks such as design rule check, layout versus schematic check in analog design enviroment have been done and the prelayout and post layout simulation results have been pesented.

A mixed mode universal biquad filter topology employing five OTAs and two grounded capacitors has also been presented in this chapter. The mixed mode filter configuration realizes all five filter functions in all four modes i.e., voltage mode, current mode, transresistance mode, and transconductance mode. The proposed mixed mode universal filter circuit has orthogonal electronic tunability of pole frequency and BW. The pole frequency and pole quality factor of the presented filter structure can be independently tuned through the transconductane of OTAs. The pole frequency of the proposed filter has a ratio term. By making this ratio very small compare to 1, the pole frequency can be set to a very low value, making the filter suitable for biomedical applications. Non-ideal analyses have also been carried out to determine the parasitic effect on filter parameters. The active and passive sensitivities evaluated for this mixed mode biquad filter configuration are found to be not more than 1. Monte-Carlo analysis and noise analysis have also been carried out to check the robustness of the proposed filters.

The workability of this proposed mixed mode filter configuration has been validated using Cadance Virtuoso simulations tool employing CMOS OTA achitecture and MATLAB evaluations. This chapter, thus, has enriched the existing reportire of OTA–based MISO type filters.

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Chapter 3

Third Order Quadrature Sinusoidal Oscillators Using OTAs

3.1 Introduction

In chapter 2, we have presented several new circuits of MISO type universal biquads which support voltage mode and mixed mode operations. Harmonic oscillators on the other hand, play an important role in instrumentation, communications, and control systems. The present chapter deals with the realization of OTA–C harmonic oscillators.

Harmonic oscillators belong to a class of autonomous, closed loop, analog circuits in which the output signal is a sinusoidal signal whose frequency and amplitude can be set by the designer. Since these circuits are autonomous, no input signal at signal frequency is applied to the circuits. For low and medium frequency applications, these oscillators are usually realized with an amplifier, which is built with one or more ABBs, resistors and capacitors. These harmonic oscillators may be classified in several ways viz

(i) Voltage mode and current mode: Based on the type of output signal,

the oscillators may be called as voltage mode, or current mode.

(ii) Single phase, multiphase/quadrature: Depending upon the phase difference between different output voltages/currents, the oscillator may be called a single phase or multiphase. If a quadrature relationship exists between different voltages/currents in an oscillator circuit, the oscillator is known as quadrature oscillator.

(iii) Second order, third order or higher order oscillators: If the characteristic equation of the oscillator circuit is of order '2', then the oscillator is called as second order oscillator. Usually, the canonic realization of such RC oscillators employ two capacitors. However, it has been reported in literarture, that higher order oscillators (where the number of capacitors employed is '3' or more) have better accuracy, low harmonic distortion and high quality factor.

(iv) Fixed frequency oscillators (FFO), single resistance controlled oscillators (SRCO) and single capacitor controlled oscillators (SCCO): In an RC oscillator, if the frequency of oscillation (FO) cannot be changed without changing the condition of oscillation (CO), then such oscillator is known as FFO. On the other hand, if the FO can be changed without changing the CO, by varying either a resistor or a capacitor, then the oscillator is called as SRCO/SCCO. If in an oscillator, the FO and CO can be controlled by different set(s) of passive elements, then such type of oscillators are preferred from the point of view of amplitude stabilization and control.

(v) Voltage/current controlled oscillators (VCOs/CCOs): If the FO in harmonic oscillators can be tuned by varying some external voltage/current, then, such oscillators are also known as voltage/current controlled oscillators. These oscillator circuits (VCOs/CCOs) are very useful for frequency modulation or phase modula-

tion by applying a modulating signal to the control input.

From a detailed perusal of the research work carried out on harmonic oscillators available in an open literature, it has been observed that compared to second order oscillators [1–16] with different properties, relatively less work has been done on the realization of third order oscillators [17].
Since this chapter deals with the realization of third order sinusoidal oscillators using OTAs, in the following, we present a detailed account of the work presented on the realization of third order sinusoidal oscillators using differnt active building blocks, so that the work presented in this chapter can be put in proper perspective.

Two configurations of TOQSO were proposed in [18] by **Prommee** and **Dehjan** in which one configuration employed three OTAs and three capacitors, while the other configuration used four OTAs, three capacitors and an electronic resistor. The reported circuits have orthogonal electronic control of CO and FO. One of these reported circuits is shown in Fig. 3.1.

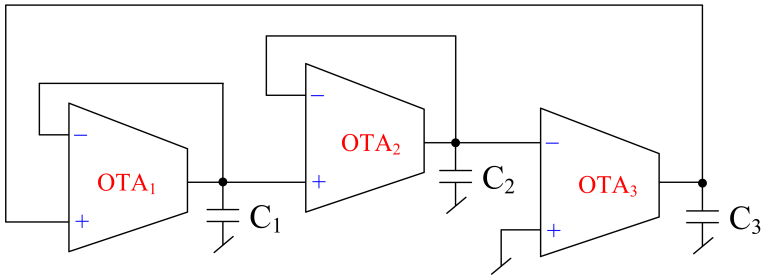


Figure 3.1: TOQSO using OTAs reported by Prommee and Dehjan [18].

Three TOQSOs employing second-generation current conveyors (CCII) were reported in [19] by **Horng, Hou, Chang, Chung, Tang** and **Wen**. Two of the proposed configurations therein, were realized using three CCIIs, five resistors and three capacitors, whereas, the third circuit requires three CCIIs, five capacitors, and three resistors. All the reported topologies have orthogonal control of CO and FO.

In [20], a current-controlled third-order translinear-C quadrature sinusoidal oscilla-

tor using four current controlled second-generation current conveyors (CCCII) and three capacitors was presented by **Maheshwari** and **Khan** with non-interacting control of FO and CO.

In [21], **Lawanwisut** and **Siripruchyanun** presented a TOQSO employing two current-controlled current conveyor transconductance amplifiers (CCCCTAs) and three capacitors. The oscillator circuit had non-interacting control of CO and FO.

A differential voltage current conveyors (DVCCs) based TOQSO was presented by **Maheshwari** in [22] employing three DVCCs and three capacitors. This circuit provides independent control of CO and FO.

In [23], a current-mode TOQSO using three CDTAs and three capacitors, providing orthogonal adjustment of CO and FO was reported by **Horng**. The reported circuit has been shown in Fig. 3.2.

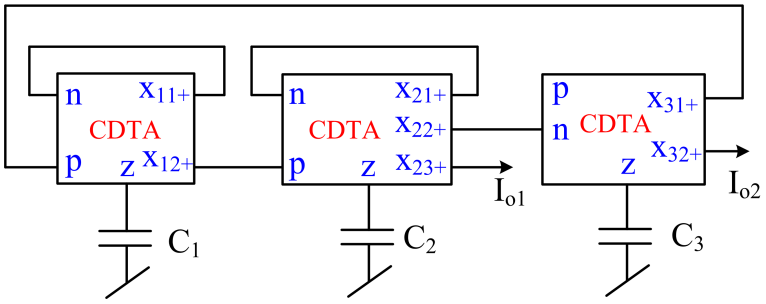


Figure 3.2: Third-order quadrature sinusoidal oscillator using CDTAs reported by Horng [23].

Another electronically tunable TOQSO circuit using CDTAs was presented by **Horng, Lee** and **Wu** in [24], which required three CDTAs and three capacitors providing non-interacting control of CO and FO. Two voltage mode and two current mode outputs with quadrature relationships have been obtained from the reported circuit.

In [25], **Maheshwari** has presented a current mode/voltage mode TOQSO as shown

in Fig. 3.3 employing three CCCIIs and three capacitors. The circuit provides non-interacting control of CO and FO.

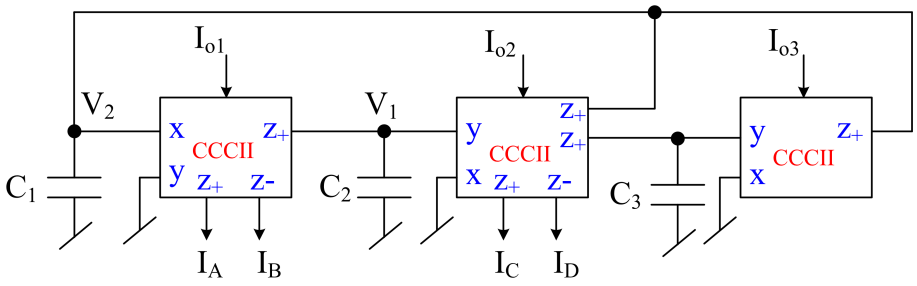


Figure 3.3: Third-order sinusoidal oscillators using CCCIIs presented by Maheshwari [25].

Two multiple-output second generation current conveyors (MO-CCII) along with three capacitors and three resistors based TOQSO was presented in [26] by **Horng**. The CO and FO of this proposed configuration were independently adjustable through resistors. The circuit has quadrature outputs in current mode.

In [27], one current controlled current differencing transconductance amplifier (CC-CDTA), one OTA and three capacitors based TOQSO has been reported by **Kumngern** and **Junnapiya**. The presented oscillator offers independent adjustment of CO and FO.

Maheshwari and **Verma** presented an electronically tunable TOQSO circuit employing four CCCIIs, three capacitors, and one resistor in [28]. The CO and FO of this oscillator can be controlled through different resistors.

A single modified current controlled current follower transconductance amplifier based TOQSO has been presented by **Kumngern** and **Torteanchai** in [29], which has independent control of CO and FO.

Kumngern and **Chanwutitum** reported a single modified current-controlled current conveyor transconductance amplifier (MCCCCTA), and three capacitors based

TOQSO in [30] that can generate two quadrature voltage outputs and four quadrature current outputs. The reported circuit has been depicted in Fig. 3.4.

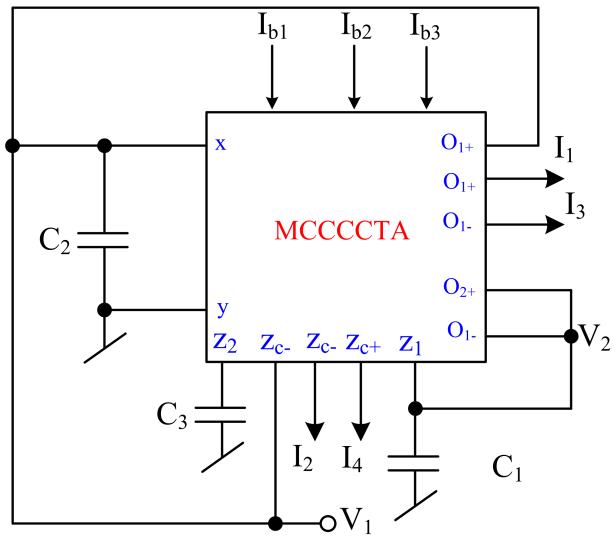


Figure 3.4: Third-order quadrature sinusoidal oscillator using MCCCCTAs presented by Kumngern and Chanwutitum [30].

A current and voltage mode TOQSO using current and voltage conveyors has been proposed in [31] by **Koton, Herencsar, Vrba** and **Metin**. The circuit uses three resistors and three capacitors. The circuit has the feature of non-interactive control of CO and FO.

Three DVCCs, three resistors and three capacitors were employed to realize a TOQSO in [32] by **Chaturvedi** and **Maheshwari**. However, the circuit CO and FO can not be adjusted independently.

In [33], a current-mode quadrature sinusoidal oscillator using one differential difference current conveyor (DDCC), a voltage differencing transconductance amplifier (VDTA), three capacitors and one resistor was presented by **Phanruttanachai** and **Jaikla**. This circuit has independent control of CO and FO.

Generation of third-order quadrature oscillator circuits using NAM expansion method

has been reported in [34] by **Soliman**. An exemplary third order sinusoidal oscillator thus derived and realized with CFOAs [34], shown in Fig. 3.5. The reported circuit does not have indepentdent control of CO and FO.

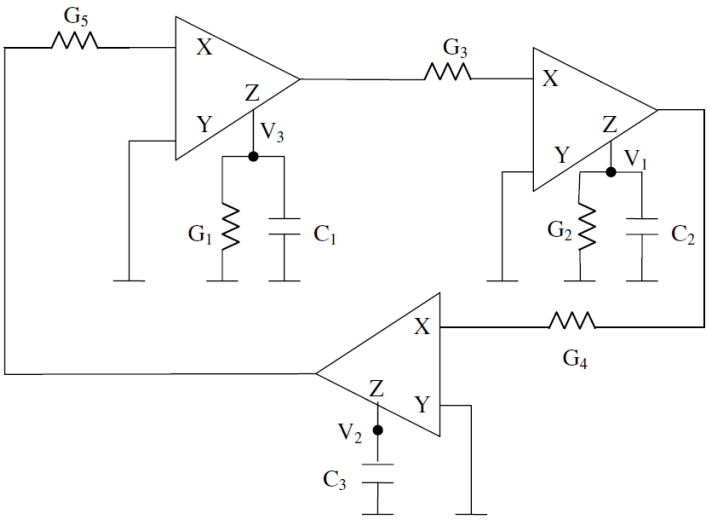


Figure 3.5: Third-order sinusoidal oscillators using CFOAs reported by Soliman [34].

Two VDTA and three capacitors based TOQSO has been presented in [35] by **Channumsin** and **Jantakun** which has both voltage and current outputs and also easy to use in amplitude modulation (AM)/ amplitude shift keying (ASK) communication systems.

In [36], **Kumngern** and **Kansiri** presented a TOQSO employing three operational transresistance amplifiers (OTRAs), six resistors and three capacitors. The oscillator has independent control of CO and FO.

Two VDTA and three capacitor based TOQSO has been presented in [37] by **Phatsornsiri, Lamun, Kumngern** and **Torteanchai** which offers independent control of CO and FO.

In [38], two structures of TOQSOs were reported by **Pandey** and **Pandey** using two differential voltage current conveyor transconductance amplifiers (DVCCTAs),

three capacitors and one resistor with independent control of CO and FO. One of the reported circuits has been depicted in Fig. 3.6.

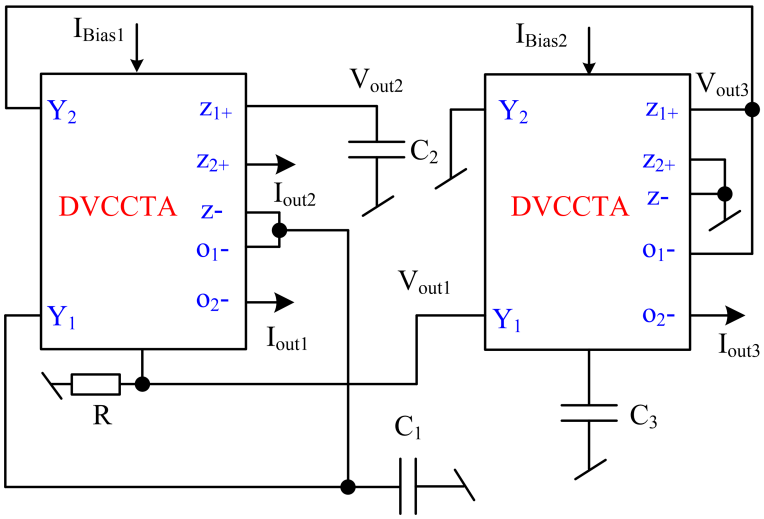


Figure 3.6: Third-order quadrature sinusoidal oscillator using DVCCTAs presented by Pandey and Pandey [38].

In [39], two current-mode third-order quadrature sinusoidal oscillators were proposed by **Jin, Wang** and **Sun**. One of these circuits employs two CDTA and three capacitors whereas the other circuit uses three CDTA and three capacitors. Both the oscillator circuits have independent control of CO and FO.

Three voltage differencing buffered amplifiers (VDBAs), three capacitors and two resistors were used by **Malhotra, Ahalawat, Kumar, Pandey** and **Pandey** to realize a TOQSO in [40] where CO and FO can be adjusted independently.

Khaw-Ngam, Kumngern and **Khateb** [41] presented a mixed-mode TOQSO circuit employing a modified current-controlled current follower transconductance amplifier (MCCCFTA) and three capacitors which provides orthogonal tunability of CO and FO.

A systematic realization of TOQSO employing two multiple-output DVCCTAs, three capacitors, and two resistors was presented in [42] by **Chen, Hwang** and

Ku. A VM non-inverting low pass filter and a VM inverting lossless integrator in feedback were used to realise TOQSO circuit. The circuit provides VM and CM quadrature outputs with independent control of CO and FO.

In [43], a TOQSO circuit employing two VDBAs, three capacitors, and one resistor was reported by **Pushkar**. The CO and FO of the reported circuit can be controlled independently and also the circuit provides quadrature voltage outputs.

Chen, Hwang and **Ku** presented a resistorless third-order quadrature oscillator using two multiple-output current controlled current conveyor transconductance amplifiers (MO-CCCCTAs) and three capacitors in [44]. The reported oscillator has independent control of CO and FO.

Single current differencing cascaded transconductance amplifier (CDCTA) and three capacitors have been used to realize a TOQSO by **Kumngern** and **Torteanchai** in [45]. The CO and FO can be controlled electronically and orthogonally through bias currents.

In [46], a fully differential second generation current conveyor (FDCCII), three resistors and three grounded capacitors were used to realize a TOQSO by **Wareechol, Knobnob** and **Kumngern**, which has independent control of both CO and FO.

In [47], a resistorless electronically tunable TOQSO employing two VDTAs, and three capacitors was reported by **Chen, Hwang** and **Ku** which offers independent control of FO and CO whereas in [48], **Chen, Wang, Chen** and **Huang** reported multi-output VDTAs based TOQSO using three capacitors. The reported circuit also has independent control of CO and FO.

In [49], **Pushkar** and **Bhaskar** presented a TOQSO which employs two voltage

differencing inverting buffered amplifiers (VDIBAs), three capacitors and a resistor. The reported TOQSO enjoys independent electronic control of CO and FO with quadrature output voltages.

Three OTAs and three capacitors based another TOQSOs has been reported in [50] by **Komal, Pushkar** and **Kumar** which is shown in Fig. 3.7. This oscillator circuit has independent control of CO and FO.

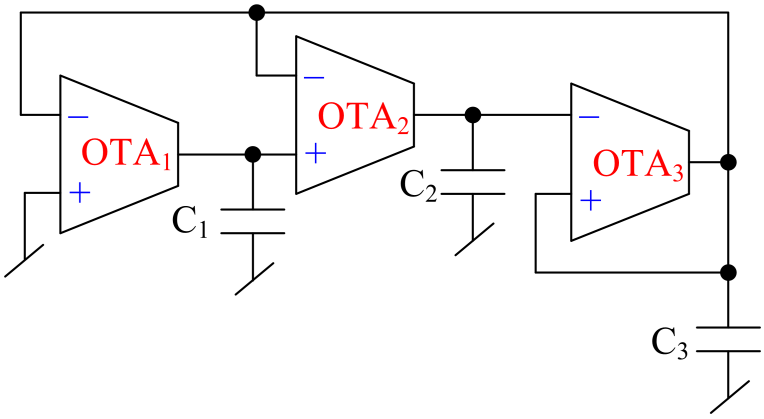


Figure 3.7: Third-order sinusoidal oscillators using OTAs reported by Komal, Pushkar and Kumar [50].

From the above discussions, it, thus, emerges that though many interesting circuits of TOQSO have been proposed by several researchers, the catalogue of TOQSO is far from complete. Also, most of the TOQSO presented previously are more suitable from the point of view of integrable designs and can not be realized with discrete components (except the circuits presented in [18, 19, 25, 34, 38, 39, 41, 42, 44, 47, 48, 51, 52]. Only two circuits of OTA–C based TOQSOs have been reported in open literature [18, 50], while one structure of CFOA based TOQSO has been presented so far [34]. In the following, therefore, we present OTA–based TOQSOs which use canonical number of OTAs and capacitors having independent electronic control of both CO and FO. Also, the TOQSOs possess voltage and current quadrature outputs. The CFOA-based TOQSOs circuits have been presented in next chapter.

3.2 VM/CM Third Order Quadrature Sinusoidal Oscillator Configurations Employing Three OTAs and Three Capacitors[1]

3.2.1 Proposed Circuits

In this section, four resistorless TOQSOs have been presented which employ canonic number of active and passive elements. These circuits can be operated in both VM as well as CM. Fig. 3.8 depicts the new proposed configurations of TOQSOs.

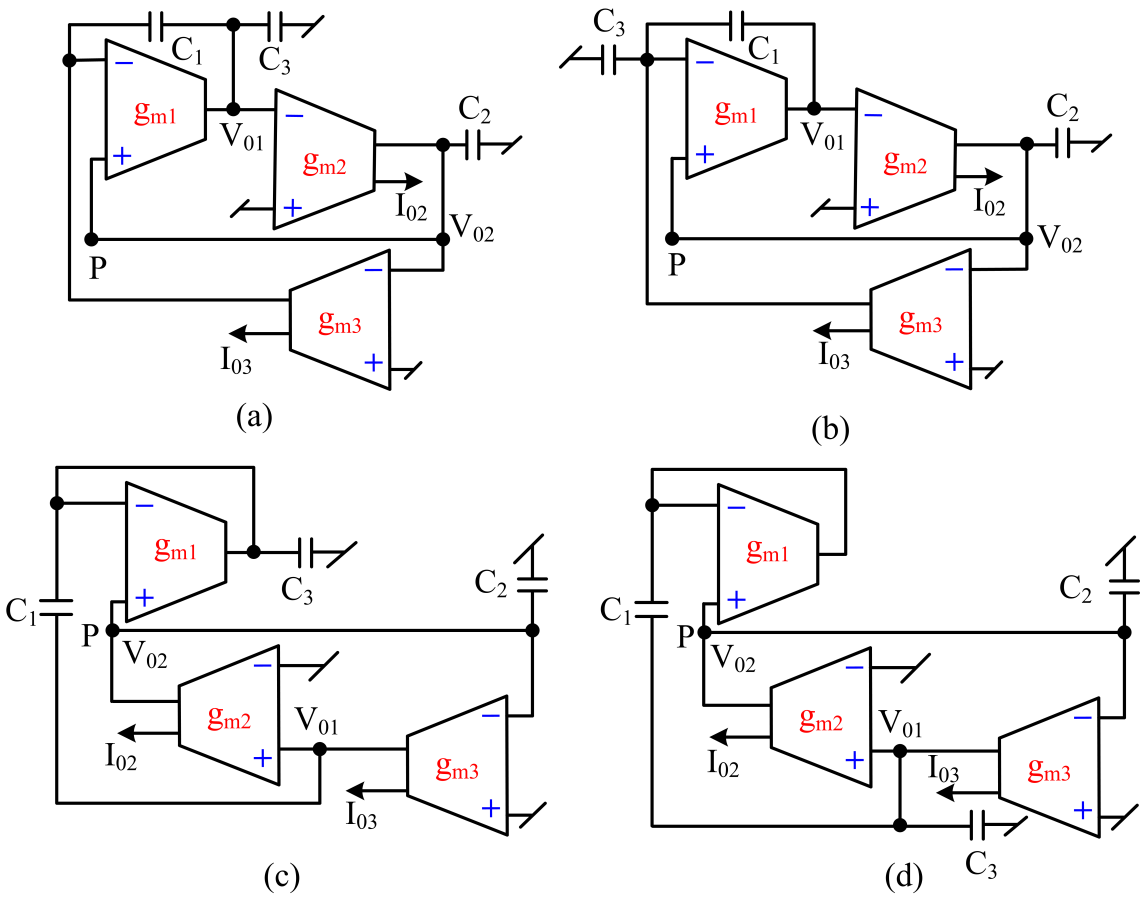


Figure 3.8: Proposed third-order quadrature sinusoidal oscillators.

Assuming ideal OTAs, a straight forward circuit analysis yields the characteristic equations (CEs) of all the four TOQSO circuits of Fig. 3.8 which are given below.

[1]The material presented in this section has been published in: D. R. Bhaskar, Ajishek Raj, and Pragati Kumar, "New Resistorless Third-Order Quadrature Sinusoidal Oscillators" Journal of Circuits, Systems and Computers, Vol. 30, No. 11, (2021), 2150194 (17 pages)

Fig. 3.8(a)

$$s^3C_1C_2C_3 + s^2C_1C_2g_{m1} + sC_1g_{m2}(g_{m1} - g_{m3}) + g_{m1}g_{m2}g_{m3} = 0 \quad (3.1)$$

Fig. 3.8(b)

$$s^3C_1C_2C_3 + s^2C_1C_2g_{m1} + s(C_1g_{m2}(g_{m1} - g_{m3}) + C_3g_{m1}g_{m2}) + g_{m1}g_{m2}g_{m3} = 0 \quad (3.2)$$

Fig. 3.8(c)

$$s^3C_1C_2C_3 + s^2C_1C_2g_{m1} + s(C_1g_{m2}(g_{m3} - g_{m1}) + C_3g_{m2}g_{m3}) + g_{m1}g_{m2}g_{m3} = 0 \quad (3.3)$$

Fig. 3.8(d)

$$s^3C_1C_2C_3 + s^2C_2(C_1g_{m1} + C_3g_{m1}) + sC_1g_{m2}(g_{m3} - g_{m1}) + g_{m1}g_{m2}g_{m3} = 0 \quad (3.4)$$

Applying Routh-Hurwitz's criterion on the derived CEs given in equations (3.1) - (3.4), the condition of oscillation (CO) and frequency of oscillation (FO) of the proposed TOQSOs have been found and are presented in Table 3.1.

Table 3.1: CO and FO of circuit of Fig. 3.8

Figure	Condition of Oscillation	Frequency of Oscillation
Fig. 3.8(a)	$g_{m1} = g_{m3}(1 + \frac{C_3}{C_1})$	$\omega_{01} = \sqrt{\frac{g_{m2}g_{m3}}{C_1C_2}}$
Fig. 3.8(b)	$g_{m1} = g_{m3}$	$\omega_{02} = \sqrt{\frac{g_{m2}g_{m3}}{C_1C_2}}$
Fig. 3.8(c)	$g_{m1} = g_{m3}$	$\omega_{03} = \sqrt{\frac{g_{m2}g_{m3}}{C_1C_2}}$
Fig. 3.8(d)	$g_{m3} = g_{m1}(1 + \frac{C_3}{C_1})$	$\omega_{04} = \sqrt{\frac{g_{m2}g_{m3}}{C_2(C_1+C_3)}}$

From Table 3.1, it is observed that in all the four cases, CO and FO, have non-interacting electronic control; i.e., CO can be adjusted using transconductance g_{m1}, while FO can be controlled through g_{m2} without affecting CO. It is interesting to note that two of the proposed configurations shown in Fig. 3.8(b) and Fig. 3.8(c), have capacitor tuning of the FO also, without disturbing CO. This feature can be

utilized in transducer oscillators together with capacitive transducers[53].
The steady state relationship between output voltages (V_{01} and V_{02}) and output currents (I_{02} and I_{03}) for the circuits of Fig. 3.8 are tabulated in Table 3.2 and Table 3.3 respectively.

Table 3.2: Quadrature relationship between voltages V_{01} and V_{02}.

Fig. 3.8(a)	$\frac{V_{02}(j\omega)}{V_{01}(j\omega)} = -\frac{g_{m2}}{\omega C_2}e^{-j90^\circ}$	Fig. 3.8(b)	$\frac{V_{02}(j\omega)}{V_{01}(j\omega)} = -\frac{g_{m2}}{\omega C_2}e^{-j90^\circ}$
Fig. 3.8(c)	$\frac{V_{02}(j\omega)}{V_{01}(j\omega)} = \frac{g_{m2}}{\omega C_2}e^{-j90^\circ}$	Fig. 3.8(d)	$\frac{V_{02}(j\omega)}{V_{01}(j\omega)} = \frac{g_{m2}}{\omega C_2}e^{-j90^\circ}$

Table 3.3: Quadrature relationship between voltages I_{01} and I_{02}.

Fig. 3.8(a)	$\frac{I_{03}(j\omega)}{I_{02}(j\omega)} = -\frac{g_{m3}}{\omega C_2}e^{-j90^\circ}$	Fig. 3.8(b)	$\frac{I_{03}(j\omega)}{I_{02}(j\omega)} = -\frac{g_{m3}}{\omega C_2}e^{-j90^\circ}$
Fig. 3.8(c)	$\frac{I_{03}(j\omega)}{I_{02}(j\omega)} = -\frac{g_{m3}}{\omega C_2}e^{-j90^\circ}$	Fig. 3.8(d)	$\frac{I_{03}(j\omega)}{I_{02}(j\omega)} = -\frac{g_{m3}}{\omega C_2}e^{-j90^\circ}$

From Table 3.2 and Table 3.3, it can be noted that the proposed oscillators of Fig. 3.8 provide quadrature outputs in both VM and CM simultaneously.

3.2.2 Non-Ideal Analysis

A frequency dependent transconductance model of the OTA [5] described below by equation (3.5) has been used (along with output parasitic of OTAs as shown in Fig. 3.9) to evaluate the CEs of the TOQSO circuits presented in Fig. 3.8 under non-ideal conditions.

$$g_{mi}(s) \approx g_{mi}(1 - \frac{s}{\omega_z}); i \to 1-3 \quad for \;\; \omega \ll \omega_z \tag{3.5}$$

Routine analysis of the circuits shown in Fig. 3.8 using the non-ideal OTA model

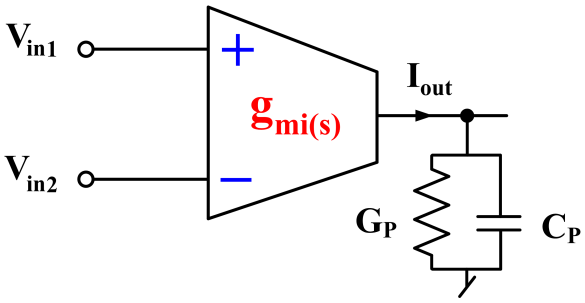


Figure 3.9: Non-ideal model of OTA.

yields the following non-ideal expressions for the frequency of oscillation (ω_{NP}; P $\rightarrow$ 1 - 4):

$$\omega_{N1} = \omega_{N2} = \omega_{N3} = \sqrt{\frac{G_1G_2G_3 + G_1g_{m1}g_{m2} + g_{m1}g_{m2}g_{m3}}{C_{P1}C_{P2}(G_3 + G_1 + g_{m1}) + C_{P1}C_{P3}G_2 - \frac{2C_{P1}g_{m2}(g_{m1}-g_{m3})}{\omega_z} + \frac{G_1g_{m1}g_{m2}}{\omega_z^2} + \frac{3g_{m1}g_{m2}g_{m3}}{\omega_z^3}}} \tag{3.6}$$

$$\omega_{N4} = \sqrt{\frac{(G_2G_3(g_{m1} + G_1) + g_{m2}g_{m3}G_1 + g_{m1}g_{m2}g_{m3})}{C_{P1}C_{P2}(g_{m1} + G_1 + G_3) + C_{P3}(C_{P2}(g_{m1} + G_1) + C_{P1}G_2) \frac{2g_{m2}C_{P1}(g_{m1}-g_{m3})-C_{P3}G_2g_{m1}}{\omega_z} + \frac{g_{m2}g_{m3}(G_1+3g_{m1})}{\omega_z^2}}} \tag{3.7}$$

where $C_{P1} = (C_P + C_1)$, $C_{P2} = (C_P + C_2)$, $C_{P3} = (C_P + C_3)$

As observed from equations (3.6) and (3.7), these equations do not lend themselves for a qualitative explanation of the effects of various non-idealities of the OTAs on FO. We have, thus, calculated the values of FO, for all the four circuits, as obtained from equations (3.6) and (3.7) by substituting the values of ω_z ($28.88 \times 10^9 rad/sec$), $G_P(1.307 \times 10^{-9}\mho)$ and $C_P(0.284 \times 10^{-18}F)$ (P $\rightarrow$ 1-3) for the CMOS OTAs used in the PSPICE simulations. The percentage errors between ideal and non-ideal FO for all the four circuits, for a designed frequency of 15.9 MHz have been calculated and found to be 0.22%, 0.22%, 0.22%, 0.062% respectively. This shows that the effect of different non-idealities of OTA, on the FO is very small.

The sensitivities of the FO with respect to transconductances and capacitors have

been calculated using the classical formula $S_x^{F(x)} = \frac{x}{F(x)}\frac{\partial F(x)}{\partial x}$ and found to be:

$$\begin{aligned} S_{g_{m2},g_{m3}}^{\omega_{01}} = S_{g_{m2},g_{m3}}^{\omega_{02}} = S_{g_{m2},g_{m3}}^{\omega_{03}} = S_{g_{m2},g_{m3}}^{\omega_{04}} = 0.5 \\ S_{C_3}^{\omega_{01}} = S_{C_3}^{\omega_{02}} = S_{C_3}^{\omega_{03}} = 0 \\ S_{C_1,C_2}^{\omega_{01}} = S_{C_1,C_2}^{\omega_{02}} = S_{C_1,C_2}^{\omega_{03}} = S_{C_1,C_2}^{\omega_{04}} = -0.5 \end{aligned} \tag{3.8}$$

Thus, from equation (3.8), it is clear that all sensitivities are low.

3.2.3 Phase Noise and Frequency Stability

For an oscillator, phase noise and frequency stability are essential figures of merit. The spectral purity of the oscillator spectrum is indicated by the phase noise of the oscillator, which is a measure of the noise power contained in the oscillator output at a frequency offset of Δf_0 in 1 Hz bandwidth. An ideal sinusoidal oscillator should have a single frequency in its spectrum. Thus, for a perfect oscillator, the phase noise must be zero. On the other hand, frequency stability factor [53] (S^F) indicates the rate of change of the phase of the open-loop transfer function of the oscillator circuit with respect to the normalized frequency (δ) $S^F = \frac{\partial \phi(\delta)}{\partial \delta}$ where $\delta = \frac{\omega}{\omega_0}$. As the frequency of oscillation of the oscillator depends on the value of phase of the open-loop transfer function, a higher value of this factor indicates that the resulting change in the oscillator frequency because of changes in the phase (as a result of changes in the operating conditions of the circuit) will be smaller. We have evaluated the phase noise spectral density of all the four oscillator circuits presented in Fig. 3.8 using the methodology presented in [54].

The noise spectral density [54] is defined as:

$$\left|\frac{Y}{X}[j(\omega_0 + \Delta\omega)]\right|^2 = \frac{1}{(\Delta\omega)^2[\frac{\partial H(\omega)}{\partial \omega}]^2} = \frac{1}{(\Delta\omega)^2[\frac{\partial A}{\partial \omega}^2 + \frac{\partial \phi}{\partial \omega}^2]} \tag{3.9}$$

where $H(j\omega) = |A(\omega)|\, e^{j\phi(\omega)}$ is the open-loop transfer function of the oscillator circuit, ω_0 is the FO and $\Delta\omega$ is the deviation in FO.

We have evaluated the open-loop transfer functions of all the four proposed oscillator circuits by breaking the loop at point 'P' as shown in Fig. 3.8 and, therefrom, determined the magnitude (A) and phase (ϕ) for these circuits, to evaluate the phase noise power spectral density (PSD) and frequency stability factor which are tabulated in Table 3.4.

Table 3.4: Phase noise power spectral density and frequency stability factor

Figures	PSD	$S^F = \frac{\partial\phi(\delta)}{\partial\delta}$ where $\delta = \frac{\omega}{\omega_0}$ $C_1 = C_2 = C_3 = C$, $g_{m1} = g_{m3} = g$ and $g_{m2} = ng$
Fig. 3.8(a)	$(\frac{\omega_0}{\Delta\omega})^2$	$\frac{1}{\sqrt{n}}$
Fig. 3.8(b)	$(\frac{\omega_0}{\Delta\omega})^2$	$\frac{2}{\sqrt{n}}$
Fig. 3.8(c)	$\frac{1}{4}(\frac{\omega_0}{\Delta\omega})^2$	$\frac{2}{\sqrt{n}}$
Fig. 3.8(d)	$\frac{1}{9}(\frac{\omega_0}{\Delta\omega})^2$	$\frac{4\sqrt{2}}{\sqrt{n}}$

From Table 3.4, it can be observed that the circuit of Fig. 3.8(d) has the lowest phase noise spectral density and highest frequency stability factor compared to the other structures presented in Fig. 3.8.

3.2.4 Simulation Results

The CMOS implementation of OTA shown in Fig. 3.10 was used to simulate the oscillator circuits presented in Fig. 3.8. The aspect ratios for Fig. 3.10 are given in Table 3.5. TSMC 0.18 μm technology parameters were used in PSPICE simulations. The supply voltages used were $\pm$ 0.9V.

Table 3.5: Aspect ratios of MOSFETs shown in Fig. 3.10

MOSFETs	Aspect Ratio (W/L)
M1, M2	3.6/0.36
M3, M4, M7, M8	1.44/0.36
M5, M6	2.88/0.36
M9	5.4/0.36

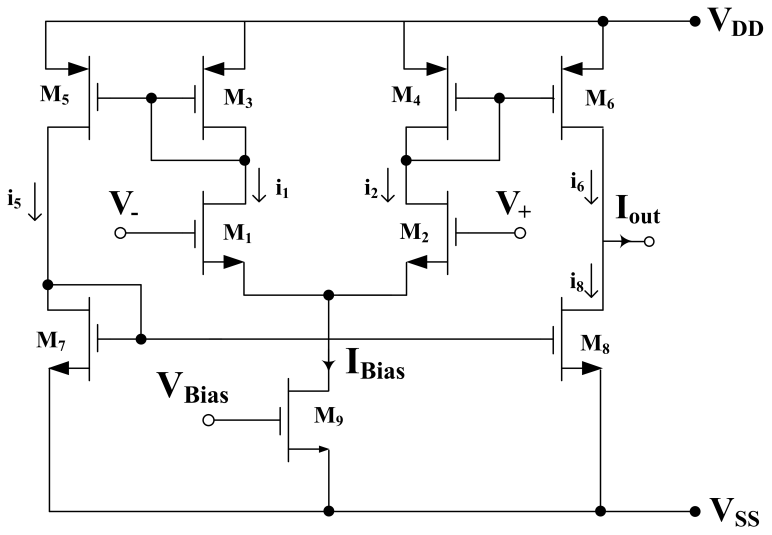


Figure 3.10: Exemplary CMOS implementation of OTA[55]

The TOQSOs presented in Fig. 3.8 were designed for a nominal frequency of oscillation equal to 15.9 MHz using identical capacitors ($C_1 = C_2 = C_3$) of value 10pF. The various transconductance values used for Fig. 3.8(a-d) (set by appropriate selection of the bias voltages (V_{Bias})) are given in Table 3.6.

Table 3.6: Various transconductance values used for Fig. 3.8.

Figures	$g_{m1}(m\text{S})$	$g_{m2}(m\text{S})$	$g_{m3}(m\text{S})$
Fig. 3.8(a)	2	1	1
Fig. 3.8(b)	1	1	1
Fig. 3.8(c)	1	1	1
Fig. 3.8(d)	1	1	2

Fig. 3.11 depicts the simulated transient and steady-state responses of the proposed TOQSOs of Fig. 3.8. The simulated frequency spectrum of the proposed TOQSOs are depicted in Fig. 3.12. Fig. 3.13 displays the steady state responses of current quadrature outputs for the Figs. 3.8(a-d) respectively.

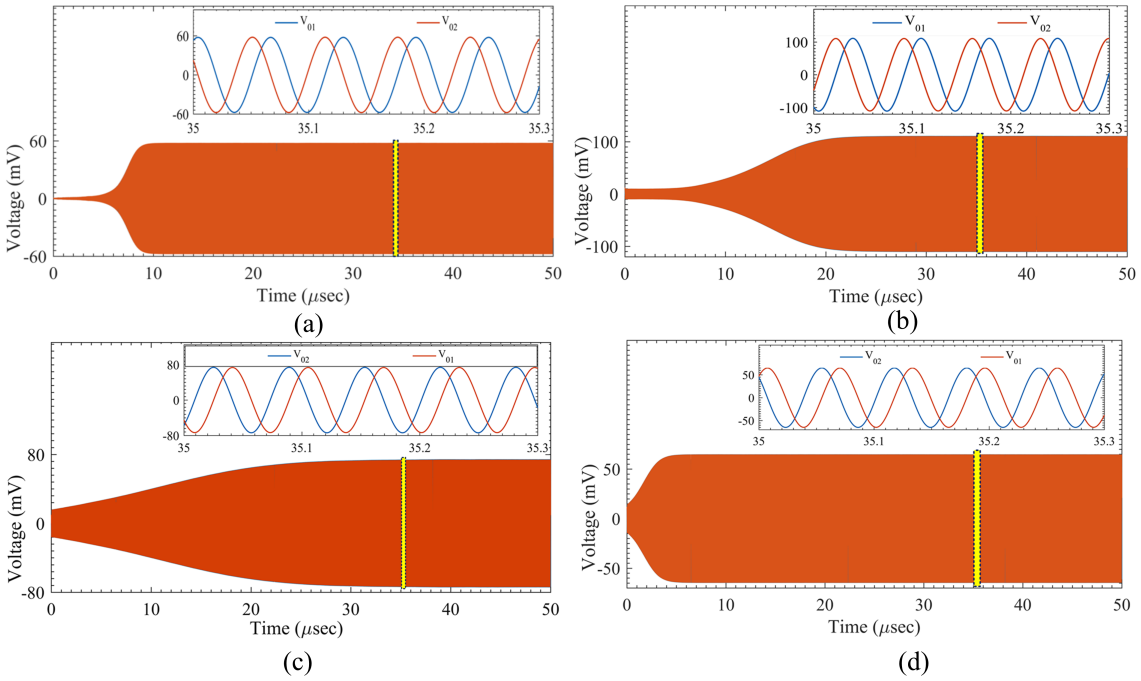


Figure 3.11: Simulated transient and steady state responses of the voltages of TO-QSOs of Fig. 3.8.

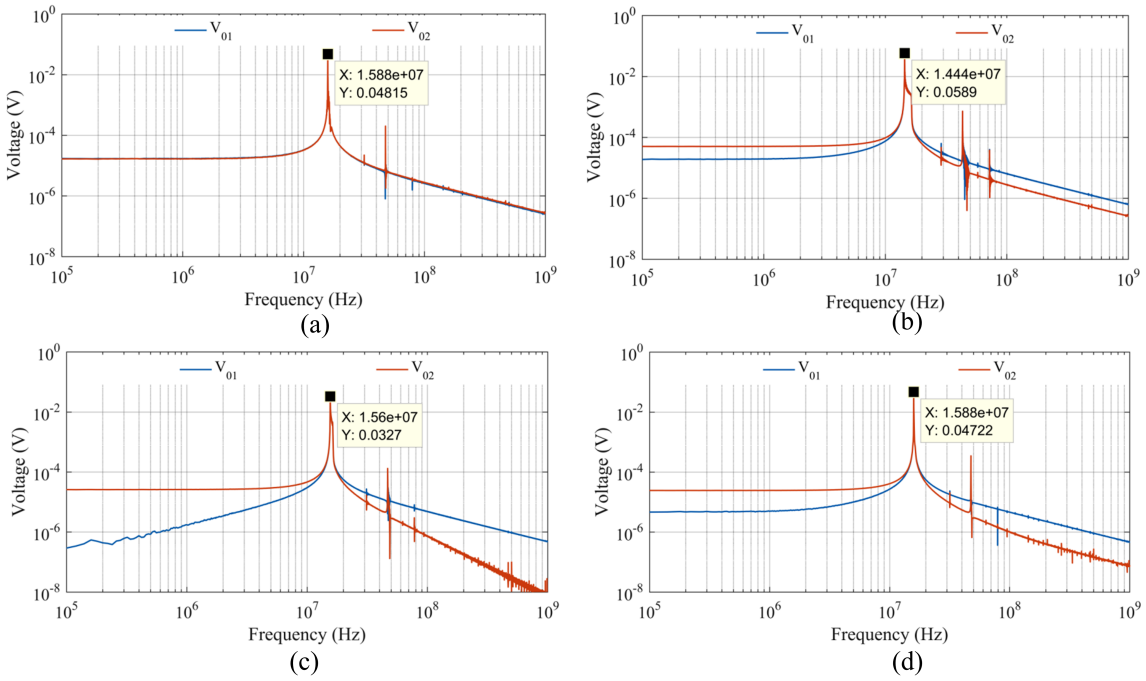


Figure 3.12: The simulated spectrum of proposed TOQSOs of Fig. 3.8.

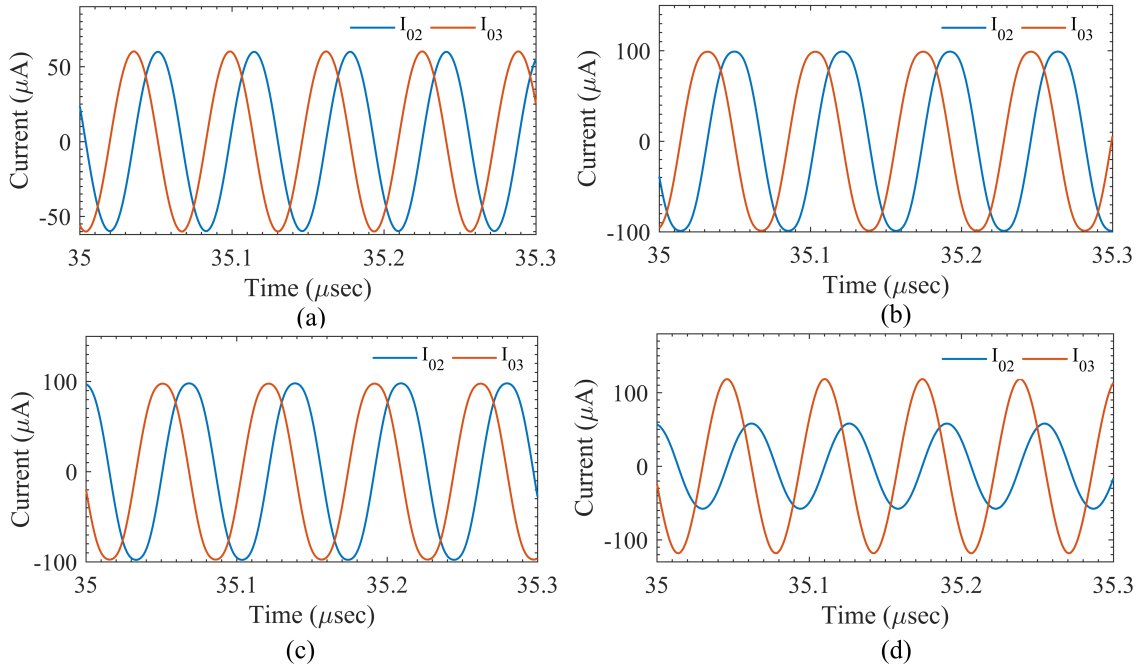


Figure 3.13: The simulated transient current quadrature outputs of Fig. 3.8.

The simulated values of FO, total harmonic distortion (%THD) and phase (ϕ) of the proposed TOQSO circuits have been given in Table 3.7.

Table 3.7: Simulated frequency, %THD, and phase (ϕ) for the circuits of Fig. 3.8.

	Fig. 3.8(a)	Fig. 3.8(b)	Fig. 3.8(c)	Fig. 3.8(d)
f_0 (MHz)	15.88	14.44	15.6	15.88
THD(%)V_{01}	0.404	1.172	0.466	0.582
THD(%)V_{02}	0.495	1.303	0.499	0.386
ϕ (Degree)	90.21	87.115	89.5	90.16

From Table 3.7, it may be noted that the simulated frequencies and phases are very close to their respective theoretical values.

3.2.5 Experimental Results

The workability of the TOQSO circuits presented in Fig. 3.8 was tested experimentally also, using discrete components. All the circuits shown in Fig. 3.8 were bread-boarded (using off-the-shelf OTA IC LM13700, 1% tolerance resistors, and 10% tolerance capacitors) and tested for experimental verification of the theory. For biasing of LM13700, $\pm V_{CC}$ was set to $\pm$15V. Identical capacitors of value 1nF were used for all the four configurations in Fig. 3.8 for a nominal oscillation frequency of 880 kHz.

Fig. 3.14 shows the snapshot of experimental setup.

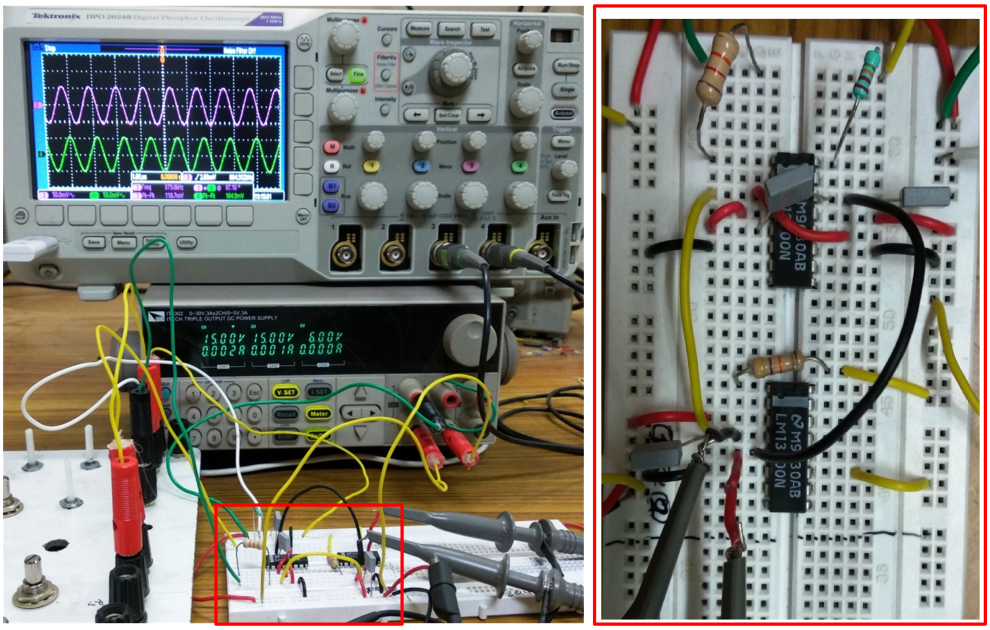


Figure 3.14: Experimental setup for TOQSO shown in Fig. 3.8(d).

The values of the various biasing resistors used for tuning the transconductances of different OTAs are given in Table 3.8.

Table 3.8: Various biasing resistors used for experimental setup.

Figure	R_{Bias1}	R_{Bias2}	R_{Bias3}
Fig. 3.8(a)	22k+22k pot	100k	100k
Fig. 3.8(b)	86k+22k pot	100k	100k
Fig. 3.8(c)	86k+22k pot	100k	100k
Fig. 3.8(d)	86k+22k pot	22k	22k

Fig. 3.15 to Fig. 3.18 represent the transient responses along with frequency spectrum of the proposed TOQSOs. From the hardware results, the obtained frequencies were found to be 875.3 kHz, 875.8 kHz, 875.7 kHz and 879.1 kHz respectively which are very close to the theoretical value of the FO (880 kHz). The experimental Lissajous patterns (X-Y plots) for Figs. 3.8(a-d) are depicted in Fig. 3.19.

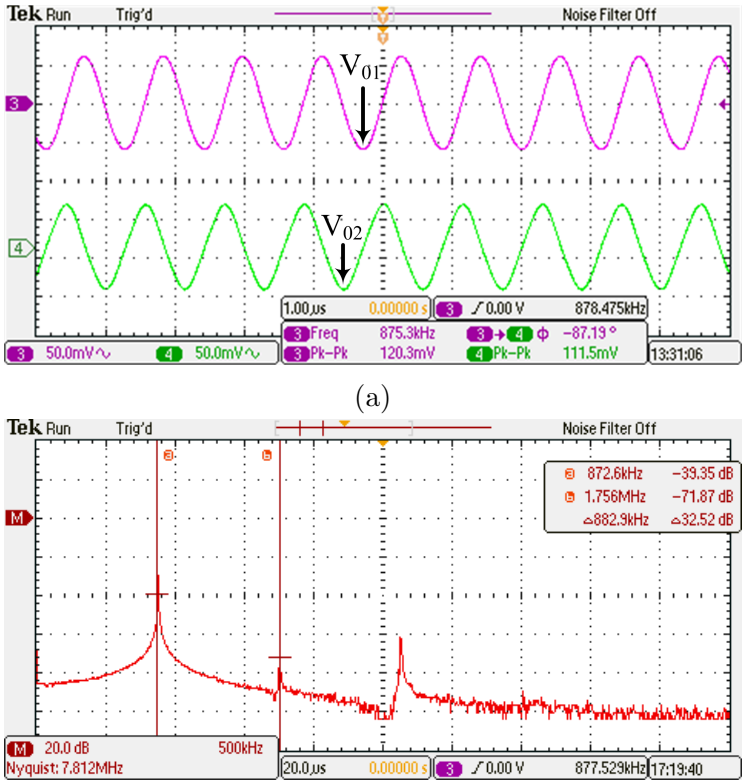
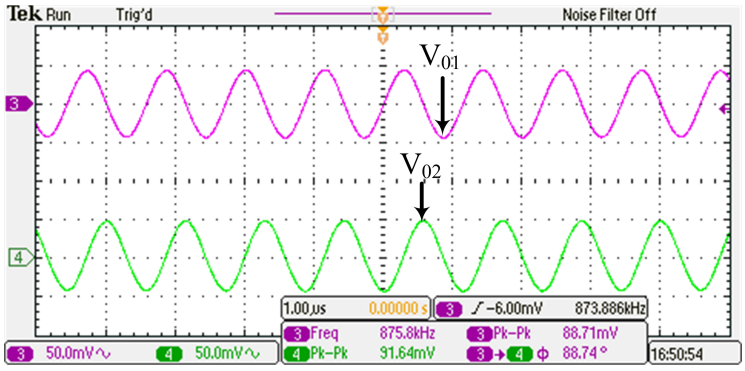
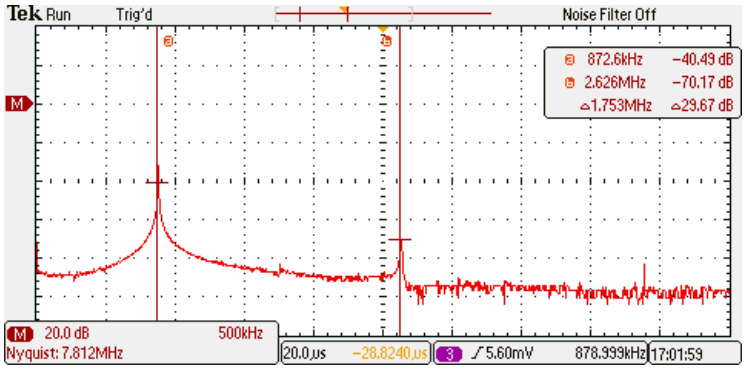


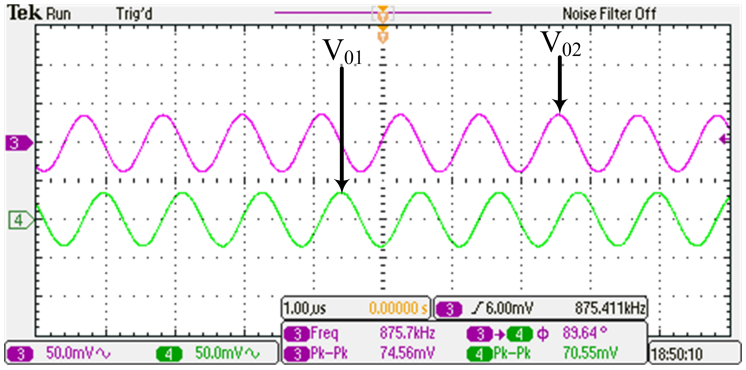
Figure 3.15: The experimental VM quadrature output waveforms and the frequency spectrum of Fig. 3.8(a).



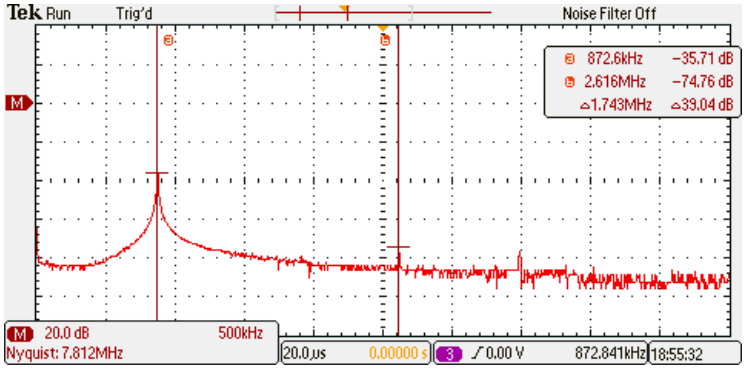


(b)

Figure 3.16: The experimental VM quadrature output waveforms and the frequency spectrum of Fig. 3.8(b).

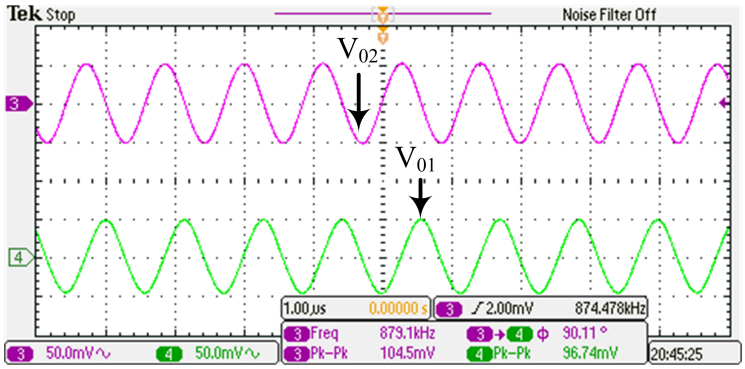


(a)

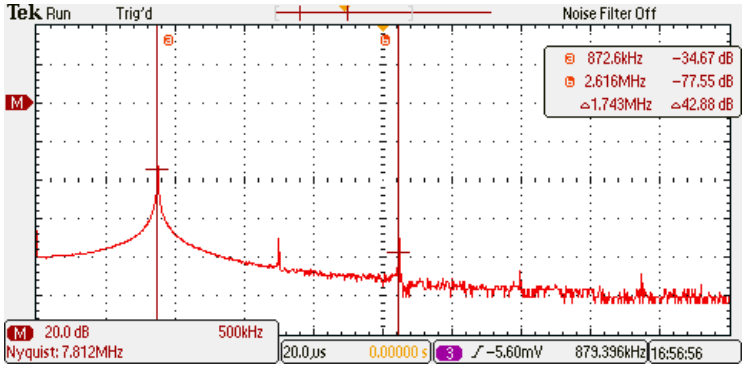


(b)

Figure 3.17: The experimental VM quadrature output waveforms and the frequency spectrum of Fig. 3.8(c).

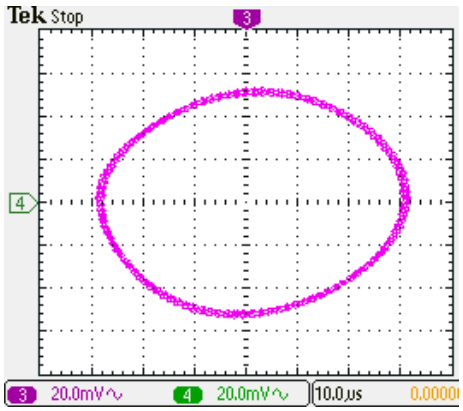


(a)

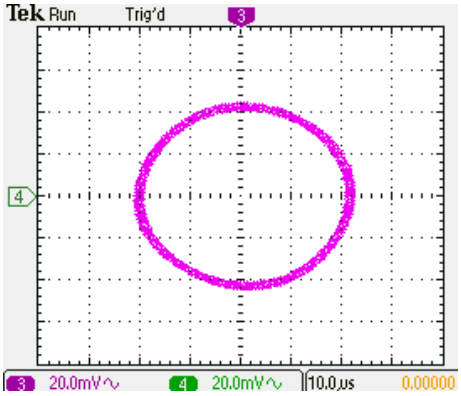


(b)

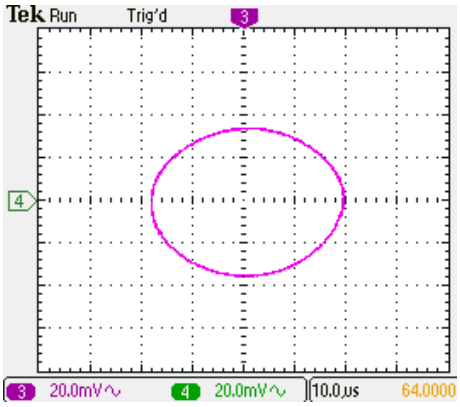
Figure 3.18: The experimental VM quadrature output waveforms and the frequency spectrum of Fig. 3.8(d).



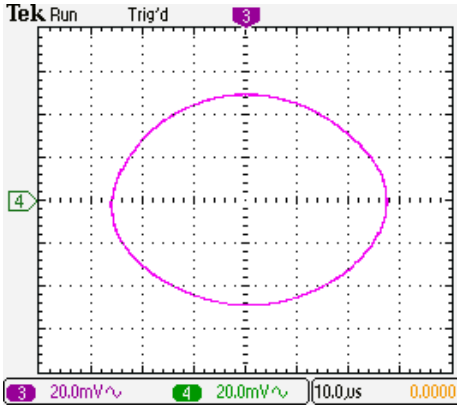
(a)



(b)



(c)



(d)

Figure 3.19: Lissajous pattern of proposed TOQSOs of Fig. 3.8

The error in frequency and phase of the proposed TOQSOs between theoretical and experimental values have been tabulated in Table 3.9.

Table 3.9: Error in experimental FO and phase of proposed TOQSOs.

Figure	Error in frequency (%)	Error in phase(%)
Fig. 3.8(a)	0.53%	3%
Fig. 3.8(b)	0.47%	1.40%
Fig. 3.8(c)	0.48%	0.40%
Fig. 3.8(d)	0.10%	0.12%

From, Table 3.9, it may be noted that the error in frequency and phase is very low for the designed frequency of 880 kHz.

3.3 Third-Order Quadrature Sinusoidal Oscillators Using four OTAs and Grounded Capacitors[2]

Though, all the circuits proposed in the previous section perform well and have the attaractive feature of operating in both VM and CM, if the multiple output OTAs are used in the realization, the use of floating capacitors is not preferred from the point of view of IC implementation.
In this section, a systematic realization of TOQSOs has been presented employing OTAs and grounded capacitors with fully decoupled control of CO and FO.

A lossless inverting integrator in feedback with a second-order voltage-mode (VM) low pass filter topology shown in Fig. 3.20 has been used to generate the third order CE.

The block diagram of the topology to realize TOQSOs is shown in Fig. 3.20

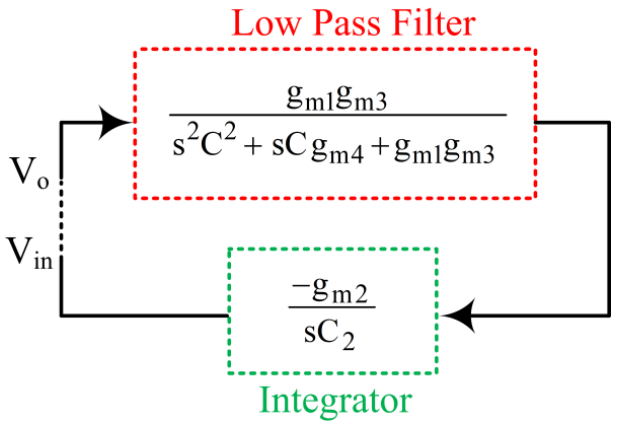
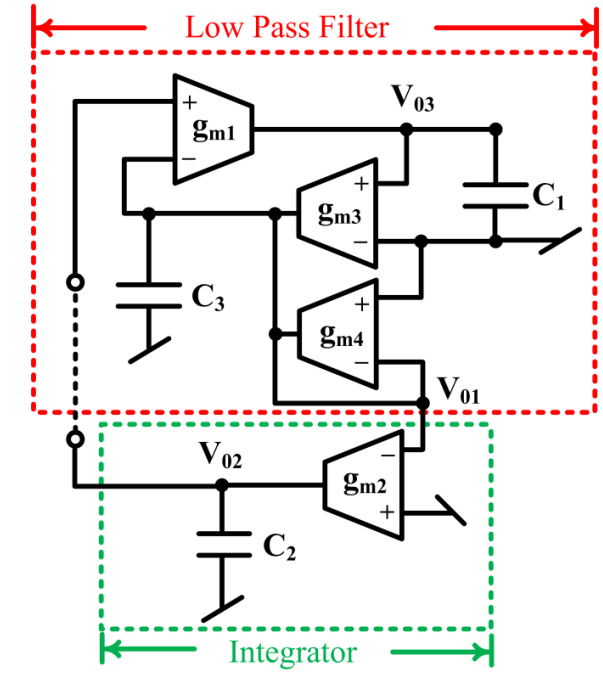


Figure 3.20: Functional block diagram used for realizing TOQSO

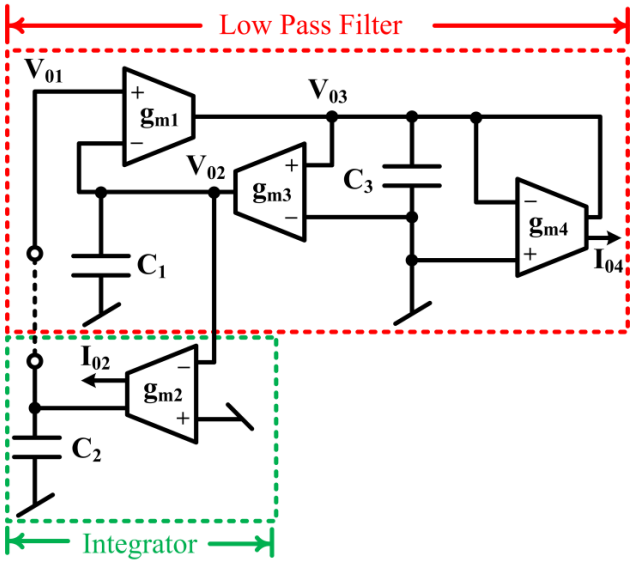
[2]The material presented in this section has been published in: Ajishek Raj, D. R. Bhaskar, and Pragati Kumar, "Two New Third-Order Quadrature Sinusoidal Oscillators" IETE Journal of Research, (2021)

3.3.1 TOQSO Circuits with Grounded Capacitors

Based on the functional block diagram shown in Fig. 3.20, two TOQSOs have been realized and are shown in Fig. 3.21.



(a)



(b)

Figure 3.21: New structures of TOQSOs

Through a routine circuit analysis of Fig. 3.21, characteristic equation (CE), CO,

and FO of both the TOQSOs are obtained as:

$$s^3C_1C_2C_3 + s^2C_1C_2g_{m4} + sC_2g_{m1}g_{m3} + g_{m1}g_{m2}g_{m3} = 0 \tag{3.10}$$

$$CO : \frac{g_{m2}}{g_{m4}} = \frac{C_2}{C_3} \quad FO : \omega = \sqrt{\frac{g_{m1}g_{m3}}{C_1C_3}} \tag{3.11}$$

Both the structures are canonical for the realization of third order oscillators, with independent control of CO and FO using separate sets of transconductances, as they use four OTAs and three capacitors only. Circuits with canonical number of components are preferred because of lower power consumption and improved reliability. It may be observed from equation (3.11) that CO of the proposed oscillators can be independently controlled electronically with the set of two separate transconductances g_{m2} and g_{m4}, while FO has independent electronic adjustment with the set of two other transconductances (g_{m1} and g_{m3}) for equal valued capacitors ($C_1 = C_2 = C_3$). Further, if we require linear electronic control of FO, which is a desirable feature to design VCOs, then g_{m1} and g_{m3} should be controlled simultaneously (i.e., $g_{m1} = g_{m3}$) without disturbing CO. The flexibility of being able to control CO independently is beneficial for incorporating amplitude stabilization into such TOQSOs.

Furthermore, the output voltages (V_{01} and V_{02} for Fig. 3.21a) and (V_{01} and V_{02}, V_{02} and V_{03} for Fig. 3.21b) of the proposed TOQSOs are in quadrature, and the quadrature relationships between the output voltages of Fig. 3.21a and Fig. 3.21b are given below.

$$Fig.3.21a \quad \frac{V_{02}(s)}{V_{01}(s)} = -\frac{g_{m2}}{sC_2} \quad \frac{V_{02}(j\omega)}{V_{01}(j\omega)} = -\frac{g_{m2}}{\omega C_2}e^{-j90^\circ} \tag{3.12}$$

$$Fig.3.21b \quad \frac{V_{02}(s)}{V_{03}(s)} = \frac{g_{m3}}{sC_1} \quad \frac{V_{02}(j\omega)}{V_{03}(j\omega)} = \frac{g_{m3}}{\omega C_1}e^{-j90^\circ} \tag{3.13}$$

$$Fig.3.21b \quad \frac{V_{01}(s)}{V_{02}(s)} = -\frac{g_{m2}}{sC_2} \quad \frac{V_{01}(j\omega)}{V_{02}(j\omega)} = -\frac{g_{m2}}{\omega C_2}e^{-j90^\circ} \tag{3.14}$$

Equations (3.12), (3.13) and (3.14) provide the voltage quadrature outputs from the proposed TOQSOs.

The amplitude ratio between different voltages in steady state (s=jω) are given in equations (3.15), (3.16), and (3.17) corresponding to the equations (3.12), (3.13) and (3.14) respectively.

$$|\frac{V_{02}(j\omega)}{V_{01}(j\omega)}| = \frac{g_{m2}}{\omega C_2} = \left(\frac{g_{m2}}{C_2}\right)\sqrt{\frac{C_1 C_3}{g_{m1} g_{m3}}} \tag{3.15}$$

$$|\frac{V_{02}(j\omega)}{V_{03}(j\omega)}| = \frac{g_{m3}}{\omega C_1} = \sqrt{\frac{g_{m3}}{g_{m1}}\frac{C_3}{C_1}} \tag{3.16}$$

$$|\frac{V_{01}(j\omega)}{V_{02}(j\omega)}| = \frac{g_{m2}}{\omega C_2} = \left(\frac{g_{m2}}{C_2}\right)\sqrt{\frac{C_1 C_3}{g_{m1} g_{m3}}} \tag{3.17}$$

It may be noted from equation (3.16) that for equal valued capacitors, the amplitude ratio of quadrature voltages (V_{02} and V_{03}) depends on the ratio of transconductances (g_{m1} and g_{m3}). These quadrature output voltages will, thus, be equal at any frequency for equal valued transconductances g_{m1} and g_{m3} (it can be achieved electronically by varying bias current of OTA_1 and OTA_3 simultaneously). The amplitude of the output voltages, thus, may be controlled by stabilizing either V_{02} or V_{03} only. The development of such an amplitude control scheme, which is entirely OTA-based, is an interesting research problem. However, this feature is not available for the quadrature output voltages available in circuit shown in Fig. 3.21a (equation (3.15)) and Fig. 3.21b (equation (3.17)).

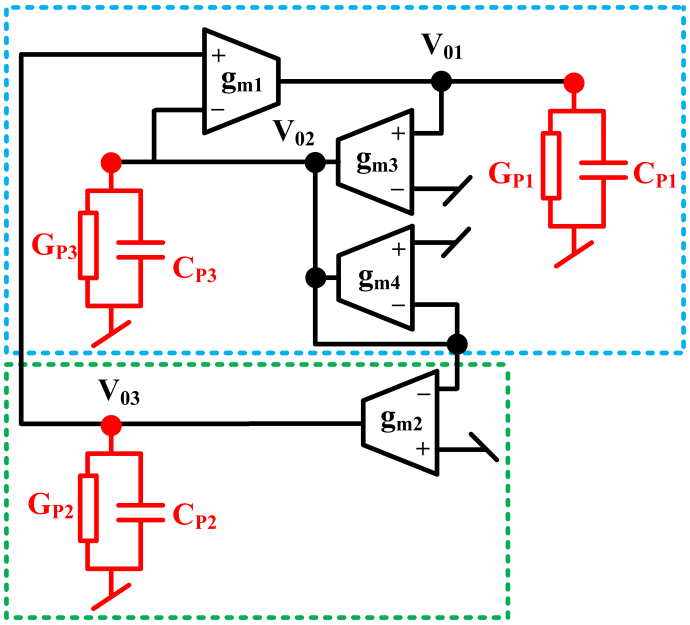
The circuit of Fig. 3.21b can also provide current outputs with quadrature as:

$$\frac{I_{02}(s)}{I_{04}(s)} = -\frac{g_{m2} g_{m3}}{s C_2 g_{m4}} \qquad \frac{I_{02}(j\omega)}{I_{04}(j\omega)} = -\frac{g_{m2} g_{m3}}{\omega C_2 g_{m4}} e^{-j90^\circ} \tag{3.18}$$

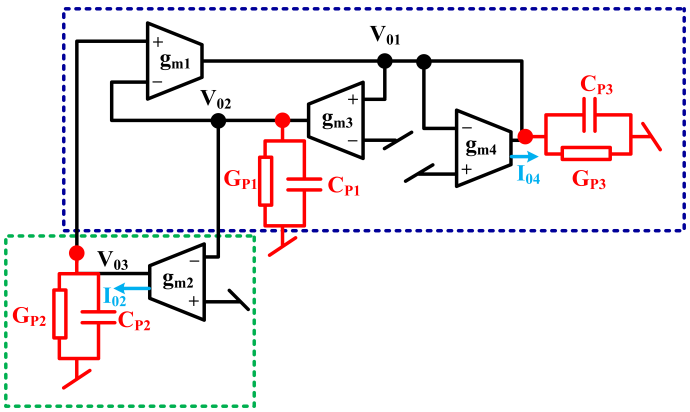
Therefore, from equation (3.18), it is clear that the two currents I_{02} and I_{04} are in quadrature.

3.3.2 Non-Ideal Analysis of Proposed TOQSO Structures

The non-ideal analysis of both the proposed oscillator circuits has been performed considering parasitic resistances and capacitances at the output terminals of the OTAs (it is interesting to note that the parasitic capacitances and resistances with the input terminals of all the four OTAs have been absorbed) as shown in Fig. 3.22.



(a)



(b)

Figure 3.22: Complete oscillator circuits including parasitic elements of OTAs

The CE and FO obtained with the influence of parasitic resistances and capacitances have been evaluated and given in equations (3.19) - (3.20).

$$CE_{ni}: \quad s^3(C_{P1}C_{P2}C_{P3}) + s^2(C_{P1}C_{P3}G_{P2} + C_{P1}C_{P2}(G_{P1} + G_{P3} + g_{m4})) + s(C_{P1}G_{P2}(G_{P1} + G_{P3} + g_{m4}) + C_{P2}(G_{P1}g_{m4} + G_{P1}G_{P3} + g_{m1}g_{m3})) + g_{m1}g_{m3}(G_{P2} + g_{m2}) = 0 \tag{3.19}$$

$$\omega_{ni} = \omega_{ideal}\sqrt{1 + \frac{C_{P2}G_{P1}(G_{P3} + g_{m4}) + C_{P1}G_{P2}(G_{P1} + G_{P3} + g_{m4})}{C_{P2}g_{m1}g_{m3}}} \tag{3.20}$$

For Fig. 3.22a: $G_{P1} = g_{o1}$, $G_{P2} = g_{o2}$, $G_{P3} = g_{o3} + g_{o4}$, $C_{P1} = C_{o1} + C_1$, $C_{P2} = C_{o2} + C_2$ and $C_{P3} = C_{o3} + C_{o4} + C_3$

For Fig. 3.22b: $G_{P1} = g_{o3}$, $G_{P2} = g_{o2}$, $G_{P3} = g_{o1} + g_{o4}$, $C_{P1} = C_{o3} + C_1$, $C_{P2} = C_{o2} + C_2$ and $C_{P3} = C_{o1} + C_{o4} + C_3$

We have measured the values of the G_{pi} = 1.307 x 10^{-9}℧ and C_{pi} = 0.284 x 10^{-18}F (i $\rightarrow$ 1 - 4) using PSPICE simulations and calculated the non-ideal value of FO. After substituting these values in equation (3.20), the value of FO was found to be 15.895 MHz, corresponding to an ideal value of 15.9 MHz. Such a small value of the %age error is not surprising, as all the parasitic capacitances are absorbed in the external capacitors.

The quadrature output voltage relationship with parasitic resistances and capacitances are also calculated and are given below:

$$\frac{V_{02}(s)}{V_{01}(s)} = -\frac{g_{m2}}{sC_{P2} + G_{P2}} = \frac{g_{m2}}{\sqrt{\omega^2 C_{P2}^2 + G_{P2}^2}} \angle - tan^{-1}\left(\frac{\omega C_{P2}}{G_{P2}}\right) \tag{3.21}$$

$$\frac{V_{02}(s)}{V_{01}(s)} = -\frac{g_{m2}}{sC_{P2} + G_{P2}} = \frac{g_{m2}}{\sqrt{\omega^2 C_{P2}^2 + G_{P2}^2}} \angle - tan^{-1}\left(\frac{\omega C_{P2}}{G_{P2}}\right) \tag{3.22}$$

$$\frac{V_{02}(s)}{V_{03}(s)} = -\frac{g_{m3}}{sC_{P1} + G_{P1}} = \frac{g_{m3}}{\sqrt{\omega^2 C_{P1}^2 + G_{P1}^2}} \angle - tan^{-1}\left(\frac{\omega C_{P1}}{G_{P1}}\right) \tag{3.23}$$

After substituting the values of ω, C_{Pi}, and G_{Pi} in equations (3.21), (3.22), and (3.23), it may be noted that the non-ideal phases of the proposed oscillators are approximately equal to 89.99°, instead of the ideal value 90°. Thus, it may be concluded that the effect of parasitics on the proposed TOQSOs is quite low.

3.3.3 Frequency Stability

We have used the open-loop transfer function of the proposed oscillator circuits given in equation (3.24) to evaluate the frequency stability factor $S^F = 2\sqrt{n}$ where $g_{m1} = g_{m3} = ng$ and $g_{m2} = g_{m4} = g$.

$$H(s) = \left(\frac{g_{m1}g_{m3}}{s^2C_1C_3 + sC_1g_{m4} + g_{m1}g_{m3}}\right)\left(\frac{-g_{m2}}{sC_2}\right) \tag{3.24}$$

As the FO and CO are uncoupled, the value of 'n' can be made very large, resulting in a very high-frequency stability.

3.3.4 Simulation Results

Both the proposed oscillator circuits were simulated using PSPICE wherein CMOS OTA implemented with TSMC 0.18µm CMOS technology parameters, as shown in Fig. 3.10 was used. The supply voltages used were ± 0.9V. The proposed oscillators were designed for a nominal frequency of oscillation equal to 15.9 MHz by taking $g_{m1} = g_{m2} = g_{m3} = g_{m4} = 1$ m℧ and capacitors of value 10 pF. Fig. 3.23 and Fig. 3.24 show the simulated steady-state responses of the proposed TOQSOs of Fig. 3.21a and Fig. 3.21b, respectively. The simulated X-Y plots of proposed TOQSOs are depicted in Fig. 3.25.

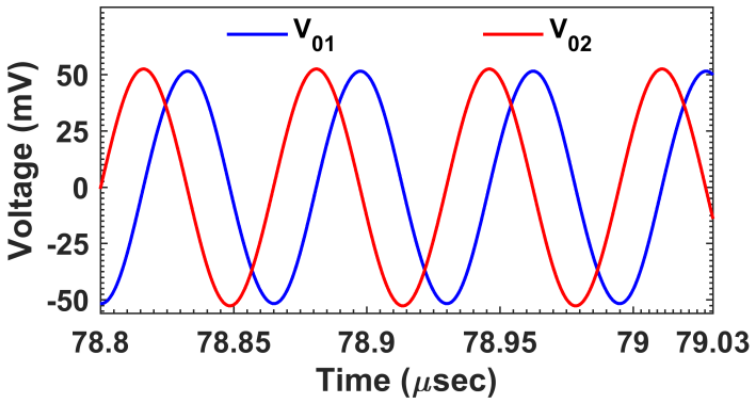
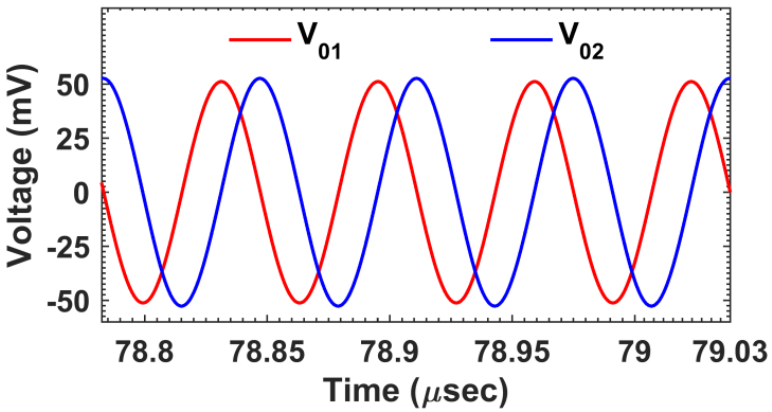
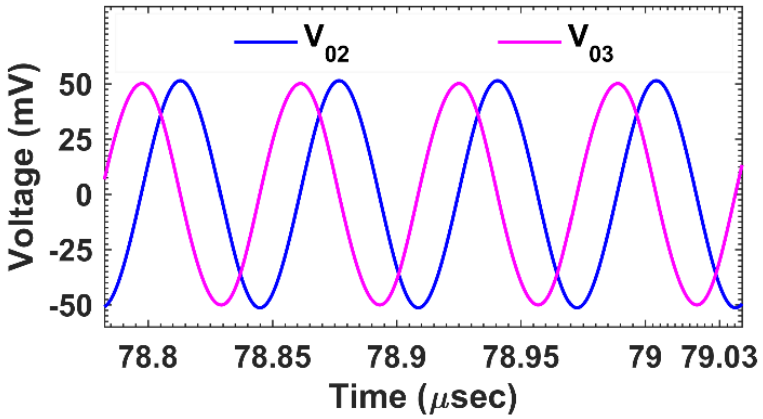


Figure 3.23: Simulated steady-state voltage responses of Fig. 3.21a

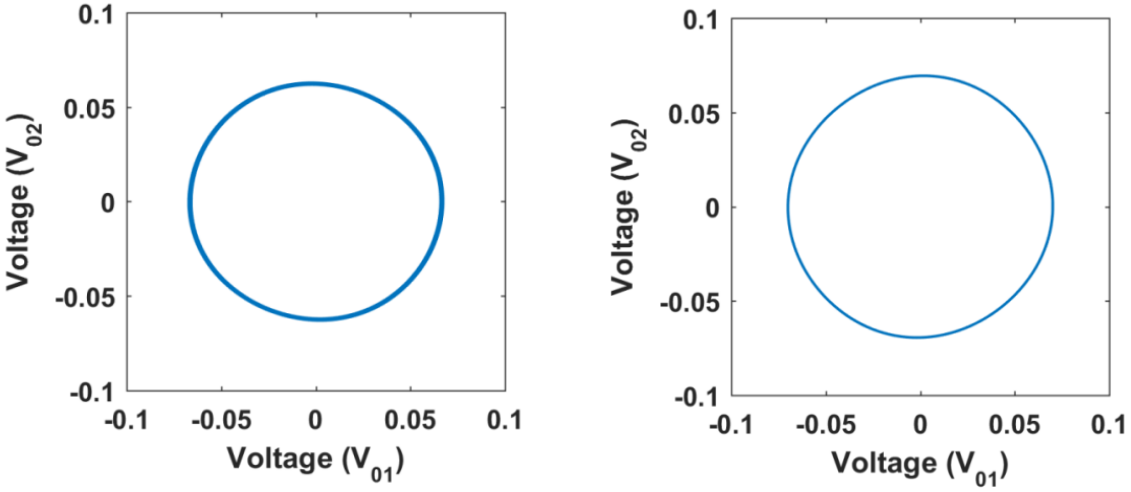


(a)



(b)

Figure 3.24: Simulated steady-state voltage responses of Fig. 3.21b



(a) (b)

Figure 3.25: Simulated Lissajous pattern (X-Y plot) of Fig. 3.21

The frequency of oscillation obtained from the simulation results for Fig. 3.21a and Fig. 3.21b are found to be 15.55 MHz and 15.64 MHz, respectively, which

concur with the theoretical analysis.

3.3.4.1 Tunability of FO with bias currents

The transconductance of the OTA [55] is given by:

$$g_{mi} = \sqrt{2K_n I_{Biasi} \left(\frac{W}{L}\right)_1} = K_x \sqrt{I_{Biasi}} \tag{3.25}$$

where $K_x = \sqrt{2K_n \left(\frac{W}{L}\right)_1}$

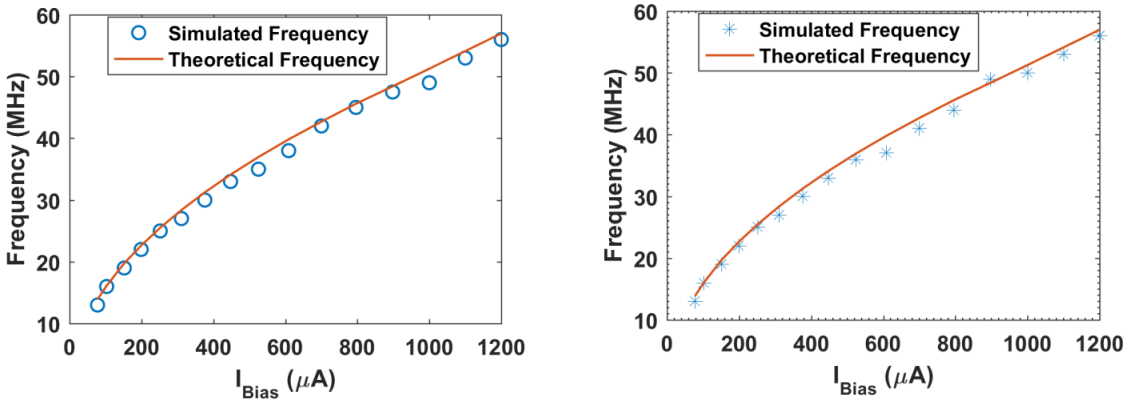
The transconductance g_{mi} (i $\rightarrow$ 1 - 4) of OTA is directly proportional to the square root of bias current (I_{Bias}). The tuning of FO of the proposed TOQSO circuits can be done by varying the bias current of OTAs. The FO of the proposed oscillators in terms of bias currents is given by:

$$\omega = \frac{K_x}{\sqrt{C_1 C_3}} (I_{Bias1} I_{Bias3})^{\frac{1}{4}} \tag{3.26}$$

To verify the decoupled adjustment of CO and FO, we have considered $I_{Bias1} = I_{Bias3} = I_{Bias}$ which reduces equation (3.26) to:

$$\omega = \frac{K_x}{\sqrt{C_1 C_3}} \sqrt{I_{Bias}} \tag{3.27}$$

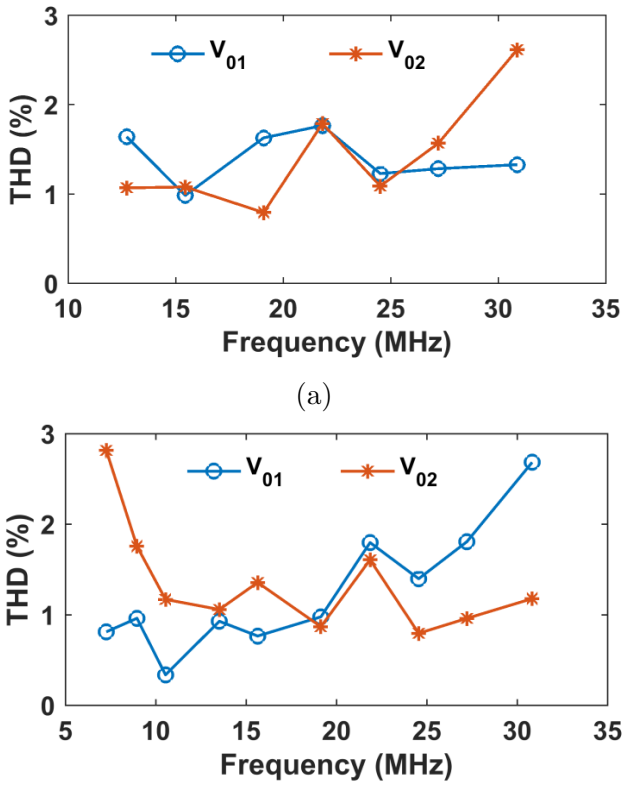
We have varied the values of $g_{m1} = g_{m3}$ from 1.06 m℧ to 3.58 m℧ (corresponding changes to I_{Bias}) while the values of $g_{m2} = g_{m4}$ were kept constant at 1 m℧. It was found that the FO varied between 13 MHz to 56 MHz. The frequency variation with I_{Bias} for both the structures of Fig. 3.21 has been depicted in Fig. 3.26.



(a) (b)

Figure 3.26: Frequency variation with I_{Bias} for Fig. 3.21

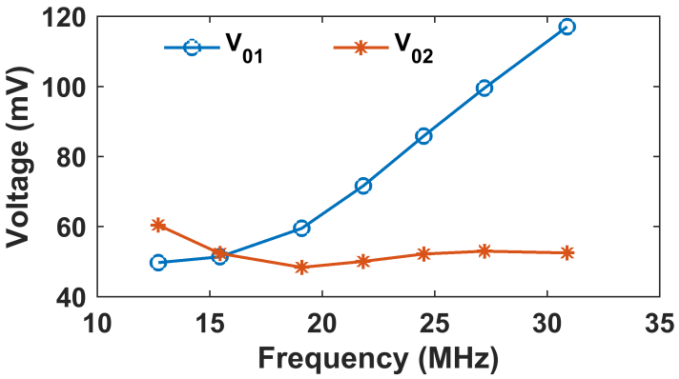
The variations of %THD and output voltages with frequency for the oscillator circuits shown in Fig. 3.21 have been displayed in Fig. 3.27 and Fig. 3.28 respectively.



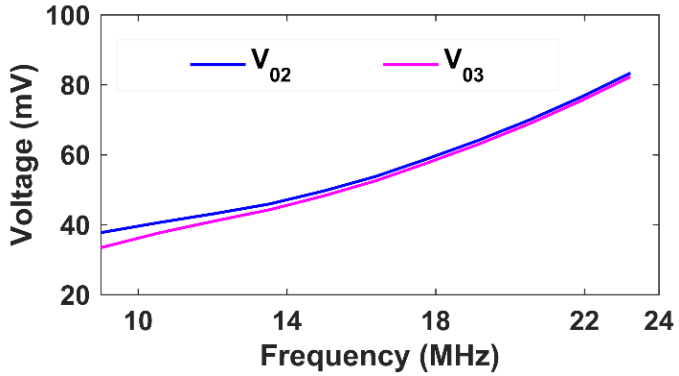
(a)

(b)

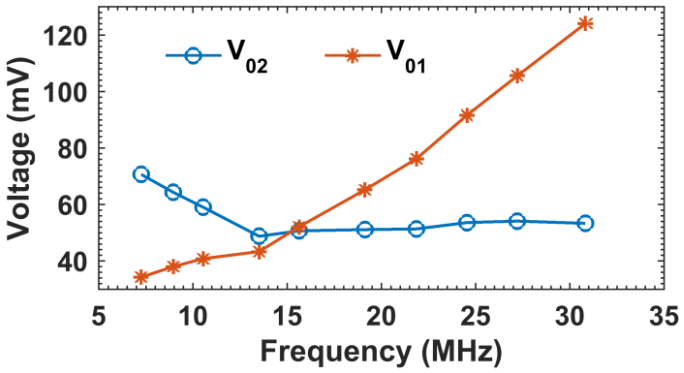
Figure 3.27: Variation in %THD with different frequencies for Fig. 3.21



(a)



(b)



(c)

Figure 3.28: Variation in voltage with different frequencies for (a) V_{01} and V_{02} of Fig. 3.21a, (b) V_{02} and V_{03} of Fig. 3.21b (c) V_{01} and V_{02} of Fig. 3.21b

The power dissipation (P_D), %THD, and phase (ϕ) of the proposed TOQSO structures observed in the simulations have been given in Table 3.10.

It is noted from Table 3.10, the P_D and %THD of the new proposed circuits are low and their phase difference between the two outputs in each case is nearly equal to 90°.

Table 3.10: Simulated frequency, %THD, P_D, and phase (ϕ) of Fig. 3.21

Parameter	Fig. 2(a)	Fig. 2(b)
THD % (V_{01})	1.255	0.904
THD % (V_{02})	1.550	1.13
P_D(mW)	1.120	1.10
ϕ(Degree)	90.27	90.7

We have also simulated the circuit of Fig. 3.21b for CM quadrature outputs for the same values of transconductances and capacitors as used for VM operation. Fig. 3.29 shows the simulated steady state response. Fig. 3.30 displays Lissajous pattern of the oscillator circuit presented in Fig. 3.21b.

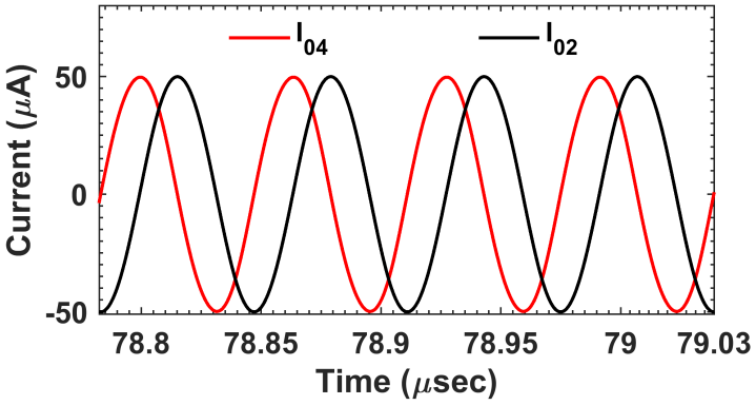


Figure 3.29: Simulated steady state quadrature current responses of Fig. 3.21b

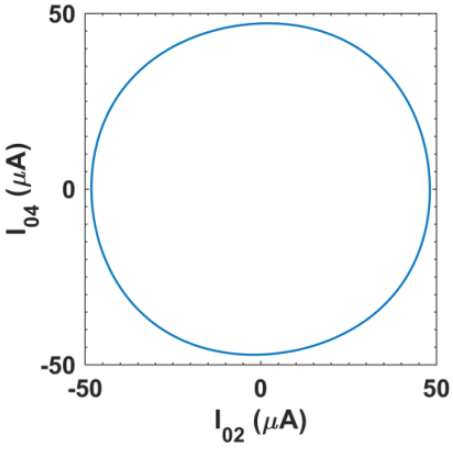


Figure 3.30: Simulated Lissajous pattern (X-Y plot) of Fig. 3.21b

These simulation results, thus, confirm the workability of the proposed TOQSO circuits.

3.3.5 Experimental Results

The workability of the proposed TOQSO circuits shown in Fig. 3.21 has also been verified experimentally using discrete components. The presented TOQSOs were bread-boarded (using off-the-shelf OTA IC LM13700, 1% tolerance resistors, and 10% tolerance capacitors) and tested for experimental verification of the theory. A single LM13700 contains two single output OTAs and two buffers within the IC package. The pin connection of $\frac{1}{2}$ LM13700 OTA, including arrangement for generation of I_{Bias} is shown in Fig. 3.31 whereas the experimental setup of Fig. 3.21b has been displayed in Fig. 3.32.

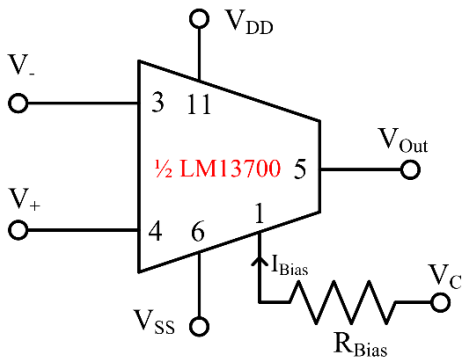


Figure 3.31: Pin connection and arrangement for generating I_{Bias}

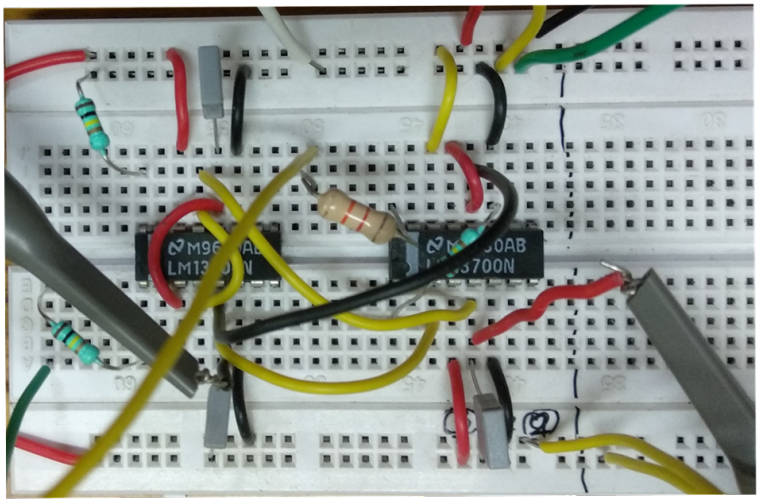
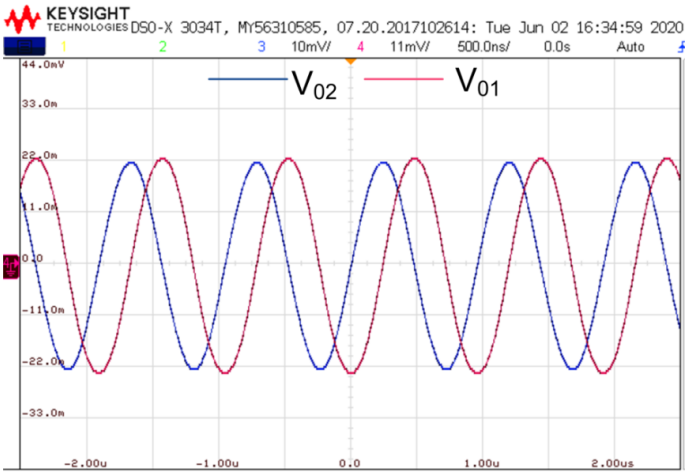
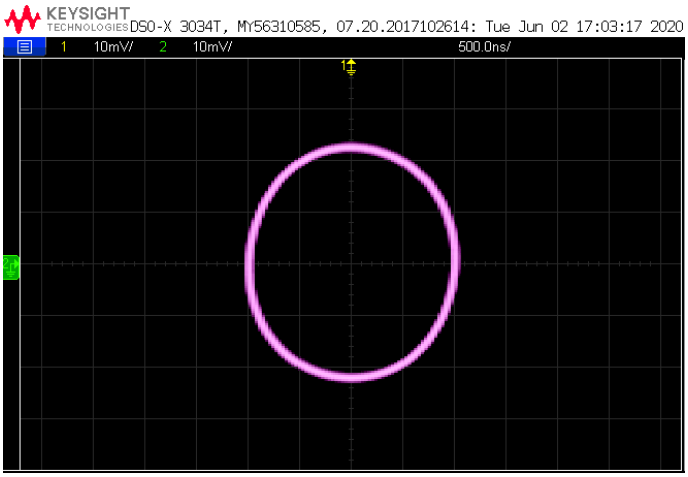


Figure 3.32: Experimental setup for TOQSO shown in Fig. 3.21b

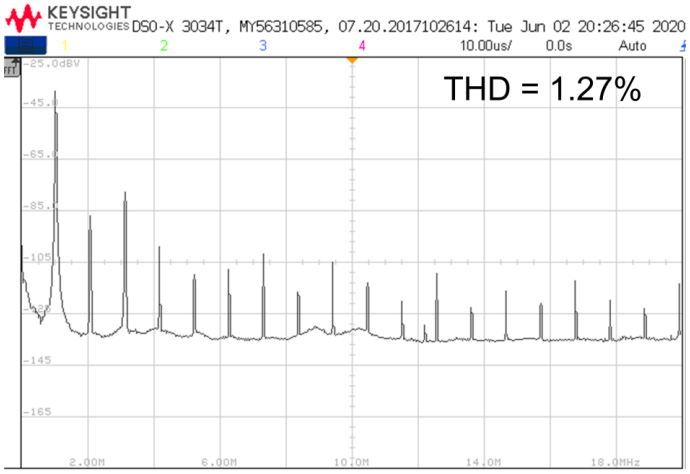
The presented TOQSO circuits were implemented for a nominal oscillation frequency of 1 MHz. For this oscillation frequency, the biasing voltages for OTA_1–OTA_4 were set at $\pm 15V$. Identical capacitors of value 1 nF were used for Fig. 3.21a and Fig. 3.21b. The biasing resistors R_{bias1}, R_{bias2}, and R_{bias3} were taken as 100 kΩ for Fig. 3.21a and Fig. 3.21b, respectively. For building up the oscillations, R_{bias4} was adjusted with (86kΩ + 47 kΩ) pot. Fig. 3.33 and Fig. 3.34 represent the transient responses, Lissajous patterns (X-Y plot), and frequency spectrum of both the quadrature output voltages of Fig. 3.21a and Fig. 3.21b, respectively.



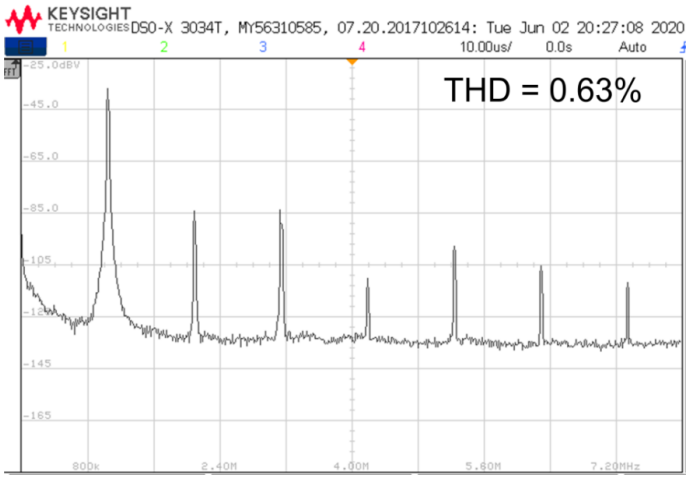
(a)



(b)

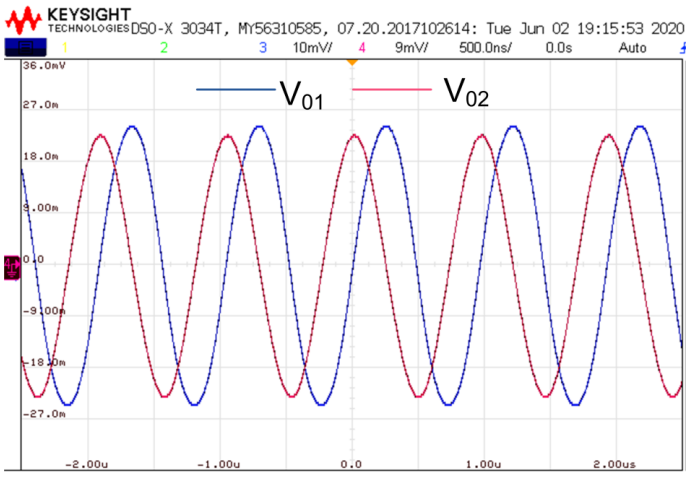


(c)

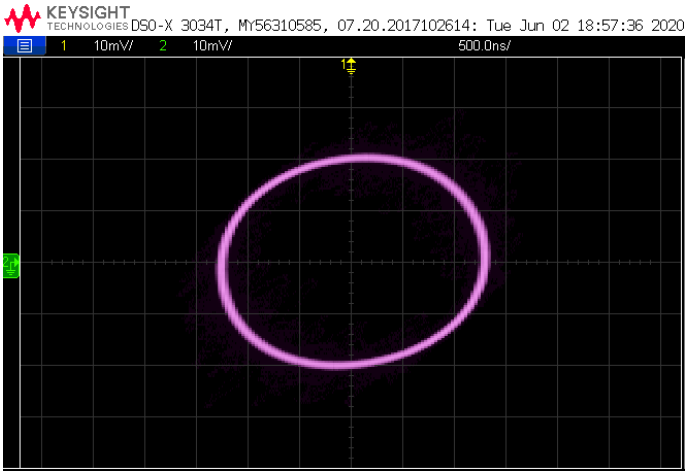


(d)

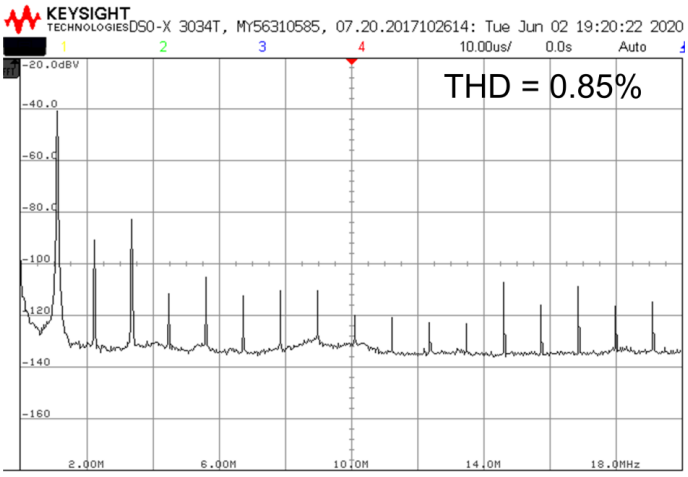
Figure 3.33: Experimental quadrature transient output waveforms, XY pattern and their frequency spectrum of Fig. 3.21a.



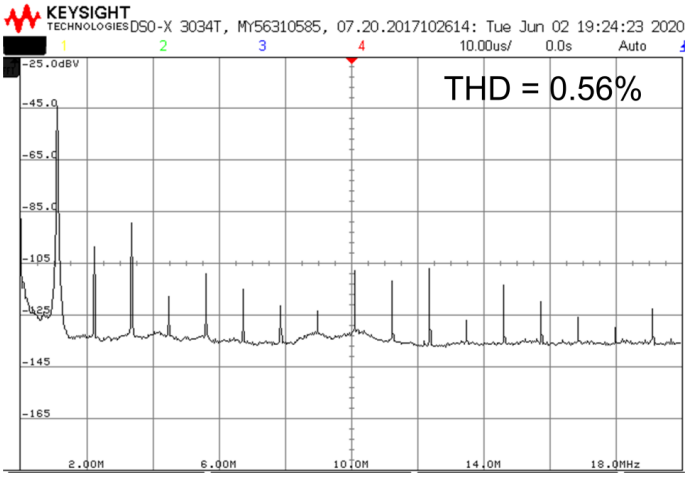
(a)



(b)



(c)



(d)

Figure 3.34: Experimental quadrature transient output waveforms, XY pattern and their frequency spectrum of Fig. 3.21b.

The peak to peak output voltages (V_{01} and V_{02}) of the oscillator circuits for Fig. 3.21a and Fig. 3.21b were recorded as 40.48 mV, 46.05 mV and 54.55 mV, 46mV

respectively. The measured cut-off frequencies and phases for both the oscillators are (1.041 MHz, 89.57°) and (1.040 MHz, 85.88°) respectively. The %THD of the output voltages of both the oscillators is less than 1.3% that ensures good sinusoidal responses of the oscillator circuits.

To validate the decoupled nature of CO and FO experimentally, we have varied the control voltage (V_C) from $\pm 7V$ to $\pm 13V$ (for a change in I_{Bias} for OTA_1 and OTA_3 simultaneously) while the biasing voltages for OTA_2 and OTA_4 were kept constant at $\pm 8V$. It was found that the FO varied between 400 kHz to 780 kHz. Fig. 3.35 shows the measured frequency with V_C for the structure of Fig. 3.21b.

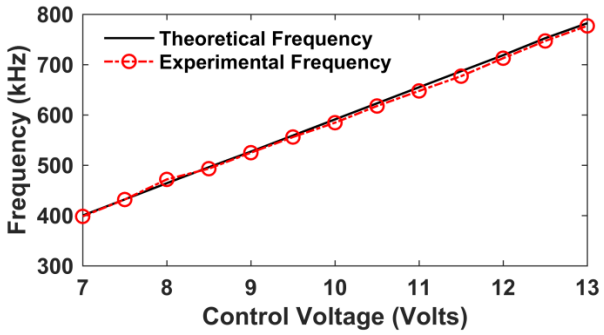


Figure 3.35: Variation of frequency with control voltage.

From Fig. 3.35, the frequency error between experimental and theoretical values was calculated and found to be less than 1.5%. We have also shown the experimental variation of quadrature output voltages when bias voltages of OTA_1 and OTA_3 were varied. The respective results have been illustrated in Fig. 3.36. From Fig. 3.36, it has been observed that the output voltages of Fig. 3.21b are approximately equal when g_{m1} and g_{m3} varied simultaneously.

The % THD of output voltages and phase errors between quadrature outputs of Fig. 3.21b have been displayed in Fig. 3.37 and Fig. 3.38 respectively.

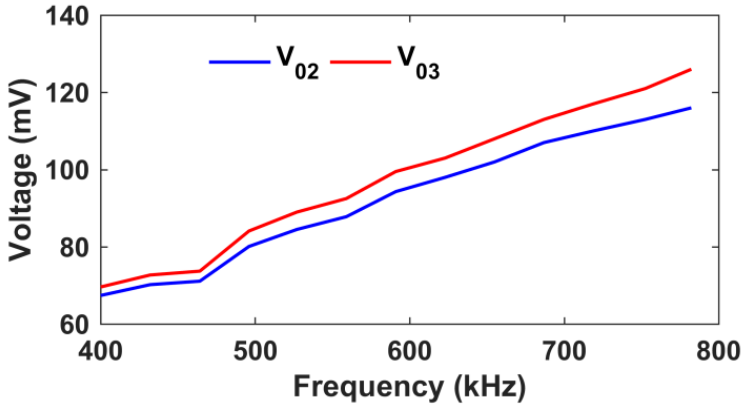


Figure 3.36: Experimental voltage variations of the proposed oscillator (3.21b) with different frequencies.

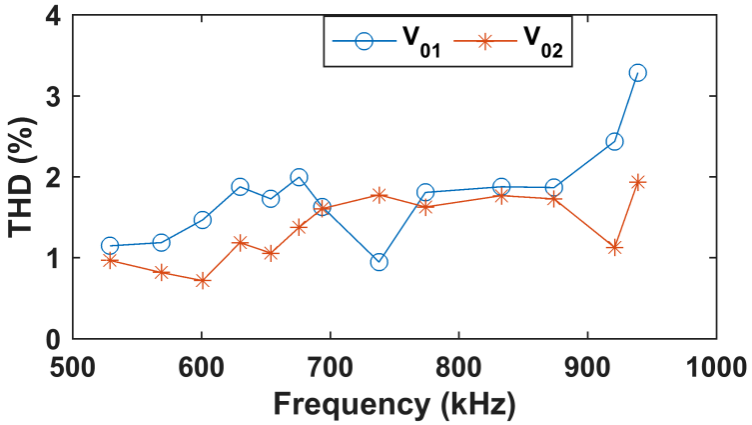


Figure 3.37: Experimental %THD variation with different frequencies for Fig. 3.21b

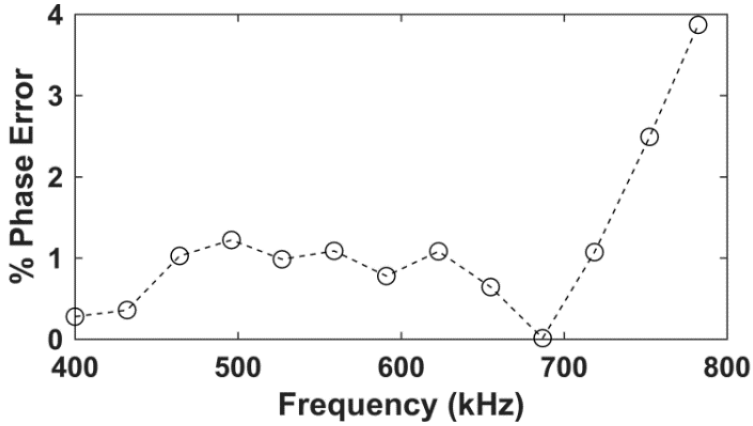


Figure 3.38: Error in phase of Fig. 3.21b with different frequencies

The maximum %THD and %phase error obtained experimentally have been recorded and found to be less than 4%. The simulation and experimental results thus, verify the validity of proposed third order quadrature sinusoidal oscillators of Fig. 3.21.

3.4 Concluding Remarks

The main contributions made in this chapter can be summarized as follows:
Four new configurations of TOQSOs employing three OTAs and three capacitors have been presented. The CO and FO of the proposed TOQSO circuits have independent electronic control and also have quadrature output voltages and quadrature output currents. Out of the four TOQSOs, two circuits have capacitor control of FO, a feature, useful in capacitive transducers. Non-ideal analyses of all the proposed TOQSO circuits have been carried out using a frequency dependent transconductance model and found that there is insignificant % error between ideal and non-ideal FO. The phase noise spectral density and frequency stability of the presented TOQSO circuits have also been evaluated. Various simulation results have been included along with the experimental results to verify the validity of the proposed TOQSO circuits. For experimental validation, off-the-shelf OTA ICs LM13700 have been employed. We have also presented a systematic realization of TOQSOs employing OTAs and grounded capacitors. The proposed technique uses a lossless inverting integrator in feedback with a second-order voltage-mode (VM) low pass filter to implement the TOQSOs. Implementation of the TOQSOs employing canonical numbers of OTAs and grounded capacitors having fully decoupled electronic control of both CO and FO have also been presented. Such sinusoidal oscillators are useful from the viewpoint of designing voltage controlled oscillators which find applications in frequency modulation or phase modulation. Non-ideal analyses of the proposed TOQSO circuits have also been carried out to support the theoretical propositions.

In conclusion, we hope that the TOQSO circuits presented in this chapter will aid and enrich the existing literature of TOQSOs

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Chapter 4

Third Order Sinusoidal Oscillators Using CFOAs

4.1 Introduction

In the previous chapter, we have presented several new circuit designs of third order quadrature sinusoidal oscillators employing OTAs.

As mentioned earlier, only one TOSO circuit has been reported so far employing current feedback operational amplifiers. In this chapter, first, we have tried to put the previously reported TOSO circuits in a unified theoretical framework then, we have proposed several new approaches for systematic realization of TOSOs using inverse filters. Several new CFOA-based TOSOs have also been realized using these approaches. Finally, we have also introduced a new approach for a systematic realization for low frequency third order sinusoidal oscillators with independent control of CO and FO.

4.2 Existing Approaches for the Design of TOSOs

The block diagram of a general feedback system in which sustained oscillations may be generated is given below in Fig. 4.1.

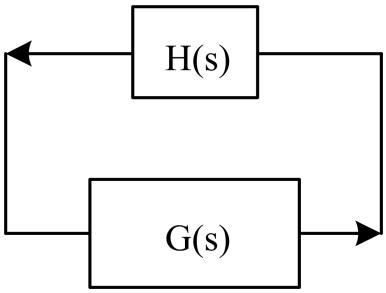


Figure 4.1: Generalized block diagram of an autonomous feedback system

The characteristic equation (CE) of the system shown in Fig. 4.1, is given by:

$$1 - G(s)H(s) = 0 \tag{4.1}$$

where G(s) is forward path gain and H(s) is the feedback gain.
Depending on the order of the above equation (4.1), the resulting oscillators may be classified as second order, third order or higher order oscillators. Since this chapter concerns with the TOSOs, we present the generalized CE of a third order sinusoidal oscillator as:

$$a_3 s^3 + a_2 s^2 + a_1 s + a_0 \ = \ 0 \tag{4.2}$$

Equation (4.2) may be rearranged in the form of equation (4.1) in different ways as follows:

4.2.1 TOSOs based on Second Order Lowpass Filter and Lossless Integrator

The CE of a third order sinusoidal oscillator as given in equation (4.2) can be rearranged in the form of:

$$s(a_3 s^2 + a_2 s + a_1) + a_0 = 0 \tag{4.3}$$

Furthermore, equation (4.3) may be rewritten as:

$$1 - \left(\frac{\mp a_0}{a_3 s^2 + a_2 s + a_1} \right) * \left(\frac{\pm 1}{s} \right) \ = \ 0 \tag{4.4}$$

Comparing equation (4.4) with (4.1), it can be concluded that for the realisation of TOSO, a cascade connection of second order inverting/non-inverting low pass filter with non-inverting/inverting lossless integrator in a unity feedback loop is required. Based on this technique, various TOQSOs have been reported [1–13]. An exemplary third order sinusoidal circuit based on this approach employing two voltage differencing inverting buffered amplifiers (VDIBAs) and three grounded capacitors has been shown in Fig. 4.2 [7].

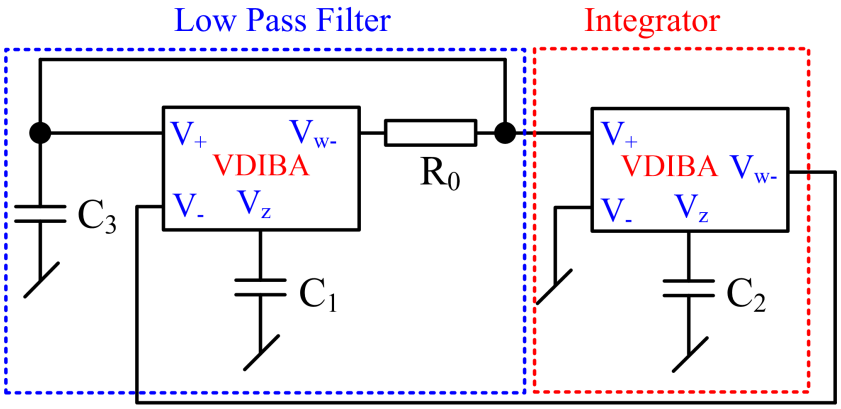


Figure 4.2: VDIBA based TOQSO circuit proposed by Pushkar and Bhaskar [7]

4.2.2 TOSOs based on Second Order Highpass Filter and Lossless Differentiator

Alternatively, equation (4.2) can also be rewritten as:

$$a_3 s^3 \;=\; -(a_2 s^2 + a_1 s + a_0) \tag{4.5}$$

Equation (4.5) can further be modified as:

$$1 - \left(\frac{\mp a_3 s^2}{a_2 s^2 + a_1 s + a_0} \right) * (\pm s) \;=\; 0 \tag{4.6}$$

From equation(4.6), it is observed that the CE of TOSO can also be derived by cascading a second order inverting/non-inverting high pass filter with a non-inverting/inverting lossless differentiator in a unity feedback loop.

Based on this approach, two TOSOs have been reported so far [8, 9]. An exemplary realization of TOSO circuit based on this technique is shown in Fig. 4.3 [8].

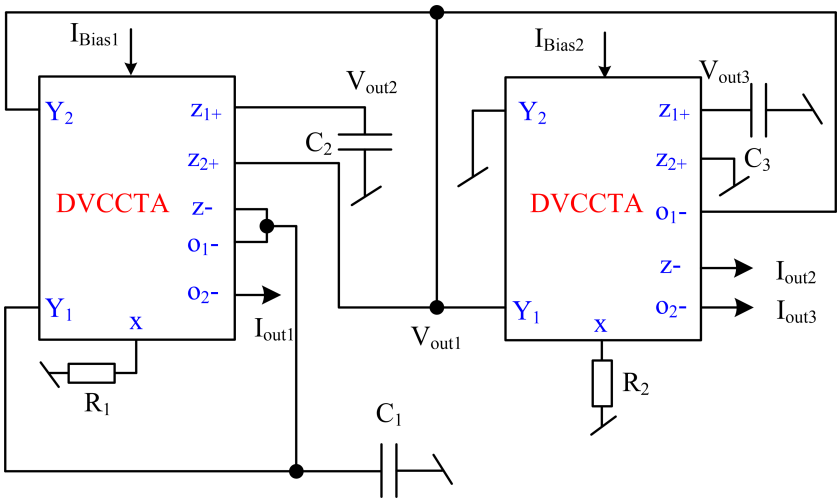


Figure 4.3: DVCCTA based TOSO circuit presented by Pandey and Pandey [8]

4.2.3 Combination of Two Lossy Integrators and One Lossless Integrator

Finally, the third order CE as given in equation (4.2) can also be represented as:

$$a_3 s^3 + (a_{21} + a_{22}) s^2 + a_1 s + a_0 \;=\; 0 \tag{4.7}$$

where $a_2 = a_{21} + a_{22}$

Now, if we take $a_3 = 1$ and $a_1 = a_{21} * a_{22}$, equation (4.7) becomes:

$$1 - \left[\left(\frac{1}{s + a_{21}} \right) * \left(\frac{-a_0}{s} \right) * \left(\frac{1}{s + a_{22}} \right) \right] \;=\; 0 \tag{4.8}$$

The implementation of equation (4.8) for the realisation of TOSO requires a cascade connection of two lossy integrators and one inverting lossless integrator in a unity feedback loop. Based on this approach, three circuits have been reported in open literature [6, 14, 15]. A TOSO based on this approach employing OTAs has been shown in Fig. 4.4 [15].

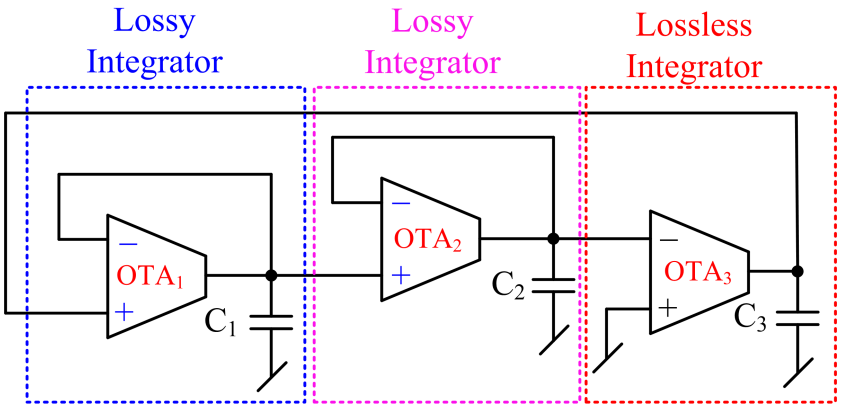


Figure 4.4: TOSO circuit reported by Prommee and Dehjan [15]

4.2.4 Combination of Two Lossless Integrators and One Lossy Integrator based TOSOs

Yet, another way to express the CE as given in equation (4.2) is:

$$s^2(a_3s + a_2) + a_1s + a_0 \;=\; 0 \tag{4.9}$$

Equation (4.9) can now be rearranged as:

$$1 - \left[\left(\frac{-1}{a_3s + a_2}\right) * \left(\frac{a_1}{s}\right) + \left(\frac{a_0}{s}\right) * \left(\frac{1}{s}\right) * \left(\frac{-1}{a_3s + a_2}\right)\right] \;=\; 0 \tag{4.10}$$

The above approach requires the combination of two lossless integrators and one lossy integrator to realise the CE of TOSO. Based on this technique, a number of TOSO circuits have been derived [6, 16–18]. One of the TOSO circuits based on this approach using OTRAs has been shown in Fig. 4.5 [6].

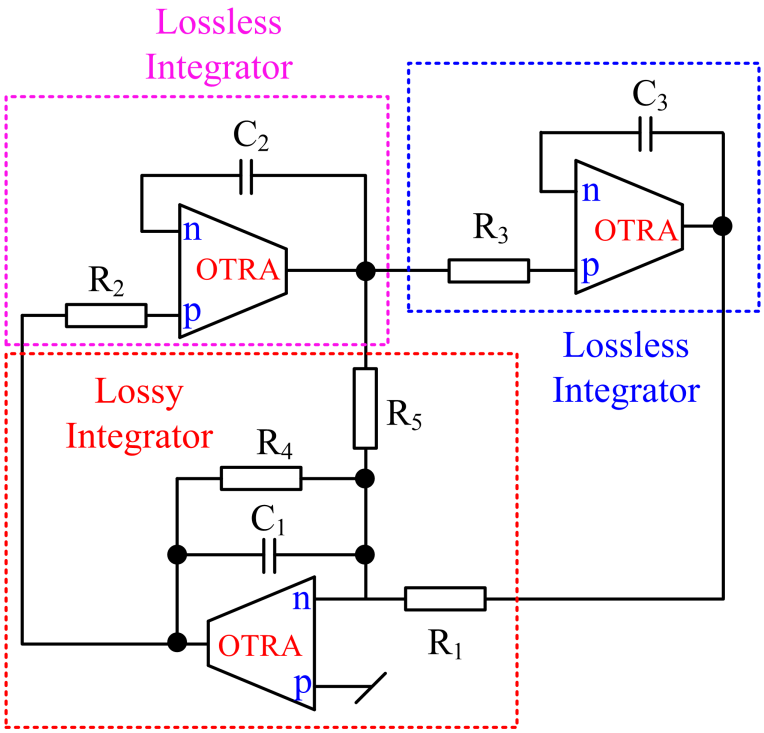


Figure 4.5: OTRA based TOSO circuit reported by Pandey, Pandey, Komanapalli and Anurag [6]

In the following, we now introduce two new decompositions of CE as given in equation (4.2) of TOSOs using which TOSO circuits may be designed with different ABBs and present exemplary realizations of TOSOs using CFOAs.

4.3 Proposed Approaches Using Inverse Filters for the Design of TOQSOs

The proposed approaches are based on a novel decomposition of the standard CE of a TOQSO, in terms of first order and second order inverse filters and lossy/lossless integrators.

4.3.1 First Order Inverse Highpass Filter, One lossy Integrator and One Lossless Integrator based Realization

The CE given in equation (4.2) can also be rearranged in the form of:

$$s^2(a_3 s + a_2) = -(a_1 s + a_0) \tag{4.11}$$

$$1 - \left(\frac{a_1 s + a_0}{s}\right) * \left(\frac{-1}{s}\right) * \left(\frac{1}{a_3 s + a_2}\right) = 0 \tag{4.12}$$

From equation (4.12), it can be observed that for the realization of third order quadrature sinusoidal oscillator, a non-inverting first order inverse high pass filter (IHPF) [19], a non-inverting lossy integrator and an inverting lossless integrator with a unity feedback are required. The block diagram representation of equation (4.12) has been shown in Fig. 4.6.

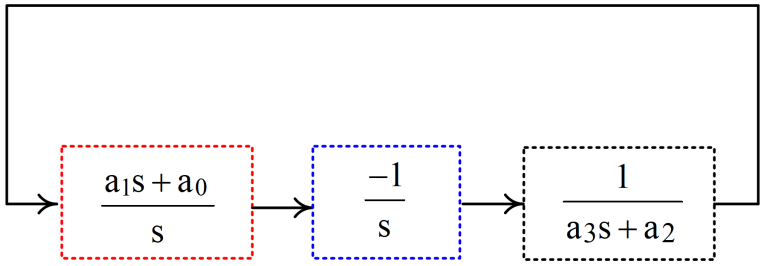


Figure 4.6: First order IHPF based TQOSO

Equation (4.12) can also be rewritten as:

$$1 - \left(\frac{a_1 s + a_0}{s}\right) * \left(\frac{1}{s}\right) * \left(\frac{-1}{a_3 s + a_2}\right) = 0 \tag{4.13}$$

From equation (4.13), it may be noted that for the implementation of CE of TOQSO, a non-inverting first order inverse high pass filter, an inverting lossy integrator and a non-inverting lossless integrator with a unity feedback are required. The block diagram representation of equation (4.13) is shown in Fig. 4.7.

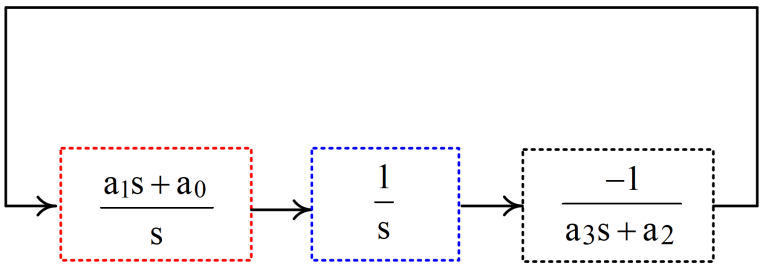
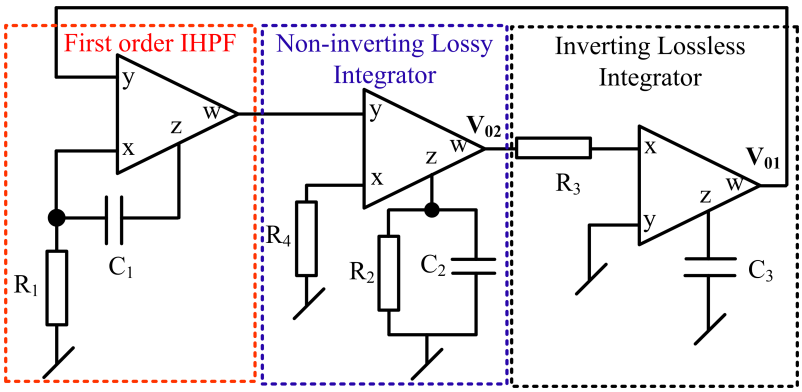


Figure 4.7: First order IHPF based TQOSO

4.3.1.1 Exemplary Implementation of Third-Order Quadrature Sinusoidal Oscillators Using first order IHPF Approach

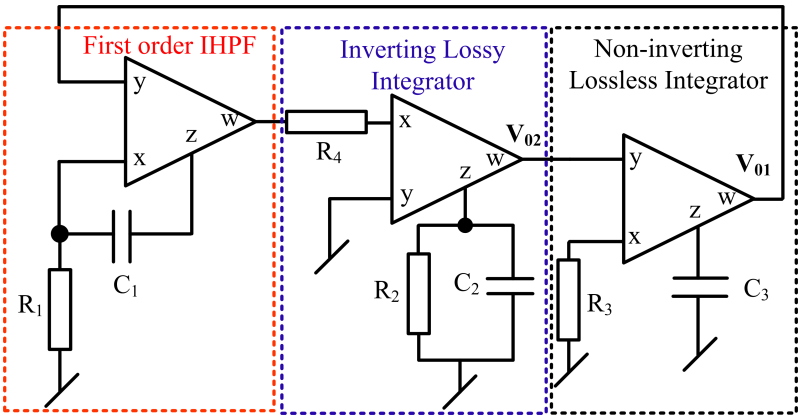
CFOA-based implementations of equations (4.12) and (4.13) employing three CFOAs, three capacitors and four resistors are shown in Fig. 4.8.



(a)

Assuming ideal CFOAs, a routine circuit analysis yields the following CE for both the circuits shown in Fig. 4.8:

$$s^3 (2C_1C_2C_4R_1R_2R_3R_4) + s^2 (2C_1C_4R_1R_3R_4) + s (2C_1R_1R_2) + R_2 = 0 \qquad (4.14)$$



(b)

Figure 4.8: Proposed CFOA-based TOQSO configurations using first order IHPF approach

Equating real and imaginary parts of equation (4.14) after substituting $s = j\omega$, CO and FO of the TOQSOs can be obtained as:

$$\begin{aligned} CO &: \frac{R_2}{2R_1} \geq \frac{C_1}{C_2} \\ FO &: \omega_0 = \frac{1}{\sqrt{C_2 C_3 R_3 R_4}} \end{aligned} \tag{4.15}$$

From equation (4.15), it may be observed that the CO and FO of the TOQSOs shown in Fig. 4.8, can be adjusted with different sets of resistors independently i.e., CO can be controlled through R_1 and R_2 (for $C_1 = C_2$), whereas, FO can be tuned independently through either R_3 or R_4. The CO and FO of the oscillators can also be independently adjusted by separate capacitors i.e., CO can be adjusted through C_1 (for $R_1 = R_2$) and FO can be independently controlled through C_3.

It is interesting to note that, because of the presence of a lossless integrator, there exists a quadrature relationship between V_{01} and V_{02} as given by:

$$\begin{aligned} \frac{V_{01}}{V_{02}} &= \mp\left(\frac{1}{sC_3R_3}\right) \\ \left|\frac{V_{01}}{V_{02}}\right| &= \frac{1}{\omega C_3 R_3} \angle \mp j90^\circ \quad = \sqrt{\frac{R_4}{R_3}\left(\frac{C_2}{C_3}\right)} \end{aligned} \tag{4.16}$$

From equation (4.16), it may be noted that the ratio of V_{01} and V_{02} has equal magnitudes when the resistors $R_3 = R_4$ are varied simultaneously with identical

values of capacitors.

4.3.1.2 Non-Ideal Analysis

To examine the effect of parasitic on TOQSO circuits shown in Fig. 4.8, we have carried out non-ideal analysis by taking a resistance r_x at terminal-X, and the parallel combination of R_p and $1/sC_p$ at terminal-Z of CFOAs. We have shown one of the oscillator circuits with the parasitic resistances and capacitances in Fig. 4.9.

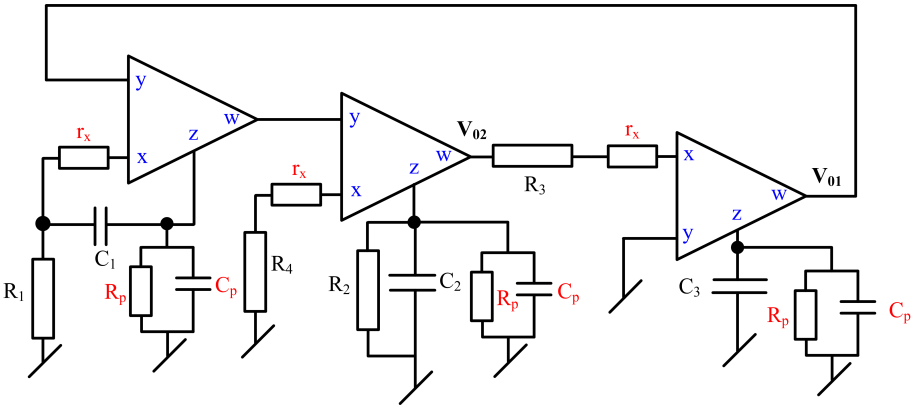


Figure 4.9: First order IHPF based TOQSO with parasitic

Considering the parasitic resistances and capacitances at the terminals X and Z of CFOAs, the non-ideal FO of the proposed oscillators shown in Fig. 4.8 is given by:

$$\omega_n^{/} = \omega_0 \sqrt{\frac{1+\frac{1}{2C_1R_p}\left(\frac{C_3^{/}}{R_2^{/}}+\frac{C_2^{/}}{R_p}\right)\left(1+\frac{r_x}{R_1}\right)+\frac{1}{R_2^{/}R_p}\left(1+\frac{r_x}{R_1}\right)\left(\frac{1}{2}+\frac{C_p}{C_1}\right)}{\left(1+\frac{r_x}{R_3}\right)\left(1+\frac{r_x}{R_4}\right)\left(1+\frac{C_p}{C_2}\right)\left(1+\frac{C_p}{C_3}\right)\left(\left(1+\frac{r_x}{R_1}\right)+\frac{C_p}{C_1}\left(\frac{1}{2}+\frac{r_x}{R_1}\right)+\frac{C_pr_x}{C_2^{/}R_2^{/}}+\frac{C_pr_x}{C_3^{/}R_p}\right)}} \tag{4.17}$$

where $R_i^{/} = R_i + r_x$, $C_i^{/} = C_i + C_p$ (for i = 1 – 3) and $R_2^{/} = R_2 \| R_p$

To reduce the influence of parasitic resistances and capacitances, the external resistances and capacitances should be selected as much larger than the parasitic resistances and capacitances such that:

$$C_i >> C_p\ (for\ i = 1\text{–}3), R_i >> r_x\ (for\ i = 1,3,4)\ and\ R_2 << R_p$$

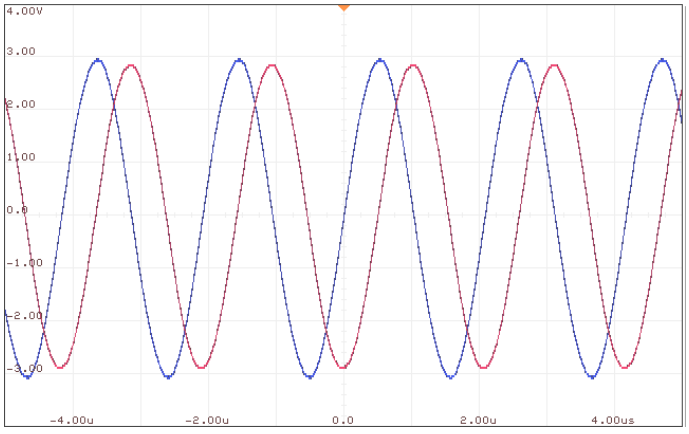
We have also evaluated the values of FO quantitatively considering $r_x = 50\Omega$, R_p

= 3MΩ, and C_p = 4.5pF, as 480.68 kHz, corresponding to the ideal value of 481.82 kHz. An error of 0.207% between ideal and non-ideal values of FO indicates that the parasitic resistances and capacitances do not affect the FO significantly.

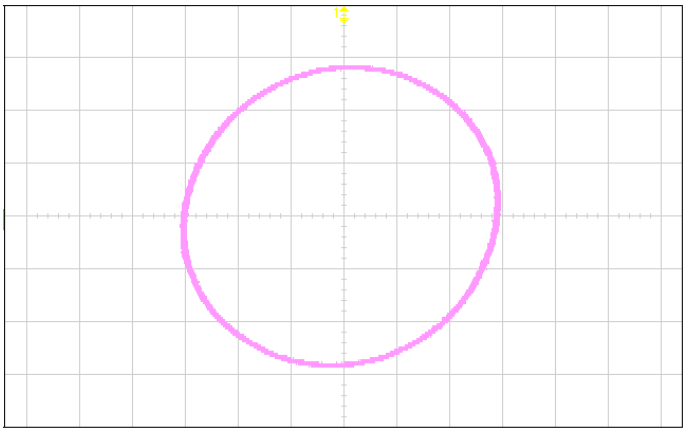
4.3.1.3 Experimental Results

For the experimental verification of the proposed TOQSOs derived using first approach, the TOQSO circuit of Fig. 4.8a was bread-boarded using AD844 type CFOAs, 5% tolerance resistors and 10% tolerance capacitors. The D.C. power supply voltages $\pm V_{CC}$ were kept at $\pm 8V$.

The oscillator circuit of Fig. 4.8a was designed for a nominal frequency of 481.82 kHz. The passive components R_1 = 1 kΩ, R_2 = 1 kΩ+ 1 kΩ (pot), R_3 = 2.2 kΩ, R_4 = 2.2 kΩ and the identical capacitors $C_1 = C_2 = C_3$ = 150 pF were used. The quadrature output voltage responses, Lissajous pattern and frequency spectrum of the first order IHPF approach-based TOQSO have been shown in Fig. 4.10a–4.10d respectively. The experimentally measured frequency of this oscillator was found to be 479.6 kHz while the phase difference between V_{01} and V_{02} was found as 87.57° (with a percentage phase error of 2.7%). The %THD in the output voltages V_{01} and V_{02} of the TOQSO were recorded as 0.76% and 1.06% respectively.



(a)



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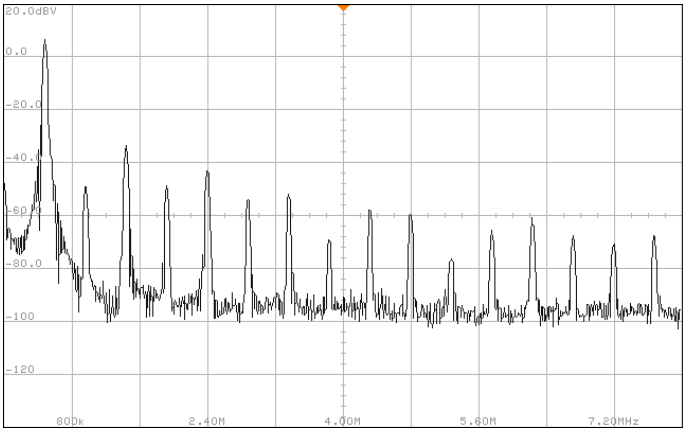
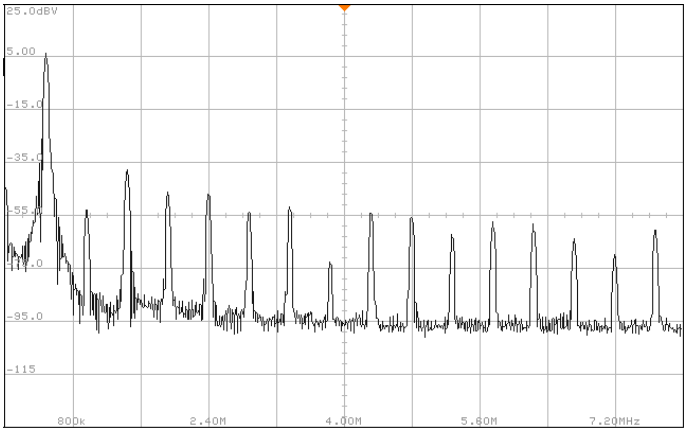


(c)



(d)

Figure 4.10: Experimental results of TOQSO shown in Fig. 4.8a (a) Transient voltage outputs (b) Lissajous pattern (X-Y plot) between V_{01} and V_{02} (c) Frequency spectrum of V_{01} and (d) Frequency spectrum of V_{02}

4.3.2 Second Order Inverse Highpass Filter and Lossless Integrator based Approach

The CE of TOQSO given in equation (4.2) can also be rewritten as:

$$a_3 s^3 = -(a_2 s^2 + a_1 s + a_0) \tag{4.18}$$

Equation (4.18) can be turned into a simplified equation as:

$$1 - \left(\frac{(a_2 s^2 + a_1 s + a_0)}{s^2}\right) * \left(\frac{-1}{a_3 s}\right) = 0 \tag{4.19}$$

From equation (4.19), it may be observed that a non-inverting second order IHPF [20] and inverting lossless integrator may also be used to realize CE given in equation (4.2) of a TOQSO. The block diagram representation of the CE as given in equation (4.19) is shown in Fig. 4.11.

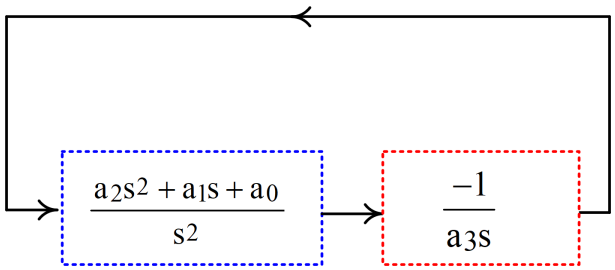


Figure 4.11: Second order IHPF based TQOSO design approach

4.3.2.1 Exemplary Implementation of TOQSO Using second order IHPF Approach

Fig. 4.12 shows a CFOA-based implementation of the TOQSO using the second approach.

The CE of this TOQSO as shown in Fig. 4.12, can be obtained (assuming ideal CFOAs) through a routine circuit analysis as:

$$s^3 (C_1 C_2 C_3 R_1 R_2 R_3) + s^2 (C_1 C_2 R_1 R_2) + s (C_1 R_1) + 1 = 0 \tag{4.20}$$

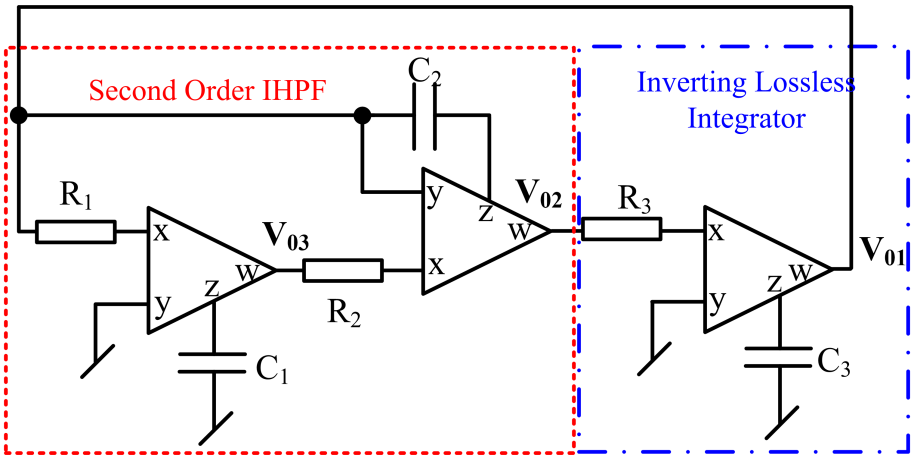


Figure 4.12: CFOA-based TOQSO using second order IHPF approach

Again equating the real and imaginary parts of equation (4.20) for $s = j\omega$, CO and FO of the proposed TOQSO are obtained as:

$$\begin{aligned} CO: &\quad \frac{R_3}{R_1} \geq \frac{C_1}{C_3} \\ FO: &\quad \omega_0 = \frac{1}{\sqrt{C_1 C_2 R_1 R_2}} \end{aligned} \tag{4.21}$$

From the above equation (4.21), it may be observed that the proposed oscillator has non-interacting control of CO and FO i.e., CO can be independently adjusted through resistor R_3 (for $C_1 = C_3$) without affecting FO which may be independently varied through R_2.

This TOQSO circuit possesses two quadrature voltage outputs. The relationships between output voltages are given by:

$$\begin{aligned} \frac{V_{01}}{V_{02}} &= -\frac{1}{sC_3R_3} \quad or \quad \left|\frac{V_{01}}{V_{02}}\right| = \frac{1}{\omega C_3 R_3} \angle -j90^\circ \\ \frac{V_{03}}{V_{01}} &= -\frac{1}{sC_1R_1} \quad or \quad \left|\frac{V_{03}}{V_{01}}\right| = \frac{1}{\omega C_1 R_1} \angle -j90^\circ \end{aligned} \tag{4.22}$$

From equation (4.22), it may be noted that in this circuit, two different sets of quadrature voltages are availabe at low output impedance terminals of CFOAs.

4.3.2.2 Non-Ideal Analysis of the Oscillator Circuit presented in Fig. 4.12

In Fig. 4.13, we have redrawn the oscillator circuit shown in Fig. 4.12 by incorporating the various parasitic immittances present in all the CFOAs.

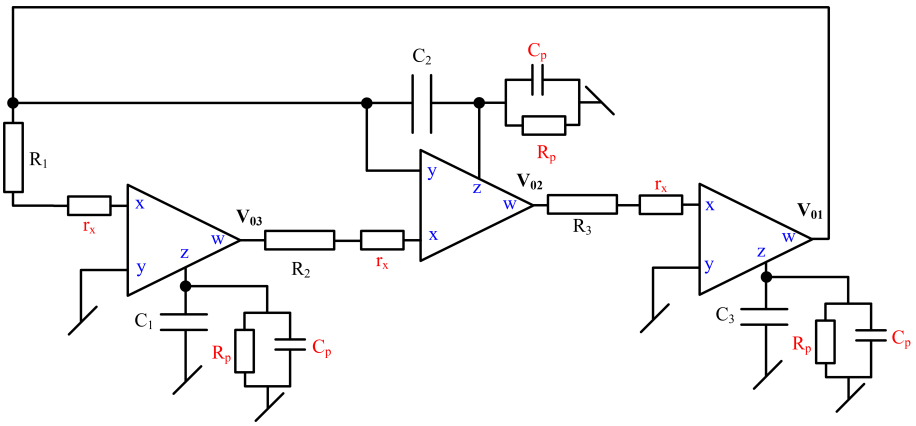


Figure 4.13: Second-order IHPF based TOQSO with parasitic

Routine circuit analysis of Fig. 4.13 yields the following expression for the nonideal FO as:

$$\omega_n^{/} = \omega_0 \sqrt{\frac{1 + \frac{R_1^{/} R_2^{/} R_3^{/}}{R_p^3}}{\left(1 + \frac{r_x}{R_1}\right)\left(1 + \frac{r_x}{R_2}\right)\left(1 + \frac{C_p}{C_1}\right)\left(\frac{R_3^{/}}{C_3 R_p}\left(C_2^{/} + C_3^{/} + \frac{C_2^{/} C_3^{/}}{C_1^{/}}\right) - 1\right)}} \tag{4.23}$$

where $R_i^{/} = R_i + r_x$, and $C_i^{/} = C_i + C_p$ (for i = 1 – 3)

To minimize the effect of parasitic on the oscillation frequency of the oscillator circuit, we may take the following assumptions:

$$C_i >> C_p,\ R_i >> r_x \text{ and } R_i << R_p \ (for\ i = 1-3)$$

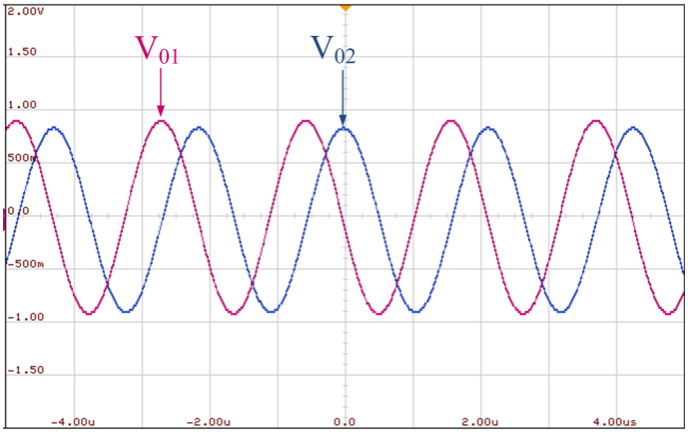
We have evaluated the non-ideal frequency of oscillation obtained from equation (4.23) where the values of parasitic resistances and capacitances taken earlier were used and found the value of FO equal to 482.340 kHz corresponding to the ideal frequency of 481.82 kHz. The error between ideal and non-ideal frequencies of the proposed oscillator is around 0.107% which shows that the effect of different non-

idealities of CFOAs, on the FO is not significant.

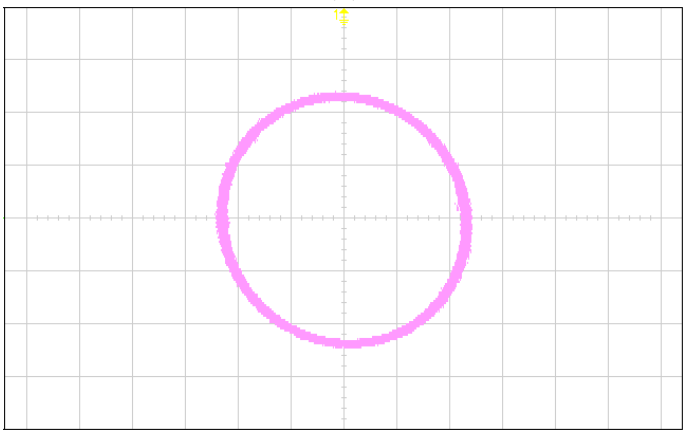
4.3.2.3 Experimental Results

For the experimental verification of the TOQSO, the circuit shown in Fig. 4.12 was bread-boarded using AD844 type CFOAs, 5% tolerance resistors and 10% tolerance capacitors. The D.C. power supply voltages $\pm V_{CC}$ were kept at $\pm 8V$.

The TOQSO circuit shown in Fig. 4.12 was designed for a nominal frequency of 481 kHz. The resistors and capacitors were chosen as: $R_1 = 2.2$ kΩ, $R_2 = 2.2$ kΩ, $R_3 = 0.3$ kΩ + 10 kΩ (pot), and $C_1 = C_2 = C_3 = 150$ pF. The experimentally measured FO was found to be 478.24 kHz with peak to peak output voltage levels (V_{01}, V_{02} and V_{03}) 1.827 V, 1.926 V and 1.744 V respectively. The experimentally obtained steady state response of output voltages, Lissajous pattern and frequency spectra of Fig. 4.12 have been displayed in Fig 4.14.



(a)



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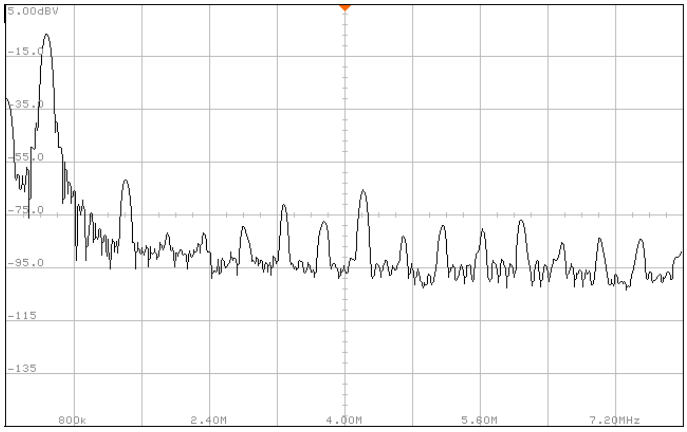

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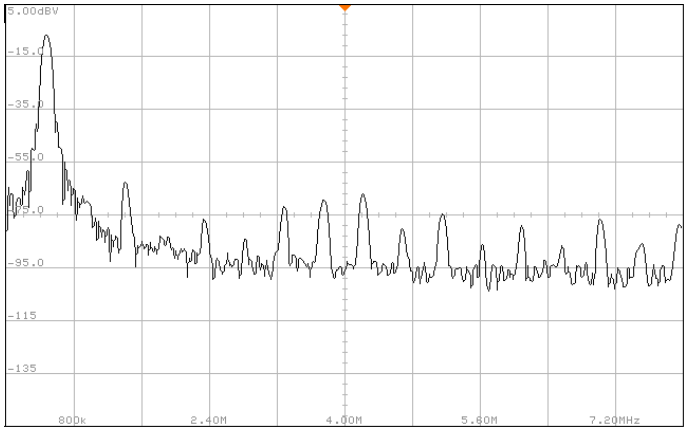
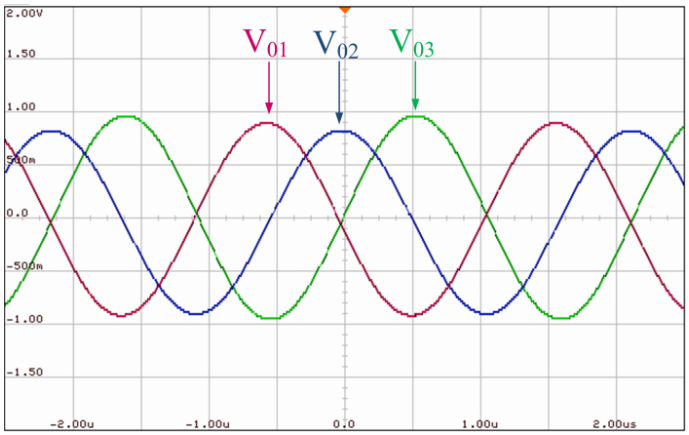


(d)



(e)

Figure 4.14: Experimental results of TOQSO shown in Fig. 4.12 (a) Transient voltage outputs (b) Lissajous pattern (X-Y plot) between V_{01} and V_{02} (c) Spectrum of V_{01} and (d) Spectrum of V_{02} (e) Transient output waveforms of three voltages

The experimentally obtained phase difference between V_{01} and V_{02} was found 92.792° while the phase difference between V_{01} and V_{03} was measured as 92.671° for the

designed frequency of 481 kHz, which are close to theoretical values (90°). The experimental %THD obtained for output voltages V_{01}, V_{02} and V_{03} are 0.23%, 0.24% and 0.24% respectively.

These experimental results, thus, validate the workability of the derived TOQSOs using proposed approaches.

4.4 Low Frequency Third Order Sinusoidal Oscillators with Grounded Capacitors[1]

Low frequency sinusoidal oscillators are useful in the context of bio-medical applications, instrumentation and measurement situations where they are utilized to measure the unknown capacitance, geophysical, or control applications [21]. In this section, we present, systematic realisation of third order low frequency sinusoidal oscillators employing CFOAs and grounded capacitors.

4.4.1 Design of Low Frequency Third Order Sinusoidal Oscillators

The general characteristic equation (CE) of a third order sinusoidal oscillator is given by:

$$a_3 s^3 + a_2 s^2 + a_1 s + a_0 = 0 \tag{4.24}$$

The roots of equation (4.24) must lie in the right half of s-plane for self-starting the oscillations, and, on $\pm j\omega$ axis for sustained oscillations. Using the Routh-Hurwitz's criterion, the CO and FO of equation (4.24) may, thus, be obtained as:

$$CO: \quad a_0 a_3 \geq a_1 a_2 \tag{4.25}$$

$$FO: \quad \omega = \sqrt{\frac{a_0}{a_2}} \ \ or \ \ \sqrt{\frac{a_1}{a_3}} \tag{4.26}$$

where $a_i \rightarrow (0-3)$ are constants, usually, expressed as sum/product or a combinations thereof of various resistors and capacitors used in the realization.

Equation (4.24) may lead to generate low frequency (LF) oscillations if the coefficients a_1 and a_0 in (4.24) are expressed as difference terms of the form: $a_1 = (b_3–b_2)$ and $a_0 = (b_1–b_0)$ resulting into the modified CE:

[1]The material presented in this section has been published in: Ajishek Raj, Pragati Kumar, and D. R. Bhaskar, "Systematic Realization of Low Frequency Third Order Sinusoidal Oscillators" International Journal of Circuit Theory and Applications, (2021).

$$a_3 s^3 + a_2 s^2 + (b_3 - b_2)s + (b_1 - b_0) = 0 \tag{4.27}$$

The modified CO and FO obtained from equation (4.27) are given by:

$$CO: \quad (b_1 - b_0)a_3 \geq (b_3 - b_2)a_2 \tag{4.28}$$

$$FO: \quad \omega = \sqrt{\frac{b_1 - b_0}{a_2}} \ \ or \ \ \sqrt{\frac{b_3 - b_2}{a_3}} \tag{4.29}$$

From equation (4.29), we may conclude that if b_1 is slightly greater than b_0 or b_3 is slightly greater than b_2, provided that equation (4.28) is satisfied, the circuit will produce very low frequency oscillations.

As we stated earlier that the coefficients of CEs of third order oscillator circuits given in equations (4.24) and (4.27) consist of combination of resistors and capacitors to realize these oscillators, the number of resistors and capacitors required to synthesize these oscillators is explained below.

To determine the minimum number of resistors and capacitors required to realize a low frequency third order sinusoidal oscillator (LFTOSO) in which the CO and FO can be controlled by independent resistors, let us consider the following type of tuning laws for FO and CO:

$$FO: \quad \omega_0 = \sqrt{\frac{1 - \frac{R_3 C_3}{R_4 C_1}}{C_2 C_3 R_2 R_3}} \ \ and \ \ CO: \quad R_1 C_1 - R_3 C_3 \ \leq \ 0 \tag{4.30}$$

It may be observed from these tuning laws that FO can be tuned by resistor R_4 without disturbing CO, which in turn, can be adjusted by R_1 without disturbing FO. Thus, it emerges that the minimum number of resistors and capacitors required for the realization of LFTOSO with independent control of CO and FO are four and three respectively.

To obtain the CE, as presented in equation (4.27), we start with a three port network 'N', represented by the short circuit admittance matrix Y_N, terminated with three grounded capacitors at the respective ports as shown in Fig. 4.15.

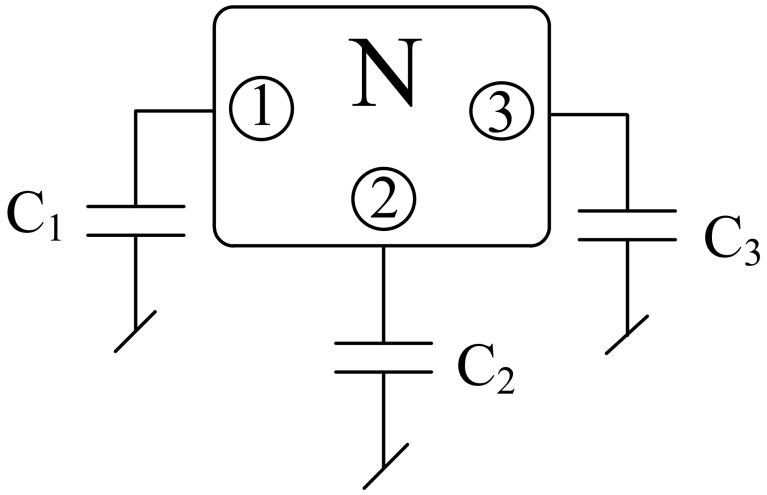


Figure 4.15: Generalized structure for the synthesis of third order oscillators

The short circuit admittance matrix of the capacitively terminated network 'N' may be expressed as:

$$[Y] = \begin{bmatrix} sC_1 + y_{11} & y_{12} & y_{13} \\ y_{21} & sC_2 + y_{22} & y_{23} \\ y_{31} & y_{32} & sC_3 + y_{33} \end{bmatrix}.$$

where $[y_{ij}]$ $(i, j \rightarrow 1\text{-}3)$ are the elements of short circuit admittance matrix of network 'N' given by:

$$[Y_N] = \begin{bmatrix} y_{11} & y_{12} & y_{13} \\ y_{21} & y_{22} & y_{23} \\ y_{31} & y_{32} & y_{33} \end{bmatrix}.$$

Using routine circuit analysis, the CE of the circuit shown in Fig. 4.15 can now be expressed as:

$$\begin{aligned} & s^3 C_1 C_2 C_3 + s^2 (C_2 C_3 y_{11} + C_1 C_3 y_{22} + C_1 C_2 y_{33}) \\ & + s(C_1 y_{22} y_{33} + C_2 y_{11} y_{33} + C_3 y_{11} y_{22} - C_1 y_{23} y_{32} - C_2 y_{13} y_{31} - C_3 y_{12} y_{21}) \\ & + (y_{11} y_{22} y_{33} + y_{13} y_{21} y_{32} + y_{12} y_{23} y_{31} - y_{11} y_{23} y_{32} - y_{13} y_{22} y_{31} - y_{12} y_{21} y_{33} +) = 0 \end{aligned} \tag{4.31}$$

From equation (4.31), following points may be noted for the realization of low frequency third order sinusoidal oscillator:

(i) For the design of third order oscillator, at least one out of the three principal diagonal elements, namely, y_{ii} $(i \rightarrow 1 - 3)$ must be non-zero, failing which, CE will not remain a third order CE

(ii) Under the condition of only a single non-zero principal diagonal element $y_{ii} \neq 0$ $(i \rightarrow 1 - 3)$, if a difference term is to exist in the constant term of equation (4.31), then the off diagonal elements $y_{jk} \neq 0$ $(j, k \rightarrow 1 - 3,\ j \neq i, k \neq i)$ corresponding to the non- diagonal element y_{ii} should not be zero.

(iii) Under the condition of only a single non-zero principal diagonal element $y_{ii} \neq 0$ $(i \rightarrow 1 - 3)$, if a difference term is to exist in the coefficient of 's' then the two off diagonal pair sets (y_{jk}, y_{kj}), for $(j, k \rightarrow 1 - 3\ ,\ j \neq k)$ must be non-zero, failing which, the coefficient of 's' will become zero. This can be achieved by having at least three non-zero elements out of the four elements present in the two off diagonal element pair sets.

(iv) Also, under the condition of only a single non-zero principal diagonal element, in the off-diagonal element sets, $y_{12} - y_{21},\ y_{13} - y_{31},\ y_{23} - y_{32}$, in one set, the sign of y_{ij} must be opposite to the sign of y_{ji} $(i \rightarrow 1 - 3), j \rightarrow 1 - 3$ and $k \rightarrow 1 - 3$), failing which, there will not be any difference term in the coefficient of 's', an essential condition if equation (4.31) is to represent the CE of an LFO.

From the above discussion, it thus, emerges that at least six non-zero elements must be present in the short circuit admittance matrix Y_N of the three port network 'N' for generation of low frequency oscillations.

Considering all four points discussed above, twelve different matrices have been obtained which may lead to sustained LF oscillations using four resistors and three grounded capacitors, which is the minimum requirement for independent control of

CO and FO. These short circuit admittance matrices are given below:

$$[Y_{1a}] = \begin{bmatrix} -G_1 & -G_4 & G_4 \\ G_2 & 0 & -G_2 \\ 0 & -G_3 & 0 \end{bmatrix} [Y_{1b}] = \begin{bmatrix} -G_1 & G_4 & -G_4 \\ 0 & 0 & -G_3 \\ G_2 & -G_2 & 0 \end{bmatrix} [Y_{1c}] = \begin{bmatrix} 0 & 0 & -G_3 \\ G_4 & -G_1 & -G_4 \\ -G_2 & G_2 & 0 \end{bmatrix}$$

$$[Y_{2a}] = \begin{bmatrix} 0 & G_3 & -G_3 \\ -G_2 & 0 & 0 \\ -G_4 & G_4 & -G_1 \end{bmatrix} [Y_{2b}] = \begin{bmatrix} 0 & -G_3 & G_3 \\ -G_4 & -G_1 & G_4 \\ -G_2 & 0 & 0 \end{bmatrix} [Y_{2c}] = \begin{bmatrix} 0 & -G_2 & 0 \\ G_3 & 0 & -G_3 \\ G_4 & -G_4 & -G_1 \end{bmatrix}$$

$$[Y_{3a}] = \begin{bmatrix} -G_1 & 0 & G_4 \\ -G_2 & 0 & G_2 \\ -G_3 & G_3 & 0 \end{bmatrix} [Y_{3b}] = \begin{bmatrix} -G_1 & G_4 & 0 \\ -G_3 & 0 & G_3 \\ -G_2 & G_2 & 0 \end{bmatrix} [Y_{3c}] = \begin{bmatrix} 0 & G_3 & -G_3 \\ G_2 & 0 & -G_2 \\ G_4 & 0 & -G_1 \end{bmatrix}$$

$$[Y_{4a}] = \begin{bmatrix} 0 & G_3 & -G_3 \\ -G_2 & 0 & G_2 \\ 0 & G_4 & -G_1 \end{bmatrix} [Y_{4b}] = \begin{bmatrix} 0 & G_2 & -G_2 \\ -G_4 & -G_1 & 0 \\ G_3 & -G_3 & 0 \end{bmatrix} [Y_{4c}] = \begin{bmatrix} 0 & -G_3 & G_3 \\ 0 & -G_1 & G_4 \\ -G_2 & G_2 & 0 \end{bmatrix}$$

where $G_i = \frac{1}{R_i}$ $(i \rightarrow 1-4)$

A careful perusal of Y_{1a}–Y_{1c}, Y_{2a}–Y_{2c}, Y_{3a}–Y_{3c}, and Y_{4a}–Y_{4c} reveals that these four sets of three matrices each will lead to the same CE because they are related to each other by row and column transformations.

4.4.2 Low Frequency Oscillators With Independent Control of CO and FO Using CFOAs

It is observed from the short circuit admittance matrices given in section 4.4.1 that the realization of a TOLFSOs with independent control of CO and FO using any one of the twelve three-ports represented by their Y-matrices, requires four resistors and three capacitors along with the three port which can be realized using different active building blocks like CFOAs, operational transconductance amplifiers, etc. CFOA, because of its very versatile architecture, which contains a translinear implementation of second-generation current conveyor (CCII+), whose output terminal is buffered to create a low impedance output terminal, has received prominent attention in the implementation of analog signal processing and generation circuits. The performance of CFOA-based circuits, unlike the conventional op-amp-based circuits, is not limited by very low value of slew rate and gain bandwidth conflict. In addition, the low output impedance enables easy cascadability of the output, a desirable feature in many circuits. In the present work CFOAs have been employed as the active elements because the performance of the operational transconductance amplifier-based circuits is limited by the very small linear range of input voltage in which its transconductance remains constant.

It may be pointed out that out of the twelve matrices derived, only four distinct LF oscillator configurations have been obtained using CFOAs, as only four of these matrices have different structures. The resulting TOLFSO circuits derived from the matrices Y_{1a} – Y_{1c}, Y_{2a} – Y_{2c}, Y_{3a} – Y_{3c}, and Y_{4a} – Y_{4c} are shown in Fig. 4.16a – Fig. 4.16d respectively.

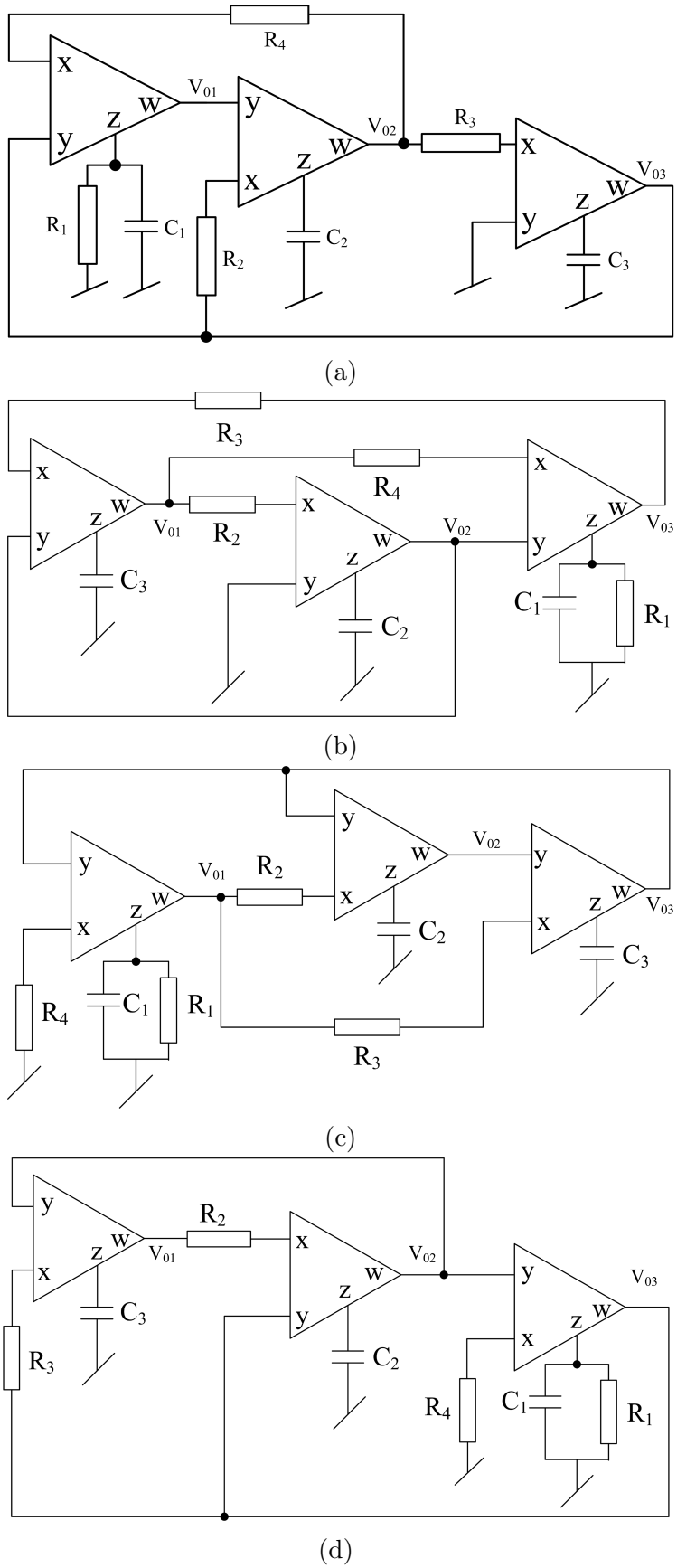


Figure 4.16: Proposed very low frequency third order sinusoidal oscillators

Assuming ideal CFOAs, a routine circuit analysis of Fig. 4.16 provides the CE with corrosponding COs and FOs of the derived LF oscillators as:

$$Fig.4.16a: \quad s^3C_1C_2C_3 + s^2C_2C_3G_1 + sG_2(C_3G_4 - C_1G_3) + G_2G_3(G_4 - G_1) = 0$$

$$CO: \quad R_1 \leq R_3\left(\frac{C_3}{C_1}\right) \quad FO: \quad \omega_1 = \sqrt{\frac{\frac{R_3}{R_4}\left(\frac{C_3}{C_1}\right) - 1}{C_2C_3R_2R_3}} \quad for\ R_4C_1 < R_3C_3 \tag{4.32}$$

$$Fig.4.16b: \quad s^3C_1C_2C_3 + s^2C_2C_3G_1 + sG_3(C_1G_2 - C_2G_4) + G_2G_3(G_1 - G_4) = 0$$

$$CO: \quad R_1 \leq R_2\left(\frac{C_2}{C_1}\right) \quad FO: \quad \omega_2 = \sqrt{\frac{1 - \frac{R_2}{R_4}\left(\frac{C_2}{C_1}\right)}{C_2C_3R_2R_3}} \quad for\ R_4C_1 > R_2C_2 \tag{4.33}$$

$$Fig.4.16c: \quad s^3C_1C_2C_3 + s^2C_2C_3G_1 + sG_3(C_2G_4 - C_1G_2) + G_2G_3(G_4 - G_1) = 0$$

$$CO: \quad R_1 \leq R_2\left(\frac{C_2}{C_1}\right) \quad FO: \quad \omega_3 = \sqrt{\frac{\frac{R_2}{R_4}\left(\frac{C_2}{C_1}\right) - 1}{C_2C_3R_2R_3}} \quad for\ R_4C_1 < R_2C_2 \tag{4.34}$$

$$Fig.4.16d: \quad s^3C_1C_2C_3 + s^2C_2C_3G_1 + sG_2(C_1G_3 - C_3G_4) + G_2G_3(G_1 - G_4) = 0$$

$$CO: \quad R_1 \leq R_3\left(\frac{C_3}{C_1}\right) \quad FO: \quad \omega_4 = \sqrt{\frac{1 - \frac{R_3}{R_4}\left(\frac{C_3}{C_1}\right)}{C_2C_3R_2R_3}} \quad for\ R_4C_1 > R_3C_3 \tag{4.35}$$

From equations (4.32) - (4.35), we can conclude that all the proposed third order LF sinusoidal oscillators have independent control of CO and FO. CO can be independently adjusted through resistor R_1 and FO can be varied independently through resistor R_4. The FO may also be varied independently through R_2 in case of Fig. (4.16a) and (4.16d) while for Fig. (4.16b) and (4.16c), FO can be tuned through resistor R_3 too!

It may also be noted that in the oscillator circuits shown in Fig. 4.16a and Fig. 4.16b, quadrature output voltages are also available for which relationships are given as:

$$Fig.4.16a: \quad \frac{V_{03}(s)}{V_{02}(s)} = \frac{-1}{sC_3R_3}$$

$$Fig.4.16b: \quad \frac{V_{02}(s)}{V_{01}(s)} = \frac{-1}{sC_2R_2}$$

4.4.3 Effect of Non-Idealities on LF Oscillators

The parasitic resistances and capacitances associated with various terminals of CFOAs affect the performance of the oscillators. We have considered the parasitic resistance r_x at terminal-X and a parallel combination of resistance and capacitance $(R_P||\frac{1}{sC_P})$ at terminal-Z (neglecting the output resistance at terminal W). For the circuits shown in Fig. 4.16, it may be observed that the resistors R_2, R_3, and R_4 will absorb $r_{xi}(i \rightarrow 2-3)$. Furthermore, the external resistance R_1 will absorb R_P. Similarly, all the three external grounded capacitors will absorb parasitic capacitances C_P. The non-ideal expressions for FO $(\omega_{ni}, i \rightarrow 1-4)$ of the LFO circuits shown in Fig. 4.16 are given as:

$$\omega_{n1} = \sqrt{\omega_1^2 + \frac{1}{R_P^2 C_1 C_2 C_3}\left(C_1 + (C_2 + C_3)\left(1 + \frac{R_1}{R_P}\right)\right)}$$

$$\omega_{n2} = \sqrt{\omega_2^2 + \frac{1}{R_P^2 C_1 C_2 C_3}\left(C_1 + (C_2 + C_3)\left(1 + \frac{R_1}{R_P}\right)\right)}$$

$$\omega_{n3} = \sqrt{\omega_3^2 + \frac{1}{R_P^2 C_1 C_2 C_3}\left(C_1 + (C_2 + C_3)\left(1 + \frac{R_1}{R_P}\right)\right)}$$

$$\omega_{n4} = \sqrt{\omega_4^2 + \frac{1}{R_P^2 C_1 C_2 C_3}\left(C_1 + (C_2 + C_3)\left(1 + \frac{R_1}{R_P}\right)\right)}$$

The percentage error between ideal and nonideal FO for all the circuits presented in Fig. 4.16 have been calculated assuming $r_x = 50\ \Omega$, $R_p = 3\ \text{M}\Omega$, $C_p = 4.5$ pF (the external resistors and capacitors were predistorted to absorb r_x and C_P as explained earlier). These errors are found to be below 0.445%, which are very low.

4.4.3.1 Sensitivity Analysis

The FO of the proposed oscillators deviate from the predicted values obtained by theory due to the component tolerances, thermal drift and component aging. Therefore, we have evaluated the sensitivity of FO with respect to component tolerances using the classical formula of sensitivity given as:

$$S_X^{\omega} = \left(\frac{X}{\omega}\right)\frac{\partial \omega}{\partial X} \tag{4.36}$$

where X is the parameter of interest.

The sensitivities of the proposed oscillator circuits shown in Fig. 4.16 have been tabulated in Table 4.1.

Table 4.1: Sensitivity of ω with respect to passive components

Circuits	S_X^{ω}		
Fig. 4.16a	$S_{R2}^{\omega} = S_{C2}^{\omega}$ = -0.5,	$S_{R_3}^{\omega} = S_{C_3}^{\omega} = \frac{1}{2(k_1-1)}$,	$S_{R_4}^{\omega} = S_{C_1}^{\omega} = \frac{-k_1}{2(k_1-1)}$
Fig. 4.16b	$S_{R_3}^{\omega} = S_{C_1}^{\omega}$ = -0.5,	$S_{R_2}^{\omega} = S_{C_2}^{\omega} = \frac{1}{2(k_2-1)}$,	$S_{R_4}^{\omega} = S_{C_3}^{\omega} = \frac{-k_2}{2(k_2-1)}$
Fig. 4.16c	$S_{R_3}^{\omega} = S_{C_2}^{\omega}$ = -0.5,	$S_{R_2}^{\omega} = S_{C_3}^{\omega} = \frac{1}{2(k_3-1)}$,	$S_{R_4}^{\omega} = S_{C_1}^{\omega} = \frac{-k_3}{2(k_3-1)}$
Fig. 4.16d	$S_{R_2}^{\omega} = S_{C_2}^{\omega}$ = -0.5,	$S_{R_3}^{\omega} = S_{C_3}^{\omega} = \frac{1}{2(k_4-1)}$,	$S_{R_4}^{\omega} = S_{C_1}^{\omega} = \frac{-k_4}{2(k_4-1)}$

where $k_1 = k_4 = \frac{R_3C_3}{R_4C_1}$, $k_2 = \frac{R_2C_2}{R_4C_3}$ and $k_3 = \frac{R_2C_3}{R_4C_1}$

From Table 4.1, it may be noted that the value of sensitivity of FO with respect to different passive components can be kept below unity by appropriately selecting the values of k_1, k_2, k_3 and k_4.

4.4.3.2 Frequency Stability

A higher value of frequency stability factor implies smaller change in the frequency of oscillation because of changes in the operating conditions in the circuit. To compare the proposed LF oscillator circuits between themselves, we have evaluated the frequency stability of each circuit using the formula $S^F = \frac{\partial \phi(u)}{\partial u}$, where $u = \frac{\omega}{\omega_0}$ and $\phi(u)$ is the phase of open loop transfer function of oscillator circuit [21]. The evaluated S^F of the presented LFO circuits are tabulated in Table 4.2.

Table 4.2: Frequency stability factors of the proposed low frequency sinusoidal oscillators

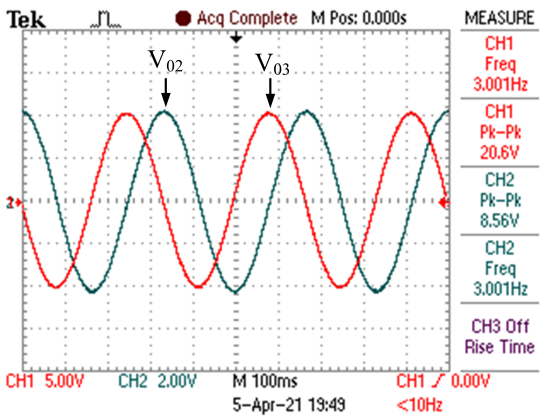
Circuits	S^F
Fig. 4.16a	$S^F = -2\sqrt{n-1} \approx -2\sqrt{n}$, for n ¿¿1
Fig. 4.16b	$S^F = \frac{-2n\sqrt{1-n}}{2-n} \approx -n$, for n ¡¡1
Fig. 4.16c	$S^F = -2\sqrt{n-1} \approx -2\sqrt{n}$, for n ¿¿1
Fig. 4.16d	$S^F = \frac{-2\sqrt{1-n}}{n} \approx \frac{-2}{n}$, for n ¡¡1

where $R_1 = R_2 = R_3 = R$, $C_1 = C_2 = C_3 = C$, and $R_4 = \frac{R}{n}$.

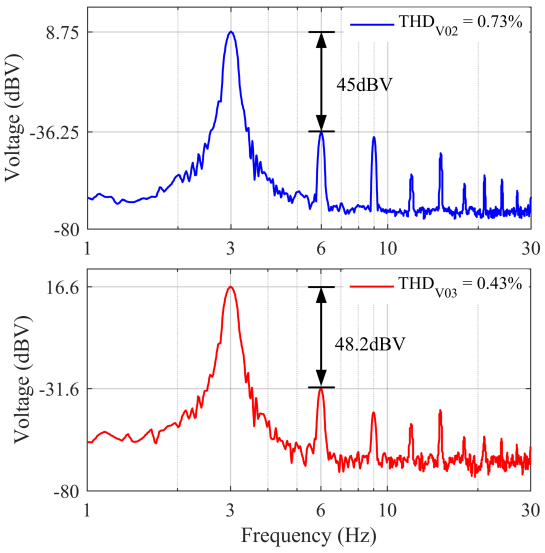
From Table 4.2, it may be observed that the LF oscillator circuits presented in Fig. 4.16a and Fig. 4.16c have higher values of S^F if 'n' is selected appropriately as indicated in Table 4.2.

4.4.4 Experimental Results

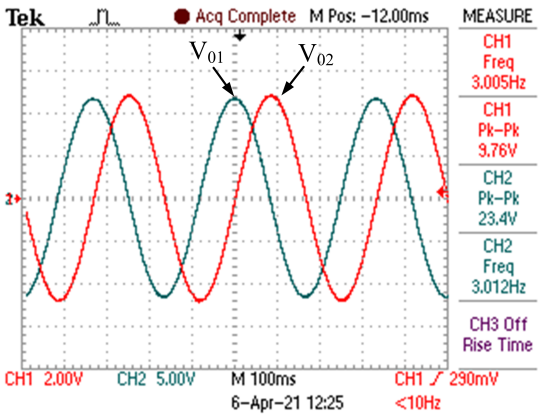
For establishing the workability of all the new LF oscillator circuits of Fig. 4.16 were bread boarded for experimental verification using off-the-shelf ICs AD844 CFOAs. The power supply voltages used to bias CFOAs were taken as ± 15V DC. The circuits were designed for a nominal frequency of 3.03 Hz. The passive components used were $R_2 = R_3 = 100$ kΩ, $R_4 = 87.3$ kΩ (for Fig. 4.16a) and 117 kΩ (for Fig. 4.16b) with identical capacitors $C_1 = C_2 = C_3 = 200$ nF (5% tolerance). The CO was controlled through resistor $R_1 = (47\ \text{k}\Omega + 100\ \text{k}\Omega$ pot). The quadrature output voltages and frequency spectrum for the circuits shown in Fig. 4.16a and Fig. 4.16b have been depicted in Fig. 4.17.



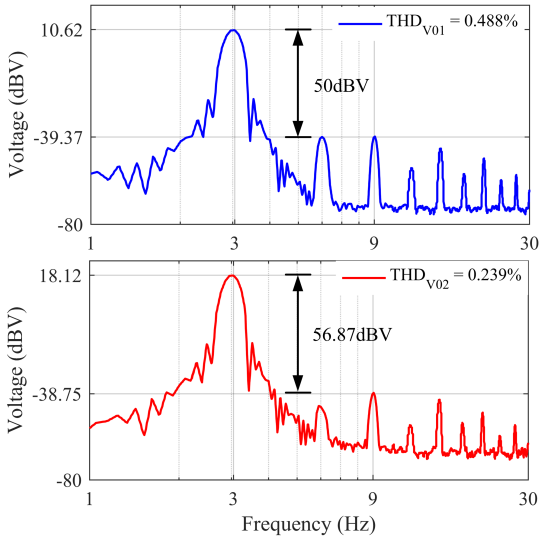
(a)



(b)



(c)

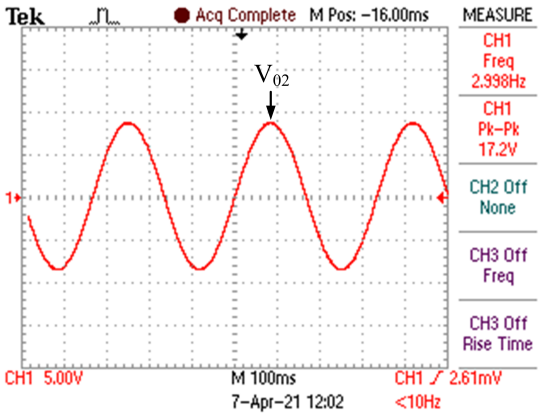


(d)

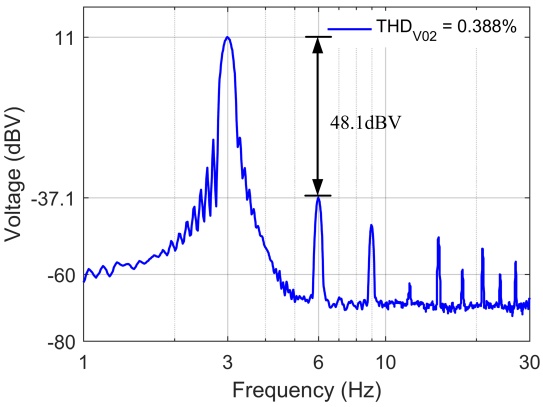
Figure 4.17: Experimental quadrature voltage waveforms and frequency spectrum of circuits of Fig. 4.16a and Fig. 4.16b

The measured frequency of oscillation for the circuits of Fig. 4.16a and Fig. 4.16b are found to be 3.001 Hz, and 3.005 Hz respectively. The percentage total harmonic distortions (%THD) of the output quadrature voltages (V_{01}, V_{02}) were also recorded experimentally and found to be low as (0.73%, 0.43%) and (0.488%, 0.239%) respectively for Fig. 4.16a and Fig. 4.16b.

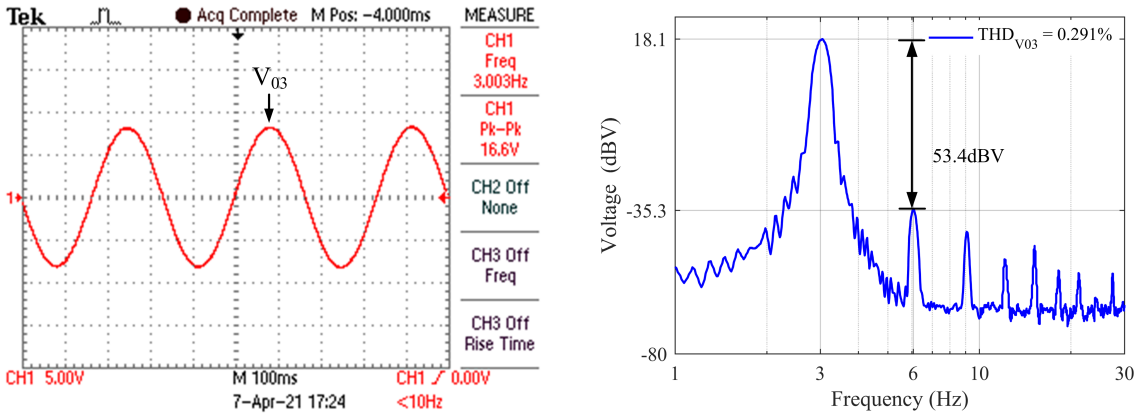
The same component values which were used in Fig. 4.16a and Fig. 4.16b have been taken to verify circuits shown in Fig. 4.16c and Fig. 4.16d respectively. The experimental voltage waveforms and frequency spectrum have been displayed in Fig. 4.18.



(a)



(b)



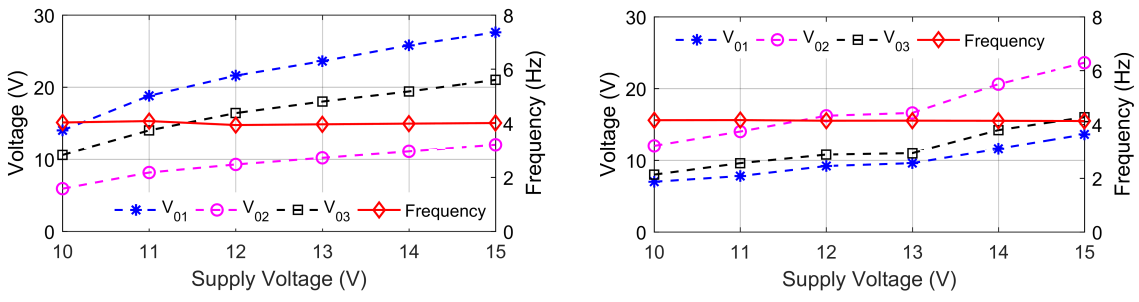
(c) (d)

Figure 4.18: Experimental transient voltage waveforms and frequency spectrum of circuits of Fig. 4.16c and Fig. 4.16d

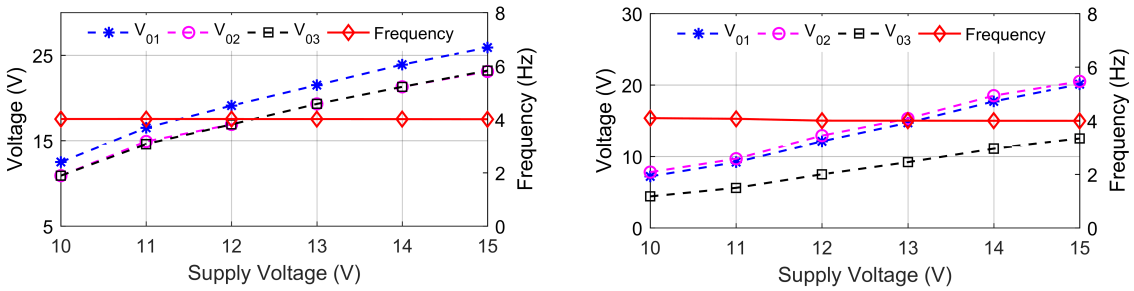
The measured frequency of oscillation for the circuits of Fig. 4.16c and Fig. 4.16d are found to be 2.998 Hz, and 3.003 Hz respectively. The percentage total harmonic distortions (%THD) of the output voltages V_{02} of Fig. 4.16c and V_{03} of Fig. 4.16c were also recorded experimentally and found to be low as 0.388% and 0.291%.

4.4.4.1 Sensitivity of FO with Power Supply Voltages

To determine the sensitivity of the FO with respect to power supply variations, we have performed simulations and verified the observations experimentally also. To analyse the behaviour of FO with respect to power supply voltages, we have varied the power supply voltages in the range of ± 10V to ± 15V and recorded the readings of FO, and the output voltages of CFOAs. The variation of FO, and amplitude of the output voltages with power supply for all the oscillator circuits are shown in Fig. 4.19.



(a) (b)



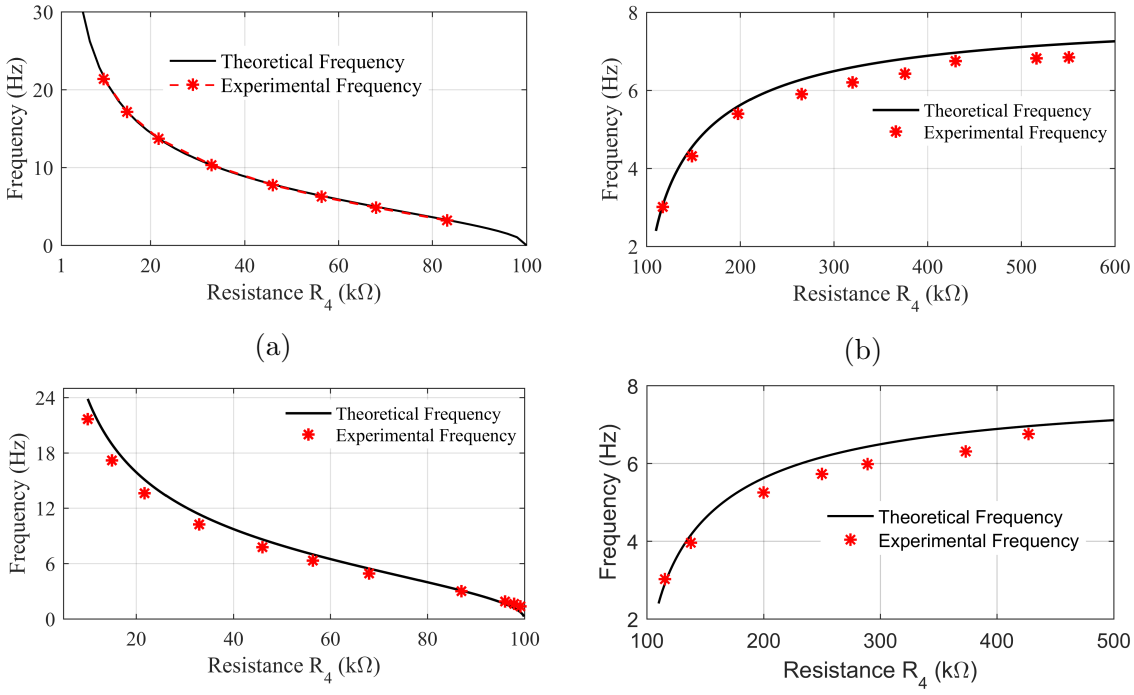
(c) (d)

Figure 4.19: Variation in the output voltages with power supply voltages (a) Fig. 4.16a (b) Fig. 4.16b (c) Fig. 4.16c and (d) Fig. 4.16d

From Fig. 4.19, it has been found that the FO remains almost constant with respect to power supply voltage variations while the voltage obtained at the output terminals of CFOAs, linearly increases when the power supply voltage increases.

4.4.4.2 Tunability of FO of Proposed LF Oscillators

We have also varied the oscillation frequency of all the proposed LF oscillator circuits as shown in Fig. 4.16 by varying the resistor R_4. Fig. 4.20 demonstrates the frequency variation of all the proposed LF oscillator circuits.



(a) (b)

(c) (d)

Figure 4.20: Variation of frequency with resistance R_4 of Fig. 4.16a–Fig. 4.16d

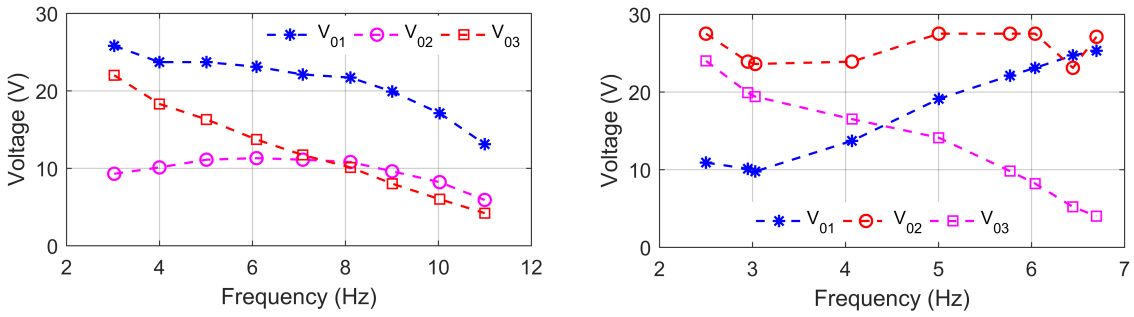
From Fig. 4.20, it may be noted that the experimental value of oscillation frequencies for all the presented LF oscillators are very close to the theoretical values with a maximum frequency error of approximetly 5%.

4.4.4.3 Amplitude Limitation Mechanism of the Proposed LF Oscillators

In the oscillator circuits derived from the proposed approach, no external amplitude gain control mechanism has been employed. The saturation characteristics of the CFOAs limit the output voltage. To identify the amplifier(s) responsible for amplitude limitation in each oscillator circuit presented in Fig. 4.16, we have performed additional experimental work as described below.

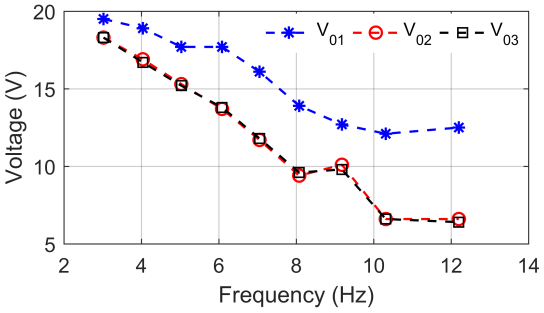
The different output voltages (available at the output of the respective CFOA), were measured while the FO was varied between 3 Hz to 11 Hz for Fig. 4.16a and Fig. 4.16c, and 3 Hz to 7 Hz for Fig. 4.16b and Fig. 4.16d by varying the frequency tuning resistor R_4. The graphs plotted between output voltages and frequency of the presented LF oscillator circuits have been displayed in Fig. 4.21.

From the observed readings, for each circuit, the CFOA, for which the output voltage was rising at a higher rate was identified. The corrosponding CFOA, thus limits the output voltage in each circuit. In Fig. 4.21, we have shown the variation of the amplitude of the output voltages (V_{01}, V_{02} and V_{03}) with respect to frequency.

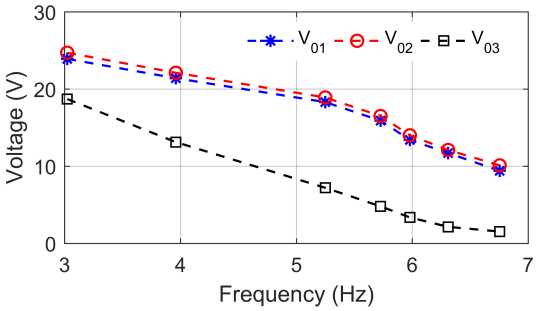


(a) (b)

From Fig. 4.21a - Fig. 4.21d, it is thus, noted that for the oscillator circuits shown in Fig. 4.16a, Fig. 4.16b, Fig. 4.16c and Fig. 4.16d, the output voltage



(c)



(d)

Figure 4.21: Variation of output voltages of CFOAs with FO (a) Fig. 4.16a (b) Fig. 4.16b (c) Fig. 4.16c and (d) Fig. 4.16d

amplitudes are limited by $CFOA_1$, $CFOA_2$, $CFOA_1$ and $CFOA_2$ respectively.

4.5 Concluding Remarks

In this chapter, after classifying the realization methodologies of the previously proposed third order sinusoidal oscillator circuits, we have proposed three new approaches for systematic realization of third order sinusoidal oscillators (including minimal realization of low frequency third order sinusoidal oscillators). Two of the proposed approaches are based on the use of inverse filters while the third approach is network synthetic in nature.

The first approach using inverse filters, uses a first order inverse HPF in cascade with a conventional lossy and lossless integrator in a unity feedback loop to synthesize TOQSO circuit while, in the second approach, second order inverse HPF in cascade with a conventional lossless integrator in a unity feedback loop has been used. The realized circuits have independent control of CO and FO. Exemplary implementations of TOQSOs based on both the approaches using CFOAs have been presented.

The network synthetic approach, on the other hand, is based on determination of the short-circuit admittance matrix of an autonomous three-port, whose characteristic equation represents the characteristic equation of a low frequency

third order sinusoidal oscillator with independent control of CO and FO. Twelve matrices, out of which four matrices are distinct, have been derived using which third order low frequency sinusoidal oscillator circuits having independent control of CO and FO with different resistors can be realized employing canonic number of resistors (04) and grounded capacitors (03). Minimal realizations of low frequency third order sinusoidal oscillators employing three CFOAs, four resistors and three grounded capacitors have been presented to verify the theoretical propositions. Two of the proposed structures have quadrature relationship between output voltages. These low frequency sinusoidal oscillators may be useful in biomedical signal processing/generation circuits. To establish the workability of all the proposed oscillator circuits, experimental results using off-the-shelf commercially available IC AD844 type CFOAs have been presented

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Chapter 5

Non-Linear Analog Circuits Using OTA and CFOA

5.1 Introduction

In the preceeding chapters, we have proposed several new circuits of analog active filters and sinusoidal oscillators using OTAs and CFOAs. We now present novel configurations of VM analog divider and square root circuits employing a single OTA and MOSFETs. We have also proposed a novel structure of analog multiplier/divider circuit using a single CFOA and four MOSFETs in VM.

In the following, we present a detailed account of the various analog divider circuits, square root circuits and analog multiplier circuits realized with different ABBs so that the proposed works are put in proper perspective.

Analog multipliers/dividers have a wide range of applications in analog signal processing, telecommunications, and electronic systems [1], A/D-D/A converters, peak detectors, phase detectors, synthesizers as well as in analog computational systems based on biological 'neural' paradigms [2, 3]. Analog divider circuit designs using numerous active building blocks (ABBs) have received wide attention. Various

researchers have proposed CM [4–17] and VM [18–25] analog divider circuits in the past using a variety of ABBs such as OTAs [4–6, 18, 19], current-controlled current conveyors (CCCII) [8], current controlled current differencing buffered amplifier (CCCDBA) [9], current differencing transconductance amplifiers (CDTA) [10, 11], current-controlled current differencing transconductance amplifiers (CCCDTA) [12], current amplifier (CA) [13], second-generation current conveyors (CCII) [14, 15, 20, 21], multiple output current-controlled current through transconductance amplifier (MO-CCCTTA) [16], current follower transconductance amplifier (CFTA) [17], current feedback operational amplifiers (CFOA) [22, 23], operational amplifiers [24] and operational transresistance amplifier (OTRA) [25]. Several circuit implementations of both analog multiplier and dividers together [4–6, 8–22, 26–34] and in addition, only analog multipliers [33, 35–39] using different ABBs have also been reported in the literature.

Square root circuits [40–49], on the other hand, are useful in measurement and instrumentation for the linearization of a signal from a differential pressure flow meter, or to calculate the root mean square value of an arbitrary waveform [1]. Geometric mean of two signals can also be found employing square root circuits. As the proposed research work deals with the realization of analog multipliers, dividers and square-root circuits in VM, in the following, we present a brief description of VM analog multipliers, dividers and square-root circuits realized with various ABBs.

In [**18**], **Sinencio, Angulo, Barranco** and **Vazquez** reported a number of nonlinear function generation circuits using OTAs in which analog multiplier, divider, squaring, square rooter and exponential blocks have been presented. The reported analog multiplier and divider circuits have four quadrant and two quadrant mode of operations respectively.

In [**19**], an analog multiplier using four OTAs and one resistor was reported by **Bhanja** and **Ray** which is shown in Fig. 5.1. Using this analog mutiplier along

with two OTAs and two resistors, an analog divider circuit has also been presented.

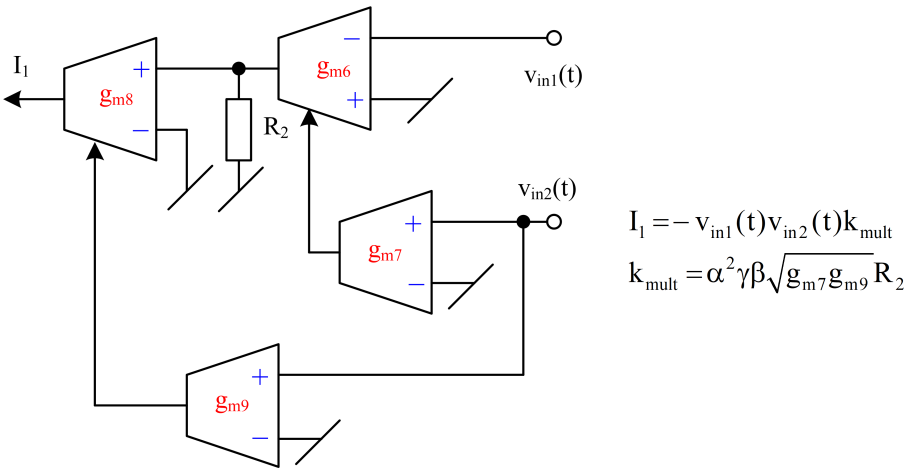


Figure 5.1: Analog multiplier reported by Bhanja and Ray [19]

In [**20**], **Hwang, Liu, Tu** and **Chen** reported an analog multiplier and divider circuit employing a multiplication mode current conveyor (MMCC). The presented analog multiplier has four quadrant mode of operations. For the implementation of analog divider, a CCII and two resistors along with MMCC have been used.

Liu, Wu Tsao, Wu and **Tsay** reported an integrable analog divider circuit in [**21**] using a voltage to current converter realized with a CCII and four MOSFETs (biased in the non-saturation region) and a multiplier circuit constructed with two CCIIs along with two MOSFETs (biased in non-saturation region).

CFOA-based differential multiplier and divider circuit has been presented in [**22**] by **Bajaj** and **Govil**. The circuit employs five CFOAs, six matched MOS transistors (biased in the triode region), and four identical capacitors.

In [**23**], CFOA-based analog divider (shown in Fig. 5.2) was proposed by **Liu** and **Chen** which employs two CFOAs and four MOSFETs (operated in the triode region). The circuit did not employ any passive components and thus, could be integrated easily.

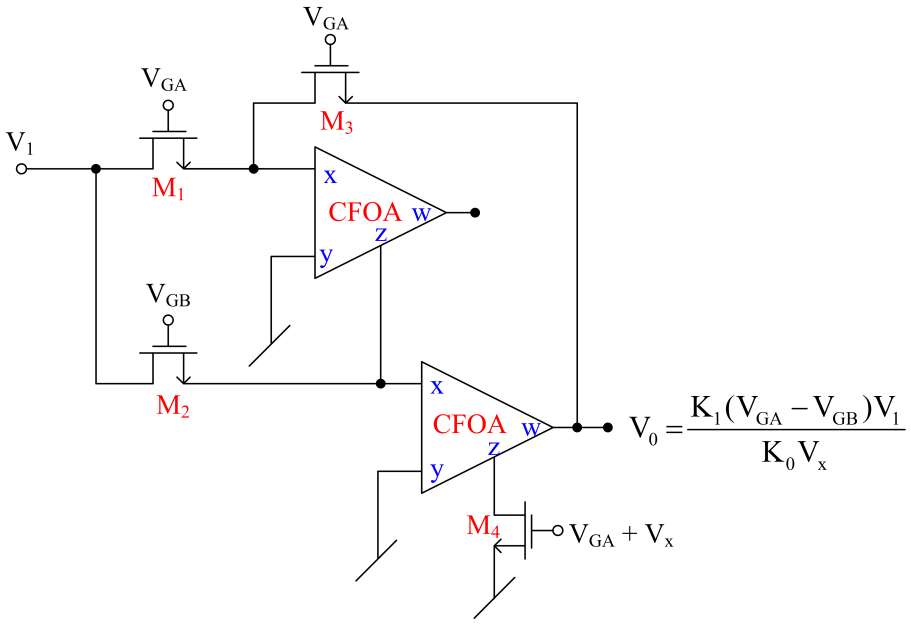


Figure 5.2: Analog multiplier reported by Liu and Chen [23]

An analog divider using voltage variable resistance property of MOSFET was proposed in [**24**] by **Ghosh** and **Patranabis**. The authors presented three analog divider circuits in which, the first two circuits employed two op-amps, six resistors and one field effect transistor (FET) while the third circuit required three op-amps along with six resistors and two FETs.

In [**25**], an OTRA-based analog divider circuit was presented by **Nagar** and **Paul** employing a single OTRA and four matched MOSFETs (operated in the triode region). The reported circuit has two quadrant modes of operations.

A single OTRA and six MOSFETs based multiplier/divider circuit has been reported in [**28**] by **Chadha** and **Arora**. The reported circuit has been shown in Fig. 5.3. The presented circuit has four quadrant mode of operation in multiplier mode and two quadrant mode of operation in division mode.

In [**29**], **Arora** and **Sharma** proposed a four quadrant multiplier and two quadrant divider circuit employing two third generation current conveyors, six MOSFETs and one buffer. Applications of the multiplier and divider circuits have been used to realize amplitude modulation, squarer and finally the novel cubic function generator.

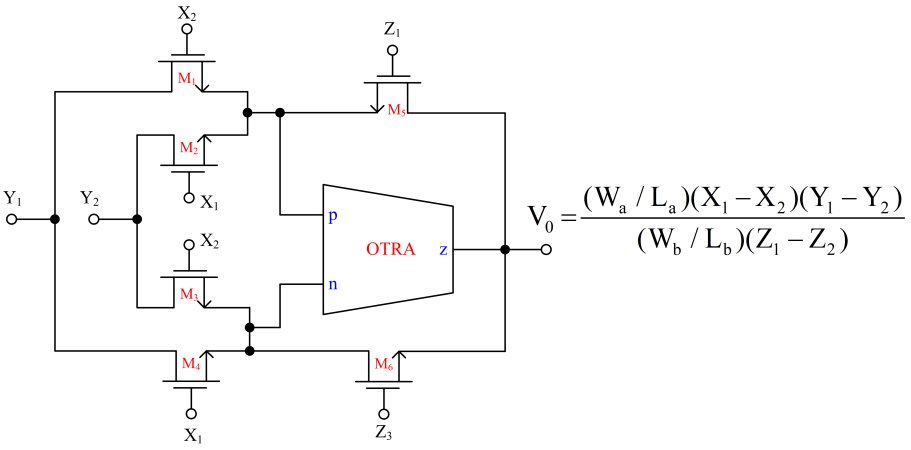


Figure 5.3: Analog multiplier reported by Chadha and Arora [28]

A single CDBA and seven MOSFETs based multiplier/divider circuit has been presented by **Pathak, Singh** and **Senani** in [**31**]. The presented circuit has four quadrant mode of operations in multiplication mode and it has a BW of around 83.2 MHz.

In [**33**], two multiplier/divider circuits based on single CDBA along with four MOSFETs have been presented by **Roy, Paul, Maiti** and **Pal**, out of which, one of the circuit has been displayed in Fig. 5.4. The reported circuit have a BW of 59 MHz.

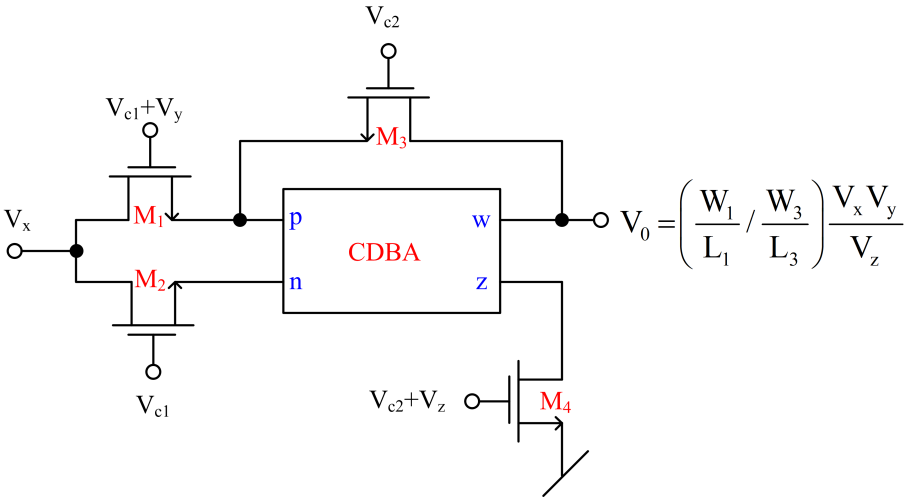


Figure 5.4: Analog multiplier reported by Roy, Paul, Maiti and Pal [33]

In [**35**], **Roy, Paul** and **Pal** reported a four quadrant analog multiplier circuit which

employs three op-amps, six resistors and two MOSFETs. The applications of the multiplier as a squarer, an amplitude modulator and a frequency doubler have also been presented.

A VM multiplier employing five op-amps and ten resistors has been presented in [**36**] by **Riewruja** and **Rerkratn**. The realization of multiplier is based on the quarter-square technique, which utilises the inherent square-law characteristic of class-AB output stage of the op-amp. The reported VM multiplier has four quadrant operation. The performance analysis in terms of error in the multiplier, high frequency response have also been discussed.

In [**37**], a four quadrant analog multiplier using a single OTRA and four MOSFETs has been reported by **Pandey, Pandey, Sriram** and **Paul**. As an application of multiplier, squarer and amplitude modulator also have been discussed.

Rajpoot and **Maheshwari** presented a four quadrant analog multiplier circuit using a single dual-X second generation current conveyor in [**38**]. The circuit has a BW of 19.30 GHz and 0.79% total harmonic distortion for the input voltage of 250 mV.

A simple analog multiplier circuit employing one current-mode extra-X second generation current conveyor and two NMOS transistors is presented in [**39**] by **Kumar**. The reported circuit has four quadrant mode of operations with good dynamic range and low power consumption.

In [**40**], **Filanovsky** and **Bates** presented a CMOS analog square-root and squaring circuits using an op-amp and two nested transistors. In the nested transistor pair, one of these transistors operates in pinch-off mode while, the other operates in linear

region.

The differential difference current conveyors (DDCCs) based squarer and square rooter circuits were reported by **Chiu, Liu, Tsao** and **Chen** in [**41**] employing two MOSFETs, one voltage to current converter and a voltage follower.

In [**42**], a square-root circuit (as shown in Fig. 5.5) has been reported by **Riewruja** and **Kamsri**. The reported circuit uses an op-amp, six resistors and a diode. This circuit is based on the use of op-amp supply-current sensing technique.

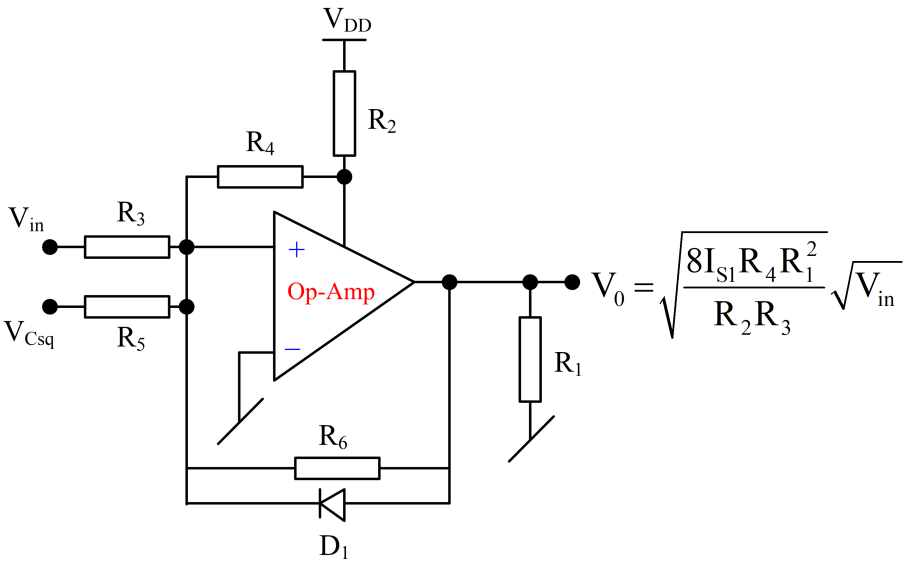


Figure 5.5: Op-amp based square root circuit reported by Riewruja and Kamsri [42]

Using OTAs, two square-root circuits (one in VM and another in CM) were reported in [**43**] by **Riewruja**. In the first circuit, four OTAs and one resistor were used to produce VM square-root function, whereas another CM square-root circuit comprised of four OTAs only. The implementation of square root circuits is based on an electronically tuned resistor formed by an OTA whose magnitude is controlled by the output currents.

Another OTA-based square-root circuit was presented in [**45**] by **Sen, Ray** and **Ray** where three OTAs and two resistors were used.

In [**46**], **Dehjan** and **Netbut** reported two CCCII-based VM and CM square-root circuits where two CCCIIs along with three resistors/one resistor were used in VM and CM respectively. Both the circuits use current mode technique which makes the circuitry simple with wide dynamic range and bandwidth.

In [**47**], a square-rooter circuit was presented by **Liu** which employs a CCII, one unity gain inverting amplifier, one resistor and two MOSFETs (biased in the triode region). The reported bandwidth of the presented circuit was 400 kHz.

CDBA-based two square-root circuits were proposed in [**48**] by **Pathak, Singh** and **Senani**. One of them required one CDBA, one resistor, one buffer and two MOSFETs and another circuit used one CDBA and four MOSFETs. The used MOSFETs were matched and biased in the triode region.

Low voltage, square-root circuit employing OTRA was reported in [**49**] by **Aggarwal, Garg, Bansal, Gangwar** and **Pandey** which required single OTRA and three MOSFETs (biased in the triode region).

From the above description, it may be noted that the reported multiplier, divider and square-root circuits use either more number of active and passive components [18–25, 41–43, 45–47], or more number of MOSFETs [19, 23, 25, 40, 41, 47–49]. It may also be mentioned that the no single CFOA and four MOSFETs based analog multiplier and divider circuit has been previously reported. Similarly, no square root circuit operating in VM, realized with minimum number of ABBs and MOSFETs has been reported so far.

Therefore, in this chapter, we now present a very simple architecture of analog divider circuit that requires only one single output OTA with two NMOS transis-

tors (operating in the triode region) while, in analog square root circuit, a single output OTA with only one NMOS transistor (operating in the saturation region) are used. Finally, a new architecture of analog multiplier/divider circuit employing single CFOA and four NMOS transistors has also been proposed.

5.2 Proposed Analog Divider Circuit Using OTA[1]

Figure 5.6 shows the proposed analog divider circuit.

The circuit employs one single output OTA and two matched NMOS transis-

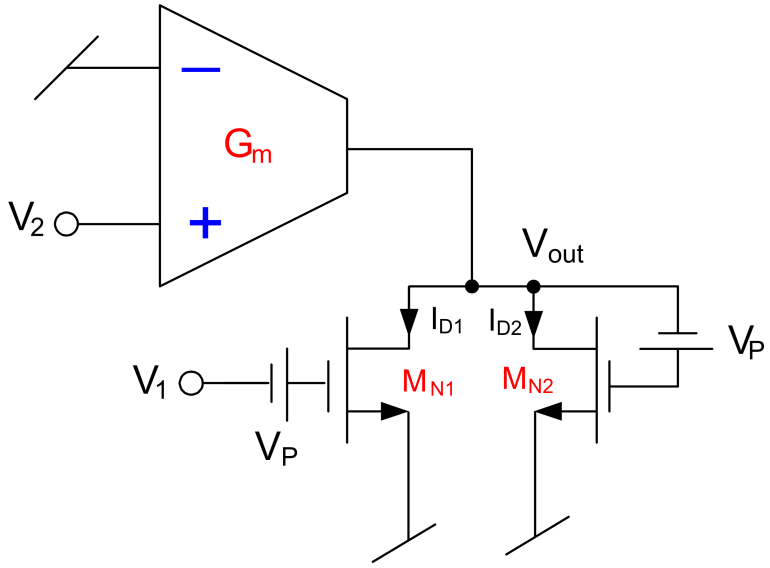


Figure 5.6: Proposed new configuration of VM analog divider

tors, operating in the triode (linear) region, to obtain analog divider function. The expression for drain current of NMOS in triode region (neglecting channel length modulation) is given by [50]:

$$I_{Di} = K_{ni}[\{(V_{GSi} - V_{THi})\, V_{DSi} - \frac{1}{2}V_{DSi}^2\}] \tag{5.1}$$

where i = (1-2), $V_{DS} < (V_{GS} - V_{TH})$, $V_{GS} > V_{TH}$ and $K_n = \mu_n C_{ox}\left(\frac{W}{L}\right)$, μ_n is the surface mobility, C_{ox} is the gate oxide capacitance per unit area, $\left(\frac{W}{L}\right)$ is the aspect ratio, V_{TH} is the threshold voltage, and V_{GS} and V_{DS} are the gate-to-source and drain-to-source voltages, respectively, of the NMOS transistor.

A straightforward analysis of the circuit in Fig. 5.6 reveals that the drain currents

[1]The material in this section has been published in: Ajishek Raj, D. R. Bhaskar, and Pragati Kumar, "Two Quadrant Analog Voltage Divider and Square-Root Circuits Using OTA and MOSFETs." Circuit Systems and Signal Processing, Vol. 39, pp. 6358-6385, (2020).

I_{D1} and I_{D2} are given by:

$$I_{D1} = K_n[\{(V_1 + V_P) - V_{TH}\}V_{out} - \frac{1}{2}V_{out}^2] \tag{5.2}$$

$$I_{D2} = K_n[\{(V_{out} + V_P) - V_{TH}\}V_{out} - \frac{1}{2}V_{out}^2] \tag{5.3}$$

From Fig. 5.6, the output current of the OTA can be expressed as:

$$I_{out} = G_m V_2 = I_{D1} + I_{D2} \tag{5.4}$$

where G_m is the transconductance of the OTA [51] and is given by:

$$G_m = \sqrt{2K_n I_{Bias}\left(\frac{W}{L}\right)} \tag{5.5}$$

Substitution of equations (5.2) and (5.3) in equation (5.4), the following expression can be obtained:

$$G_m V_2 = K_n[\{V_1 + 2\,(V_P - V_{TH})\}] \tag{5.6}$$

Now if $V_P = V_{TH}$, equation (5.6) reduces to:

$$V_{out} = K\left(\frac{V_2}{V_1}\right) \quad where \quad K = \frac{G_m}{K_n} \tag{5.7}$$

where V_1, V_2 are the analog input voltage signals and V_P is the external DC voltage. The floating voltage V_P may be generated as shown in Fig. 5.7.

From equation (5.7), it can be seen that the output voltage of the proposed circuit shown in Fig. 5.6 provides a division of two analog input voltage signals. The output voltage can also be scaled electronically through the transconductance of OTA.

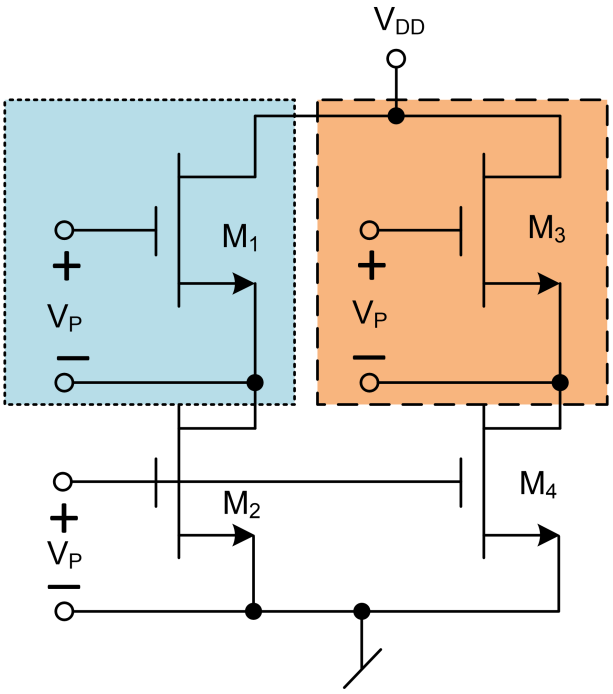


Figure 5.7: Generation of floating voltage source [52]

5.2.1 Mismatch Analysis

5.2.1.1 Mismatch Between Threshold Voltages of M_{N1} and M_{N2}

The MOSFETs M_{N1} and M_{N2} of Fig.5.6 are assumed to be matched, but in practical case, it is very challenging to make threshold voltages of MOSFETs exactly equal. Assuming both MOSFETs M_{N1} and M_{N2} have different threshold voltages V_{TH1} and V_{TH2}, the output voltage of divider circuit may be expressed as:

$$V_{out} = K\left[\frac{V_2}{V_1 + 2V_P - (V_{TH1} + V_{TH2})}\right] \tag{5.8}$$

From equation (5.8), it may be noted that the effect of mismatch in threshold voltage of the MOSFETs may be eliminated by selecting appropriate value of the external DC voltage V_P.

5.2.1.2 Mismatch Between the Aspect Ratios of M_{N1} and M_{N2}

To consider the effect of mismatch in the aspect ratios of the MOSFETs on the output voltage of the divider circuit, we have defined $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right) + \Delta\left(\frac{W}{L}\right)$ and

$\left(\frac{W}{L}\right)_2$=$\left(\frac{W}{L}\right)$-$\Delta\left(\frac{W}{L}\right)$. Thus, re-analysing the divider circuit shown in Fig. 5.6, the following quadratic equation is obtained:

$$V_{out}^2\left(\frac{\Delta\left(\frac{W}{L}\right)}{\left(\frac{W}{L}\right)}\right) - V_{out}\left\{2\left(V_P - V_{TH}\right) + V_1\left(\frac{\Delta\left(\frac{W}{L}\right)}{\left(\frac{W}{L}\right)}\right)\right\} + KV_2 = 0 \tag{5.9}$$

Solution of the quadratic equation with $V_P = V_{TH}$ gives the following output voltage:

$$V_{out} \cong \frac{V_1\left(1+\frac{\Delta\left(\frac{W}{L}\right)}{\left(\frac{W}{L}\right)}\right) - V_1\left(1+\frac{\Delta\left(\frac{W}{L}\right)}{\left(\frac{W}{L}\right)}\right)\left(1-\left(\frac{4KV_2\left(\frac{\Delta\left(\frac{W}{L}\right)}{\left(\frac{W}{L}\right)}\right)}{V_1^2\left(1+\frac{\Delta\left(\frac{W}{L}\right)}{\left(\frac{W}{L}\right)}\right)}\right)\right)^{\frac{1}{2}}}{2\left(\frac{\Delta\left(\frac{W}{L}\right)}{\left(\frac{W}{L}\right)}\right)} \tag{5.10}$$

Using binomial expansion of the radical term in equation (5.10) and neglecting the higher order terms in the expansion we get:

$$V_{out} \cong \frac{KV_2}{V_1}\left(\frac{1}{1+\frac{\Delta\left(\frac{W}{L}\right)}{\left(\frac{W}{L}\right)}}\right) \tag{5.11}$$

From equation (5.11), it may be noted that the effect of mismatch in the aspect ratios does not change the nature of the output voltage function.

5.2.2 Effect of Variation in the Supply Voltage on V_P

The effect of variation in supply voltage on V_P in the output voltage expression of the voltage divider circuit may be considered by assuming $V_P = (V_P \pm \Delta V_P)$. Hence, re-analysing the divider circuit shown in Fig. 5.6, the new output voltage of divider circuit is obtained as:

$$V_{out} = K\left[\frac{V_2}{V_1 + 2(V_P \pm \Delta V_P) - 2V_{TH}}\right] \tag{5.12}$$

From equation (5.12), it may be noted that the voltage V_P must be selected in such a way that the term ΔV_P in parenthesis in the denominator of equation (5.12) is

not significant. An exemplary way of minimizing ΔV_P has been presented below. For generation of external voltage V_P, we have used a voltage divider circuit as shown in Fig. 5.8 with three matched MOSFETs (operating in saturation region).

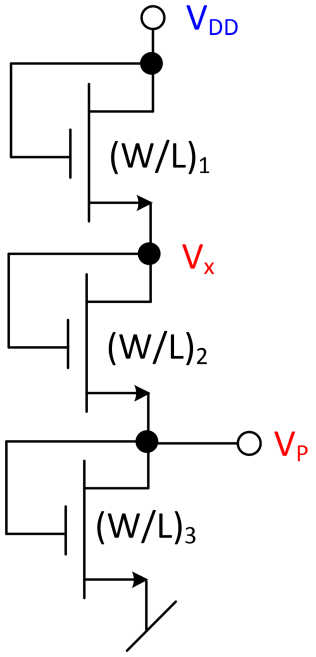


Figure 5.8: Voltage divider circuit

The current flowing through each MOSFET is same and is equal to:

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH1})^2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{DD}V_x - V_{TH1})^2 \quad (5.13)$$

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TH2})^2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_x - V_P - V_{TH2})^2 \quad (5.14)$$

$$I_{D3} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_3 (V_{GS3} - V_{TH3})^2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_3 (V_P - V_{TH3})^2 \quad (5.15)$$

Solving equations (5.13) – (5.15), assuming equal threshold voltages, we get:

$$\begin{aligned} V_P &= \frac{\sqrt{\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}}(V_{DD} - V_{TH})}{1 + \sqrt{\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}} + \sqrt{\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_3}}} \\ &\approx \sqrt{\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}}(V_{DD} - V_{TH})\left(1 - \sqrt{\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}} - \sqrt{\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_3}}\right) \end{aligned} \quad (5.16)$$

Now, in equation (5.16), if a deviation is introduced in V_{DD} by a value of $\pm\Delta V_{DD}$, then equation (5.16) becomes:

$$V_P \approx V_P + V_P^{/} \tag{5.17}$$

where

$$V_P^{/} = \pm \frac{\Delta V_{DD}}{1 + \sqrt{\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}} + \sqrt{\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_3}}} \tag{5.18}$$

Therefore, from equation (5.18), the effect of changes in V_{DD} may be made negligible small, if $(W/L)_2 >> (W/L)_1$ and $(W/L)_2 >> (W/L)_3$. The effect of variation in V_P on the output has been evaluated through simulation results.

5.2.3 High-Frequency Response of Divider Circuit

The high-frequency performance of the divider circuit presented in Fig. 5.6 has been investigated by determining the poles associated with (i) the OTA and (ii) the M_{N1}–M_{N2} network which is connected at the output of the OTA. The transconductance G_m of the OTA may be modeled by a one pole model [53] as:

$$G_m(s) = \frac{G_{m0}}{1 + \frac{s}{\omega_b}} \tag{5.19}$$

On the other hand, the pole of the M_{N1}–M_{N2} network has been determined by carrying out a small-signal analysis of this network and has been found to be:

$$\omega_{3dB}^P = \left(\frac{1 + g_2(r_{o1}||r_{o2})}{(C_{gd1} + C_{ds1} + C_{ds2} + C_{gs2})(r_{o1}||r_{o2})} \right) \cong \frac{g_2}{C_o} for g_2 r_o >> 1 \tag{5.20}$$

where $C_o = (C_{gd1} + C_{ds1} + C_{ds2} + C_{gs2})$, g_2 is the transconductance of the MOSFET M_{N2} and $r_o = r_{o1}||r_{o2}$. From simulations, the values of ω_{3dB}^P and ω_b have been found to be 53.7 GHz and 4.68 GHz, respectively. Thus, the high-frequency performance of the voltage divider circuit will be limited by the pole of the OTA circuit as $\omega_b < \frac{\omega_{3dB}^P}{10}$.

5.3 Inverse Function

The proposed divider circuit can be modified to provide an inverse function. It can be obtained by keeping V_2 constant and making V_1 as an input signal, the output voltage of equation (5.7) reduces to:

$$V_{out} = K_1 \left(\frac{1}{V_1} \right) \quad where \quad K_1 = KV_2 \tag{5.21}$$

From equation (5.21), it may be noted that the output voltage V_{out} is proportional to the inverse of the analog input voltage signal V_1. In this case too, V_{out} can be electronically controlled through the transconductance G_m of OTA.

5.4 Simulation Results of Divider and Inverse Functions

The workability of the circuit presented in Fig. 3.10 has been verified through simulations by Cadence Virtuoso tool using $0.18\mu m$ TSMC CMOS technology parameters. The same CMOS OTA shown in Fig. 2.15 has been used to simulate both the divider and inverse functions. The power supply voltages used were ± 0.9V. The transconductance (G_m) of OTA was set in such a way that the $\frac{G_m}{K_n}$ equal to 1. It may be noted that a voltage follower (buffer) will be required at the output of each divider circuit to prevent loading.

5.4.1 Voltage Division Mode

For voltage division mode of operation, the aspect ratios of M_{N1} and M_{N2} were selected as 1.44 $\mu m/0.36\mu m$. The aspect ratios of all the four MOSFETs used in the level shifter circuit (Fig. 5.7), used for generating the floating voltage source of 380 mV (equal to V_{TH}), were taken as 3.6 $\mu m/3.6$ μm.

5.4.1.1 DC Characteristics

The DC transfer characteristics of the proposed divider circuit are illustrated in Fig. 5.9, in which, the variation of output voltage with V_1 is shown when the input voltage V_2 was varied from -50 mV to +50 mV in steps of 10 mV whereas, in Fig. 5.10, the variation of output voltage with V_2 is shown when the input voltage V_1 is varied from 0.5 V to 1.5 V. An offset of -2.94 mV, -2.65 mV and -2.04 mV was observed in output voltage when V_2 was equal to zero and V_1 was taken as 0.5 V, 1 V and 1.5 V respectively.

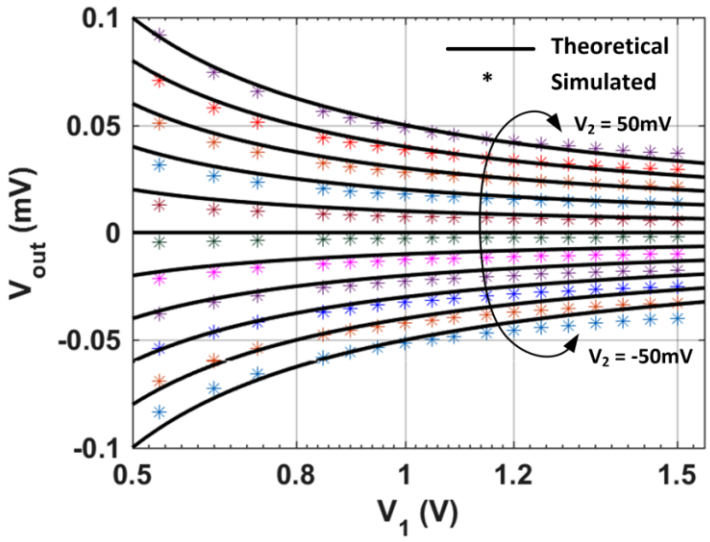


Figure 5.9: DC transfer curve of V_{out} and V_1 with V_2 as a variable parameter

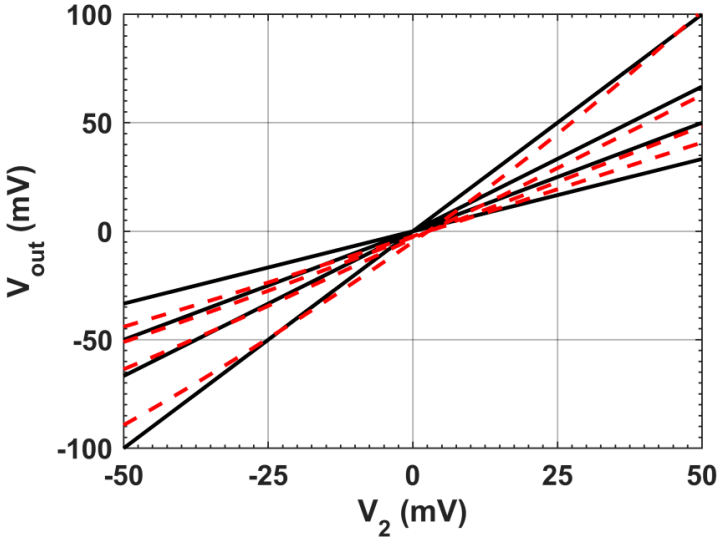


Figure 5.10: DC transfer curve of V_{out} and V_2 with V_1 as a variable parameter

We have computed the error between theoretical and simulated outputs when the input voltage V_1 was varied from 0.5 V to 1.5 V and V_2 was varied between – 50 mV to +50 mV and the same has been presented in Table 5.1.

Table 5.1: Theoretical and simulated output voltages with error for different values of V_1 and V_2

	V_1=0.5V			V_1=1V			V_1=1.5V		
V_2 (mV)	V_{out}(T) (mV)	V_{out}(S) (mV)	Error (%)	V_{out}(T) (mV)	V_{out}(S) (mV)	Error (%)	V_{out}(T) (mV)	V_{out}(S) (mV)	Error (%)
50	100	100.43	0.43	50	48.33	3.34	33.33	34.60	3.81
40	80	78.14	2.32	40	38.13	4.67	26.67	27.65	3.67
30	60	57.72	3.8	30	28.85	3.83	20	21.08	5.4
20	40	38.32	4.2	20	18.98	5.1	13.33	13.5	1.27
10	20	18.90	5.5	10	9.47	5.3	6.67	6.35	4.79
0	0	-2.94		0	-2.65		0	-2.04	
-10	-20	-21.05	5.2	-10	-10.52	5.2	-6.67	-7.08	6.14
-20	-40	-40.84	2.1	-20	-21.12	5.6	-13.33	-14.277	7.05
-30	-60	-58.78	2.03	-30	-31.26	4.2	-20	-21.86	9.3
-40	-80	-77.96	2.55	-40	-41.78	4.45	-26.67	-29.29	9.82
-50	-100	-95.25	4.75	-50	-51.02	2.04	-33.33	-36.71	10.14

As the input voltage V_2 is applied to the OTA directly, the maximum/minimum value of V_2 which can be applied is restricted by the linear range of the CMOS OTA (±50 mV). For the input voltage V_1, the minimum value is restricted by the saturation voltage (±0.9 V) of the OTA while, the maximum value of V_1 is restricted by the linearity error. After the repeated simulations, we have found that the divider circuit works satisfactorily when V_1 was kept in the range of 0.5 V to 1.5 V and V_2 was kept in the range of -50 mV to +50 mV.

5.4.1.2 Frequency and Transient Responses

The frequency response of the proposed analog divider circuit has been displayed in Fig. 5.11 from which –3 dB bandwidth is found to be 4.5 GHz.

We have verified the transient performance of the divider circuit at 1 MHz, 100 MHz, 1 GHz and 4 GHz by applying a triangular input voltages, $V_2 = \pm$ 20 mV_{PP} and $V_1 = \pm$ 100 mV_{PP} with an offset of 150 mV. The simulated output voltage

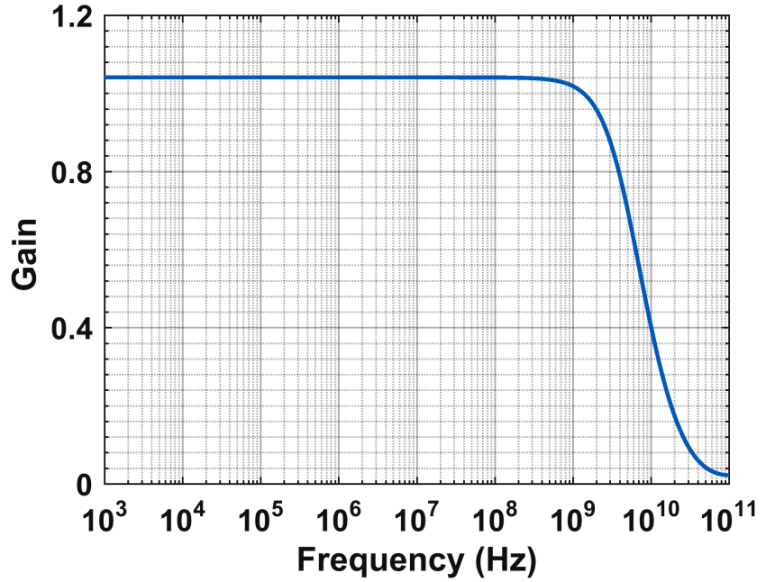
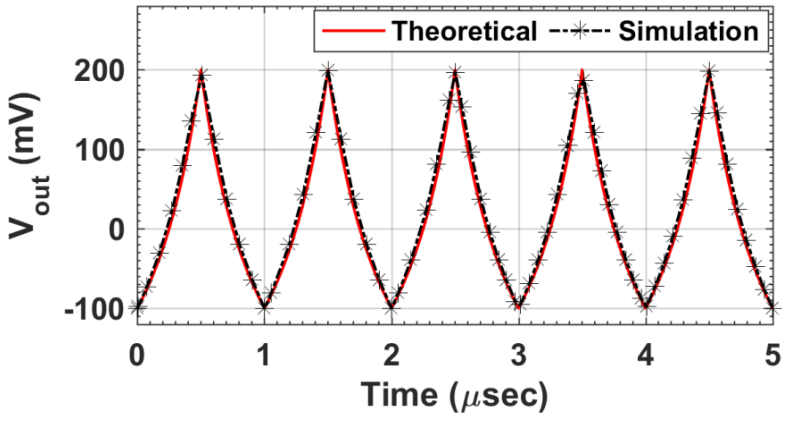
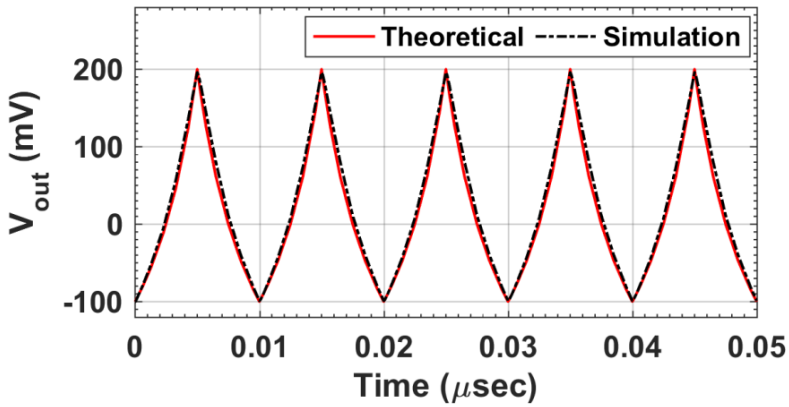


Figure 5.11: Frequency response of the proposed analog divider circuit

obtained by the divider circuit has been shown in Fig. 5.12.

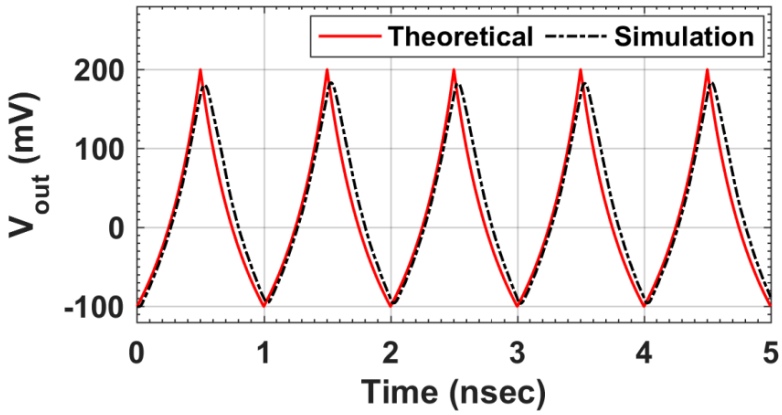


(a)

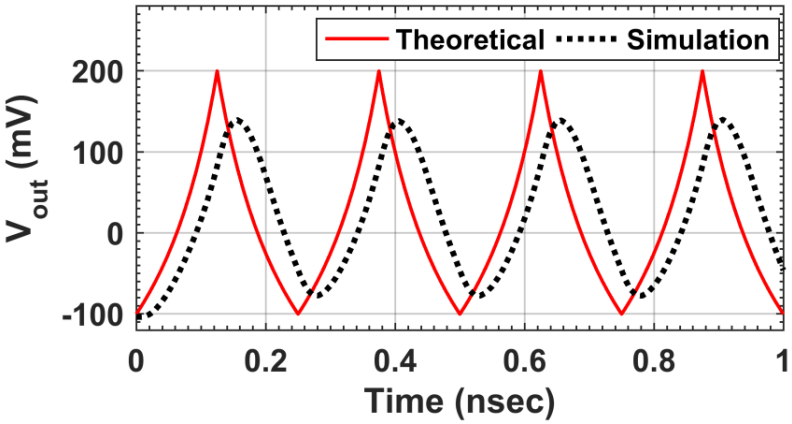


(b)

In Fig. 5.13, we have shown the output voltage with 1%, 2%, 5% and 10% variation in V_P. Fig. 5.14 displays the electronic controllability of output voltage when G_m



(c)



(d)

Figure 5.12: Transient output responses of the proposed divider circuit at (a) 1 MHz (b) 100 MHz (c) 1 GHz (d) 4 GHz

was varied from 1 mS to 2 mS.

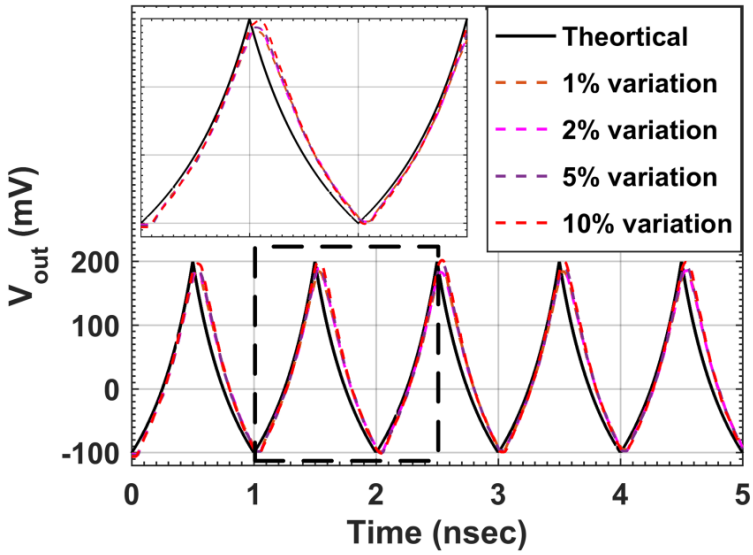


Figure 5.13: Output voltage of voltage divider circuit with variation in V_P

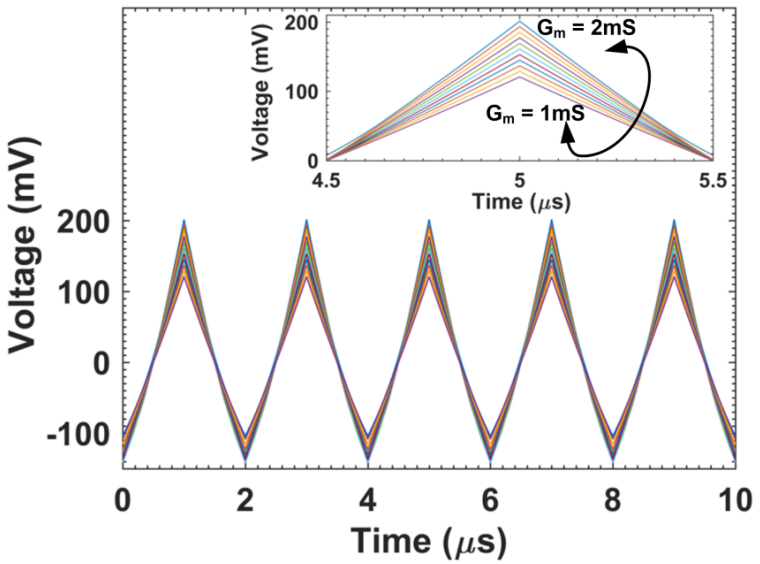


Figure 5.14: Electronic tunability of output voltage of proposed divider circuit

5.4.1.3 Temperature Analysis

As the output voltage depends on G_m and K_n (both of which depend on temperature), we have evaluated the effect of variations in temperature on the output voltage when the temperature was varied from -10°C to 50°C and the simulated output voltages are shown in Fig. 5.15. The maximum power consumption for the divider circuit was found to be 821 μW.

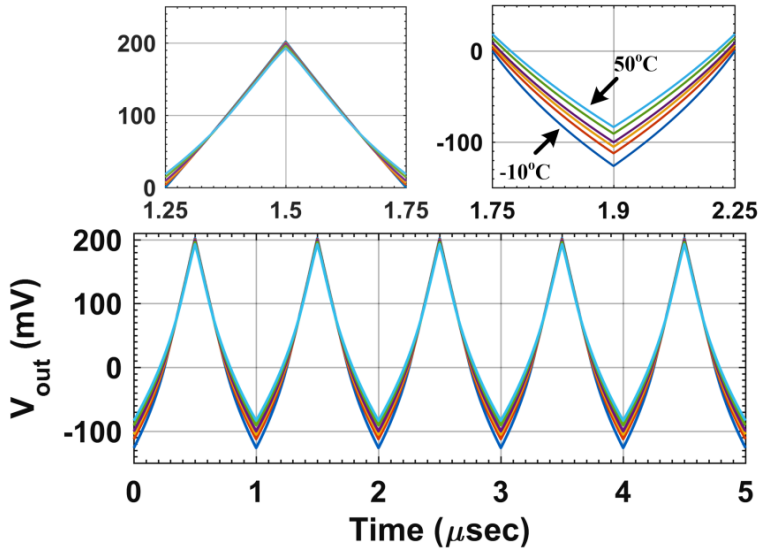


Figure 5.15: Effect of temperature on output voltage of divider circuit of Fig. 5.6

5.4.2 Inverse Function Generation Mode

For the inverse function generator circuit, we have applied V_1 as a triangular wave with amplitude of 20 mV_{PP} at frequency of 500 kHz while V_2 was taken as 10 mV (DC). The transient responses of input and output voltage of the inverse function generator circuit are displayed in Fig. 5.16.

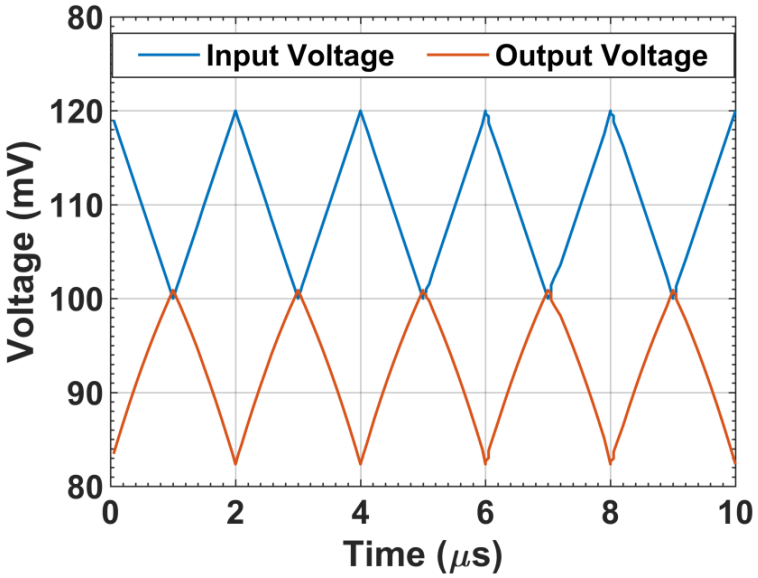


Figure 5.16: Input and output transient responses of inverse function of Fig. 5.6

5.5 Analog Square Root Circuit using OTA

The proposed square-root circuit employing one single output OTA and one MOSFET is shown in Fig. 5.17.

The drain current of MOSFET in the saturation region (neglecting channel length modulation) is given by [50]:

$$I_D = \frac{K_n}{2}(V_{GS} - V_{TH})^2 \tag{5.22}$$

where $V_{DS} > (V_{GS} - V_{TH})$, $V_{GS} > V_{TH}$.

A straightforward analysis of the proposed circuit in Fig. 5.17 yields the following

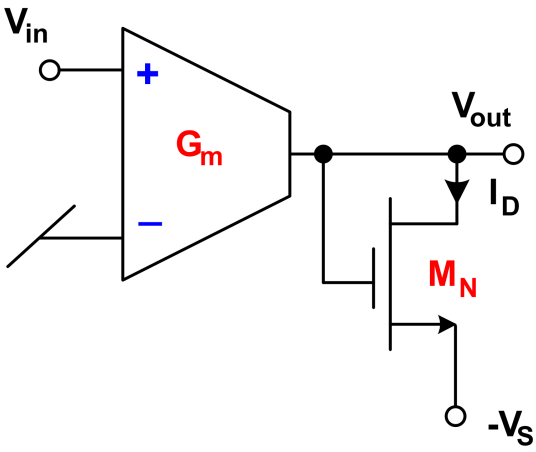


Figure 5.17: Proposed square-root circuit

output voltage:

$$G_m V_2 = K_n \left(V_{out} + V_s - V_{TH}\right)^2 \tag{5.23}$$

Now if $V_s = V_{TH}$, equation (5.23) becomes

$$V_{out} = \sqrt{2KV_{in}} \tag{5.24}$$

From equation (5.24), we can see that the output voltage is proportional to the square root of the input signal voltage which can also be scaled electronically through the transconductance of OTA. If channel length modulation effect is taken into account, the drain current of the MOSFET will be expressed by [50]:

$$I_D = \frac{K_n}{2}\left(V_{GS} - V_{TH}\right)^2 \left(1 + \lambda V_{DS}\right) \tag{5.25}$$

The modified output voltage of the square-root circuit with channel length modulation may be approximated (with $V_s = V_{TH}$) as:

$$V_{out} \cong \sqrt{2KV_{in}} \left(1 - \frac{\lambda}{2} V_{TH}\right) \left(1 + \frac{\lambda}{2} V_{in}\right) \tag{5.26}$$

From equation (5.26), it is noticed that the channel length modulation coefficient introduces some error in the output of the square-root circuit. However, the error introduced, because of the channel length modulation effect ($\lambda = 0.094$), when the

input voltage V_{in} in Eqs. (5.24) and (5.26) was varied between 0 and 100 mV, has been found to be less than 1.7 %, which is adequately low.

5.5.1 Simulation and Experimental Results of Square-Root Circuit

5.5.1.1 DC Characteristics

The DC transfer characteristic of the proposed square-root circuit when the input voltage was varied from 0 to 100 mV is illustrated in Fig. 5.18. The error between the theoretical and simulated output is given in Table 5.2.

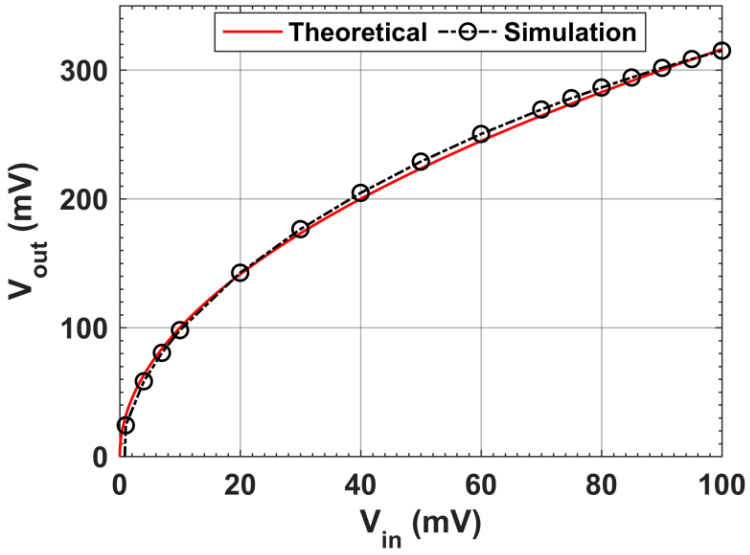


Figure 5.18: DC transfer characteristics of output voltage for different bias currents of Fig. 5.17

Table 5.2: Theoretical and simulated output voltage and % error in output voltage

Input Voltage (V_{in})	Output Voltage (V_{out})		%Error
	Theoretical	Simulated	
0	0	0.3 mV	0.3%
20 mV	141.421 mV	142.634 mV	0.85%
40 mV	200 mV	304.653 mV	2.3%
60 mV	245 mV	250 mV	2.04%
80 mV	282.843 mV	286.456 mV	1.27%
100 mV	316.228 mV	315.088 mV	0.36%

5.5.1.2 Frequency and Transient Responses

The frequency response of the presented square-root circuit has been shown in Fig. 5.19, from which the bandwidth of the circuit is found to be 4.42 GHz.

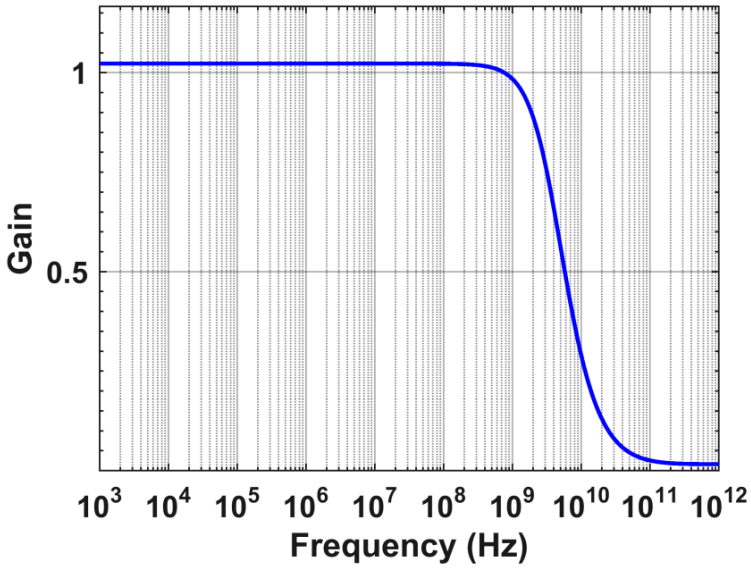
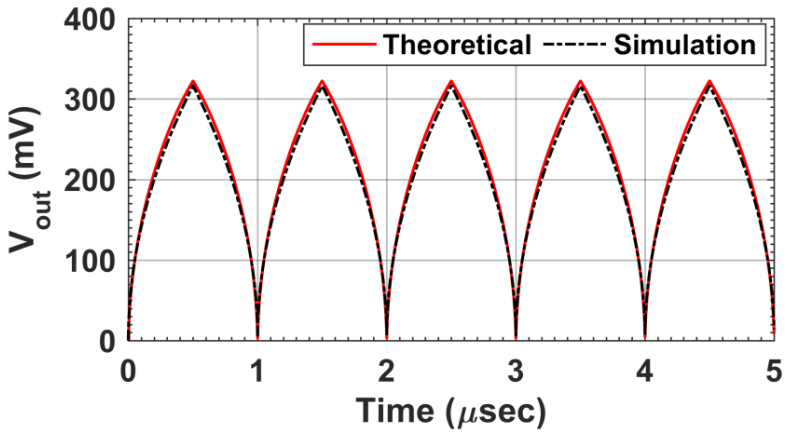


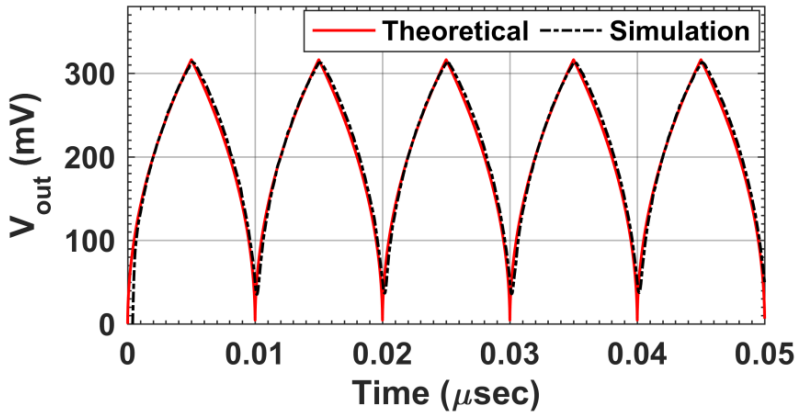
Figure 5.19: Frequency response of the proposed square-root circuit of Fig. 5.17

We have verified the transient performance of the square-root circuit at 1 MHz, 100 MHz and 1 GHz by applying a triangular input voltage $V_{in} = \pm 100$ mV_{PP} with an offset of 50 mV. The simulated output voltage obtained by the square-root circuit has been displayed in Fig. 5.20.

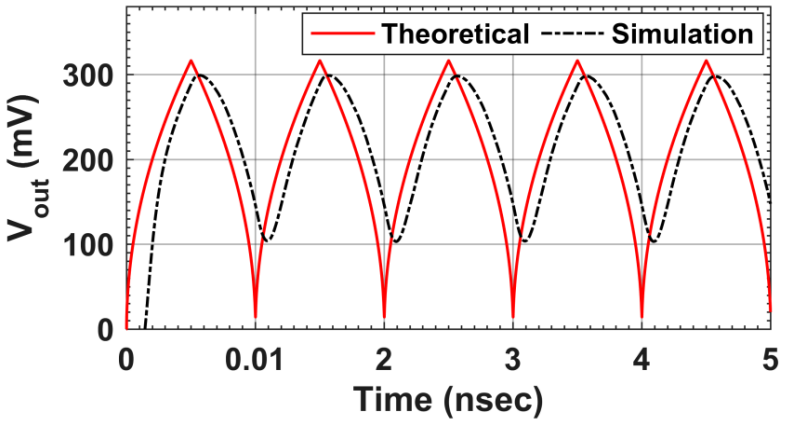


(a)

A sinusoidal waveform of magnitude 100 mV_{PP} with an offset of 50 mV at a frequency of 1 MHz was also applied as the input and the corresponding output voltages (V_{01},



(b)



(c)

Figure 5.20: Transient output responses of the proposed square root circuit at (a) 1 MHz (b) 100 MHz (c) 1 GHz

V_{02} and V_{03}) for different values of bias current (682 μ A, 303 μ A and 75 μ A) have been shown in Fig. 5.21.

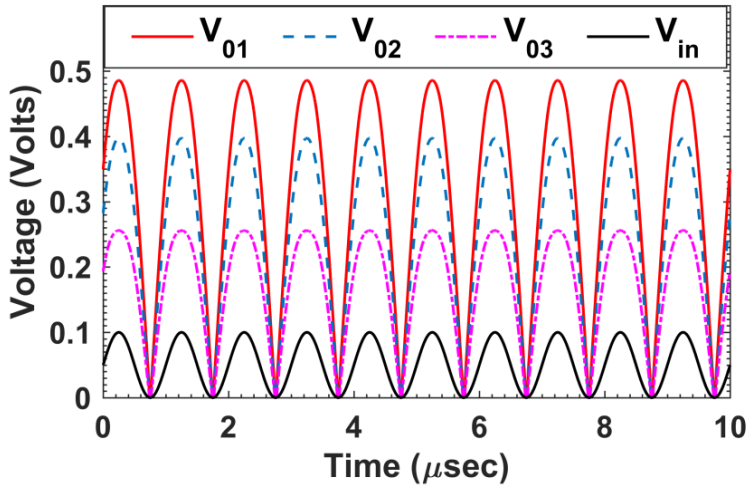


Figure 5.21: Transient input and output responses for the sine wave signal of 1 MHz

5.5.1.3 Temperature Analysis

The output voltage of the square-root circuit depends on G_m and K_n thus, we have evaluated the effect of variations in temperature on the output voltage when the temperature was varied from -10°C to 50°C and the simulated responses are shown in Fig. 5.22. The maximum power consumption for the square-root circuit was found to be 442 μW.

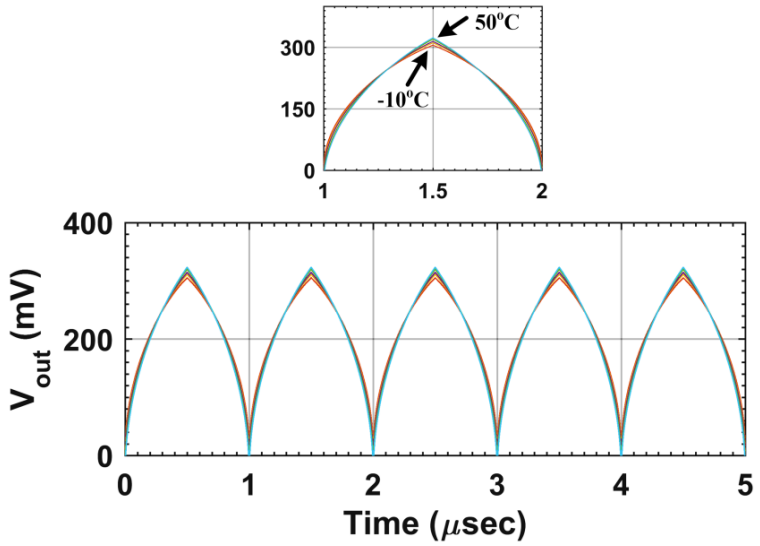
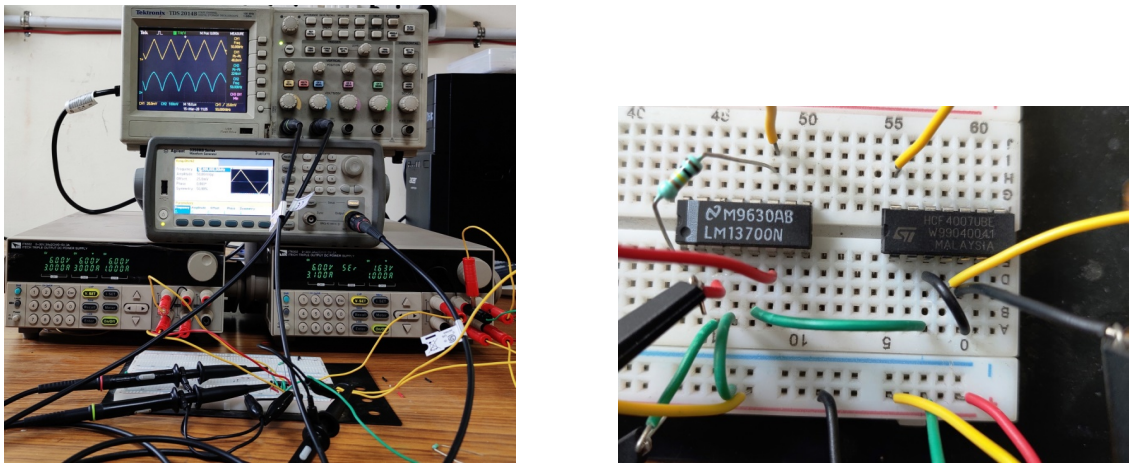


Figure 5.22: Effect of temperature on output voltage of square-root circuit

5.5.1.4 Experimental Results

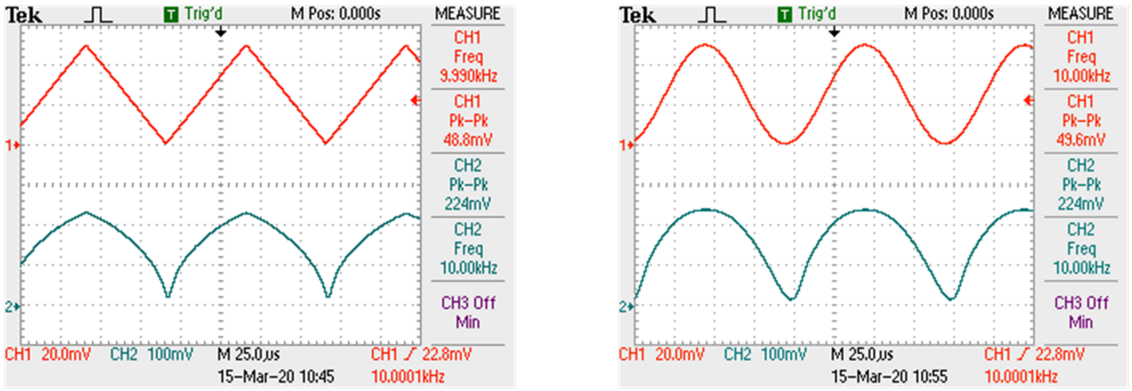
To validate the theoretical propositions, square-root circuit was bread-boarded using off-the-shelf available OTA IC LM13700 and CMOS transistor array HCF4007UBE. The experimental setup of proposed square root circuit has been shown in Fig. 5.23.

The power supplies used to bias the OTA and the transistor array were taken as ± 6V. A resistor of 100 kΩ was used to set the transconductance value of OTA at 2.04 mS while the source of NMOS transistor M_N was kept at -1.63 V. The performance of the square root circuit was verified by applying (i) triangular wave and (ii) sinusoidal wave of 50 mV_{PP} with 25 mV offset at 10 kHz, 50 kHz and 100 kHz. The corresponding output voltages are illustrated in Fig. 5.24, Fig. 5.25 and Fig. 5.26 respectively.



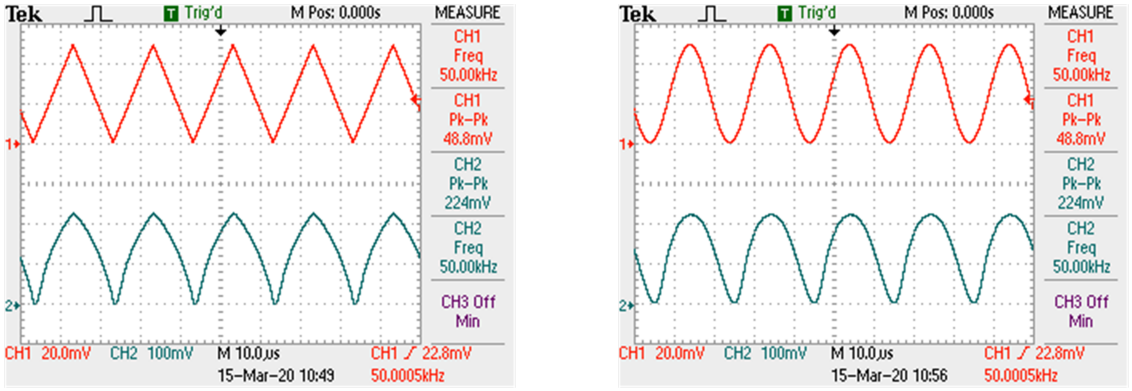
(a) (b)

Figure 5.23: Experimental setup for proposed square-root circuit of Fig. 5.17



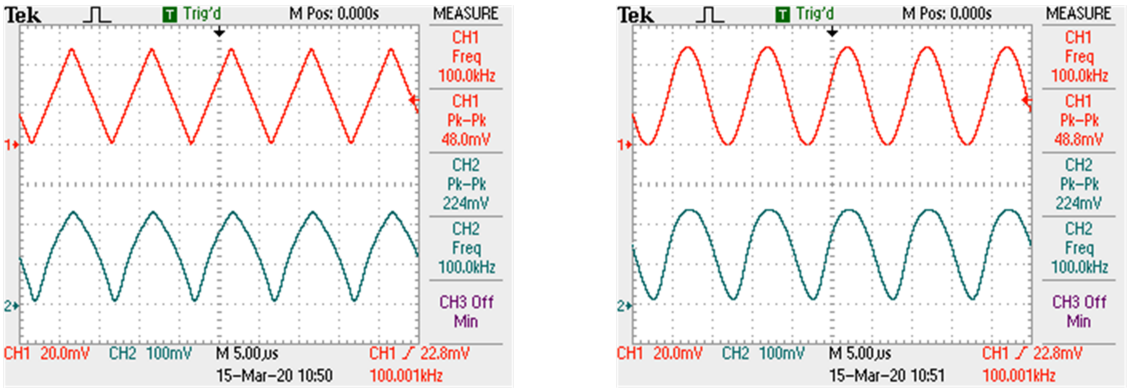
(a) (b)

Figure 5.24: Experimental input and output transient responses of the proposed square-root circuit at 10 kHz (a) triangular wave (b) sinusoidal input



(a) (b)

Figure 5.25: Experimental input and output transient responses of the proposed square-root circuit at 50 kHz (a) triangular wave (b) sinusoidal input



(a) (b)

Figure 5.26: Experimental input and output transient responses of the proposed square-root circuit at 100 kHz (a) triangular wave (b) sinusoidal input

The above simulation and experimental results, thus, establish the workability of the presented circuits.

5.6 Application Examples

5.6.1 Use of Divider Circuit to Linearize Transducer Output

The divider circuit presented in this chapter may be used to control electronically the sensitivity of the linearized transducer output [24] as shown in Fig. 5.27.

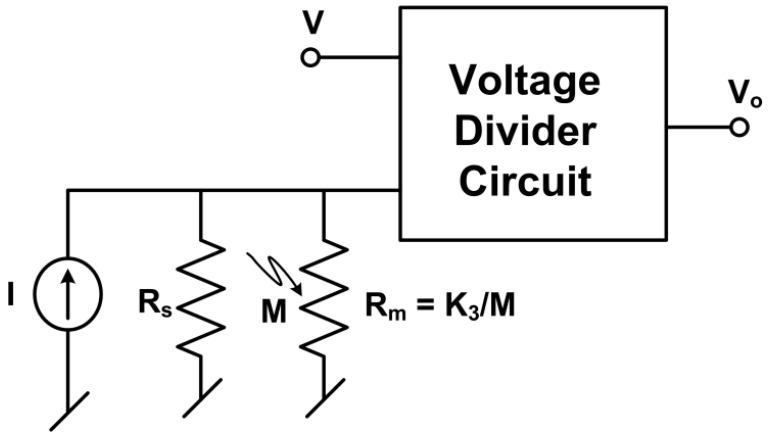


Figure 5.27: Scheme to linearize transducer output [24]

The output voltage equation with the presented divider circuit (Fig. 5.6) may

be expressed as:

$$V_o = \frac{VG_m}{K_n I R_s} + \left(\frac{V}{K_n I K_3}\right) G_m M \tag{5.27}$$

From equation (5.27), it may be noted that as G_m can be controlled by changing the bias voltage of the OTA (as shown in Fig. 5.14), the sensitivity of the transducer output may be controlled electronically.

5.6.2 Linear Voltage Controlled Resistor Using Analog Divider Circuits

The analog divider circuit presented in this paper can be used to modify the characteristics of the linearized voltage controlled resistor [52] by deriving the control voltages from the output of analog divider circuits as shown in Fig. 5.28.

Assuming MOSFETs M_x and M_y to be matched and operating in saturation region,

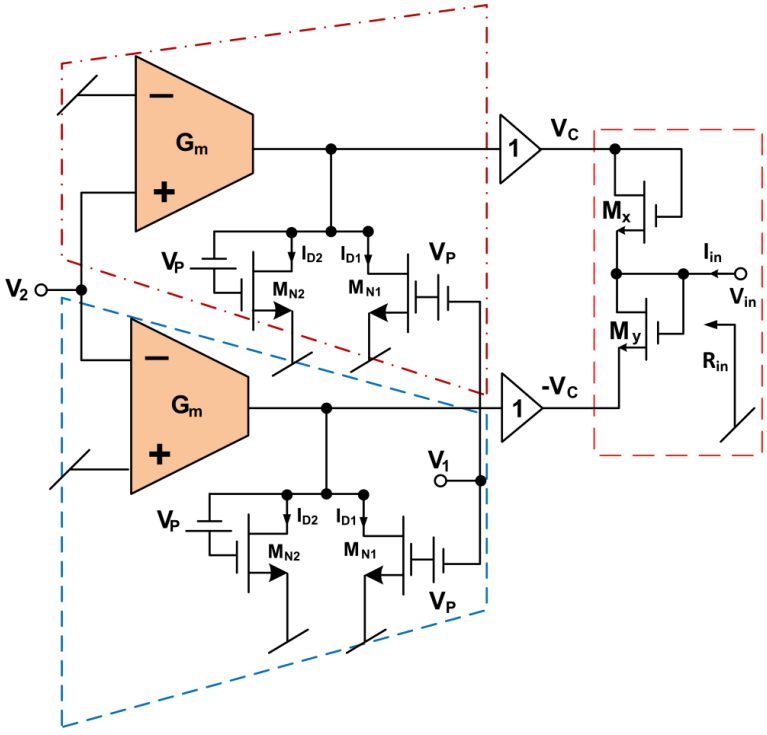


Figure 5.28: Scheme to control resistor through output of the divider circuit

the input resistance R_{in} can be expressed as:

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{1}{2K_x(V_C - V_{TH})}; where \quad K_x = K_y = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{x,y} \tag{5.28}$$

Since V_C is the output voltage of the divider circuit which is given by: $V_C = \frac{G_m}{K_n}\left(\frac{V_2}{V_1}\right)$, now if we keep V_2 constant and vary V_1, the simulated resistance will increase which has been displayed in Fig. 5.29.

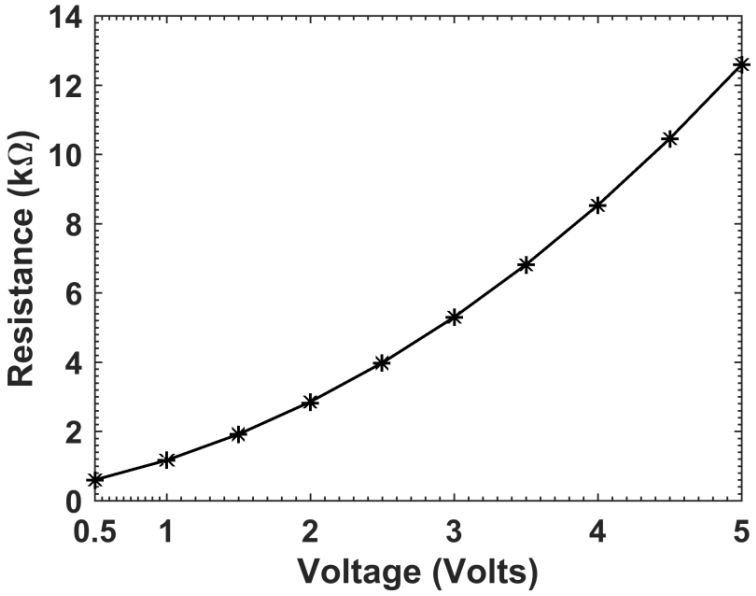


Figure 5.29: Variation of R_{in} with V_1

5.7 Multiplier and Divider Circuit Using a Single CFOA

From a detailed survey of the relevant literature, as presented in section 5.1, it has been found that only two circuits have been reported yet for the design of non-linear analog functions employing CFOA. In this section, we have presented all MOS VM analog multiplier/divider circuit which employs a single CFOA alongwith four MOSFETs operated in triode (linear) region.

5.7.1 Non-Linear Analog Multiplier and Divider Circuit Using CFOA[2]

The proposed multiplier/divider circuit employing single CFOA and four MOSFETs is shown in Fig. 5.30.

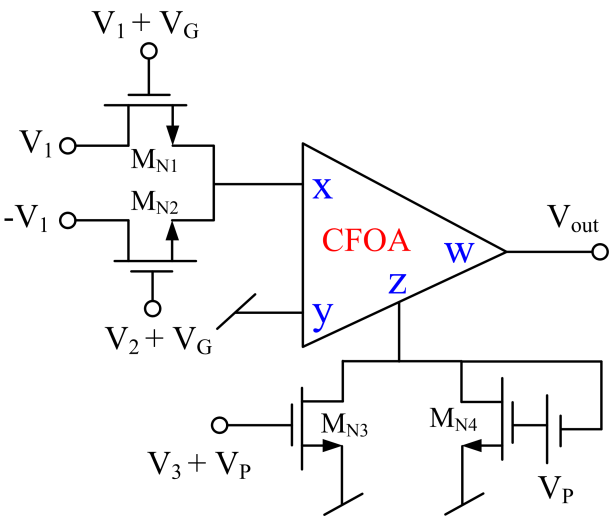


Figure 5.30: VM analog multiplier/divider configuration

Assuming ideal CFOA (characterized by $i_y = 0, v_x = v_y, i_z = i_x$, and $v_w = v_z$), a routine analysis of the circuit shown in Fig. 5.30, yields the following expression

[2]The material in this section has been published in: Ajishek Raj, D. R. Bhaskar, and Pragati Kumar, "Novel Architecture of Four Quadrant Analog Multiplier/Divider Circuit Employing Single CFOA." Analog Integrated Circuits and Signal Processing, (2021).

relating the output voltage and the input voltages:

$$V_{out} = \frac{V_1 V_2}{V_3 + 2(V_P - V_{TH})} \tag{5.29}$$

If we select $V_P = V_{TH}$,equation (5.29) reduces to

$$V_{out} = \frac{V_1 V_2}{V_3} \tag{5.30}$$

where V_1, V_2, V_3 are input analog voltage signals.

From equation (5.30), it may be noted that the output voltage of the proposed circuit of Fig. 5.30 is directly proportional to the multiplication of input voltages V_1 and V_2, and is inversely proportional to V_3. The circuit, thus, can be used in (i) multiplier mode, if the voltage V_3 is kept constant and (ii) divider mode, if either V_1 or V_2 is constant and the signals to be used in division being taken as V_2 or V_1 and V_3, without changing the structure of the circuit. It may also be noted from equation (5.30) that the output voltage of proposed multiplier/divider topology is independent from transconductance parameters of MOSFETs.

5.7.1.1 Mismatch Analysis between Threshold Voltages of MOSFETs

Because of variation in the process parameters, the threshold voltages of the four NMOS transistors may not be exactly same and the output voltage of the circuit may be different from its ideal value. We have evaluated the effects of the mismatch in the threshold voltages analytically. Assuming different threshold voltages V_{TH1}, V_{TH2}, V_{TH3} and V_{TH4} for MOSFETs M_{N1}, M_{N2}, M_{N3} and M_{N4} respectively, the output voltage of multiplier and divider circuit may be expressed as:

$$V_{out} = \frac{V_1 V_2 - V_1(V_{TH2} - V_{TH1})}{V_3 + 2V_P - (V_{TH3} + V_{TH4})} \tag{5.31}$$

From equation (5.31), it is observed that any mismatch between the threshold voltages of M_{N1} and M_{N2} will be reflected as DC offset in the output. However, the

effect of any mismatch between the threshold voltages of M_{N3} and M_{N4} on the output may be eliminated altogether by selecting appropriate value of V_P.

5.7.2 Simulation Results

To verify the theoretical propositions of the proposed multiplier/divider topology, PSPICE simulations have been carried out. An exemplary CFOA implemented using 0.18µm TSMC technology parameters as shown in Fig. 5.31 has been used for the verification of proposed multiplier/divider structure.

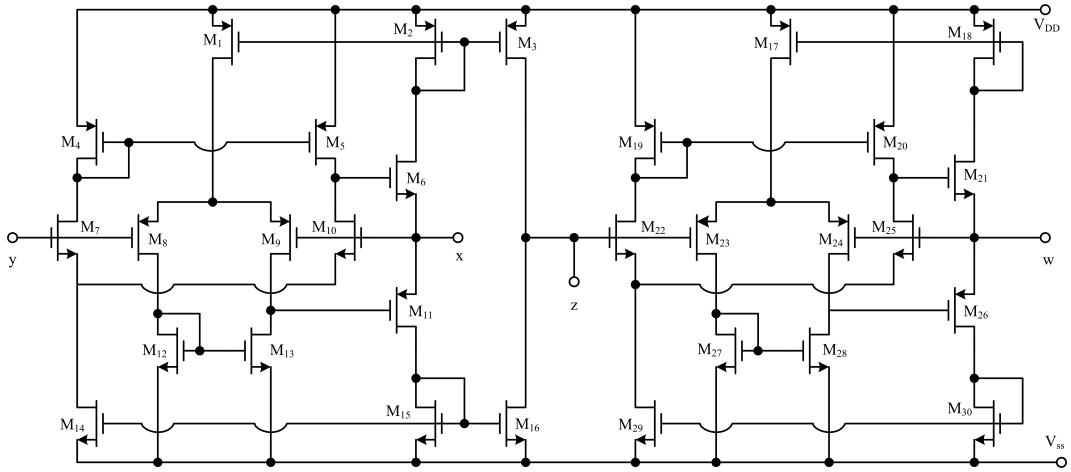


Figure 5.31: CMOS implementation of CFOA [54]

The aspect ratios used for various MOSFETs in Fig. 5.31 have been tabulated in Table 5.3. The power supply voltages $V_{DD} = -V_{SS}$ were taken as 1.25 V.

Table 5.3: Aspect ratios of MOSFETs as shown in Fig. 5.31

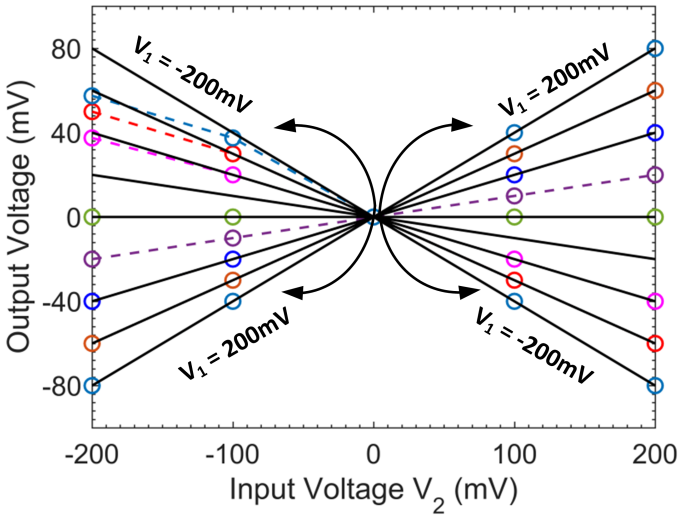
MOSFETs	Aspect Ratio (W/L)
M1 - M5, M8 - M9, M17 - M20, M23 - M24	54/0.72
M11 , M26	270/0.72
M6, M21	135/0.72
M7, M10, M12 - M16, M22, M25, M27 - M30	18/0.72

The aspect ratios of all external MOSFETs used were taken as 3.6 μm/3.6 μm. The discrete MOSFETs used in the realization of multiplier/divider (M_{N1}, M_{N2}, M_{N3} and M_{N4}) circuit were operating in triode region and the MOSFETs used for floating voltage source (M_{F1}, M_{F2}, M_{F3} and M_{F4}) were operating in saturation

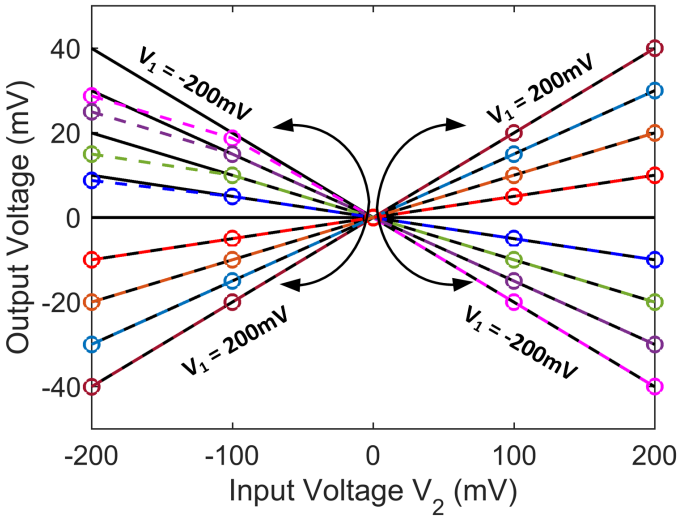
region.

5.7.2.1 Voltage Multiplication Mode

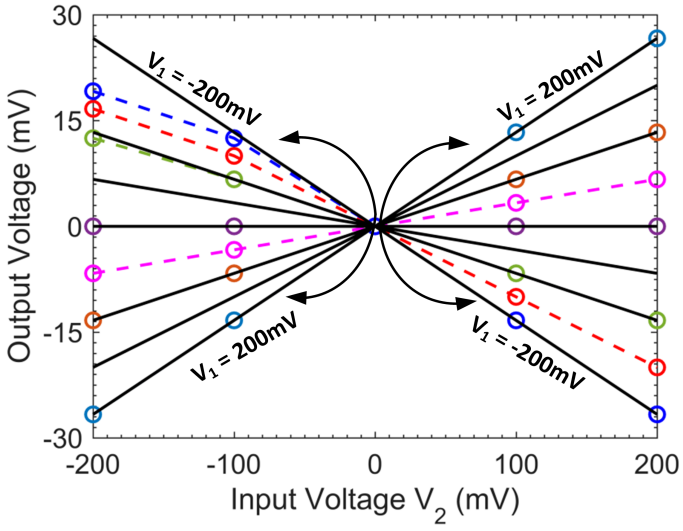
The DC characteristics of the voltage multiplier circuit are illustrated in Fig. 5.32, wherein, the variation of the output voltage with V_2, when the input voltage V_1 was varied from -200 mV to +200 mV in steps of 50mV for different values of V_3 (a) 500 mV, (b) 1 V and (c) 1.5 V have been shown.



(a)



(b)



(c)

Figure 5.32: DC analysis curves of V_{out} and V_2 with V_1 as a variable parameter

From the above simulated output voltages, it may be observed that the error between theoretical and simulated output voltage is more when the input voltage V_1 is less than -100 mV for different values of input voltage V_2. It may be pointed out that the MOSFETs M_{N3} and M_{N4} must operate in the triode region for the implementation of both the multiplier as well as divider circuit. The maximum output voltage V_{out} will thus, be limited by the input voltage V_3 as given below.

$$V_{out} \leq (V_3 + V_G - V_{TH}) \tag{5.32}$$

Fig. 5.33 shows the AC responses of the multiplier circuit and the -3dB frequency was found to be 200 MHz when input signals V_1, V_2 were applied and V_3 was kept constant at 100 mV.

5.7.2.2 Application Examples of Multiplier Circuit

(a) Amplitude Modulator:

For the application of multiplier circuit as amplitude modulator, the input voltage (V_1) was taken as a sinusoidal wave of 100 kHz with peak to peak amplitude of 200

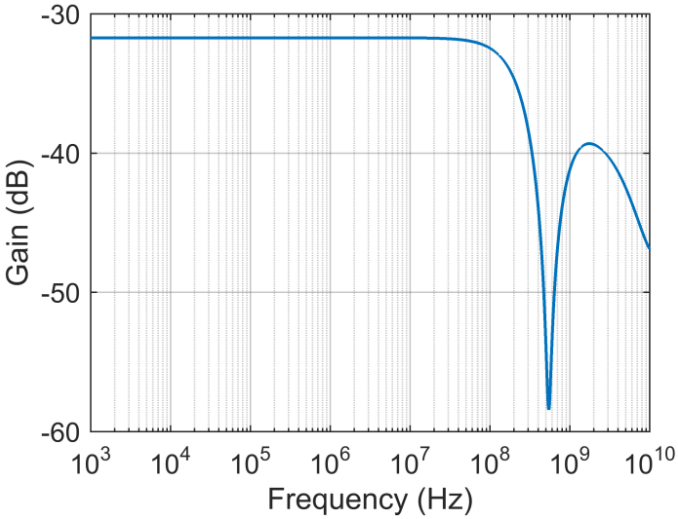


Figure 5.33: Frequency response of proposed multiplier circuit

mV while the voltage (V_2) was taken as sinusoidal of 1 MHz with a peak to peak voltage of 200 mV as shown in Fig. 5.34 (a) and 5.34 (b) respectively. A DC input voltage applied at V_3 with amplitude of 200 mV. The simulated output voltage of modulator circuit has been shown in Fig. 5.34 (c). The frequency spectrums (in dB) of inputs and output are also displayed in Fig. 5.34.

In Fig. 5.35, we have shown the sample modulator output voltages when the frequency of V_2 was (a) 100MHz and (b) 200 MHz while the frequency of V_1 was kept 2 MHz.

The performance of multiplier circuit has also been evaluated with variations in the aspect ratios of external MOSFETs (M_{N1}, M_{N2}, M_{N3} and M_{N4}). Fig. 5.36 shows the output voltage of modulator when width of the MOSFETs have deviation of $\pm$ 10%.

To test the robustness of the multiplier circuit, we have carried out Monte-Carlo simulations by varying the input voltage V_2 with a nominal tolerance of 10% (considering Gaussian distribution) for 100 runs and the histogram of the Monte-Carlo simulations has been shown in Fig. 5.37. From Fig. 5.37, it may be noted that the maximum output voltage of the multiplier circuit is 48.97mV after 100 iterations which is close to the theoretical value (50 mV).

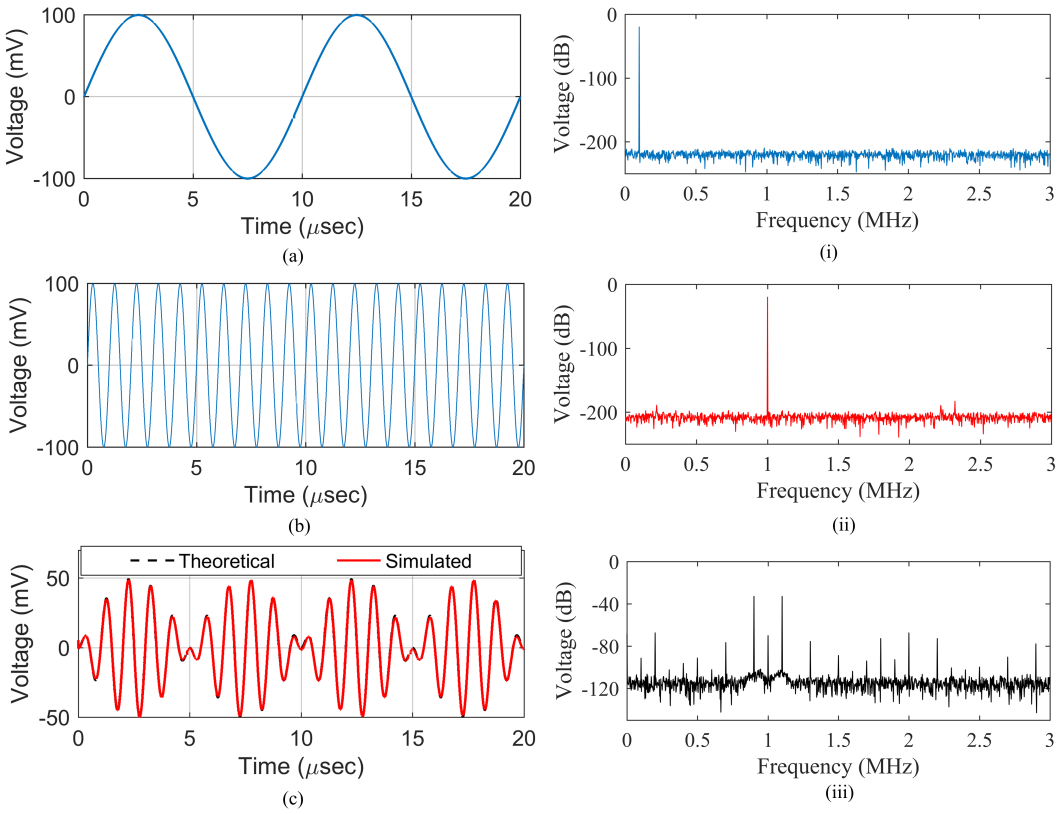
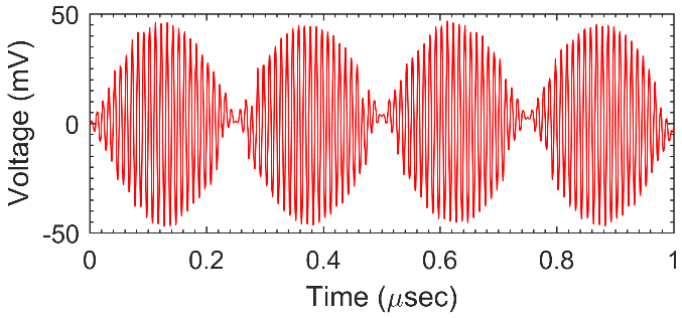
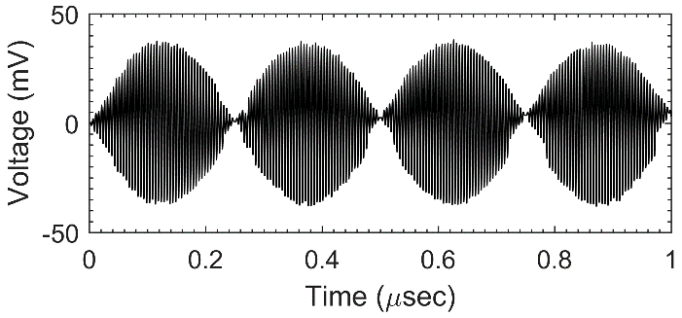


Figure 5.34: Transient input-output voltages of modulator circuit and their respective frequency spectrums



(a)

To evaluate the prefabrication performances of multiplier circuit such as process-voltage-temperature (PVT) analysis have also been carried out. The effect of different process corners i.e., slow slow (SS), slow fast (SF), fast slow (FS), fast fast (FF), and typical typical (TT) on the output of modulator circuit have been shown in Fig. 5.38a, whereas in Fig. 5.38b, the output voltage of modulator has been displayed with the presence of ±10% variations in bias voltage. The effect of temperature on



(b)

Figure 5.35: Simulated transient output voltage of modulator circuit at (a) 100 MHz and (b) 200 MHz

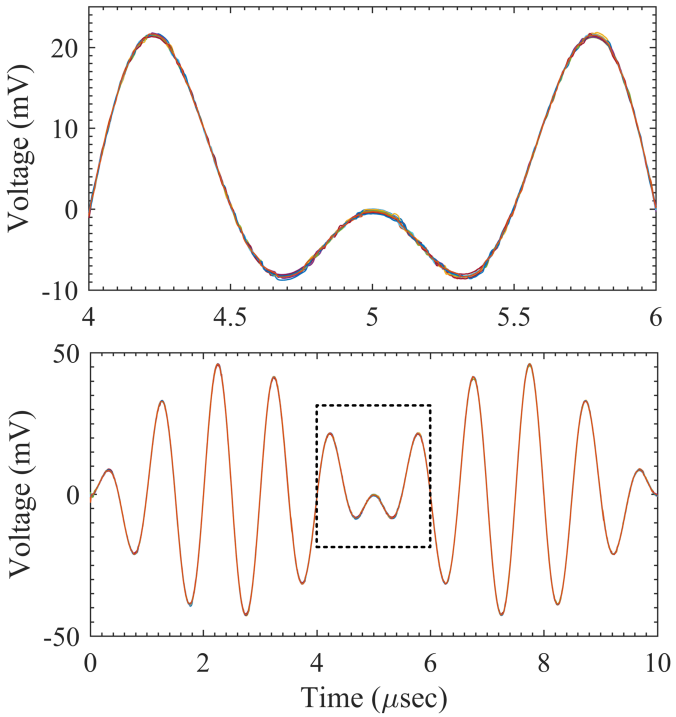
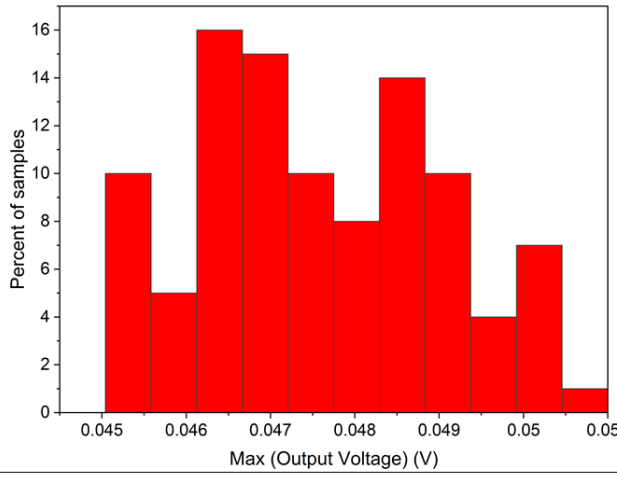


Figure 5.36: Output voltage of amplitude modulator with variation in aspect ratio of MOSFETs

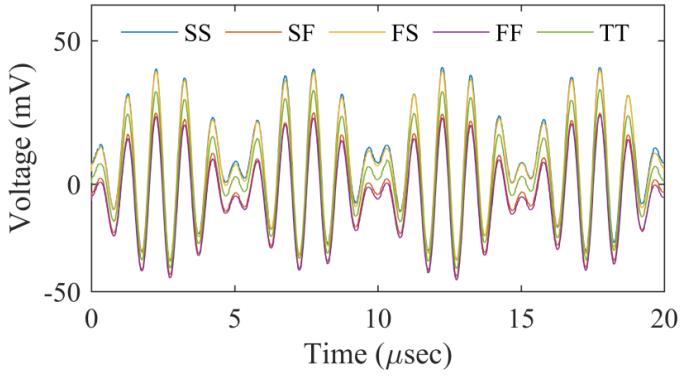
the output voltage of the amplitude modulator has also been evaluated at different temperatures (-10°C, 10°C, 20°C, 30°C) and the simulated results have been displayed in Fig. 5.38c. The effect of process corners, variations in bias voltage and change in temperature on the output of proposed multiplier circuit has been found to be very small.

We have also evaluated the noise performance of the modulator circuit using



n samples	=	100	10th %ile	=	0.046238
n divisions	=	10	median	=	0.0477604
mean	=	0.0475368	90th %ile	=	0.086631
sigma	=	0.000938927	maximum	=	0.0489792
minimum	=	0.0453873	3*sigma	=	0.00281678

Figure 5.37: Histogram of the amplitude modulator



(a)

PSPICE (V_1 -100mV, 100MHz, V_2 -100mV, 2MHz) and the result is shown in Fig. 5.39. The maximum output noise in the chosen frequency is found to be less than 70nV/sqrt(Hz).

(b) Frequency Doubler and Squarer Function

The circuit of Fig. 5.30 can also be configured as frequency doubler if input voltages $V_1 = V_2 = V_{in}$ and V_3 is taken as a constant voltage. With same inputs applied to the Fig. 5.30, the output obtained from this circuit is square of the input signal. To verify the results of frequency doubler and squarer circuits, the input voltage V_{in} was taken as a sinusoidal voltage of 1MHz with peak to peak amplitude of 200mV

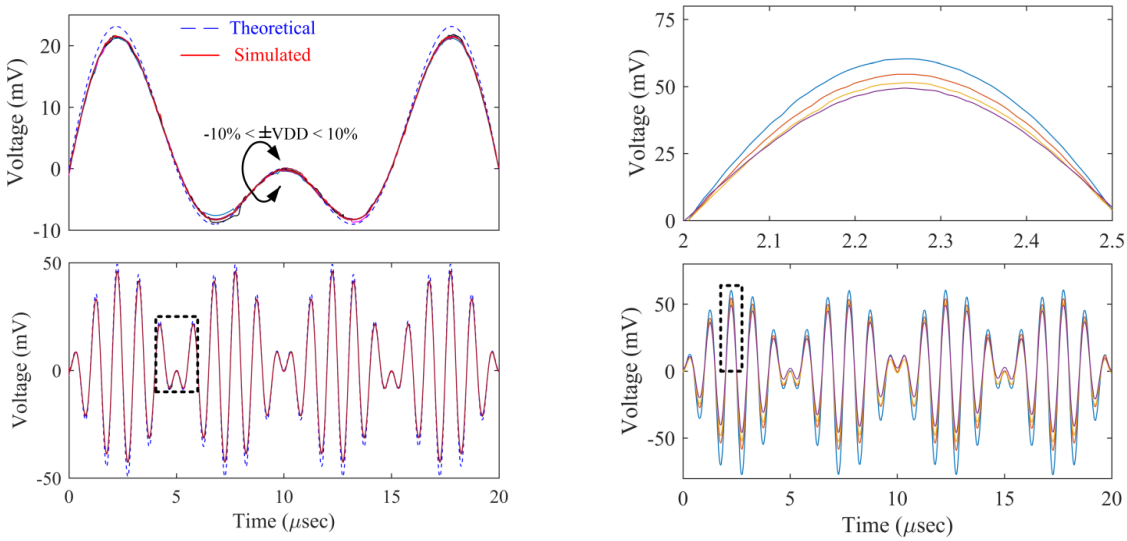


Figure 5.38: Output voltage of amplitude modulator corresponding to (a) process variations (b) supply voltage variations and (c) temperature variations

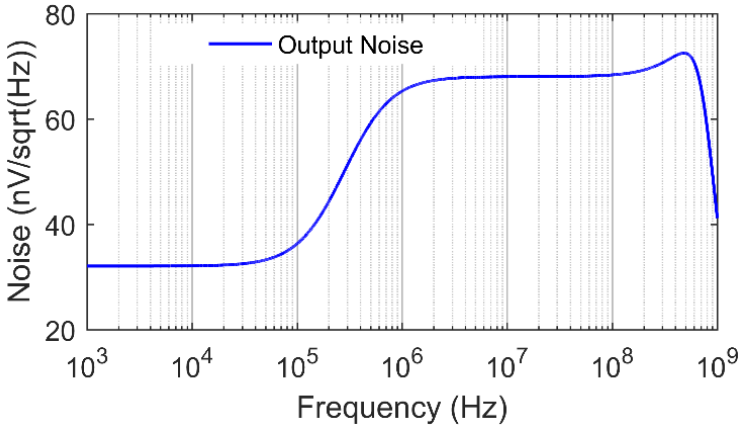


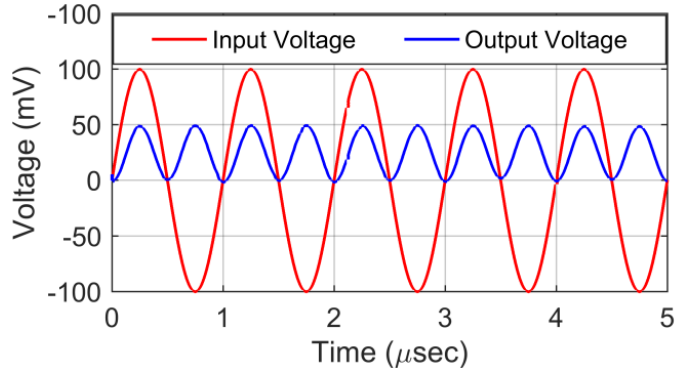
Figure 5.39: Output noise of amplitude modulator

and V_3 was also set to 200mV D.C. The transient input and output voltage have been displayed in Fig. 5.40a and the frequency spectrums have been depicted in Fig. 5.40b.

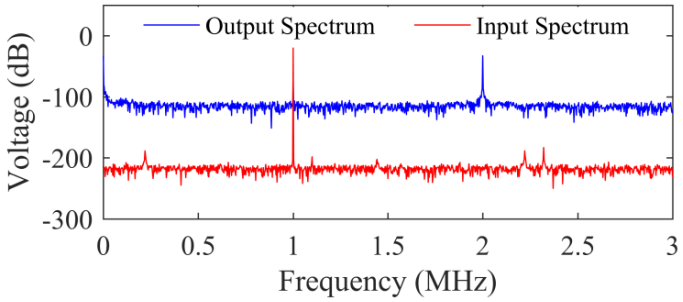
As shown in the frequency spectrum, the frequency of output voltage is double that of the input frequency.

5.7.2.3 Voltage Divider Mode

The transfer characteristics for the voltage division mode of operation were plotted by keeping the input voltage V_1 at 100mV and determining the output voltage vari-



(a)



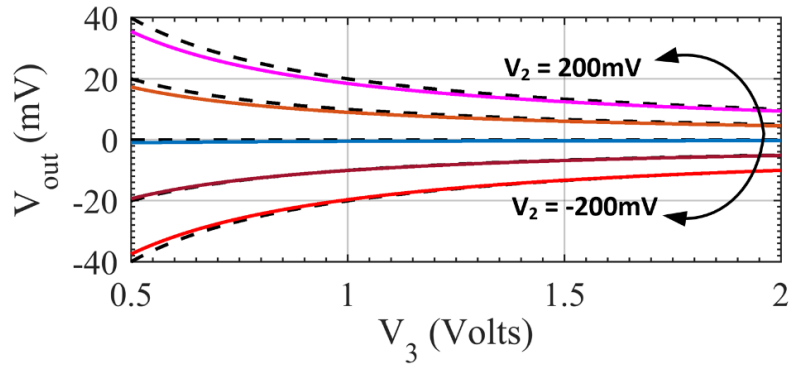
(b)

Figure 5.40: Transient input and output voltages of squarer circuit and its frequency spectrums

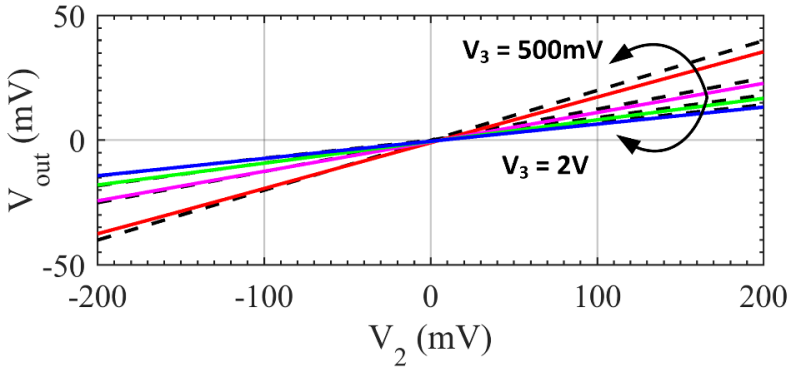
ation with V_2 and V_3. Fig. 5.41a shows the output voltage when the input voltage V_2 was varied from -200mV to +200mV in steps of 50mV, whereas the variation of output voltage with V_2 is shown in Fig. 5.41b when the input voltage V_3 is varied from 0.5 V to 2 V (dashed line-Theoretical, coloured line- Simulated).

We have also computed the error in output voltage, when V_2 was varied from -200mV to 200mV and V_3 was varied between 0.5 V to 2 V. Fig. 5.42 illustrates the error in output voltage of divider circuit. From the error graph, it may be observed that the percentage error in output voltage is quite low when V_3 increases gradually.

The time response of the divider circuit was tested by applying a triangular voltage of 400m V_{PP} (V_2) and 1.5 V_{PP} (V_3) at a frequency of 100kHz to both the inputs. The voltage V_1 was kept constant at 200mV (D.C.). The inputs and output of divider



(a)



(b)

Figure 5.41: DC response of analog divider circuit (a) when V_2 is varied (b) when V_3 is varied

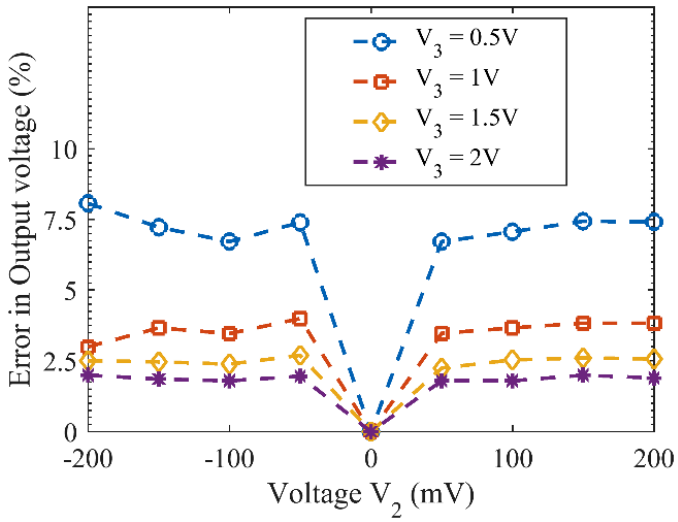
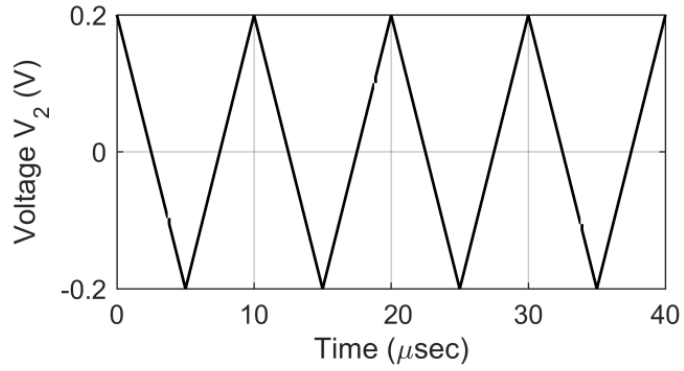


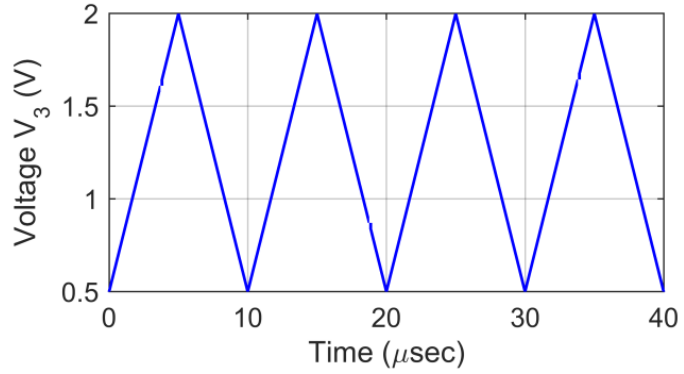
Figure 5.42: Error in output voltage of divider for different values of V_2 and V_3

circuit have been illustrated in Fig. 5.43.

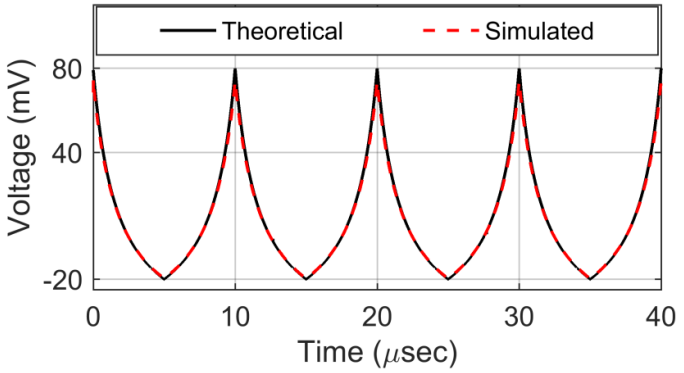
The AC response of the proposed circuit for division mode of operation has been simulated using PSPICE and illustrated in Fig. 5.44a. The -3dB bandwidth of the



(a)



(b)

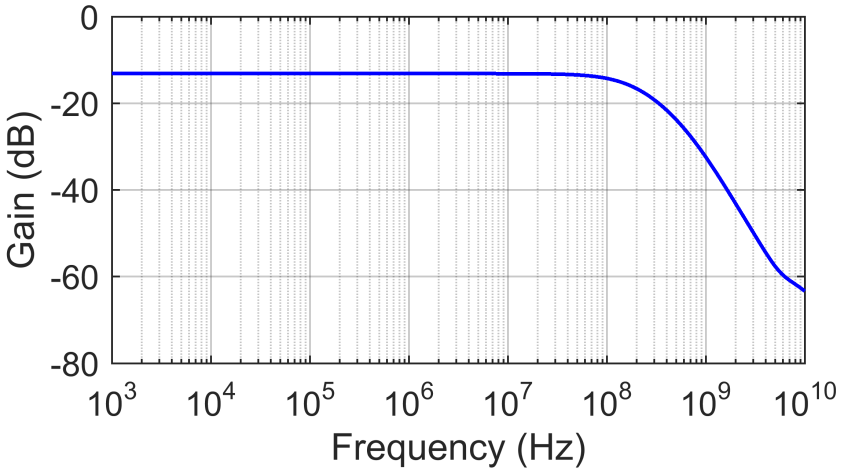


(c)

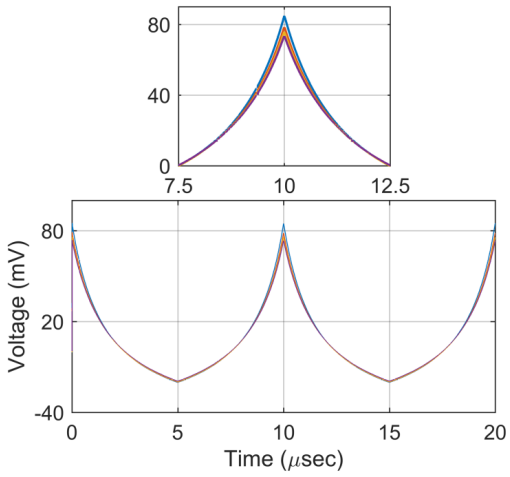
Figure 5.43: Time response of the circuit in division mode

divider circuit was found to be 182MHz approximately. The effect of temperature on divider circuit has also been evaluated for different temperatures between -10°C to 30°C and depicted in Fig. 5.44b. From Fig. 5.44b, it may be noted that the effect of temperature on divider circuit is quite low.

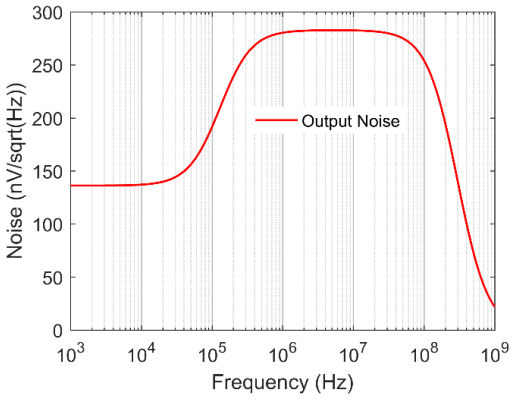
We have also carried out the noise analysis using PSPICE for the analog divider circuit and the simulation results have been shown in Fig. 5.44c. The maximum output noise measured for divider circuit is 280nV/sqrt(Hz).



(a)



(b)



(c)

Figure 5.44: (a) Frequency responses of proposed divider circuit (b) Variation in temperature on divider circuit (c) Output noise of analog divider circuit

5.8 Concluding Remarks

In this chapter, we have proposed new circuit realizations of analog multiplier, analog dividers and analog square root circuits employing single OTA and single CFOA.

The first proposed OTA based VM analog divider circuit employs an OTA and two MOSFETs (operating in triode region). The divider circuit has two quadrant mode of operation.The effect of mismatch in the thrsehold voltages of different MOSFETs, aspect ratio of different on the performance of the divider circuit have been determined analytically. We have also considered the effect of variation in the external DC power supply voltages on the output voltage of the circuit and proposed

a design in which these effects can be mimimized.Performance of the proposed circuit at high frequencies has also been evaluated. The presented divider circuit can also be used as analog inverse function generator in which the output voltage can be electronically controlled through transconductance of the OTA. A VM analog square root circuit with a single OTA and single MOSFET has also been proposed. Some application examples with simulation results have also been presented. The workability of the presented analog divider, inverse function and square root circuit has been verified using Cadence Virtuoso simulation tools with exemplary CMOS OTA implemented in 180nm technology parameters. Electronic tunabilty of the output voltage and satisfactory performance of the circuit under different operating temperatures of the proposed analog divider and square root circuits have been verified through simulations. Sample experimental results of square root circuit have also been demonstrated using off-the-shelf OTA IC LM13700 and CMOS transistor array HCF4007UBE.

As the last contribution in this chapter, a single CFOA based VM analog multiplier/divider circuit with four MOSFETs has also been proposed. Both the functions can be obtained from the same configuration without any structural change. The multiplier circuit has four quadrant operation whereas the divider circuit supports two quadrant operation. Application examples of analog multiplier circuit as amplitude modulator, frequency doubler and squarer have been presented.

The workability of the proposed analog multiplier/divider circuit has been verified using CMOS CFOA. Various analyses viz. mismatch analysis, PVT analysis, Monte-Carlo analysis have also been performed using PSpice simulations tool and included to support the theoretical propositions.

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Chapter 6

Conclusions and Future scope

6.1 Conclusions

In **Chapter 2**, we have presented single output OTA-based MISO type universal biquad filters. The first OTA-C universal biquad filter employs five OTAs and two grounded capacitors. The presented biquad filter configuration can provide all five generic filter functions by appropriate choice(s) of input voltages. The proposed filter circuit offers orthogonal electronic tunability of pole frequency and BW. Sensitivity of pole frequency with respect to transcondutors and capacitors has been evaluated and found to be less than half. However, this circuit requires an additional OTA (voltage inversion) to obtain LPF function. To overcome this limitation, we have also proposed two VM universal biquad filter circuits employing only four single output OTAs with two grounded capacitors. The presented circuits have orthogonal electronic tunability of pole frequency and pole quality factor. An exemplary CMOS OTA, implemented in 180nm TSMC technology parameters, has been used to validate the proposed biquad filter circuits. Simulation results such as frequency reponses, Monte-Carlo simulations and noise analysis using PSPICE have been performed to check the workability of the proposed circuits. We have also made the complete layout design for one of the presented circuits using Cadence Virtuoso simulations tool. Various checks such as design rule check, layout versus schematic check in analog design enviroment have been performed and the prelayout and post

layout simulation results have been pesented.

Finally, a mixed mode universal biquad filter employing five OTAs and two grounded capacitors has also been presented in this chapter. The mixed mode filter configuration realizes all five filter functions in all four modes i.e., voltage mode, current mode, transresistance mode, and transconductance mode. The proposed mixed mode universal filter circuit has orthogonal electronic tunability of pole frequency and BW while, the pole frequency and pole quality factor of the presented biquad filter circuit can be independently tuned through the transconductane of various OTAs. Non-ideal analyses have also been performed to determine the effect of parasitic on filter parameters. The active and passive sensitivities evaluated for this mixed mode biquad filter circuit are found to be not more than 1. Monte-Carlo analysis and noise analysis have also been carried out to check the robustness of the proposed filters. The workability of the proposed mixed mode filter configuration has been validated using Cadance Virtuoso simulations tool employing CMOS OTA achitecture and MATLAB simulations.

The main contributions made in **Chapter 3** can be summarized as follows:

Four new configurations of TOQSOs employing three OTAs and three capacitors have been presented. The CO and FO of the proposed TOQSO circuits have independent electronic control and also have quadrature output voltages and quadrature output currents. Out of the four TOQSOs, two circuits have capacitor control of FO, a feature, useful in capacitive transducers.

Finally, we have proposed two new TOQSOs using a systematic methodology (a closed loop circuit employing a second order LPF in a forward path and a lossless inverting integrator in the feedback loop) having fully decoupled control of CO and FO. The proposed circuits employ four OTAs and three grounded capacitors.

Non-ideal analysis, PSPICE simulations and experimental results for different circuits proposed in this chapter have been presented.

In **Chapter 4**, after classifying the realization methodologies of the previously proposed third order sinusoidal oscillator circuits, we have proposed three new approaches for systematic realization of third order sinusoidal oscillators (including minimal realization of low frequency third order sinusoidal oscillators). Two of the proposed approaches are based on the use of inverse filters while the third approach is network synthetic in nature.

The first approach using inverse filters, uses a first order inverse HPF in cascade with a conventional lossy and lossless integrator in a unity feedback loop to synthesize TOQSO circuit while, in the second approach, second order inverse HPF in cascade with a conventional lossless integrator in a unity feedback loop has been used. The realized circuits have independent control of CO and FO. Exemplary implementations of TOQSOs based on both the approaches using CFOAs have been presented. The network synthetic approach, on the other hand, is based on determination of the short-circuit admittance matrix of an autonomous three-port, whose characteristic equation represents the characteristic equation of a low frequency third order sinusoidal oscillator with independent control of CO and FO. Twelve matrices, out of which four matrices are distinct, have been derived using which third order low frequency sinusoidal oscillator circuits having independent control of CO and FO with different resistors employing canonic number of resistors (04) and grounded capacitors (03). Minimal realizations of low frequency third order sinusoidal oscillators employing three CFOAs, four resistors and three grounded capacitors have been presented to verify the theoretical propositions. Two of the proposed structures have quadrature relationship between output voltages. To establish the workability of all the proposed oscillator circuits, experimental results using off-the-shelf commercially available IC AD844 type CFOAs have been presented

In **chapter 5**, we have proposed new circuit realizations of analog divider, analog square root and analog multiplier/divider circuits employing single OTA and single CFOA.

The proposed OTA based VM analog divider circuit employs an OTA and two MOS-

FETs (operating in triode region). The divider circuit has two quadrant mode of operation.The effects of mismatch in the thrsehold voltages of different MOSFETs, aspect ratio of different on the performance of the divider circuit have been determined analytically. We have also considered the effect of variation in the external D.C. power supply voltage on the output voltage of the circuit and proposed a design using which these effects can be mimimized. Performance of the circuit at high frequencies has also been evaluated. The presented divider circuit can also be used as analog inverse function generator in which the output voltage can be electronically controlled through transconductance of the OTA. A VM analog square root circuit with a single OTA and single MOSFET has also been proposed. As the last contribution in this chapter, a single CFOA based VM analog multiplier/divider circuit with four MOSFETs has also been proposed. Both the functions can be obtained from the same configuration without any structural change. The multiplier circuit has four quadrant operation whereas the divider circuit supports two quadrant operation. Application examples of analog multiplier circuit as amplitude modulator, frequency doubler and squarer have been presented.

The workability of the proposed analog multiplier/divider circuit has been verified using CMOS CFOA. Various analyses viz. mismatch analysis, PVT analysis, Monte-Carlo analysis have also been performed using PSPICE simulation tool and included to support the theoretical propositions.

6.2 Future Scope

In this thesis, we have proposed several new circuits of analog active filters, third order sinusoidal oscillators and non linear function generators using operational transconductance amplifiers and the current feedback opeational amplifiers. But the class of the circuits reported can not be said to be exhausted completely.The work reported in this thesis can be extended in the following directions:

(i) Realization of voltage mode/mixed mode circuits with independent tunability of all the three parameters of the filters without any matching constraint

(ii) Realization of voltage mode/mixed mode circuits which employ minimum number of active and passive elements and provide independent tunability of all the three parameters of the filters

(iii) Minimal realization of third order sinusoidal oscillators employing CFOAs with grounded capacitors having independent control of CO and FO

(iv) Implementation of insensitive very low frequency third order sinusoidal oscillators with non-interacting control of CO and FO

(v) Realization of analog multiplier and divider circuit employing different active building blocks without any voltage matching conditions.

Author Biography

Ajishek Raj received his B.Tech degree in Electrical and Electronics Engineering from Dr. M.G.R. Educational and Research Institute, Chennai in 2012 and M.Tech degree from Delhi Technological University, Delhi in 2016. He has pursued Doctoral studies in the Department of Electrical Engineering at Delhi Technological University, Delhi. During the course of his research work, he has co-authored 08 research papers in various international journals and conferences of repute.

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