Technological Computer Aided Design and Simulation of Novel Ferroelectric-Dual Material Oxide Stack-Double Gate FET

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IN

PHYSICS

Submitted by

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CANDIDATE'S DECLARATION

I, **ISHA DAHIYA (2K19/MSCPHY/07)**, student of M.Sc. (Physics), hereby declare that the project Dissertation titled **"TECHNOLOGICAL COMPUTER AIDED DESIGN AND SIMULATION OF NOVEL FERROELECTRIC-DUAL MATERIAL OXIDE STACK-DOUBLE GATE FET"** which is submitted by me to the Department of Applied Physics, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Science, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

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CERTIFICATE

I hereby certify that the Project Dissertation titled **"TECHNOLOGICAL COMPUTER AIDED DESIGN AND SIMULATION OF NOVEL FERROELECTRIC-DUAL MATERIAL OXIDE STACK-DOUBLE GATE FET"** which is submitted by ISHA DAHIYA (2K19/MSCPHY/07) Department of Applied Physics, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Science, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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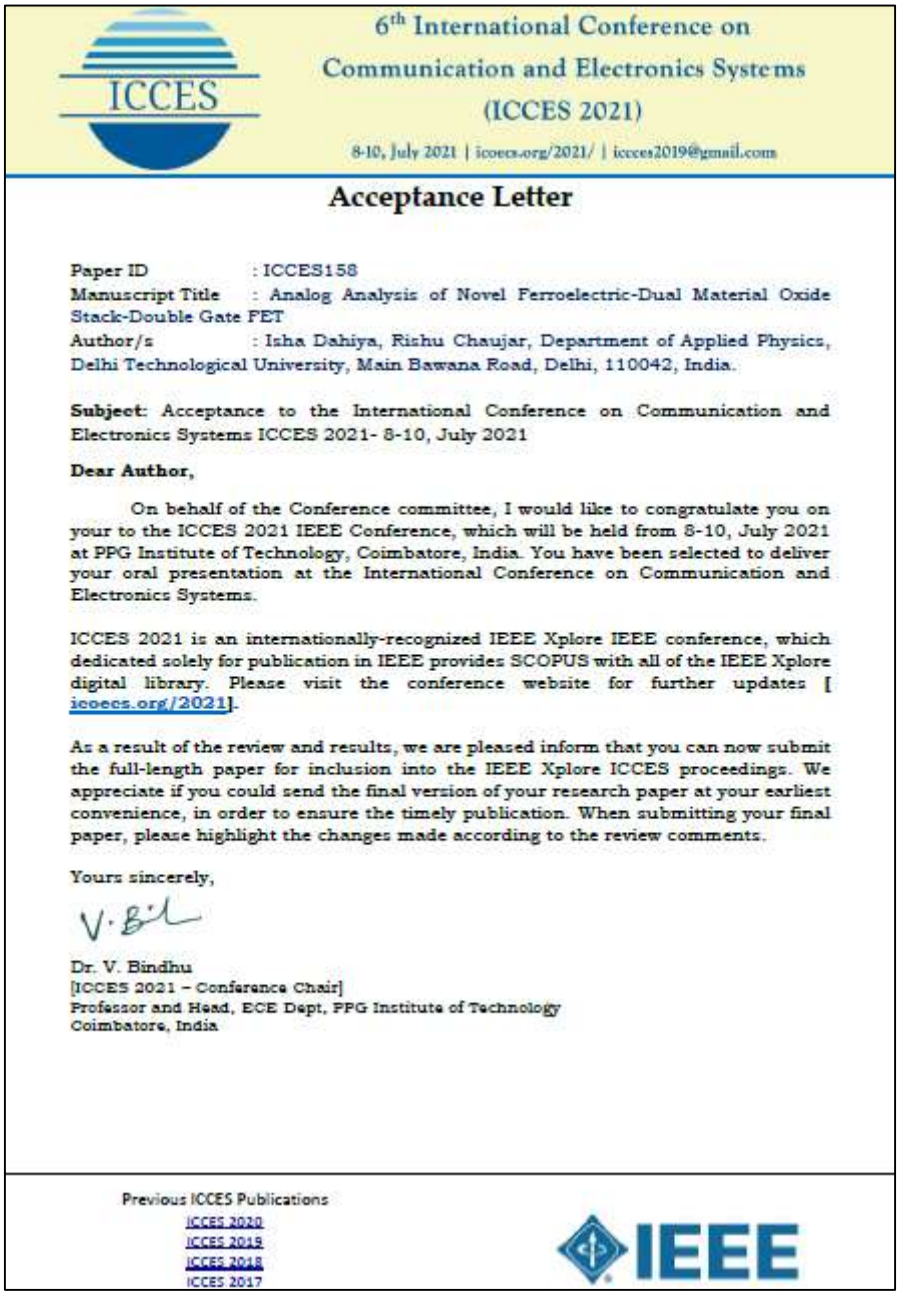
Acceptance Letter



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Acceptance Letter

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Subject: Acceptance to the International Conference on Communication and Electronics Systems ICCES 2021- 8-10, July 2021

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On behalf of the Conference committee, I would like to congratulate you on your to the ICCES 2021 IEEE Conference, which will be held from 8-10, July 2021 at PPG Institute of Technology, Coimbatore, India. You have been selected to deliver your oral presentation at the International Conference on Communication and Electronics Systems.

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ABSTRACT

In this work, the analog performance for Ferroelectric-Dual Material Oxide Stack-Double Gate FET (Fe-DMOS-DG FET) has been assessed and its effectiveness in reducing short channel effects (SCEs) has been analyzed. The derived parameters and results have been analysed in comparison with the conventional bulk MOSFET having same channel length. We are using gate metal comprising of two different materials to have better control over the channel. To reduce the injection of hot carriers, in one case we have used a ferroelectric layer on a thin SiO_2 interface layer, and in another case, we have used a ferroelectric layer on an oxide stack consisting of high k-dielectric and SiO_2 as gate insulator material. Parameters like ON current, OFF current, Id vs. Vg plot, Transconductance vs. Vg plot, threshold voltage, and value of sub-threshold slope are considered. It has been concluded that the new device has less subthreshold current, resulting in a lower subthreshold slope when compared to bulk MOSFET. Also, the electric field and carrier concentration along the channel are investigated, and it has been found that the novel device enhances carrier transport in the channel. The silvaco ATLAS device simulation software is used to do the numerical calculations in order to validate the results.

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List of Symbols, abbreviations and Nomenclature

CMOS	Complementary metal oxide semiconductor
CLM	Channel length modulation
MOSFET	Metal-oxide-semiconductor field effect transistor
DG	Double gate
SCE	Short channel effect
DM	Dual material
Fe-FET	Ferroelectric field effect transistor
Fe-DM-DG MOSFET	Ferroelectric-Dual Material-Double Gate MOSFET
Fe-DMOS-DG FET	Ferroelectric-Dual Material Oxide Stack-Double Gate FET
DIBL	Drain induced barrier lowering

1. Introduction

The continuous reduction of device size has allowed considerable technical advancement, resulting in denser, faster, and more practical integrated circuits. Developing devices that can perform massive computations while having a limited footprint (in terms of size) has been a significant motivator. Most of this has been made possible by the fact that the size of ordinary MOSFET has diminished by a magnitude of around 20 over the last two decades, and the MOS transistors that are being fabricated these days have a channel of length less than 100 nm. [1]. The elementary planar structure of the MOSFET has stayed mainly unaltered but its size has decreased by many orders of magnitude in the last three decades. These days the numbers of components/devices on an integrated circuit are increasing exponentially and the law that explains this trend is Moore's Law. Moore in 1965 predicted this trend and gave a law, according to which the number of transistors in an integrated circuit doubles after two years. This law seems to be applicable since then. In conventional MOSFET, short channel effects like injection of hot carriers into insulator layer, charge carriers' velocity saturation, drain induced barrier lowering (DIBL), carrier multiplication due to impact ionization hence causing various leakage currents and surface scattering have increased due to downscaling of the device. Therefore, the significant issue faced these days during transistor development is the reduction of short channel effects while improving the device's performance. For low-power and high-speed processes, the subthreshold swing and the DIBL should be as small as possible. However, at room temperature, the bulk MOSFET subthreshold swing has a theoretical limit of 60 mV/dec [11].

1.1 Motivation

Various alternatives, including the multiple-gate structure and advanced technologies such as gate oxide engineering, gate work function engineering, and so on, are being used these days to suppress short channel effects. [2]-[3]. Out of the various gate geometries, double gate geometry is the most promising. Two gates offer better controllability from both sides of the channel, subsequently resulting in stronger switching signals [4]. The short channel effect suppression capability of such a Dual Material Gate (DMG) design has been discovered to be very effective [5]. In gate workfunction engineering, the gate metal of appropriate work function is used in such a way that charge carriers are accelerated rapidly in the channel [2].

The material's workfunction at the source side is higher in a dual material gate configuration than the workfunction of the gate electrode near the source. Gate stack architecture is being incorporated to reduce high fringing fields and gate tunneling [9]. The most prominent motive in current literature and system design discussions is to improve switching speed and attain ultra-low power operation. The threshold voltage regulates the lower bound of the operating voltage, and in a traditional bulk MOSFET, lowering the threshold voltage increases the off-state current (Ioff), and hence the static power consumption [6]. To minimize power consumption, abrupt-turn-on devices are being extensively researched. Also, ferroelectric based insulator design is found to improve the short channel immunity in conventional dual metal gate device [13] and use of high-k dielectric as interfacial layer improves endurance and retention in FeFET devices during operation at lower switching voltages [14]. Hence, it is anticipated that the use ferroelectric as insulator in dual gate structure along with an interface layer will improve device performance as compared to conventional MOSFET structure.

1.2 Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)

MOSFET consists of two heavily doped regions, source and drain, separated by a mildly doped substrate. The schematic of n-MOSFET is represented in figure 1. The voltage applied to the gate terminal generates the channel by inversion of the semiconductor beneath the gate terminal. The distance between the source region and drain region is called channel length. Inside the transistor, two electric fields govern its operation: the vertical electric field generated due to applied gate voltage and lateral electric field because of source-to-drain voltage. A dielectric material is needed to insulate the gate contact from the conducting channel; generally, SiO_2 is used. Since flow of current is limited to 10-100 Å at the semiconductor's surface, the bulk of the semiconductor, known as the substrate, is usually inactive [1].

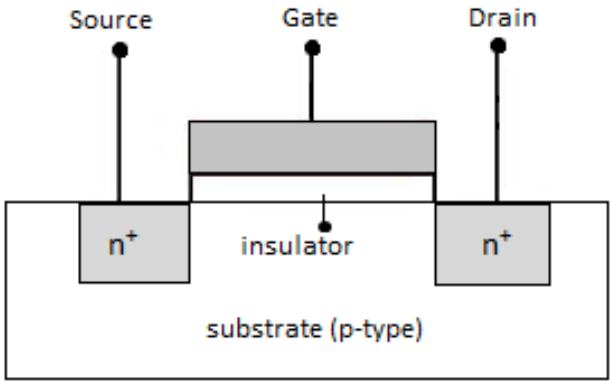

Figure 1. N-MOS structure

1.2.1 MOSFET Operation

The MOS transistor's operation is dependent on the MOS capacitor, which consists of gate metal contact, the substrate and the dielectric insulator that separates both of them. The applied voltage will induce charges in the metal and the counter charges in the interfacial layer of the semiconductor, as we would anticipate in the metal plates of a traditional parallel plate capacitor. The ability of the MOSFET to generate and modify a conducting layer consisting of minority carriers at the semiconductor–oxide interface is the fundamental of its operation. On applying voltage to the gate contact, charges are induced at the silicon-insulator interface in the semiconductor. For n-MOS transistor, p-type substrate is used, therefore on applying Vg>0, holes start moving away from the Si-Insulator interface, forming a depletion layer that consists of immovable negative charge carriers. On further increasing the gate voltage, the depletion layer reaches the substrate further, and for a particular gate voltage, i.e. for the threshold voltage, electrons start injecting from the source to the drain, hence forming a channel. For p-MOS transistor, channel formed is of holes for n-type substrate. According to the mode of operation, MOSFETs are categorized in two types.

1.2.2 Enhancement Mode

In enhancement-mode MOSFET, a conducting channel doesn’t exist in-between source and drain region when no voltage is given to the gate electrode. To induce the channel, a certain minimum gate voltage must be applied which will turn the device on.

1.2.3 Depletion Mode

In depletion-mode MOSFET, a conducting channel (inversion layer) is present even when no gate voltage has been applied. Threshold voltage in this case, will turn the device off.

1.3 Drawbacks and Limitations of Conventional MOSFETs

Conventional bulk MOSFETs have been a fundamental component for very large scale integration in semiconductor technology. However, as its size is reduced to nano-scale, various short channel effects poses a limitation on the size of the device. Due to the reduction of the MOS transistor's size, there is an appreciable gate-source and gate-drain overlap causing edge effects leading to an increase in longitudinal field, which was negligible compared to the perpendicular field in long channel transistor. Various parasitic capacitances also increases making the device unsustainable, consumes more energy along with increase in the time delay. Downscaling of MOSFET requires proper scaling of the gate length and width, thickness of oxide layer along with the other dimensions.

1.3.1 Short Channel Effects (SCEs)

In long channel MOSFET, electrostatics of the channel of device are controlled by gate electrode but in short channel MOSFET source and drain also appreciably controls the electrostatics of channel. Also, Drain current increases on decreasing the channel length which makes switching easier but this also decreases the threshold voltage to a greater extent.

1.3.2 Velocity Saturation

In short channel device, value of lateral electric field increases which leads to saturation of velocity for charge carriers at about 10^7 cm/sec. Consequently, the obtained value of device current is lesser than the drain current value expected from mobility model.

1.3.3 Drain Induced Barrier Lowering (DIBL)

This is a phenomenon in which threshold voltage is reduced for the applied high value of drain voltage (Vds). The potential barrier between the source region and channel in reduced as Vds is increased. DIBL is determined as |ΔVth|/|ΔVds| for Vds changing from 0.05V to 1.0V.

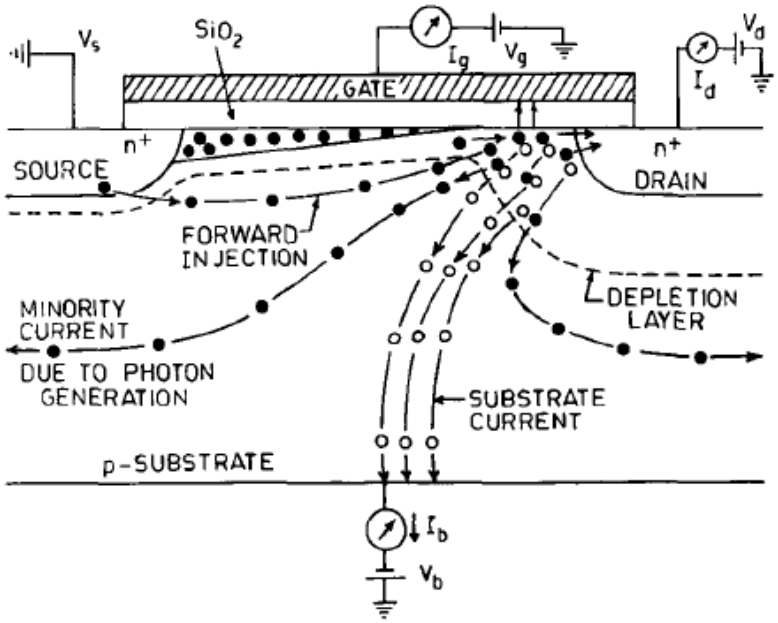

Figure 2. Representation of Hot carrier effects

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1.3.4 Surface Scattering

The inversion layer formed in the device is confined to a very narrow region in the silicon near the silicon-insulator interface. Due to the increased value of lateral electric field inside the channel of short channel MOSFET and also the electric field applied vertically, charge carriers experience collision among them while accelerating towards the drain region causing degradation of mobility. This is known as surface scattering which lead to reduction in drain current.

1.3.5 Hot Carrier Effects

In short channel device, value of electric increases in the channel regions causing the carriers to move at high velocity. This acquired high kinetic energy could cause impact ionization which ultimately leads to degradation of insulator layer causing gate leakage current. These

high energy charge carriers are called hot-carriers. These can also lead to undesirable substrate current.

1.4 Double Gate FETs

To overcome the shortcomings of the conventional MOSFET, double gate structure is found to be effective. Schematic of Double gate MOSFET is shown in figure 3. In this, the body is replaced by a back gate which reduces the leakage current and size is also reduced. Two gates offer better controllability from both sides of the channel, subsequently resulting in stronger switching signals. Operation of double gate MOSFET is similar to conventional MOSFET; the applied gate voltage forward biases the source-body junction hence causing the movement of carriers into the channel towards drain.

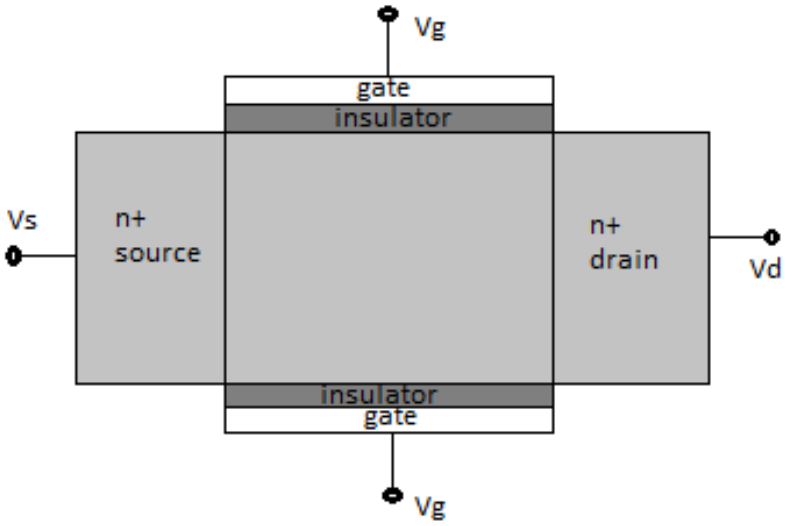

Figure 3. Schematic of Double gate MOSFET

1.4.1 Modifications in Double Gate Structure

Variations used in double gate FET structure include the use of Dual Metal or Triple Metal gate. By using gate material consisting of a combination of metal having different workfunction, we can have more control over the channel. Using a metal of higher workfunction near the source causes the carriers to move speedily in the channel; and to slow down the carriers near the drain, metal of lower workfunction is used for the gate. This reduces the injection of hot carriers in the insulator layer.

1.4.2 Problems with Double Gate FET structure

While dual gate FET structure improves device performance like increased drain current and transconductance, better short channel reliability; at the same time, the misalignment of two gates can degrade device performance as compared to single gate structure. Overlapping of any of gate electrode with source or drain can affect the device properties, as the overlapped part of source or drain is now controlled by the gate. The deviation from expected behaviour caused by the misalignment of gates can come from either the overlapped regions or non-overlapped regions. In this project, symmetric dual gate structure is considered.

1.5 Ferroelectric Field Effect Transistor

The main difference between ferroelectric FETs and MOSFETs is found in the gate stack of the device. MOSFETs have an insulating dielectric layer between the gate and the channel, typically SiO_2, whereas FeFETs use ferroelectric materials.

1.5.1 Ferroelectric materials

Ferroelectric materials are the material that becomes spontaneously polarized on application of electric field. All materials experience polarization on application of external electric field, which is proportional to the intensity of the applied field. However, ferroelectric dielectric crystals show a spontaneous electric polarization and have two stable polarized states, and polarization state can be reversed using electric field. These materials are ideal candidates for memory applications because of their switching efficiency. Digital bits, 0 or 1, are stored using the direction of spontaneous polarization, and the memory is non-volatile and electrically switchable. Typical hysteretic response of ferroelectric material is as shown figure 4. On the y-axis, the remnant polarization charges, denoted by PR+ and PR-, are shown, and on the x-axis, Ec+ and Ec- are marked, which represents the coercive fields.

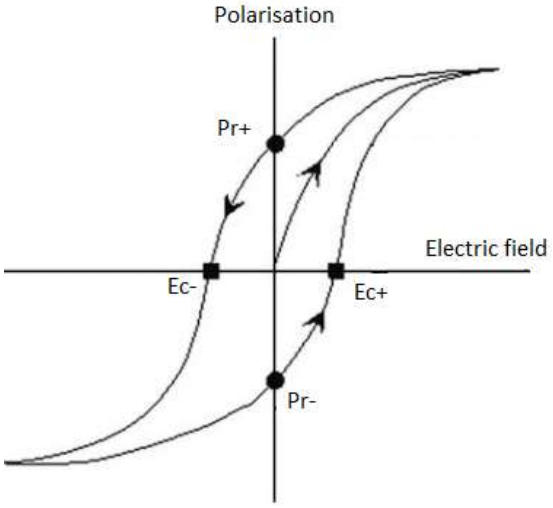

Figure 4. Hysteresis loop for ferroelectric material

1.5.2 FeFET device and operation

Ferroelectric films are currently being studied in order to achieve ultra-low power operation in devices that incorporate them. When doped with La, Sr, Si, Gd, Zr, Y, and Al, CMOS-compliant HfO_2-based films exhibit ferroelectric properties and are also lead-free [7]. Working of ferroelectric FETs is quite similar to MOSFETs', with the primary differences being in the device's gate stack. However, there are specific challenges in interfacing Si and ferroelectrics, like intermixing of the two layers, and regardless of the application, all Fe FETs experience a substantial field drop across the low-k interface layer, raising the power requirement for reversing the polarization while decreasing lifetime [8]. Several buffer layer configurations and alternative gate stack layouts have been using different combinations of metal, ferroelectric and dielectric insulator. However, the immediate deposition of ferroelectric layer over silicon is complicated due to the chemical reaction [10]. Therefore, to shrink the chip's size for artificial intelligence operation, combinations of an oxide layer, a thin ferroelectric material layer, a semiconductor and a fatigue-free electrode should be widely examined [10]. The approach to hysteresis-free FeFET architecture is aligning the positive capacitance of intrinsic MOSFET so as to stabilize the negative capacitance of ferroelectric; and experimentally ferroelectric-dielectric bilayer shows non-hysteretic electrical characteristics [12].

2 Simulation of MOSFET and FeFET in ATLAS software

There are various sub-packages in Silvaco for device simulation. They are DevEdit, ATHENA, ATLAS, DeckBuild, TonyPlot. Out of these ATALS is main device simulator and Tonyplot is used to plot the simulation results.

2.2 ATLAS overview

Simulation in ALTLAS is done through an input text file which is written in DeckBuild. The text file comprises information of all the parameters like doping, composition of different regions, biasing of electrodes and physical dimensions of the device. To create a structure, a mesh is defined; and solution of differential equations to find the values of all the required parameters is evaluated at these grid points also called nodes. Program is written in DeckBuild and after loading it in ATLAS, log file and structure files are generated. Sequence followed to write the program is given in the figure 5. The table 1 provides the sequence of commands to be followed in ATLAS.

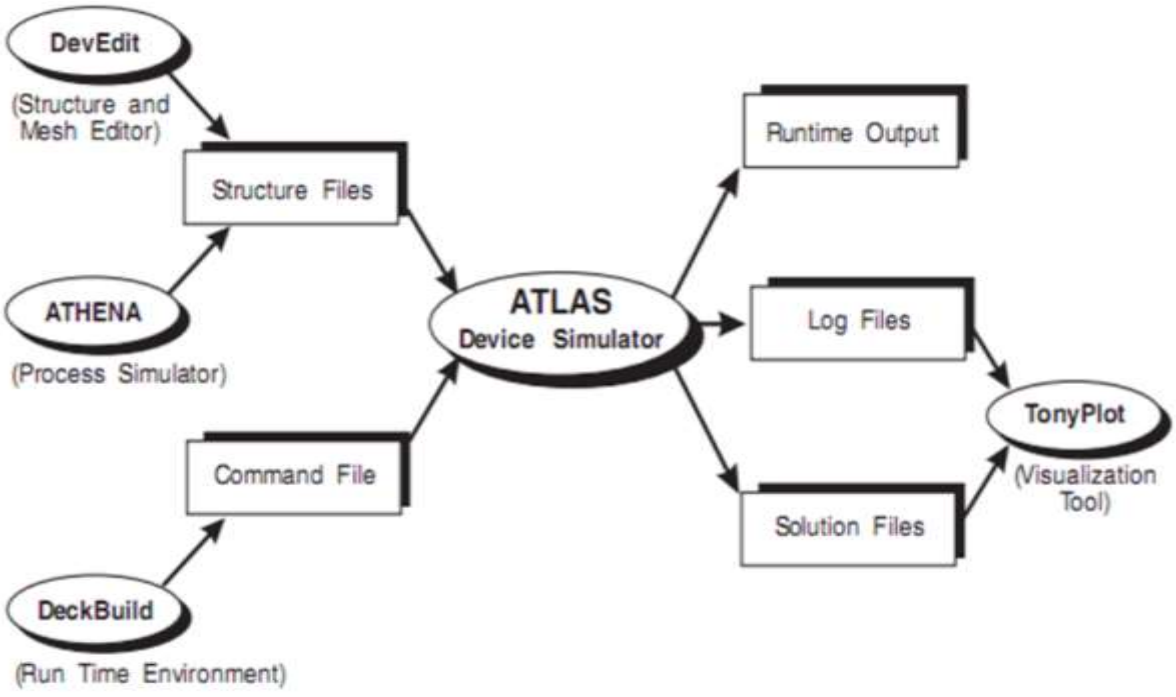

Figure 5. Simulation flow in ATLAS

Group	*Statements*
1. Structure Specification	MESH REGION ELECTRODE DOPING
2. Material Models Specification	MATERIAL MODELS CONTACT INTERFACE
3. Numerical Method Selection	METHOD
4. Solution Specification	LOG SOLVE LOAD SAVE
5. Results Analysis	EXTRACT TONYPLOT

Table 1. Order of commands in ATLAS

Types of input and output files for ATLAS :

a) Input files
- ATLAS commands written in text file
- structure file made in DevEdit or ATHENA

b) Output files
- After loading the input, a runtime time output window giving error warnings
- file storing information of current and voltages-log file
- files storing 2D and 3D output data - structure file

2.3 Device description

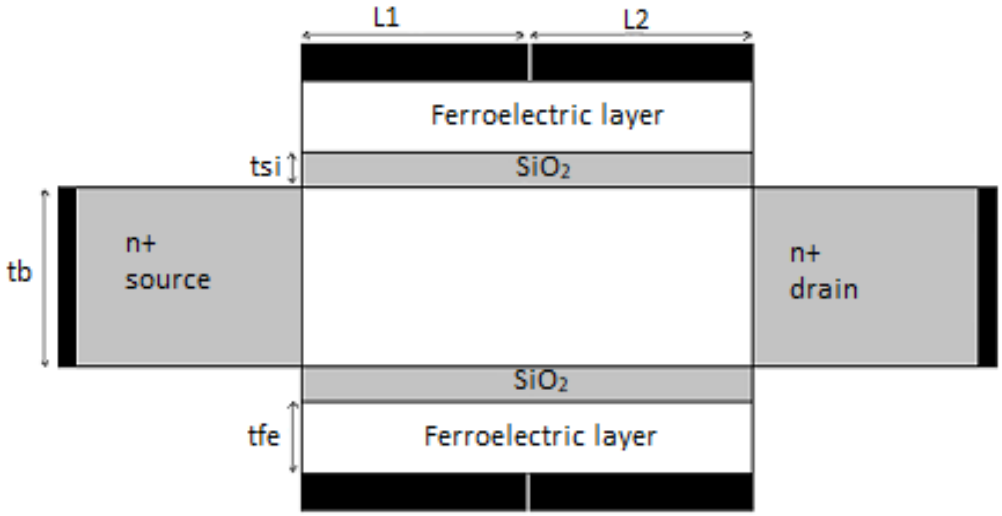

Figure 6. Schematic structure of Fe-DM-DG MOSFET

Figure 6 depicts a cross-sectional illustration of a Ferroelectric-Dual Material-Double Gate MOSFET with ferroelectric material as a gate insulator and SiO_2 as an interface layer. The overall purpose of using an interface layer is to minimize inter-diffusion between the ferroelectric layer and the semiconductor. The thickness assumed for the ferroelectric and SiO_2 layer is 4nm (tfe) and 2nm (tsi), respectively. The simulations are performed for top and bottom gate of length (L1 + L2) 80nm and each gate are divided into two equal parts. Workfunction of gate regions near the source is taken to be 4.8eV and for the parts near the drain, it's 4.4eV. The thickness of the substrate (tb) used is 10nm with uniform doping of 10^{18} cm^{-3}. The doping of source and drain regions is uniform and value is 10^{20} cm^{-3}.

For the conventional MOSFET, work function is 4.6eV for gate electrode; substrate thickness is 30nm and the parameters like channel length and source/drain doping are the same as above. Schematic of conventional MOSFET is represented in Figure 1.

Figure 7 shows the cross-sectional structure of Ferroelectric-Dual Material Oxide Stack-Double Gate FET (Fe-DMOS-DG FET). Except for the gate oxide, which consists of a 1.5nm high-k material layer (tk) with dielectric constant 25, on a 1.5nm thick SiO_2 layer of dielectric constant 3.9, all other parameters are the same as above for Ferroelectric-Dual Material Oxide Stack-Double Gate FET.

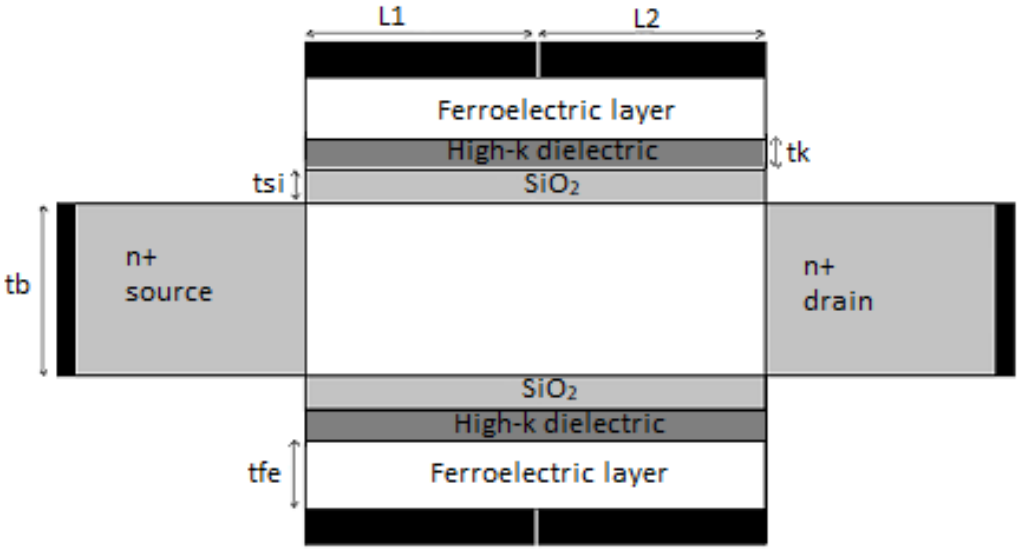

Figure 7. Schematic structure of Fe-DMOS-DG FET

3 Results

This section presents the performance analysis of Ferroelectric-Dual Material-Double Gate MOSFET (Fe-DM-DG MOSFET) and Ferroelectric-Dual Material Oxide Stack-Double Gate FET (Fe-DMOS-DG FET) in comparison with conventional MOSFET (C-MOSFET).

3.1 Transfer Characteristics

Figure 8 represents the transfer characteristics of the Fe-DM-DG MOSFET, Fe-DMOS-DG FET and C-MOSFET at Vds=0.5V. The threshold voltage for both the devices having ferroelectric material as gate insulator is higher as compared to the conventional MOSFET, which indicates the reduction of OFF state current.

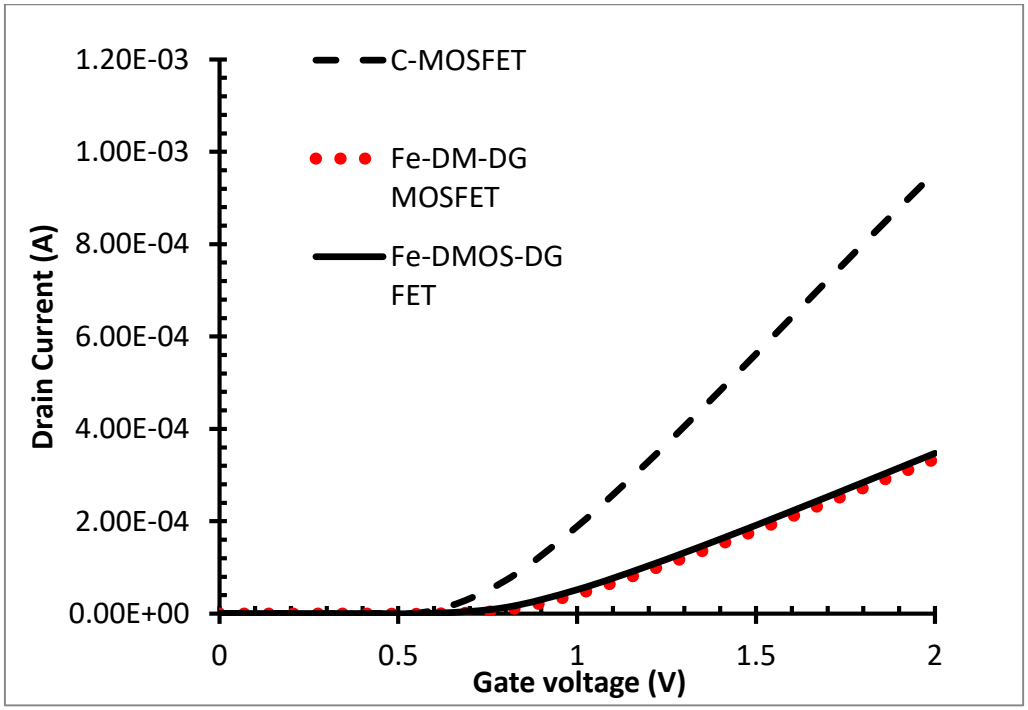

Figure 8. Drain Current vs. Gate Voltage (transfer characteristics) obtained for drain voltage=0.5V

3.2 Transconductance

Figure 9 shows transconductance vs. gate voltage plot for the three devices. Gate transconductance is expressed as the ratio of change in the output drain current to change in the applied gate voltage while maintaining the drain and substrate voltages constant. Transconductance is a crucial parameter since it evaluates device gain and controls device switching speed. Devices with high gain can operate at low gate voltages. From the figure, transconductance increases at lower gate voltage; at higher gate voltage, it starts decreasing for C-MOSFET, however for the Fe-DM-DG MOSFET and Fe-DMOS-DG FET transconductance becomes independent of the gate voltage.

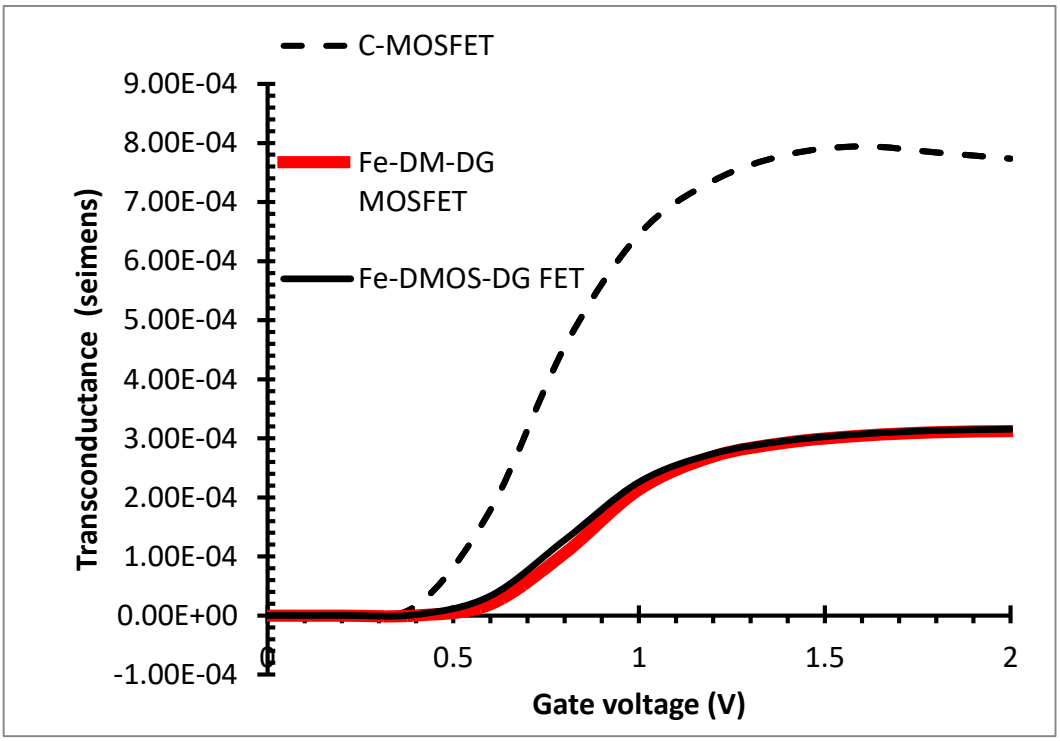

Figure 9. Transconductance vs. Gate voltage

3.3 Electrical Characteristics

Table 2 compares electrical characteristics of C-MOSFET, Fe-DM-DG MOSFET and Fe-DMOS-DG FET for drain voltage (Vds) equal to 0.5V. Fe-DM-DG MOSFET gives the lowest off-state current with highest ratio of Ion and Ioff. Both the ferroelectric devices have lower sub-threshold slope values than the conventional MOSFET; and threshold voltage increases implying better short channel immunity. However, a minimal increase in values of DIBL can be seen for both the new devices, which is defined as $|\Delta Vth|/|\Delta Vds|$. The values of Vth at Vds= 0.05V and 1.0V are taken to derive ΔVth in this study.

Model	**Sub-Threshold slope (V/dec)**	**Vth**	**Ion(Vg=1V)**	**Ioff(Vg=0V)**	**Ion/Ioff**	**DIBL**
C-MOSFET	0.0929308	0.541862	0.000189	3.56E-10	530834	0.473247
Fe-DM-DG MOSFET	0.0785244	0.679169	4.24E-05	6.01E-15	7.06E+09	0.494781
Fe-DMOS-DG FET	0.0853542	0.648264	5.17E-05	1.08E-13	4.79E+08	0.504489

Table 2. Electrical characteristics extracted at Vds=0.5V

3.4 Electric Field

From the figure 10, in C-MOSFET, the electric field in the channel is higher as compared to the Fe-DM-DG MOSFET and Fe-DMOS-DG FET. The high value of field towards the drain terminal of the device, which leads to pronounced hot carrier effects in conventional MOSFET, has been decreased with the introduction of a ferroelectric layer as gate insulator. No significant impact of introducing an oxide stack in place of the SiO_2 layer in Fe-DM-DG MOSFET is observed on the electric field variation along the channel.

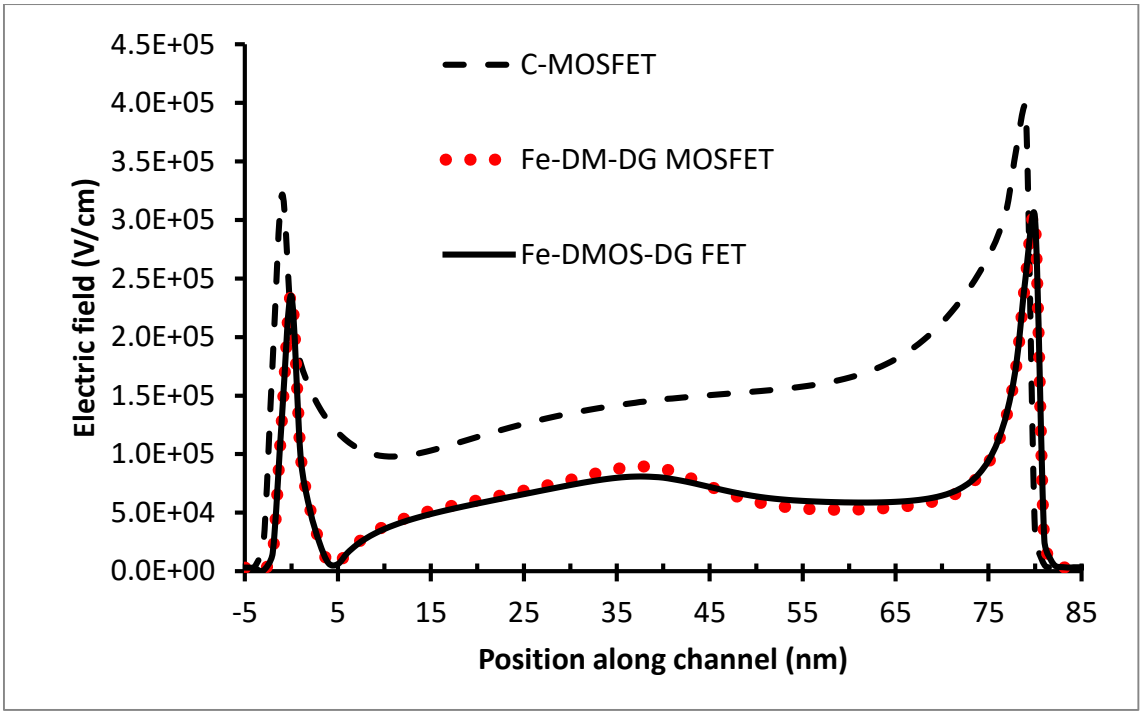

Figure 10. Variation of electric field along the channel for C-MOSFET, Fe-DM-DG MOSFET and Fe-DMOS-DG FET

3.5 Electron Concertation

From Figure 11, it is observed that the carriers are distributed non-uniformly in the C-MOSFET, which leads to mobility (μ) degradation, and the exact thickness of the conducting channel could be challenging to determine. Meanwhile, the gate controllability over the carriers in the channel would be reduced, and high carrier concentration towards the drain side could increase the hot carrier effects in the device. The introduction of ferroelectric layer has improved the electron density towards the source end, and the carrier concentration becomes more uniform along the channel compared to the C-MOSFET. However, variation of electron concentration is the same for Fe-DM-DG MOSFET and Fe-DMOS-DG FET.

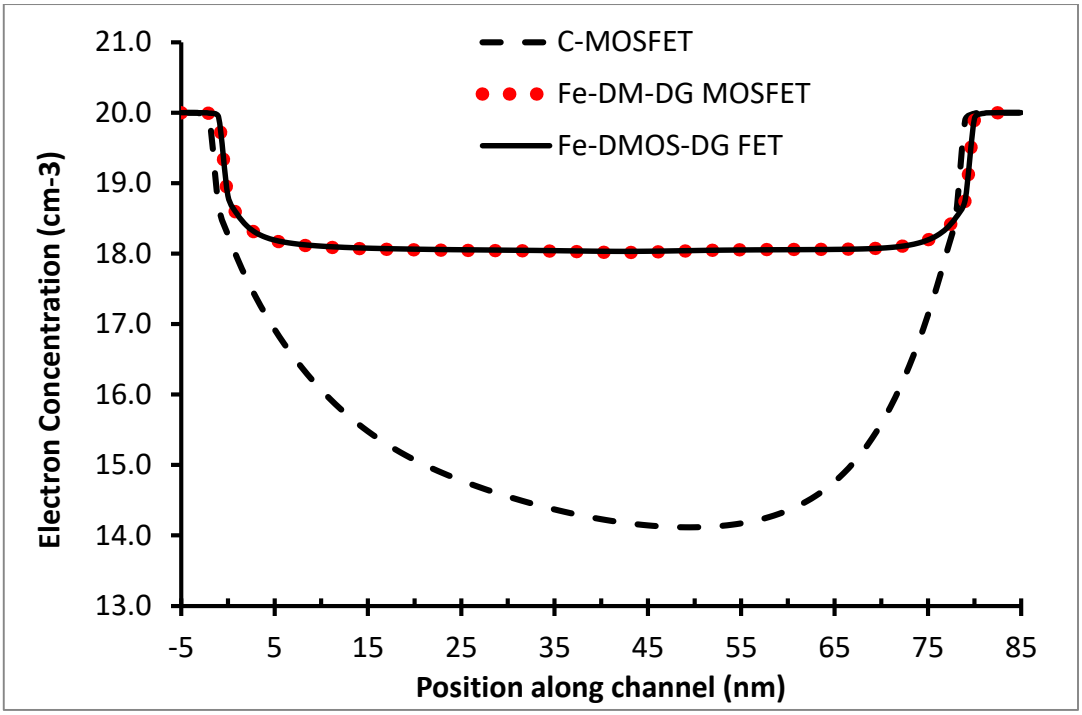

Figure11. Variation of electron concentration along the channel for C-MOSFET, Fe-DM-DG MOSFET and Fe-DMOS-DG FET

3.6 Potential

Figure 12 shows potential distribution along the channel for three of the devices. In C-MOSFET, there is a formation of potential well which spans whole of the channel length, whereas in both of the ferroelectric devices, a potential barrier near the source is formed because of negative capacitance effect of ferroelectric layer. The higher potential towards source in Fe-DM-DG MOSFET and Fe-DMOS-DG FET causes injection of carrier from the source into channel at higher speed as compared to C-MOSFET. This results in improved short channel immunity.

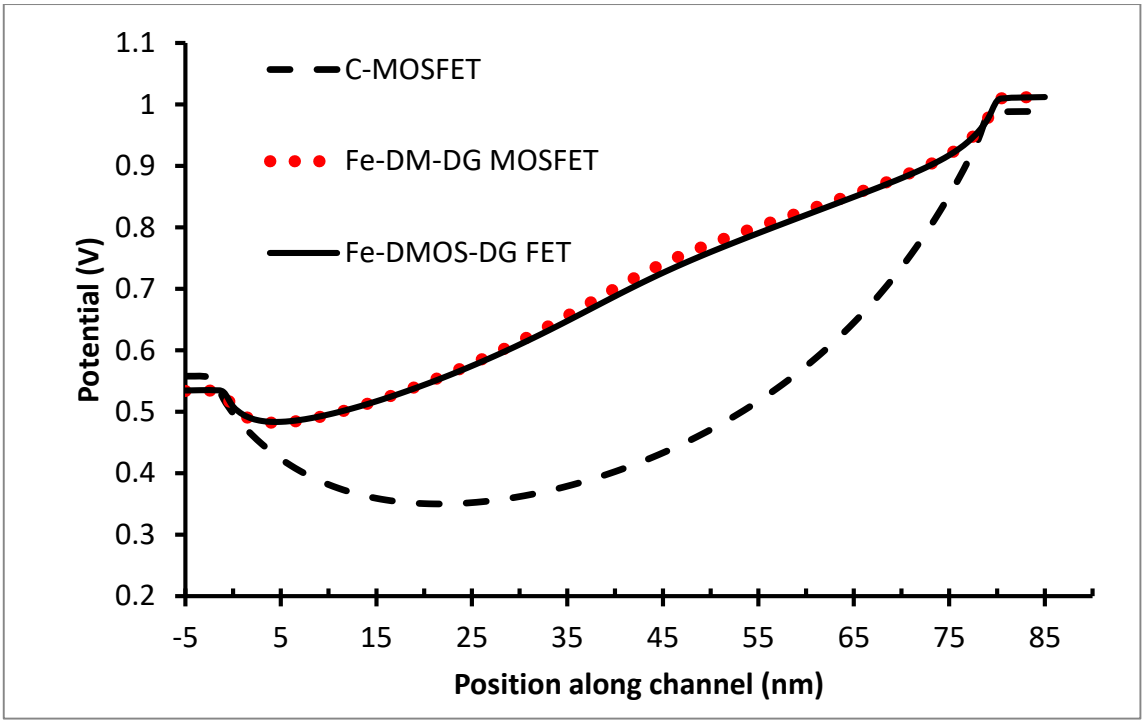

Figure 12. Variation of potential (V) along the channel

CONCLUSION

A 2-D analytical model for Ferroelectric-Dual Material-Double Gate MOSFET (Fe-DM-DG MOSFET) and Ferroelectric-Dual Material Oxide Stack-Double Gate FET (Fe-DMOS-DG FET) has been developed to diminish short-channel effects (SCEs) in nano-scale bulk MOSFETs, as well as to improve device reliability. Fe-DM-DG MOSFET improves nearly all of the parameters such as off current, sub-threshold slope, variation of carrier concentration along channel when compared to conventional short channel MOSFET; and is found to be effective for reduction of HCEs. Further, the parameters like variation of electric field, potential and carrier concentration along the channel obtained for Fe-DM-DG MOSFET and Fe-DMOS-DG FET are nearly identical. Thus, it has been illustrated that incorporating a ferroelectric layer along with the SiO_2 layer as insulator for dual metal gate electrode configuration improves hot carrier reliability and short channel immunity, resulting in improved performance and better carrier transport efficiency when compared to conventional bulk MOSFET design.

Dual Gate FETs have assuring future in VLSI and IC design as they have notably small structures. Other advantages include less power consumption, high reliability, and mostly nano-scale size, making them very valuable for CMOS circuits. Incorporating ferroelectric material and Dual Gate structure in FETs can provide promising results in fast programming, high ON/OFF ratio, low power dissipation, and other applications, which makes them suitable to be used as an electronics synapse.

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Analog Analysis of Novel Ferroelectric-Dual Material Oxide Stack-Double Gate FET

Isha Dahiya[1], Rishu Chaujar[2]
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***Abstract*—In this work, the analog performance for Ferroelectric-Dual Material Oxide Stack-Double Gate FET (Fe-DMOS-DG FET) has been assessed and its effectiveness in reducing short channel effects (SCEs) has been analyzed. The obtained results have been compared with the conventional MOSFET having the same channel length. We are using gate metal comprising of two different materials to have better control over the channel. To reduce the injection of hot carriers, in one case we have used a ferroelectric layer on a thin SiO_2 interface layer, and in another case, we have used a ferroelectric layer on an oxide stack consisting of high k-dielectric and SiO_2 as gate dielectric material. Parameters like ON current, OFF current, Ion/Ioff current ratio, Id vs. Vg plot, Transconductance vs. Vg plot, threshold voltage, and sub-threshold slope are considered. It has been recorded that the new device has less subthreshold current, resulting in a lower subthreshold slope when compared to bulk MOSFET. Also, the electric field and carrier concentration along the channel are investigated, and it has been found that the novel device enhances carrier transport in the channel. The silvaco ATLAS device simulation software is used to do the numerical calculations in order to validate the results.**

Keywords*— *Ferroelectric-Dual Material-Double Gate MOSFET (Fe-DM-DG MOSFET), Ferroelectric-Dual Material Oxide Stack-Double Gate FET (Fe-DMOS-DG FET), high k-dielectric, short channel effects.

I. INTRODUCTION AND BACKGROUND

The continuous reduction of device dimensions has enabled considerable technical advancement, resulting in denser, faster, and more practical integrated circuits. Developing devices that can perform massive computations while having a limited footprint (in terms of size) has been a significant motivator. Most of this has been made possible by the fact that the size of ordinary MOSFET has diminished by a magnitude of around 20 over the last two decades, and the MOS transistors that are being fabricated these days have a channel of length less than 100 nm. [1]. Due to the reduction of the MOS transistor's size, there is an appreciable gate-source and gate-drain overlap causing edge effects leading to an increase in longitudinal field, which was negligible compared to the perpendicular field in long channel transistor [1]. Furthermore, short channel effects like injection of hot carriers into the gate oxide, velocity saturation of carriers, drain induced barrier lowering (DIBL), carrier multiplication due to impact ionization hence causing various leakage currents and surface scattering have increased due to downscaling of MOSFET. Therefore, the significant issue faced these days during transistor development is the reduction of short channel effects while improving the device's performance. For low-power and high-speed processes, the subthreshold swing and the DIBL should be as small as possible. However, at room temperature, the conventional MOSFET subthreshold swing has a theoretical limit of 60 mV/dec [11].

Various alternatives, including the multiple-gate structure and advanced technologies such as gate oxide engineering, gate work function engineering, and so on, are being used these days to suppress short channel effects. [2]-[3]. Out of the various gate geometries, double gate geometry is the most promising. Two gates offer better controllability from both sides of the channel, subsequently resulting in stronger switching signals [4]. The short channel effect suppression capability of such a Dual Material Gate (DMG) design has been discovered to be very effective [5]. In gate workfunction engineering, the gate metal of appropriate work function is used in such a way that charge carriers are accelerated rapidly in the channel [2]. The workfunction of the material at the source side is higher in a dual material gate configuration than the workfunction of the gate electrode near the source. Gate stack architecture is being incorporated to reduce high fringing fields and gate tunneling [9]. The most prominent motive in current literature and system design discussions is to improve switching speed and attain ultra-low power operation. The threshold voltage regulates the lower bound of the operating voltage, and in a traditional bulk MOSFET, lowering the threshold voltage increases the off-state current (Ioff), and hence the static power consumption [6]. To minimize power consumption, abrupt-turn-on devices are being extensively researched.

A. Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)

MOSFET consists of two heavily doped regions, source and drain, separated by a moderately substrate. The structure of an n-MOSFET is represented in figure 1. The voltage applied to

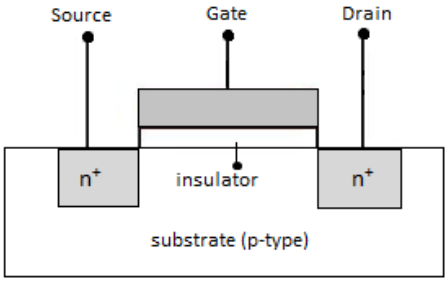

Figure 1. N-MOS structure

the gate terminal generates the channel by inversion of the semiconductor beneath the gate terminal. Inside the transistor, two electric fields govern its operation: the vertical electric field generated due to applied gate voltage and lateral electric field because of source-to-drain voltage. A dielectric material is needed to insulate the gate contact from the conducting channel; generally, SiO_2 is used. Since flow of current is limited to 10-100 Å at the semiconductor's surface, the bulk of the semiconductor, known as the substrate, is usually inactive [1].

The MOS transistor's operation is dependent on the MOS capacitor, which consists of gate metal contact, the substrate and the dielectric insulator that separates both of them. On applying voltage to the gate contact, charges are induced at the silicon-insulator interface in the semiconductor. For n-MOS transistor, the substrate is of p-type, therefore on applying Vg>0, holes start moving away from the Si-Insulator interface, forming a depletion layer that consists of immovable negative charge carriers. On further increasing the gate voltage, the depletion layer reaches the substrate further, and for a particular gate voltage, i.e. for the threshold voltage, electrons start injecting from the source to the drain, hence forming a channel.

B. Ferroelectric materials and FeFETs

Ferroelectric films are currently being studied in order to achieve ultra-low power operation in devices that incorporate them. All materials experience polarization in the presence of external electric field, which is proportional to the intensity of the applied field. However, ferroelectric dielectric crystals show a spontaneous electric polarization and have two stable polarized states, and an external electric field may be used to change the direction of polarization. These materials are ideal candidates for memory applications because of their switching efficiency. Digital bits, 0 or 1, are stored using the direction of spontaneous polarization, and the memory is non-volatile and electrically switchable. Typical hysteretic response of ferroelectric material is as shown figure 2. On the y-axis, the remnant polarization charges, denoted by PR+ and PR-, are

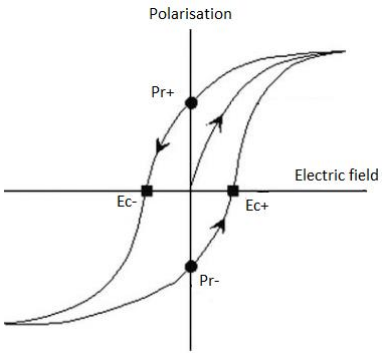

Figure 2. Hysteresis loop for ferroelectric material

shown, and on the x-axis, Ec+ and Ec- are marked, which represents the coercive fields.

The main difference between ferroelectric FETs and MOSFETs is found in the gate stack of the device. MOSFETs have an insulating dielectric layer between the gate and the channel, typically SiO_2, whereas FeFETs use ferroelectric materials. When doped with La, Sr, Si, Gd, Zr, Y, and Al, CMOS-compliant HfO_2-based films exhibit ferroelectric properties and are also lead-free [7]. However, there are specific challenges in interfacing Si and ferroelectrics, like intermixing of the two layers, and regardless of the application, all Fe FETs experience a substantial field drop across the low-k interface layer, which raises the power required for polarization reversal while decreasing lifetime [8]. Several buffer layer configurations and alternative gate stack layouts have been developed, like metal-ferroelectric-insulator-metal (MFIM), metal-ferroelectric-silicon (MFS), metal-ferroelectric-metal (MFM), and metal-ferroelectric-insulator-silicon (MFIS). The MFS structure is preferred to reduce the device's operating voltage; however, the immediate deposition of ferroelectric layer over silicon is complicated due to the chemical reaction [10]. Therefore, to shrink the chip's size for artificial intelligence operation, combinations of an oxide, a semiconductor, a thin ferroelectric material layer, and a fatigue-free electrode should be widely examined [10]. The approach to hysteresis-free FeFET architecture is aligning the positive capacitance of intrinsic MOSFET so as to stabilize the negative capacitance of ferroelectric; and experimentally ferroelectric-dielectric bilayer shows non-hysteretic electrical characteristics [12]. Also, ferroelectric based insulator design is found to improve the short channel immunity in conventional dual metal gate device [13] and use of high-k dielectric as interfacial layer improves endurance and retention in FeFET devices during operation at lower switching voltages [14]. Hence, it is anticipated that the use ferroelectric as insulator in dual gate structure along with an interface layer will improve device performance as compared to conventional MOSFET structure.

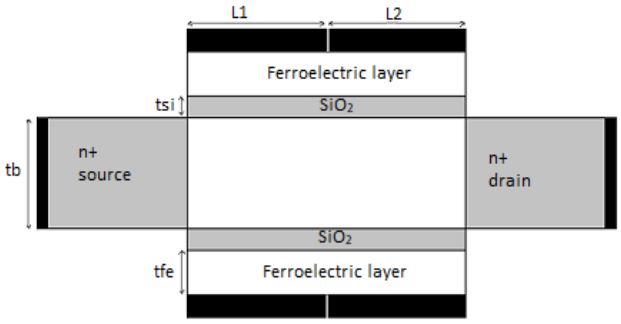

Figure 3. Schematic structure of Fe-DM-DG MOSFET

Device Description

Figure 3 depicts a cross-sectional illustration of a Ferroelectric-Dual Material-Double Gate MOSFET with ferroelectric material as a gate insulator and SiO_2 as an interface layer. The overall purpose of using an interface layer is to minimize inter-diffusion between the ferroelectric layer and the semiconductor. The thickness assumed for the ferroelectric and SiO_2 layer is 4nm (tfe) and 2nm (tsi), respectively. The simulations are performed for top and bottom gate of length (L1 + L2) 80nm and each gate are divided into two equal parts. Workfunction of gate regions near the source is taken to be 4.8eV and for the parts near the drain, it's 4.4eV. The thickness of the substrate (tb) used is 10nm with uniform doping of 10^{18} cm^{-3} and the source and drain regions have uniform doping of 10^{20} cm^{-3}. Figure 4 shows the cross-sectional structure of Ferroelectric-Dual Material Oxide Stack-Double Gate FET (Fe-DMOS-DG FET). Except for the gate oxide, which consists of a 1.5nm high-k material layer (tk) with dielectric constant 25, on a 1.5nm thick SiO_2 layer of dielectric constant 3.9, all other parameters are the same as above for Ferroelectric-Dual Material Oxide Stack-Double Gate FET. For the conventional MOSFET, work function of gate is taken to be equal to 4.6eV; substrate thickness is 30nm and the parameters like channel length and source/drain doping are the same as above.

To perform 2D numerical device simulation, mobility and recombination models included are standard concentration dependent mobility, Auger recombination model, Shockley-Read-Hall recombination with fixed carrier lifetimes, Bandgap Narrowing and parallel field mobility. For device simulation of FeFet devices, the Ferro model is incorporated to define the ferroelectric material [16].

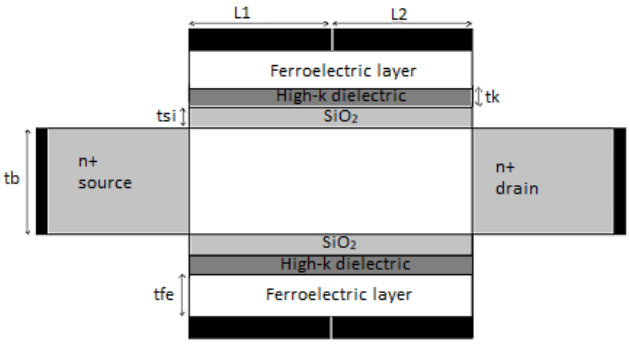

Figure 4. Schematic structure of Fe-DMOS-DG FET

II. Results and Discussion

This section presents the performance analysis of Ferroelectric-Dual Material-Double Gate MOSFET (Fe-DM-DG MOSFET) and Ferroelectric-Dual Material Oxide Stack-Double Gate FET (Fe-DMOS-DG FET) in comparison with conventional MOSFET (C-MOSFET). Figure 5 represents the transfer characteristics of the Fe-DM-DG MOSFET, Fe-DMOS-DG FET and C-MOSFET at Vds=0.5V. It can be seen that the threshold voltage for both the devices having ferroelectric material as gate insulator is higher as compared to the conventional MOSFET, which indicates the reduction of OFF state current.

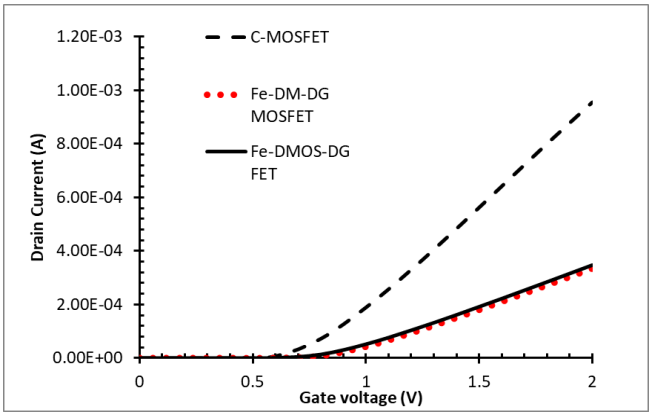

Figure 5. Drain Current vs. Gate Voltage (transfer characteristics) obtained for drain voltage=0.5V

Figure 6 shows transconductance vs. gate voltage plot for the three devices. Gate transconductance is expressed as the ratio of change in the output drain current to change in the applied gate voltage while maintaining the drain and substrate voltages constant. Transconductance is a crucial parameter since it evaluates device gain and controls device switching speed. Devices with high gain can operate at low gate voltages. The electric field in the channel increases as the device channel length decreases, resulting in velocity saturation of charge carriers, thereby limiting device current and transconductance. From the figure, transconductance increases at lower gate voltage; at higher gate voltage, it starts decreasing for C-MOSFET, however for the Fe-DM-DG MOSFET and Fe-DMOS-DG FET transconductance becomes independent of the gate voltage.

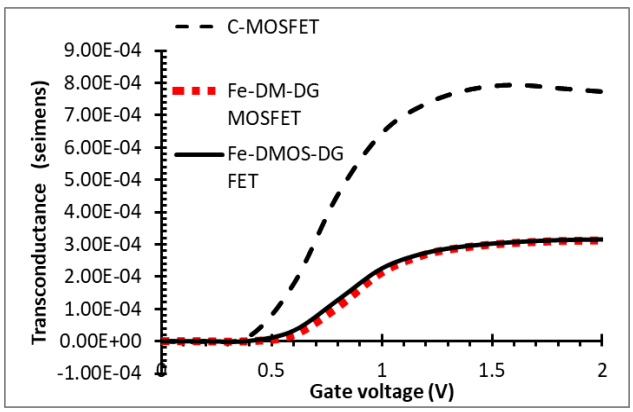

Figure 6. Transconductance vs. Gate voltage

Table 1. Electrical characteristics extracted at Vds=0.5V

Model	Sub-Threshold slope (V/dec)	Vth	Ion(Vg=1V)	Ioff(Vg=0V)	Ion/Ioff	DIBL
C-MOSFET	0.0929308	0.541862	0.000189	3.56E-10	530834	0.473247
Fe-DM-DG MOSFET	0.0785244	0.679169	4.24E-05	6.01E-15	7.06E+09	0.494781
Fe-DMOS-DG FET	0.0853542	0.648264	5.17E-05	1.08E-13	4.79E+08	0.504489

Table 1 compares electrical characteristics of C-MOSFET, Fe-DM-DG MOSFET and Fe-DMOS-DG FET for drain voltage (Vds) equal to 0.5V. The electrical features extracted are sub-threshold slope, threshold voltage (Vth), on and off current, the ratio of Ion and Ioff and DIBL. Fe-DM-DG MOSFET gives the lowest off-state current with highest ratio of Ion and Ioff. Both the ferroelectric devices have lower sub-threshold slope values than the conventional MOSFET; and threshold voltage increases implying better short channel immunity. However, a minimal increase in values of DIBL can be seen for both the new devices, which is defined as $|\Delta Vth|/|\Delta Vds|$. The values of Vth at Vds= 0.05V and 1.0V are taken to derive ΔVth in this study.

Figure 7 shows the variation of electric field in the channel for C-MOSFET, Fe-DM-DG MOSFET and Fe-DMOS-DG FET. The reduction of channel length leads to various leakage currents due to the high electric field in the channel. It can be seen that the electric field along the channel in C-MOSFET is higher as compared to the Fe-DM-DG MOSFET and Fe-DMOS-DG FET. The high value of field towards the drain terminal of the device, which leads to pronounced hot carrier effects in conventional MOSFET, has been decreased with the introduction of a ferroelectric layer as gate insulator. No significant impact of introducing an oxide stack in place of the SiO_2 layer in Fe-DM-DG MOSFET is observed on the electric field variation along the channel.

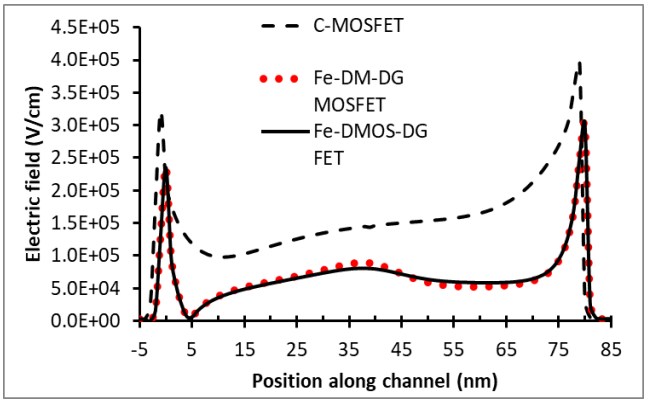

Figure 7. Variation of electric field along the channel for C-MOSFET, Fe-DM-DG MOSFET and Fe-DMOS-DG FET

Figure 8 compares the variation of electron concentration along the channel for all three devices. It is observed that the carriers are distributed non-uniformly in the C-MOSFET, which leads to mobility (μ) degradation, and the exact thickness of the conducting channel could be challenging to determine. Meanwhile, the gate controllability over the carriers in the channel would be reduced, and high carrier

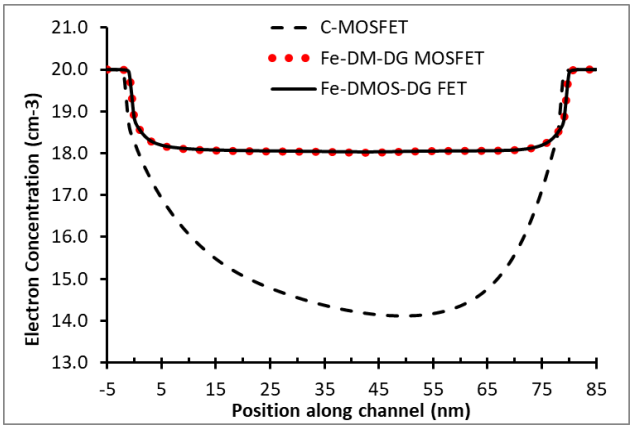

Figure 8. Variation of electron concentration along the channel for C-MOSFET, Fe-DM-DG MOSFET and Fe-DMOS-DG FET

concentration towards the drain side could increase the hot carrier effects in the device. The introduction of ferroelectric layer has improved the electron density towards the source end, and the carrier concentration becomes more uniform along the channel compared to the C-MOSFET. However, variation of electron concentration is the same for Fe-DM-DG MOSFET and Fe-DMOS-DG FET.

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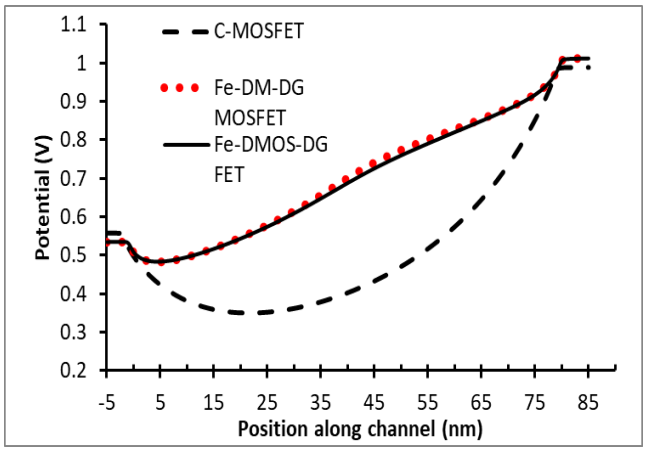

Figure 9. Variation of potential (V) along the channel

effect of ferroelectric layer. The higher potential towards source in Fe-DM-DG MOSFET and Fe-DMOS-DG FET causes injection of carrier from the source into channel at higher speed as compared to C-MOSFET. This results in improved short channel immunity.

III. Conclusion

A two-dimensional analytical model for Ferroelectric-Dual Material-Double Gate MOSFET (Fe-DM-DG MOSFET) and Ferroelectric-Dual Material Oxide Stack-Double Gate FET (Fe-DMOS-DG FET) has been developed to diminish short-channel effects (SCEs) and hot carrier effects (HCEs) in nano-scale bulk MOSFETs, as well as to improve device reliability. Fe-DM-DG MOSFET improves nearly all of the parameters such as off current, sub-threshold slope, variation of carrier concentration along channel when compared to conventional short channel MOSFET; and is found to be effective for reduction of HCEs. Further, the parameters like variation of electric field, potential and carrier concentration along the channel obtained for Fe-DM-DG MOSFET and Fe-DMOS-DG FET are nearly identical. Thus, it has been illustrated that incorporating a ferroelectric layer along with the SiO_2 layer as insulator for dual metal gate electrode configuration improves hot carrier reliability and short channel immunity, resulting in improved performance and better carrier transport efficiency when compared to conventional bulk MOSFET design.

Dual Gate FETs have assuring future in VLSI and IC design as they have notably small structures. Other advantages include less power consumption, high reliability, and mostly nano-scale size, making them very valuable for CMOS circuits. Incorporating ferroelectric material and Dual Gate structure in FETs can provide promising results in fast programming, high ON/OFF ratio, low power dissipation, and other applications, which makes them suitable to be used as an electronics synapse.

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