M. Tech (Power System)

GRID INTEGRATION OF PV-STATCOM USING FIVE LEVEL MULTILEVEL INVERTER

A DISSERTATION

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Submitted by:

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I, ALLU BHARGAV, Roll No. 2K17/PSY/02 student of M.Tech. (Power System), hereby declare that the project Dissertation titled "Grid Integration of PV-STATCOM using Five Level Multilevel Inverter" which is submitted by me to the Department of Electrical Engineering Department, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associate ship, Fellowship or other similar title or recognition.

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I, ALLU BHARGAV, Roll No. 2k17/PSY/02 student of M. Tech. (Power System), hereby declare that the dissertation/project titled "Grid Integration of PV-STATCOM using Five Level Multilevel Inverter" under the supervision of Prof. ALKA SINGH of Electrical Engineering Department Delhi Technological University in partial fulfillment of the requirement for the award of the degree of Master of Technology has not been submitted elsewhere for the award of any Degree.

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ABSTRACT

Due to increase in non-linear/linear Loads exponentially, power quality has been a major concern nowadays. PQ issues and solutions for problems such as injection of harmonics by non-linear loads, voltage regulation, power factor correction etc. are current topics of research. So, harmonic mitigation using a five- level shunt multilevel inverter is the focus of this Thesis. In this work, PV-STATCOM is designed and simulated; its working is checked in two modes. In mode-1, both active and reactive power are supplied to grid, which is performed during day time only. In mode-2, only reactive power is supplied to the grid, and this mode works during night time. Therefore, the proposed PV-STATCOM can be utilized to its full potential throughout the day. Incremental conductance algorithm is utilized to extract maximum power. SRF control technique and PV feed forward term are combined to generate reference currents. Phase shift (PS)-PWM technique is implemented to generate the pulses. The whole complete system is simulated in both the modes under various load conditions. Some hardware results for the developed 5 level prototype are also illustrated.

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LIST OF ABBREVIATIONS

1. PV- Photovoltaic
2. VSI-Voltage Source Inverter
3. MPPT- Maximum Power Point Transfer
4. CHBMLI- Cascaded H- Bridge Multilevel Inverter
5. DCMLI- Diode Clamped Multilevel Inverter
6. NPCMLI-Neutral Point Clamped Multilevel Inverter
7. FCMLI-Flying Capacitor Multilevel Inverter
8. SCMLI- Symmetric Cascaded Multilevel Inverter
9. ACMLI- Asymmetric Cascaded Multilevel Inverter
10. PWM- Pulse Width Modulation
11. PDPWM- Phase Disposition Pulse Width Modulation
12. PODPWM-Phase Opposition Disposition Pulse Width Modulation
13. APODPWM- Alternative Phase Opposition Disposition Pulse Width Modulation
14. PSPWM- Phase Shifting Pulse Width Modulation
15. PCC- Point of Common Coupling
16. FFT- Fast Fourier Transform
17. DSTATCOM- Distribution Static Compensator
18. PV-STATCOM- Photovoltaic Static Compensator
19. Op-amp- Operational amplifier

Chapter 1

Introduction

1.1 Background

The energy shortage makes it an exciting study subject for renewable energy sources to be integrated into the system. The number of renewables and power generators is growing very quickly, which also threatens the power network. Modern digital power engineering is a significant component in distributed production and the incorporation of renewables into the modern electricity grid in attempt to preserve or even enhance the energy generation efficiency and performance of the power scheme by distributed generation. It is used extensively in the grid system [1]. Since there are more or less environmental conditions based on the production of micro-sources (photovoltaics, wind energy, etc.) such as radiance and solar, certain command strategic systems are required to be used or some energy conservation (batteries or super-capacitors, etc.) are required to account for changes. One traditional route to incorporate the micro, power conservation and various kinds of load into DC bus is with distinct kinds of converters [2]-[3]. PV devices are categorized into four classifications according to design and setup [4]. Each is described shortly below.

1.1.1. Central Structure:

Individual PV panels / modules are linked to a chain in a sequence in this circuit framework. The DC voltage, which can be fed directly into the inverter, can be increased. Then several strings are connected parallel to a higher current level by string diodes. Because of losses in the string diodes, the Central Structure System lacks efficiency. The high voltage DC wires between the boards and the inverter are needed [5].

1.1.2. String Structure:

In reality the PV system string structure is a reduced central configuration form, where only one string of PV modules is attached with an inverter. String diodes are not needed and therefore losses related to them are eliminated. Loss of mismatch and partial shading associated with modules is reduced as each string has its own MPPT. This improves the system's general efficiency. The structure of the string increases the system reliability [5].

1.1.3. Multistring Structure:

This is a string structure advancement. This configuration is usually used with high-performance rating systems. There'll be one converter in each chain, which is prevalent to all strings, but there is only one inverter. This configuration has both central and string structures

advantages, as this configuration can achieve higher energy levels and increased efficiency. Strings can be integrated into the system with different orientations [5].

1.1.4. AC module

The PV board and inverter incorporation into a single unit is the module of AC. The module contains all the required functions, such as voltage amplification and MPPT. Since only one board exists, there are no mismatch casualties. Increase of the PV system's capability is far more costly than other structures.

1.2 Grid Connected PV Systems:

The PV devices linked to the Grid are classified according to the amount of power stages. In the previous technology single phase inverter configurations were centrally controlled. The current and prospective engineering focuses mainly on the two stage inverters where a DC / DC converter between the pv units and the DC / AC inverter is attached.[6]

1.2.1 Single Stage PV system:

The inverter stage accomplishes all functions in one single stage system that include MPPT, grid current control and voltage amplification, if necessary. One drawback of this setup is that the inverter must be built to manage the nominal power twice [6].

1.2.2 Double Stage PV system:

Two power processing stages are the most common configuration for two-stage systems. A DC-DC converter is one of these two stages, and the other is a converter. In this scenario, the DC-DC inverter handles MPPT. Either the DC-DC converter output is DC or the output current moduled to follow a corrected sinusoidal wave in two stages [6]. In case of a DC output, the converter can handle the nominal power only, and the inverter can control grid power using the pulse width modulation. In the other case, the converter needs to handle the nominal current twice and control the ripple current as well, while the inverter changes the rippled sinus wave stream to a complete sine wave at line frequency.

Maximum power point tracking (MPPT) is vital if the maximum available power is to be extracted from the PV array. The literature presents various MPPT methods [7]-[11]. Using a boost converter, PV integration into the system is accomplished. The output voltage is increased and its working process is controlled by MPPT. A boost converter is a step-up conversion and plays an important part in PV applications, because low voltage from the PV module is not enough to handle the load. Boost converter is used to boost the PV voltage and connect it to each inverter's DC link. MPPT controller generates the required duty cycle.

Certain problems are as follows with conventional two or three levels:

- There are a number of power electronic converters in this scheme, so the harmonic injection would be very high , which makes the harmonics filter more expensive and bigger.
- If the level of voltage is very high, the power device's switching stress increases.
- Due to high power losses on various converters, efficiency would be small.

1.3 Multilevel Inverter:

In order to overcome these defects, a multi-level inverter, a modular electronics technology is suggested in the literature[12]-[13] that is highly suitable for integrating renewable energy. The core idea is to achieve the desired ac voltage by multi-level inverter voltage from various levels. The theoretically, multilevel inverters can be selected at arbitrary concentrations, so that even without using a transformer the input voltage of the inverter can achieve a high level.. Moreover, the production voltage can be near sinusoidal because of its phase characteristics, which in effect, reduces the filter size. Three commonly used topologies are mentioned in literature diode-clamped inverters (neutral clamped), capacitor clamped (flying capacitor) and cascaded multi-level inverters for the multilevel inverter. The Cascaded H Bridge (CHB) Multi-level inverter is among those topologies considered the most appropriate renewable energy integration topology, the topology uses the different DC components required can be supplied straight from PV array, wind turbine or gas cell inputs. Moreover, several energy storage systems can be integrated into the scheme in attempt to account for the fluctuation in the production power of PV panels and wind turbines. In addition, as the number of DC sources can be selected arbitrarily, the output voltage and power level can be increased.

1.4 Literature Review:

The VSI is first created and deployed by two-stage three-Level inverters. Different control methods were suggested in the study papers for the control of VSI as STATCOM. In response to the difference in voltage, the compensator transfers reactive power between the compensator and the connected network. No reactive power transmission occurs if there's no difference in tension between STATCOM and Grid. Where the STATCOM voltage exceeds the System voltage, STATCOM will provide the reactive power needed and when the device voltage is higher than that of STATCOM the STATCOM observes the surplus reactive power.

Hirofumi Akagi et al[14] propose the instantaneous reactive power elimination technique. The source current after compensation, however, has certain disadvantages and doesn't match that sinusoidal waveform.

The self and independent DC bus based compensator VAr was introduced by Luis T. Moran et al.[15] No external controller loop is necessary for regulating the dc voltage of the dc bus in an independent dc bus method. But the hardware configuration and costs are increased. The technique Pulse Width Modulation (PWM) for maximum reduction of the reactive element size is discussed here. Jacobus D. Van Wyk et al[16] for Var's compensation are analyzed for a PWM converter. It causes greater failure of switch, owing to the high frequency of shifting. However, the filter is small.

Alper Akdagetal[17] has investigated the PWM inverter in order, by designing PI controls for DQ axis currents, to compensate for the energy reactive power demand and voltage controller of the power systems. In modeling and laboratory set-up, the settlement period of the q-axis current element is almost identical.

Bacher et al[18] have found a sequence of inverter linked to a single stage H-bridge in sequence to create the raised ac voltage with enhanced PQ than the two tier converter and a distinct dc voltage source is synthesized. It is known as Cascaded CMLI (Cascaded Multi Level Inverter). Baker[19] later introduced the changed inverter topology in 1980. e.g. Diode Clamped MLI (DCMLI). The only dc voltage source in this topology is supplied by a set of sequence linked capacitors to provide distinct dc voltage levels. The diodes are linked together in sequence to tighten output dc voltage according to the primary changing unit voltage score. This design is known as a Neutral Point Clamped Inverter (NPC). It is also called the DCMLI topology.

The scientists concentrated on MLI during 1990. The flying capacitor MLI was experimentally implemented in 1997 by Lavieville J.P et al[20]. With the capacitor clamping the different voltage levels in the product are reached. More inverter devices (VSIs) can easily be connected in sequence or in conjunction, based on the voltage and energy requirements, using high-voltage reactive power storage. Jih-Sheng Lai and al[21] have been discussing in detail the diode clamped, flying capacitor and cascaded MLI type with its application. Jose Rodríguez et al[22] presented applications and control of some newly emerged modulating topologies. The Cascaded MLI (CMLI) is categorized in two different kinds by h-bridge unit's dc voltage. They are Symmetric Multilevel Inverter (SCMLI) and Asymmetric Cascading Multilevel Inverter (ACMLI). Within SCMLI all h-bridge devices have the same dc voltage magnitude.

In unbalanced voltage conditions Zang Chunyan et al[23] researched sophisticated cascade MLI compensation method. Three phase MLI delta connection is controlled via 3 separate current control loops to provide an adequate compensation for reactive power.

The individual voltage balance system (IVBS) control technique in SCMLI was discussed by Jon Andoni Barenna et al[24], for the same compensation in each of the series of PWM-

connected cells connected with the h-bridge and dc voltage balance. Each h-bridge cell provides reactive power equal to the dc bus voltage control over each h-bridge cell. In order to maintain the DC bus voltage as constant as the reference values, the active power that every h-bridge inverter absorbs is controlled.

Chia-Tse lee et al.[25] explained an average dc bus voltage change and reactive power flow control method, while power system voltage is decreasing. The voltage is controlled at the same value on each h-bridge cell of each phase.

Multilevel inverters have various benfits compared to conventional two or three level inverter. Scientists have been focused on harmonic eliminations using multilevel converters. Various multilevel converters have been proposed.[26]-[42]. Various modulation techniques have been proposed and implemented practically.[43]-[60]. Practical applications of multilevel inverters and harmonic eliminations using multilevel inverters have been described in literature[61]-[64].

1.5 Chapter Summary and Thesis Outline

In chapter 1 A short overview of the background of the work submitted in this thesis. Some initial content on multi-level converters their need and application in renewable energy integration are listed. A overall description and some benefits and disadvantages were provided of the multilevel converter. Some multi-level converter applications have also been given.

Chapter 2 A general definition of the multilevel converter was given along with some advantages and disadvantages. Also, some applications of the multilevel converter were given. The multilevel fundamental switching scheme was introduced and compared to typical PWM schemes.

Chapter 3 discusses different types of Switching schemes for Multilevel Inverter.

Chapter 4 discusses the DSTATCOM Operation and Control and Design and Simulation results for the performance of the DSTATCOM.

Chapter 5 discusses the PV-STATCOM operation and control in different modes and simulation results for the performance of the PV-DSTATCOM

Chapter 6 discusses a brief summary of the hardware development and practical results of Five Level Cascaded H-Bridge Multilevel Inverter are discussed.

Chapter 2

Configurations of Multilevel Inverter

2.1 Introduction:

This section focuses on a short analysis of the most popular multilevel converter topologies[1-10] presenting the nomenclature used and the operational basis for this sort of converter. This section discusses implementation of a multi-level converter switching technique and its integration with renewable energy sources [11-23] using appropriate controllers[24-25].

Compared to traditional and well-known two-level converters, multi-level converters have numerous benefits[26]-[27]. These benefits are mainly aimed at improving the performance of the output signal and increasing nominal capacity of the converter. These characteristics render multilevel converters very appealing to the energy sector and nowadays, scientists all over the globe are making numerous attempts to improve the efficiency of multilevel converters in terms of simplified structures and improved efficiency of various optimization control algorithms to the balance of the DC capacitors voltages and so on . Moreover ,scientists are focusing on the harmonic elimination using multilevel converter topologies and the focussing on new and improved control strategies using pre-calculated tuning features[28]-[32]. This thesis present work on 5-level converters, and its application in PV based grid tied system

2.2 Conventional Two Level and Three Level Voltage Source Inverters:

Switching mode DC to AC inverters provides a sinusoidal AC output voltage that can be regulated in scope and recurrence. The shortest challenging topology for two levels of a square wave voltage rating is half expansion inverter. The half-scaffold topology circuit design is provided in the Fig.2.1. Either turn S1 and Switch S2 is switched ON to offer a heap voltage to remain back from shooting by fault. Vs/2 of Va as shown in Fig.2.2. S1 is switched OFF to complete the process and S2 is switched ON to provide a storage voltage, Va of -Vs/2.

The complete extension topology circuit arrangements is extened as full bridge configuration in Fig.2.3. This topology is used to obtain a waveform with a three-level square wave output. Table 2.1 shows the three conceivable levels. To preven short through switches S_1 and S_3should not be switched on simultaneously.

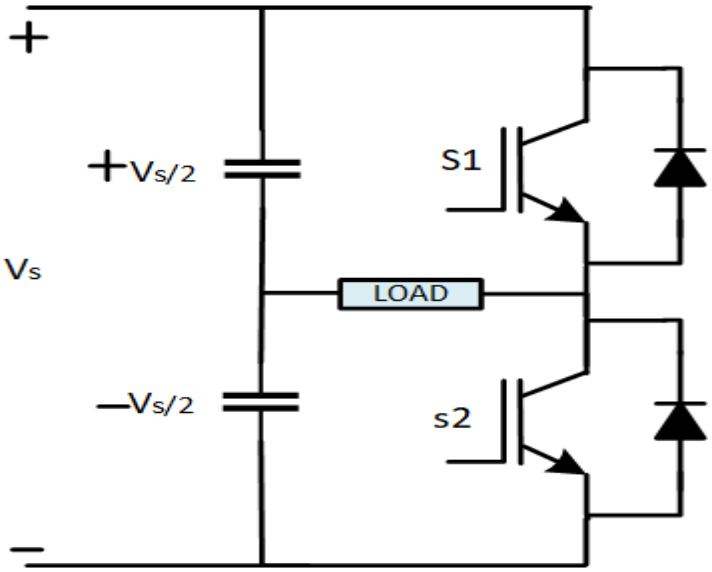


Fig.2.1 Half Bridge configuration [33]

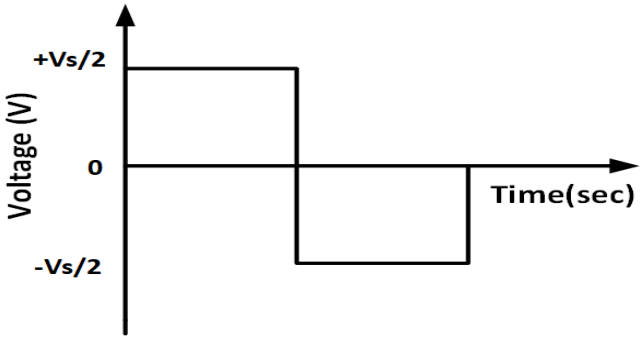


Fig.2.2 Output votage waveform of Half Bridge configuration

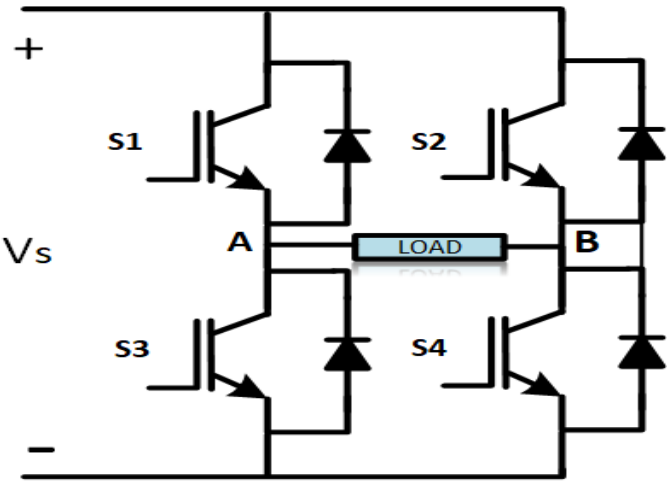


Fig.2.3 Full Bridge configuration

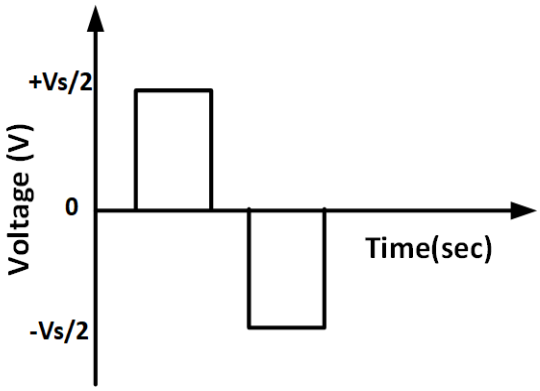


Fig.2.4 Output voltage waveform of Full Bridge configuration

Table.2 1 Switching states of Full bridge configuration

S.no	Conducting Switches	Output Voltage
1	S_1 and S_4	$+V_s$
2	S_2 and S_3	$-V_s$
3	S_1 and S_2 or S_3 and S_4	0

2.3 Multilevel Inverter:

Many manufacturing industries in latest years have started using high-energy devices. Specifically associating a single power semiconductor transition is problematic for a moderate voltage matrix. In intermediate and high-power apps, a multi-level inverter design was provided as an alternative[34]. With this kind of inverters, it is possible to achieve improvements in the consonant quality of the output voltage. Multilevel inverter achieves high-power assessments and enables the use of viable forms of vitality. For instance, photovoltaic, solar and energy systems can be efficiently interfaced with a multi-level inverter system for small what is more, high-power systems. Multilevel inverter generates a coveted waveform of AC voltage from a few DC voltage levels. These DC voltages may or may not be measured to that extent. The air conditioning voltage generated by these DC voltages is the waveform that is ventured. One downside of using a multilevel inverter is inaccurate sinusoidal waveforms from a ventured waveform. The waveform of the staircase provided by the multilevel inverter contains sharp progress. The Fourier arrangement hypothesis makes it clear that this marvel produces sounds, not resisting the sinusoidal waveform's fundamental recurrence. The power character of the power framework is influenced by the sounds on the side of the AC.

The power nature of the inverter is improved by changing the power in small voltage steps. Multilevel inverter generally substitutes the usual two-level three-level voltage source inverters by executing them, such as reducing exchange pull (dv / dt) and reducing THD on input voltage. The multilevel inverter starts at three levels. As the level amount reaches endlessness, the THD production becomes small and negligible. However, the increased voltage levels is limited by voltage unbalance problems, voltage clamping requirements, panel design and storage limitations. A multilevel inverter has many advantages over a standard two-level inverter that uses high frequency PWM.

The attractive characteristics of a multi-level converter can are summarized:

Not only Multi-level inverter can produce very low distortion output voltages, but also reduce dv / dt stresses. Therefore, issues can be decreased with electromagnetic compatibility. Multi-level inverters generate smaller voltage of Common Mode(CM). The stress in the motor coils attached to a multi-level inverter can therefore be reduced. In addition, advanced modulation techniques can also eliminate CM voltage. Multilevel inverters produce small distortion output power. Both fundamental and high frequency changing PWM techniques can work on multi-level inverter modules. Lower switching frequency typically results lower switching loss and greater efficiency.

The undesirable aspects associated with Multilevel Inverter are :

The main disadvantage lies in the fact that the number of switches increases with the amount of level. Another disadvantage of this inverter is the need for various DC voltage sources, which are mostly given by the DC link capacitors or interfacing with sources . It is an essential test to adjust voltage sources in various load conditions during operation. In the last two centuries, several multilevel inverter topologies have been suggested. Three major structures of multilevel inverters have also been reported. They are:

1. Diode Clamped/ Neutral clamped Multilevel Inverter.
2. Flying capacitor/ capacitor clamped Multilevel inverter.
3. Cascaded H-bridge Multilevel Inverter.

2.4 Multilevel Notion:

Since 1975 the concept of a multilevel inverter is launched [35]. However, the fundamental idea of a multilevel inverter to achieve high control is to use the progression of energy

semiconductor switches with some low voltage DC sources to change control, combining a waveform of a staircase voltage. Fig.2.5 shows one phase arm of a multi-level inverter. This schematic outline contains a perfect switch with a few states for operations of semiconductors. The semiconductors need to withstand restricted capacitor voltages.

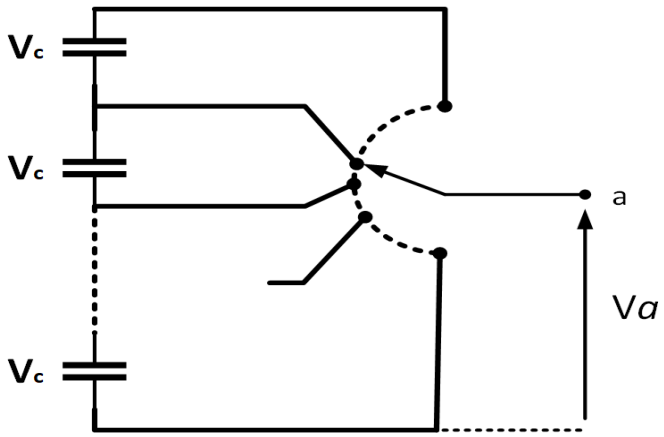


Fig.2.5 One pahse leg of Multilevel Inverter

Multi-level inverters are being used in the world of power electronics for almost two decades. They are designated according to the amount of voltage levels they produce and the various topologies they are based on. The number of output voltage levels is usually selected odd rather than even. It means that the definition of zero voltage level in the inverter output, as in three or five-level inverters, makes it more sinusoidal with less harmonics.

2.5 Diode Clamped Multilevel Inverter:

Fig. 2.6 displays a three-level diode-clamped inverter[36]-[38]. The output voltage is expressed as the V_{a0} where n is selected as the neutral point. The C_1 and C_2 series-connecting capacitors can divide the V_{dc} DC bus voltage. For three levels. The switching status leads to the different output.

- The output voltage $v_{a0} = \frac{V_{dc}}{2}$, when the upper two switches S_1 and S_2 are closed.
- v_{a0}=0, when the switch S_2 and S_1' are closed.
- The output voltage $v_{a0} = \frac{V_{dc}}{2}$,when the upper two switches S_1' and S_2' are closed.

In this type of inverter that can clamp the switching voltage at quarter of the DC connecting voltage the D_1 and D_1' clamping diodes perform a significant part. The V_{a0}= V_{dc}/2 input voltage is supplied as an instance. Switch S_1 and S_2 should be switched off in this case. D_1' serves to

balance the voltage distribution between the two S_1' and S_2' switches. The voltage over C_1 is blocked with S_1' and C_2 is blocked with S_2'.

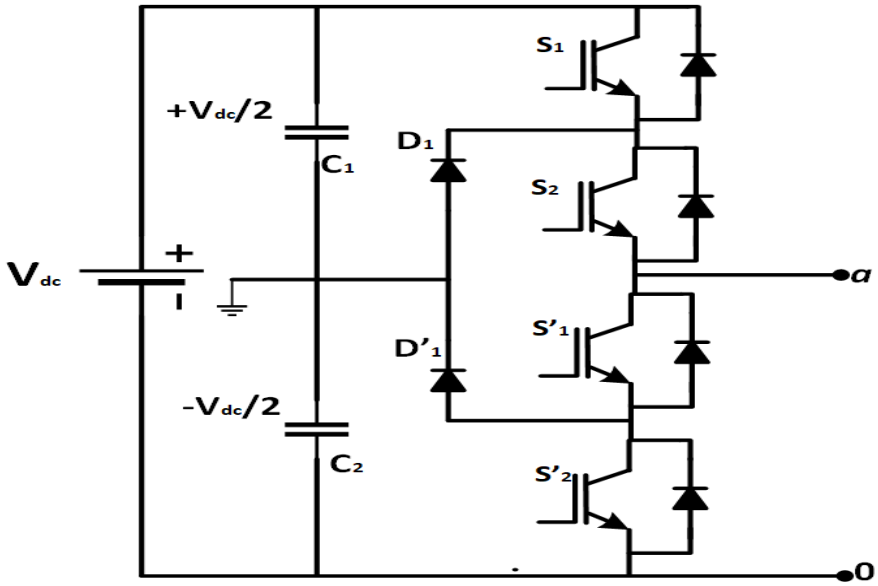


Fig.2.6 Three level Diode Clamped Multilevel Inverter

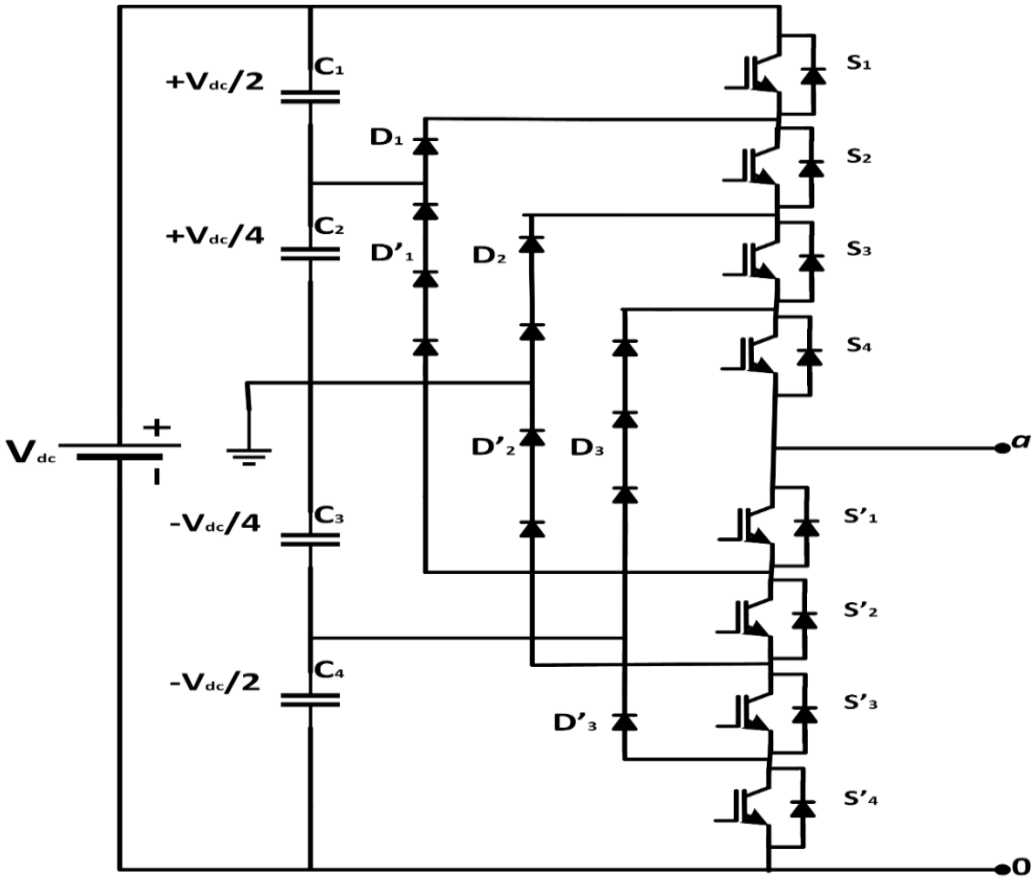


Fig.2.7 Five level Diode Clamped Multilevel Inverter

Fig.2.7 displays the five-level diode-clamped inverter. The V_{dc} DC connection voltage is evenly distributed across fourC_1, C_2, C_3 and C_4 capacitors. Table 2.2 shows the output voltage V_{an} and the respective switch state.

One drawback of this type of inverter is the clamping diodes different reverse blocking voltage rating. In the multilevel inverter five-level diode clamped, the active switching device only

Table.2.2 Switching states of Five Level Diode Clamped Multilevel Inverter

Output Voltage V_{an}	Switch State							
	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
$V_{an} = V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{an} = V_{dc}/4$	0	1	1	1	1	0	0	0
$V_{an}=0$	0	0	1	1	1	1	0	0
$V_{an} = -V_{dc}/4$	0	0	0	1	1	1	1	0
$V_{an} = -V_{dc}/2$	0	0	0	0	1	1	1	1

needs to block $V_{dc}/4$. For the clamping diodes this is not the case. For example, the clamping diode D_3 must be able to handle a voltage level of $3V_{dc}/4$ when the upper switch S_1, S_2 and S_3 is closed. The clamping diode D_2 must block $V_{dc}/2$ when the switch S_1 and S_2 are closed. The clamping diode D_1' is required to block $3V_{dc}/4$ if the lower switches S_2', S_3' and S_4' are closed. When the inverter level is L and the clamping diode is of the same rating as the active inverter ($V_{dc}/4$ in this five-level diode clamping multi-level inverter), then the diode clamping rating (L- 1) x (L-2) is indicated. It can be seen that with level L, the number of clamping diodes will increase quadratically. Therefore, if the level of the inverter is high enough, the amount of clamping diodes needed in the circuit is very high and the whole system becomes impractical.

Advantages:

1. All of the phases share a common dc bus, which minimizes the capacitance requirements of the converter. For this reason, a back-to-back topology is not only possible.
2. The capacitors can be pre-charged as a group.
3. Efficiency is high for fundamental frequency switching

4. When the number of levels is high enough, harmonic content will be low enough to avoid the need for filters

Disadvantages:

1. Real power flow is difficult for a single inverter because the intermediate dc levels will tend to overcharge or discharge without precise monitoring and control.
2. The number of clamping diodes required is quadratically related to the number of levels , which can be cumbersome for units with a high number of levels.

2.6 Capacitor-Clamped Multilevel Inverter:

Fig.2.8 and Fig.2.9 shows the topologies of the three- and five-level multi-level capacitor - clamped inverter[39]-[40] with a similar structure as the diode-clamped multi-level inverter. In topology instead of diodes the capacitors are used.

The multilevel inverter capacitor clamped three-level is shown in Fig.2.8. One benefit of this type of topology is that a certain yield voltage can be provided with some redundancies. For instance, for V_{an}= 0, either couple (S_1, S_1'), or (S_2, S_2') must be turned on, taking the three-level Capacitor-Clamped Inverter. The amount of redundancies will improve as the rate of output

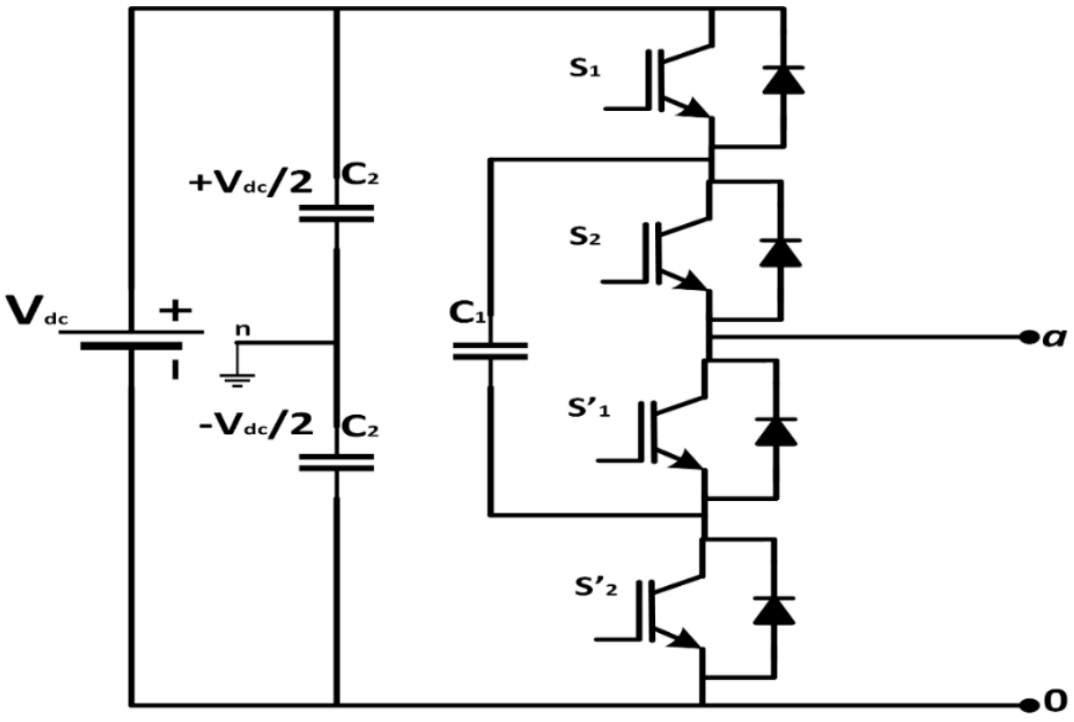


Fig.2.8 Three level Capacitor Clamped Multilevel Inverter

voltage rises. Table 2.3 shows the switch state and its respective output voltage for a five-level capacitor -clamped inverter. These redundancies make it easy to balance capacitor voltages with certain control strategies and modulation techniques since it is feasible to decide which capacitor to charge and which one to discharge. Given the voltage rating of the equipment in

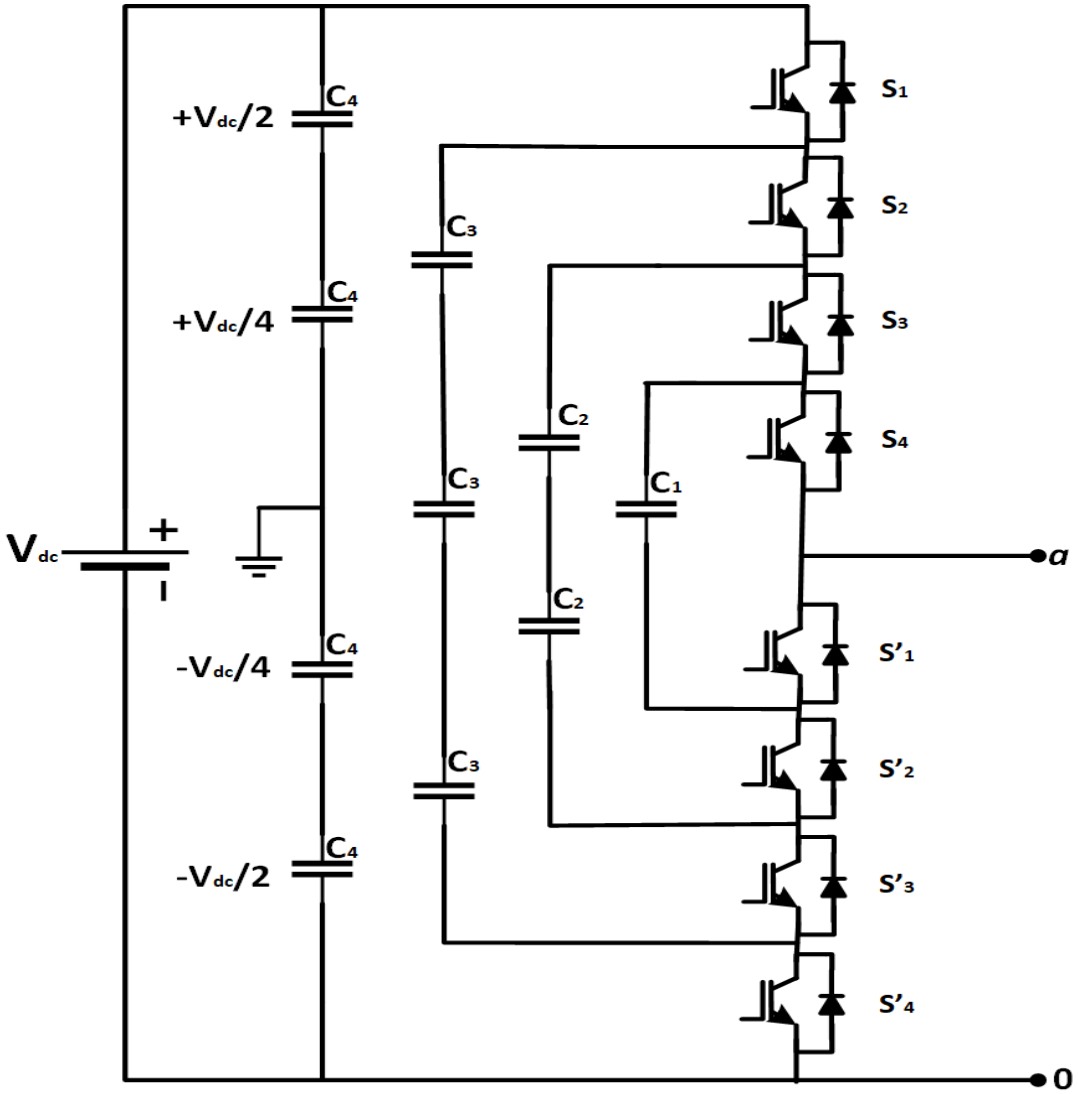


Fig.2.9 Five level Capacitor Clamped Multilevel Inverter

the circuit, the number of capacitors used for clamping voltage can be seen to be very large. If the voltage value for all capacitors is assumed to be the same as the major dc-bus capacitors ($V_{dc}/4$ for the 5-level capacitor clamped inverter as illustrated in Fig.2.9), the number of additional capacitors in addition to the main dc-bus capacitor can be set to (L-1)x (L-2)/2, where L is the inverter level. The multilevel inverter with a capacitor clamping has the same problem as the multilevel inverter with a diode clamping at high inverter levels.

Table 2.3 Switching states of Five Level capacitor Clamped Multilevel Inverter

Output Voltage V_{an}	Switch State							
	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
V_{an} = V_{dc}/2 (no redundancies)								
$V_{dc}/2$	1	1	1	1	0	0	0	0
V_{an} = V_{dc}/4 (redundancies)								
$V_{dc}/2- V_{dc}/4$	1	1	1	0	1	0	0	0
$3V_{dc}/4-V_{dc}/2$	0	1	1	1	0	0	0	1
$V_{dc}/2-3V_{dc}/4+V_{dc}/2$	1	0	1	1	0	0	1	0
V_{an} = 0 (redundancies)								
$V_{dc}/2- V_{dc}/2$	1	1	0	0	1	1	0	0
$V_{dc}/2- V_{dc}/2$	0	0	1	1	0	0	1	1
$V_{dc}/2-3V_{dc}/4+V_{dc}/2-V_{dc}/4$	1	0	1	0	1	0	1	0
$V_{dc}/2-3V_{dc}/4- V_{dc}/4$	1	0	0	1	0	1	1	0
$3V_{dc}/4- V_{dc}/2+V_{dc}/4- V_{dc}/2$	0	1	0	1	0	1	0	1
$3V_{dc}/4- V_{dc}/4- V_{dc}/2$	0	1	1	0	1	0	0	1
V_{an} = -V_{dc}/4 (redundancies)								
$V_{dc}/2-3 V_{dc}/4$	1	0	0	0	1	1	1	0
$V_{dc}/4- V_{dc}/2$	0	0	0	1	0	1	1	1
$V_{dc}/2-V_{dc}/4-V_{dc}/2$	0	0	1	0	1	0	1	1
V_{an} = -V_{dc}/2 (no redundancies)								
$-V_{dc}/2$	0	0	0	0	1	1	1	1

Advantages:

1. Additional clamping diodes are not needed.
2. It has switching redundancy within the phase, which can be used to balance the flying capacitors so that only one DC source is needed.
3. The required number of voltage levels can be achieved without the use of the transformer.
4. This assists in reducing the cost of the converter and again reduces power loss.

Disadvantages:

1. Converter initialization i.e., before the converter can be modulated by any modulation scheme the capacitors must be set up with the required voltage level as the initial charge. This complicates the modulation process and becomes a hindrance to the operation of the converter.
2. Control is complicated to track the voltage levels for all of the capacitors.
3. Precharging all of the capacitors to the same voltage level and startup are complex.
4. Switching utilization and efficiency are poor for real power transmission.
5. Since the capacitors have large fractions of the dc bus voltage across them, rating of the capacitors are a design challenge.
6. The large numbers of capacitors are required and it is more expensive and bulkier than clamping diodes in multilevel diode-clamped converters.
7. Packaging is also more difficult in inverters with a high number of levels.

2.7 Cascaded H-Bridge(CHB) Multilevel Inverter:

Multilevel CHBs are converters formed using two or more single-phase H-bridge inverters,[41]-[42] hence their names. Each H-bridge is equivalent to two phase legs, where the line-line voltage is the converter power. A single H-bridge converter in Fig.2.10 can therefore be used to produce three distinct levels of voltage. Each leg has two switching states, in order to prevent short-circuit dc-link capacitor. As there are two legs, there are four different

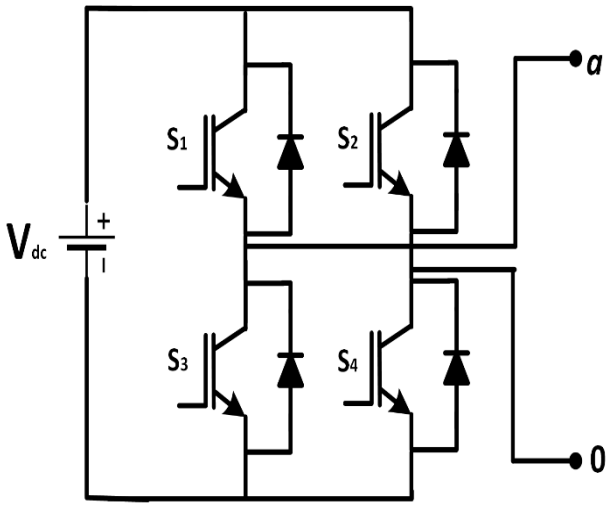


Fig.2.10 Three level Cascaded H-Bridge Multilevel Inverter

switching states, although the two of them are redundant. Fig.2.11 shows three different voltage levels and their associated circuits. The zero level may be produced by connecting the phase outputs to the inverter's positive or negative Bars (only the first is shown in Fig. 2.11).

When two or more H-bridges are connected in series, their output voltage may be combined into several output levels and the total output voltage of the inverter and its rated capacity can be improved. The Fig.2.12 shows two connected H-bridges and a qualitative example of their possible 3-level output voltages. The total output voltage of the converter is also shown with

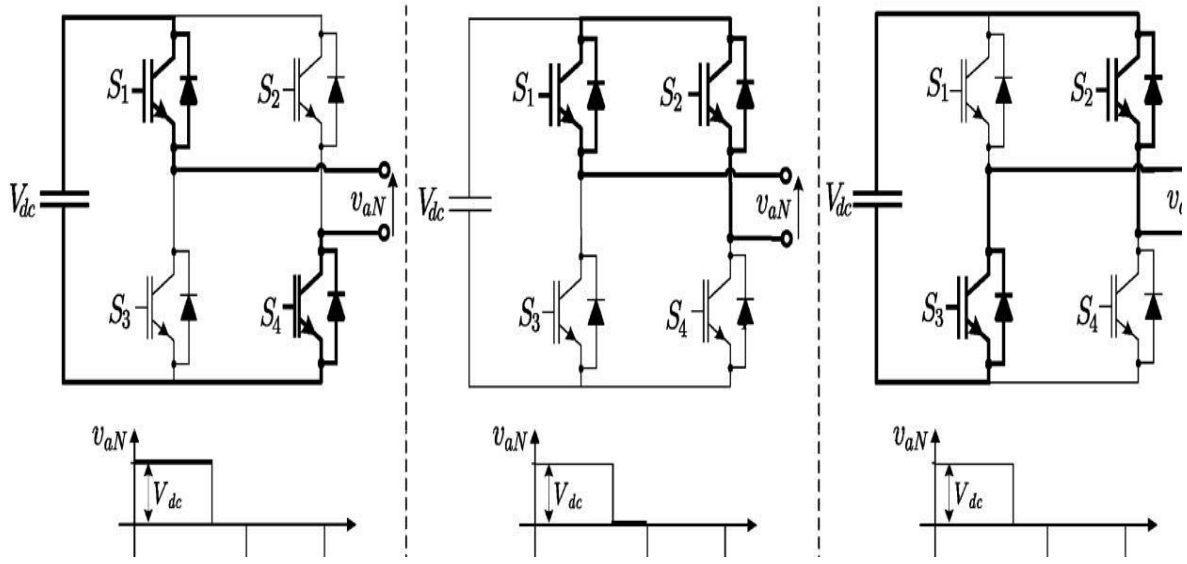


Fig.2.11 Three level H-bridge switching states

five different voltage levels. In general, the 2k + 1 voltage level (two per H-bridge and zero, which are common to all) is achieved by connecting k H-bridges in series and the maximum output voltage is possible in kVdc. CHB presents more redundancies than previous topologies, as a redundant switching state exists on each H-bridge or power cell, and the connection series inherently introduces more redundancies.

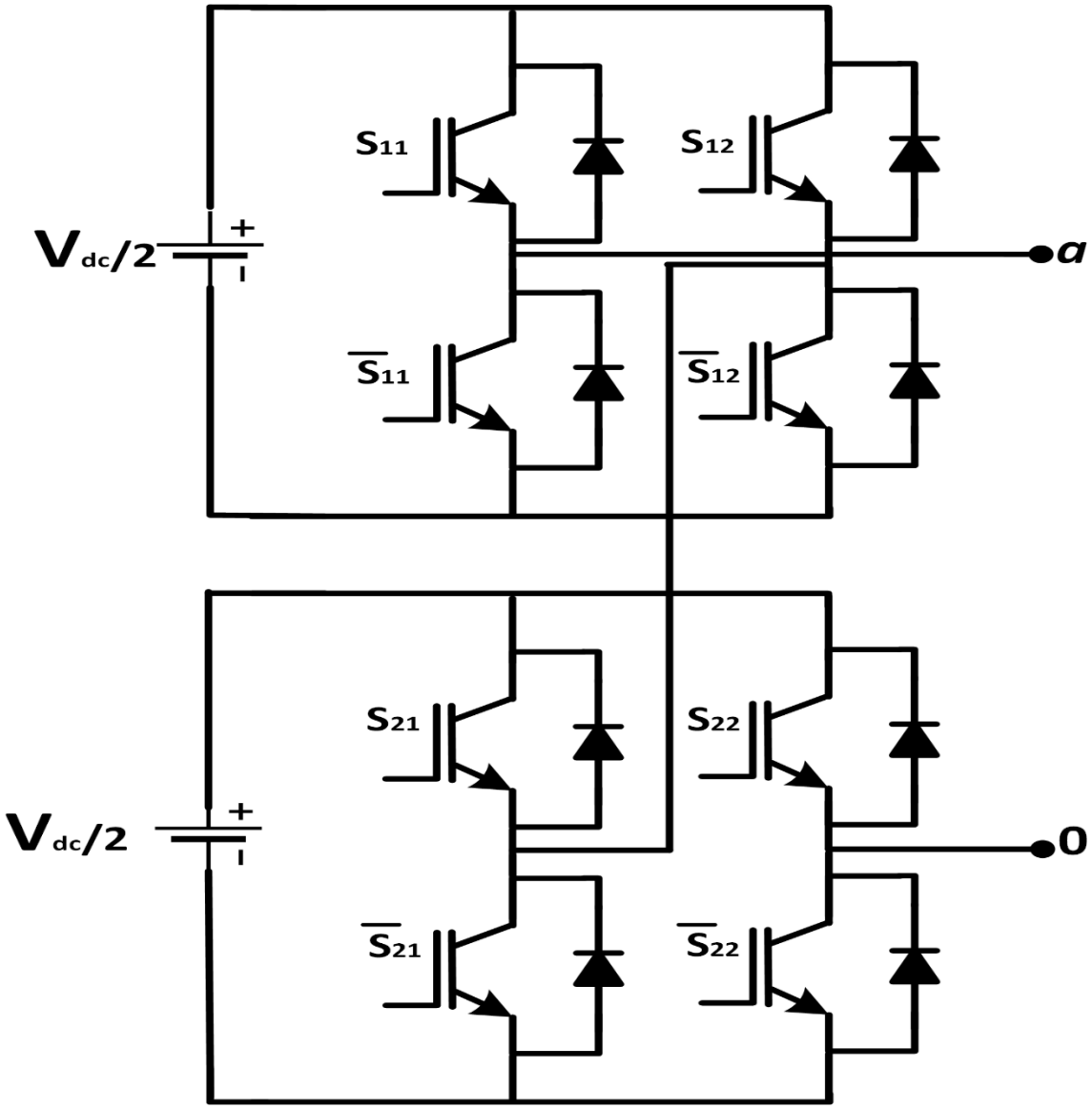


Fig.2.12 Five level Cascaded H-Bridge Multilevel Inverter

This can be clearly noted in Table.2.4, which lists all the switching states of the CHB inverter of two cell H bridge or five level. When the number of cells increases, the amount of redundancies expands excessively. These redundancies and the inherent modularity of this design offer benefits that permit the procedure of fault-tolerant. The efficient increase in output and power is another advantage as all semiconductors only block Vdc.

Table.2.4 Switching states of Five Level Cascaded H-Bridge Multilevel Inverter

Total inverter output voltage	**Switching state**				**Individual cell output voltage**	
$\boldsymbol{V_{an}}$	**S_{11}**	**S_{12}**	**S_{21}**	**S_{22}**	$\boldsymbol{V_{a1}}$	$\boldsymbol{V_{a2}}$
$\boldsymbol{V_{dc}}$	1	0	1	0	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$
$\frac{\boldsymbol{V_{dc}}}{\boldsymbol{2}}$	1	0	1	1	$\frac{V_{dc}}{2}$	0
			0	0		
	1	1	1	0	0	$\frac{V_{dc}}{2}$
	0	0				
0	0	0	0	0	0	0
	0	0	1	1		
	1	1	0	0		
	1	1	1	1		
	1	0	0	1	$\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$
	0	1	1	0	$-\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$
$-\frac{\boldsymbol{V_{dc}}}{\boldsymbol{2}}$	0	1	0	0	$-\frac{V_{dc}}{2}$	0
			1	1		
	0	0	0	1	0	$-\frac{V_{dc}}{2}$
	1	1				
$-\boldsymbol{V_{dc}}$	0	1	0	1	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$

Advantages:

1. Modularity of control can be achieved. Unlike the diode clamped and capacitor clamped inverter where the individual phase legs must be modulated by a central controller, the full-bridge inverters of a cascaded structure can be modulated separately.
2. Requires the least number of components among all multilevel converters to achieve the same number of voltage levels.

Disadvantages:

1. Communication between the full-bridges is required to achieve the synchronization of reference and the carrier waveforms.
2. Needs separate dc sources for real power conversions, and thus its applications are somewhat limited.

In the subsequent Chapters of the thesis, work focuses is on 5-Level H-Bridge Cascaded Multilevel converter Only.

Chapter-3

Modulation Techniques

3.1 Introduction

The power electronic converters are mainly operated in the "switched mode." This implies that the switches in the converter are always switched off or on (saturated by just a tiny voltage drop onto the switch) in either one of the two statements. Any operation, other than an inevitable transition from conducting to non-conducting in a linear environment, causes unwanted efficiency loss and an unbearable rise in the power dissipation of switches. The switches alternate between these two states (i.e. on and off) to regulate the power flow in the converter. This takes place quickly enough to filter the switched signal by the inductors and conductors at the input and output nodes of the converter. The switching element is attenuated and the required DC or low-frequency AC element is maintained. This is called pulsed width modulation (PWM), as it controls the desired average value by modulating the pulse width.

The switch frequency fc should be high many times the frequency of the basic desired AC component f1 seen on the input or input terminals for the maximum attenuation of the switching component. This conflicts with the bottom threshold on the changing frequency by changing errors in big converters. In the case of converters from GTO, the ratio between the switch frequency and fundamental frequency fc / f1 (= N, pulse number). Another application with a low pulse number can be used in converters that are better described as amplifiers, with a relatively high basic output frequency. These switch modes with high energy are used to filter active power, to generate test signal, servo and audio amplifiers. The small pulse figures require efficient modulation as much as necessary in order to decrease distortion. In these conditions, multi-level converters can significantly decrease their distortion by astonishing multi-switch changing instants and improving the obvious pulse amount of the general converter.

3.2 PWM Techniques

The basic pulse-width measurement (PWM) techniques are split into conventional voltage-source and current-regulated techniques. The Digital Signal Processing (DSP) or Programmable Logic Device (PLD) is easier to handle by voltage source techniques. Current checks are typically contingent on event planning, so analog systems are only worked reliably

to a certain power level. The harmonic efficiency in separate current controlled techniques is not as great as that in techniques of voltage source. The following is a sample PWM technique.

Inverter output voltage $V_{A0} = V_{dc}/2$, When $V_{control} > V_{tri,}$ and $V_{A0} = -V_{dc}/2$, When $V_{control} < V_{tri.}$ PWM frequency is the same as the frequency of V_{tri}. Amplitude is controlled by the peak value of $V_{control}$ and Fundamental frequency is controlled by the frequency of $V_{control}$.

Modulation index(m) is given by:

$$m = \frac{V_{control}}{V_{tri}} \tag{3.2.1}$$

Let, frequency of $V_{tri} = f_s$= PWM frequency and frequency of $V_{control} = f_l$ = fundamental frequency. Then

Amplitude modulation ratio (m_a) is given by:

$$m_a = \frac{peak\ \ amplitude\ \ of V_{contro\ l}}{amplitude\ \ of\ V_{tri}} \tag{3.2.2}$$

Frequency modulation is given by

$$m_f = \frac{f_s}{f_1} \tag{3.2.3}$$

m_f should be an odd integer. If m_f is not an integer, there may exist sub harmonics at output voltage. If m_f is not odd, DC component may exist and even harmonics are present at output voltage. m_f should be multiple of 3 for three phase PWM inverter.

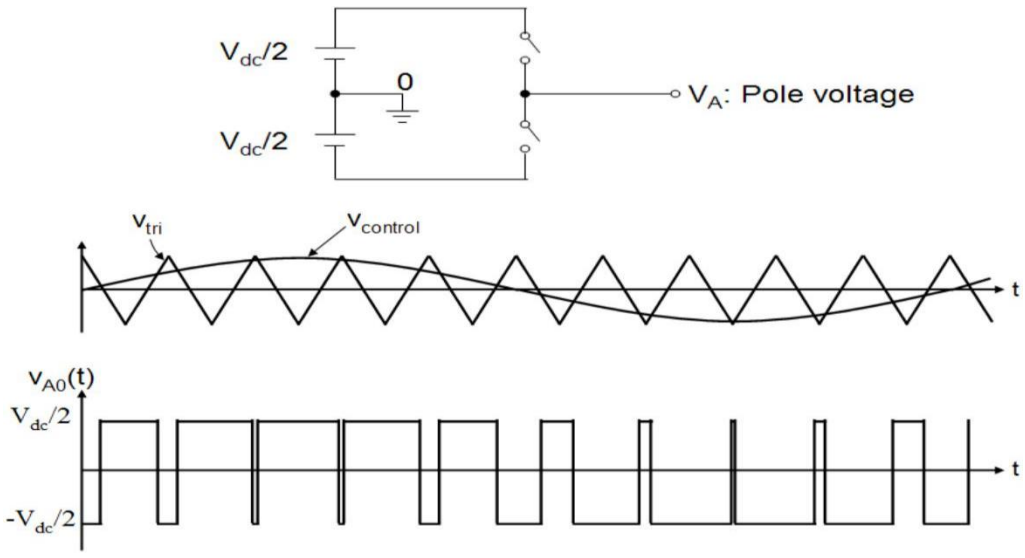


Fig.3.1 Pulse Width Modulation

The challenge to expand traditional modulation methods to a multi-level case was together with the development of the multilevel converter topologies. On the one hand, the added complexity that more powerful electronic equipment can be used to control is inherent, and on the other, the additional freeness provided by the additional switching states produced by these topologies can be exploited. As a result, a big amount of distinct modulation algorithms was adjusted or created, each with distinctive benefits and drawbacks, based on implementation and converter topology. The most frequent modulation techniques are provided in the Fig.3.2 for multi-level inverters. In this respect the modulation algorithms are classified according to the average switching frequency, i.e., high or low. High frequencies above 1 kHz are regarded for high-power applications.

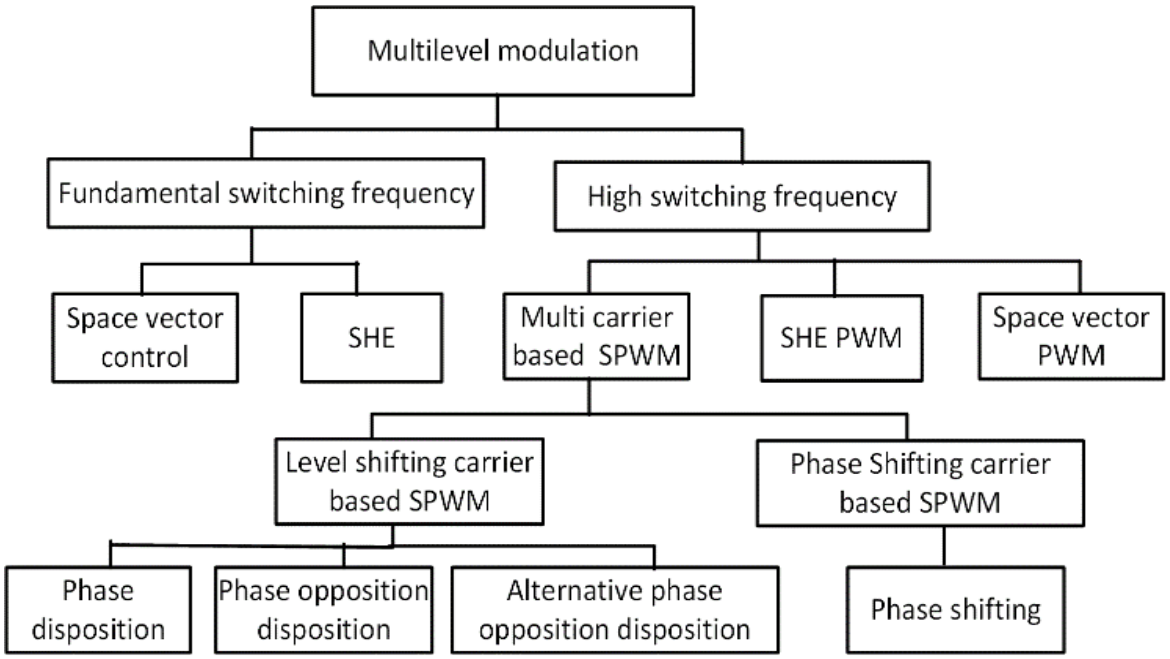


Fig 3.2 Multilevel converter Modulation Methods [43]

3.3 Selective Harmonic elimination (SHE)[45]-[47]:

Converters are generally used with small conventional carriers-based PWM techniques to reduce the carrier frequency to those concentrations, with low voltage harmonics, which increases distortion which thus turns into efficiency issues. A low frequency switching PWM method developed for traditional converters in which a few switchable angles per quarter basic cycle (generally 3 to 7) are pre-defined and pre-calculated using Fourier analysis to eliminate unwanted low-order harmonics. Essentially, for those undesired harmonics, the SHE Fourier coefficients or harmonic elements with unknown angles of switch of the predefined wave form are equal to zero, whereas the fundamental component is equivalent to the desired reference

amplitude. This number of variables can be fixed by numerical methods and an angle equation is obtained.[44]

This idea is expanded also for waveforms of multiple levels [45]-[47]. The fundamental idea is maintained, i.e. the converter generates a predefined Voltage waveform with a fixed number of switching angles, as shown in Fig 3.3. A certain amount of unwanted low-order harmonics in the production voltage can be eliminated by correctly calculating the turning corners. With m switching angles in the quarter cycle, m control degrees are achieved which enable m-1 to remove unwanted harmonics, and the last to control the amplitude of the basic reference component.

$$h_n = \frac{4V_{dc}}{n\pi}\sum_{k=1}^{m}\cos(n\alpha_k) \qquad (3.2.4)$$

The harmonics to be removed are kept null. The series of variables is then fixed several times using numerical techniques for covering a wide range of signal indexes. In a lookup table the solutions (angles) are then modulated to modulate the converter. For example, a typical

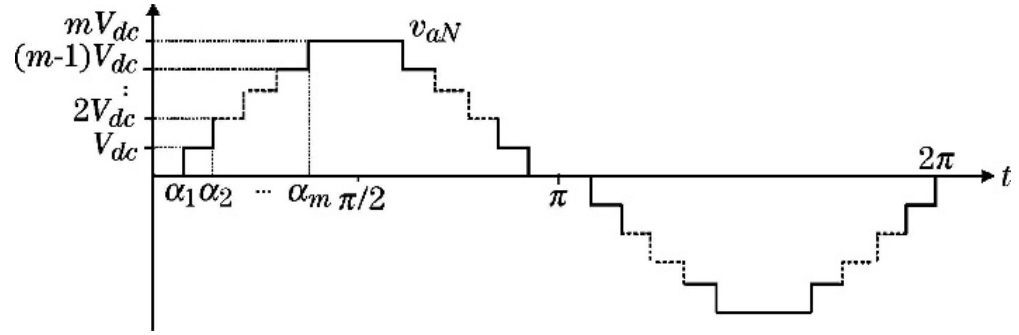


Fig 3.3 Multilevel selective harmonic elimination.

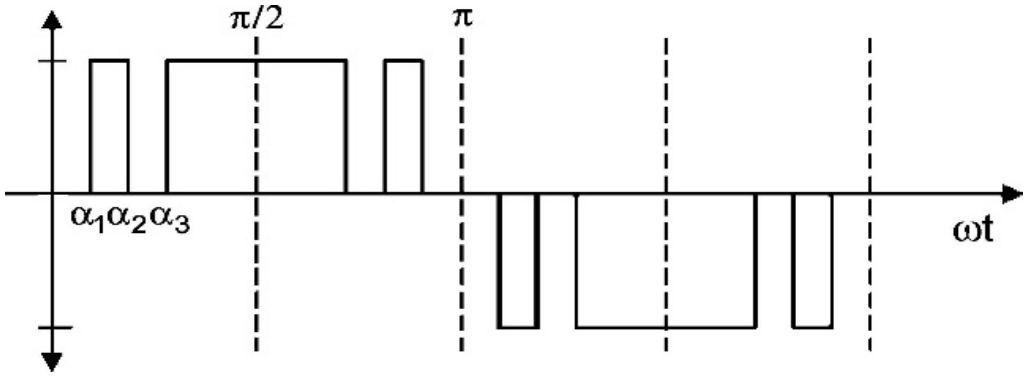


Fig 3.4 Three level selective harmonic elimination

waveform with three switch angles (α_1, α_2, α_3)) is given in the Fig.3.4 for a three-level converter such as a NPC. The appropriate Fourier series is given by

$$V_{aN} = \frac{4V_{dc}}{\pi}\sum_{n=1}^{\infty}\frac{1}{n}\{\cos(n\alpha_1) + \cos(n\alpha_2) + \cos(n\alpha_3)\} \times \sin(n\omega t) \quad (3.2.5)$$

Three Fourier series coefficients may be compelled to a required significance by this equation. Of course, the first coefficient corresponds to the fundamental component and is fixed to the desired modulation index, whereas the 5th and 7th coefficients are usually fixed to zero (for the fifth and 7th harmonic elimination)

$$M.\frac{\pi}{4} = \cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) \quad (3.2.6)$$

$$0 = \cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) \quad (3.2.7)$$

$$0 = \cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) \quad (3.2.8)$$

Where M is the indice of modulation. SHE usually doesn't eliminate the third harmonics and its multiples as the three-phase charging link is eliminated naturally. Fig.3.5 shows, for example, the angles of implementation and the output voltage with its corresponding spectrum, from which it can effectively be seen to eliminate fifth and seventh harmonic.

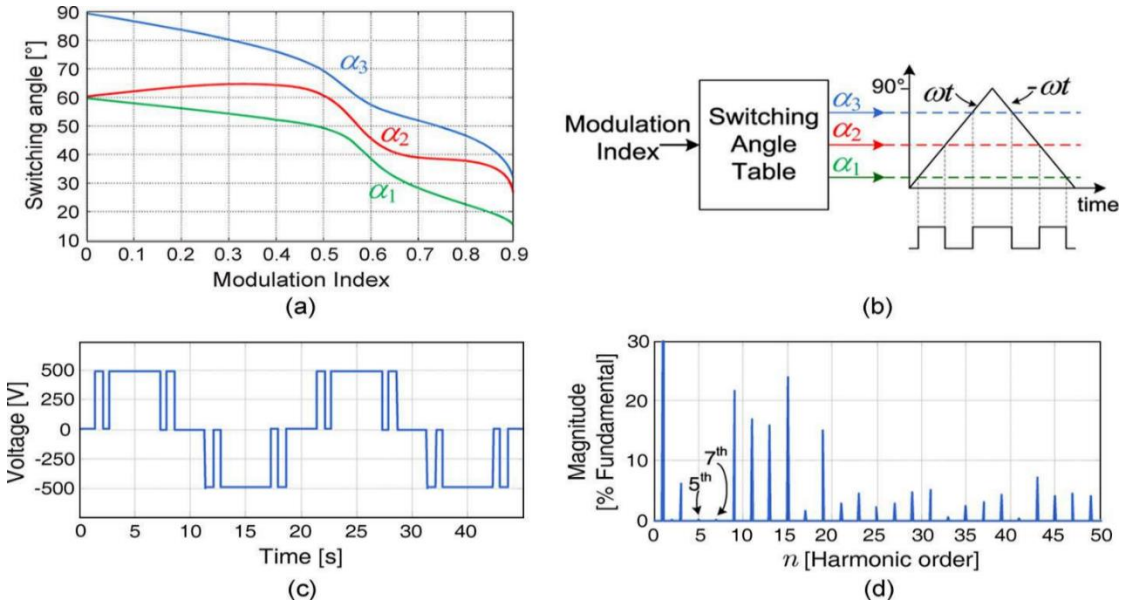


Fig.3.5 Three-level selective harmonic elimination: (a) angles solution, (b) implementation diagram, (c) output voltage, and (d) output voltage spectrum.

Note that there is no control over the harmonics that are not eliminated and usually increase because the harmonic energy in the shifted waveform that is eliminated is redistributed over the others. If these harmonics are not appropriate for a specific application, extra angles can be introduced, thereby eliminating more harmonics. For high-performance power grid linked

converters, very large system systems require several perspectives, increasing the frequency of shifting and failures or using extra filters. The SHE variant known as the selective harmonic mitigation (SHM) is more appropriate in this instance. It does not force the angles to completely remove the harmonics by setting them to zero, as the main distinction of SHE. Inequalities are used instead to restrict harmonics to appropriate numbers [48]. The harmonic spectrum of the waveforms acquired can thus comply with the present grid code rules on the inclusion of energy systems within the transport network. The big benefit of SHM over SHE is that the required interfacing filters are reduced (or even eliminated) without affecting the system's energy performance. The price, quantity and weight of the entire energy scheme are therefore reduced economically.

SHE is also regarded as staircase modulation for converters with higher levels such as CHB, as the voltage form of the waveform is stair-like. The fundamental concept is the same as SHE, because each angle is linked with a specific cell. In order to produce the multi-level yield waveform, the working concept of this method is to link each inverter unit at a particular angle, creating only minimal switches. As with SHE, the primary benefit is that the converter changes very few occasions a period and minimizes the losses. Low-order harmonics are also removed, which reduces output filter capacity, weight and cost. These methods all require numerical algorithms to solve a set of equations conducted for a number of modulation indexes, which leads to important calculations that cannot be performed with present micro processing devices in real time and are thus done offline. The alternatives are therefore placed in lookup lists, and for those unsolved modulation indexes, interpolation is applied. This prevents SHE modulation algorithms from being appropriate for high-dynamic applications.

3.4 Space vector Modulation [49]:

The SVM (Space Vector Module) algorithm is essentially a PWM strategy that calculates switching times on the basis of a three-phase representation of the reference space-vector and inverters switching states, and not on the basis of the time- and output levels per phase, as in previously analysed modes.

A. State-Space Vector Representation of the inverter:

The voltage space vector combines the values of the three-phase variables simultaneously and maps them to become a single vector within the α-β complex plane.

$$V_s = \frac{2}{3}[V_a + V_b + a^2 V_c] \tag{3.2.9}$$

Where $\alpha = (-1/2) + (j\sqrt{3}/2)$. The inverter state-space vectors can be achieved by exchanging the stage input voltages of the inverter with every feasible changing state. An instance is provided in Fig.3.6, for a three-phase NPC inverter. Please note that the NPC has three stages and 3 yield or switching states, which can lead to 3^3 feasible solutions and thus to 27 state-space vectors (amount of three-phase N-level converters in particular is N^3). But only 19 are distinct and 8 auxiliaries. The zero-state vector is redundant three times and the six short-stage vectors are redundant two times. The zero vector, for instance, can be achieved three ways: 1) Connecting 3-phase results with the positive bar busbar ($V_a = V_b = V_c = V_{dc}$), corresponds to the state of switching (+,+,+); or to the neutral point ($V_a = V_b = V_c = 0$) the state associated (0,0,0); or to the negative busbar($V_a = V_b = V_c = -V_{dc}$), the state associated $(-,-,-)$.

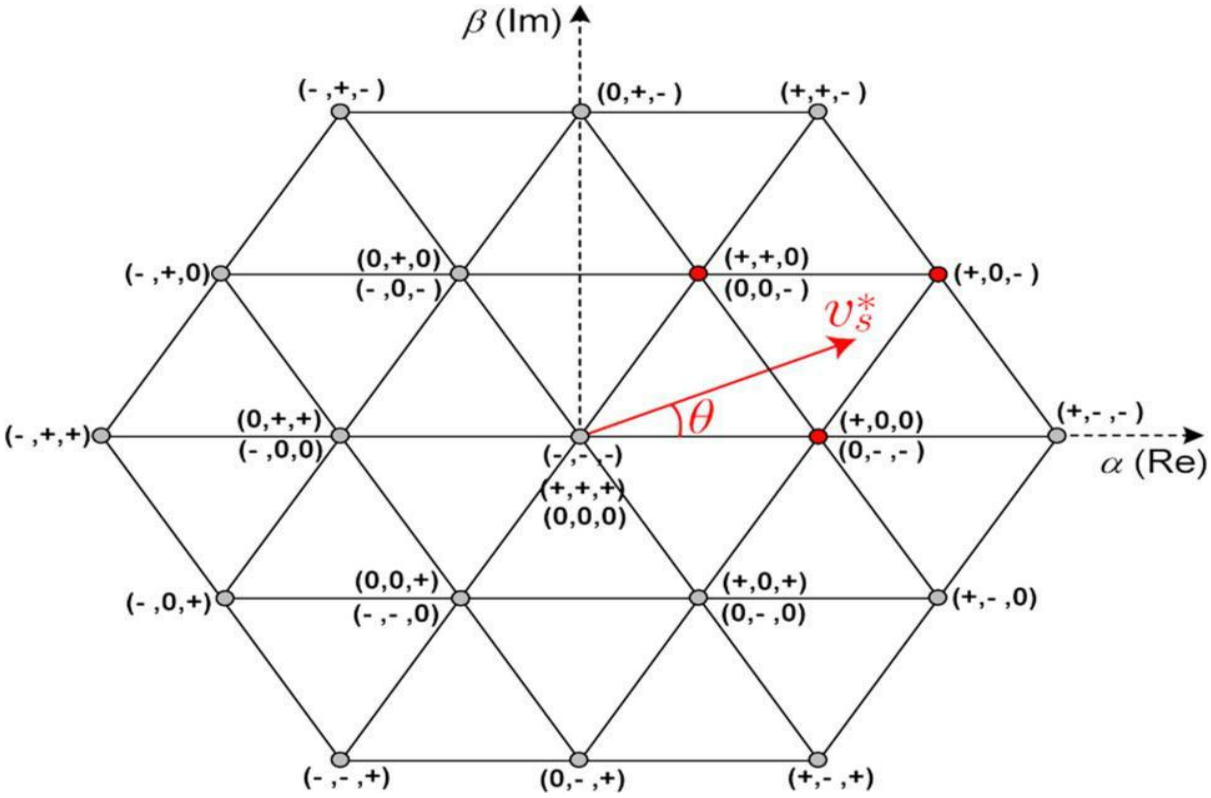


Fig3.6 Three-phase three-level converter state-space vectors

From the load standpoint, redundant vectors exert exactly the same influence, and what is used makes no difference. From the inverter viewpoint, the switching states are different and can be used in other controls as an additional degree of freedom. Since the possible output levels of the inverters have been fixed ($-V_{dc}$, zero, and V_{dc}), vectors in the state-space are also fixed. Note that only seven different space vectors can be obtained from the conventional two-level VSI, and 19 can be produced by simply adding a third level such as the NPC. This increases

more proportionally with regard to the number of levels and is directly consistent with the quality of the output power because a denser vector representation is achieved in the α-β plane. Likewise, more levels have a denser amplitude range coverage per phase of time representation.

In addition, the three-phase reference can be mapping with the same transformation, instead of phase output voltages, to the α-β plane. Based on the fact that the reference variables with fixed voltage values as the inverter output voltages are not switched on, the reference space vectors can be mapped to anywhere in the α-β plane and do not necessarily match any of the inverter space vectors, similar to the time display per phase, where the reference signal do not correspond with an inverter output level. The resulting reference vector V_s is a rotating space vector with the same amplitude and angular speed as in the case of the sinusoid references, as usual in power converter systems, with an instantaneous position with respect to the α real axis as given by $\theta = \omega t$ as illustrated.

Depending on the application, SVM techniques can be divided into algorithms for balanced or unbalanced systems. It is important to know whether there are also harmonics in the reference vector, or if the control technique must compensate harmonics or zero sequence elements in four-wire three-phase systems with neutral. When only sinusoidal reference voltages are generated, balanced algorithms are sufficient, but 3D techniques must be considered in the case of other cases.

A. SVM algorithms for Multilevel Balanced systems:

SVM has as its core idea that the state-space vector representation previously introduced can be used to combine and modulate three State-space vectors of the inverter, so that its time-period average is equal to the reference space vector. The SVM modelling concept can be summed up by

$$V_s^* = \frac{1}{T_s}(t_1 V_1 + t_2 V_2 + t_3 V_3) \qquad (3.2.10)$$

Where $T_s = t_1 + t_2 + t_3$ is a fixed period of modulation in PWM, V_1, V_2, and V_3, and the three vectors that are closest to the reference. It reduces the problem then to an algorithm that can find the nearest vectors to the reference and calculate the ON times of every vector t1, t2 and t3. Once calculated, each vector is created during the corresponding time, which is equal to the reference time of the desired average over Ts.

Additional challenges arise, such as the use of vector redundancies for other purposes, such as

the reduction of frequencies by using a specific sequence where the vectors are generated or for dc-link voltage imbalance control using redundancies.[49]

Several SVM algorithms were recorded depending on the prior notion. They differ in the manner in which the three closest vectors are chosen, the calculation of times, the sequence used to generate a vector and the computational effort required. The α-β plane is transformed by coordinate, moving the complex axis from 90^0 to 60^0, in respect of the α-axis, also referred to as the h-g or hexagonal co-ordinates. The benefit is that each vector can be normalised, instead of using fractional parts of the-axis, by two integer readings in the h and G-axis. This makes it much easier to determine the three nearest points to the target as they can be positioned with round (floor and ceiling) features. Furthermore, the ON moments can be achieved readily as fractional parts of the h and g-axis references.

The main difference is that the space vectors and the ON times are calculated using very simple geometrical considerations, and that the method of alternative SVM is based on this iteration algorithm in[50]. The necessary rotation in the iterative algorithm is prevented by this geometrical algorithm, which reduces the calculation costs even more. Moreover, this method always has the same low calculation costs and depends on the number of the converter levels.

The geometric modulation algorithm uses the standard reference voltage vector as an input, so that it is independent of the voltage of the dc-links and the converter voltage. Thus, the converter's state-space vectors are placed in geometric positions in the control area, which are denoted by complete values between zero and np-1, in which np is the number of the multilevel converter levels. Furthermore, this voltage is again normalized, scaling up the imagined portion and divided by $\sqrt{3}$[51]. The control region here is defined by triangular regions of 45^0 slope and makes it possible to determine switch sequence and ON times using very simple online calculations.

A. SVM algorithms for Multilevel Unbalanced Systems [52]:

The two-dimensional plane is not sufficient to fully represent the system in power converter with neutral connection (typically called unbalanced systems), since the common-mode voltages and currents via the neutral are not considered.

$$\gamma = (V_a + V_b + V_c).$$

This 3-D region now contains the reference vector and the switching states of the converter, which is the origin of 3D-SVM methods.

The $\alpha - \beta - \gamma$ representation gives interesting information about the zero-sequence element of currents and voltages, but the extra dimensions make the modulation algorithm more complex. The real cartesian co-ordinates are therefore used to promote these calculations for the modulation of 3-D multi-level converters. An expansion of the method for three-dimensional cartesian a–b–c planes in [52] presented has been noted. The 3D-SVM method considers the nearest four space vectors to the reference vector (four because the reference voltage vector is now mapped to the 3-D space). The monitoring region shall be described by a cube with vertex in the locations from zero to np-1 in each quadrant a, b, c, following a normalisation of the target voltage vector. This cube consists of a number of sub cubes, depending on the number of converter levels. For instance, three level converter state-space

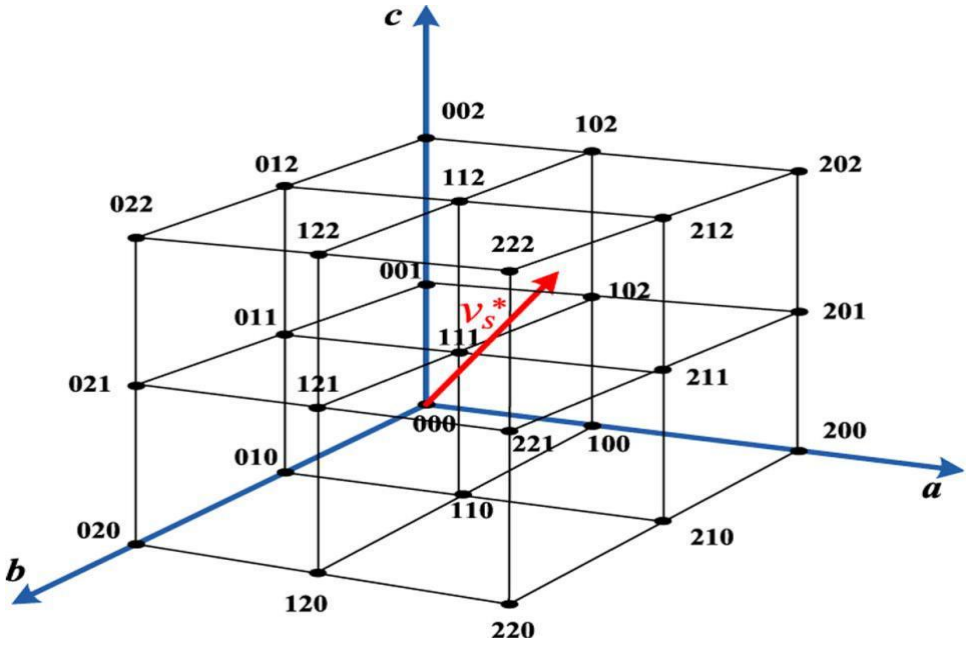


Fig3.7 state space vectors of a three phase three level converter using 3-D cartesian co ordinates

vectors are displayed in Fig.3.7. For these representations of space vectors, the switching states are defined as 0, 1 and 2 to -,0 and + respectively. This 3D-SVM algorithm takes account of the sub cube to the place of the target vector. The nearest vector in this sub cube can easily be calculated as the integer part of every component of the reference voltage vector to the normalization of the desired reference voltage vector.

The four closest vectors for state-space must be recognized within each sub-cube to the target vector [52]. The sub-cubes are divided into six normal tetrahedrons so that the 3D-SVM can

find the tetrahedron where the vector of reference lies, for the vertexes of this tetrahedron represent the state-space vectors used for modulation and for the sequence of switching. The tetrahedron determinations are a very quick, computer cost-effective method, since they imply easy similarities. In [52], a table is presented that summarizes the sequence of changes and the working cycles of each tetrahedron. The ON time numerical calculations are limited to easy conversions. It significantly reduces the requirements of computing and enables the method of modulation in the applications where a 3-D vector region (systems with or without neutrals, unbalanced loads, triple harmonics) is required, and this technique is independent of the number of converter levels. Finally, the 3D-SVM can also be used for competitive multi-level devices that achieve zero common-mode voltage.

3.5 Multi carrier pulse width modulation[53]-[55]:

The carrier-based modulation schemes [53]-[55] for multilevel inverters can be generally classified into two categories: phase-shifted and level-shifted modulations. Both modulation schemes can be applied to the cascaded H-bridge(CHB) inverters. An m-level CHB inverter using level-shifted multicarrier modulation scheme requires (m-1) triangular carriers, all having the same frequency and amplitude. The (m-1) triangular carriers are vertically disposed such that the bands they occupy are contiguous. In phase-shifted all the carriers have same amplitude and frequency and shifted by a certain phase angle.There are four PWM strategies with different phase relationships for the multicarrier modulation:

A. Phase disposition
B. Phase opposition disposition
C. Alternative phase opposition disposition
D. Phase shifting

A. Phase disposition [53]:

In phase disposition (PD) carrier-based PWM, all the carriers will be in same phase angle, same frequency and equal magnitude, but the difference will be in dc offsets so as to occupy contiguous bands. This is illustrated in Fig.3.8.The gate control is obtained when each of carrier waveforms with sinusoidal reference signal are compared, which in turn controls respective gate.

In the present work, in the carrier-based implementation the phase disposition PWM scheme is used. Fig. 3.8 demonstrates the sine-triangle method for a five-level inverter. Therein, the phase modulation signal is compared with four (n-1 in general) triangle waveforms.

waveforms.

The rules for the phase disposition method, when the number of level N = 5, are the N –1 = 5-1=4 carrier waveforms arearranged so that every carrier is in phase.

- The converter is switched to $+2V_{dc}$ when the reference is greater than four carrier waveforms.
- The converter is switched to $+V_{dc}$ when the reference is greater than lower carrier waveforms below reference and less than top most carrier waveform
- The converter is switched to zero when the reference is greater than the lower carrier waveforms but less than the upper carrier waveforms.
- The converter is switched to - V_{dc} when the reference is greater than lower most carrier waveform and less than the other three waveforms.
- The converter is switched to - $2V_{dc}$ when the reference is less than all four carrier waveforms.

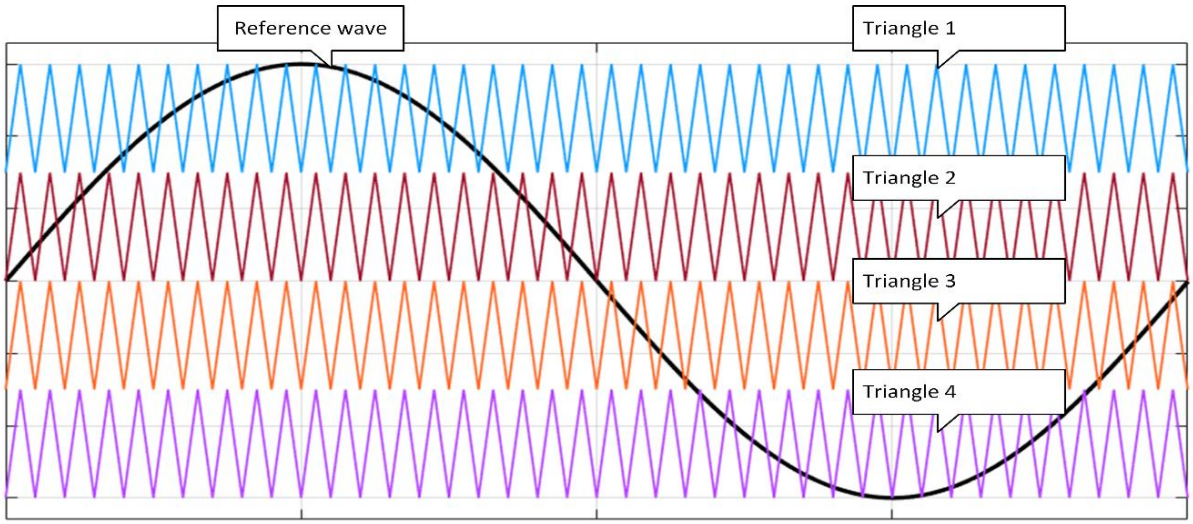


Fig 3.8. PD modulation carrier waveforms with reference waveform

In the carrier-based implementation, at every instant of time the modulation signals are compared with the carrier and depending on which is greater, the switching pulses are generated. As seen from Figure 3.9, the figure illustrates the switching pattern produced by the carrier-based PWM scheme. In the PWM scheme there are four triangles, the upper triangles ranges from 1 to 0 and the lower triangle ranges from 0 to –1. In the similar way for an N –level inverter, the (N-1) triangles are used and each has a peak-to-peak value of 2/ (N-1). Hence the upper most triangle magnitude varies from 1 to (1-2/ (N-1)), second carrier waveform from (1-4/ (N-1)), and the bottom most triangle varies from (2-2/ (N-1)) to –1. In Fig.3.9, simulation of carrier-based PWM scheme using the phase

disposition (PD) can be seen. The switching function for the devices is given by

- Reference < Triangle -1 & Reference > Triangle -2 & Triangle -3 & Triangle -4; P_1= 1 otherwise P_1= 0
- Reference > Triangle -1 & Triangle -2 & Triangle -3 & Triangle -4; P_2= 1 otherwise P_2= 0.
- Reference < Triangle -1 & Triangle -2 & Triangle -3 & Reference > Triangle -4; P_3= 1 otherwise P_3= 0.
- Reference < Triangle -1 & Triangle -2 & Triangle -3 & Triangle -4; P_4= 1 otherwise P_4= 0.

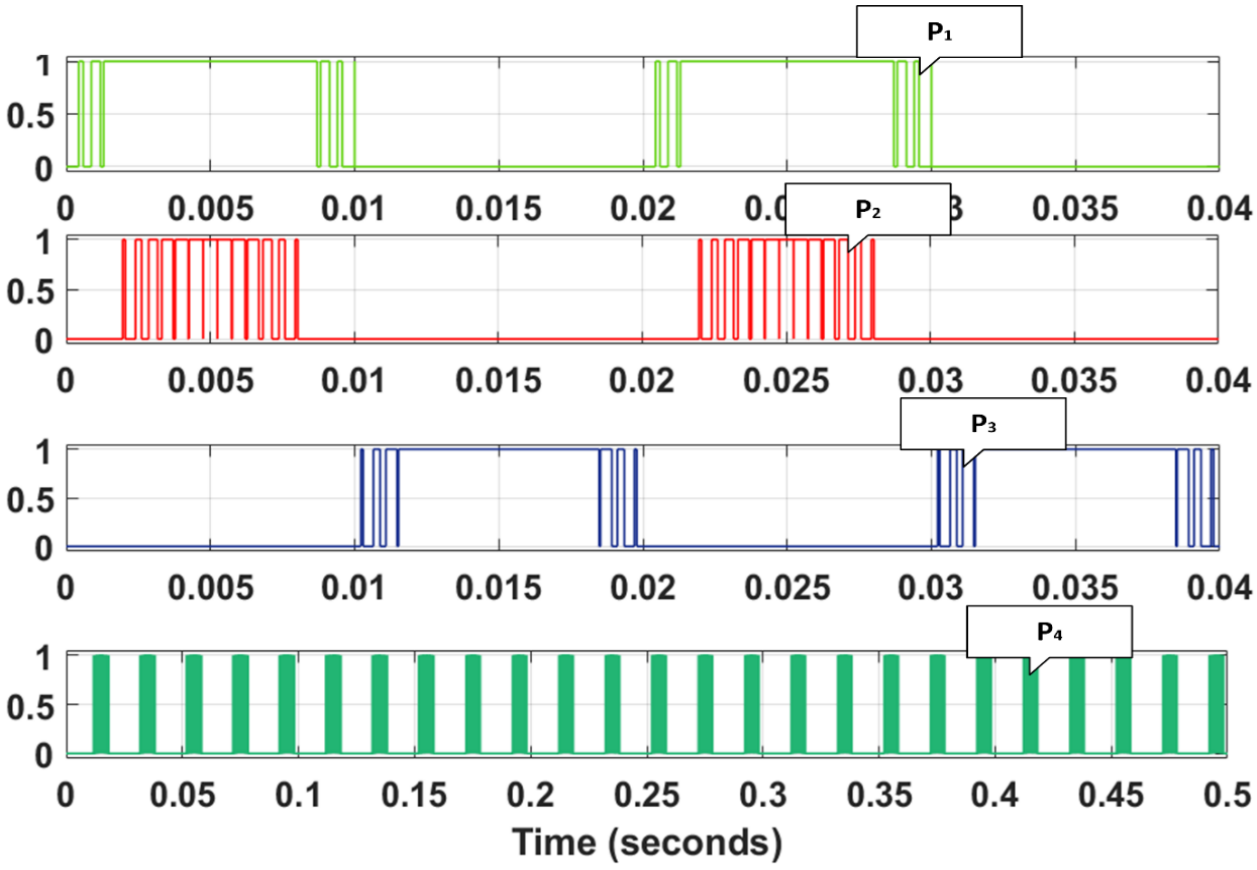


Fig 3.9. PD-PWM switching pattern

B. Phase opposition disposition[53]:

In this modulating technique as shown in Fig.3.10, phase opposition disposition (POD) carrier-based PWM, the carriers are having equal magnitude and same frequency, but the carriers have difference in dc offset and the carriers just above the zero reference will be in same phase angle and just below the zero reference carriers are in same phase angle and the phase angle difference between the above zero reference carriers and below zero reference carriers will have the 180^0 phase shift. The maximum harmonic energy is found around the carrier wave

frequency as side band harmonics.

The rules for the phase disposition method, when the number of level N = 5, are the N –1 = 5-1=4 carrier waveforms arearranged so that every carrier is in phase.

- The converter is switched to $+2V_{dc}$ when the reference is greater than four carrier waveforms.
- The converter is switched to $+V_{dc}$ when the reference is greater than lower carrier waveforms below reference and less than top most carrier waveform
- The converter is switched to zero when the reference is greater than the lower carrier waveforms but less than the upper carrier waveforms.
- The converter is switched to $-V_{dc}$ when the reference is greater than lower most carrier waveform and less than the other three waveforms.
- The converter is switched to $-2V_{dc}$ when the reference is less than all four carrier waveforms.

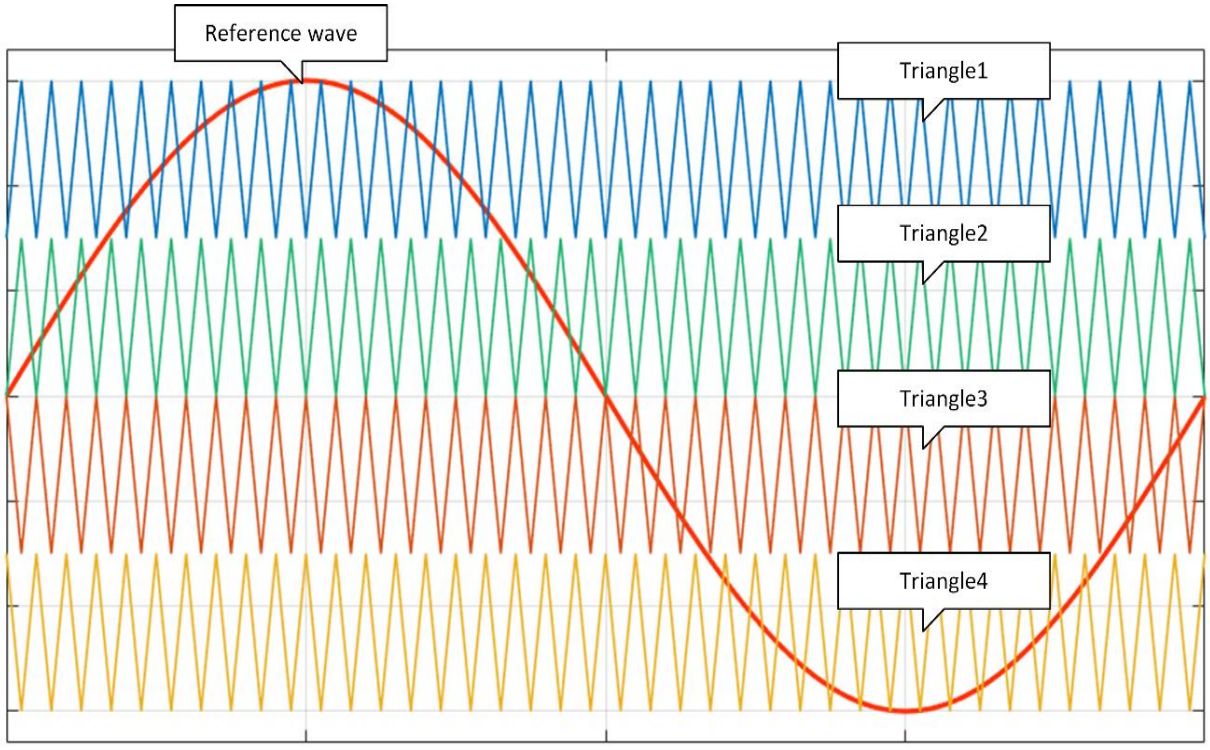


Fig 3.10. POD modulation carrier waveforms with reference waveform

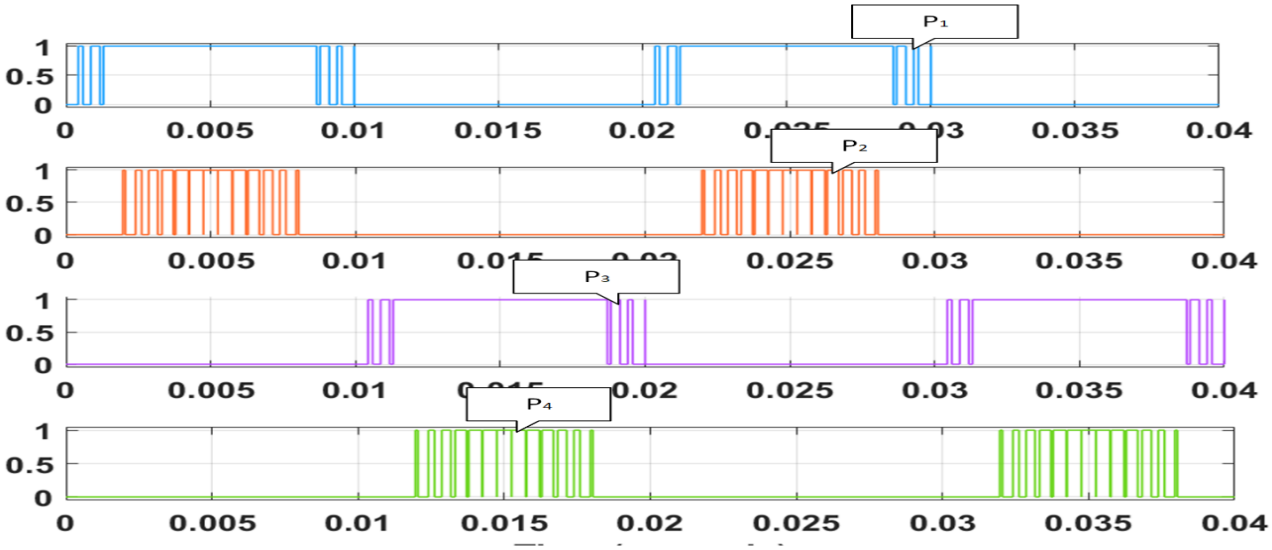


Fig 3.11. POD-PWM switching pattern

In Fig.3.11, simulation of carrier-based PWM scheme using the phase opposition disposition (POD) can be seen. The switching function for the devices is given by

- Reference < Triangle -1 & Reference > Triangle -2 & Triangle -3 & Triangle -4; P_1= 1 otherwise P_1= 0
- Reference > Triangle -1 & Triangle -2 & Triangle -3 & Triangle -4; P_2= 1 otherwise P_2= 0.
- Reference < Triangle -1 & Triangle -2 & Triangle -3 & Reference > Triangle -4; P_3= 1 otherwise P_3= 0.
- Reference < Triangle -1 & Triangle -2 & Triangle -3 & Triangle -4; P_4= 1 otherwise P_4= 0.

C. Alternative phase opposition disposition[53]:

In alternate phase opposition disposition (APOD) carrier-based PWM, all the carriers will have equal magnitude and same frequency, but the carriers have difference in dc offset and phase shifted by 180^0 alternately. The maximum harmonic energy is centred around carrier wave frequency as side band harmonics and no harmonics at carrier wave frequency. This is represented in Fig.3.12.

The rules for the phase disposition method, when the number of level N = 5, are the N –1 = 5-1=4 carrier waveforms arearranged so that every carrier is in phase.

- The converter is switched to $+2V_{dc}$ when the reference is greater than four carrier waveforms.

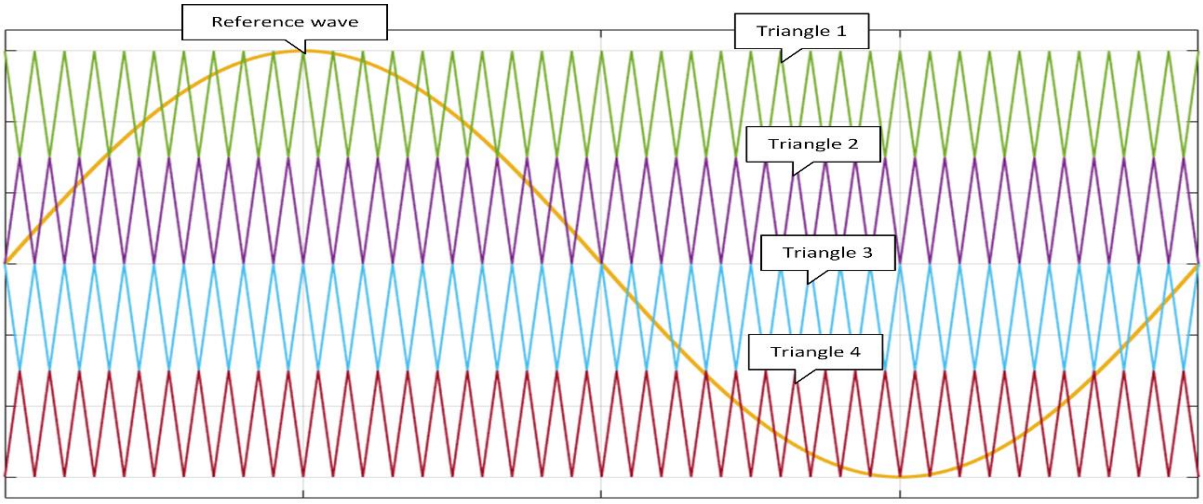


Fig 3.12. APOD modulation carrier waveforms with reference waveform

- The converter is switched to $+V_{dc}$ when the reference is greater than lower carrier waveforms below reference and less than top most carrier waveform
- The converter is switched to zero when the reference is greater than the lower carrier waveforms but less than the upper carrier waveforms.
- The converter is switched to $-V_{dc}$ when the reference is greater than lower most carrier waveform and less than the other three waveforms.
- The converter is switched to $-2V_{dc}$ when the reference is less than all four carrier waveforms.

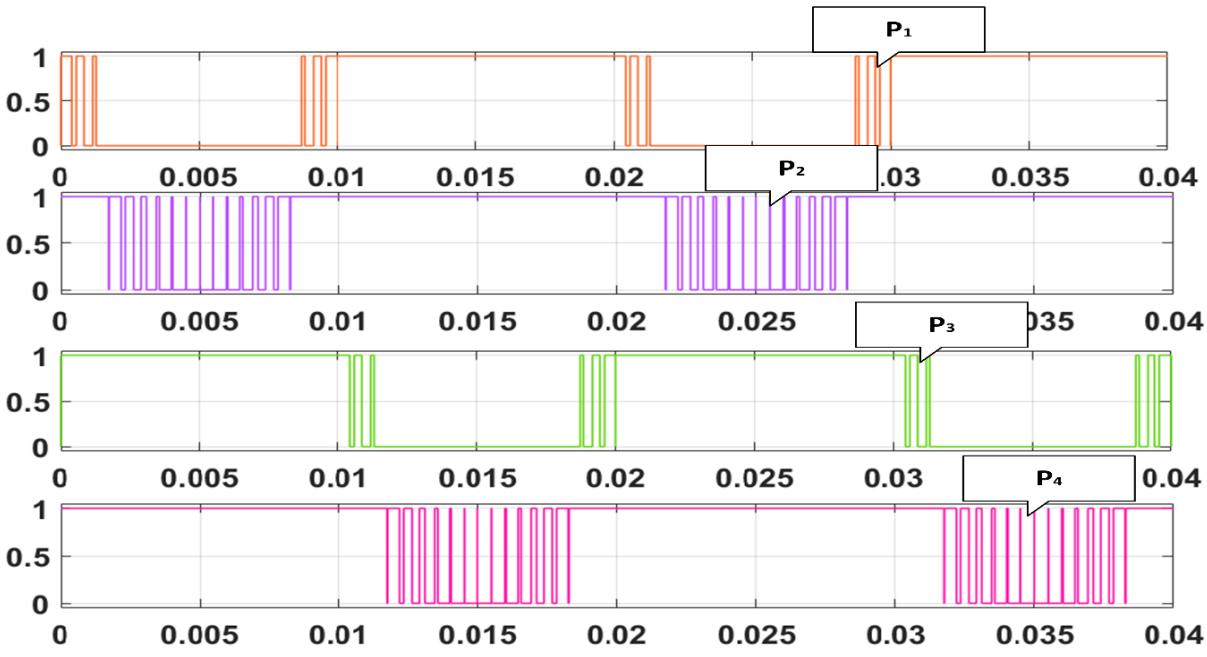


Fig 3.13. APOD-PWM switching pattern

In Fig.3.13, simulation of carrier-based PWM scheme using the alternative phase opposition disposition (APOD) can be seen. The switching function for the devices is given by

- Reference < Triangle -1 & Reference > Triangle -2 & Triangle -3 & Triangle -4; P_1= 1 otherwise P_1= 0
- Reference > Triangle -1 & Triangle -2 &Triangle -3 & Triangle -4; P_2= 1 otherwise P_2= 0.
- Reference < Triangle -1 & Triangle -2 & Triangle -3 & Reference >Triangle -4; P_3= 1 otherwise P_3= 0.
- Reference < Triangle -1 & Triangle -2 & Triangle -3 & Triangle -4; P_4= 1 otherwise P_4= 0.

B. Phase shifting[55]-[59]:

In phase shifting (PS) carrier-based PWM[55]-[59], all the carriers will have equal magnitude and same frequency and dc offset but the difference is that, each carrier will have certain phase shift angle π/m where, m= number of cascaded H bridges that are connected in series. This technique gives rise to cancellation of all the carrier and associated sideband harmonics. This is represented in Fig.3.14.

In Fig.3.15, simulation of carrier-based PWM scheme using the alternative phase opposition disposition (APOD) can be seen. The switching function for the devices is given

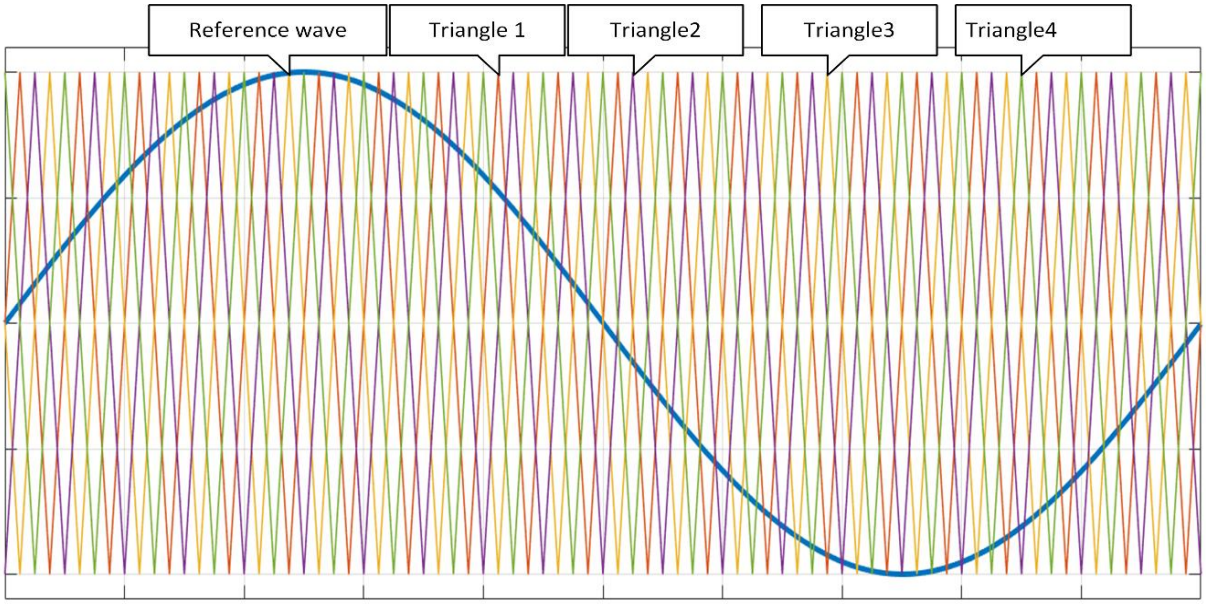


Fig 3.14. PS modulation carrier waveforms with reference waveform

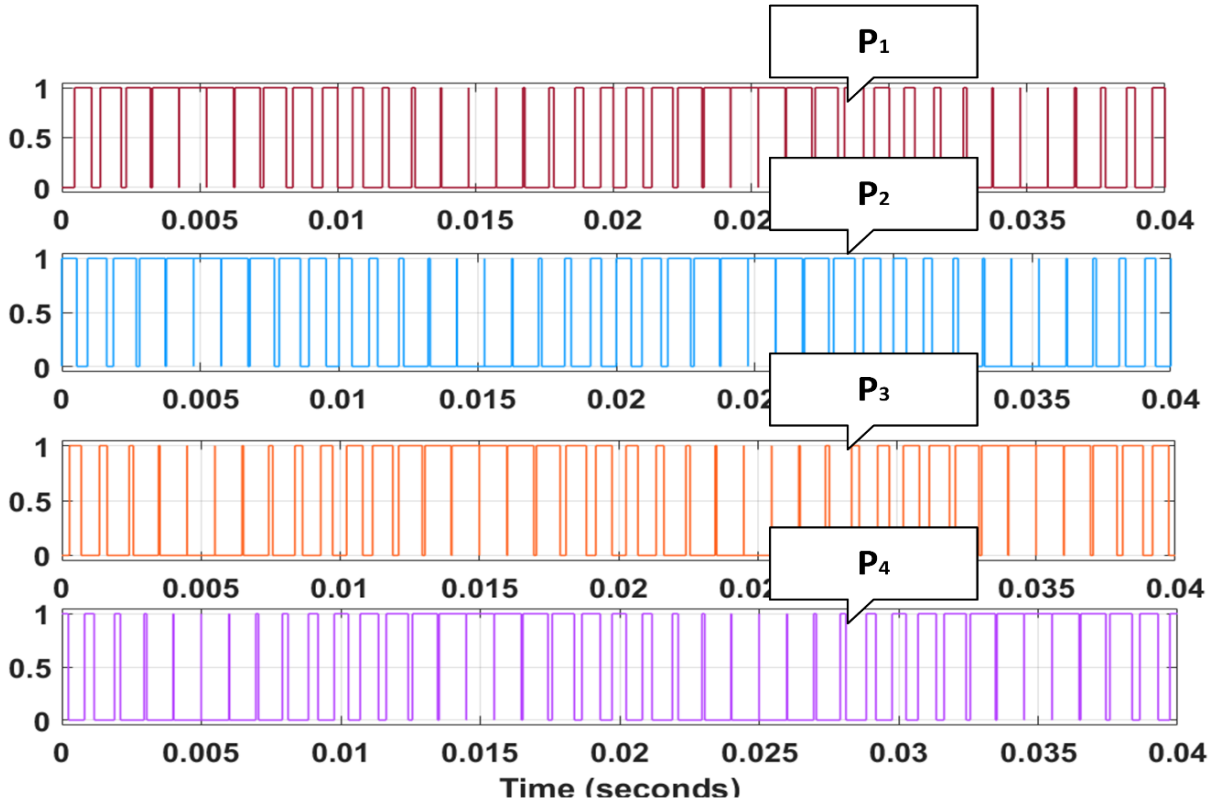


Fig 3.15. PS-PWM switching pattern

- Reference < Triangle -1; P_1= 1 otherwise P_1= 0
- Reference > Triangle -1 P_2= 1 otherwise P_2= 0.
- Reference < Triangle -1; P_3= 1 otherwise P_3= 0.
- Reference < Triangle -1; P_4= 1 otherwise P_4= 0.

3.6 Results:

Various modulation techniques have been implemented upon Cascaded H-Bridge multilevel Inverter and have been displayed below. Phase Disposition pulse width modulation have been implemented and output voltage wave form of five level cascaded H-bridge multilevel inverter is shown in Fig. 3.16. Phase opposition Disposition pulse width modulation have been implemented and output voltage wave form of five level cascaded H-bridge multilevel inverter is shown in Fig. 3.17. Alternative Phase opposition Disposition pulse width modulation have been implemented and output voltage wave form of five level cascaded H-bridge multilevel inverter is shown in Fig. 3.18. Phase Shifting pulse width modulation have been implemented and output voltage wave form of five level cascaded H-bridge multilevel inverter is shown in Fig. 3.19.

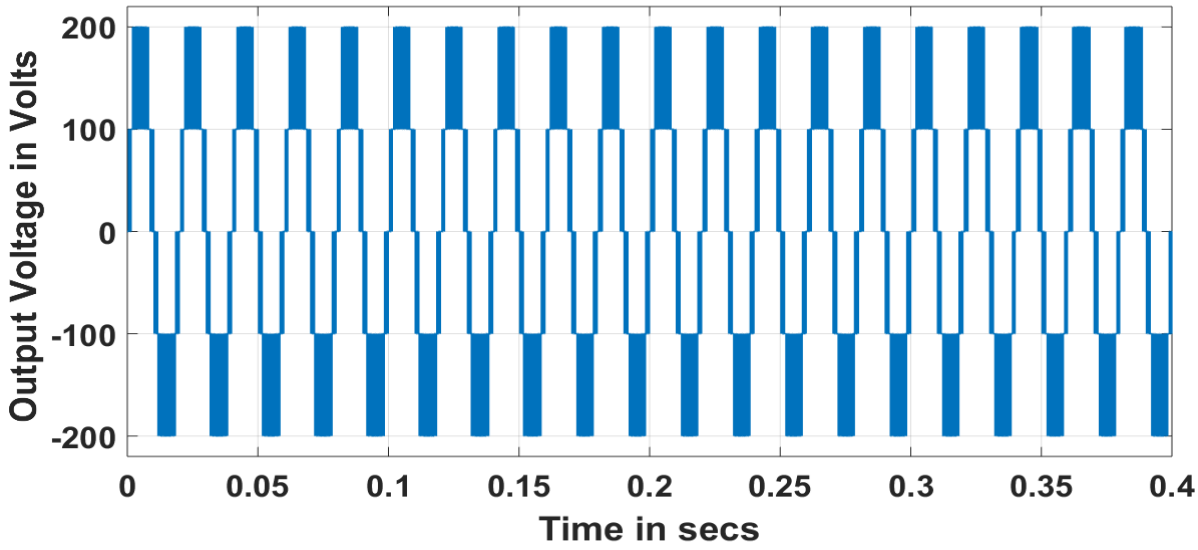


Fig. 3.16 Output Voltage Wave form of Phase Disposition-PWM

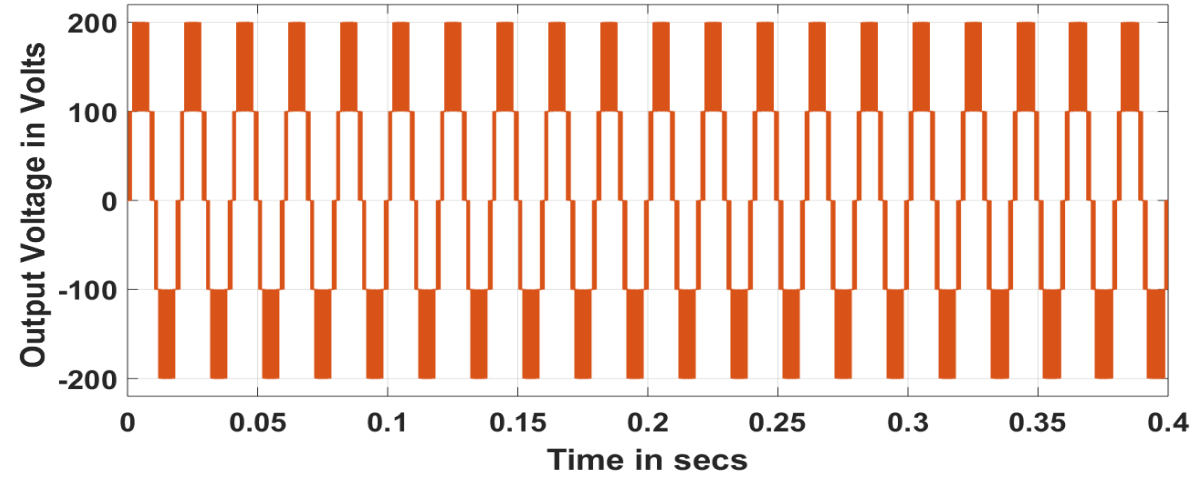


Fig. 3.17 Output Voltage Wave form of Phase Opposition Disposition-PWM

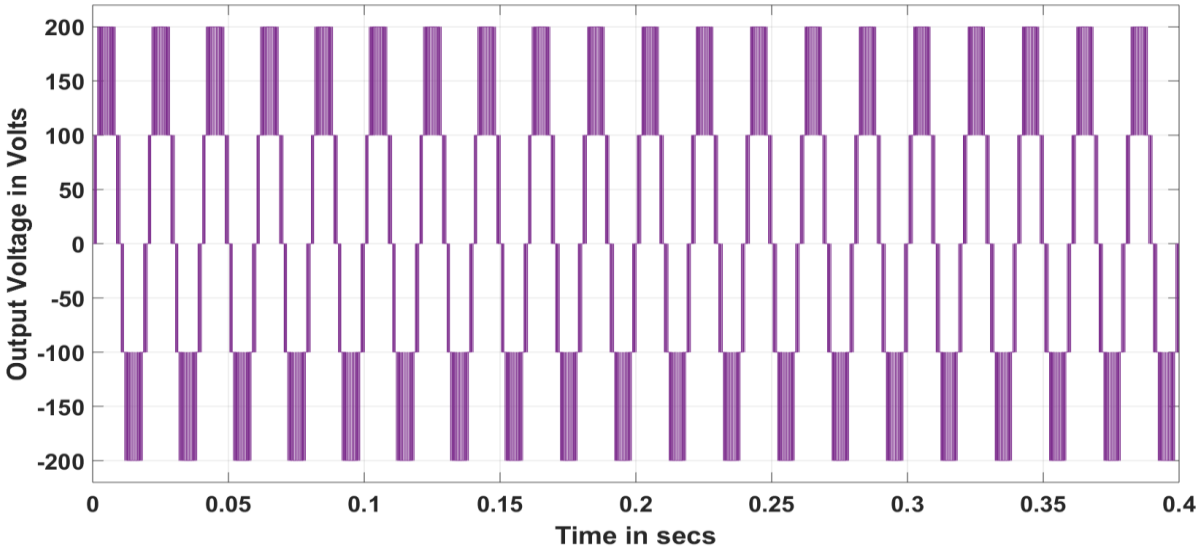


Fig. 3.18 Output Voltage Wave form of Alternative Phase Opposition Disposition-PWM

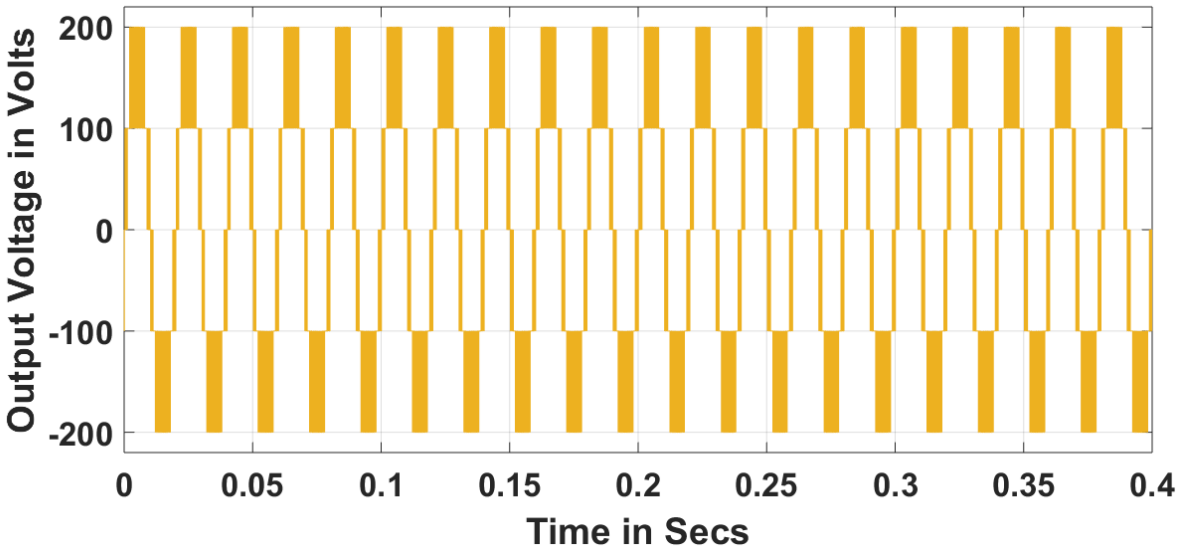


Fig. 3.16 Output Voltage Wave form of Phase Shifting-PWM

3.7 Conclusions:

From the above results, we have been found that that THD values for the PD-PWM has 30.59% and for the POD-PWM has 31.59% and APOD has 31.78% and PS-PWM has 29.59%.From the above THD values we can conclude that Phase Shifting technique gives less percentage THD as compared to the other techniques. It is preferable to use PS-PWM technique for Five level cascaded H bridge multilevel inverter.

Chapter 4

Application of Five-Level Converter as a Shunt Compensator

In this Chapter Five Level Cascaded-H Bridge Multilevel Inverter as Shunt active Filter is implemented. Phase Shifting Pulse Width Modulation is implemented for generation of pulses because of uniform distribution of voltage stress on each switch. This chapter involves switching frequency range 1-5 kHz for analysis of the operation of active shunt filter application of Five level Cascaded H-Bridge. The performance analysis is validated for linear and non-linear loads.

4.1. Basics of Shunt Compensator

The Distribution Static Compensator (DSTATCOM) [61]-[64] is a static compensator based on a voltage source converter that is used for the PQ mitigation problem. DSTATCOM is capable of continuously generating variable inductive or capacitive shunt compensation at the maximum MVA level. DSTATCOM is controlled to check the line waveform for the ac signal reference, which injects the right amount of reactive power compensation. The primary components for the DSTATCOM are presented in Fig. 4.1. It consists of a DC capacitor, one or more inverter modules, an ac filter, and a PWM control approach. A voltage-source inverter converts the dc voltage into three phase AC voltage in this DSTATCOM implementation, which can be connected to and synchronized to the AC line through a small tie reactor.

A DSTATCOM is similar to the basic operating principle of synchronous machine. The synchronous machine will provide lagging current when under excited and leading current when over excited. Similar to a synchronous machine, the DSTATCOM can produce and extract reactive power and can produce real power when supplied with an DC supply.

A) Real power exchange: DC capacitor needs to provide the necessary real power for the switches, as the switching devices are not lossless. Therefore, a real power exchange with an AC system is necessary in order to keep the capacitor voltage constant in the event of direct voltage control. The AC system also has a real power exchange if the DSTATCOM has been connected with an external DC source or renewable source is connected. The actual power from the capacitor or DC supply is provided to the AC circuit to control the device voltage if the VSC input voltage leads system voltage

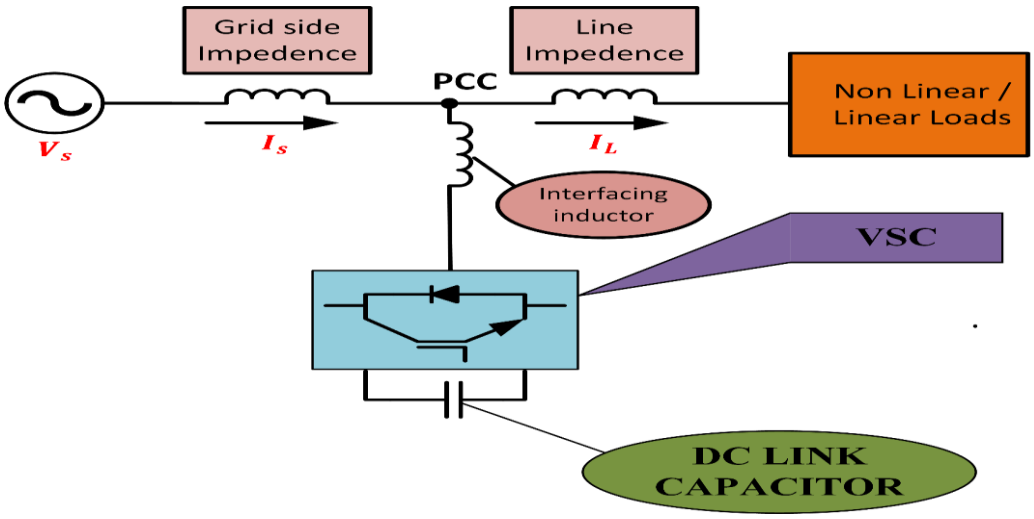


Fig 4.1 Single line diagram of DSTATCOM

B) Reactive power exchange: The DSTATCOM will supply Q act as a capacitor when the output voltage of the converter is higher than the system voltage, and generate reactive power.

The exchange of real power and reactive power between the voltage converter and AC system is the main phenomenon required to regulate distribution system. DSTATCOM provides reactive power, as necessary, for reactive power compensation and therefore keeps source current at the unity power factor (UPF). Since the source supplies only real power, the balance of load is achieved by balancing the source reference current. The source of reference used for determining DSTATCOM's switching has a fundamental frequency component of the load current extracted through different control techniques.

On the transmission level, STATCOM only covers basic reactive power and offers voltage support, while DSTATCOM is used for power factor enhancement and voltage control on the supply stage or at load point. In the distribution network, DSTATCOM can be one of the viable SVC alternatives. A DSTATCOM can also act as an active shunt filter in order to eliminate unbalance or distortions in the source power or voltage according to the standard limits. DSTATCOM is a multifunctional device and can be suitably controlled to achieve PQ improvement feature.

Every compensation scheme aims primarily to have a quick, flexible and easy to implement response. The DSTATCOM control algorithms are mostly used for the following steps:

- Systems voltage and current measurements
- Conditioning of the signal

- Compensation signal calculation
- Pulse generation of switching devices

Generating proper PWM firing pulses is the major part of DSTATCOM control algorithm and has a major effect on compensation objectives, both transient and stable state performance. Because DSTATCOM shares a number of concepts with STATCOM, a few control algorithms have been directed into a DSTATCOM using Pulse Width Modulation (PWM) rather than Fundamental Frequency Switching (FFS) methods.

4.2 System description and design:

A Five-level CHBMLI-based DSTATCOM shown in Fig.4.2 is analysed and investigated, and connected to the grid via an L filter. The CHBMLI (VSC) provides power capacities comparable to the classic three-level inverter for the DSTATCOM implementation. The only difference among the inverters is that the earlier inverter needs more gate signals. But the advantage of the proposed system is that the converter voltage is subject has reduced total harmonic distortion (THD). Using the suitable power system with an optimal inverter stage, a voltage sensor inverter is produced that can produce parallel voltage at input voltage. The DSTATCOM analysis is also carried out using the filter used between the system and VSC. The inverter voltage level is −2Vdc, −Vdc, 0, Vdc and 2Vdc, which are added to supply the synchronization of the MLI output. The voltage waveform comprises of five levels with two H bridges, each stage of the five-level cascaded converter.

4.2.1 DC Link Bus Voltage:

The DC bus voltage (V_{DC}) value depends on the lowest voltage level required for the required AC output voltage during the VSC DSTATCOM PWM operation. The DC voltage is defined over the capacitor as

$$V_{DC} = \sqrt{2}V/m \qquad (4.2.1)$$

Where m is the modulation index and V is the AC output phase voltage of the DSTATCOM. The designed value is chosen to be 200V for a voltage input of 110V.

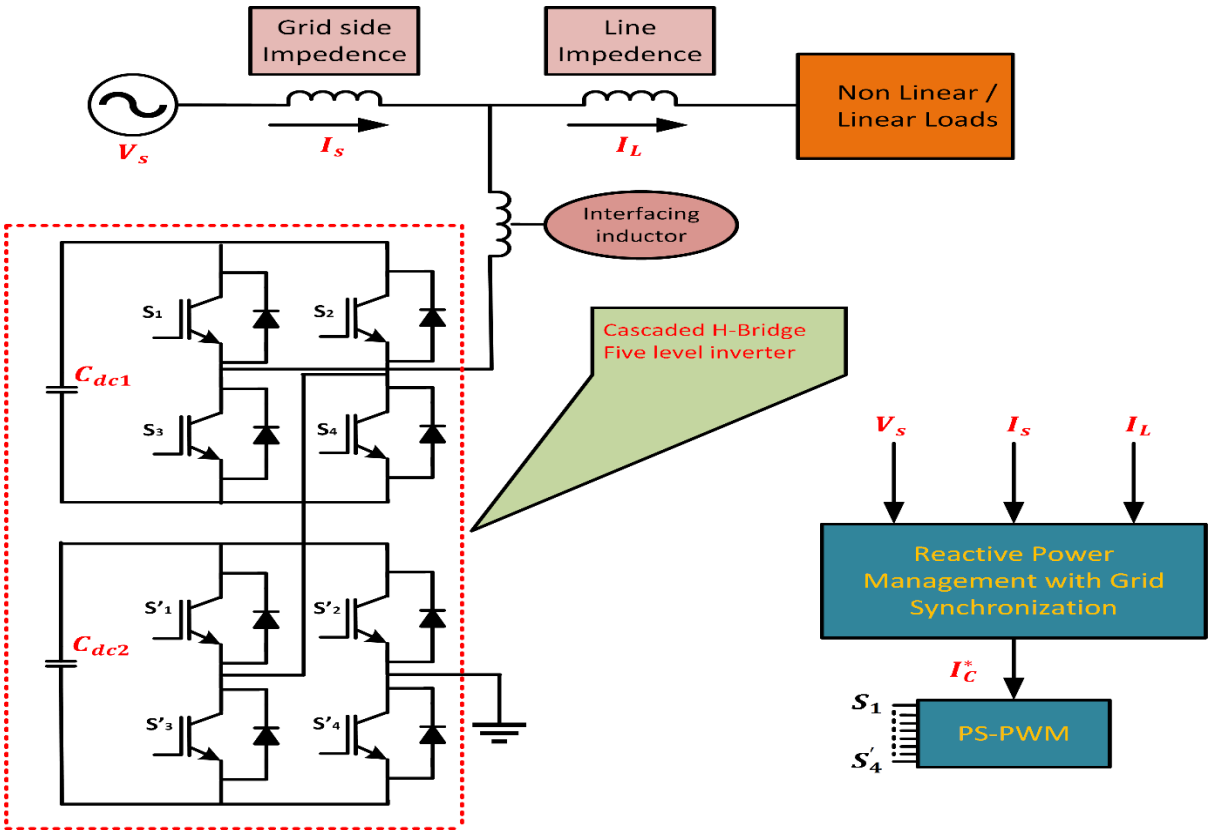


Fig .4.2 Five Level Cascaded H-Bridge Multilevel Inverter as DSTATCOM

4.2.2 Selection of a DC Bus Capacitor:

DC capacitor is designed by lowering the DSTATCOM DC bus voltage upon load application and increasing the DC bus voltage upon load removal. However, in the DC bus voltage, the second harmonic is shown under unbalanced load conditions. The capacitance is calculated across the capacitor as

$$C_{DC} = I_o/(2\omega V_{DC,ripple}) \tag{4.2.2}$$

Where I_o is the capacitor current, ω is the angular frequency, and $V_{DC,ripple}$ is the ripple in capacitor voltage. The designed value is chosen to be 1650μF.

4.2.3 Selection of Interfacing Inductor:

The selection of the Interfacing Inductor depends on the current ripple I_{ripple}. Inductor value is taken as 5mH calculated from the eq.4.2.3

$$L_f = mV_{DC}/(4af_sI_{ripple}) \tag{4.2.3}$$

4.3 SYNCHRONOUS d-q THEORY:

4.3.1 Three-phase d-q transformation:

Three voltage / current signals (ABC) for the 3-phase system are then turned to an orthogonal stationary frame (α-β) by use of (4.3.1) and to a synchronous (d-q) frame. The necessary components can be extracted in d-q frame according to the control requirements. The reverse transformation from d-q to α-β and then to ABC frame is performed, with help of (4.3.3)and (4.3.4) respectively, in order to generate the reference signals and return them to the original frame.

abc to α-β transformation:

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & 1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \quad (4.3.1)$$

Where x represents the variable under consideration, and can be voltage or current

α-β to d-q transformation:

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \begin{bmatrix} sin\theta & -cos\theta \\ cos\theta & sin\theta \end{bmatrix} \cdot \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \quad (4.3.2)$$

d-q to α-β inverse transformation:

$$\begin{bmatrix} x_\alpha{}^* \\ x_\beta{}^* \end{bmatrix} = \begin{bmatrix} sin\theta & cos\theta \\ -cos\theta & sin\theta \end{bmatrix} \cdot \begin{bmatrix} x_d{}^* \\ x_q{}^* \end{bmatrix} \quad (4.3.3)$$

α-β to abc inverse transformation:

$$\begin{bmatrix} x_a{}^* \\ x_b{}^* \\ x_c{}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ 1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} x_\alpha{}^* \\ x_\beta{}^* \end{bmatrix} \quad (4.3.4)$$

In (4.3.3) and (4.3.4) the quantities with notation "*" represent the reference signals

A simple and efficient method is used to calculate the output of the unit vector model in SRF method to produce the synchronisation template. It has an significant role to play in the AC Grid synchronization The main voltage and power can ideally be presumed to be sinusoidal, regardless of the composition of the load current without phase shifts. The required source voltage can be considered to be sinusoidal and

$V_{sa}=V_{sm}*\sin\omega t$ (4.3.5)

$V_{sb}=V_{sm}*\sin(\omega t\text{-}120^0)$ (4.3.6)

$V_{sc}=V_{sm}*\sin(\omega t+120^0)$ (4.3.7)

Where V_{sm} denotes the peak value of the source voltage and ω is the angular fundamental frequency. The unit voltage model is determined by the equation below.

$U_a=V_{sa}/V_{sm}=\sin\omega t$ (4.3.8)

$U_b=V_{sb}/V_{sm}=\sin(\omega t-120^0)$ (4.3.9)

$U_c=V_{sc}/V_{sm}=\sin(\omega t+120^0)$ (4.3.10)

Next, instantaneous source voltages are sensed and transform using Clarke transform equation from the three-phase voltage to the α-β component . The voltage in α-β coordinates is the output of Clarke transformations that can be simplified as in the below equations.

$$V_{s\alpha}=\frac{\sqrt{3}}{2}V_{sm}\sin(\omega t) \quad (4.3.11)$$

$$=\frac{\sqrt{3}}{2}V_{sm}\cos(\omega t) \quad (4.3.12)$$

The generated estimated space vector magnitude is given by Equation

$$V_s=V_{s\alpha}+jV_{s\beta}=\sqrt{{V_{s\alpha}}^2+{V_{s\beta}}^2} \quad (4.3.13)$$

By dividing the α-β components of the source voltage with the magnitude of space vector, the unit vector generation is thus defined as

$$cos\theta=\frac{V_{s\alpha}}{\sqrt{{V_{s\alpha}}^2+{V_{s\beta}}^2}}=\sin\omega t \quad (4.3.14)$$

$$sin\theta=\frac{V_{s\beta}}{\sqrt{{V_{s\alpha}}^2+{V_{s\beta}}^2}}=-\cos\omega t \quad (4.3.15)$$

One of the advantages of this system is that the angle of the current is measured directly from the source voltage to allow for frequency independence.

4.3.2 Single-phase d-q Transformation:

However, transformation of the park in (4.3.1) applies to three-phase systems. An analog modification is needed in order to implement the concept of d-q transformation successfully for the single-phase system. Here a method by which a single-phase system can be directly represented in α-β frames without the use of a transformation matrix. In order to attain linear α

signal, along with the imaginary signal, could thus be seen in the orthogonal α-β frame as equivalent depiction of a single-phase system. This method was later developed as a p-q concept of one-phase. The load current in a α-β frame can be represented as a single stage p-q theory as [4.3.16-4.3.18]:

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} = \begin{bmatrix} i_L(\omega t + \varphi) \\ i_L(\omega t + \varphi + \pi/2) \end{bmatrix} \tag{4.3.16}$$

The approach to use an imaginary variable as a single-phase p-q theory to reflect the single-phase system in d-q frame described. The d-q frame representation in (4.3.16) shown as:

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \begin{bmatrix} sin\theta & -cos\theta \\ cos\theta & sin\theta \end{bmatrix} \cdot \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} \tag{4.3.17}$$

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \begin{bmatrix} \overline{i_{Ld}} + \widetilde{i_{Ld}} \\ \overline{i_{Lq}} + \widetilde{i_{Lq}} \end{bmatrix} = \begin{bmatrix} i_{L\alpha}.sin\theta - i_{L\beta}.cos\theta \\ i_{L\alpha}.cos\theta + i_{L\beta}.sin\theta \end{bmatrix} \tag{4.3.18}$$

The basic active and reactive current components in load i_L are the terms $\overline{i_{Ld}}$ and $\overline{i_{Lq}}$ which are DC terms, while the AC terms $\widetilde{i_{Ld}}$ and $\widetilde{i_{Lq}}$ represent the harmonic, active, reactive current components. With Low pass filter (LPF) and High pass filter (HPF), the AC and DC components can be easily extracted from the i_{Ld} and i_{Lq} respectively. Two types of control techniques, namely direct and indirect, are possible. An indirect current control method is considered in this report. In indirect control, only a DC component of current i_{Ld} is used to generate the reference current signal for the source current. This is because ideally, only a fundamental active portion of the load demand should be supplied from the source, and shunt APF should support load harmonics and reactive energy requirements .

Therefore, reference d,q components are computed as

$$\begin{bmatrix} {i_{Ld}}^* \\ {i_{Lq}}^* \end{bmatrix} = \begin{bmatrix} \overline{i_{Ld}} + 0 \\ 0 + 0 \end{bmatrix} \tag{4.3.19}$$

The reference source current signal in α-β frame can be transformed to α,β and transformed to Single phase system quantities.

$$\begin{bmatrix} {i^*}_{s\alpha} \\ {i^*}_{s\beta} \end{bmatrix} = \begin{bmatrix} sin\theta & -cos\theta \\ cos\theta & sin\theta \end{bmatrix}^{-1} \begin{bmatrix} {i_{Ld}}^* \\ {i_{Lq}}^* \end{bmatrix} \tag{4.3.20}$$

$$\begin{bmatrix} {i^*}_{s\alpha} \\ {i^*}_{s\beta} \end{bmatrix} = \begin{bmatrix} sin\theta & cos\theta \\ -cos\theta & sin\theta \end{bmatrix} \cdot \begin{bmatrix} \overline{i_{Ld}} + i_{dc} \\ 0 \end{bmatrix} \tag{4.3.21}$$

The term i_{dc} in (4.3.21) represents the required component for a continuous, self-supporting DC bus voltage throughout the active filter. The word $i^*_{s\beta}$ is the imaginary component of the original system.

$$i^*_s(\omega t) = i^*_{s\alpha}(\omega t) = \sin(\theta)\,.\,(\bar{\imath}_{Ld} + i_{DC}) \tag{4.3.22}$$

The block diagram of d-q synchronous indirect current controller-based reference frame is shown in Fig. 4.3. As noted in (4.3.21), the source current generated is independent of the supply voltage profile. In other words, if supply voltage is distorted the d-q single-phase theory can be used.

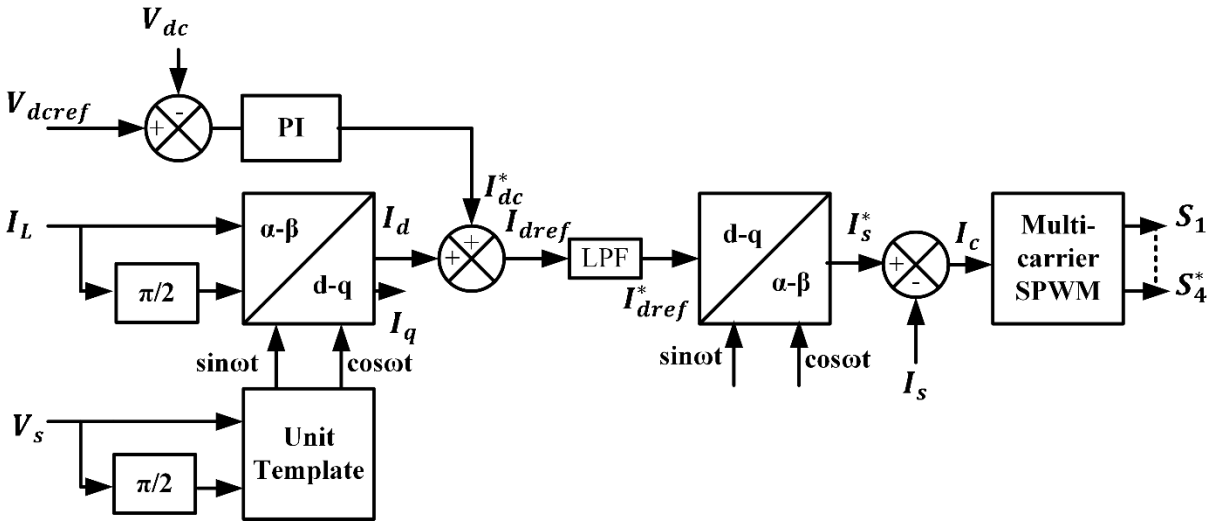


Fig.4.3 Block diagram of d-q Synchronous indirect current control

4.3 Results and Discussion:

In the unity power factor (UPF) mode, the system DSTATCOM shown in Figure 4.2 was implemented and controlled and simulated to force the grid to supply the essential active components of the power through the correct generation of the reference current. In linear and non-linear operations under UPF, the CHBMLI-based DSTATCOM created by MATLAB Simulink (2018b) was analyzed. The values of every parameter of the proposed system are displayed in Table 4.1. These values are applied to the 110V line-to-line voltage system, provided that two bridges are located in the system, generating the same levels of voltage, and maintaining a value of 100V on each bridge.

Table.4.1 Simulation Data used to describe the DSTATCOM performance

S. No.	Simulation Parameter	Values
1	Source voltage	110V
2	Frequency	50Hz
3	Source Reactance	0.05mH
4	L Filter	5mH
5	DC Link Voltage	200V
6	K_p, K_i	0.5,10
7	DC Capacitor	1650µF
8	Switching Frequency	1KHz
9	Linear Load	500VA
10	Non-Linear Load	15Ω,20mH

4.4.1 Linear Load Condition:

In view of the linear load connected to the system, the efficiency of the DSTATCOM system is analysed. The resulting reference current force DSTATCOM to supply the reactive power that the load requires, thus it is observed that the supply voltage is in phase supply current. Fig.4.4 shows a source voltage and a current for the DSTATCOM output to show the grid in UPF. In case of DSTATCOM load performance analysis, load current and DSTATCOM current a linear load of up to 0.4 Secs and a non-linear load change of 0.4 s is shown respectively in Fig.4.5-Fig.4.6 The compensation current allows the source current to supply a balanced active power as shown in Figure 4.7, The entire DC voltage connection is retained at a steady voltage of 200V and at each single H-bridge voltage remains at 100V as shown in Fig.4.8. The output and PCC voltage of the multi-level inverter as shown in Fig. 4.9.

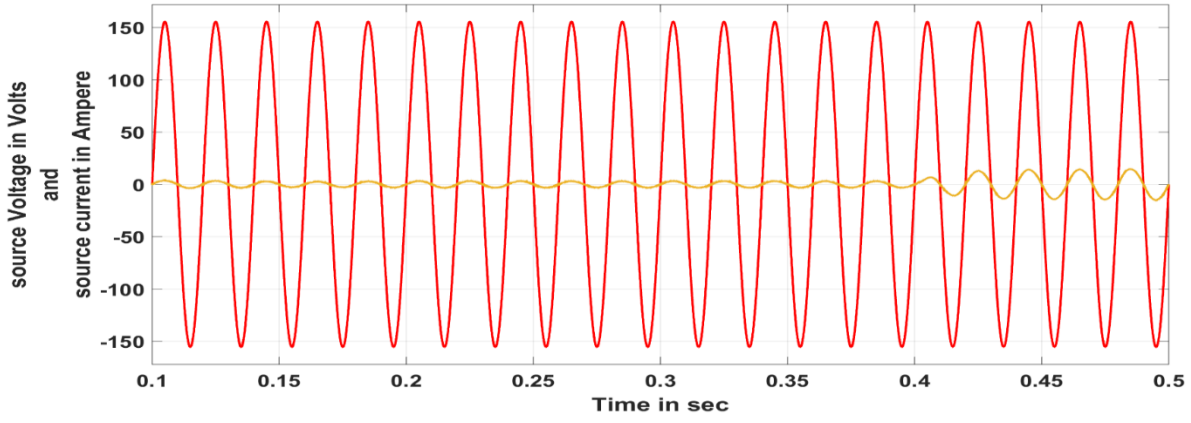


Fig 4.4 Source Voltage and Source current Waveforms with Load change at 0.4 s

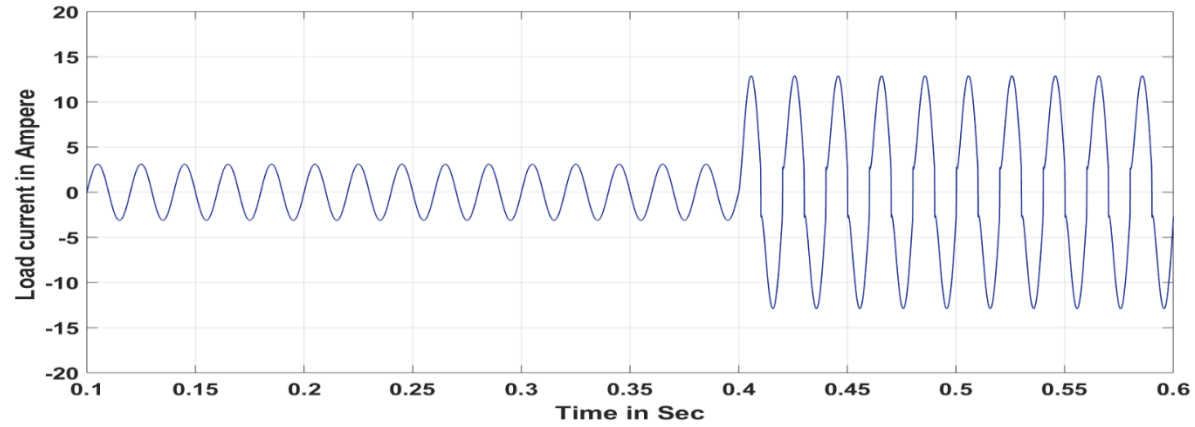


Fig 4.5 Load current waveforms with load change at 0.4 s

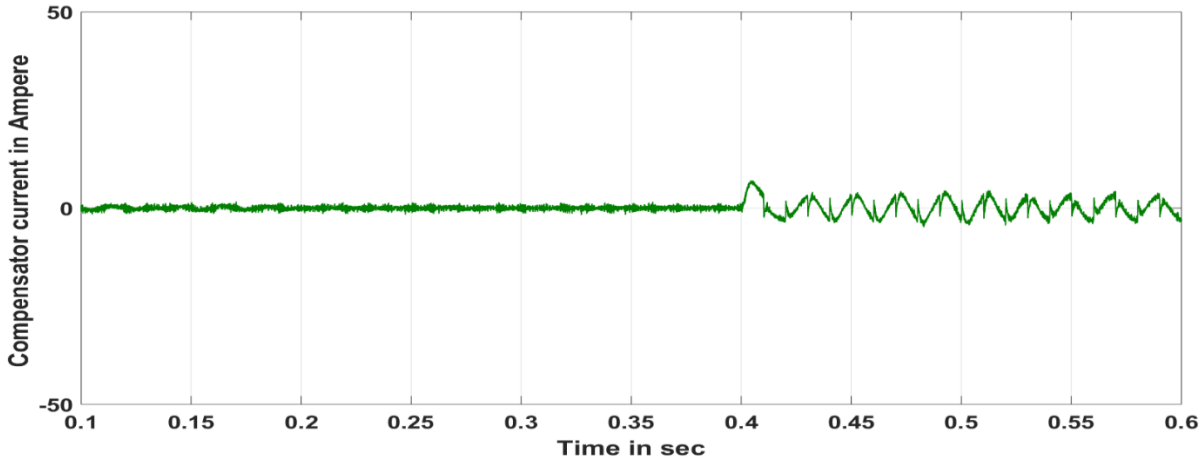


Fig 4.6 DSTATCOM current waveform with load change at 0.4 s

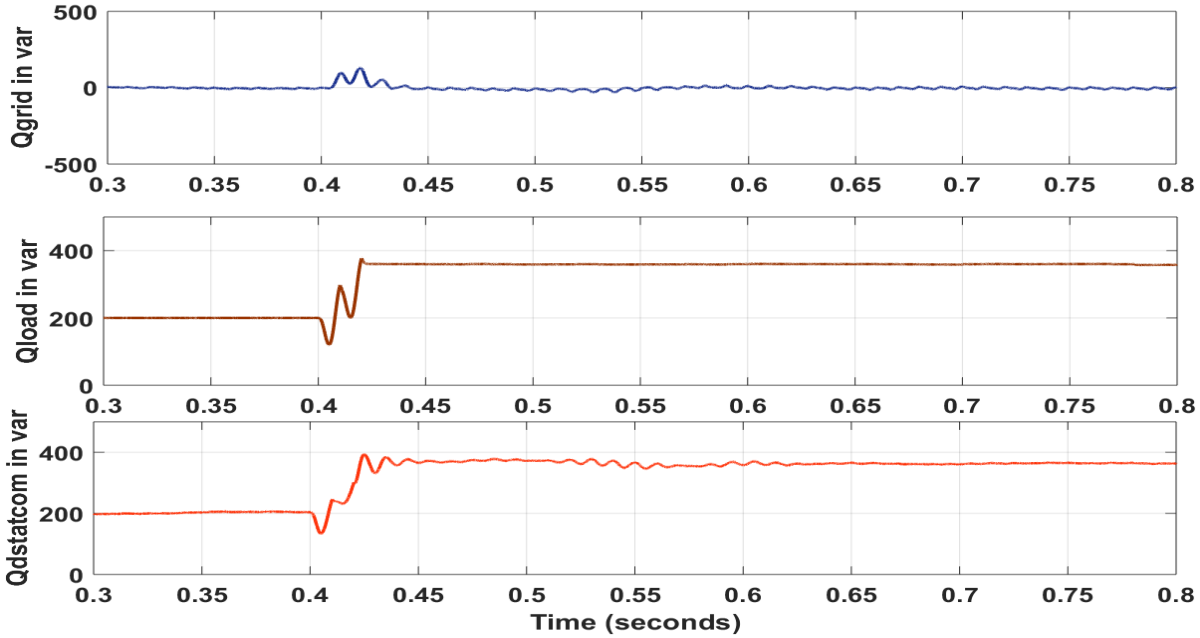


Fig.4.7 Reactive Power of Grid and DSTATCOM and Load with load change at 0.4 s

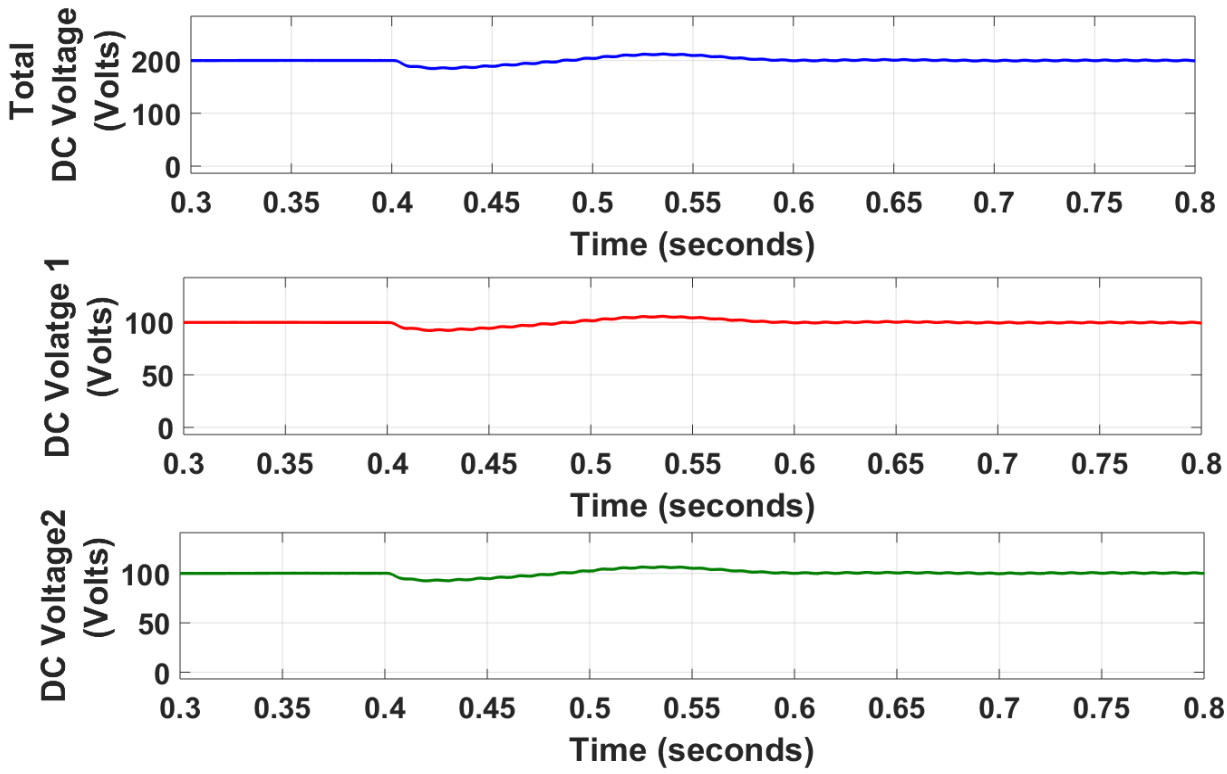


Fig 4.8. Total and Individual DC link voltage waveforms with load change at 0.4 s

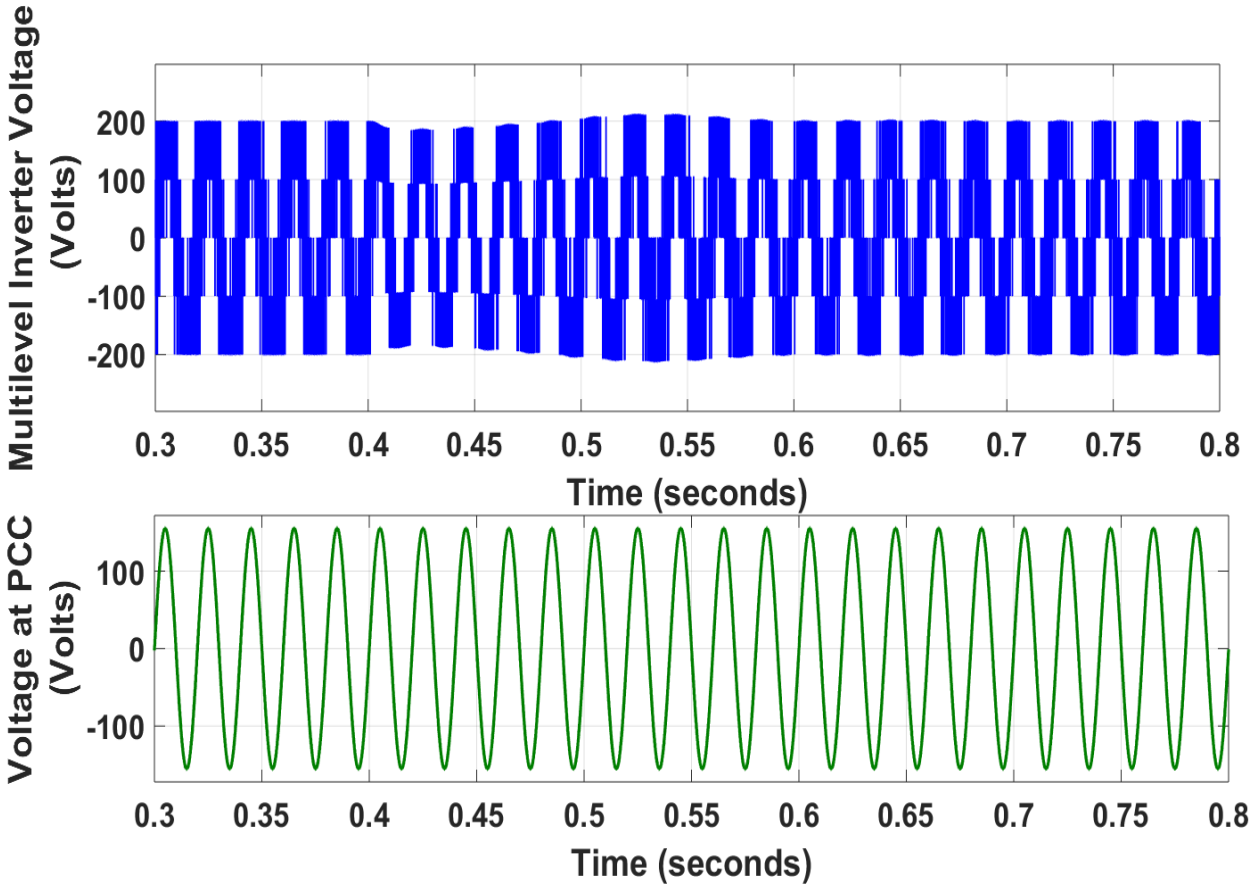


Fig 4.9. PCC and Multilevel inverter output voltage waveforms with load change at 0.4 s

4.4.2 Non-Linear Load condition:

In view of the nonlinear load condition needed to validate the system performance, DSTATCOM System was examined. A non-linear type load was considered as an R-L diode bridge rectifier with the nonlinear load change at 0.4 s. It is observed that the current is in phase with supply voltage and reactive power is supplied by DSTATCOM . In Fig. 4.10, the source voltage and current for the DSTATCOM output is shown. For DSTATCOM performance evaluation, Load and the DSTATCOM current are shown in Fig.4.11 to Fig.4.12. The compensating current allows for a balanced active load power supply, as illustrated in Fig. 4.13. The complete DC link voltage remains constant at 200V and at each single H bridge dc link voltage is maintained at 100 V. illustrated in Fig. 4.14. As shown in Fig. 4.15, multilevel inverter and PCC voltage are provided.

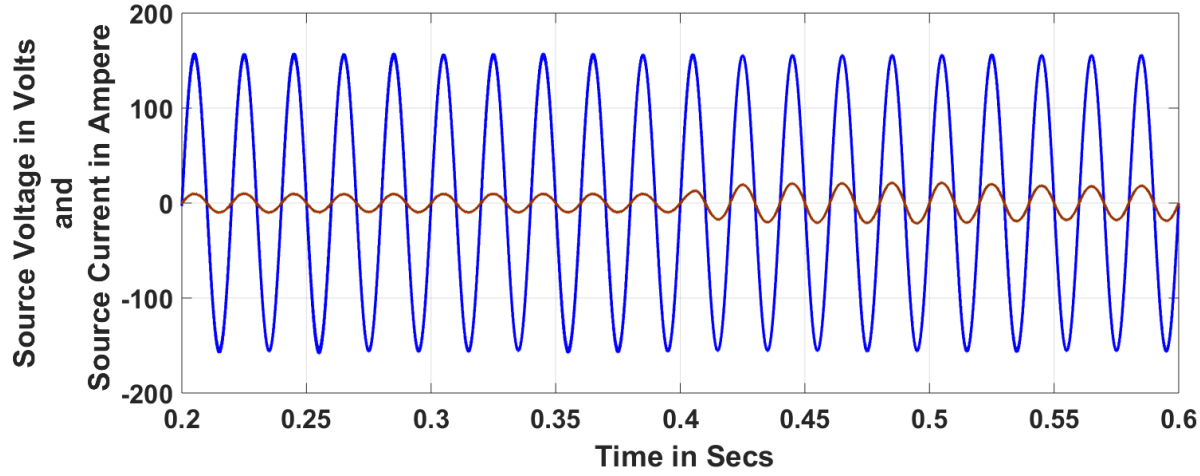


Fig 4.10 Source Voltage and Source current Waveforms with Non-Linear Load

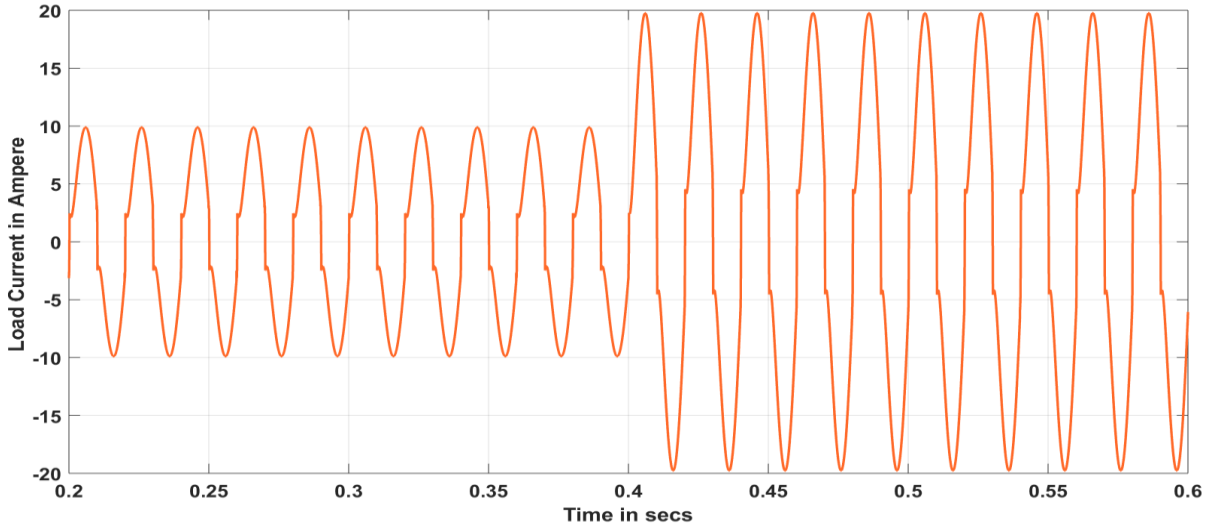


Fig 4.11 Load current waveform with Non-Linear Load

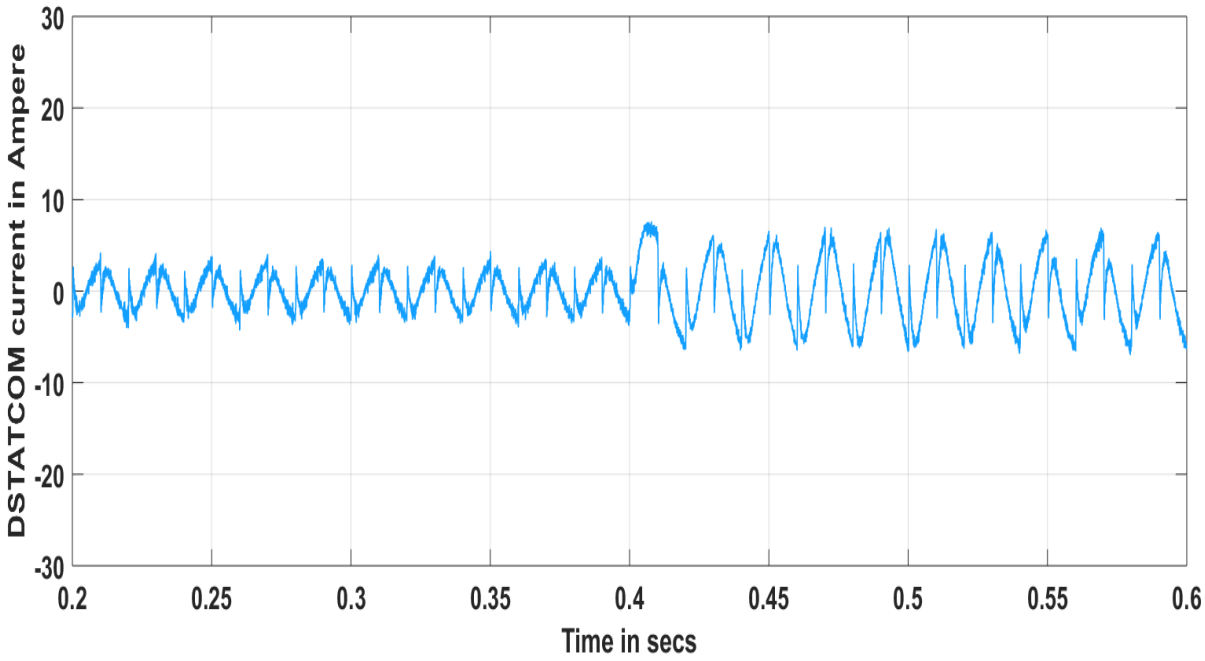


Fig 4.12 DSTATCOM current waveform with Non-Linear Load

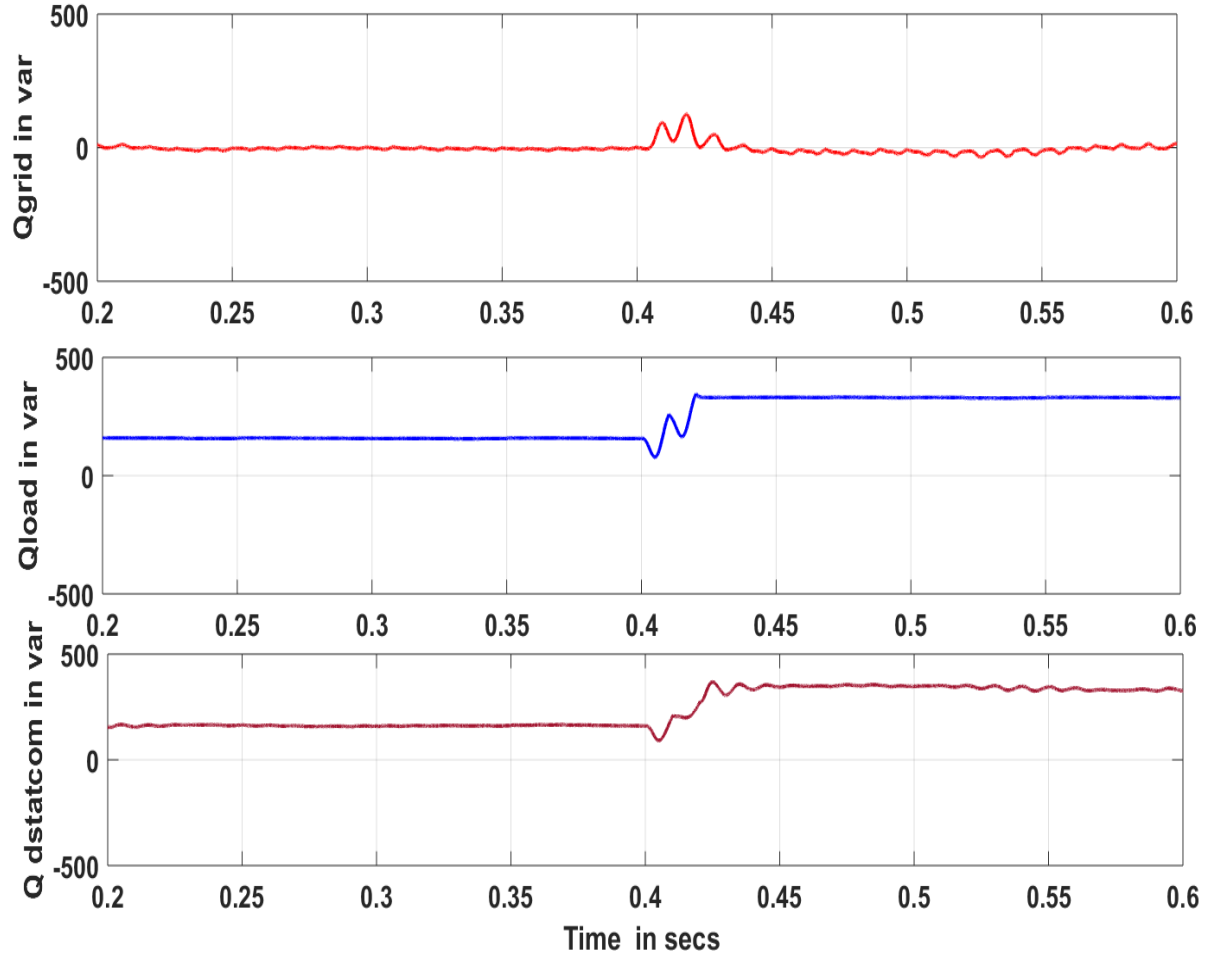


Fig.4.13 Reactive Power of Grid and DSTATCOM and Load in Non-Linear Load

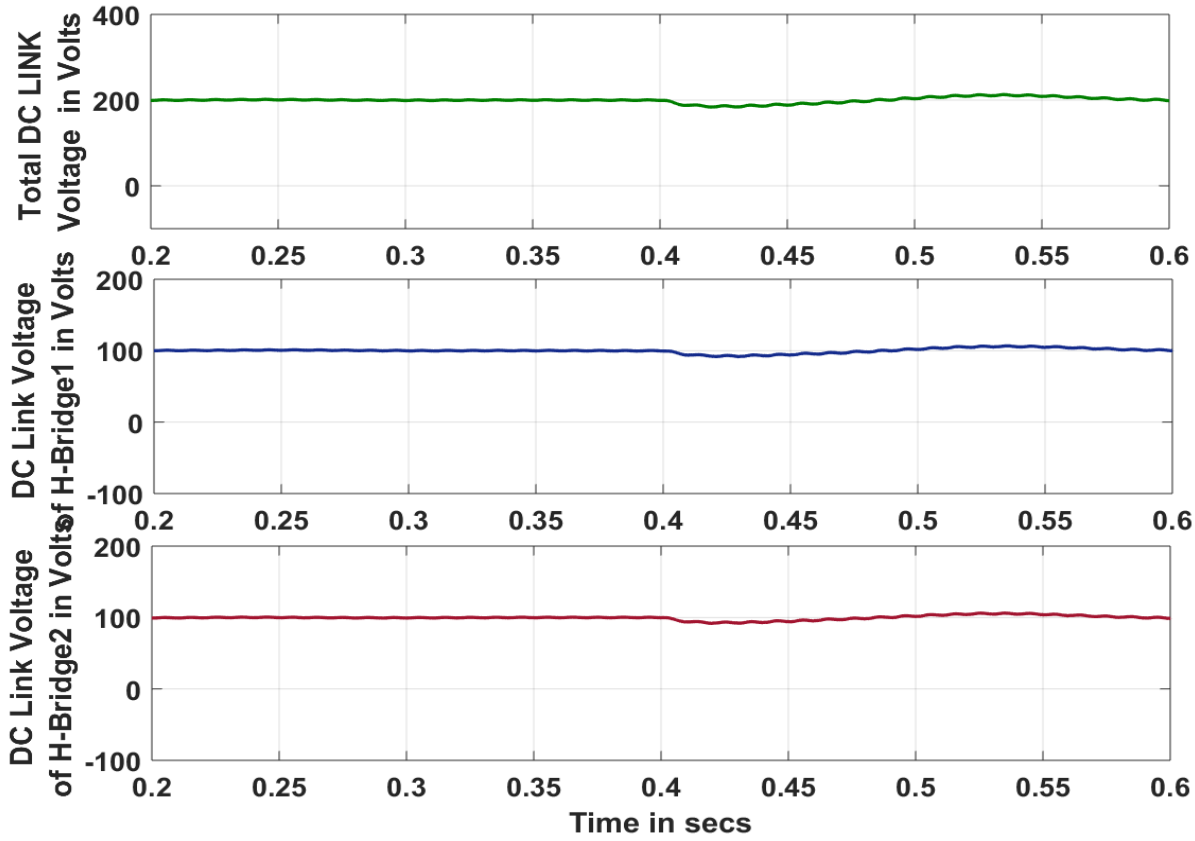


Fig 4.14. Total and Individual DC link voltage waveforms with Non-Linear Load

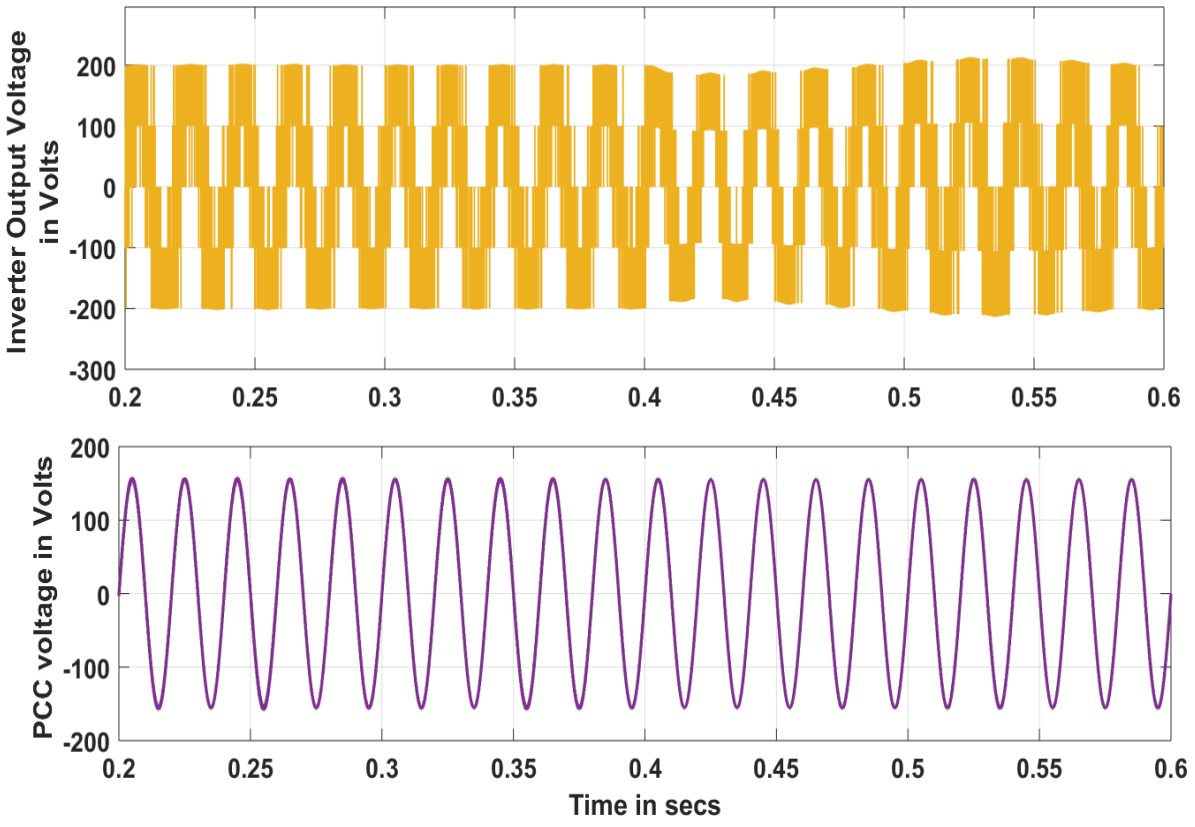


Fig 4.15. PCC and Multilevel inverter output voltage waveforms with Non-Linear Load

4.4.3 Fast Fourier Transform Analysis of Source Current under Various Load Conditions: With changes to the switching frequency (i.e. increases in this case) the source current is the other important system parameter affected, and under non- linear load conditions the source current THD decreases, as shown in Table 4.2. For the better application of the system, the frequency should therefore be high, while the frequency should remain in the optimal limit for multilevel operation in order to ensure that the interrupting losses do not exceed acceptable limits, as shown in Figure 4.16- Fig.4.20. Load current FFT analysis is shown in Fig.4.20

Table 4.2 Source Current THD under different switching Frequencies

S.no	Switching Frequency	Source Current (THD%)
1	1000	4.11
2	2000	3.01
3	3000	2.96
4	4000	2.92

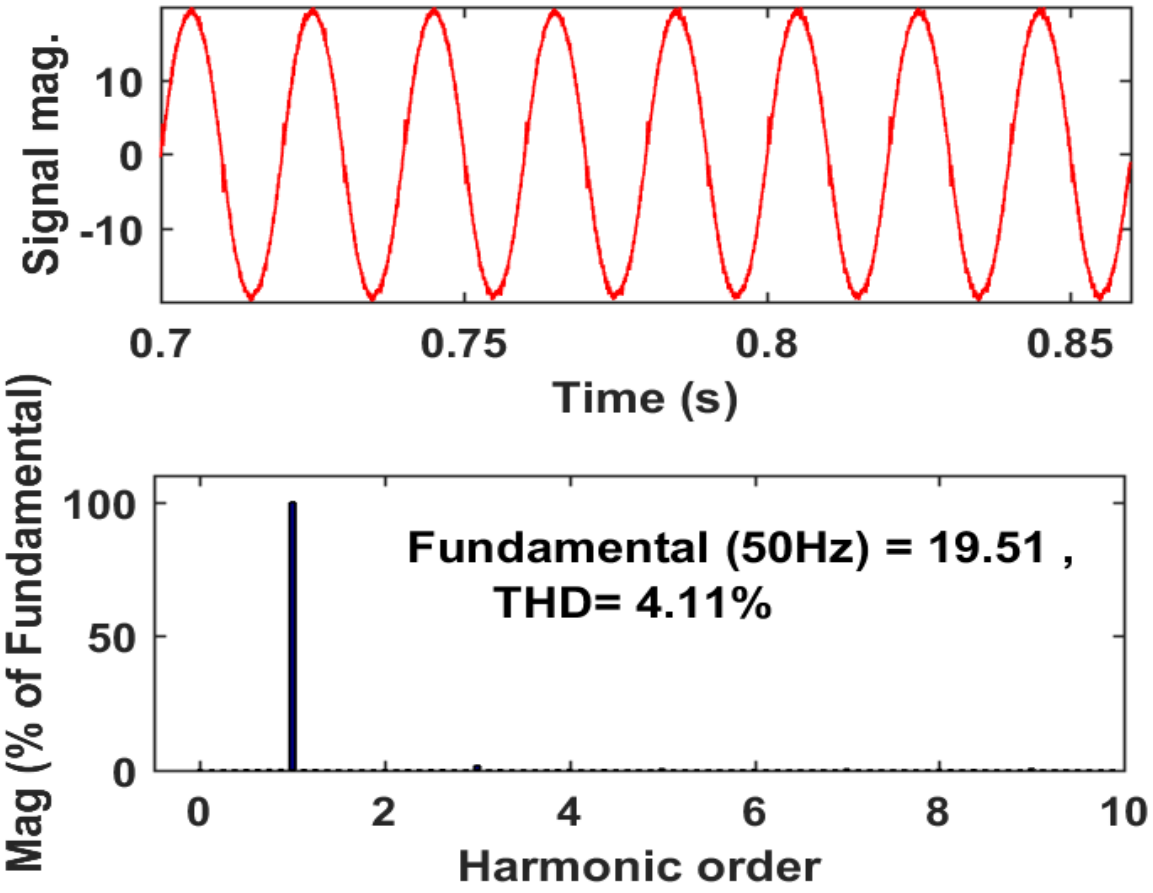


Fig 4.16 FFT analysis of Source current with switching frequency 1000Hz

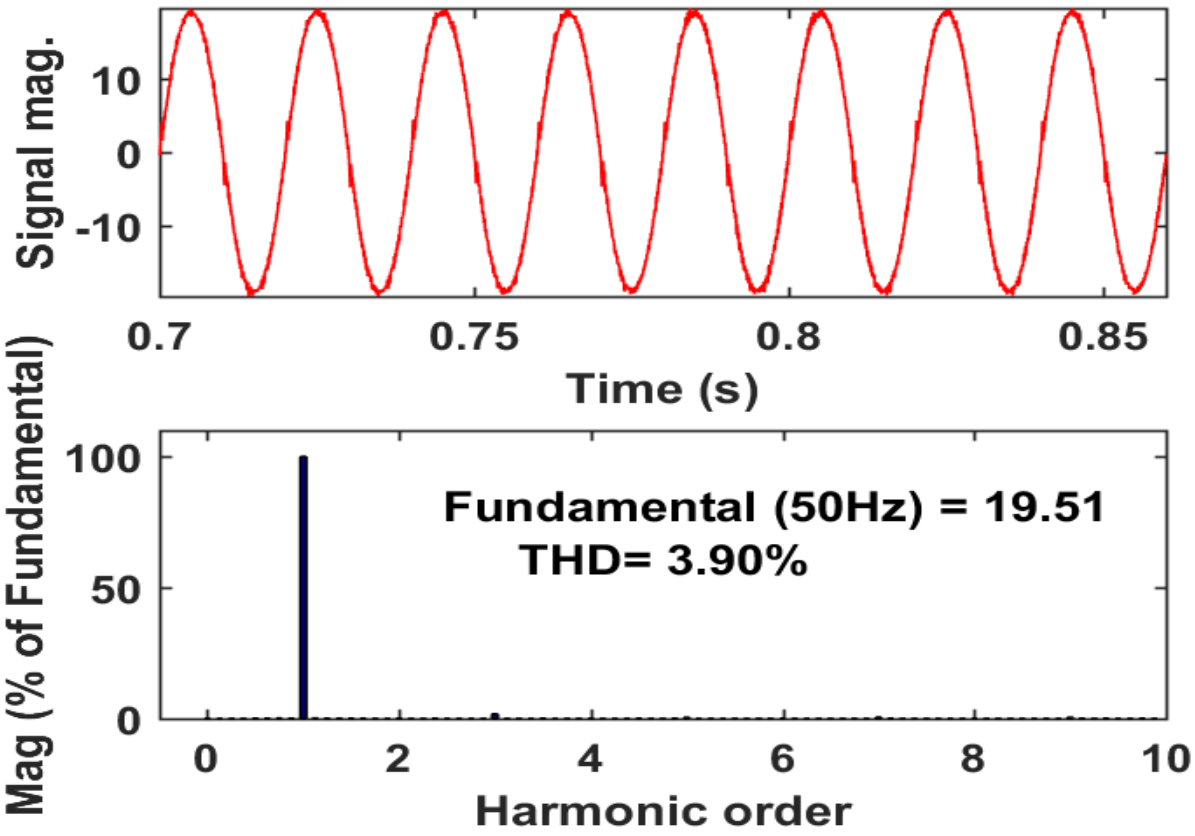


Fig 4.17 FFT analysis of Source current with switching frequency 2000Hz

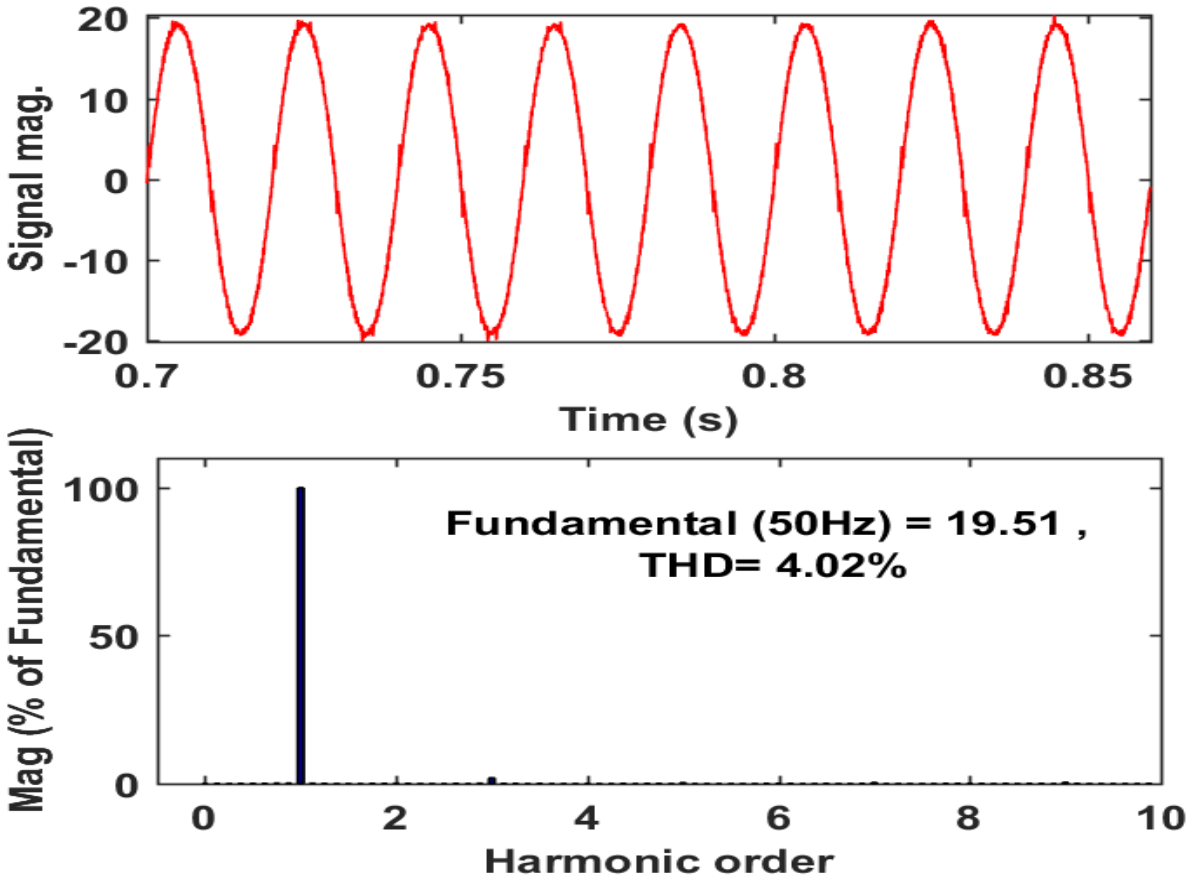


Fig 4.18 FFT analysis of Source current with switching frequency 3000Hz

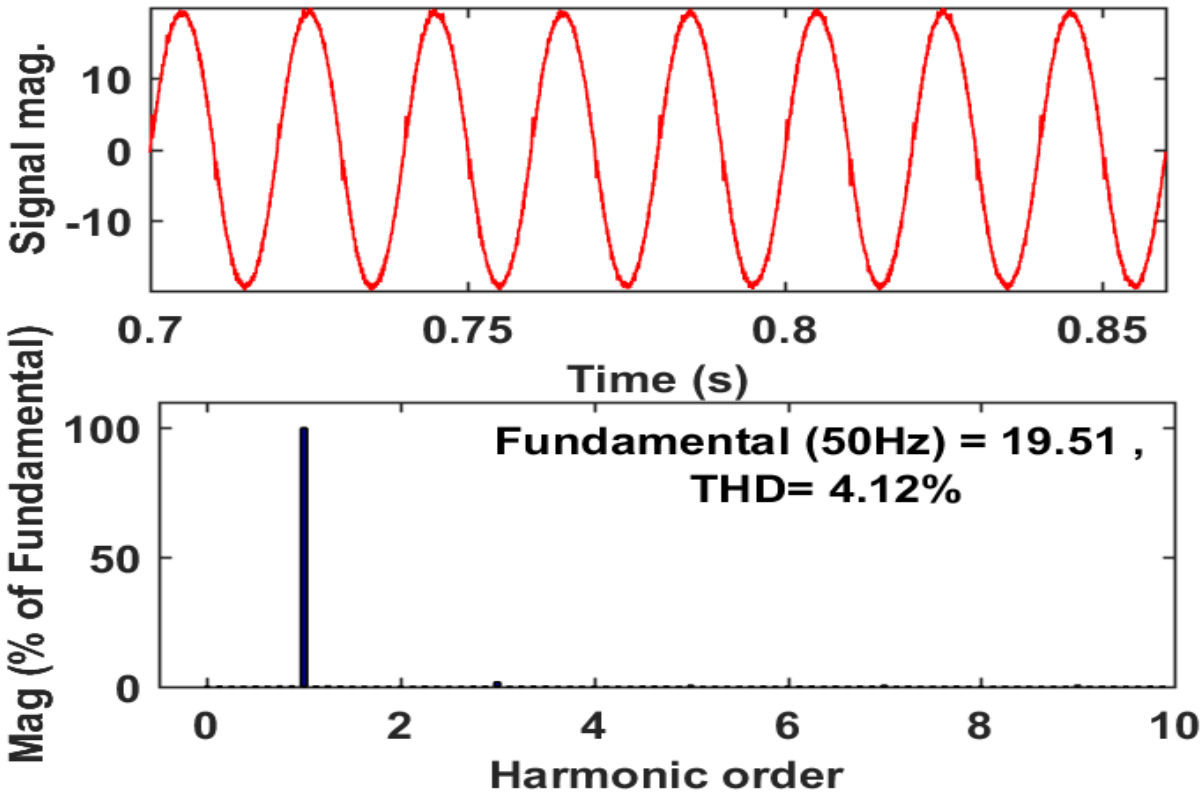


Fig 4.19 FFT analysis of Source current with switching frequency 4000Hz

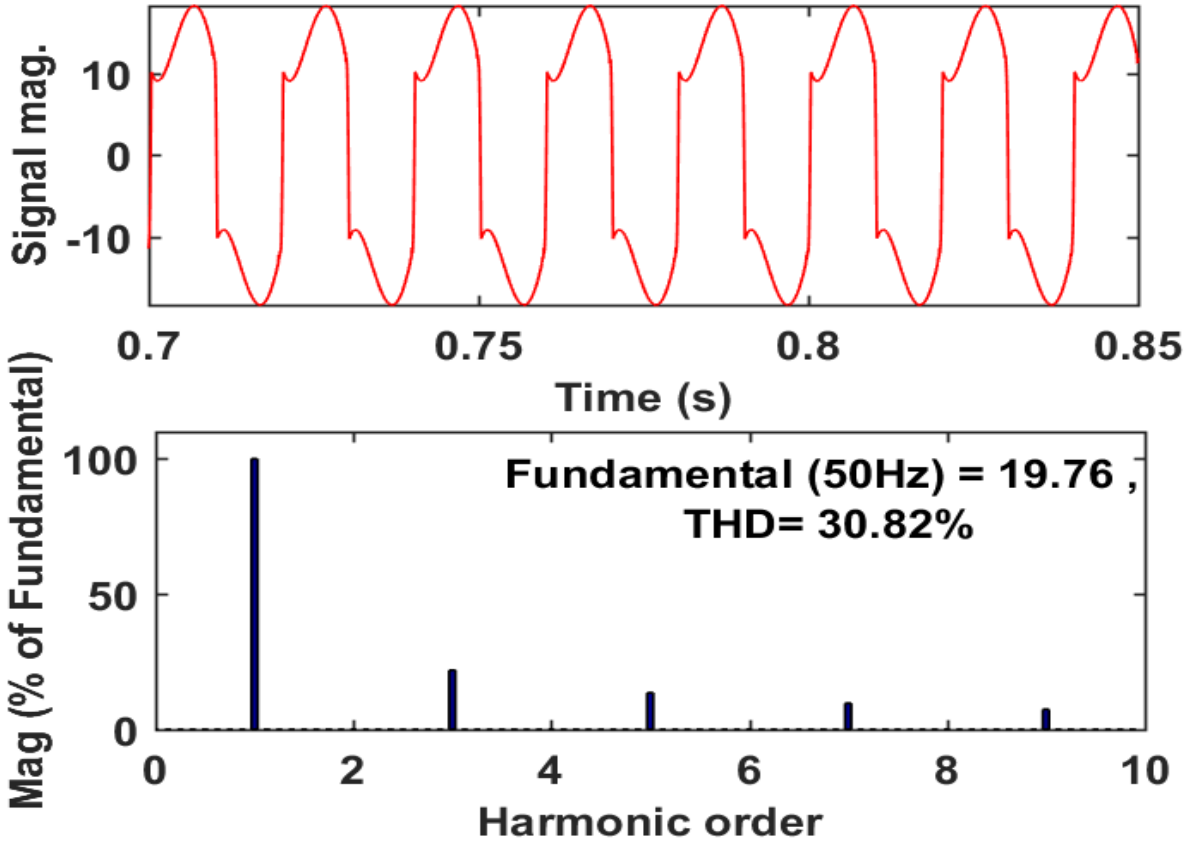


Fig 4.20 FFT analysis of Load current

The IEEE Standard 519/92 provides for an acceptable current THD of less than 5% (IEEE Recommended Practices and Harmonic Control Requirements for Electric Power Systems). The decrease in the distortion at source shows the effectiveness of components like the MLI, the L filter and the DC Link and the switching technology at various frequencies.

4.5 Conclusions:

Multilevel Inverter with two H bridges is simulated in Cascaded mode and operates as DSTATCOM. The Shunt compensator is controlled using SRF technique and tested with linear and non-linear loads. The results show that Q_{load} is met by Multilevel Inverter and grid current is in phase with supply voltage and sinusoidal, thereby improving power quality features.

Chapter 5

Implementation of PV-STATCOM using Five Level Converter

This chapter discuss the integration of grid tied PV using Five Level Multilevel Inverter. This chapter starts with PV system detailed modelling followed by MPPT Techniques. Thereafter Design of PV-STATCOM modelling have been discussed. Thereafter performance of PV with Multilevel Converter with various loads is presented.

5.1 Mathematical Model of PV:

PV systems connected to the grid are designed to work parallel to the grid. The inverter is the major part of a grid-associated PV system. It transforms direct power (DC) into AC power in line with grid voltage and power. Currently PWM voltage source (VSI) controlled inverters are used for grid interconnecting with PV to enhance system stabilization.

Photovoltaic arrays consist of series and parallel PV modules connected. Series and parallel connecting PV cells are available for each PV module. There are four elements that can be modelled on a PV cell. It comprises of a current source with series resistance to the diode and the shunt. As p-n junction form, PV cells are of non-linear property. It is helpful to develop a circuit equivalent, based on electrical components, whose behaviour is known, in order to understand electronic behaviour of PV cells. Figure 5.1 illustrates such an equivalent circuit. The I_{Ph} current source produced by the light represents a generation in the semiconductor of the charge carrier, which is caused by incident sunlight on the PV surface. The shunt diode is a recombination of these carriers with high forward voltage. The R_p shunt resistor enables high current trajectories through the semiconductor.

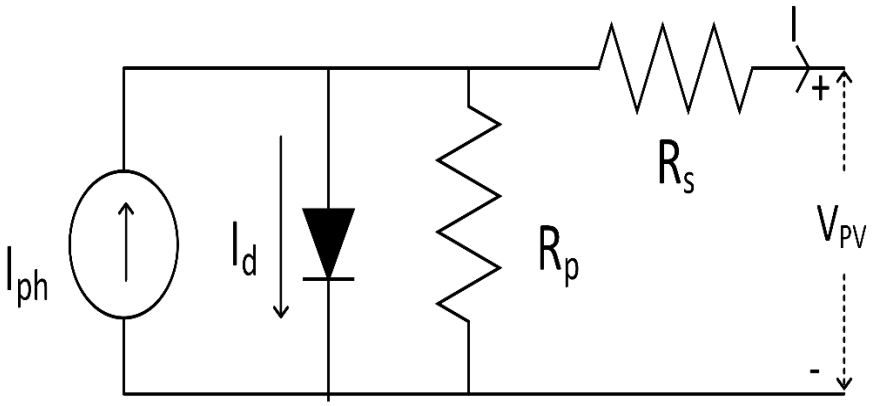


Fig. 5.1 PV cell model

The equivalent circuit of PV cell is shown in Fig. 1 The modelling design of PV module is described below [65]:

The output PV module current is given in Eq. (5.1.1)

$$I = N_p I_{ph} - N_p I_d - I_p \quad (5.1.1)$$

where I_{ph}= photo current in Amperes, I_d = diode current in Ampere, I_p = leakage current in Amperes in shunt resistance R_p.

The Photo current (I_{ph}) can be computed from Eq. (5.1.2)

$$I_{ph} = [I_s + K_s(T_e - 298)] \times I_r/1000 \quad (5.1.2)$$

where I_s = short circuit current in Amperes, K_s = short circuit current constant, T_e= operating temperature in kelvin, I_r = solar irradiation in W/m^2

The diode current (I_d) is computed from Eq. (5.1.3)

$$I_d = I_O \left[\exp\left(\frac{V_{oc}}{A.NV_T}\right) - 1\right] \quad (5.1.3)$$

where I_O = saturation current, V_{oc} = open circuit voltage in volt, A = ideality factor, N = Number of series connected solar cell, V_T = thermal voltage

The thermal voltage V_T is given in eq. (5.1.4)

$$V_T = \frac{kT_e}{q} \quad (5.1.4)$$

where k = Boltzmann's constant, q = charge of electron in coulombs

The saturation current (I_o) is given in eq. (5.1.5) below

$$I_O = I_{rs}\left(\frac{T_e}{T_r}\right)^3 \times exp\left[\frac{qE_g}{Ak}\left(\frac{1}{T_r} - \frac{1}{T_e}\right)\right] \quad (5.1.5)$$

where I_{rs} = reverse saturation current, T_r = nominal temperature in kelvin, E_g= band gap energy in eV

The reverse saturation current (I_{rs}) is given in eq. (5.1.6) below

$$I_{rs} = \frac{I_s}{\exp\left(\frac{qV_{oc}}{NkAT_e}\right) - 1} \quad (5.1.6)$$

The leakage current (Ip) is given in eq. (5.1.7) below

$$I_p = \frac{V \times \frac{N_p}{N_s} + I \times R_s}{R_p} \tag{5.1.7}$$

where N_p = number of parallel connected modules, N_s = number of series connected modules

The P-V characteristics and I-V characteristics of PV array is illustrated in Fig. 5.2 and Fig.5.3.

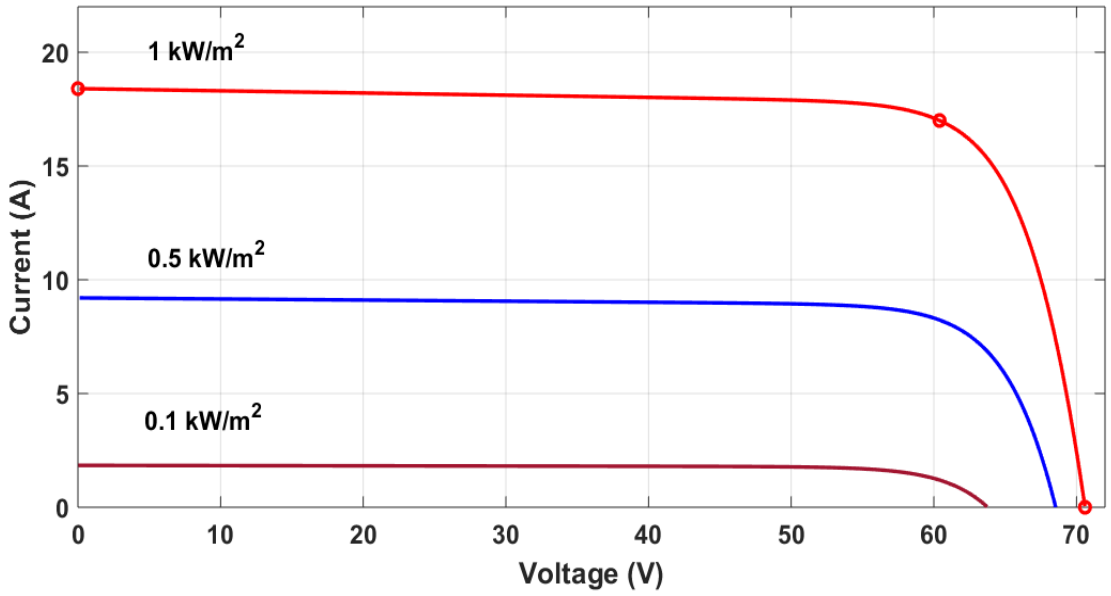


Fig. 5.2 I-V characteristics of PV Array

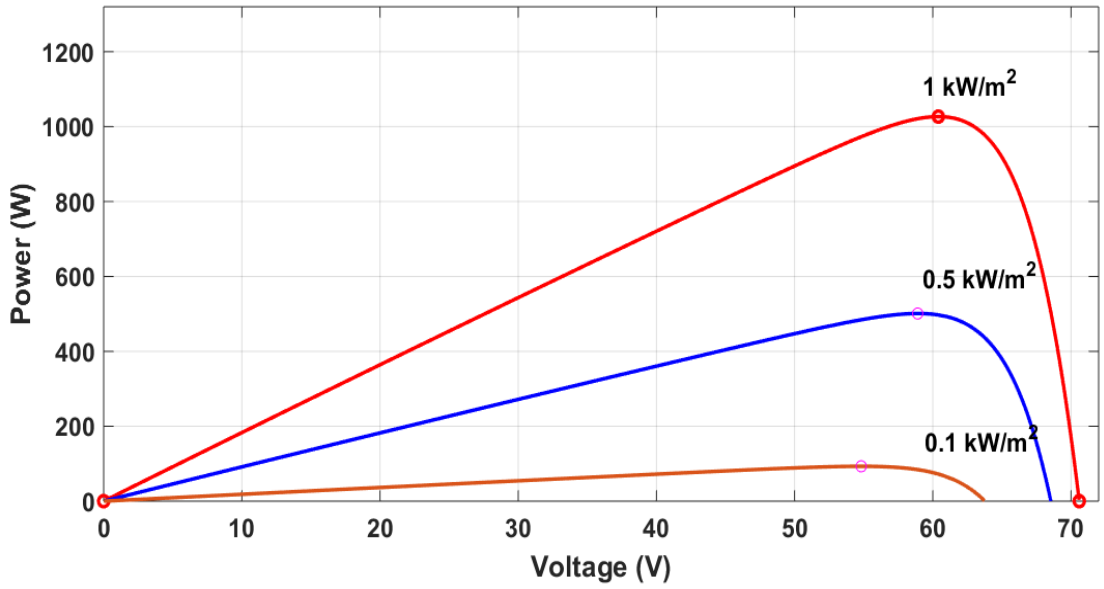


Fig. 5.3 P-V characteristics of PV Array

Table.5.1 PV Array Characteristics

Parameters	Value
V_{oc}	70.6 V
I_s	18.4 A
P_{max}	1000 W
N	80
N_s	2
N_p	2
R_{sh}	284.3372Ω
R_s	0.4193 Ω
V_{mp}	60.4V
I_{mp}	17 A

5.2 Maximum power point tracking (MPPT):

Changing environment conditions would influence the PV array's output power. The maximum power energy can always be ensured under the respective climate situation by placing the MPPT on the PV system. In the research publications, there are several MPPT algorithms proposed. The P&O and Incremental Conductance Methods (P&O) are described in this chapter. The feature power curve of a PV grid is shown in Fig.5.4. For various environmental circumstances this characteristic curve would alter. The key concept of MPPT is then to modify the input voltage and flow for V_{MPP} and I_{MPP} automatically in order to achieve optimal production by the PV set. There are various MPPT algorithms for PV schemes created. These include the discussion and implementation of P & O and incremental conductance algorithms. systems. Among them P&O and incremental conductance algorithms are discussed and implemented.

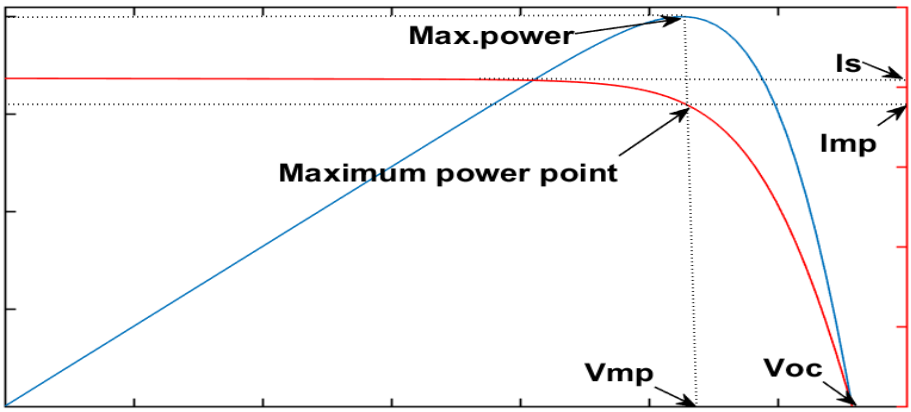


Fig 5.4 Characteristic curve of PV Array

5.2.1 P&O algorithm [7]-[11]:

The working voltage of the PV panel is the quantity to be improved and/or reduced in the MPPT in perturbation and observation technique. Figure5.4 shows that increasing the operating voltage in the PV array increases the power output and decreases the power output if the operating point is on the left side of the MPP. When the point is on the right of MPP, however, the increasing operating voltage of the PV array would reduce power output and increase the output power by reducing the operating voltage of the PV array. The interference would therefore be kept identical if the output power was increased while the perturbation direction was changed if the output power was reduced. In Fig.5.5 is shown the algorithm.

When MPP is reached by the working voltage, it swings around the MPP. The choice of the perturbation sizes is just the difference between this oscillation and the MPPT response time. The oscillation of around MPP would be extremely small, but MPPT would have a very long response time. There are already some alternatives to this issue. In literature, for instance, the perturbation size can be adjusted which ensure large perturbation far from MPP and comparatively tiny disturbance magnitude around MPP.

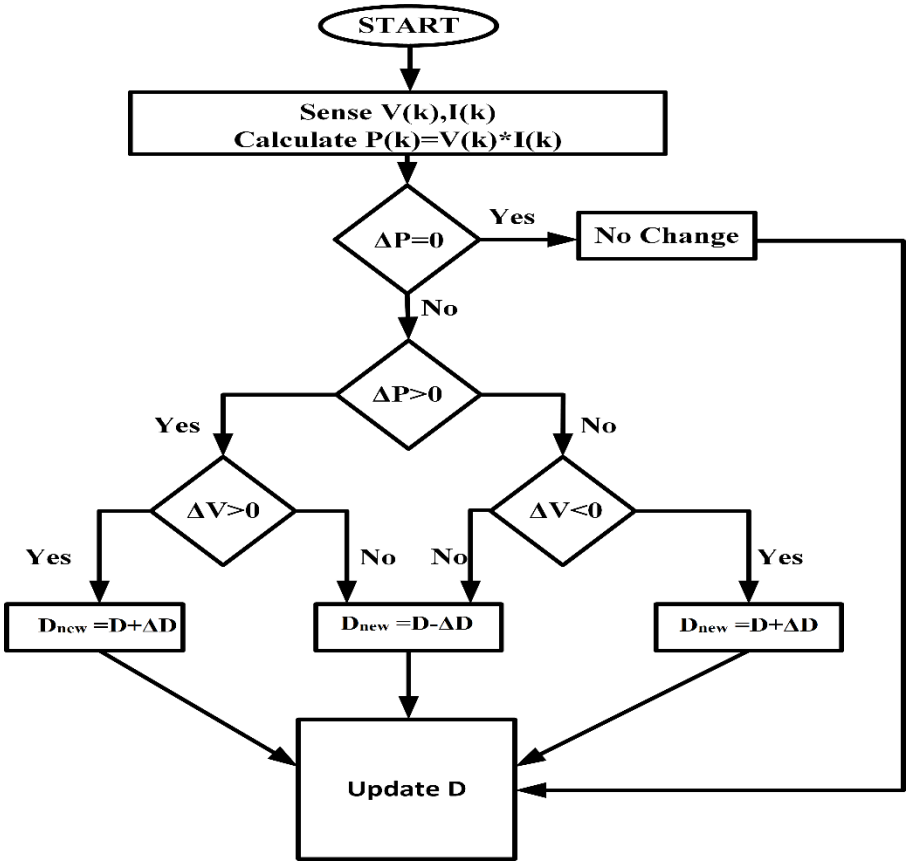


Fig 5.5 flow chart of P&O algorithm

5.2.2 Incremental conductance algorithm [7]-[11]:

In the power curve as shown in Figure 5.3, the curve slope defined as dP/dV at various operating points can be seen to differ. If the point of operation is at the left side of MPP, dP/dV>0, if it is at the right side, dP/dV< 0, if the point is at MPP, dP/dV=0. The incremental algorithm of conduct shown in Fig 5.6 is based upon the above fact. The term dP/dV is provided by

$$\frac{dP}{dV} = \frac{d(IV)}{dV} = I + V\frac{dI}{dV} = I + V.\frac{\Delta I}{\Delta V} \tag{5.2.1}$$

I / V is given as the instantaneous conductance and $\Delta I/\Delta V$ is defined as incremental conductance. The operation point of the photovoltaic array can then be achieved by combining the instantaneous with the incremental conductance shown in the next equation.

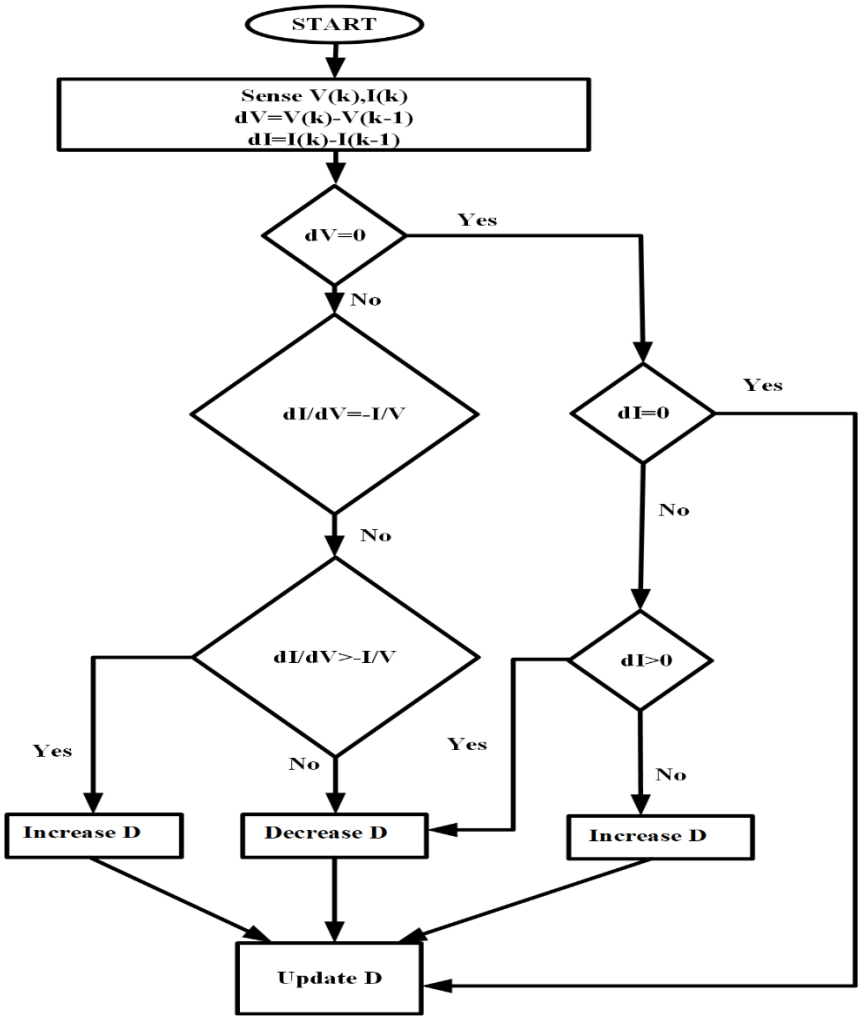


Fig 5.6 Incremental Conductance Algorithm

$$\begin{cases} \Delta I/\Delta V = -I/V\,, at\ MPP \\ \Delta I/\Delta V > -I/V\,, Left\ of\ MPP \\ \Delta I/\Delta V < -I/V\,, Right\ of\ MPP \end{cases} \quad (5.2.2)$$

The operating voltage can be increased or reduced to close to V_{MPP} when the operating point has been achieved. Here, V_{ref} is the voltage at the maximum power point that is the same as VMPP. V_{ref} will retain this value if the MPP is achieved unless a change to the ΔI occurs due to weather. Then the algorithm increases or decreases V_{ref} for the fresh MPP to be tracked. The incremental conductance method is used in this thesis for maximum power point tracking as the output voltage better follows changes in weather and the oscillation around MPP is smaller than the P&O.

5.3 System description:

Fig. 5.7 shows a proposed photovoltaic system comprising 2-Kw solar photovoltaic panel grid-tied five-level cascaded H-Bridge Multilevel Inverter. Isolated 1 kW PV boards with separated DC-DC connected to two H-bridges using an IC MPPT scheme. The PV array is developed according to the procedure in [65]. To incorporate the scheme into the grid, interface inductors are used. Table 5.1 shows the parameters of the proposed PV.

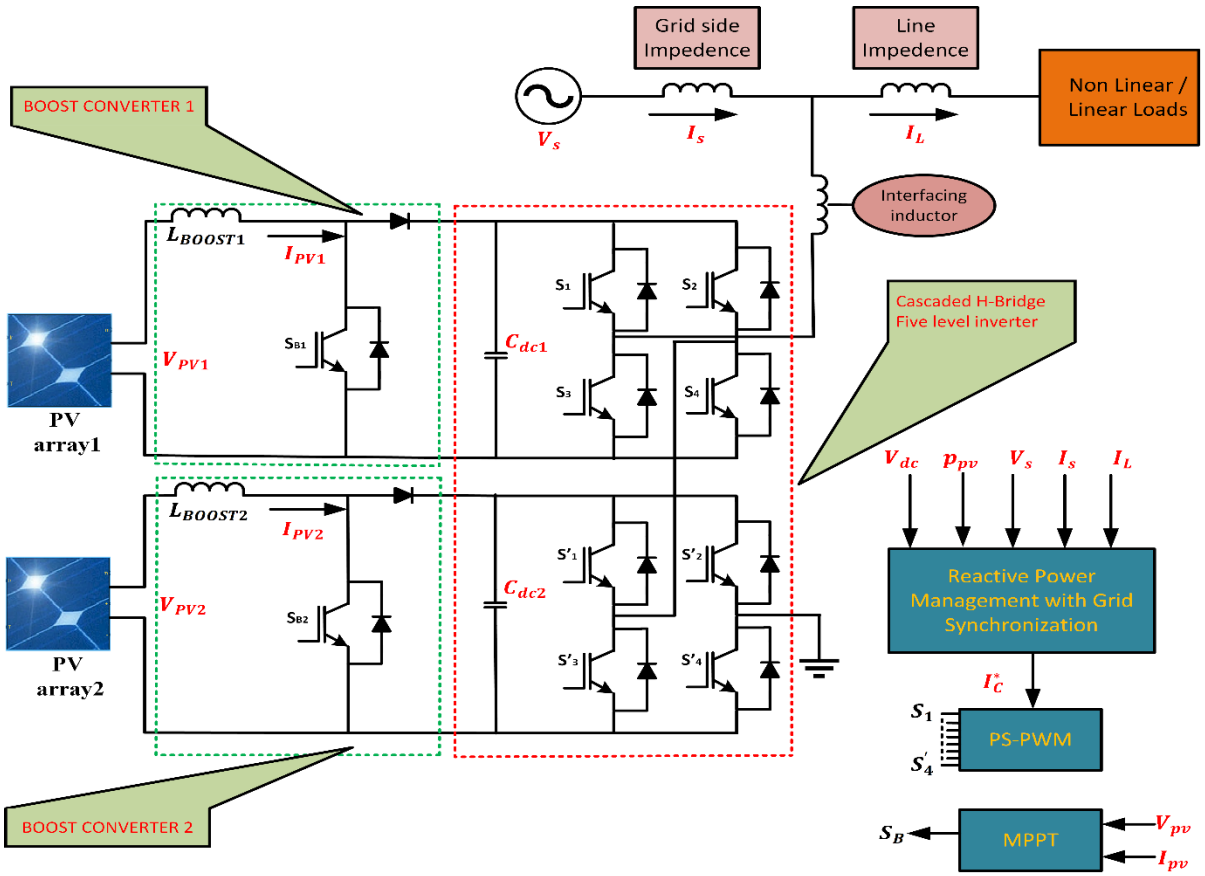


Fig 5.7 PV-STATCOM

5.3.1 Principle of operation PV-STATCOM:

The efficient utilization of the PV-STATCOM with a great number of grid interfaces is generally low because it only works during sunlight. They can be operated in two modes to increase the use of PV-STATCOM, namely

A. Active power mode along with Reactive power compensation mode (PV-STATCOM operation), called as mode-1
B. Reactive power compensation mode (STATCOM operation) called as mode-2

A. Active power mode along with Reactive power compensation mode:

This mode is applicable every day when the intelligent inverter exchanges reactive power with the grid using the remaining inverter capacity after real power. In this method, real power generation takes priority. Both active and reactive power are transmitted via VSC in this mode-1. Grid here requires reactive power, that is to say grid current lags grid voltage as shown in Fig.5.8.

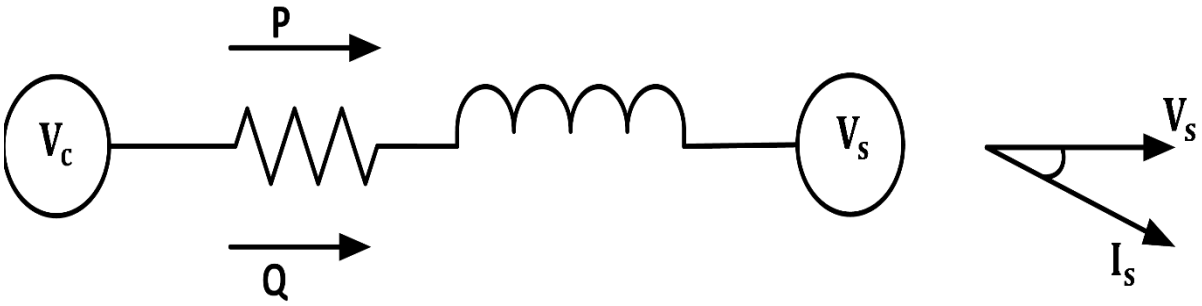


Fig.5.8 Single line diagram of the SPV-STATCOM in mode-1

B. Reactive power compensation mode:

This mode applies at night, when the intelligent inverter switches reactive power from the grid using the inverter capacity. In this method, real power generation is null. Only reactive power is transferred in this Mode-2 with VSC. Grid requires reactive capacity, meaning that the grid current lags at grid voltage shown in fig.5.9.

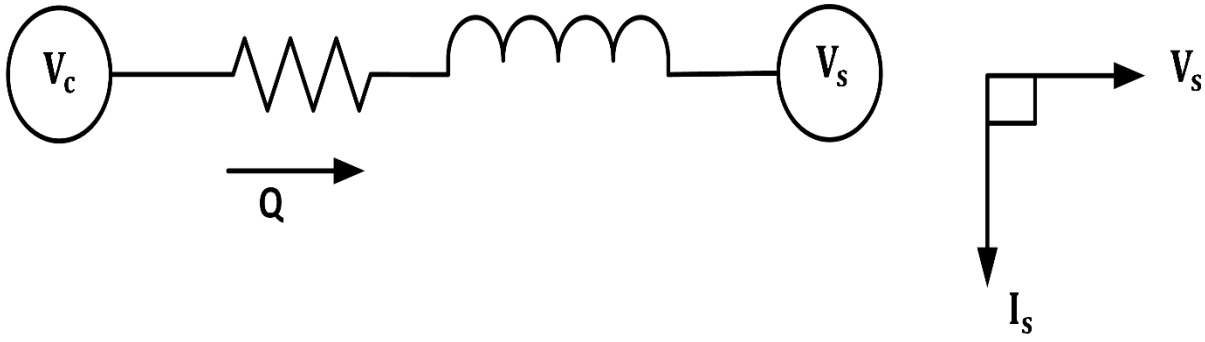


Fig.5.9 Single line diagram of the SPV-STATCOM in mode-2

5.3.2 Controller Design

Figs. 5.10 and 5.11 demonstrate current controller and the unit template and DC voltage controller used for the PV-STATCOM 5-level MLI. Specific MPPTs are used for boosting converters to get separate DC links.

DC-DC boost converter's rated capacity is 1KW shown in the fig.5.7 and the switching frequency is 20 kHz. A DC component and switching ripple are present in the current passage through the inductor $L_{boost.s}$ The inductor size L_{boost} can be measured using eq.5.3.1 to limit the

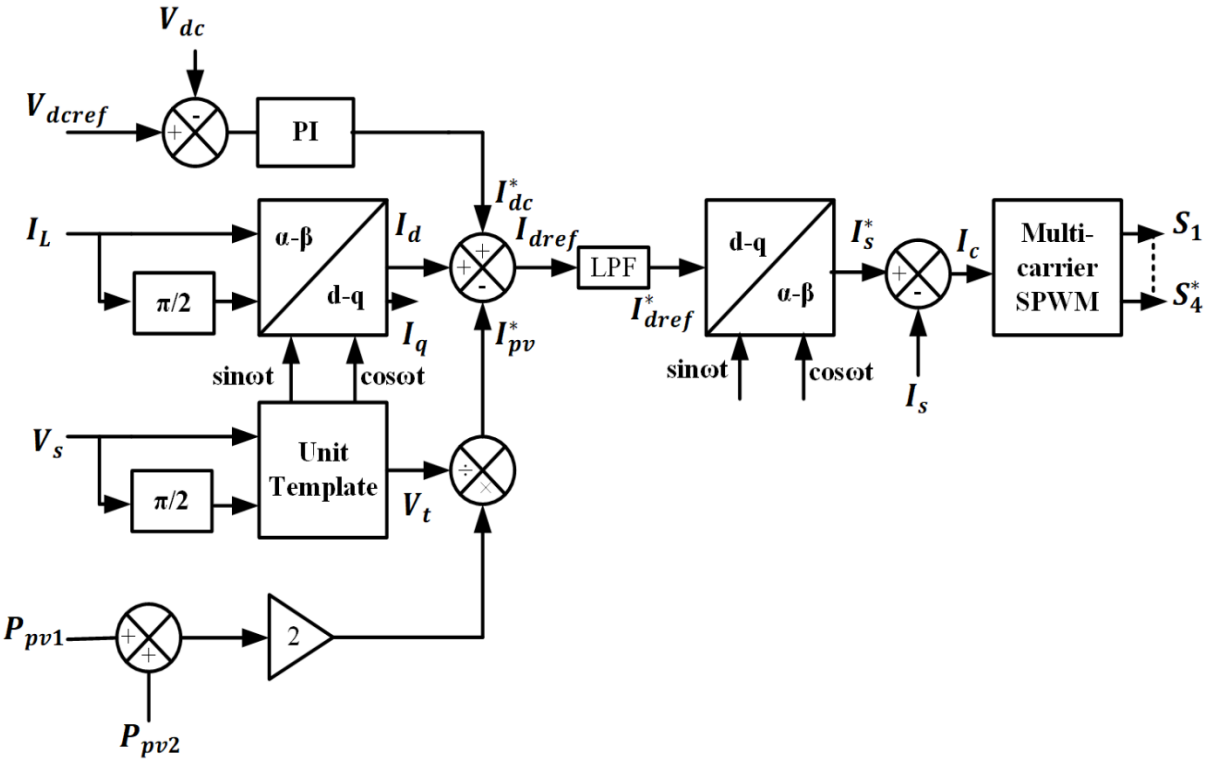


Fig 5.10 Controller design for PV-STATCOM

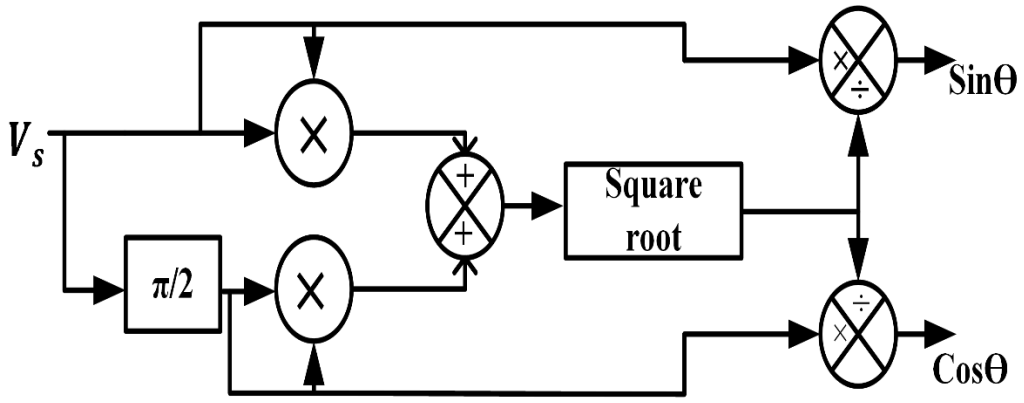


Fig 5.11 Unit Template

current ripple Δi_l associated with the switching frequency of the current owing through the inductor. V_{pv} is the voltage throughout the PV panel in (5.3.1).

$$\text{Inductor } (L_{boost}) = \frac{V_{pv} \times D \times T}{\Delta i_l} \quad (5.3.1)$$

where D is Duty cycle and T is Switching time period

When the PV Array is near the MPP, V_{pv} is near 60 V. Therefore, it can be computed that the L_{boost} inductor operates at its rated capacity as 5 mH to limit i_l to 5 percent of the D.C. current through the L_{boost} inductor. The converter DC-DC Boost can separate the PV set from the dynamics of the AC-side. The C_{pv} capacitor in the PV array output has been selected for the 2.5 times the C_{dc} capacitor for the grid connected PV system. With the C_{pv} value you can reduce to 10% the ripple of 100 Hz voltage that appeared on the terminals of a PV array, when the C_{pv} is operated at the rated capacity. The ripple voltage is 100Hz. The large C_{pv} time-constant efficiently disconnects the PV array from the grid-connected PV dynamics. C_{pv} also minimizes the ripple current of the switching frequency taken from the PV array.

Fig. 5.10 showing DC bus voltage reference and a sum of sensed DC bus voltage is compared and V_e error is passed through a PI control (Proportional Integrator) which indicates the active loss current component (I_{dc}^*) in the reactive control system and is evaluated as the active losses in the DC link capacitor, as well as the loss component of dielectric in the DC Link capacitor. I_{dc}^* is evaluated as

$$I_{dc}^*(n) = I_{dc}^*(n-1) + K_p\{V_e(n) - V_e(n-1)\} + K_i V_e(n) \quad (5.3.2)$$

where $V_e = V_{ref} - \sum_{n=1}^{2} V_{dcn}$ and K_p and K_i are proportional gain and integral gain constants.

The feed-forward term equation in 5.3.3 gives the photovoltaic current of PV array (I_{pv}^*) The use of feed-forward term provides a fast-dynamic response and reduces the stress on PI controller.

$$I_{pv}^* = 2\sum_{n=1}^{2} P_{pvi}/3V_d \quad (5.3.3)$$

Thus the reference direct axis current I_{dref} consists of two components I_{dc}^* , I_{pv}^* is required to meet active loss component and I_{pv} gives the photovoltaic current of PV array. Thus, I_{dref} is expressed as

$$I_{dref} = I_{dc}^* - I_{pv}^* \quad (5.3.4)$$

5.4 Results:

The proposed PV-STATCOM is modelled and its performance is simulated in MATLAB 2018b. It consists of design and selection of PV array, IC MPPT, Unit template and current controller and Five Level Cascaded H-bridge Multilevel Inverter tied to grid. Steady state Analysis is done for both mode of operations. The Photovoltaic array voltage and current and power is demonstrated in Fig.5.12. The DC-DC Boost converter output 100volts is maintained constant is shown in Fig.5.13. The source voltage and current and load current is demonstrated in Fig.5.14. to show that source current is sinusoidal. For the PV-STATCOM performance analysis, P_{pv1}, P_{pv2}, P_{grid}, Q_{grid}, P_{load}, Q_{load} is shown in Fig.5.16 for a mode-2 up to 0.4 sec and mode-1 is at 0.4 secs, respectively. The total DC voltage link is maintained constant voltage at 200V and individual H-bridge voltage is maintained at 100V as shown in Fig.5.15. Multilevel Inverter output and PCC voltage are as shown in Fig.5.17.

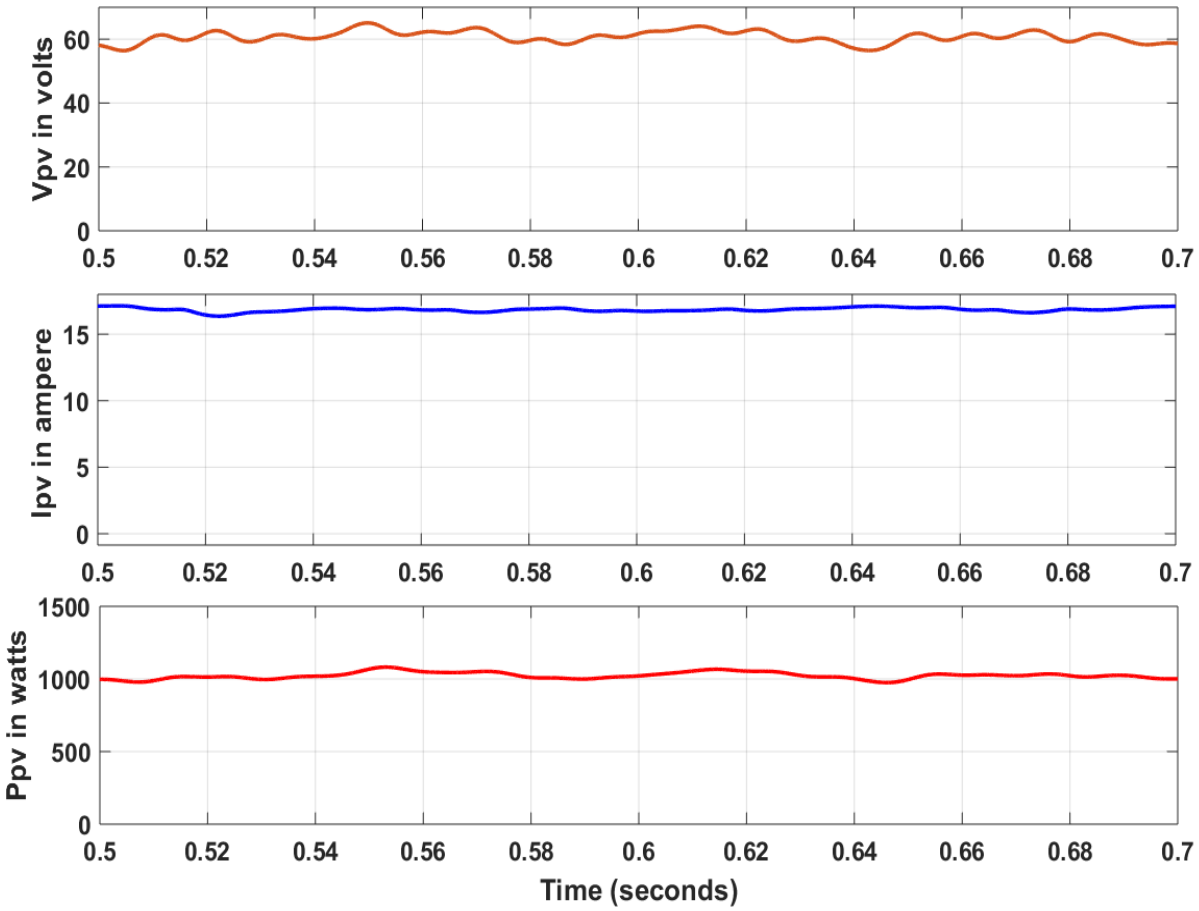


Fig 5.12 Voltage and Current and Power of PV Array

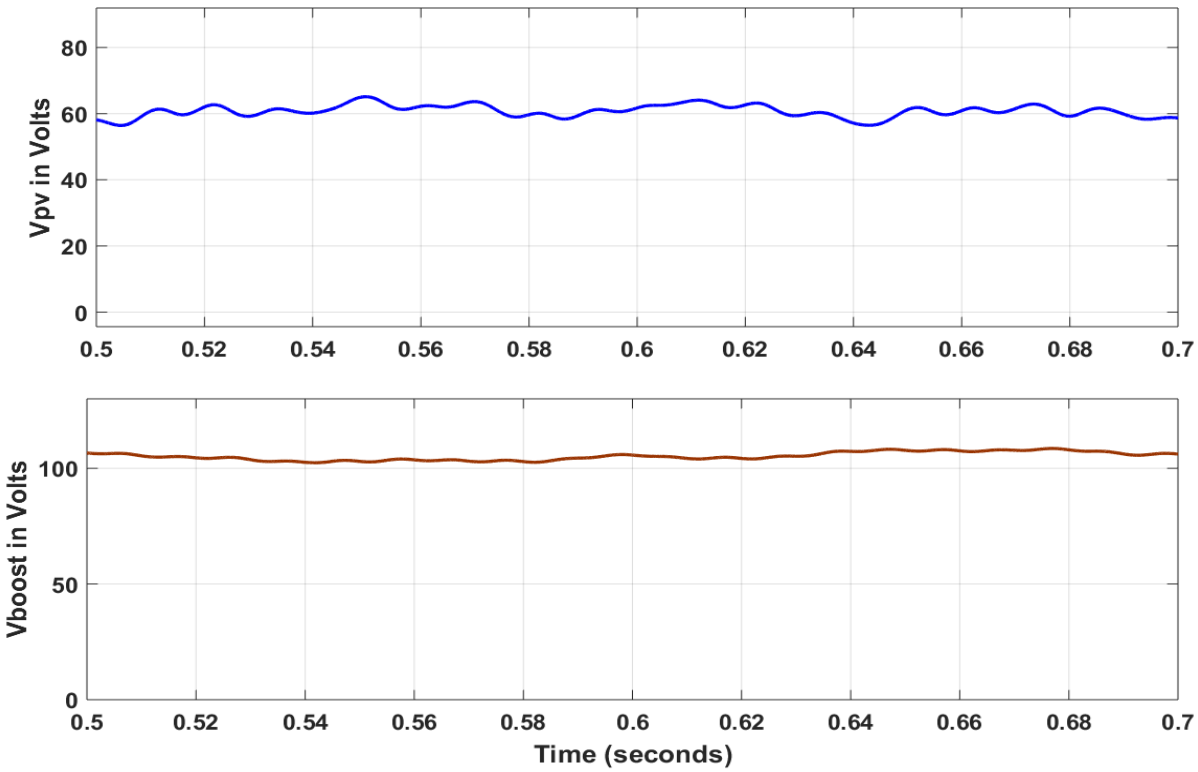


Fig.5.13 PV Voltage and voltage at end of DC-DC Boost converter

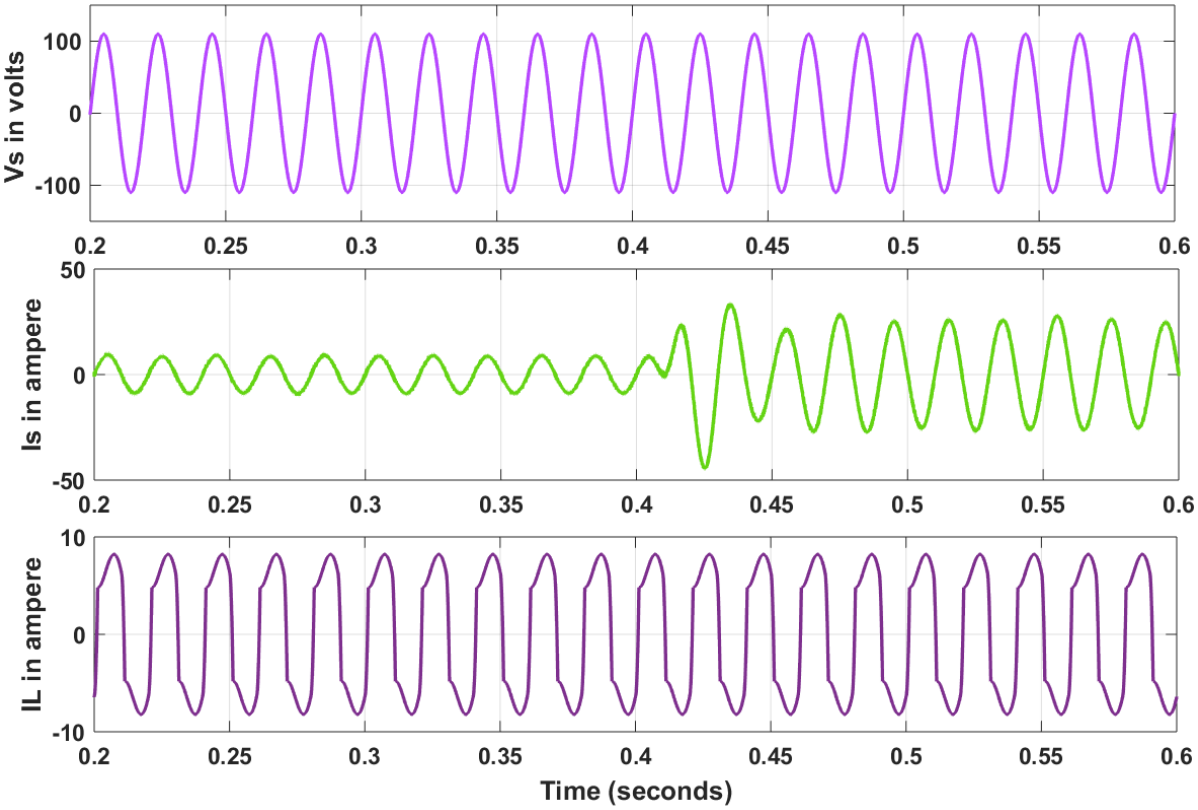


Fig.5.14 Source Voltage and Source current and Load current of PV-STATCOM

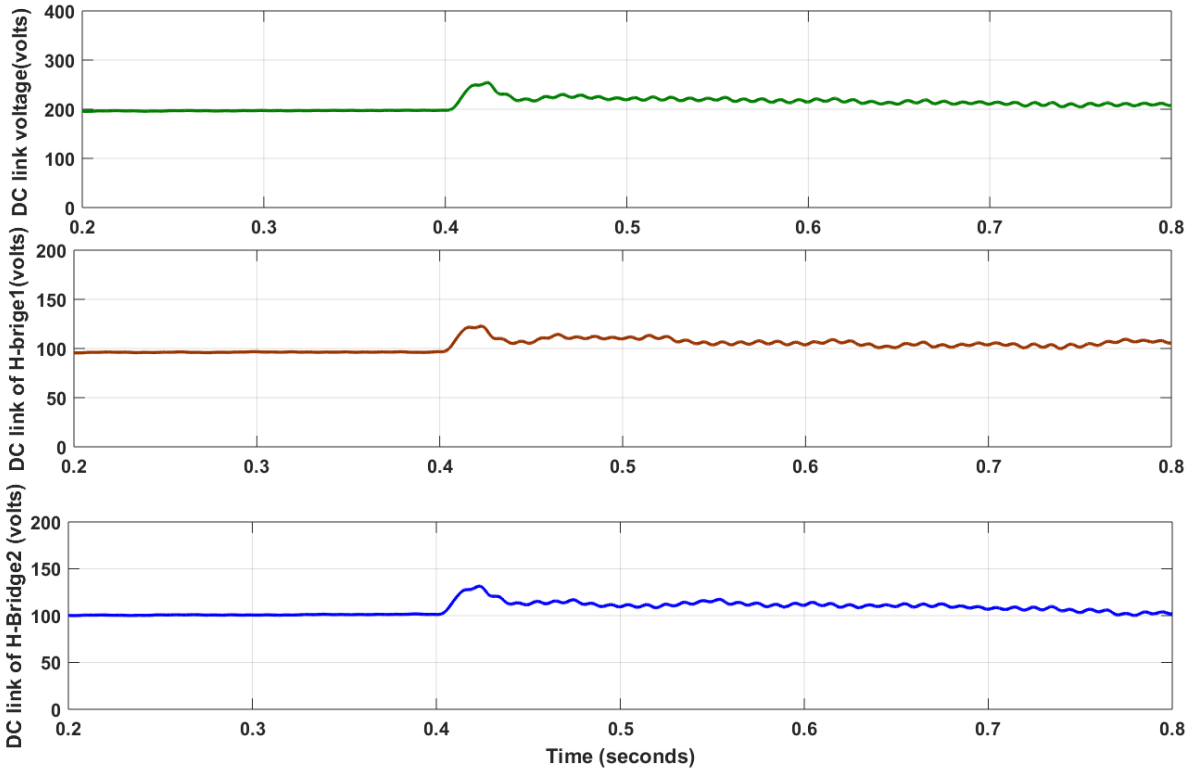


Fig.5.15 DC-Link Voltages of the Each H-Bridge and Total DC-Link Voltage

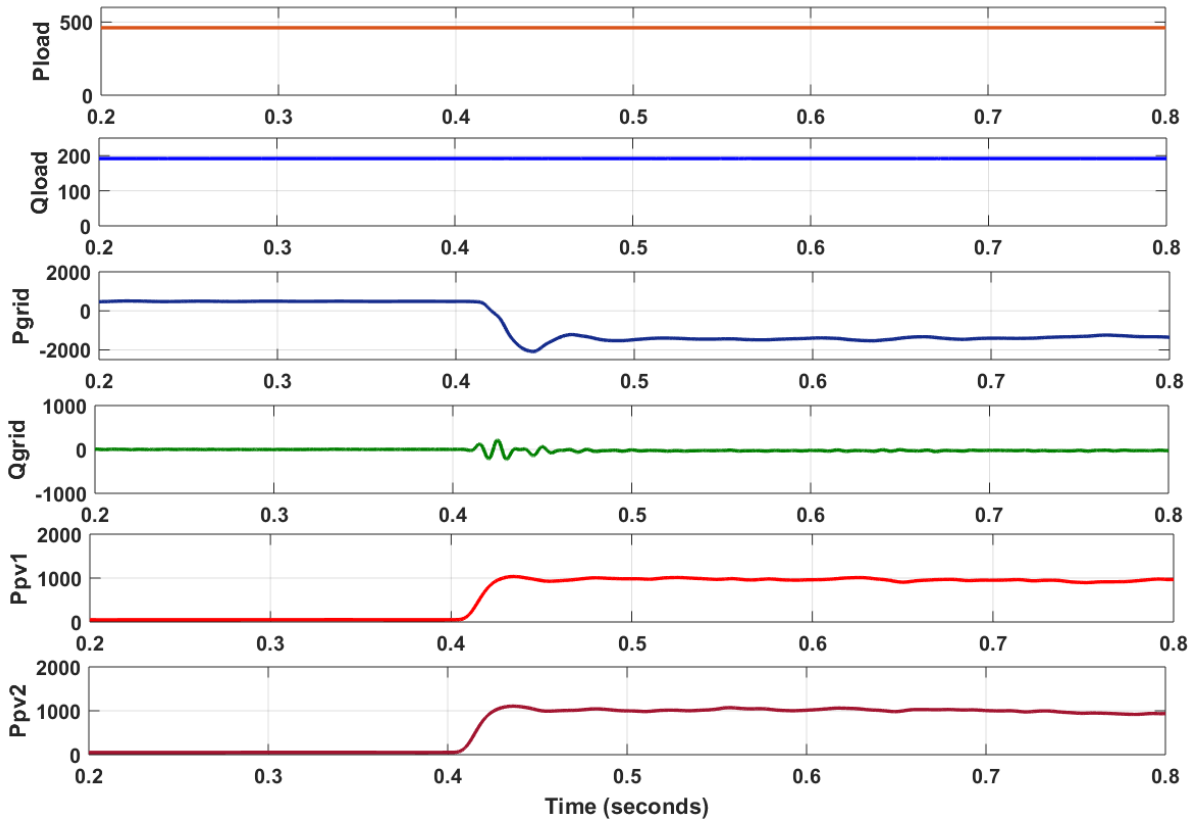


Fig.5.16 Plots for Powers of system

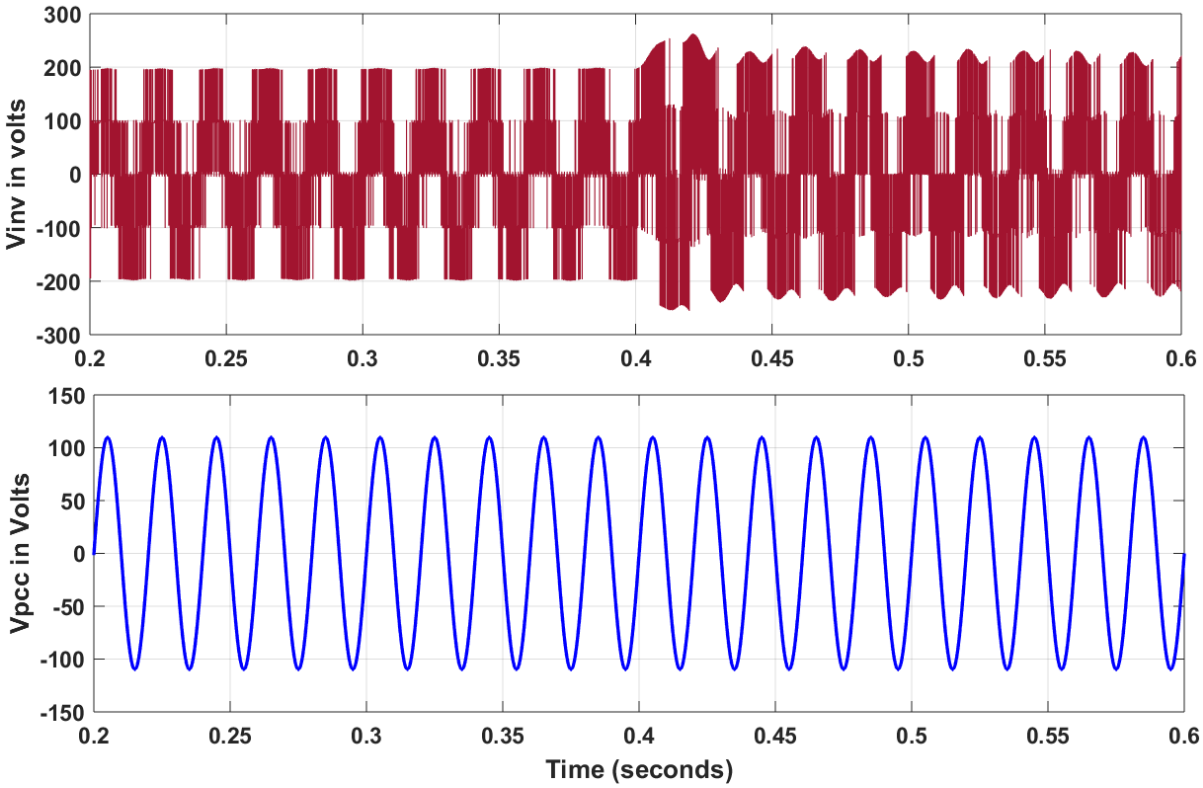


Fig.5.17 Multilevel Inverter output voltage and PCC Voltage of PV-STATCOM

5.5 Conclusion:

PV Array with Five Level Cascaded H- Bridge Multilevel inverter is operated as PV-STATCOM. PV-STATCOM supplies required reactive power to the load and active power to grid during day time as per its capacity. During night time, it acts as only DSTATCOM and supplies reactive power to load. The PV-STATCOM has been tested under different load conditions and the results show effective working of multilevel inverter during the entire day.

Chapter 6

HARDWARE IMPLEMENTATION

6.1 Introduction:

This chapter discusses the hardware implementation of Five Level cascaded H-Bridge Multilevel Inverter in open loop condition. All the H- Bridges, Gate logic circuits have been designed in laboratory. The pulse generation and the output voltage waveform are depicted. The whole Hardware system consisting of Cascaded H- Bridge Multilevel inverter, Gate logics circuits is given in Fig.6.1

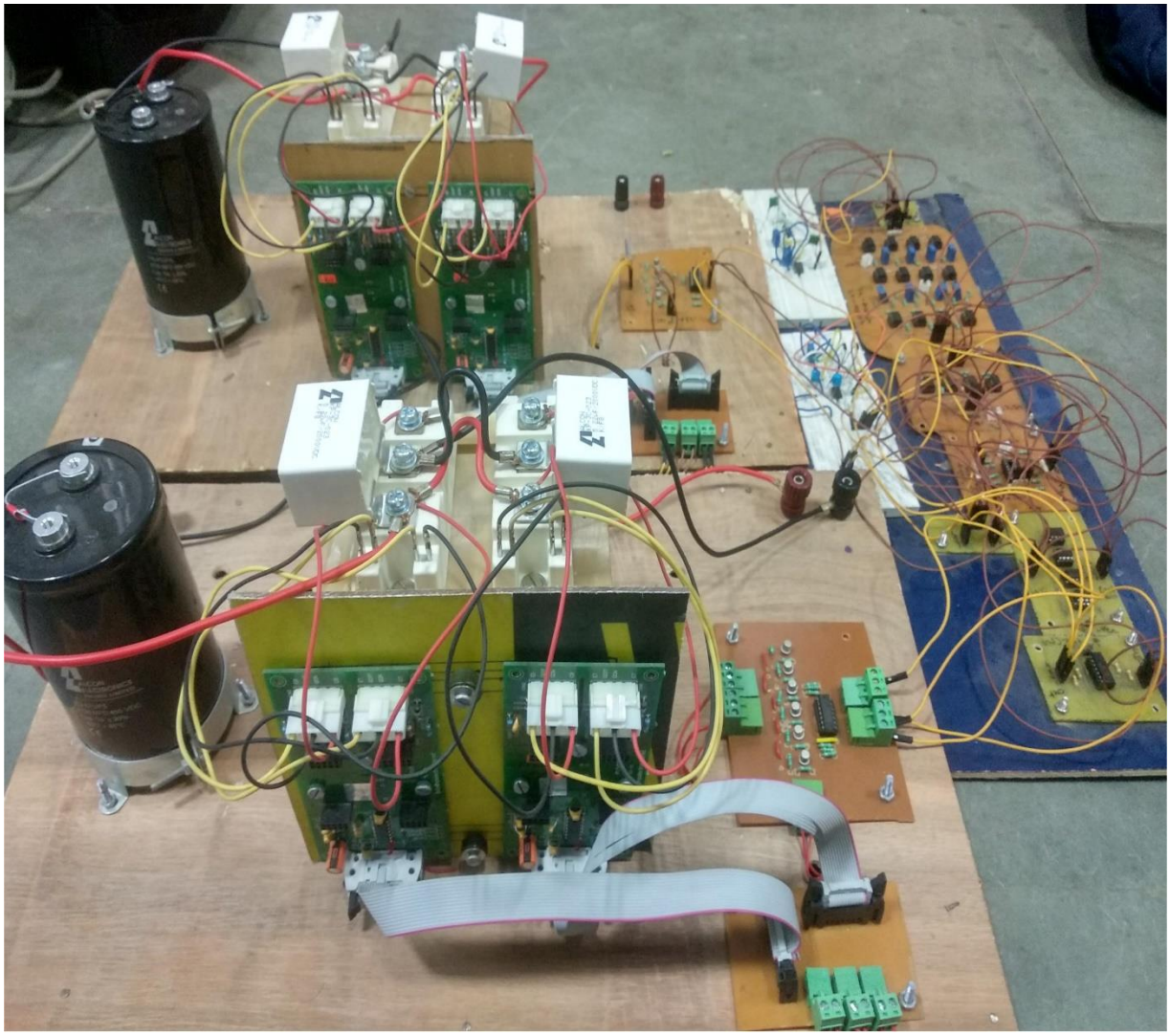


Fig.6.1 Hardware System of the Cascaded H-Bridge Multilevel Inverter

Figure 6.2 illustrates the system's overall working idea. The triangular reference wave and the sinusoidal signal wave are produced separately from this circuit. If the input sine wave is 50 Hz, the input AC of the multi-level inverter is 50 Hz. The input phase frequency defines a frequency of the signal output. Each triangle wave is moved to its position for the multiple carrier wave form by adding various DC offset voltages. The Triangular Wave Generator circuit utilizes two working systems: one is an Astable multivibrator and the other an integrating amplifier.

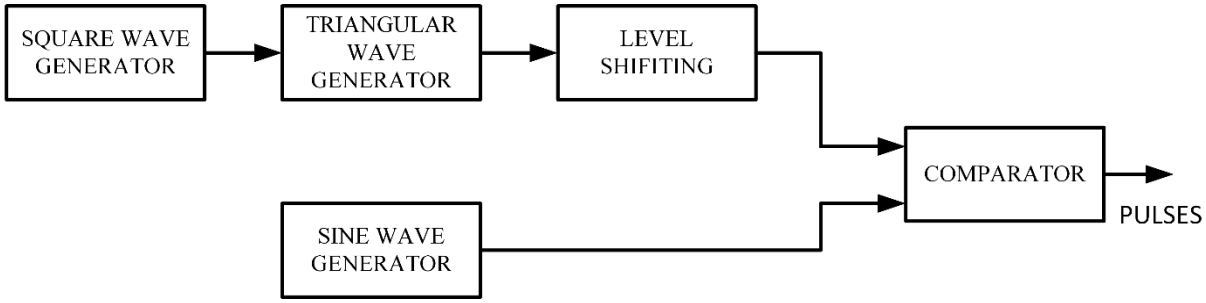


Fig .6.2. Basic circuit used for generating pulses

6.2 SQUARE WAVE GENERATOR:

A very flexible instrument that can be used in many distinct electronic circuits and apps, from voltage amplifiers to filters and signal-conditioners is operational amplifier or op-amp. But the Astable Op-Amp Multi-Vibrator shown in Fig.6.3 is a very simple and very practical circuit built around every general-purpose operational amplifier.

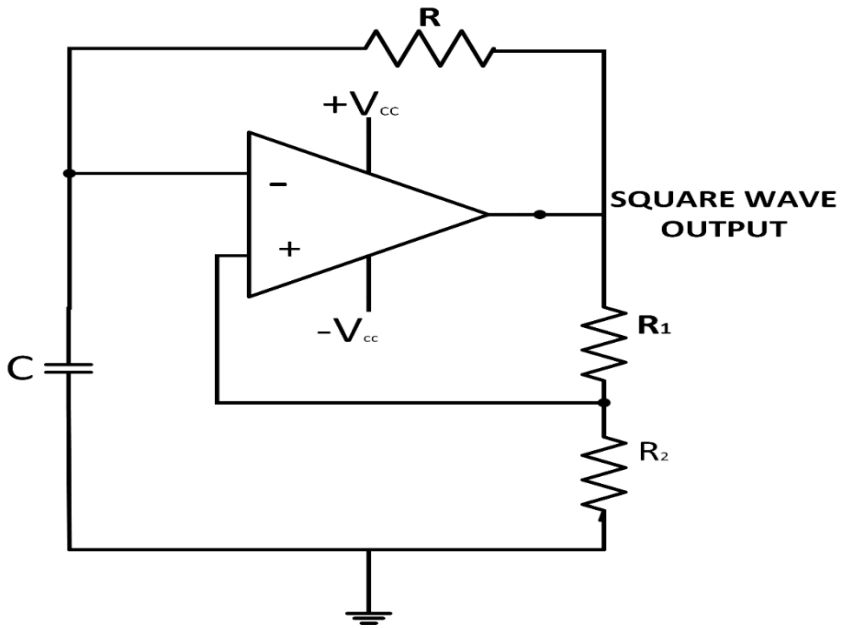


Fig .6.3. Astable multivibrator using op-amp

The OP-amp multivibrator is an oscillator circuit which is Astable, which produces a square waveform via the RC timing network linked to the operating amplifier inverter and the other non-inverting device by means of a voltage divider linked network. The multivibrator Astable has two stages, unlike the monostable or Bistable, since it constantly switches between these two states as time spent in each state controlled by a resistor loading or discharging the capacitor.

The time period of the square wave is given as below

$$T = 2RC\ ln\left(\frac{1+\beta}{1-\beta}\right) \quad (6.2.1)$$

where β is given as below

$$\beta = \frac{R_2}{R_1+R_2} \quad (6.2.2)$$

and the frequency is given as

$$f = 1/T \quad (6.2.3)$$

From the above equation it can observed that for a multi-vibrator frequency oscillation does not only depend on the time constant of the RC but also on the feedback fraction. However the rate of coil oscillation would be equivalent to 1/2RC only, if we used resistor values $R_2 = 10k\Omega$ and $R_1 = 11.6k\Omega$ such that they offered us a feedback portion of 0.462, (β=0.462) as demonstrated. The frequency of square waveform is 1kHz. The values of R and C are 10kΩ and 100nF.

6.3. TRIANGULAR WAVE GENRATOR:

We need a wave input to generate triangular waves. We use square waves to input this project. Just like triangular waves, square waves have equal times of rise and fall to become triangular waves.

$$T = RC \quad (6.3.1)$$

Where frequency is given as

$$f=1/T \quad (6.3.2)$$

where f is 1kHz and values of R and C are 10kΩ and 0.01nF

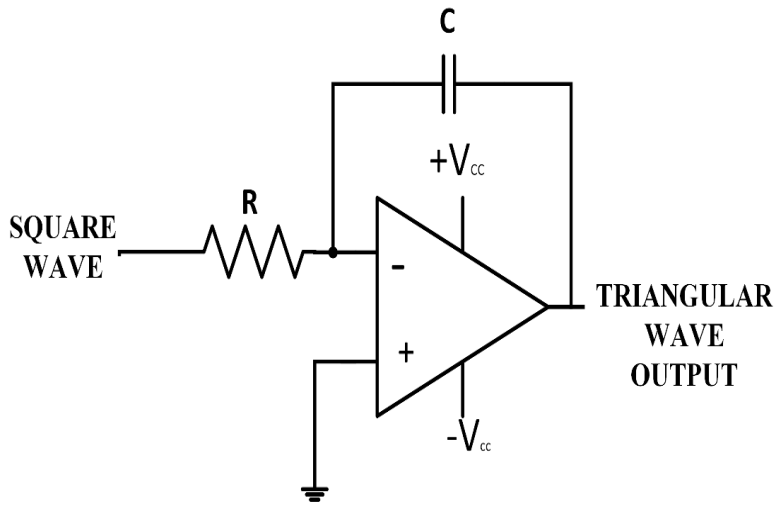


Fig .6.4. Triangular wave generator circuit using op-amp

6.4. SINE WAVE GENERATOR:

A Wien bridge oscillator is one of the easiest sinusoidal wave oscillators to generate a sinusoidal wave form using an RC network instead of a standard LC matched tank circuit is illustrated in Fig.6.5. The oscillator of the bridge Wein is called because the system is focused on the Wheatstone loop in a frequency-selective shape. The Wien Bridge Oscillator is a two-stage, RC-coupled amp system with excellent stabilization, small distortion and simple to adjust, and is a common audio-frequency oscillator circuit.

The operating amplifier output is returned to the two inputs of amplifier. A part of a feedback is connected via the resistor dividing system in R_f and R_b to the inverting input terminal (negative or degenerative feedback), which allows the amplifiers to adjust the voltage increase within narrow boundaries.

The rest, which forms the series and the parallel combinations of R and C, form the feedback network and are redirected via the RC Wien Bride network back to the non-inverting input terminal (positive or regenerative feedback).

In the positive feedback path of the amplifier, the RC network is connected and a single frequency has no phasing shift. The voltages used for the inverting and non-inverting inputs are the same at the selected resonant frequency(f_r) and "in phase" so that positive feedback cancels the negative Feedback Signal that causes the circuit to oscillate.

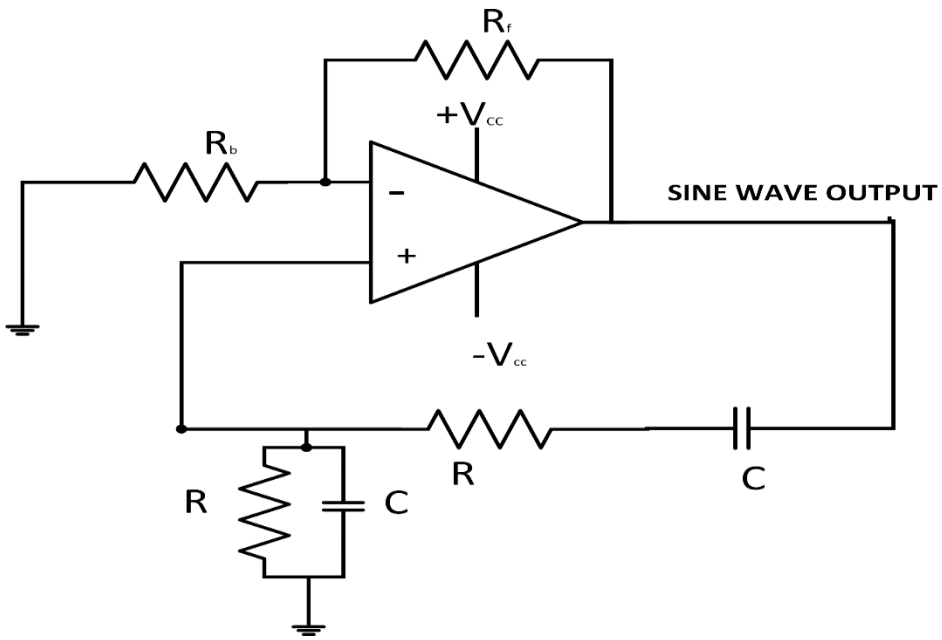


Fig. 6.5. Wein bridge oscillator

For oscillations to start, the voltage gain of the amplifier circuit must be equal to or greater than three "Gain=3" because, as we saw, the input is 1/3 of the output. This value is set by the R_b and R_f feedback resistor network and is given in the ratio $1 + (R_f / R_b)$ in the case of a non-inversion amplifier.

The frequency of oscillations is given as below

$$f = \frac{1}{2\pi RC} \tag{6.4.1}$$

The condition for oscillations is given as

$$R_f = 2R_b \tag{6.4.2}$$

To generate oscillations the values of the R_f and R_b are taken as $2k\Omega$ and $1k\Omega$ and for 50 Hz frequency sine wave, the values of the R and C are taken as 3.183KΩ and 1μF.

6.5. LEVEL SHIFTER CIRCUIT:

We have to generate four triangular with certain dc offset level which can be obtained using level shifter circuit. After triangular wave form generator, we connect to this basic summer circuit which raise the triangular wave by adding the $+V_{dc}$ or $-V_{dc}$. The proposed Circuit is illustrated in Fig.6.6.

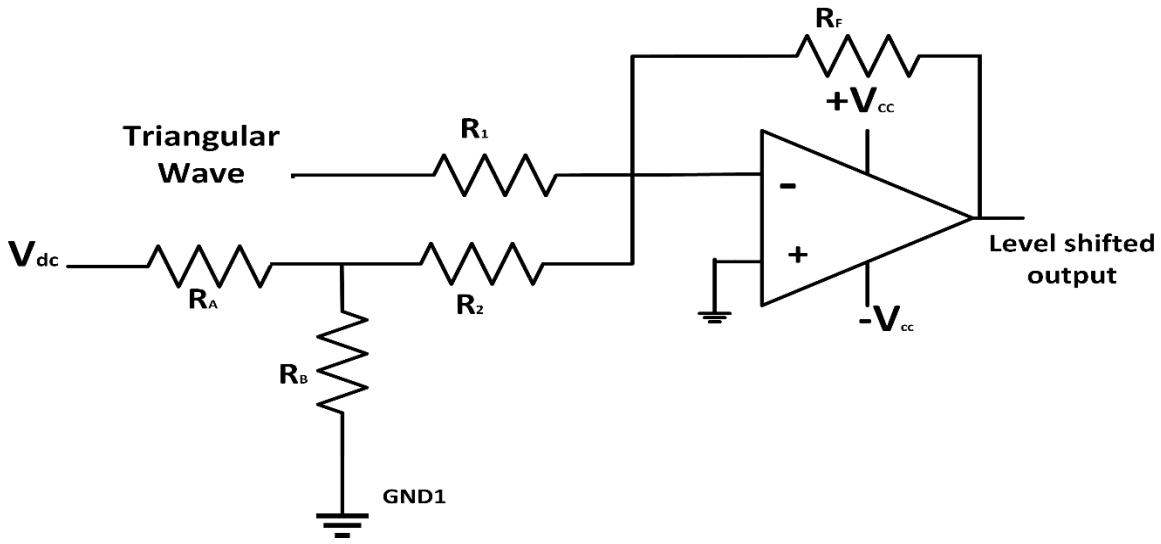


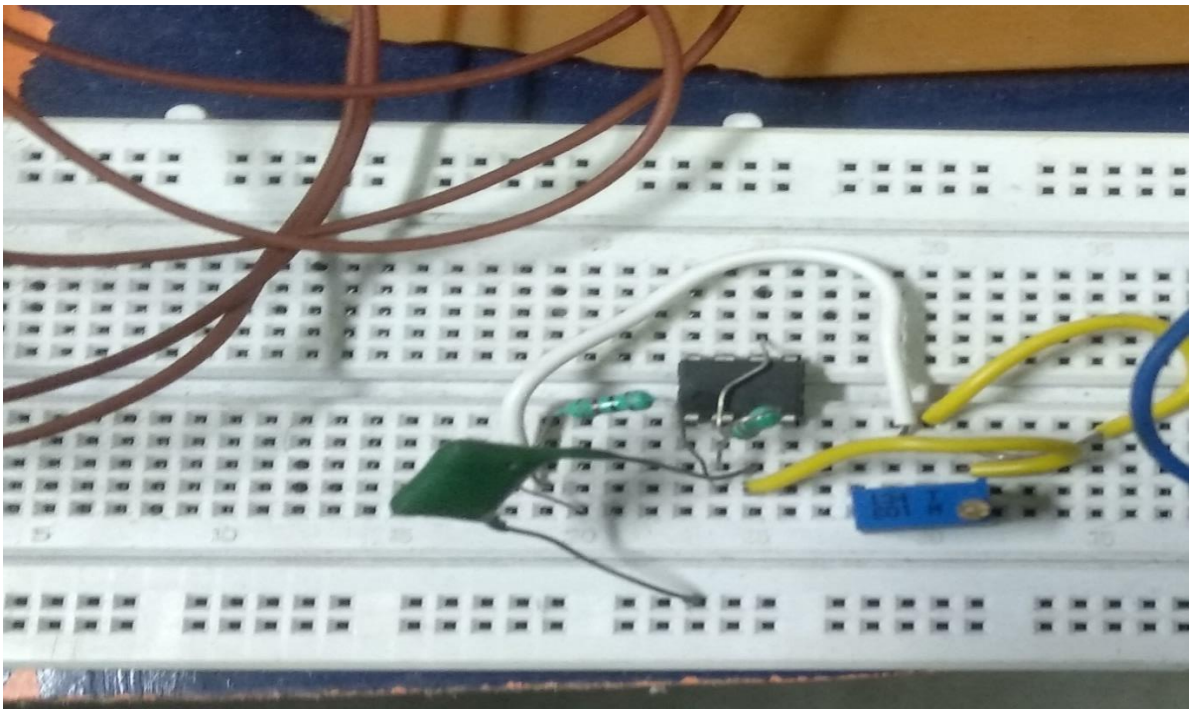
Fig. 6.6. Level shifter circuit

6.6. COMPARATOR:

Here we use basic comparator IC LM339 which gives output as pulses with constant voltage when positive pin signal is greater than negative pin signal with voltage of $+V_{dc}$ given to IC.

6.7. HARDWARE RESULTS:

The square wave generator hardware circuit is shown in Fig.6.7. The output of the Square wave generator is shown in Fig.6.8



1. Fig.6.7. Hardware circuit of Square wave form generator

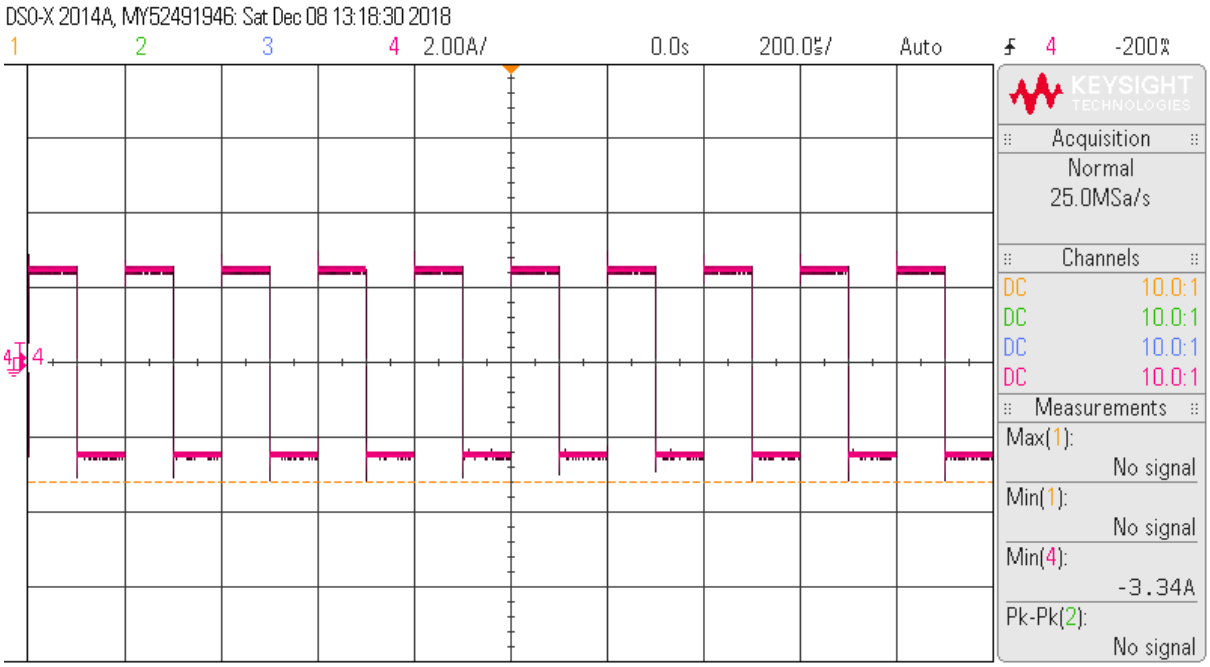


Fig.6.8. Square wave form generator output

The Triangular wave generator hardware circuit is shown in Fig.6.9. The output of the Triangular wave generator is shown in Fig.6.10. The Frequency of the Triangular wave form is 1 kHz.

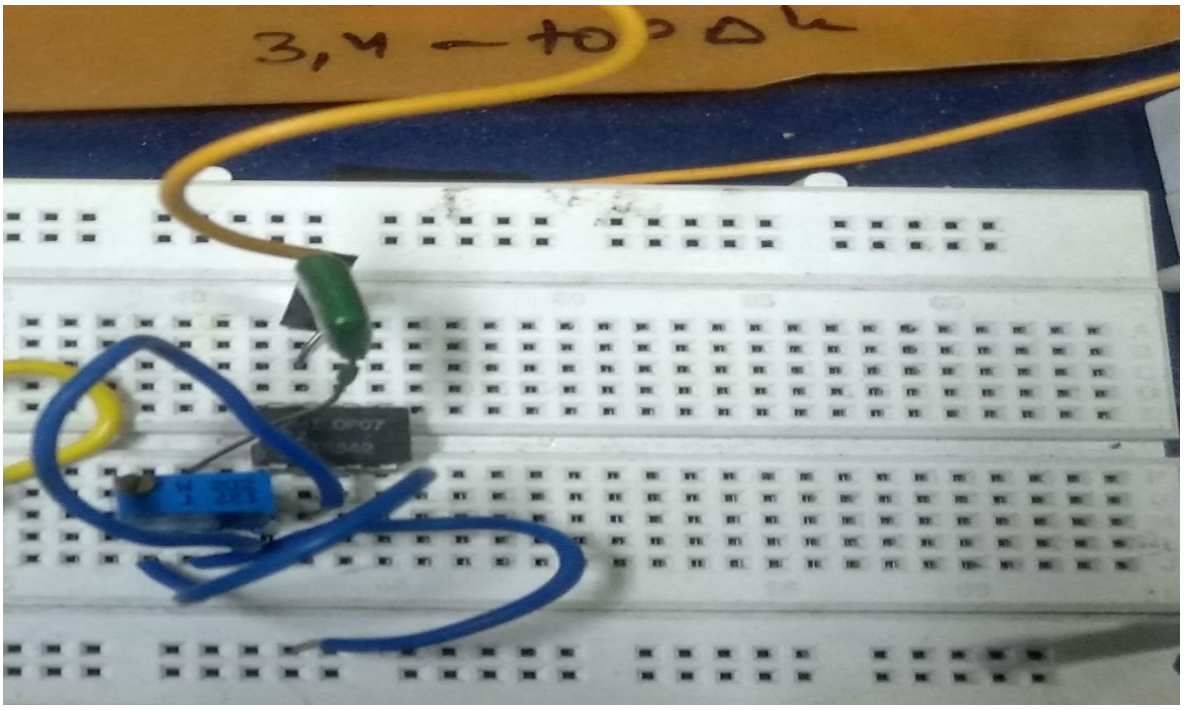


Fig.6.9. Hardware circuit of Triangular wave form generator

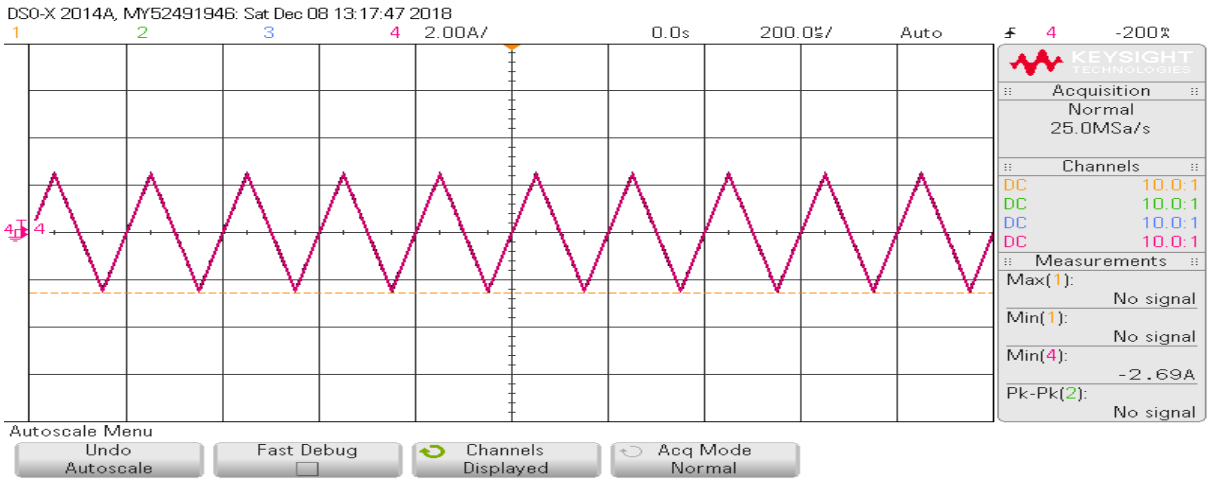


Fig. 6.10. Triangular wave form generator output

The Level Shifter hardware circuit is shown in Fig.6.11. The outputs of level shifter is Four Wave forms having different Dc offsets which are obtained after level Shifting is shown in Fig.6.12.

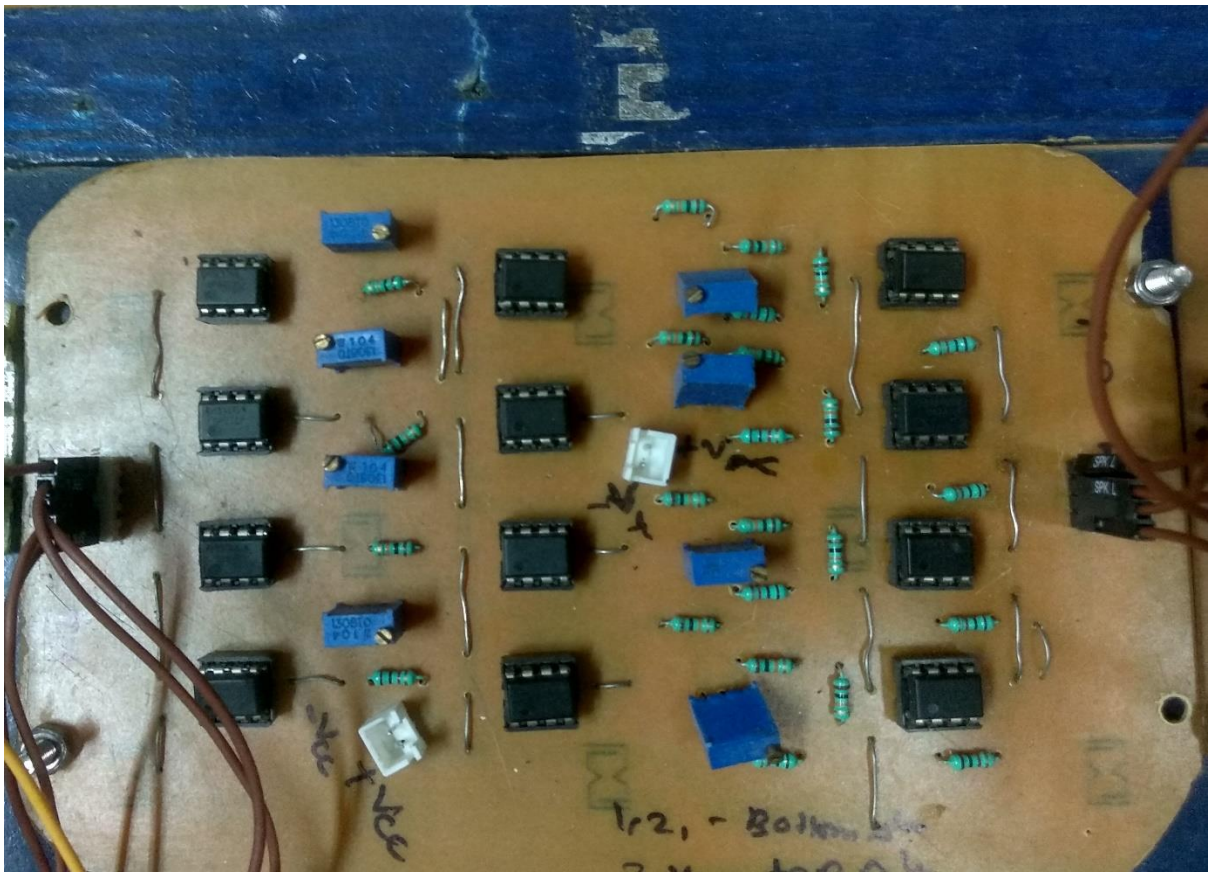


Fig.6.11. Hardware circuit of Level Shifter

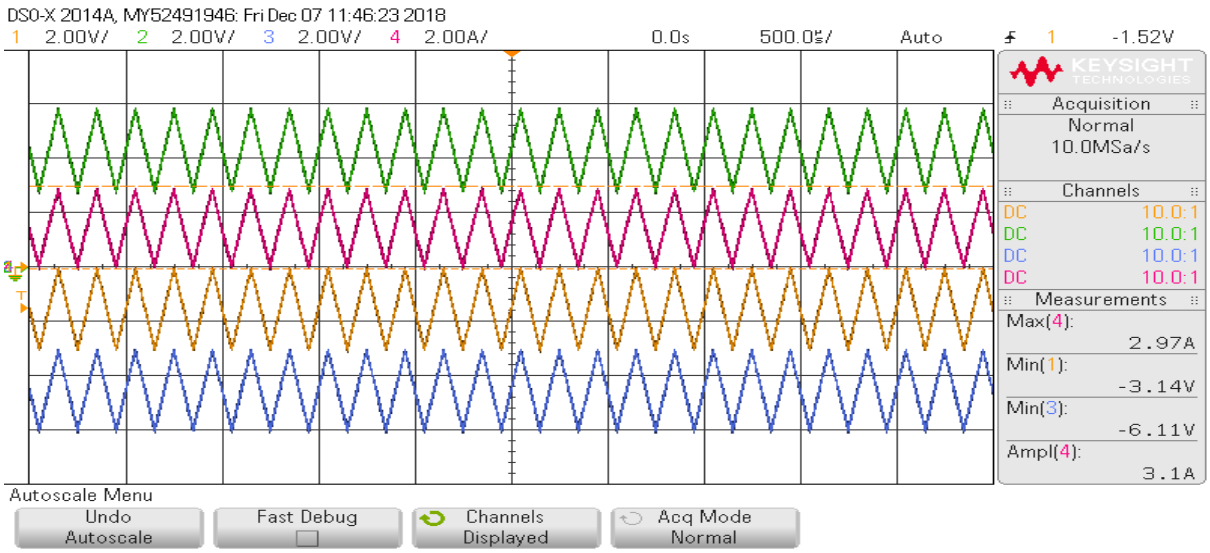


Fig.6.12. Output of level shifter (four triangular waveforms)

The sine wave generator hardware circuit is shown in Fig.6.13. The output of the Sine wave generator whose fundamental frequency is 50 Hz is shown in Fig.6.14

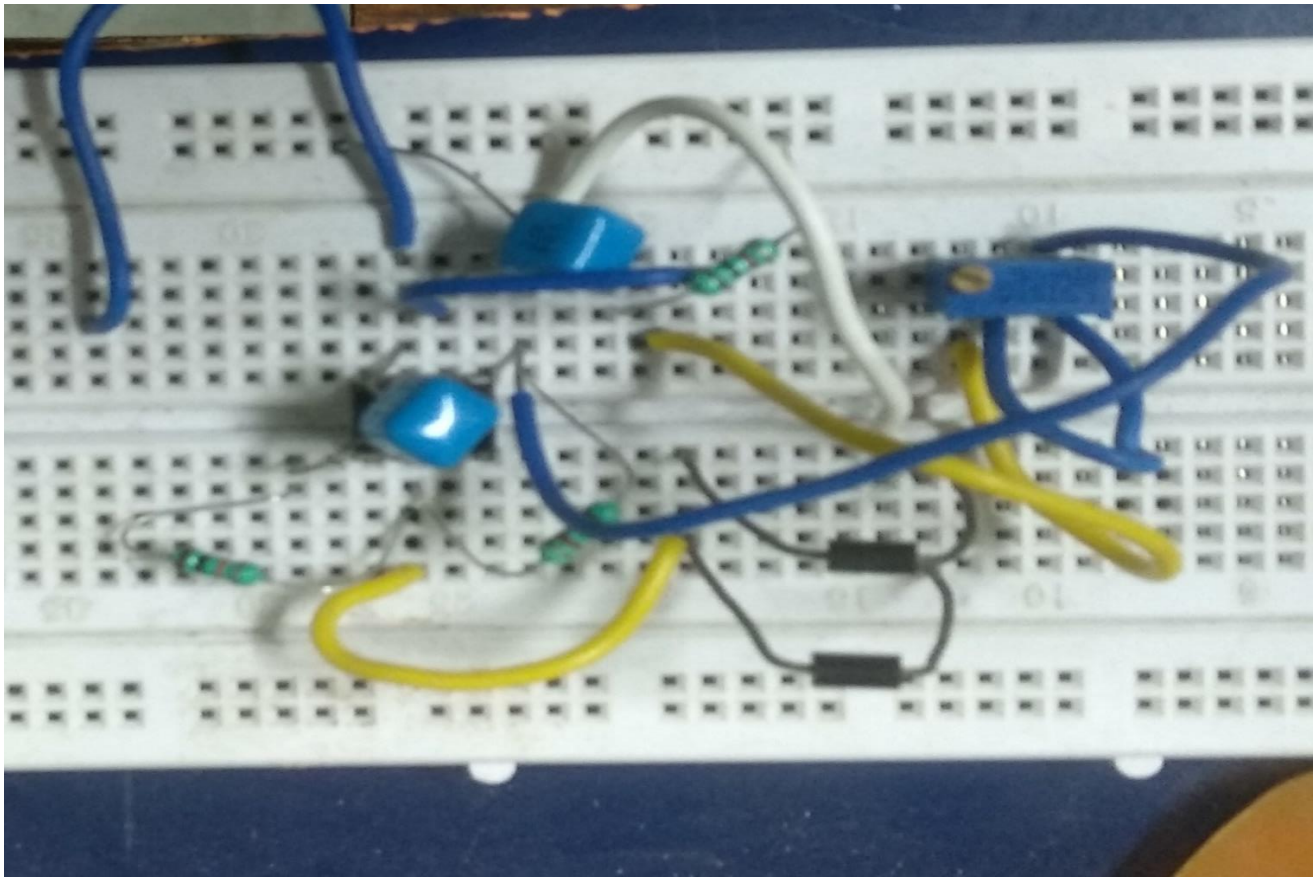


Fig.6.13. Hardware circuit of Sine wave form generator

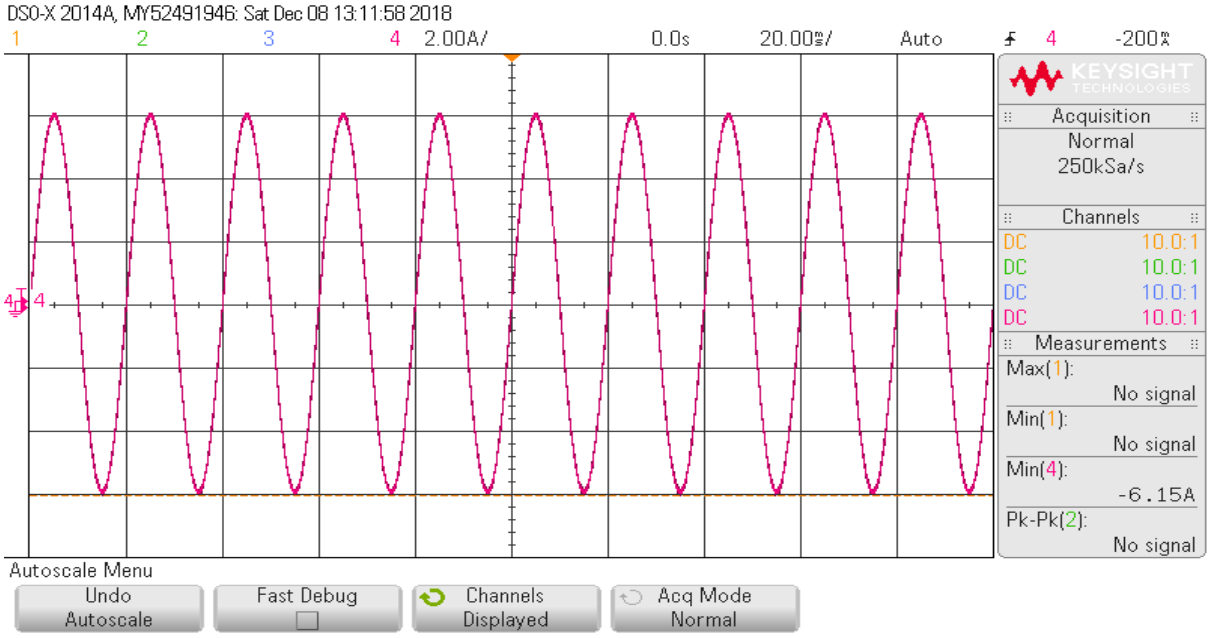


Fig.6.14. output of Wien bridge oscillator

The Comparator hardware circuit is shown in Fig.6.15. Here Sine and four triangular waveforms are compared and pulses are generated. The generated pulses are shown in Fig.6.16

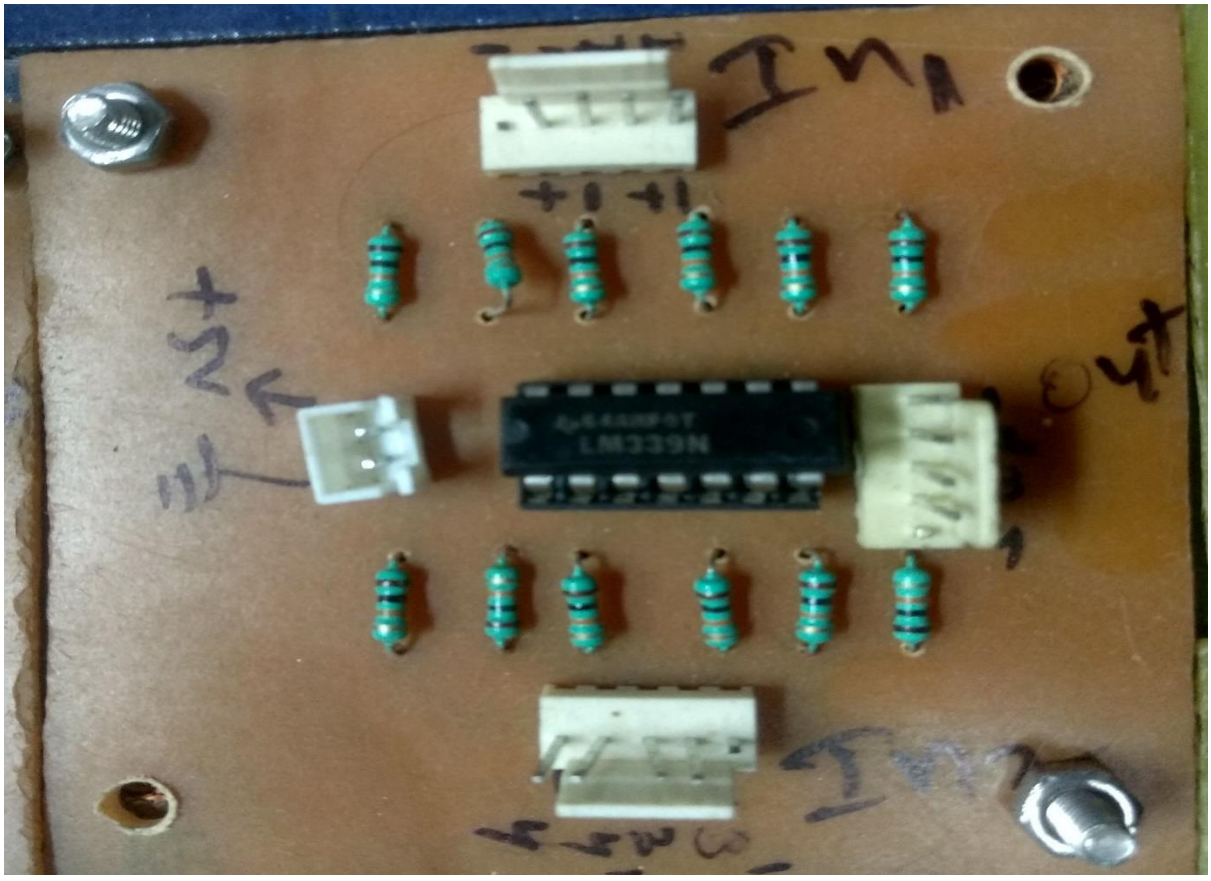


Fig.6.15. Hardware circuit of comparator

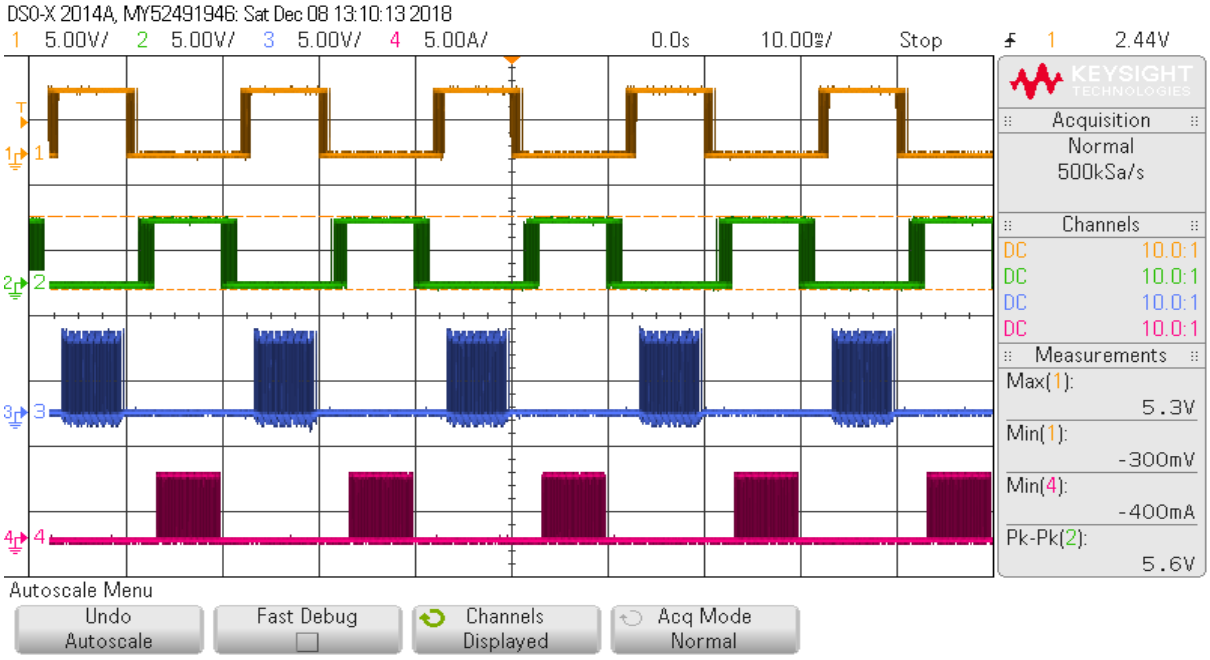


Fig.6.16. Generated pulses

The above pulses are now provided to NOT gate and total eight pulses are given to Cascaded H-Bridge Multilevel Inverter shown in Fig.6.1 and the output Voltage wave form for Five level multilevel inverter is shown in fig.6.17

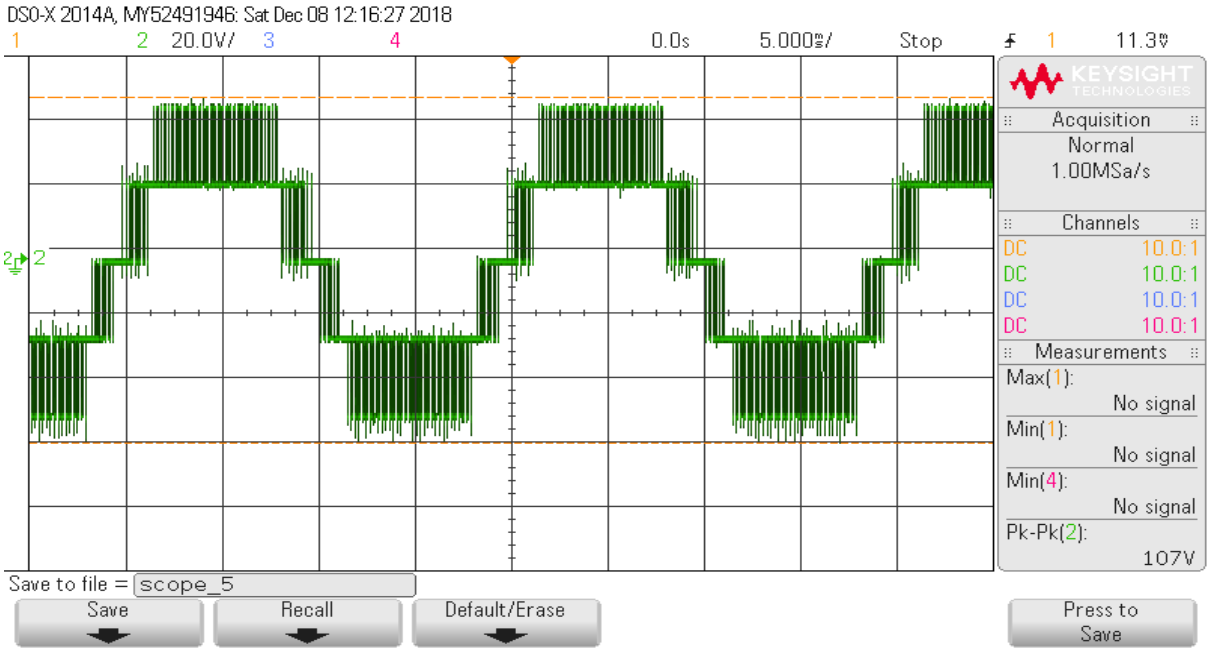


Fig .6.17. Output voltage wave form of Five level multilevel inverter

6.8 Conclusion:

This Chapter has discussed the brief theory of square wave generator, triangular Wave Generator, sine wave generator, level Shifter and comparator required to produce gating Pulses which are then used to turn ON or turn OFF the switches of two H-Bridges connected in Five Level Multilevel Inverter. This Chapter shows the five levels are obtained satisfactorily using designed analog circuits.

Chapter 7

Conclusion and Future Scope

Conclusion

- The main conclusion of this thesis are to study the open loop response of five level MLI Using different modulation techniques. Phase disposition, phase opposition disposition , alternative phase opposition disposition, phase shifting techniques.
- A Five Level MLI has been designed and simulated for load compensation, PQ problems such as harmonic elimination, voltage regulation, reactive power compensation have been mitigated and results have shown for both linear and non-linear loads
- PV-STATCOM has been designed and simulated which is controlled using SRF technique. Tests are carried out to investigate the performance of PV-STATCOM performance under various load conditions
- Cascaded H- Bridge Five level Multilevel inverter prototype have been developed in laboratoty and analog circuits such as square wave generator, triangular wave generator, sine wave generator have been implemented. Performance of Five level inverter has been tested satisfactorily.

Future scope of work

- Closed loop operation of MLI
- Design and testing of new algorithms on Cascaded H-bridge
- Development of PV-STATCOM, its controller design and its implementation in laboratory
- Possible extension of higher level in voltage

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