A NOVEL DTMOS BASED CCCDCC WITH ITS APPLICATIONS

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I, Bharti, Roll No. 2K17/VLS/07 student of M.Tech (VLSI DESIGN AND EMBEDDED SYSTEM), hereby declare that the project Dissertation titled **"A NOVEL DTMOS BASED CCCDCC WITH ITS APPLICATIONS"** which is submitted by me to the Department of ELECTRONICS AND COMMUNICATION ENGINEERING, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associate ship, Fellowship or other similar title or recognition.

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ABSTRACT

In modern electronic devices, there is an essential requirement to decrease the power consumption and minimize the voltage supply to meet the demand of portable devices. This ever - increasing demand of low voltage and low power application has arisen the necessity to design analog circuit working at low supply voltage. DTMOS is one of the non-conventional techniques to design the circuit with low leakage current with low supply voltage.

In this thesis, a novel circuit design of CCCDCC that utilizes DTMOS technique has been proposed. This technique enhances the performance of the circuit design at low supply voltage. To show its applicability, the low pass and high pass filters have been simulated by this technique. The simulations are carried out using PSPICE software and technology used is TSMC 180nm.

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LIST OF ABBREVIATIONS

Abbreviation	Full Form
LV	Low Voltage
LP	Low Power
IC	Integrated Circuit
CMOS	Complementary Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
DTMOS	Dynamic threshold MOSFET
BD-MOSFET	Bulk-driven MOSFET
FG-MOSFET	Floating-gate MOSFET
QFG-MOSFET	Quasi-floating-gate
BD-FG MOSFET	Bulk driven floating gate MOSFET
BD-QFG MOSFET	Bulk driven Quasi-floating gate MOSFET
CM	Current Mode
PMOS	Positive channel Metal Oxide Semiconductor
NMOS	Negative channel Metal Oxide Semiconductor
VLSI	Very Large Scale Integration
CCI	First generation Current Conveyor
CCII	Second generation Current Conveyor

CCIII	Third generation Current Conveyor
DDCC	Differential Difference Current Conveyor
DO-DDCC	Dual Output Differential Difference Current Conveyor
DVCC	Differential Voltage Current Conveyor
CC-CDCCC	Current Controlled Current Differencing Copy Current Conveyor
CCCII	Second-Generation Current-Controlled Conveyor
CCCDCC	Current Controlled Current Differential Current Conveyor
CCCDTA	Current Controlled Current Differential Transconductance Amplifier
FD-CCII	Fully Differential Second Generation Current Conveyor
OPAMPS	Operational Amplifiers
LPF	Low Pass Filter
HPF	High Pass Filter

CHAPTER 1

INTRODUCTION

Emergence of the necessity of analog IC circuit designs operating at low voltage (LV) has been seen in the preceding decade. During latest years, there is an enormous insistence for portable devices which require low power dissipation. High performance digital systems, electronic devices used in medical, engineering, other research field etc. and handheld electronic devices such as tabs, laptops and mobile phones etc that are powered by battery, they all require low power (LP) design.

Thus, a low power approach has appeared as a fast emerging field. The low power operation enhances the battery life and decreases excessive cooling cost. It decreases the size and weight of the devices by using battery with a smaller size and weight. It also avoids failures because of the heating problem.

Integrated circuit (IC) technologies trend to reduce the minimum feature size of MOS transistors so to increase more electronic functions per unit area. However, higher the device density of an IC means a large number of transistors are present in small areas which lead to higher power dissipation and overheating. Thus, it is very essential to reduce the power dissipation of an IC to guarantee the device reliability and functionality [1].

1.1 Motivation for low power techniques

Shrinking in the dimensions of a transistor has lead to the dwindling in the power supply voltage so that the reliability of the device can be maintained. However, decreasing the threshold voltage (V_{TH}) below a certain limit can increases the impact of noise margin and leakage currents [2]. Therefore, scaling down of VTH is considered to be a major challenge in LV and LP applications. This is the main limitation in LP and LV analog circuit designs.

To eliminate this restriction, several CMOS based techniques have been introduced in the literature [3-30]. By utilizing these techniques, the threshold voltage (V_{TH}) is decreased or even removed. The proposed work analyzes the low power DTMOS technique on current conveyor (CCCDCC) and employed them in the first order filters. The filters have a broad range of applications in communication, signal processing and biomedical instruments.

The mostly used low power and low voltage techniques are:

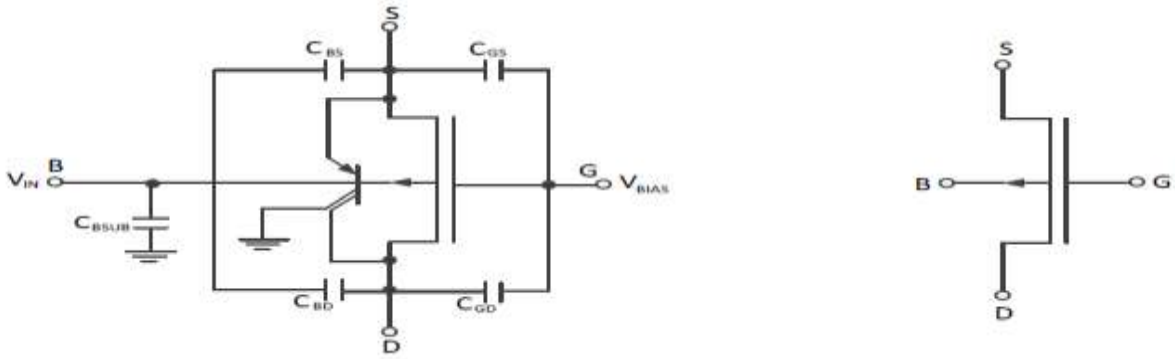
- MOSTs operating in weak inversion [3].
- Self cascode techniques [4].
- Level shifter techniques [2].
- Bulk-driven MOSFET (BD-MOSFET) [5-10].
- Floating-gate approach (FG-MOSFET) [11-15].
- Quasi-floating-gate approach (QFG-MOSFET) [16-19].
- Bulk driven floating gate MOSFET (BD-FG MOSFET) and Bulk driven Quasi-floating gate MOSFET (BD-QFG MOSFET) [20].
- DTMOS [21-30].

The last five techniques are considered as un-conventional. They were proposed to operate under ultra-low voltage and low power conditions.

1.1.1 Bulk- driven MOSFETS

The main feature of bulk-driven MOSFET is that input signal is given to body terminal rather than the gate of a MOS and a minimum voltage is applied between the gate and source terminal so that an inversion layer is formed [5][6]. It will overcome the problem of threshold voltage by removing it from the input signal.

When compared to a same size gate-driven MOS, BD-MOSFET has lower frequency transition and high input noise. It has smaller transconductance because of the smaller depletion layer capacitance as given in [7][8]. These demerits can be counterbalanced by enhancing bias current and altering the dimensions of the device as suggested in [9][10]. Fig. 1.1 illustrates the circuit symbol of BD-MOS.



(a) (b)

Fig. 1.1 (a) Equivalent circuit (b) circuit symbol of BD-MOSFET [5]

1.1.2 Floating-gate MOSFETS

FG-MOS is also known as a multiple-gate device as it has usually two control gates as presented in Fig. 1.2. A bias voltage (V_{bias}) is given to one control gate through large value capacitance. The input signal is given to the second gate G_{in}. It facilitates to shift the threshold voltage of the MOSFET by removing it from the input signal gate [11]. The floating gate voltage is given as:

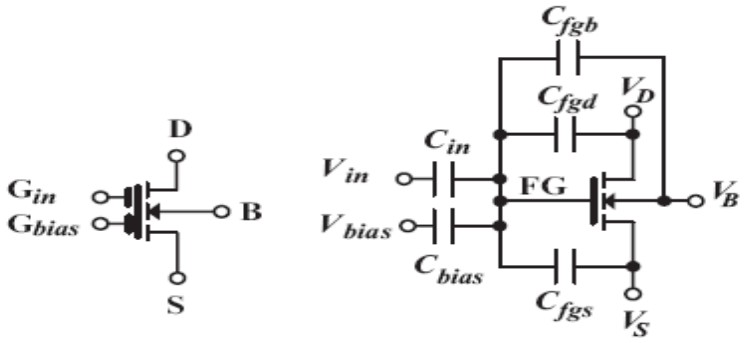
$$V_{FG} = \frac{C_{in}V_{in} + C_{bias}V_{bias} + C_{fgd}V_D + C_{fgs}V_s + C_{fgb}V_B + Q_{FB}}{C_{Total}} \quad (1.1)$$

Where the capacitances C_{in} and C_{bias} are the control gates capacitances at which the input signal V_{in} and the bias voltage V_{bias} is applied respectively. C_{fgb}, C_{fgd} and C_{fgs} denote the floating gate-bulk, gate-drain and gate-source capacitances respectively. C_{Total} is the sum of these capacitances.

$$C_{Total} = C_{in} + C_{bias} + C_{fgd} + C_{fgs} + C_{fgb} \quad (1.2)$$

FG-MOS is mainly used to accumulate data in digital EEPROMs, EPROMs and flash memories [12]. The main concern of FGMOS is that during manufacturing process some residual charges get cumulated on the gate which affects its threshold voltage. In literature [13][14], there are many techniques to eliminate such charges.

But the main problem is that the reliability of device could not be negotiated in the long run by using these methods. Moreover, this technique entails additional circuits and thus increases the silicon areas. Therefore, it is not considered to be an effective technology as compared to others [15]. The most effective technique is a quasi floating gate.

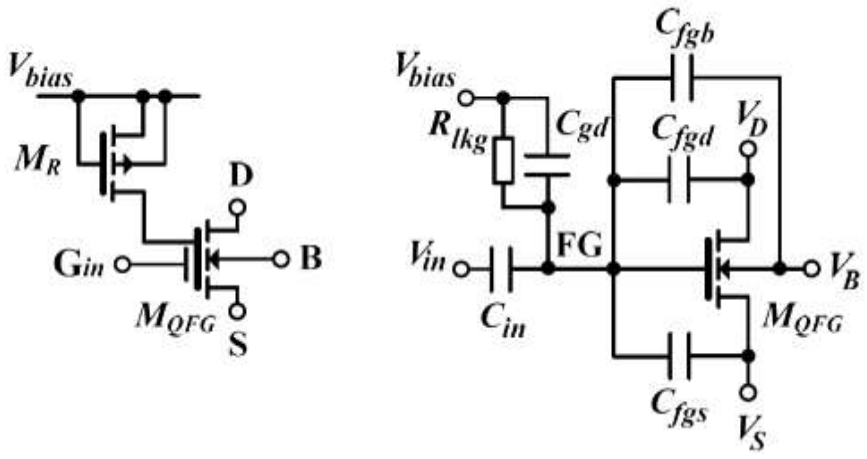


(a) (b)

Fig. 1.2 (a) Circuit symbol (b) Equivalent circuit of Floating gate [11]

1.1.3 Quasi-floating-gate MOSFETS

QFG-MOSFET is considered to be an advanced version of FGMOS as it overcomes the shortcoming faced by the FGMOS [16]. The floating gate is tied to a dc bias voltage using a large-value resistor (R_{large}). This resolves the problem of storing charge by connecting the floating gate to the supply voltage but still, the challenge of usage of the area remains the same. Usually, R_{large} is implemented by a PMOS transistor M_R in a diode- connected form with reversed biasing, which operates in the cut-off region as presented in Fig. 1.3 [17].



(a) (b)

Fig. 1.3 a) QFG-MOS symbol b) realization circuit [17]

A supply voltage is provided at the gate of PMOS to make sure that the no current flows in PMOS. This works as a large pull-up resistor. This circuit connection always guarantees that the PMOS operates in the cut-off region and thus leaving the gate of NMOS in a quasi floating state. This topology eradicates the problem of accumulation of charge. For the realization of QFG based PMOS transistor, a pull-down resistor (R_{large}) should be implemented by NMOS i.e. its gate is connected to ground which makes sure it is always operated in the cut-off region [18].

The advantages of QFG-MOS are as follows:

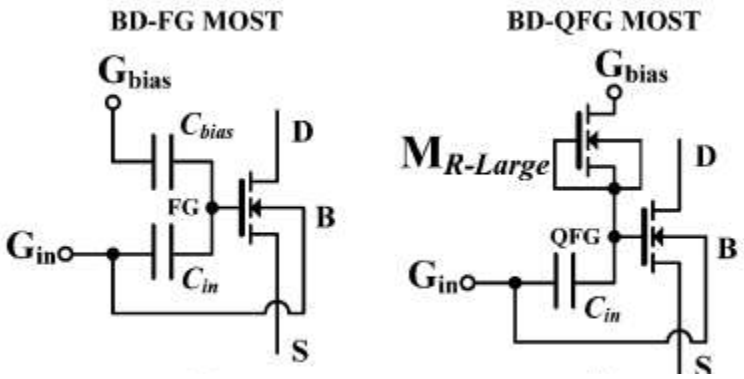
- Elimination of charge being stored at the floating gate.
- Required less silicon area as compared to FGMOS.
- QFG-MOS has the smaller overall transconductance and transition frequency than conventional MOSFET but greater than FGMOS.

This technique uses a large value of resistor due to which low frequency signals are not affected. The main concern with the QFG-MOSFET is that greater the overall output conductance, lesser the overall gain of the circuit as compared to the FGMOS technique [19]. Another challenge is to make sure that that the cut-in voltage of diode-connected transistor must be always less than the voltage at the floating gate. Some of these disadvantages will be overcome by the following techniques.

1.1.4 Bulk driven floating-gate MOSFETS and Bulk driven Quasi floating-gate MOSFETS

It is emerging as the most capable un-conventional techniques which contain all the advantages of BD, FG and QFG-MOS and repress their limitations [20]. In BD-FG MOST, a DC bias (G_{bias}) is given to the control terminal of FGMOS. The input gate (G_{in}) is tied to the body terminal of the FGMOS as depicted in Fig. 1.4(a).

It is observed from Fig. 1.4(b) that input signal (G_{in}) is applied to body terminal and its other side is tied to a suitable input capacitance (C_{in}). The terminal QFG is connected to a diode- connected MOSFET ($M_{R\text{-}large)}$ which is CMOS realization of a resistor. This resistor is pulled up by a bias voltage (G_{bias}).



(a) (b)

Fig. 1.4 (a) Symbol of BD-FG MOS [20] (b) BD-QFG MOS [20]

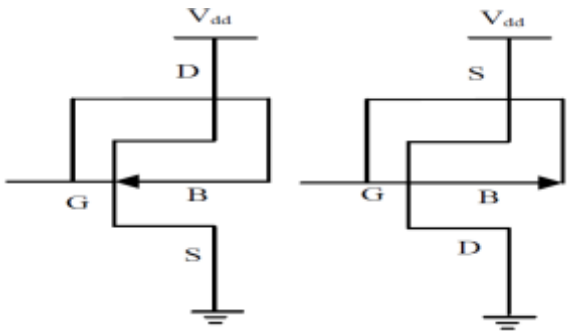
Despite that, the techniques FG, BD, QFG provide the advantage of designing the analog circuits in LV and LP but they also have some shortcomings. One of which is that their overall transconductance is smaller than that of a traditional MOSFET which not only reduces gain-bandwidth product but also increases input noise.

Moreover, FG and QFG-MOS do not support DC signals due to their control input capacitances. These disadvantages were conquered by BD-FG MOS and BD-QFGMOS techniques. They processed AC as well as DC signals. Unlike QFG, BD and FG, they have high transconductance which is very near to traditional MOSFET transconductance. They also have higher bandwidth and low input noise as compared to QFG, BD and FG-MOS.

1.1.5 Dynamic threshold MOSFETS (DTMOS)

DTMOS is one of the non-conventional techniques where the gate which is the input terminal is tied to the body terminal of a transistor as shown in Fig. 1.5 [21][22]. Scaling down of supply voltage is done to reduce power consumption. But the reduction of supply voltage below $3V_{TH}$ will degrade the speed of the circuit [23]. Moreover, tolerance of leakage current determines the reducing factor of the threshold voltage. This value should not be less than 0.7V.

To solve these problems, DTMOS technique is used that has a high V_{TH} at zero bias and low V_{TH} at $V_{GS} = V_{DD}$. This technique reduces the V_{TH} without the degradation of the circuit's performance as conferred by authors in [24-28]. For fabrication of DTMOS based CMOS, triple well technology is used in which NMOS and PMOS are independently biased [29]. This is crucial to circumvent any latch-up problems [30].



(a) (b)

Fig. 1.5 DTMOS based (a) NMOS transistor (b) PMOS transistor [29]

1.2 Current Conveyors

The emergence of the need for novel circuit designs in LV and LP has been observed in the past decade. Designs with a current mode (CM) technique have been preferred over voltage mode (VM) technique [31][32]. It has superiority over voltage mode because of higher bandwidth, speed advantages, better operational accuracy, large dynamic range, and low power consumption with a simple circuit [33]. Therefore, the CM design topology emerges to be an apt design for analog VLSI.

CM design consists of circuits which are controlled by current stimuli. The circuit designs with CM approach have better performance in respect of slew rate, bandwidth and low-voltage characteristics than in VM approach. Moreover, the constraint of a constant gain-bandwidth product has been corrected using CM approach [34].

There are many applications in the literature which are based on CM design approach. Some of them are CCI [35], CCII [36], CCIII [37], DDCC [38], DVCC [39], CCCII [40], CC-CDCCC [41], CCCDTA [42], MO-DDCC [43] and CCCDCC [44].

1.2.1 Generation of Current Conveyor

The current conveyor is widely employed as a functional block for the applications working in current mode. In literature [35-37], the author had introduced the first (CCI), second (CCII) and third the generation current conveyors (CCIII) respectively.

1.2.1.1 First Generation Current conveyor (CCI)

The first generation current conveyor (CCI) was introduced in 1968 [35]. It has basically three ports- two input port (X and Y) and one output port (Z) as shown in Fig. 1.6. In CCI±, positive and negative signs indicate that the output current is in the same and opposite direction as that of input current at X port respectively.

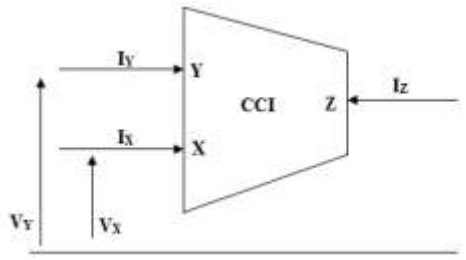


Fig. 1.6 Symbol of CCI [35]

It has following characteristics.

- the port Y current is equal to the port X current.
- voltage of port X will appear at port Y.
- the port Z current follows the port X current.

The following matrix provides the working operation of CCI [35].

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1.3)$$

The main disadvantage of CCI was that their application ranges were limited because of low input impedance of both the input ports. This set problems to acquire practical designs. At that time this design was considered as less flexible and versatile.

1.2.1.2 Second Generation Current conveyor (CCII)

To overcome the inadequacy of CCI, CCII was introduced in 1970 [36]. It also has three ports – two input ports and one output ports. But now port Y has been made a high impedance port as shown in Fig. 1.7.

To evade the loading effect at the input of CCII, one of the two input port has been made a high impedance port. This change in the circuit design of CCII has enabled its applicability to a wide range of applications. It has also made the circuit more flexible as now it can be applied to voltage mode along with current mode applications.

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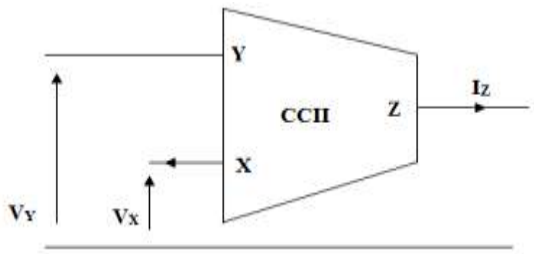


Fig. 1.7 Symbol of CCII [36]

The CCII also provide a substitute design against operational amplifiers. CCII has also overcome the limitations of low slew rate and finite gain-bandwidth product of operational amplifies. The applications of OPAMP can also be realized by CCII with improved characteristics and fewer circuit components such as oscillators, integrators, filters and differentiators [46-53].

The characteristic of CCII has been described by the following the matrix [36].

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1.4)$$

1.2.1.3 Third Generation Current conveyor (CCIII)

Like CCI and CCII, CCIII has three ports namely X, Y and Z as illustrated in Fig. 1.8 [37]. The correlation between the currents and voltages port is shown in the matrix (1.5). The matrix is similar to that of CCII with the difference that the port Y gets the inverted current of X port.

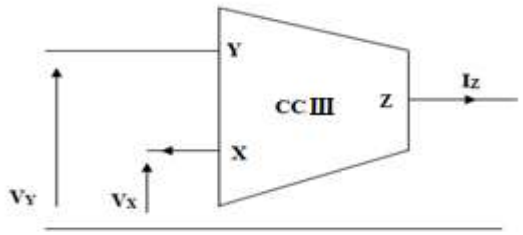


Fig. 1.8 Block representation of CCIII [37]

This property is used in floating current circuit designs [54]. CCIII is functional for the current flowing in the floating branch of any circuit. This design is employed in the realization of floating inductance, multifunction filters, etc [55].

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{1.5}$$

In the CMOS realization of CCIII, current mirrors having high performance are used. These current mirrors facilitate the features of cascading circuits [56]. These offer high output resistance and the excellent dynamic swing [56].

It has the following characteristics:

- broad frequency response
- High accuracy
- High linearity

These basic current conveyors have various applications in current mode circuits but they suffered some of the limitations which are covered by the other current conveyors like CCCII, DDCC, DVCC and MO-DDCC. The next chapter contains the literature review about the limitation of the basic current conveyors and it also describes another current conveyor i.e. CCCDCC with its significances.

1.3 Thesis Organization

Organization of the thesis has been done in five chapters.

CHAPTER 1: A summary of low power techniques has been explained in this chapter. It also gives a brief of basic current conveyors and their limitations.

CHAPTER 2: This section comprises a brief overview of literature work on DTMOS. Due to restriction in performance of older current conveyor, new circuit CCCDCC was introduced. This chapter explains the circuit design of conventional CCCDCC.

CHAPTER 3: This chapter describes the proposed work in which the use of DTMOS technique in the conventional CCCDCC circuit design has been done. The DTMOS technique has been applied in the current controlled current differential current conveyor (CCCDCC) and has enhanced the characteristic over conventional circuit design. To show the applicability of proposed DTMOS CCCDCC, it has been employed in the LPF and HPF.

CHAPTER 4: In this chapter, simulations and results analysis have been carried out. A comparative study has been made consisting proposed DTMOS CCCDCC and the existing current conveyors.

CHAPTER 5: A brief conclusion and future work have been discussed in this chapter.

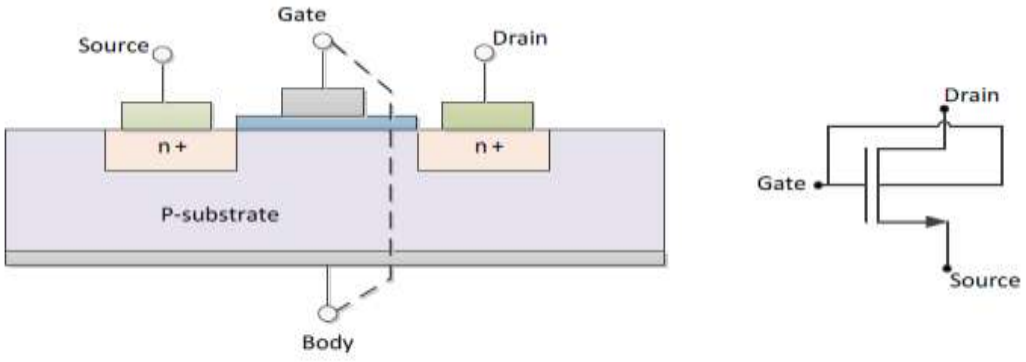
CHAPTER 2

LITERATURE SURVEY

There is no denying fact that the demand for high performance of analog circuit with low power applications has grown quickly. To minimize power consumption, the best option is to scale down the supply voltage. There are other parameters such as threshold voltage which also needed to be scaled down with its less impact on leakage currents. Such a challenge is overcome by technique DTMOS i.e. Dynamic Threshold MOSFET [22].

2.1 Dynamic threshold MOSFET (DTMOS)

Assaderaghi in 1997 proposed the DTMOS technique, which is accomplished by joining the gate terminal to the body terminal of the transistor which dynamically changes its threshold voltage as portrayed in Fig. 2.1 [24].



(a) (b)

Fig. 2.1 (a) Cross-section view (b) Circuit symbol of DTMOS [24]

In this technique when input is applied at the gate, threshold voltage is reduced as shown in equation (2.2) and thus driving capability of transistor is increased [25]. Turning off the transistor results in high threshold voltage which leads to low leakage current. When voltage is applied to the input terminal i.e. gate terminal, the body-source voltage can be controlled as input voltages changes. Thus, ensuring V_{GS} = V_{BS} all the time, threshold voltage decreases as the body source junction experiences the forward biasing. Threshold voltage (V_{T0}) without body biased is given as [22]:

$$V_{T0} = 2\Phi_F + V_{FB} + \frac{\sqrt{2\epsilon_S q N_a (2\Phi_F)}}{C_{OX}} \tag{2.1}$$

Here, C_{OX} denotes gate oxide capacitance, N_a represents channel doping, Φ_F is Fermi potential, ϵ_S is permitivity, q denotes electron charge and V_{FB} signifys flat band voltage. Threshold voltage (V_{TH}) due to applied V_{BS} is given as:

$$V_{TH} = V_{T0} - \gamma\left(\sqrt{|2\Phi_F|} - \sqrt{|2\Phi_F| - V_{BS}}\right) \tag{2.2}$$

Where γ is given by $\frac{\sqrt{2\epsilon_S q N_a}}{C_{OX}}$. To attain the lowest value of threshold voltage, V_{BS} should be equal to $|2\Phi_F|$ which is shown as [22]:

$$V_{THmin} = |2\Phi_F| + V_{FB} \tag{2.3}$$

2.1.1 Theory of operation

The small signal model is illustrated in Fig. 2.2. Body transconductance (g_{mb}) is also taken into consideration when body biased voltage is used. Thus, DTMOS transistor has higher effective transconductance (g_{eff}) as given in equation (2.4). The effective transconductance (geff) is increased from g_m to (g_m + g_{mb}) and both transconductances contribute to the conduction current [26].

$$g_{eff} = g_m + g_{mb} \tag{2.4}$$

The relationship between the gate and body transconductance is given in equation (2.5). Here, C_{BC} is body channel capacitance and C_{GC} is gate channel capacitance [23].

$$\frac{g_m}{g_{mb}} = \frac{C_{BC}}{C_{GC}} = 0.2 - 0.4 \tag{2.5}$$

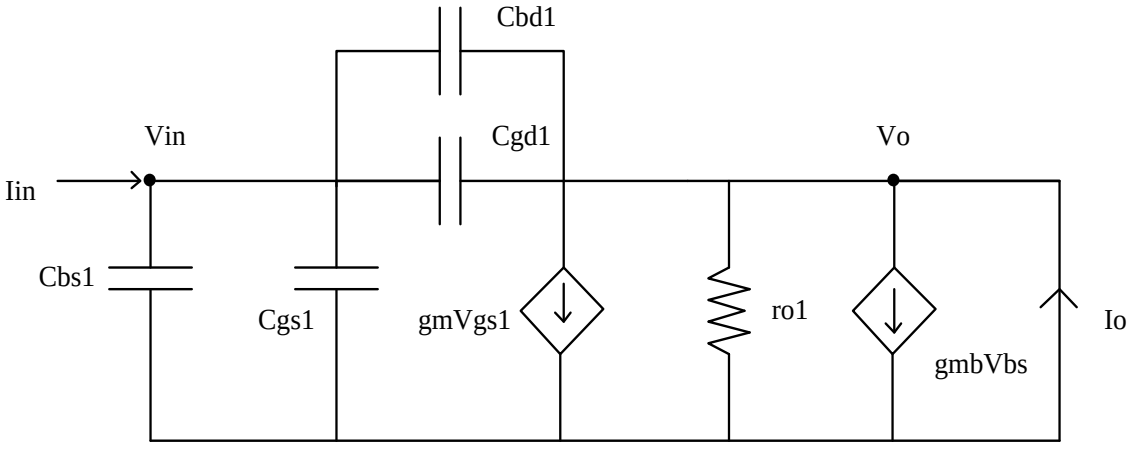


Fig. 2.2: DTMOS based small signal model of transistor

Determining the transition frequency (f_t) for frequency performance of DTMOS transistor.

Applying input voltage $V_{in:}$

$$V_{gs1} = V_{bs1} = V_{in} \tag{2.6}$$

using KCL at input terminal:

$$I_{in} = V_{in}\left(sC_{bs1} + sC_{gs1}\right) + (V_{in} + V_o)(sC_{bd1} + sC_{gd1}) \tag{2.7}$$

using KCL at output terminal:

$$I_o = \frac{V_o}{r_{o1}} + g_{mb}V_{gs1} + g_m V_{gs1} + (V_{in} + V_o)(sC_{bd1} + sC_{gd1}) \tag{2.8}$$

as $V_{gs1}=V_{in,\ the}$ equation (2.8) will be:

$$I_o = \frac{V_o}{r_{o1}} + (g_{mb} + g_m)V_{in} + (V_{in} + V_o)(sC_{bd1} + sC_{gd1}) \tag{2.9}$$

For unity gain current gain, $I_{in}=I_o$, Vo=0 and neglecting ro1:

$$\left(g_{mb} + g_m - sC_{bd1} - sC_{gd1}\right) = \left(sC_{bs1} + sC_{gs1} + sC_{bd1} + sC_{gd1}\right) \tag{2.10}$$

To get frequency response, substitute s = jω and $\omega=\omega_t$ when for unity current gain

$$\omega_t = \frac{g_{mb} + g_m}{C_{bs1} + C_{gs1} + 2C_{bd1} + 2C_{gd1}} \tag{2.11}$$

$$f_t = \frac{g_{mb} + g_m}{2\Pi(C_{bs\,1} + C_{gs\,1} + 2C_{bd\,1} + 2C_{gd\,1})} \tag{2.12}$$

where f_t is the transition frequency. Let $C_{bs\,1} = C_{gs\,1} = C_{bd\,1} = C_{gd\,1} = C$ then,

$$f_t = \frac{g_{mb} + g_m}{12\pi C} \tag{2.13}$$

It can be seen that higher transconductance results in the enhancement of the bandwidth and diminution in noise spectral density [27][28]. The noise spectral density is expressed by the equation (2.14). Here i^2_{ni} denotes drain current produced by noise sources and its unit is $A^{2.}$

This non-conventional technique of DTMOS does not require any external components so it uses less silicon area compared to other low power techniques. Hence, DTMOS proves to be more efficient over any other body bias techniques.

$$v^2_{noise}\,(f) = \frac{i^2_{ni}}{(g_m + g_{mb})^2} \tag{2.14}$$

2.2 Current controlled current differential current conveyor (CCCDCC)

Earlier current conveyor uses single-ended topology whereas many recent analog circuits use differential signals like DDCC [38], DVCC [39], FD-CCIIs [45], CC-CDCCC [41] and CCCDTA [42]. To solve this problem, CCCDCC [44] was introduced which has the differential feature of CCCDTA and CCII advantages.

2.2.1 Principle of CCCDCC

The port X_1 and X_2 act as a current differential input. High input impedance port Y is the voltage port. The output ports Z_d and Z_{-d} behave as current differential. The Z and Z_- ports mirror the current of port X_1. The symbolic diagram of CCCDCC is presented in Fig. 2.3. I_B denotes bias current [44].

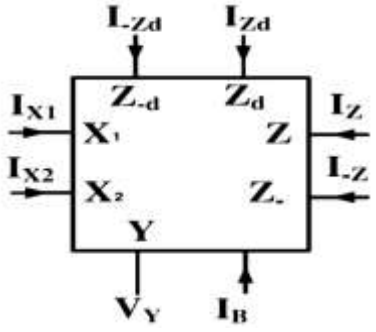


Fig. 2.3 Symbolic diagram of CCCDCC [44]

$$\begin{bmatrix} V_{X1} \\ V_{X2} \\ I_Y \\ I_Z \\ I_{-Z} \\ I_{Zd} \\ I_{-Zd} \end{bmatrix} = \begin{bmatrix} R_{X1} & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & R_{X2} & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{X1} \\ I_{X2} \\ V_Y \\ V_Z \\ V_{-Z} \\ V_{Zd} \\ V_{-Zd} \end{bmatrix} \quad (2.15)$$

The hybrid matrix represents the operation of CCCDCC [44] is shown in (2.15). Here, V_{X1},V_{X2}, V_Y,V_Z, V_{-Z}, V_{Zd}, V_{-Zd} and I_{X1}, I_{X2}, I_Y, I_Z, I_{-Z}, I_{Zd}, I_{-Zd} denote the voltages and currents of the respective port X, Y and Z. R_{X1} and R_{X2} symbolize parasitic input resistances that can be expressed as [44] :

$$R_{X1} = R_{X2} = \frac{1}{g_{m2}+g_{m6}} - \frac{I_B}{I_{in}(g_{m2}+g_{m6})}\left(\frac{g_{m2}}{g_{m1}} - \frac{g_{m6}}{g_{m5}}\right) \quad (2.16)$$

Here, g_{mi} is the gate transconductance of i^{th} transistor (for i = 1, 2, 5 and 6). I_{in} is the current to the input terminal for determining the parasitic resistances.

The CCCDCC controls parasitic resistances which in turn give rises to electronic tunability. The bias current is used to vary the parasitic resistances at port X_1 and X_2 (R_{X1} and R_{X2}). The cut-off frequency for filters applications can be varied by changing parasitic resistances. Thus, CCCDCC does not require passive resistors externally. This decreases chip area and power consumption.

2.2.2 **Conventional CCCDCC circuit design**

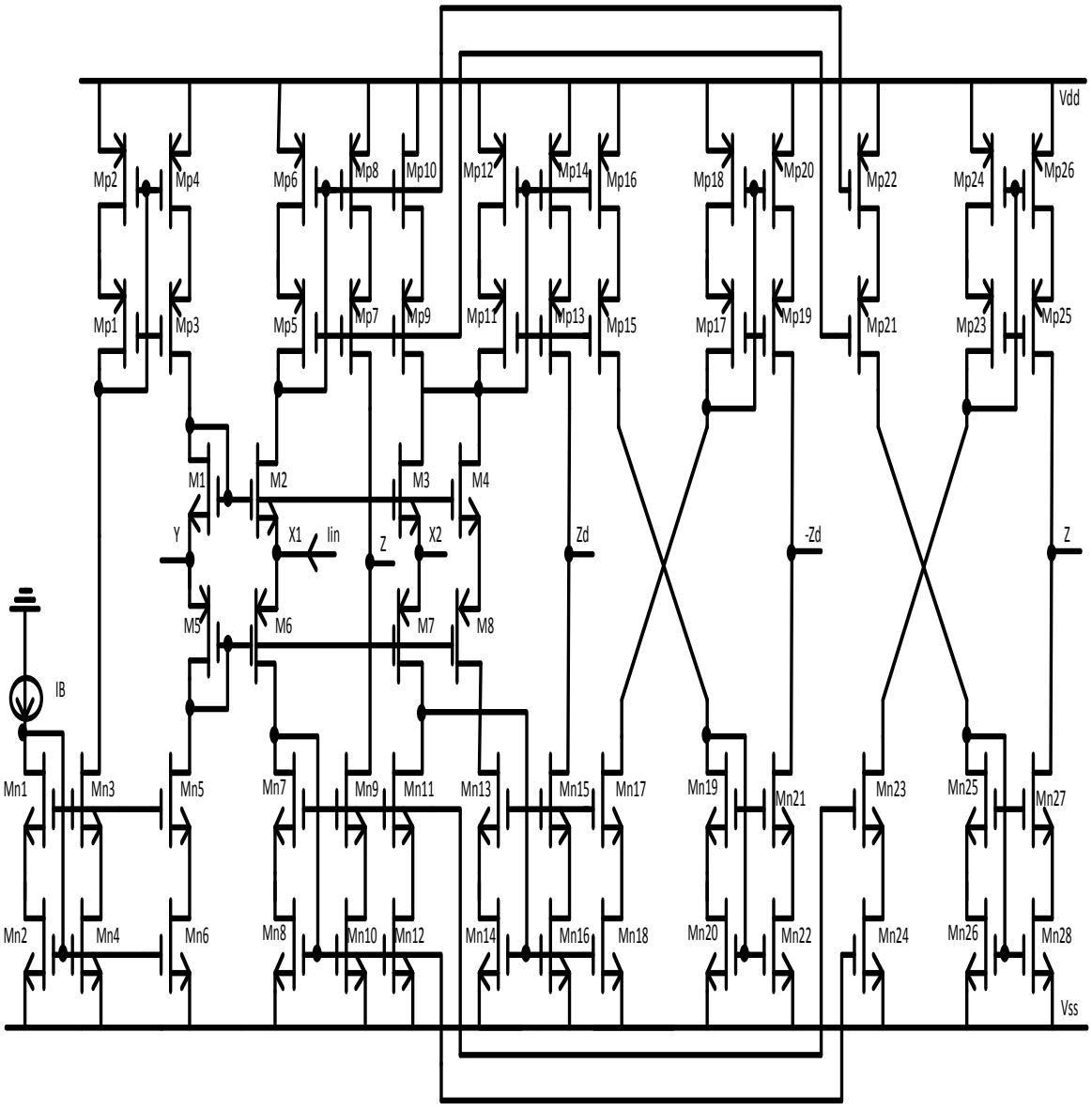


Fig. 2.4 Circuit diagram of the CCCDCC [44]

Fig. 2.4 presents CMOS implementation of the conventional circuit of CCCDCC. Transistors M1, M2, M5 and M6 form a class AB translinear loop for input X_1 terminal and transistors M1, M3, M5 and M7 for input X_2 terminal. The Z_d terminal uses NMOS transistors (Mn7-Mn8 and Mn11-Mn16) and PMOS transistors (Mp5-Mp6 and Mp9-Mp14) which generate the differential current of X1 and X_2 terminals.

The Z_{-d} terminal mirrors the inverted current at Z_d terminal using Mn19-Mn22 and Mp17-Mp20 current mirrors. The current of X_1 port follows the current of Z port using the current mirrors Mn7-Mn10 and Mp5-Mp8. The inverted current of X_1 port appears at Z_- terminal using current mirrors Mn25-Mn28 and Mp23-Mp26.

The circuit design of CCCDCC has eliminated the limitation of basic current conveyors but it has bounded characteristic. The next section will include the proposed work which uses the concept of DTMOS technique on CCCDCC. The proposed technique will enhance the characteristics of basic design which is useful for the low power and low voltage applications.

CHAPTER 3

PROPOSED WORK

The fundamentals of DTMOS technique and the proposed CCCDCC circuit design are explained in this section. To show its applicability, the low pass and high pass filters have been simulated by this technique.

3.1 Proposed CCCDCC using DTMOS technique

The body voltage of the DTMOS transistor varies with the input gate voltage which in turn varies the threshold voltage [22]. The circuit design of the proposed DTMOS CCCDCC is demonstrated in Fig. 3.1 in which the bulk/body terminal is tied to the gate of a transistor and act as input.

Simulation results and analysis depict that the proposed design operates at a lower voltage as compared to the circuit given in [44]. Reduction in the power supply to ± 0.3V results in low power consumption making it useful for low power circuit designs.

Only M1, M2, M3, M5, M6 and M7 transistors use dynamic threshold technique. This technique increases the transconductance of these transistors which minimizes the parasitic resistances at input terminals as shown in equation (3.1) without affecting output resistances.

The terminal of body is connected to the source for remaining transistors. Bandwidth is also enhanced due to an increase in transconductance. The parasitic resistances across input terminal of proposed DTMOS CCCDCC is expressed as:

$$R_{X1} = R_{X2} = \left\{ \begin{matrix} \frac{1}{g_{m\,2}+g_{mb\,2}+g_{m\,6}+g_{mb\,6}} \\ -\frac{I_B}{I_{in}\,(g_{m\,2}+g_{mb\,2}+g_{m\,6}+g_{mb\,6})}\left(\frac{g_{m\,2}+g_{mb\,2}}{g_{m\,1}+g_{mb\,1}} - \frac{g_{m\,6}+g_{mb\,6}}{g_{m\,5}+g_{mb\,5}}\right) \end{matrix} \right\} \quad (3.1)$$

Here, g_{mbi} is the body transconductance of i^{th} DTMOS transistor (for i = 1, 2, 5 and 6). g_{mi} is the gate transconductance of i^{th} transistor (for i = 1, 2, 5 and 6). I_{in} is the current to the input terminal for determining the parasitic resistances. I_B is the bias current.

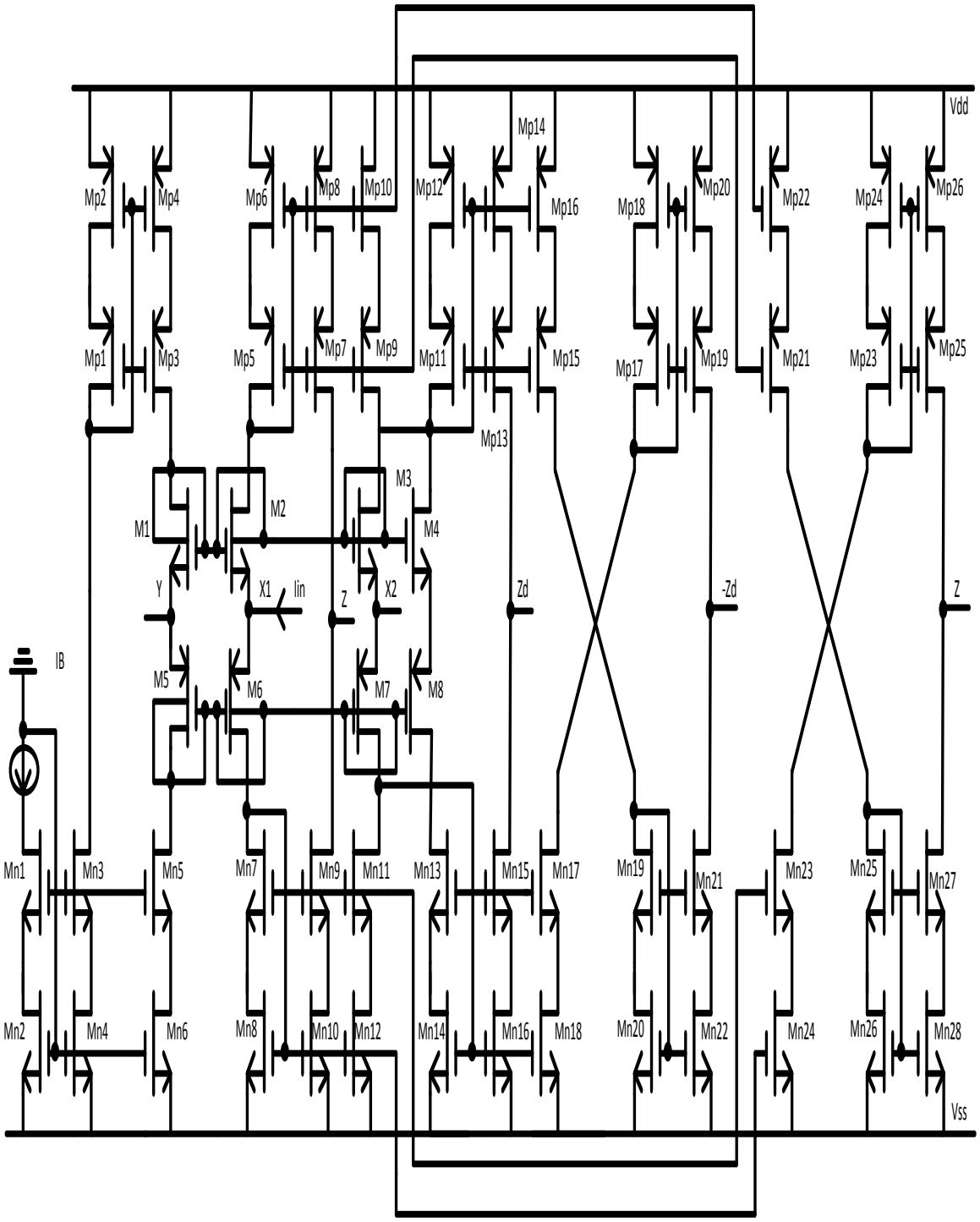


Fig. 3.1 Proposed DTMOS CCCDCC circuit design

3.2 Application of proposed DTMOS CCCDCC as low pass and high pass filters

Fig. 3.2 indicates a HPF and LPF current mode filter that is used to validate the proposed DTMOS CCCDCC. It consists of just one capacitor and one CCCDCC and hence is a very simple topology. The transfer characteristic of HPF and LPF are given in (3.2) and (3.3) respectively.

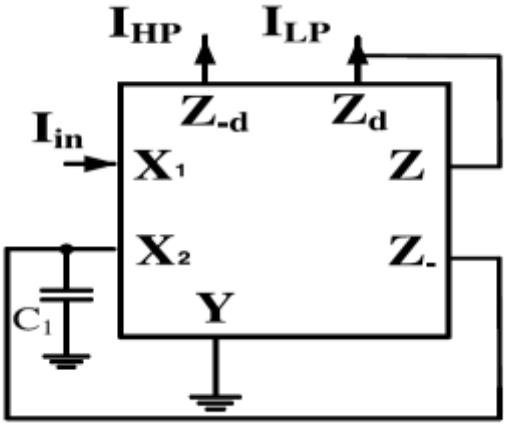


Fig. 3.2 LP and HP filters using one DTMOS CCCDCC [44]

$$I_{HP} = \frac{sR_{X2}C_1I_{in}}{sR_{X2}C_1+1} \tag{3.2}$$

$$I_{LP} = \frac{I_{in}}{sR_{X2}C_1+1} \tag{3.3}$$

The natural frequency ω_c can be expressed as:

$$\omega_c = \frac{1}{R_{X2}C_1} \tag{3.4}$$

CHAPTER 4

SIMULATION RESULTS

The simulations of the conventional CCCDCC, DTMOS CCCDCC and current mode filters have been done in PSPICE using 0.18μm TSMC technology.

4.1 Proposed CCCDCC using DTMOS technique

Simulations have been performed at ±0.3V, keeping I_B at 30uA.

4.1.1. Characteristic of DTMOS based CCCDCC

Following figure shows the DC current characteristic of DTMOS based CCCDCC.

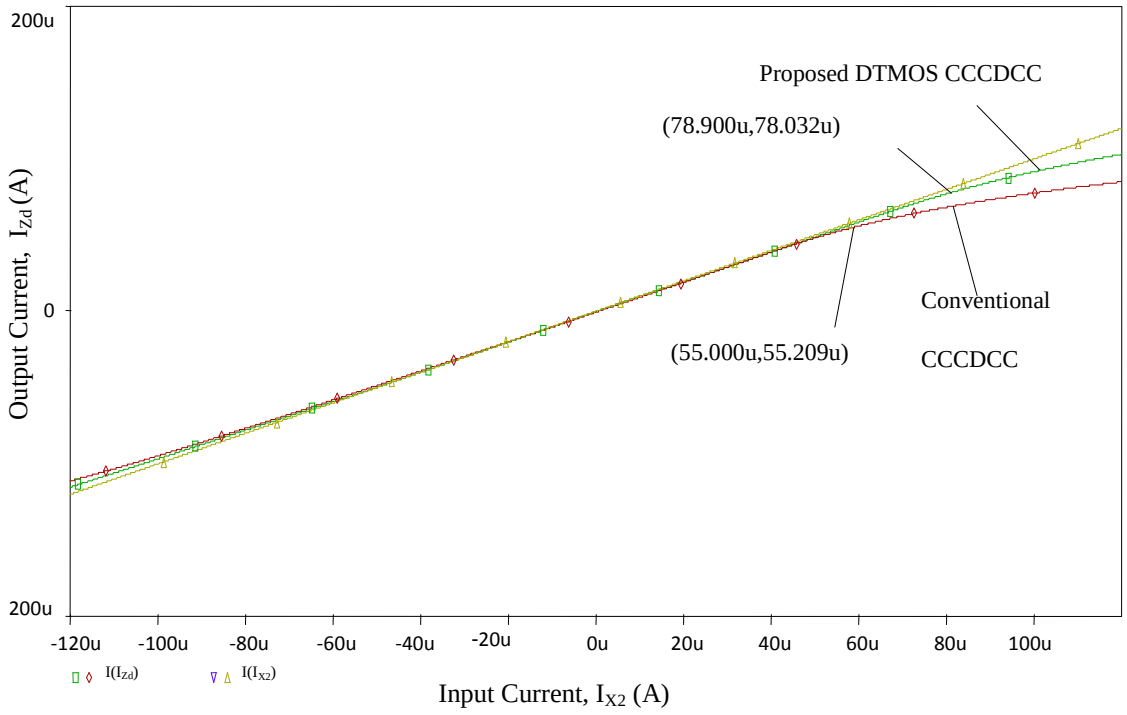


Fig. 4.1 Proposed DTMOS CCCDCC and conventional CCCDCC current characteristic

It can be seen from Fig. 4.1 that I_{Zd} follows I_{X2} till 78.9uA in the proposed DTMOS CCCDCC and 55uA in conventional CCCDCC. Thus, the current linearity of DTMOS CCCDCC increases up to 1.434 times which is 43.4% higher than the conventional CCCDCC circuit.

The simulation in Fig. 4.2 depicts that the linear range of current I_{-zd} in conventional CCCDCC is 39.355uA and 50.194uA in DTMOS CCCDCC. The linear range is enhanced by 27.54%.

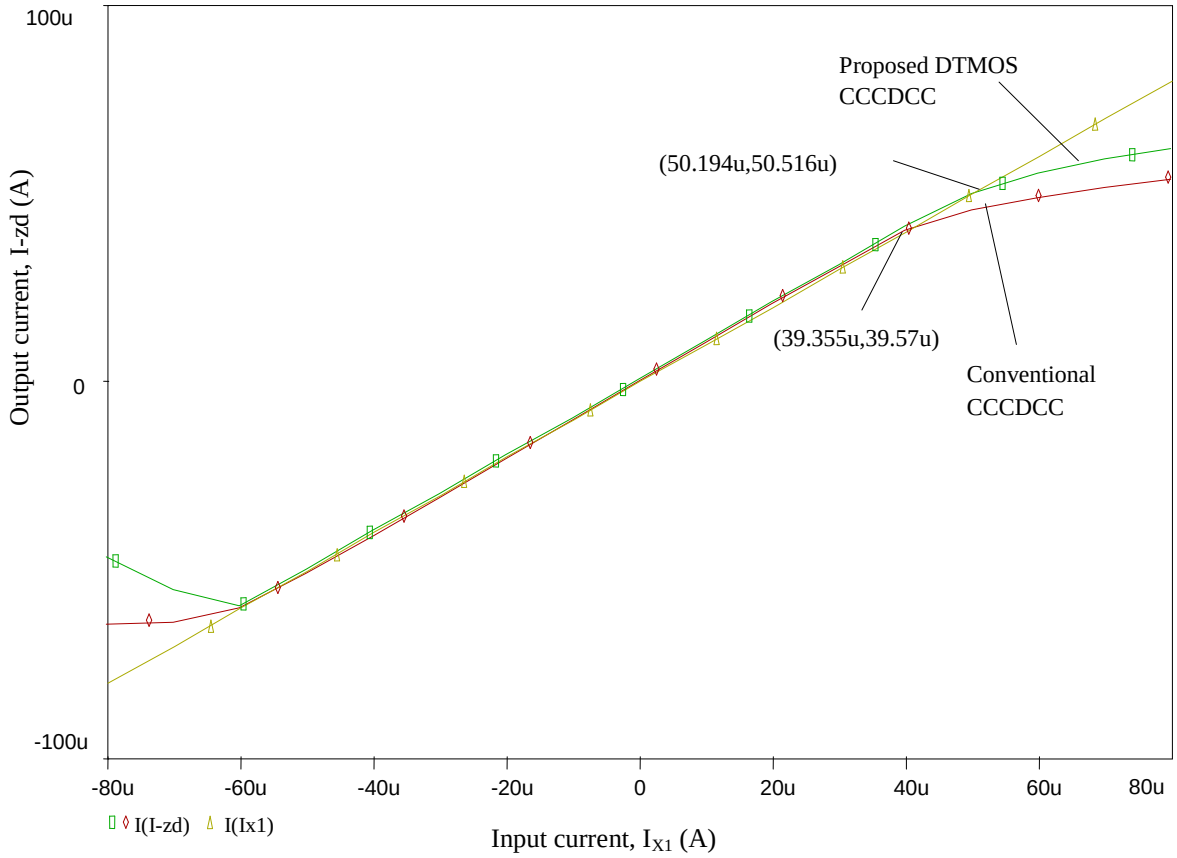


Fig. 4.2 DC curve of I_{-zd} versus I_{X1} between proposed DTMOS CCCDCC and conventional CCCDCC

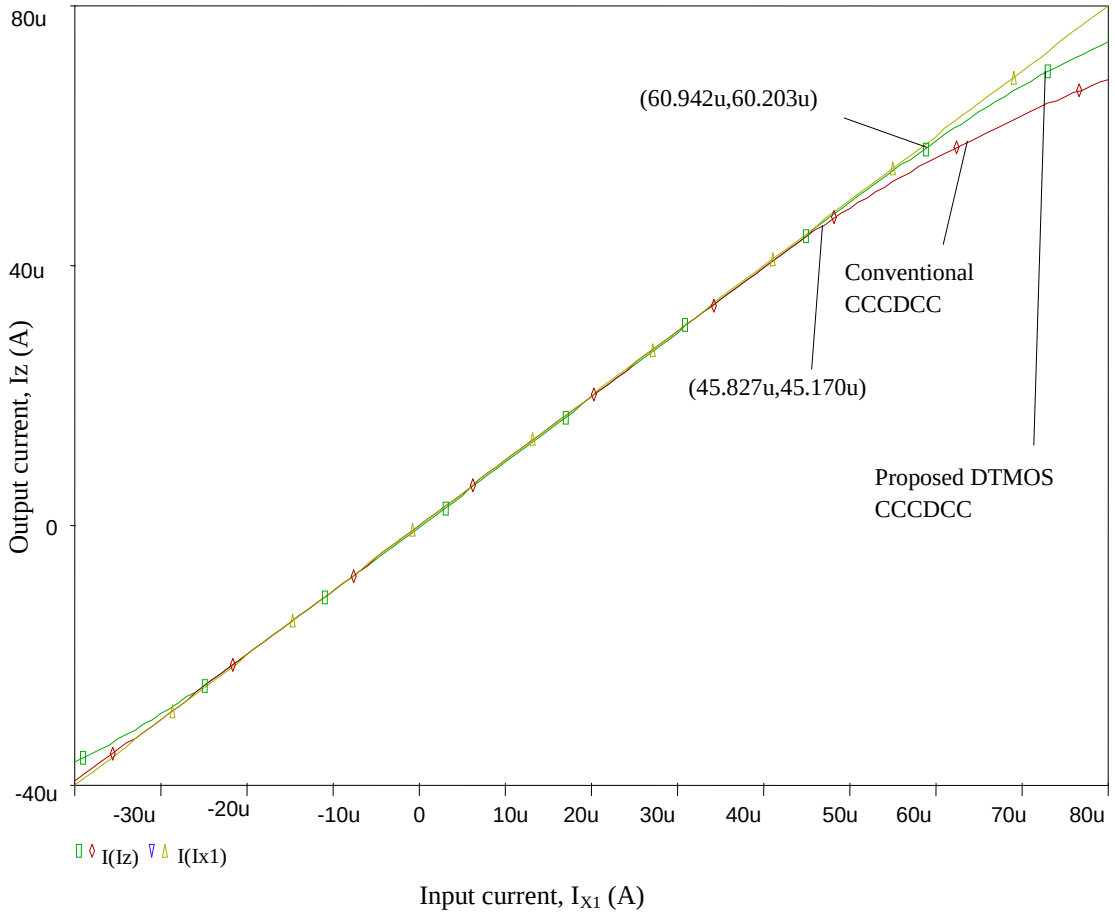


Fig. 4.3 DC curve of I_{-z} versus I_{X1} between proposed DTMOS CCCDCC and conventional CCCDCC

A comparison of DC curve of I_{-z} versus I_{X1} between proposed DTMOS CCCDCC and conventional CCCDCC is presented in Fig. 4.3. It can be analyzed that the Iz current imitate the current I_{X1} up to 60.942uA in the proposed DTMOS CCCDCC and 45.827uA in conventional CCCDCC. Therefore, there is an enhancement of linearity of Iz current by 32.98 %.

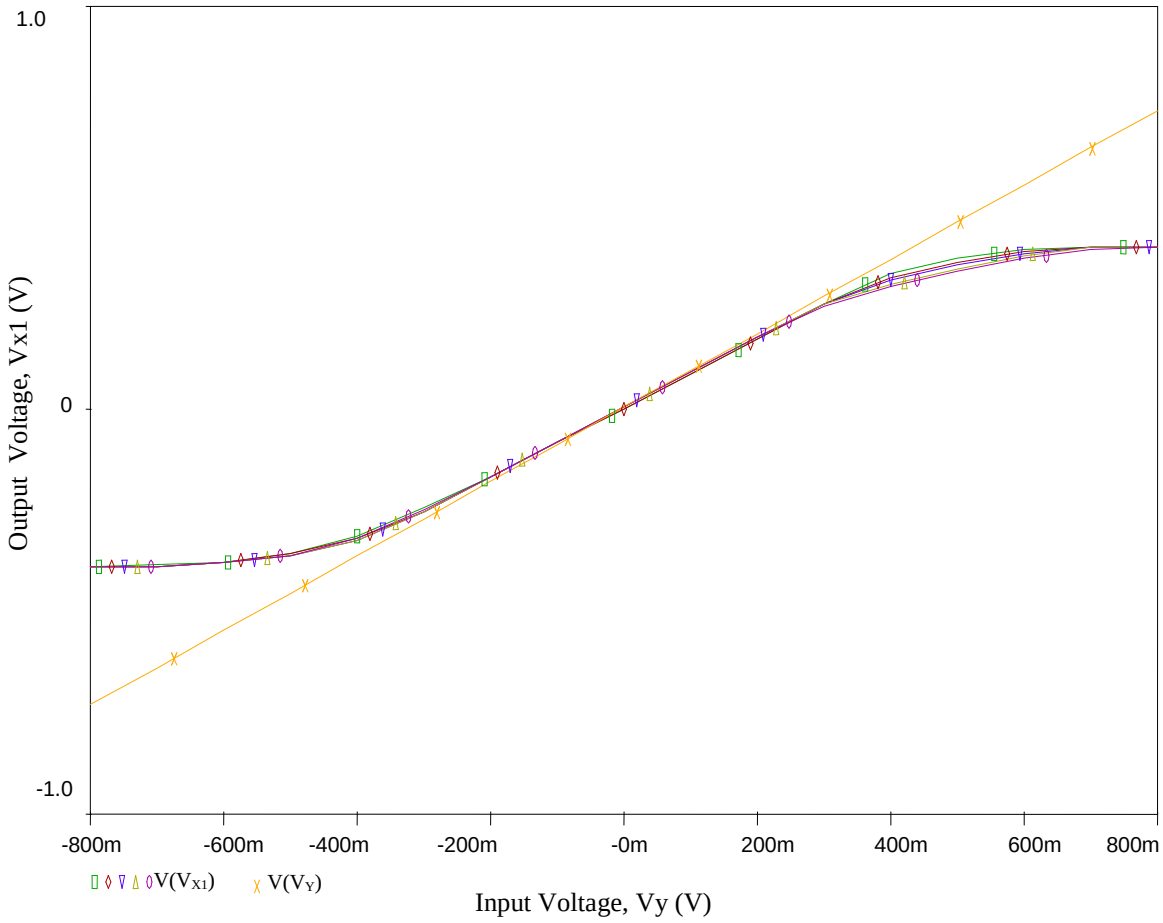


Fig. 4.4 DC characteristics of V_{X1} versus V_Y for various value of I_B

A DC voltage characteristic of V_{X1} versus V_Y for various value of I_B has been compared between DTMOS CCCDCC and conventional CCCDCC. I_B has been changed from 20uA to 40uA and its corresponding result has been plotted in Fig. 4.4. The voltage V_{X1} is approximately linear in the region -200mV to + 200mV.

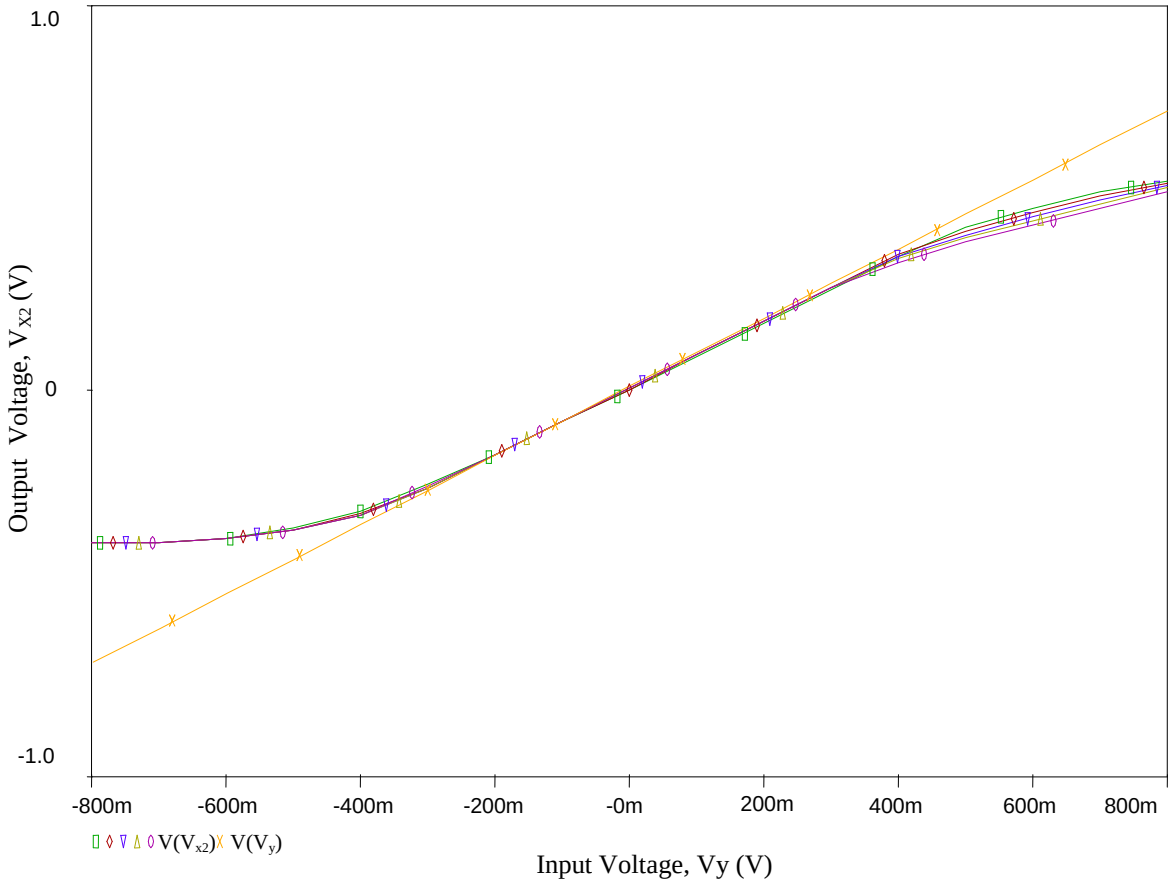


Fig. 4.5 DC curve of V_{X2} versus V_Y for various value of I_B

Fig. 4.5 depicts the DC characteristics of voltage V_{X2} versus V_Y by varying I_B from 20uA to 40uA. For the various value of bias current (I_B), voltage V_{X1} is approximately linear from -200mV to + 200mV.

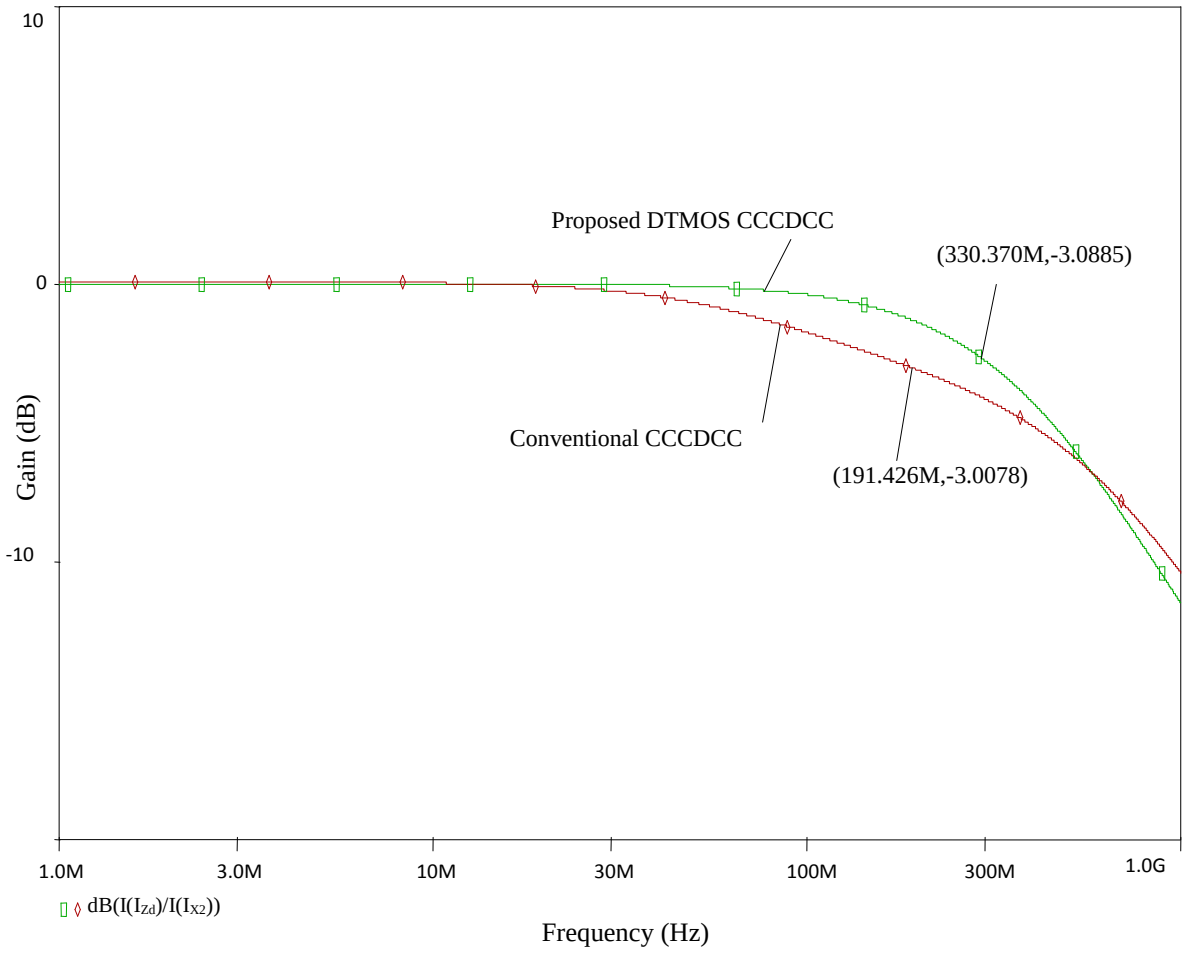


Fig. 4.6 Frequency response for current gain (I_{Zd}/I_{X2}) of proposed DTMOS CCCDCC and conventional CCCDCC

The frequency response for current gain (I_{Zd}/I_{X2}) of proposed DTMOS CCCDCC and conventional CCCDCC are presented in Fig. 4.6, which results in enhancement of -3dB bandwidth to 330.370 MHz from 191.426 MHz. Therefore, it is depicted that there is an increased in the -3dB bandwidth of proposed CCCDCC by 1.7258 times which is 72.58% higher than the conventional circuit design.

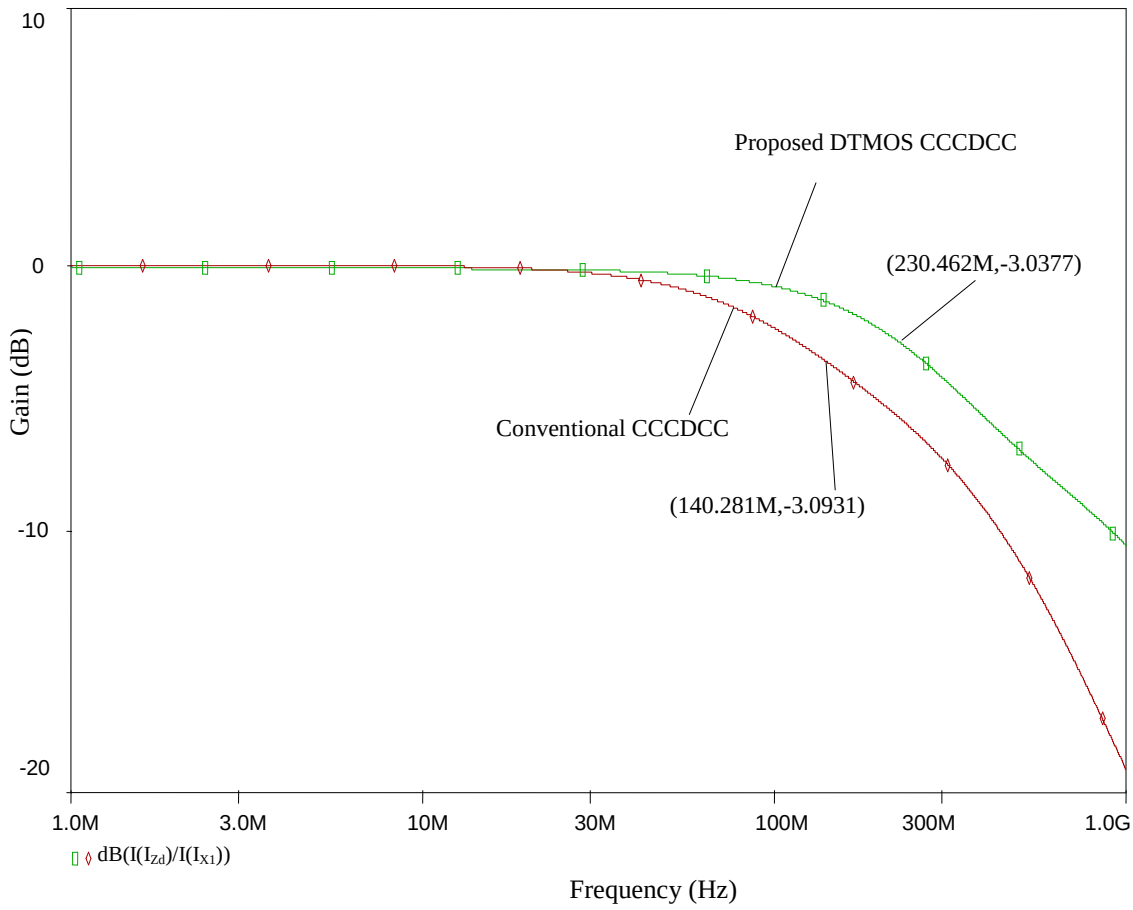


Fig. 4.7 AC characteristic for current gain (I_{Zd}/I_{X1}) of proposed DTMOS CCCDCC and conventional CCCDCC

In Fig. 4.7, a comparison of AC characteristic for the current gain (I_{Zd}/I_{X1}) between proposed DTMOS CCCDCC and conventional CCCDCC has been plotted. The -3dB bandwidth of proposed DTMOS CCCDCC is 230.462 MHz whereas -3dB bandwidth of conventional CCCDCC is 140.28 MHz. Clearly, the bandwidth is improved by 64.28% from the conventional circuit design.

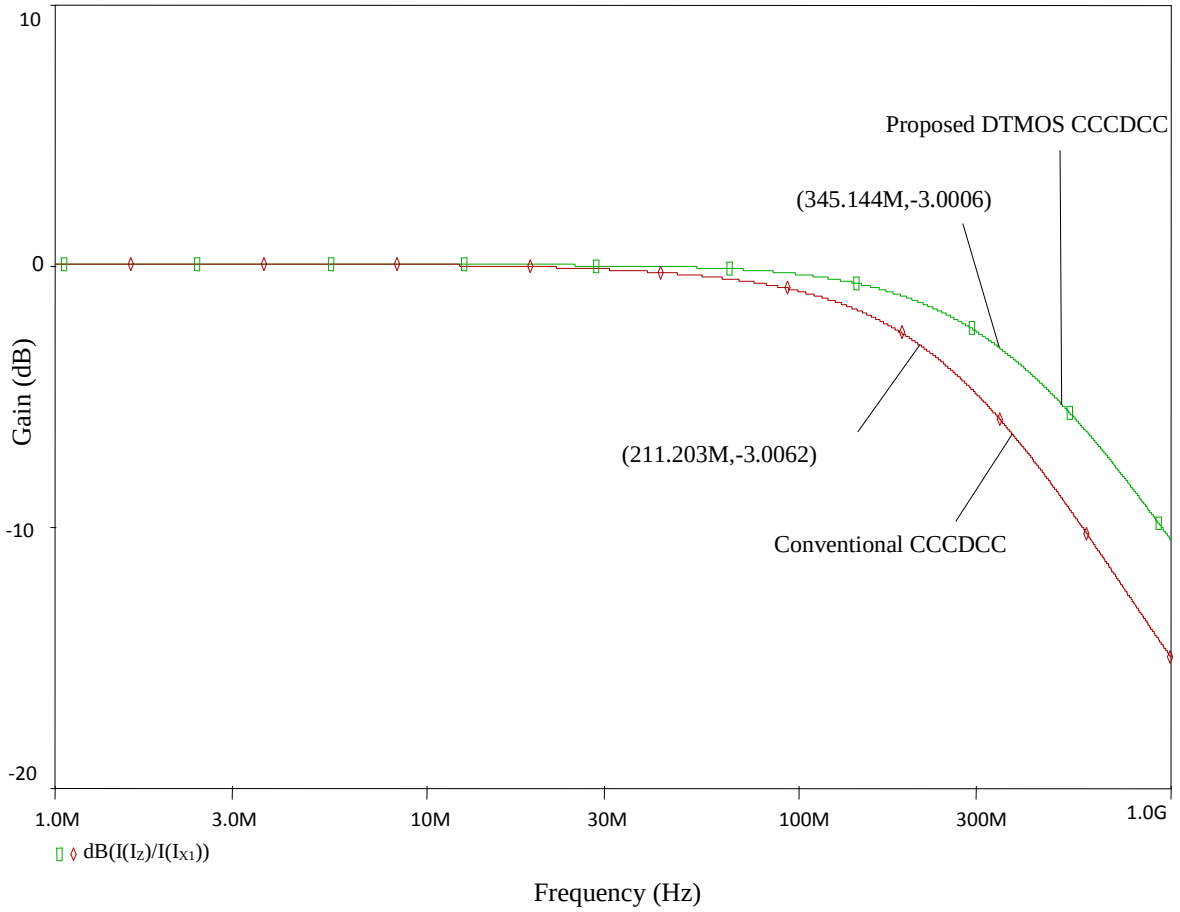


Fig. 4.8 AC characteristic for current gain (I_Z/I_{X1}) of proposed DTMOS CCCDCC and conventional CCCDCC

The frequency response for current gain (I_Z/I_{X1}) of proposed DTMOS CCCDCC and conventional CCCDCC are shown in Fig. 4.8. The graph indicates an enhancement of -3dB bandwidth to 345.144 MHz (proposed DTMOS CCCDCC) from 211.203 MHz (conventional CCCDCC) which improves it by 1.6341 times which is 63.41% higher than the conventional circuit design.

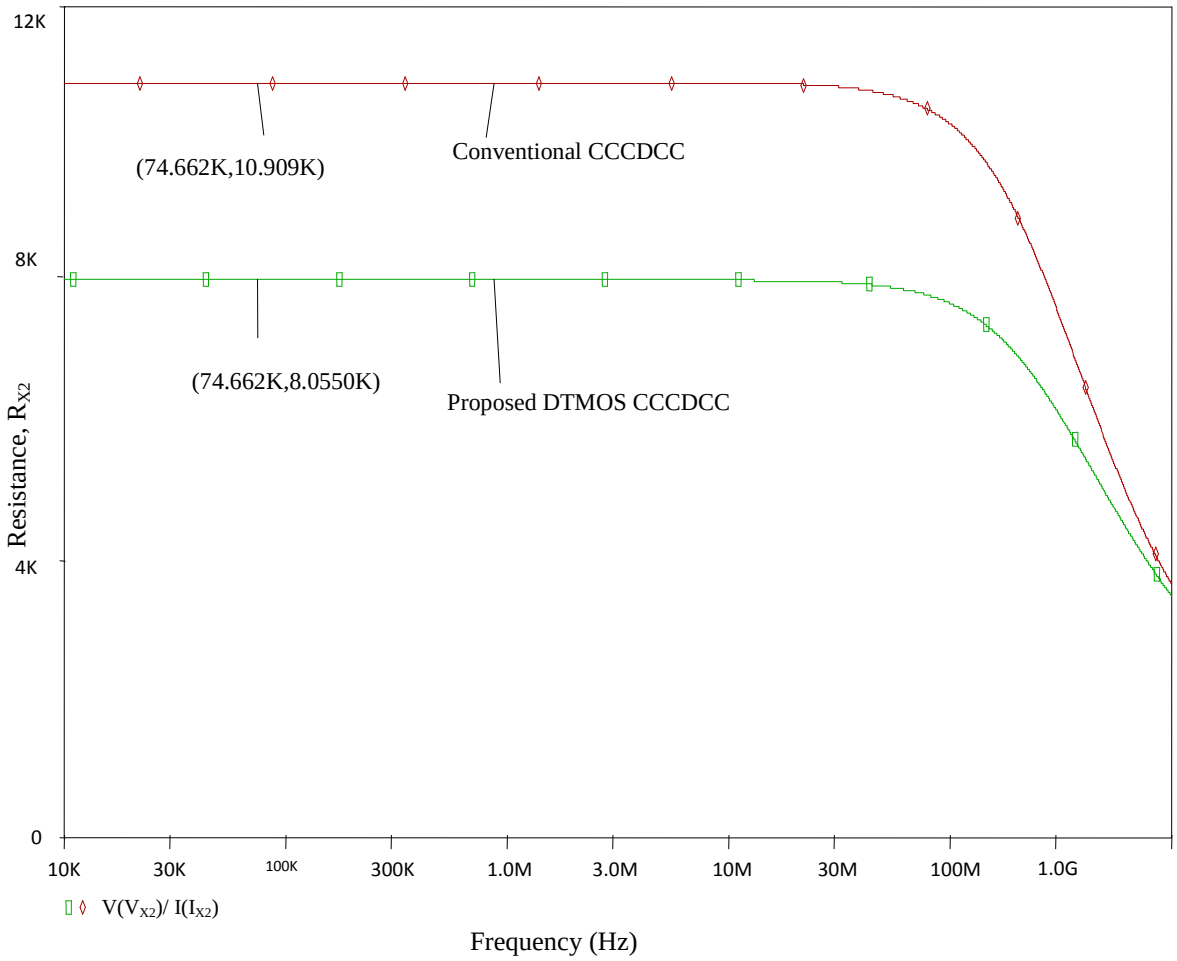


Fig. 4.9 AC characteristic for R_{X2} of proposed DTMOS CCCDCC and conventional CCCDCC

Fig. 4.9 represents the frequency response for parasitic resistance (R_{X2}) of proposed DTMOS CCCDCC and conventional CCCDCC. Parasitic resistance decreases from 10.909 kΩ (conventional CCCDCC) to 8.0550 kΩ (DTMOS CCCDCC). It is decreased by 26.16%. Hence, it is helpful for bandwidth extension in the high pass and low pass filters.

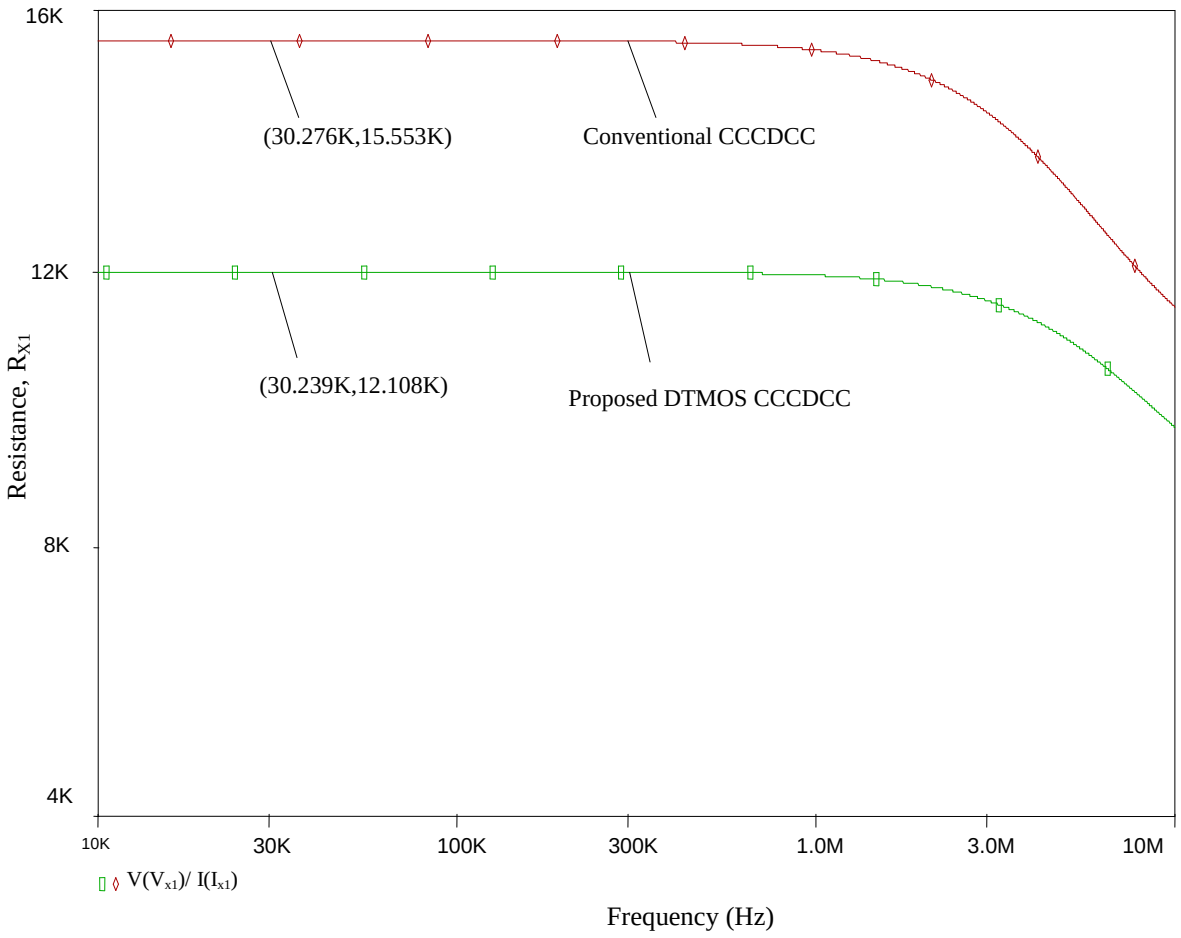


Fig. 4.10 AC characteristic for R_{X1} of proposed DTMOS CCCDCC and conventional CCCDCC

A comparison of the frequency response of R_{X1} parasitic resistance between conventional CCCDCC and proposed DTMOS CCCDCC is presented in Fig. 4.10. The value of R_{X1} in DTMOS CCCDCC is reduced to 12.108 kΩ from 15.553 kΩ of conventional CCCDCC.

Table 4.1 provides the quantitative comparison analysis of conventional CCCDCC with proposed DTMOS CCCDCC and other CCCDCC. The comparison of different parameters like technology, voltage supply, bias current, power consumption, -3dB bandwidth and resistance at port X_2 have been performed.

Table 4.1 Comparison Table

Parameters		**[42]**	**[41]**	**CCCDCC [44]**	**Proposed Circuit**
Technology(um)		0.35	0.25	0.18	0.18
Voltage supply		±1.5V	±1.25	±0.3V	±0.3V
Bias current I_B (uA)		100	100	30	30
Power consumption (mW)		1.48	2.75	0.0375	0.0363
-3dB Bandwidth (GHz)	(I_{Zd}/I_{X2})	0.311	1.1	0.19142	0.33037
	(I_{Zd}/I_{X1})	0.282	1.08	0.140	0.230
	(I_Z/I_{X1})	-	0.648	0.21120	0.34514
R_{X2} (Ω) at I_B		999.01K	437.020K	10.909 K	8.0550 K

The aspect ratio of transistors used in the circuit is provided in Table 4.2.

TABLE 4.2 Aspect Ratio

Transistors	**Aspect Ratio (W/L in um)**
M1-M4	10/0.18
M5-M8	4.14/0.18
Mn1-Mn6	4.05/0.18
Mn7 -Mn28	4.14/0.18
Mp1-Mp4	8/0.18
Mp5-Mp26	10/0.18

4.2 Application as low pass and high pass filters using DTMOS CCCDCC

The simulation of the conventional CCCDCC, DTMOS CCCDCC and first order filters have been done in PSPICE using 0.18μm CMOS technology. Simulations have been performed at ±0.3V, keeping I_B at 30uA with a capacitor value of 30pF.

Low pass filter (LPF)

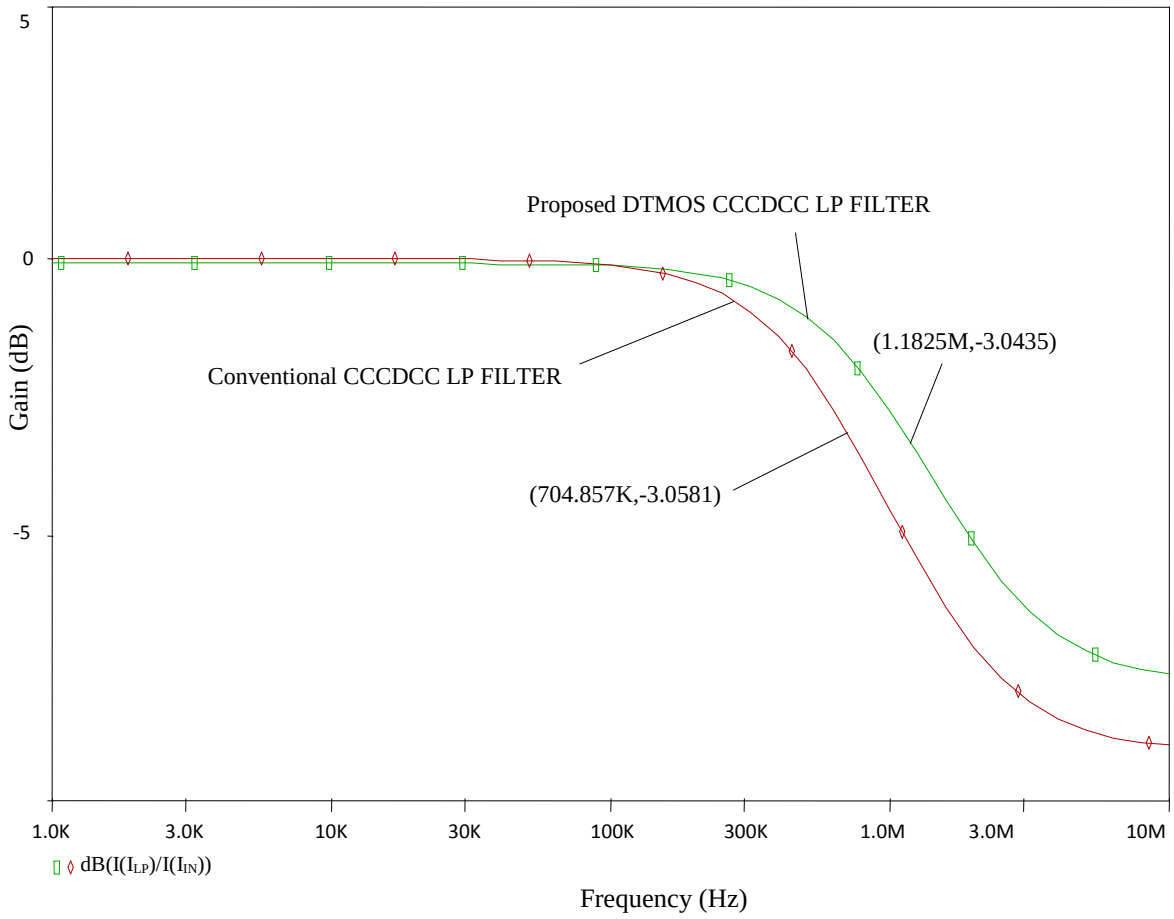


Fig. 4.11 Proposed DTMOS CCCDCC and conventional CCCDCC low pass filter

The frequency response indicated in Fig. 4.11 for low pass filter (proposed DTMOS CCCDCC) whose bandwidth is improved to 1.1825 MHz from 0.7048 MHz (conventional CCCDCC low pass filter). DTMOS technique enhanced the bandwidth by 1.678 times which is 67.78% higher than the conventional circuit design.

High pass filter (HPF)

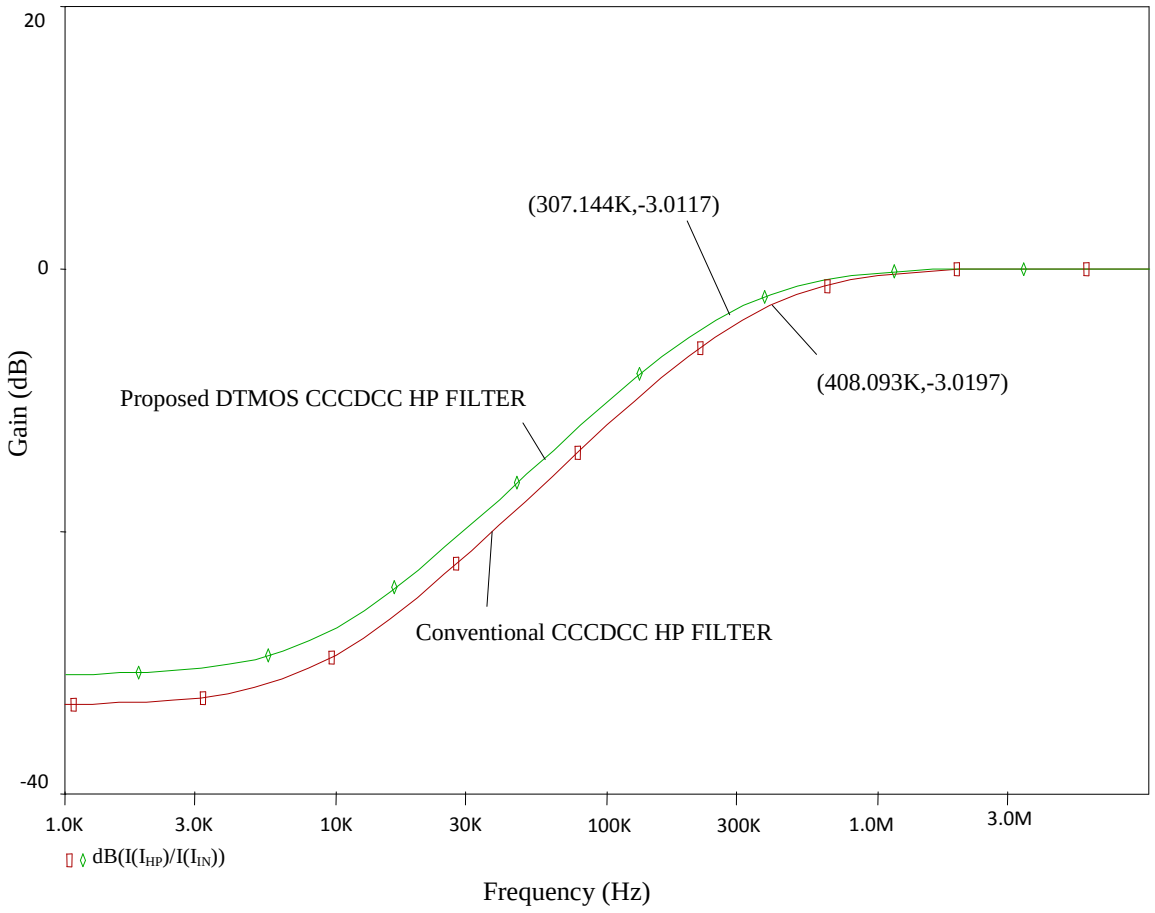


Fig. 4.12 Proposed DTMOS CCCDCC and conventional CCCDCC high pass filter

As illustrated in high pass filter frequency response (Fig. 4.12), the lower cut-off frequency (proposed DTMOS CCCDCC) decreases to 0.307 MHz from conventional CCCDCC high pass filter (0.408 MHz) and thus enhances the bandwidth. Bandwidth is increased from the conventional circuit design using DTMOS technique by 1.329 times which is 32.9% higher.

Table 4.3 demonstrates the comparison between the bandwidth of proposed DTMOS CCCDCC filters and conventional CCCDCC filters with the percentage of improvement.

Table 4.3 Comparisons between proposed DTMOS CCCDCC and conventional CCCDCC filters

S.No.	Filters	Bandwidth(Hz)		Improvement
		Conventional CCCDCC filter	Proposed DTMOS CCCDCC filter	
1	Low pass	0.7048 MHz	1.1825 MHz	1.678 times (67.78%)
2	High pass	0.307 MHz	0.408 MHz	1.329 times (32.9%)

CHAPTER 5

CONCLUSIONS & FUTURE SCOPE

- In this thesis, Dynamic threshold (DTMOS) has been successfully implemented on current controlled current differential current conveyor (CCCDCC).

- A comparison study has been done on conventional CCCDCC and proposed DTMOS CCCDCC and implemented it on first order filters.

- The linearity of various DC current characteristics in the proposed circuit has been increased from 32.98% to 43.4%. The bandwidth of various current gains also increases by approximately 63.41% to 72.58%. The linear range of DC voltage characteristics of proposed circuit, obtained by varying bias current are $\pm$ 200mV for V_{X1} and $\pm$200mV for V_{X2}.

- The parasitic resistance R_{X1} reduces by 28.45% and R_{X2} by 26.16 % as explained in chapter 3. DTMOS based CCCDCC is successfully employed in LP and HP current mode filters application which enhances the bandwidth by 67.78% and 32.9% respectively.

- A DTMOS CCCDCC circuit has been proposed demonstrating its advantage of higher transconductance, linearity, bandwidth and reduced power consumption. The proposed design is useful for low power applications as it uses ±0.3V of supply voltage.

- In the future, DTMOS technique can be used to design other circuits to enhance their properties which will also be suitable for low power applications. Further, the proposed circuit of DTMOS CCCDCC can be used to make other applications like integrator, amplifier, multiplier, oscillators, inductor etc. to improve their characteristic and make suitable for low power applications.

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PUBLICATIONS FROM THE WORK

The following publication is based on the low power DTMOS based CCCDCC. Simulations have been performed using PSPICE, 0.18µm CMOS technology.

Bharti and Anurag Chauhan, "A novel DTMOS based CCCDCC with current mode filters" IEEE- 1st International Conference on Signal Processing, VLSI and Communication Engineering (ICSPVCE-2019), Delhi Technological University, March 28 - 30, 2019. **(Accepted)**