M. Tech (VLSI)

ABHISHEK SHARMA

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SINGLE CAPACITOR SIMULATION OF FLOATING INDUCTORS USING VOLTAGE DIFFERENCING INVERTING BUFFERED AMPLIFIER

A DISSERTATION REPORT

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE AWARD OF THE DEGREE
OF

MASTER OF TECHNOLOGY
IN
VLSI AND EMBEDDED SYSTEMS

Submitted by:

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2K17/VLS/01

Under the supervision of

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JULY, 2019

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CANDIDATE'S DECLARATION

I, **ABHISHEK SHARMA**, **2K17/VLS/01** student of M.Tech (VLSI), hereby declare that the Dissertation report titled "**Single Capacitor Simulation of Floating Inductors Using Voltage Differencing Inverting Buffered Amplifier**" which is submitted by me to the Department of Electronics and Communication, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

Place: Delhi **ABHISHEK SHARMA**

Date:

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CERTIFICATE

I hereby certify that the Dissertation report titled "**Single Capacitor Simulation of Floating Inductors Using Voltage Differencing Inverting Buffered Amplifier**" which is submitted by **ABHISHEK SHARMA**, **2K17/VLS/01** [ECE Department], Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ABSTRACT

Two new simple structures for the simulation of floating lossy inductance have been proposed which realize series and parallel RL impedances employing two voltage differencing inverting buffered amplifiers (VDIBAs) as active components. The presented circuit topologies use canonical number of passive components (one resistor and one capacitor). The simulated inductor can be tuned electronically by means of transconductance of VDIBA in case of floating parallel RL structures while the inductance can be controlled through a resistance in case of series RL. The performance of the proposed configuration has been verified through SPICE simulation using TSMC 0.25um CMOS Technology.

ACKNOWLEDGEMENT

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ABHISHEK SHARMA

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LIST OF SYMBOLS, ABBREVIATIONS

CC	Current conveyors
CCCDTA	Current Controlled Current Differencing Transconductance Amplifer
CDBA	Current Differencing Buffered Amplifier
CDTA	Current differencing transconductance amplifiers
CFOA	Current feedback operational amplifiers
CCTA	Current Conveyor Transconductance Amplifier
CDDITA	Current Differencing Differential Input Transconductance Amplifier
CMOS	Complementary Metal Oxide Semiconductor
DVCCTA	Differential Voltage Current Conveyor Transconductance Amplifier
DV-OPAMP	Differential Voltage Operational Amplifier
DVCCII	Differential Voltage Current Conveyor Second Generation
DDCC	Differential Difference Current Conveyor
DVCC	Differential Voltage Current Conveyor
FDNR	Frequency Dependent Negative Resistor
LPF	Low Pass Filter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
OP-AMP	Operational amplifiers
OTA	Operational Transconductance Amplifier
OMA	Operational Mirrored Amplifier
VDTA	Voltage Difference Transconductance Amplifier
VDBA	Voltage Differencing Buffered Amplifier
VDIBA	Voltage differencing inverting buffered amplifier

CHAPTER 1

INTRODUCTION

The demand for various specifications such as small supply voltages, low dynamic power consumption, extreme speed, accuracy, compact size etc. is crucial in electronic circuits for progress of electronic technologies. Simultaneous fulfillment of all the above requirements is problematic without any tradeoffs. Thus, in order to fulfill all the demands, electronic circuits have grown and has provided ease to the circuit manufacturers in past few decades.

Inductor, one of the most widely used passive devices is one of them, which keeps on evolving depending upon the requirements of the circuit manufacturers. The inductor's applications can be found in various fields such as communications, electronics and measurements. Spiral inductor can be fabricated in integrated circuits. In spite of that, passive inductors fabricated on silicon wafer have certain limitations such as occupying excess area of chip and non-variable inductor values. Even though spiral inductors can be actualized in integrated circuits, they still have few limitations like having excess size and weight, formation of unwanted harmonics, pickings and radiating the electromagnetic waves, etc. Thus, passive inductors are being replaced by active inductance simulators where active elements are used along with passive components such as R, C to realize inductors.

Thus, in recent times, simulation of inductors using active devices (grounded and floating) has been a prominent exploration area because of their utilization in linear (active filters and oscillators) and non-linear (chaotic oscillators) circuit designs as well as their advantages over passive inductors.

Chapter 2 basically deals with the literature review highlighting the active inductance simulations employing various design techniques published in last three decades [5-51].

Floating inductance simulation configurations using various active elements like operational amplifiers (Op-amp) [52], current conveyors (CC) [53, 53], current differencing transconductance amplifiers (CDTA) [53] and current feedback amplifiers (CFA) [61] have been presented in the literature but unfortunately these reported configurations suffers from one of the corresponding downsides:

- Intemperate use of the active components (more than two) [52, 53,54,61]
- Intemperate use of the passive components (more than two) [52, 53]
- Lack of electronic controllability [58].

In order to realize the Inductor in an integrated circuit, the attention here is focused Voltage Differencing Inverting Buffered Amplifier (VDIBA), whose detailed analysis has been covered in Chapter 2 and 3.

Voltage differencing inverting buffered amplifier (VDIBA), recently introduced, is valuable active block being used across many analog signal processing and signal generation applications [60]. VDIBA is developed from the previously generated active element current differencing buffered amplifier (CDBA) [62, 63], where corresponding current difference at the input terminals of CDBA is now replaced with the voltage difference. Thus, in various voltage mode applications, circuits using VDIBA as active element have the advantage of not requiring any external passive resistors for voltage to current conversion unlike traditional CDBA circuit [64].

Also, it has the following feature that through DC bias current, VDIBA's transconductance value can be tuned electronically. When contrasted with various transconductance based active elements, like differential voltage current conveyor transconductance amplifier (DVCCTA), current conveyor transconductance amplifier

(CCTA) etc., VDIBA offers low impedance at its output terminals which makes it handy to be used in voltage-mode applications, as the loading effect is fully removed [60].

Thus, the main purpose of this dissertation is to present two simple lossy floating inductance simulator circuits with specified advantageous features:

- Low active and passive elements requirement (two VDIBA's, one capacitor and resistor).
- Electronic Tunability.
- No passive element matching constraint.

CHAPTER 2

LITERATURE SURVEY

During mid-1940, every year there was a new electronic device in the market which tried to dominate the market share of the earlier discovered products. At that time, the devices were being made with the knowledge of market value of that product which is been happening till now but now the manufacturer also take care of the other important/necessary factors like the ease of usage, environmental factors, size, weight etc.

One of the most important inventions which brought the boost in the electronics field was the invention of OPAMP in 1941 which was vacuum tube based. During early 40's to early 60's many new modifications came on the vacuum tube op-amp either it was on the type of the manufacturing technique or on some better properties than the earlier one. But the remarkable invention which caught the attention of every electronic circuit's designer was the monolithic op-amp which was small and easy to use with the remarkable property of decreased price. In the early 60's inductor size and cost was one of the most important problems. Thus, in order to overcome these problems many research papers were presented.

2.1 Overview on Inductor Simulators

In the mid 60's, an attempt was made to make an inductor with a single differential input op-amp (DV-op-amp) with few passive components (Resistance and Capacitance) [5]. In this paper, distinct amplifiers were being used for carrying out capacitance transformation into equivalent coil being termed as positive-immittance inversion and cancelling out the equivalent coil losses also known as negative-immittance

conversion. In this paper a single differential input op-amp was being used to manufacture an inductor.

In the same year another paper was published which also used the (DV op-amp) but its performance was better that the earlier one in terms of Quality factor which appeared to be limited primarily by the losses in the capacitors used [6]. Then in early 70's an attempt was made to fabricate a grounded inductor using unity gain op-amp along with few passive components [7]. In the year 1970, first attempt was made to manufacture an inductor using Gyrator which resulted in some new circuits for inductor fabrication [8]. In the next year op-amp based negative impedance converter was used to fabricate the inductor [9]. In the mid 70's, a lossy inductance was fabricated employing two amplifiers with passive resistances[10], the circuits described in this paper were much more sensitive than the earlier circuits which were presented. In the same year, lossy floating active RC realization of an inductor was published. Two operational amplifiers were used each in the unity gain configuration along with two passive capacitors and three resistors. [11], the fundamental advantages of the corresponding inductor design was unity gain, less component counts, easy value modifications, low sensitivities and stable configuration.

In the early 80's, resistance-controlled inductor circuits were fabricated. In this, a single grounded capacitor based lossless floating inductance circuit was realized employing three operational amplifiers. Operational amplifiers were used as unity gain summers along with three external resistors [12]. The inductor circuits obtained using RC circuits had remarkable sensitivity properties which lead to the realization of new op-amp based second order driving point impedances along with the smallest possible count of R, C passive elements [13]. During early 90's op-amp based grounded inductor was made which is very easy to understand and is based on general techniques presented in the corresponding paper [14].

During mid-95, a new floating impedance configuration based on operational mirrored amplifier (OMA) was published which required only three OMAs while keeping all previously discussed advantageous features [15]. In the year 2005, a

current conveyor based inductor circuits were also presented while maintaining all previously presented advantageous features [16]. In the year 2008, using modified current-feedback operational amplifiers (MCFOAs), a new grounded and floating inductance simulation circuit was presented which required minimum number of passive components [17].

During early 60's when the first monolithic design of op-amp was presented at the same time operational transconductance amplifiers (OTA) were also fabricated with control input as a current and with differential inputs like operational amplifiers without containing not a single passive resistor unlike in op-amps. The working of an OTA is primarily based on the working of current mirrors. Since the OTA's are originated from OPAMP hence the OTA based inductor model are not that mush old.

In the mid 2005 a paper was presented which employs two OTRA based grounded parallel immittance (combination of inductance and admittance) simulator topology which requires fewer passive components counts than others presented earlier in literature. The other key reason to use OTRA was the grounding of input terminals because of which most of the parasitic capacitances and resistances effects disappear [18]. During the same time another paper was published in which more passive equivalent circuit was developed which also included finite bandwidth effect and was comparable to active OTA based floating inductor [19].

In the same year, using Operational Transconductance Amplifiers (OTAs) as active elements, single grounded capacitor based floating inductance simulators (positive and negative) were introduced with advantageous feature of controlling the inductance values using the DC bias current. Moreover, inductor was simulated using 2 OTAs, no external resistor and no requirement of component matching conditions [20]. Then during mid-2007 a research paper was presented which primarily focused on the floating inductor simulation based on high performance structured OTA, requiring in total of 4 active OTA elements and this design being superior to previous 3-OTA based design [21].

After this, a paper proposed a novel graph based structured method for the realizing the active inductor simulation circuits. This technique consisted of first developing an inductor less flowgraph for the structure, whose transfer function corresponds to the inductor's impedance or an admittance, and developing a RC element proportionate circuit along with OTA controlled sources [22]. In the paper [20] four OTA based floating inductor was presented which was being reduced to one inductor based floating inductor having all the desirable properties of the earlier OTA based inductors [23].

Though, the use of OPAMP and OTA based inductor circuits have decreased the size of inductor circuits extensively, but in few cases, it is been required to use the inductor in the integrated circuits where the OPAMP and OTA based inductor circuit started showing constraints on minimizing the IC's size. Thus in order to overcome this issue complementary symmetry metal oxide semiconductor (CMOS) based inductor circuit started getting the popularity. In digital circuits, in any digital circuits, the word "complementary-symmetry" refers to use of n type and p type - complementary and symmetrical MOSFET transistors.

During mid 90's, a CMOS GIC based RF active inductor was described. The advantage of this CMOS based inductor to its counterparts was the reduction in the inductor losses by applying gain enhancement techniques based on cascoding. Moreover, the presented inductors had lower losses, high self-resonance frequency and wider inductive region [24]. After few years a new fully differential CMOS based floating inductor was realized. The main significance of shifting to active inductors design are decrease in chip area consumption by inductors and decrease in fabrication processing cost which would have occurred in fabrication of passive inductors, and extra feature of tunability where inductance values can be tuned [25].

In the year 2000 another paper was presented which tried to overcome some of the problems faced by earlier CMOS based designs. In that research, a new CMOS transistor based active inductor circuit relying on circuit configuration of VHF (Very High Frequency) was presented which allowed the circuit to have low power supply

voltages (< 2V) at very high frequency operation. For reducing inductor losses and achieving high Quality factor along with wide operating bandwidth, Gain enhancement techniques were applied [26]. After few years, surface micromachining technology designed and fabricated a highly suspended CMOS compatible spiral inductors on standard silicon substrate (1-30Ω-cm in resistivity. This CMOS compatible spiral inductor was capable of achieving Q factor of 70 at 6GHz frequency which is the highest Q factor ever reported on standard silicon substrate at this frequency [27]. In the same year, Current Controlled Current Differencing Transconductance Amplifier (CCCDTA) based grounded as well as floating inductance was simulated requiring only one active block.

The main advantage of this simulated inductance was the electronic controllability of inductance by tuning the dc current of corresponding active element. Floating and grounded Inductance simulator circuit comprised combination of 1 active CCCDTA block each, two to one voltage buffers and one grounded capacitor each respectively, as well as provided advantage for having no passive element matching conditions [28]. In 2010 CMOS technology based digitally controlled lossless floating inductor was fabricated using current conveyors along with array of resistor for providing digital tuning of inductance values. The Inductance value can be adjusted from 0.42763mH to 5.67mH [29].

In the same year, through the tapped-inductor feedback technique, a new Q-enhanced inductor was presented which helped in reducing resistive losses by minimizing the consumed power and also provided a large inductance value inductor in contrast with traditional transformer feedback architectures [30]. In the mid 2011 another paper was presented which proposed frequency dependent floating inductor (FI) simulation circuit using 2 CBTAs and 3 grounded passive components. Based on the component selection, this ci2rcuit can realize resistor, a floating FDNR, an inductor or a capacitor. Also, circuit provides a feature of no passive element matching requirements and provides better sensitivity performance in respect to tracking errors [31].

Recently, in early 2012 a grounded capacitor based floating inductance circuit employing 2 differential voltage second-generation current conveyors (DVCCIIs) operating at very low voltage levels (±0.75 V) was designed. The circuit did not need any component matching conditions [32].

During same time, current mode analog circuits getting popularity which led to invention of Current Conveyors. Observations are also made on current conveyor based inductors in the literature. In the early 70's improvised version of second current conveyor was presented which is used to form a function generator, gyrator, NIC, DVCCS/DVCVS etc. [33]. Then during early 80's a grounded inductance realization using the DVCCS/DVCVS as the active element was presented in which a single grounded capacitor was used to control the inductor magnitude [34]. Then during same time another paper was published for realizing inductance employing second generation CC-II current conveyor as the active element along with three passive components. The inductor realized was seen desirable for moderate applications [35] while in the other paper published, it was demonstrated that current conveyors based inductors can be simulated with minimum count of passive components, only 1 capacitor and 2-3 passive resistors [36]. During the same time a new lossy frequency independent floating inductance was realized employing one second generation CC-II current conveyor along with a one capacitor, and 2 resistors without need of any equality constraint [37]. In the same year it was shown that using CC-II active block and a single grounded capacitor, a grounded inductor can be realized.

The main feature of this was the automatic adjustment of Q factor and its immunity to changes in CC-II parameters which also made it appropriate for high quality applications [38]. After sometime, floating series and parallel RL impedance were demonstrated with CC-II as active element without any component matching requirements. The circuit also facilitated single resistor based automatic control of inductance value and low passive element count (R, C) [39]. During the same year, a new CC-II based lossless synthetic floating inductance circuit was proposed whose value was controllable through a single grounded resistor [40]. Next year three new active simulation circuits were published which realized floating lossless inductance and RL series/parallel impedances respectively using three and two CC-II as active blocks.

The published circuits had salient features such as no matching conditions in components, minimum possible count of passive elements (R, C) and resistance-controlled inductance values [41]. Then during early 80's a grounded inductor using single CC-II was proposed. The realization method is quite versatile and can produce a grounded impedance that may be bilinear RL, ideally inductive or inductive with a positive or negative resistive part either in series or in parallel [42]. During the end of the same year a paper was presented in which an ideal floating inductance was simulated. The main advantage of this work was that the floating inductance was tunable through a single resistor and it has been shown that it is possible to simulate these realizations with unmatched passive components [43]. During early 80's, grounded capacitor based floating lossless inductance simulation was published using a CCII as active element. [44]. Then during early 90's a lossless floating immittance using CCIIs was proposed.

The main advantage in that paper was that based on Nullator. Nullator technique various simulation circuits could be derived comprehensively [45]. During the mid-90's, various new second order current mode circuits were derived using current conveyors as basic elements. Then using these new circuits' inductors outputs were compared which were more reliable and close to the ideal characteristics of grounded inductor [46]. Thus an era had begun where changes in the CC-II were started observing which paved way for the third generation current conveyors (CC-III). During 2000 an actively simulated grounded lossy inductors using CC-III was proposed. Then during the mid2005, a new single capacitor based floating lossless inductor employing CCCII was presented. The circuit has electronic tunability as the inductor value could be adjusted through the biasing currents of the CCCIIs [47]. During 2006, two new CCCII based floating inductors were realized depending on passive components choices [48], with no constraint on component matching as its primary advantage.

During the mid of 2007, a new hybrid inductor was realized which employed hybrid consolidation of operational amplifiers and current conveyors. The circuit offered inductors with high Quality factor in contrast to traditional current conveyor circuits [49]. The other qualities of the hybrid device was that it can be utilized in many ways: (i) as a monodirectional floating inductor, (ii) as a grounded inductor, (iii) as a bidirectional

inductor. Bidirectional Inductor has utility that purely the count of active components is increased in contrast to monodirectional inductor circuits without expanding passive components count. Then in the year 2008 a paper was presented in which the inductor in been made using CC-II with improved performance even at low frequency [50]. In same year, a synthetic grounded lossless inductor using an active differential voltage current conveyor transconductance amplifier (DVCCTA) device with passive RC was developed. The advantage of this circuit is its insensitivity towards port mismatch errors over its counterparts and also no component matching constraint [51].

2.2 Overview of VDIBA

Several new active elements such as CDDITA, VDBA, VDTA etc. were introduced in [59] for the first time. The voltage differencing inverting buffered amplifier (VDIBA), updated from VDBA (presented in [60]), has been recently introduced as an active device for analog signal processing applications.

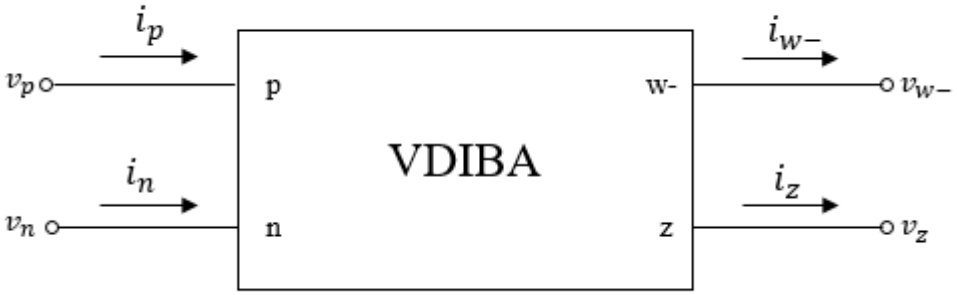

Fig. 2-1 Schematic Design of VDIBA

Voltage differencing inverting buffered amplifier (VDIBA) is a 4 terminal active block along with electronic tunability. The schematic symbolic representation and equivalent circuit of VDIBA are presented below in Fig. 2.1 and Fig. 2.2 distinctively [60]. From equivalent circuit model it can be inferred that VDIBA exhibits high-impedance at input terminals (in this dissertation labeled as p and n), high-impedance at z terminal, and low-impedance at w- terminal.

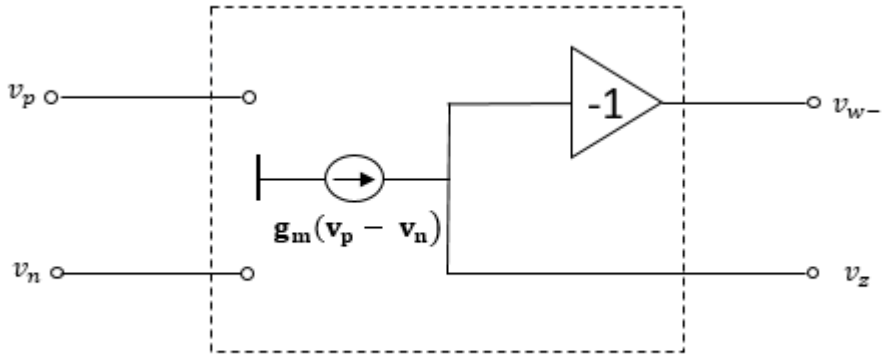

Fig. 2-2 Equivalent circuit of VDIBA

The input stage of VDIBA consists of an operational transconductance amplifier (OTA), which transforms the differential voltage at its input terminals to the output current that flows out from its z terminal. VDIBA's output is implemented by a unity gain inverted buffer. As both stages (OTA and unity gain inverted buffer) can be actualized by commercially available ICs (Integrated Circuits), VDIBA is suitable for electronically controllable circuit requisitions.

The terminal relationships between port currents and voltages of the VDIBA can be specified by the subsequent hybrid matrix:

$$\begin{bmatrix} \boldsymbol{i_p} \\ \boldsymbol{i_n} \\ \boldsymbol{i_z} \\ \boldsymbol{v_{w-}} \end{bmatrix} = \begin{bmatrix} \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \boldsymbol{g_m} & \boldsymbol{-g_m} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \boldsymbol{-\beta} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \boldsymbol{v_p} \\ \boldsymbol{v_n} \\ \boldsymbol{v_z} \\ \boldsymbol{v_{w-}} \end{bmatrix} \qquad (\mathbf{2.1})$$

Where g_m represents transconductance and β means non-ideal voltage gain of VDIBA. For an ideal VDIBA, the value of β is unity.

From Equation (2.1), it can be inferred that the differential voltage at input terminals i.e. $(v_p - v_n)$ of VDIBA is transformed into the output current flowing out from the z terminal and the voltage at z terminal is conveyed to w-port (inverted).

Generally, the transconductance is electrically adjustable by tuning the bias current in VDBIA [60].

2.3 VDIBA CMOS Implementation

A simple VDIBA CMOS implementation is presented below in Fig. 3.3 [63]

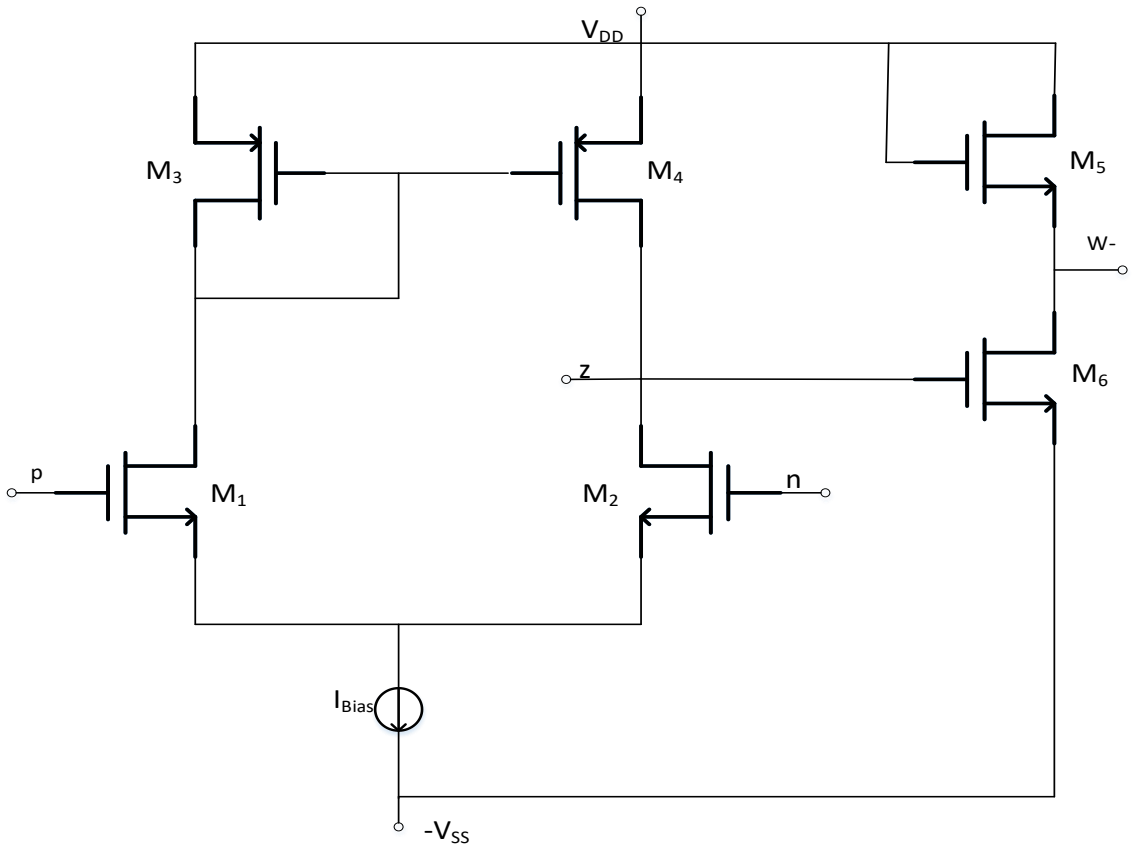

Fig. 2.3 CMOS implementation of VDIBA [60]

VDIBA consists of M1-M4 transistors as active loaded differential pair combined with unity gain inverting voltage buffer at the output stage (with M5 and M6 as matched transistors). Output stage can also be called a unity-gain common-source amplifier with diode-connected load (M5). VDD and VSS are the supply voltages provided to the circuit.

CHAPTER 3

THE PROPOSED LOSSY INDUCTOR CONFIGURATIONS

As stated in Chapter 1, Active simulation of Inductors offers various advantages over their passive counterpart. Here, single capacitor based inductor simulation using recently introduced active element VDIBA is being proposed which realizes lossy series and parallel inductances.

3.1 Proposed Floating Lossy Series Inductance Realization

The proposed tunable floating lossy series inductor employing voltage differencing inverted buffered amplifiers, along with one capacitor and resistor, is shown in Fig. 3.1.

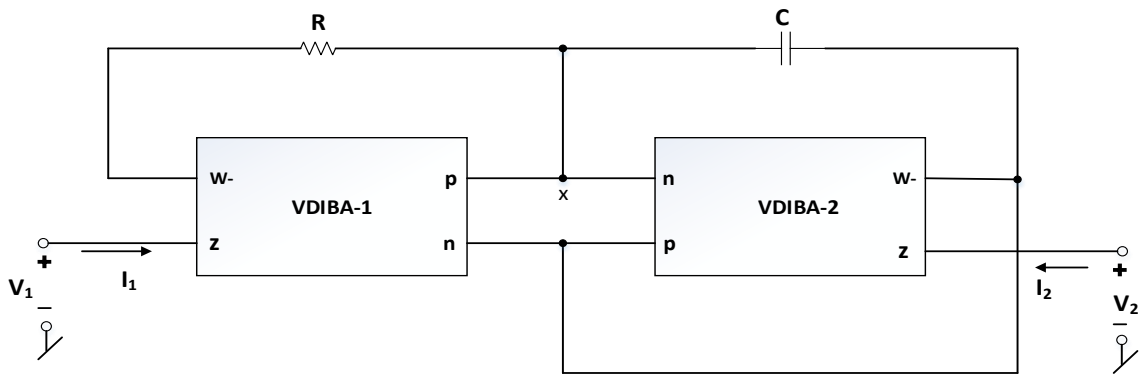

Fig. 3.1 Proposed lossy series inductance simulator

The proposed floating series inductor is realized with two VDIBAs, one resistor R and a capacitor C. Assuming Ideal VDIBA, from the VDIBA behavior description in Fig 2.1 and doing circuit analysis of Figure 3.1, with $g_{m1} = g_{m2} = g_m$, the equivalent input impedance can be derived as:

At node x,

$$(V_{w2} - V_x)sC = \frac{V_x - V_{w1}}{R} \tag{3.1}$$

From above Equation (3.1), we get

$$V_x = \frac{V_{w1-} + V_{w2-}\, sRC}{1 + sRC}$$

$$V_{w1-} = -V_{z1}, V_{w2-} = -V_{z2}, V_{z1} = V_1, V_{z2} = V_2$$

$$V_x = \frac{-V_1 - V_2\, sRC}{1 + sRC} \tag{3.2}$$

From Matrix (2.1), we know,

$$i_{z1} = g_m(V_{p1} - V_{n1})$$

$$V_{p1} = V_x$$

$$V_{n1} = -V_2$$

$$i_{z1} = -i_1$$

$$-i_1 = g_m(V_x + V_2) \tag{3.3}$$

Putting values of V_x from Equation (3.2) in Equation (3.3), we get Equation (3.4)

$$-i_1 = g_m \frac{-V_1 + V_2}{1 + sRC}$$

or

$$i_1 = g_m \frac{V_1 - V_2}{1 + sRC} \tag{3.4}$$

From Matrix 2.1:

$$i_{z2} = g_m(V_{p2} - V_{n2})$$
$$V_{p2} = -V_2$$
$$V_n = V_x$$
$$i_{z2} = -i_2$$
$$-i_2 = g_m(-V_2 - V_x) \quad (3.5)$$

Putting values of V_x from Equation 3.2 in Equation (3.5), we get Equation (3.6)

$$-i_2 = g_m \frac{-V_2 + V_1}{1 + sRC}$$

or

$$i_2 = g_m \frac{V_2 - V_1}{1 + sRC} \quad (3.6)$$

From Equation (3.4) and (3.6),

$$i_1 = g_m \frac{V_1 - V_2}{1 + sRC}$$

$$i_2 = g_m \frac{V_2 - V_1}{1 + sRC}$$

From above 2 Equations, we can say:

$$\begin{bmatrix} \mathbf{i_1} \\ \mathbf{i_2} \end{bmatrix} = \begin{bmatrix} \mathbf{\frac{g_m}{1 + sRC}} & \mathbf{-\frac{g_m}{1 + sRC}} \\ \mathbf{-\frac{g_m}{1 + sRC}} & \mathbf{\frac{g_m}{1 + sRC}} \end{bmatrix} \begin{bmatrix} \mathbf{V_1} \\ \mathbf{V_2} \end{bmatrix} \quad (3.7)$$

From standard two port network theorems, we have

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = [Y] \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

$$[Y] = \frac{1}{Z_{eq}} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \quad (3.8)$$

Thus, from above three equations, we can say that:

$$\mathbf{Y_{eq1} = g_m \left(\frac{1}{1 + sRC} \right)} \quad (\mathbf{3.9})$$

or

$$\mathbf{Z_{eq1} = \frac{1}{g_m} + \frac{s\,RC}{g_m}}$$

$$\mathbf{R_{eq} = \frac{1}{g_m}} \;\&\; \mathbf{L_{eq} = \left(\frac{C\,.\,R}{g_m} \right)} \quad (\mathbf{3.10})$$

From Equation (3.10), the proposed circuit in Fig. 3.1 realizes single capacitor based floating series R-L impedance, and equivalent RL values are described as $R_{eq} = \frac{1}{g_m}$ and $L_{eq} = \left(\frac{C\,R}{g_m}\right)$. From above analysis, the R_{eq} value can be tuned electronically via g_m, and inductance L_{eq} value can be tuned independently through R and/or C.

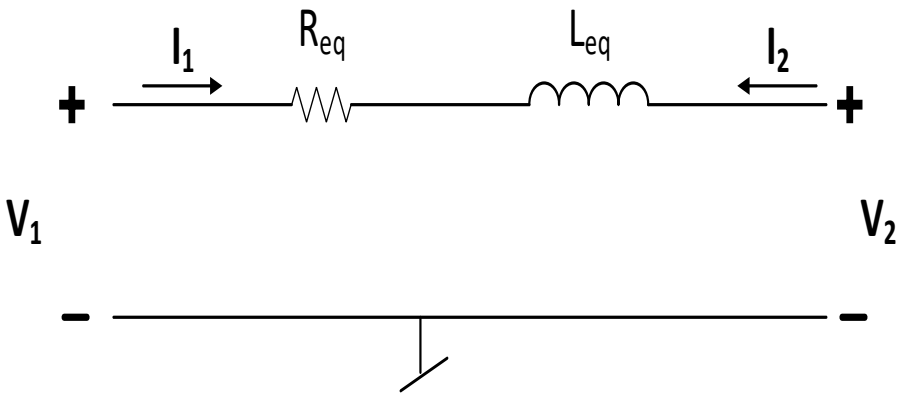

Fig. 3.2 Equivalent circuit for proposed floating series inductance

For above floating inductor circuit, the quality factor (Q) is defined as in Equation (3.11):

$$\mathbf{Q = w.R.C} \qquad (\mathbf{3.11})$$

Fig. 3.2 represents the equivalent circuit for floating series inductance between two ports with equivalent resistance $\mathbf{R_{eq} = \frac{1}{g_m}}$ and equivalent inductance as $\mathbf{L_{eq} = \left(\frac{C\,R}{g_m}\right)}$.

3.2 Proposed Floating Lossy Parallel Inductance Configuration

The proposed tunable floating parallel inductance realization employing voltage differencing inverted buffered amplifier as active element, along with resistor and capacitor, is shown in Fig. 3.3

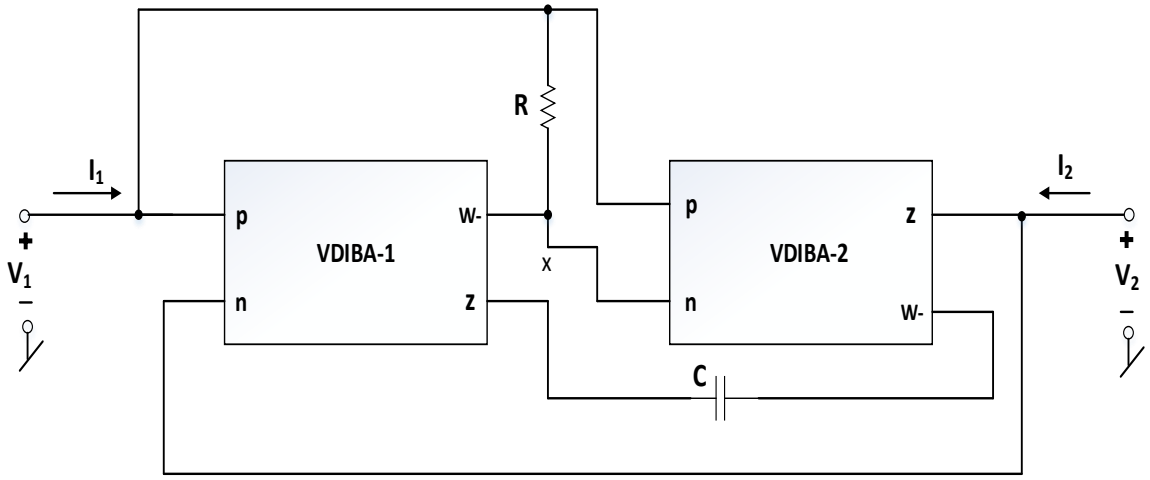

Fig. 3.3 Proposed floating parallel inductance simulator

Here, single capacitor based floating parallel inductor is realized with two VDIBAs along with one passive resistor R. From the VDIBA behavior in Matrix (2.1) circuit analysis is done below:

From Matrix (2.1), we know

$$i_{z1} = g_{m1}(V_{p1} - V_{n1})$$

$$V_{p1} = V_1$$

$$V_{n1} = V_2$$

$$i_{z1} = (V_{z1} - V_{w2})sC$$

$$V_{w2} = -V_2$$

At terminal Z1 of VDIBA-1,

$$g_{m1}(V_1 - V_2) = (V_{z1} - V_{w2})sC$$

$$g_{m1}(V_1 - V_2) = (V_{z1} - V_{w2})sC$$

On solving the above stated Equations, we get

$$V_{z1} = \frac{g_{m1}V_1 - V_2\,(g_{m1} + sC)}{sC} \qquad (3.12)$$

$$V_x = V_{w1} = -V_{z1}$$

$$i_1 = \frac{V_1 - V_x}{R}$$

$$i_1 = \frac{V_1 + V_{z1}}{R}$$

Putting Value of Vz1 from equation (3.12), we get i_1 as

$$i_1 = \frac{1}{R}\left[V_1 + \frac{g_{m1}V_{1-}\,V_2\,[g_{m1} + sC]}{sC}\right]$$

$$i_1 = \frac{1}{R}\left(\frac{(g_{m1} + sC)}{sC}\right)[V_{1-}\,V_2] \qquad (3.13)$$

From Matrix (2.1), we get

$$i_{z2} = g_{m2}(V_{p2} - V_{n2})$$

$$V_{p2} = V_1$$

$$V_{n2} = V_x$$

$$i_{z2-} = -i_2$$

$$-i_2 = g_{m2}(V_1 - V_x)$$

$$V_x = V_{w1} = -V_{z1}$$

$$-i_2 = g_{m2}(V_1 + V_{z1})$$

Putting value of V_{z1} from Equation (3.12), we get

$$-i_2 = g_{m2}[V_1 + \frac{g_{m1}V_{1-}\ V_2\ [g_{m1} + sC]}{sC}]$$

$$i_2 = g_{m2}\left(\frac{(g_{m1} + sC)}{sC}\right)[V_{2-}\ V_1]$$

$$i_2 = \left(g_{m2} + \frac{g_{m1}g_{m2}}{sC}\right)[V_{2-}\ V_1] \qquad (3.14)$$

From Equations (3.13) and (3.14), For $\mathbf{R} = \frac{1}{g_{m2}}$ we get,

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} (g_{m2} + \frac{g_{m1}g_{m2}}{sC}) & -(g_{m2} + \frac{g_{m1}g_{m2}}{sC}) \\ -(g_{m2} + \frac{g_{m1}g_{m2}}{sC}) & (g_{m2} + \frac{g_{m1}g_{m2}}{sC}) \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \qquad (3.15)$$

From standard two port network theorem, we have Y matrix defined as:

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = [Y] \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

$$[Y] = \frac{1}{Z_{eq}} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}$$

Thus, on comparing above three equations, we get

$$\mathbf{Y_{eq}} = \left(\mathbf{g_{m2}} + \frac{\mathbf{g_{m2}}\,\mathbf{g_{m1}}}{\mathbf{sRC}}\right) \qquad (\mathbf{3.16})$$

$$\mathbf{R_{eq1}} = \frac{\mathbf{1}}{\mathbf{g_{m2}}} \,\&\, \mathbf{L_{eq1}} = \frac{\mathbf{C}}{\mathbf{g_{m1}}\mathbf{g_{m2}}} \qquad (\mathbf{3.17})$$

Thus, from Equation (3.17), it can be inferred that the circuit in Fig. 3.3 realizes single capacitor based floating parallel RL impedance, and equivalent R, L values being described as $\mathbf{R_{eq}} = \frac{\mathbf{1}}{\mathbf{g_{m2}}}$ and $\mathbf{L_{eq}} = \frac{\mathbf{C}}{\mathbf{g_{m1}}\mathbf{g_{m2}}}$. From this it is seen that R_{eq} value can be tuned through R and/or g_{m2} and the L_{eq} is electronically tunable through g_{m1}.

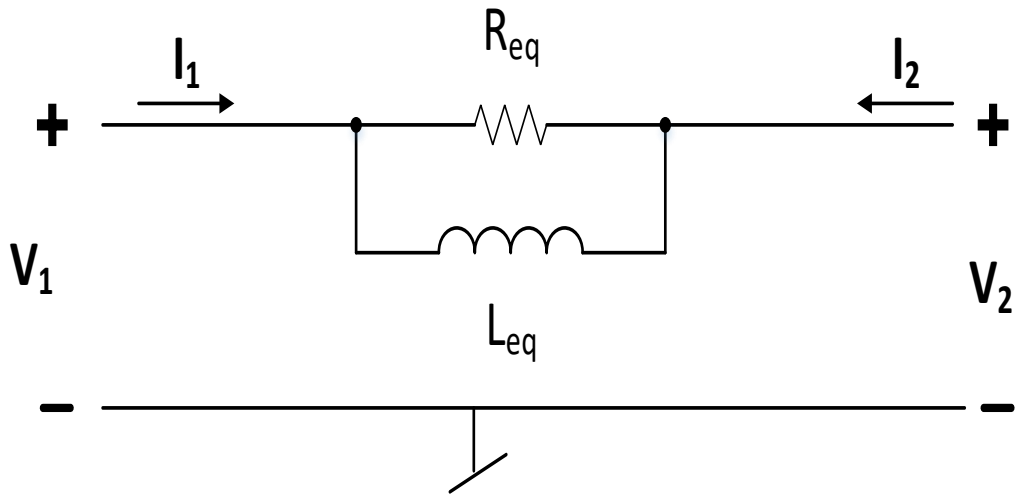

Fig. 3.4 Equivalent Circuit of Proposed floating parallel inductance

For above circuit, the quality factor (Q) is described as:

$$\mathbf{Q} = \frac{\boldsymbol{\omega}.\mathbf{C}}{\mathbf{g_{m1}}} \qquad (\mathbf{3.18})$$

Fig. 3.4 represents the equivalent circuit of lossy floating parallel inductance between two ports with equivalent resistance $R_{eq} = \frac{1}{g_{m2}}$ and equivalent inductance as $L_{eq} = \frac{C}{g_{m1}g_{m2}}$. And ω is the angular frequency of operation.

3.3 VDIBA Non-Ideal Performance Analysis

VDIBA non ideal model with its parasitic elements is depicted in Fig. 3.5. Practical VDIBA has parasitic resistances and capacitances at terminals p, n, and z to the ground **(Rp//Cp, Rn// Cn, and Rz//Cz)**, and a serial parasitic resistance $\mathbf{R_w}$ at the terminal w.

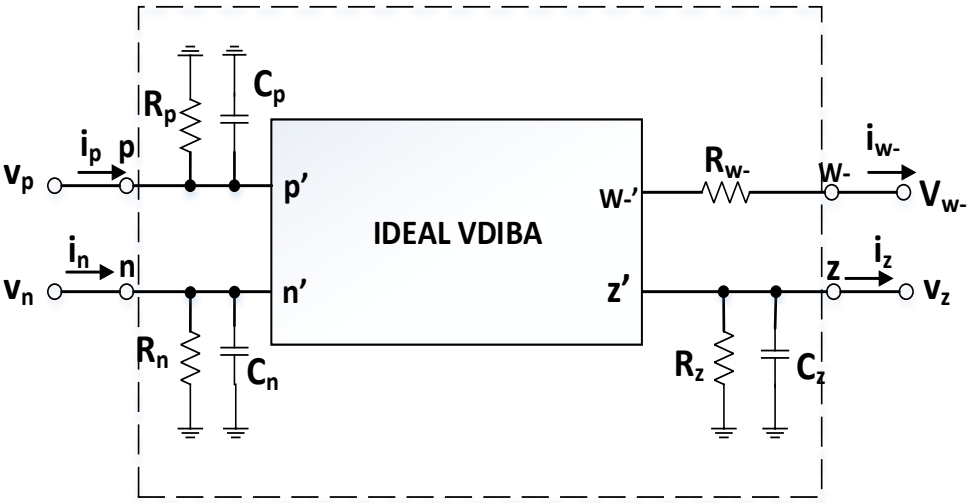

Fig. 3.5 VDIBA Non-Ideal Model showing its parasitic elements

Considering the parasitic resistance R_z and capacitance C_z of terminal z, the terminal voltages and current relationship is given by:

$$\begin{bmatrix} \boldsymbol{i_p} \\ \boldsymbol{i_n} \\ \boldsymbol{i_z} \\ \boldsymbol{v_{w-}} \end{bmatrix} = \begin{bmatrix} \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \boldsymbol{g_m} & \boldsymbol{-g_m} & \boldsymbol{sC_z + \frac{1}{R_z}} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \boldsymbol{-\beta} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \boldsymbol{v_p} \\ \boldsymbol{v_n} \\ \boldsymbol{v_z} \\ \boldsymbol{v_{w-}} \end{bmatrix} \qquad (\mathbf{3.19})$$

Where β= (1-e_v), | e_v| < < 1, represents voltage tracking error from z terminal to terminal w-, g_m represents transconductance and C_z and R_z are the parasitic elements of terminal z.

3.3.1 VDIBA Parasitic Elements Effect on Floating Series Inductor

Considering parasitic effects at Z terminal, Non-Ideal analysis is being done for determining floating lossy series inductance for Fig. 3.1.

At node x,

$$(\mathrm{V_{w2}} - \mathrm{V_x})\mathrm{sC} = \frac{\mathrm{V_x} - \mathrm{V_{w1}}}{\mathrm{R}} \qquad (3.20)$$

From above Equation (3.20), we get

$$\mathrm{V_x} = \frac{\mathrm{V_{w1-}} + \mathrm{V_{w2-}}\,\mathrm{sRC}}{1 + \mathrm{sRC}}$$

$$\mathrm{V_{w1-}} = -\beta_1 \mathrm{V_{z1}}, \mathrm{V_{w2-}} = -\beta_2 \mathrm{V_{z2}}, \mathrm{V_{z1}} = \mathrm{V_1}, \mathrm{V_{z2}} = \mathrm{V_2}$$

$$\mathbf{V_x} = \frac{\boldsymbol{-\beta_1 V_1 - \beta_2 V_2\,sRC}}{\mathbf{1 + sRC}} \qquad (\mathbf{3.21})$$

Assuming,

$$\mathrm{g_{m1}} = \mathrm{g_{m2}} = \mathrm{g_m}$$

$$\mathrm{i_{z1}} = \mathrm{g_m}\left(\mathrm{V_{p1}} - \mathrm{V_{n1}}\right) + \mathrm{V_{z1}}\left(\mathrm{sC_{z1}} + \frac{1}{\mathrm{R_{z1}}}\right)$$

$$\mathrm{V_{p1}} = \mathrm{V_x}$$

$$V_{n1} = -\beta_2 V_2$$

$$i_{z1} = -i_1$$

$$-i_1 = g_m(V_x + \beta_2 V_2) + V_{z1}\left(sC_{z1} + \frac{1}{R_{z1}}\right)$$

Putting value of V_x from Equation (3.21) in above Equation, we get Equation (3.22)

$$-i_1 = g_m \frac{-\beta_1 V_1 + \beta_2 V_2}{1 + sRC} + V_{z1}(sC_{z1} + \frac{1}{R_{z1}})$$

$$\mathbf{i_1 = g_m \frac{V_1\left(\frac{\beta_1 - (1 + sRC)(sC_{z1} + \frac{1}{R_{z1}})}{g_m}\right) - \frac{\beta_2 V_2}{g_m}}{1 + sRC}} \qquad (\mathbf{3.22})$$

Similarly, from Equation (3.19) we get,s

$$i_{z2} = g_m(V_{p2} - V_{n2}) + V_{z2}(sC_{z2} + \frac{1}{R_{z2}})$$

$$V_{p2} = -\beta_2 V_2$$

$$V_n = V_x$$

$$i_{z2} = -i_2$$

$$-i_2 = g_m(-\beta_2 V_2 - V_x) + V_2\left(s.C_{z2} + \frac{1}{R_{z2}}\right)$$

Putting values of V_x from equation (3.21) in above equation, we get:

$$-i_2 = g_m \frac{-\beta_2 V_2 + \beta_1 V_1}{1 + sRC} + V_2\left(sC_{z2} + \frac{1}{R_{z2}}\right)$$

$$\mathbf{i_2 = g_m \frac{V_2\left(\frac{\beta_2 - (1 + sRC)(sC_{z2} + \frac{1}{R_{z2}})}{g_m}\right) - \frac{\beta_1 V_1}{g_m}}{1 + sRC}} \qquad (3.23)$$

From Equation (3.22) and (3.23), we get,

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} (g_m\boldsymbol{\beta_1} + (\mathbf{1} + \mathbf{sRC})(\mathbf{sC_{z1}} + \frac{\mathbf{1}}{\mathbf{R_{z1}}})) & -(g_{m2}\boldsymbol{\beta_2}) \\ -(g_{m2}\boldsymbol{\beta_2}) & (g_m\boldsymbol{\beta_2} + (\mathbf{1} + \mathbf{sRC})(\mathbf{sC_{z2}} + \frac{\mathbf{1}}{\mathbf{R_{z2}}})) \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

Assuming $\beta_1, \beta_2 = 1, C_{z2} = C_{z1} = C_z$ and $R_{z2} = R_{z1} = R_z$, we get

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} (g_m + (1 + sRC)(sC_z + \frac{1}{R_z})) & -(g_m) \\ -(g_m) & (g_m + (1 + sRC)(sC_z + \frac{1}{R_z})) \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

Thus from above equation, we can infer that equivalent impedance is affected by parasitic elements.

3.3.2 VDIBA Parasitic Elements Effect on Floating Parallel Inductor

Considering parasitic effects, Non-Ideal analysis is being done for determining floating lossy parallel inductance for Fig. 3.3. As we have already seen the non-ideal circuit equations with the help of Equation (3.19).

$$i_{z1} = g_{m1}(V_{p1} - V_{n1}) + V_{z1}(sC_{z1} + \frac{1}{R_{z1}})$$

$$V_{p1} = V_1$$

$$V_{n1} = V_2$$

$$i_{z1} = (V_{z1} - V_{w2})sC$$

$$V_{w2} = -\beta_2 V_2$$

$$g_{m1}(V_1 - V_2) + V_{z1}(sC_{z1} + \frac{1}{R_{z1}}) = (V_{z1} - V_{w2})sC$$

$$g_{m1}(V_1 - V_2) + V_{z1}\left(sC_{z1} + \frac{1}{R_{z1}}\right) = (V_{z1} + \beta_2 V_2)sC$$

On solving the above Equation, we get V_{z1} as shown in Equation (3.24)

$$V_{z1} = \frac{g_{m1}V_1 - V_2\,(g_{m1} + sC\beta_2)}{(sC - sC_{z1}) - \frac{1}{R_{z1}}} \qquad (3.24)$$

$$V_x = V_{w1} = -\beta_1 V_{z1}$$

$$V_{w1} = -\beta_1 V_{z1}$$

$$i_1 = \frac{V_1 - V_x}{R}$$

$$i_1 = \frac{V_1 + \beta_1 V_{z1}}{R} \qquad (3.25)$$

$$i_1 = \frac{g_{m1}}{R\left((sC - sC_{z1}) - \frac{1}{R_{z1}}\right)}\left[\left(\frac{V_1\left((sC - sC_{z1}) - \frac{1}{R_{z1}}\right)}{g_{m1}} + \beta_1 g_{m1}\right) - V_2\,[g_{m1}\ \beta_2 sC]\right] \qquad (3.26)$$

From Equation (3.19), we have

$$i_{z2} = g_{m2}(V_{p2} - V_{n2}) + V_{z2}(sC_{z2} + \frac{1}{R_{z2}})$$

$$V_{p2} = V_1$$

$$V_{n2} = V_x$$

$$V_x = V_{w1} = -V_{z1}$$

$$-i_2 = g_{m2}(V_1 + \beta_1 V_{z1}) + V_{z2}\left(sC_{z2} + \frac{1}{R_{z2}}\right)$$

On putting V_{z1} value from Equation (3.24) in above Equation, we get Equation (3.27)

$$-i_2 = g_{m2}\left[V_1 + \frac{g_{m1}V_{1-}\, V_2\,[g_{m1} + sC\beta_1]}{(sC - s\,C_{z2}) + \frac{1}{R_{z2}}}\right] + V_2\left(sC_{z2} + \frac{1}{R_{z2}}\right) \qquad (3.27)$$

$$i_2 = -g_{m2}\left[\frac{V_1\left[\left((sC - sC_{z2}) + \frac{1}{R_{z2}}\right)\right] + \beta_1 g_{m1}V_1 - V_2\,[g_{m1} + sC\beta_1]}{(sC - s\,C_{z2}) + \frac{1}{R_{z2}}}\right] + V_2(sC_{z2} + \frac{1}{R_{z2}})$$

$$\mathbf{i_2} = \frac{\mathbf{g_{m2}}}{(\mathbf{sC} - \mathbf{C_{z2}}) + \frac{\mathbf{1}}{\mathbf{R_{z2}}}}\left[-\mathbf{V_1}\left[\left[\left((\mathbf{sC} - \mathbf{sC_{z2}}) + \frac{\mathbf{1}}{\mathbf{R_{z2}}}\right)\right] + \boldsymbol{\beta_1 g_{m1}}\right] + \boldsymbol{D}\right] \qquad (\mathbf{3.28})$$

where D $= \mathbf{V_2}\left[\,[\mathbf{g_{m1}} + \mathbf{sC\beta_1}] + (\mathbf{sC_{z2}} + \frac{\mathbf{1}}{\mathbf{R_{z2}}})\left((\mathbf{sC} - \mathbf{sC_{z2}}) + \frac{\mathbf{1}}{\mathbf{R_{z2}}}\right)\right]$

Thus from above equation (3.28) and Equation (3.26), we can infer that Equivalent impedance is affected by parasitic elements of VDIBA.

CHAPTER 4

SIMULATION RESULTS

VDIBA CMOS circuit is simulated using TSMC 0.25-µm real transistor model and the corresponding dimensions of VDIBA transistors are mentioned in below Table [64].

Transistors	$\frac{W}{L}(\mu m)$
M1-M2	$\frac{2.5}{0.25}$
M3-M4	$\frac{2.5}{0.25}$
M5-M6	$\frac{75}{0.25}$

Table I: Dimensions of VDIBA CMOS transistors

Supply voltage of V_{dd} = -V_{ss} = 0.75 V, along with DC biasing current of I_{bias} = 100mA are used which corresponds to $g_m = 336\frac{uA}{V}$. The g_m value is controllable through external biasing DC current $\mathbf{I_{bias}}$ based on the following expression:

$$\mathbf{g_m} = \sqrt{\mu\, \mathbf{C_{ox}} \frac{\mathbf{W}}{\mathbf{L}} \mathbf{I_{bias}}} \qquad (\mathbf{4.1})$$

Where μ represents carrier mobility, C_{ox} represents the gate capacitance per unit area, L and W are the effective channel length and width of transistors and $\boldsymbol{I_{bias}}$ is the DC biasing current.

4.1 VDIBA Block Simulation Results

VDIBA DC transfer characteristics [60] are shown in Fig. 4.1- Fig. 4.3

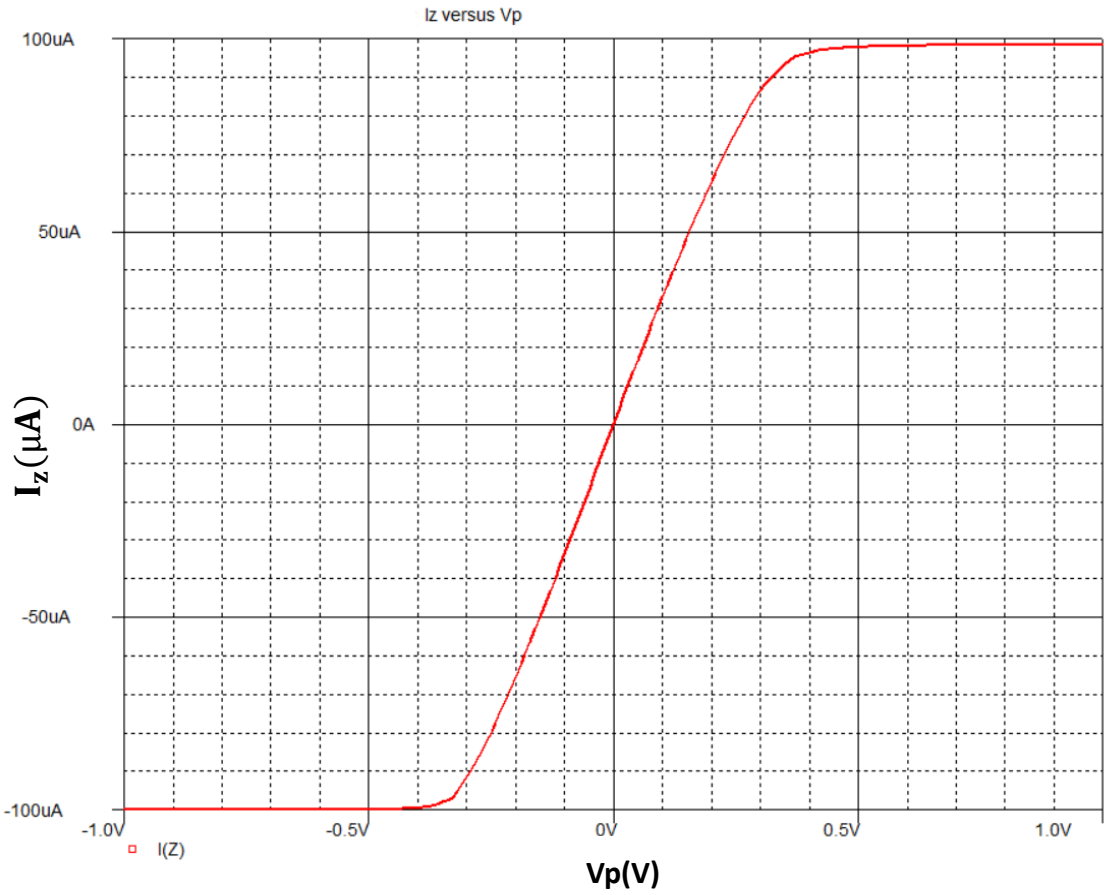

Fig. 4.1 I_Z vs V_p curve

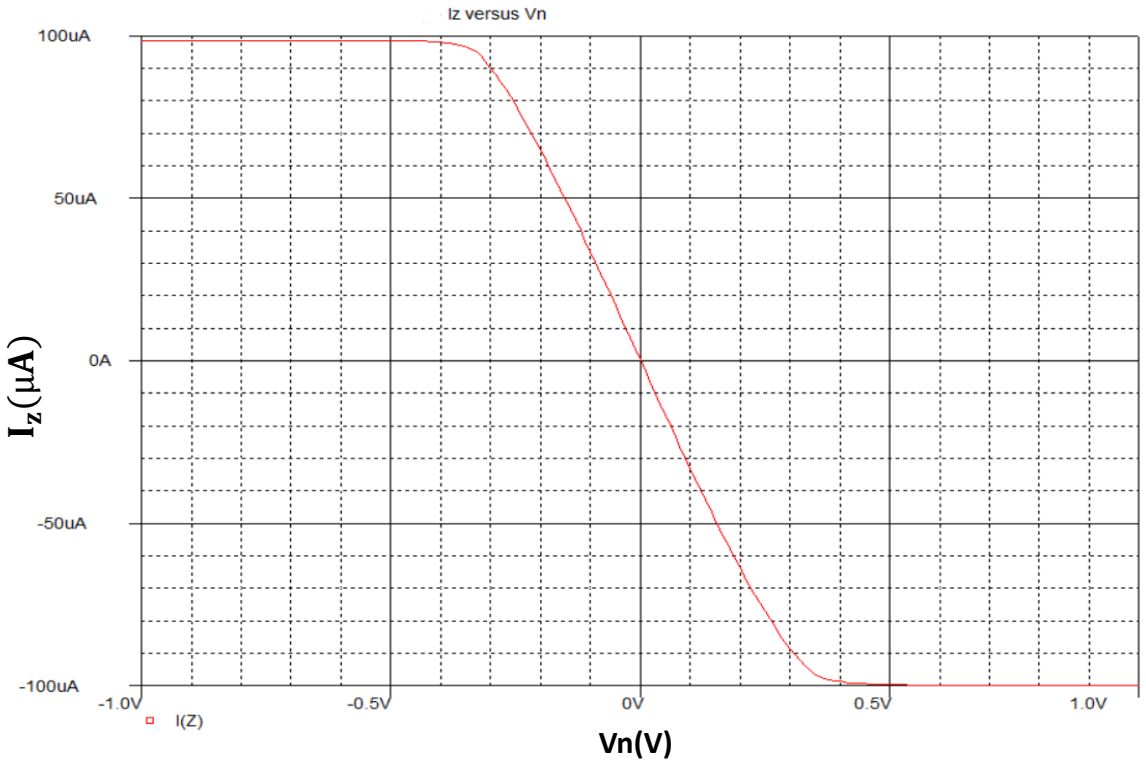

Fig. 4.2 I_Z vs V_n curve

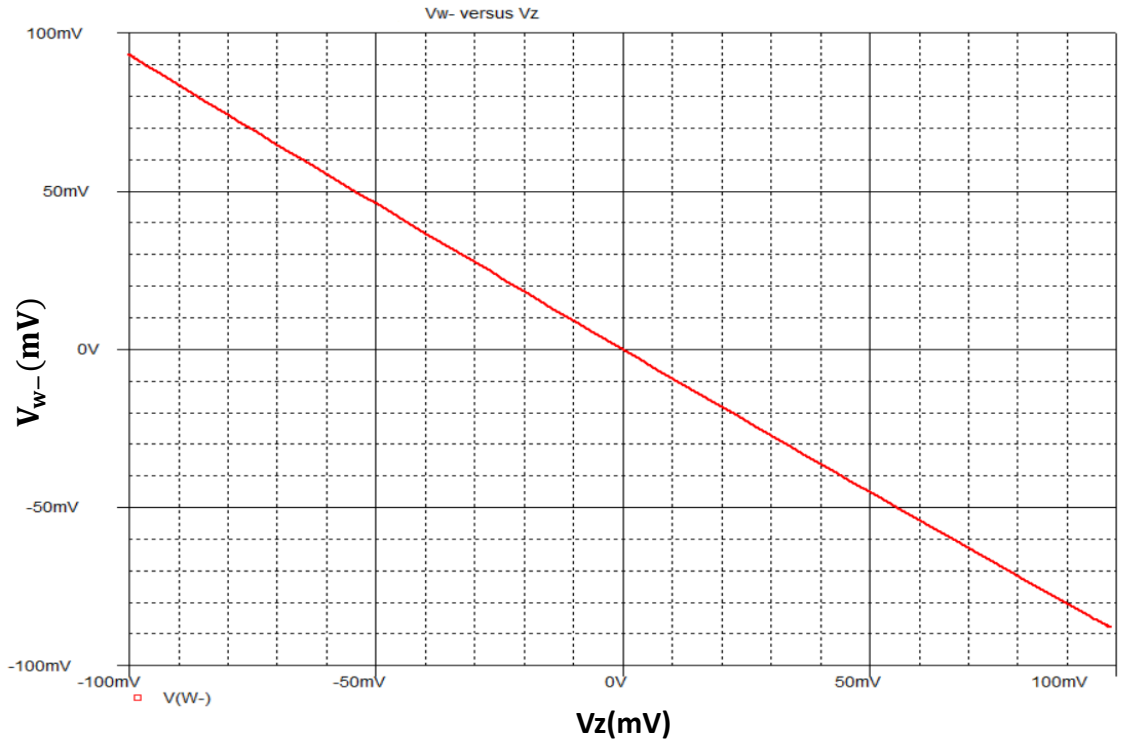

Fig. 4.3 V_{w-} vs V_z curve

VDIBA AC transfer characteristics shown in Fig. 4.4

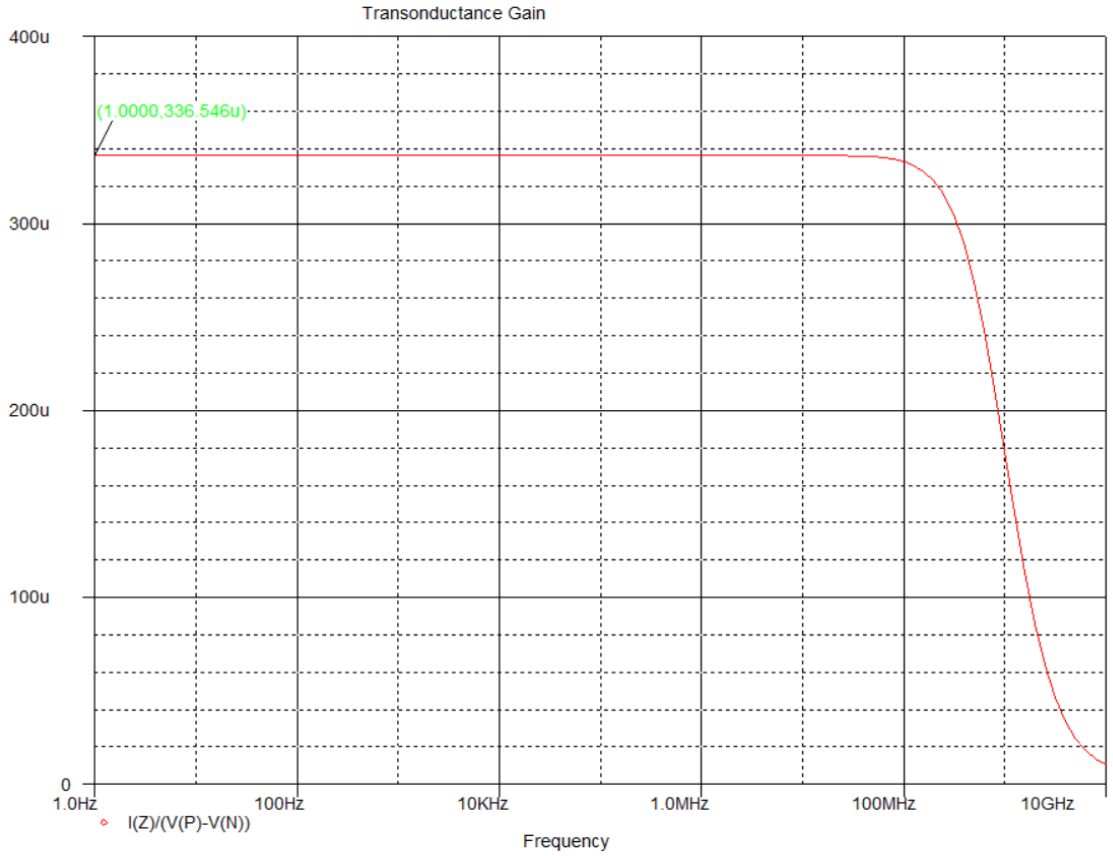

Fig. 4.4 Transconductance Gain of VDIBA ($g_m = 339\frac{uA}{V}$)

4.2 Proposed Lossy Series Inductor Simulation Results

For simulation of floating lossy series inductor of Fig. 3.1, the component values were selected as $C = 150pF$ and $R = 3k\Omega$.

1. The biasing current of the CMOS VDIBA is set to $I_{bias} = 100\mu A$ to obtain the value of $g_m = 336\mu A/V$(approx) (from equation).

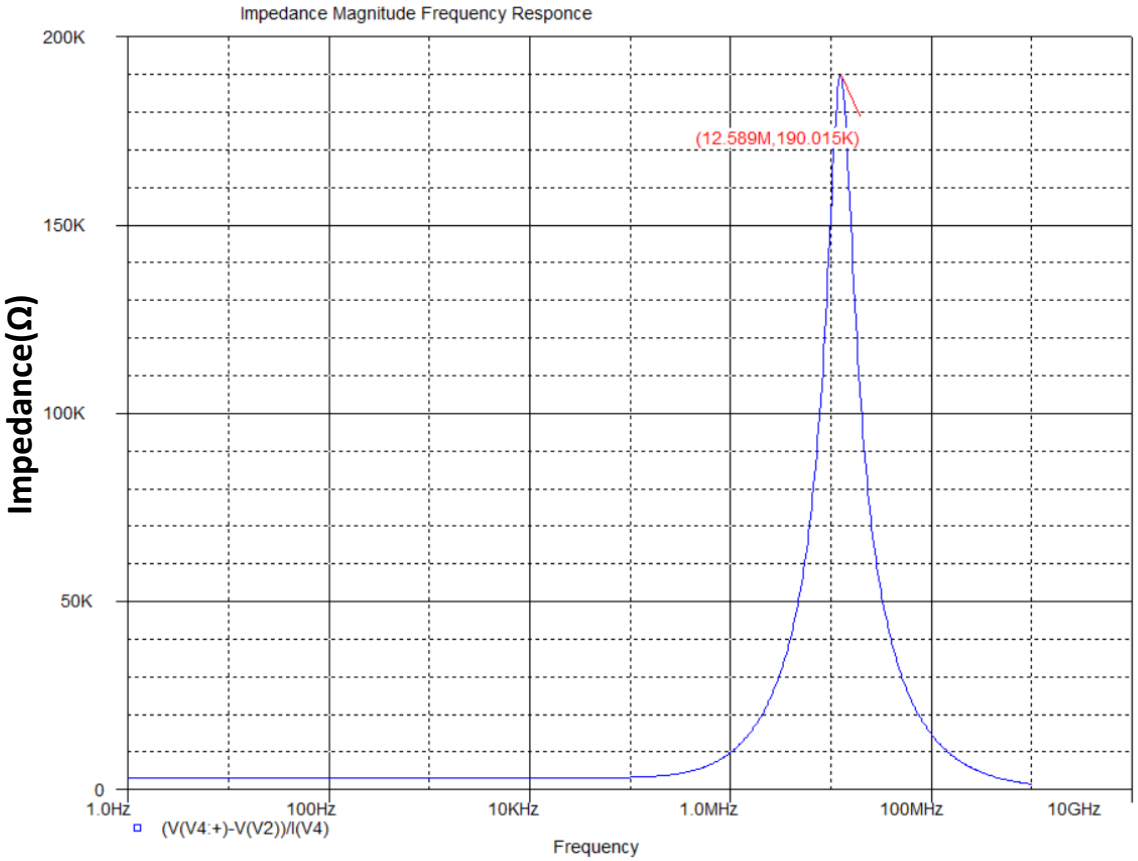

Fig. 4.5 Impedance magnitude–frequency response of Fig. 3.1 for $I_{bias} = 100\mu A$

In above simulation,

- $Z_{eq} = 4.9k$ is obtained through simulation at frequency of 266.65kHz
- On carrying out theoretical calculations, $Z_{eq} = 4.5k$ is obtained at 266.65kHz frequency.

2. The biasing current of the CMOS VDIBA is set to $I_{bias} = 120\mu A$ to obtain the value of $g_m = 354.387\mu A/V$.

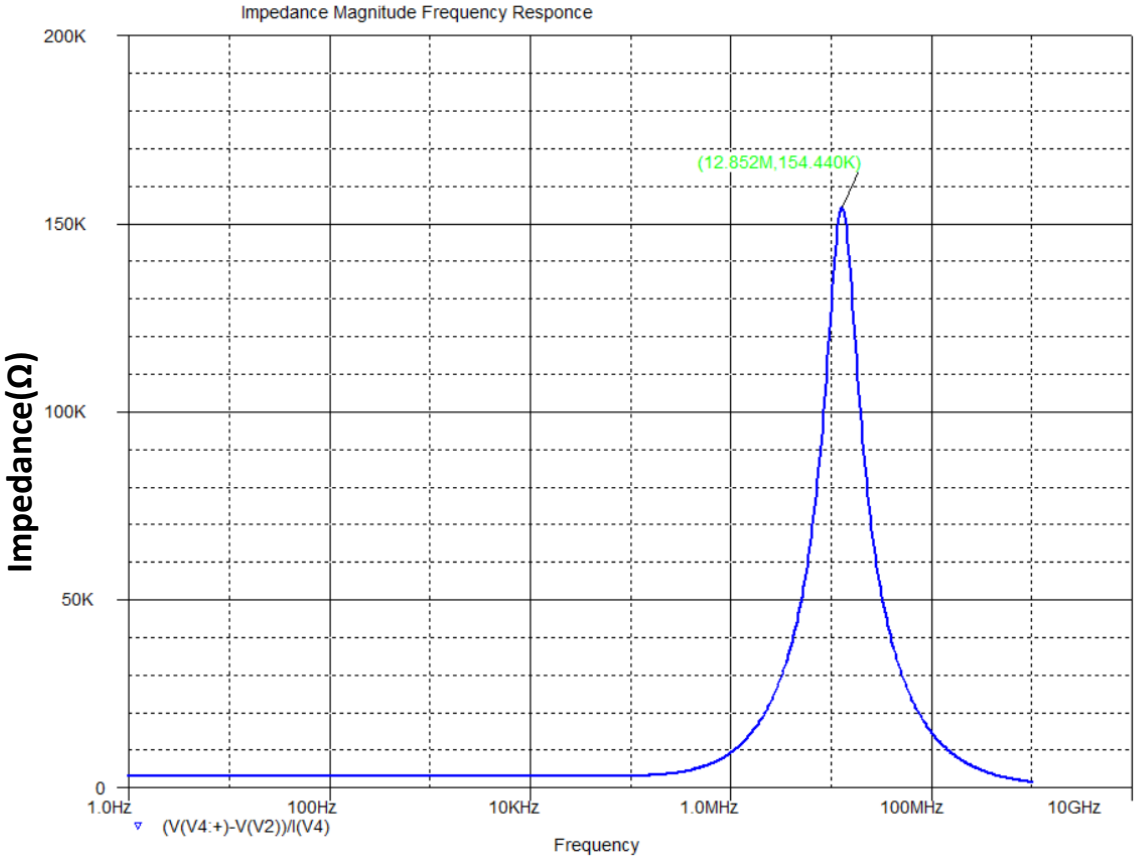

Fig. 4.6 Impedance magnitude–frequency responses of Fig. 3.1 for $I_{bias} = 120\mu A$

In above simulation,

- $Z_{eq} = 5.3k$ is obtained through simulation at frequency of 504.11kHz
- On carrying out theoretical calculations, $Z_{eq} = 4.9k$ is obtained at 504.11kHz frequency.

3. The biasing current of the CMOS VDIBA is set to $I_{bias} = 120\mu A$ to obtain the values of $g_m = 375.335\mu A/V$.

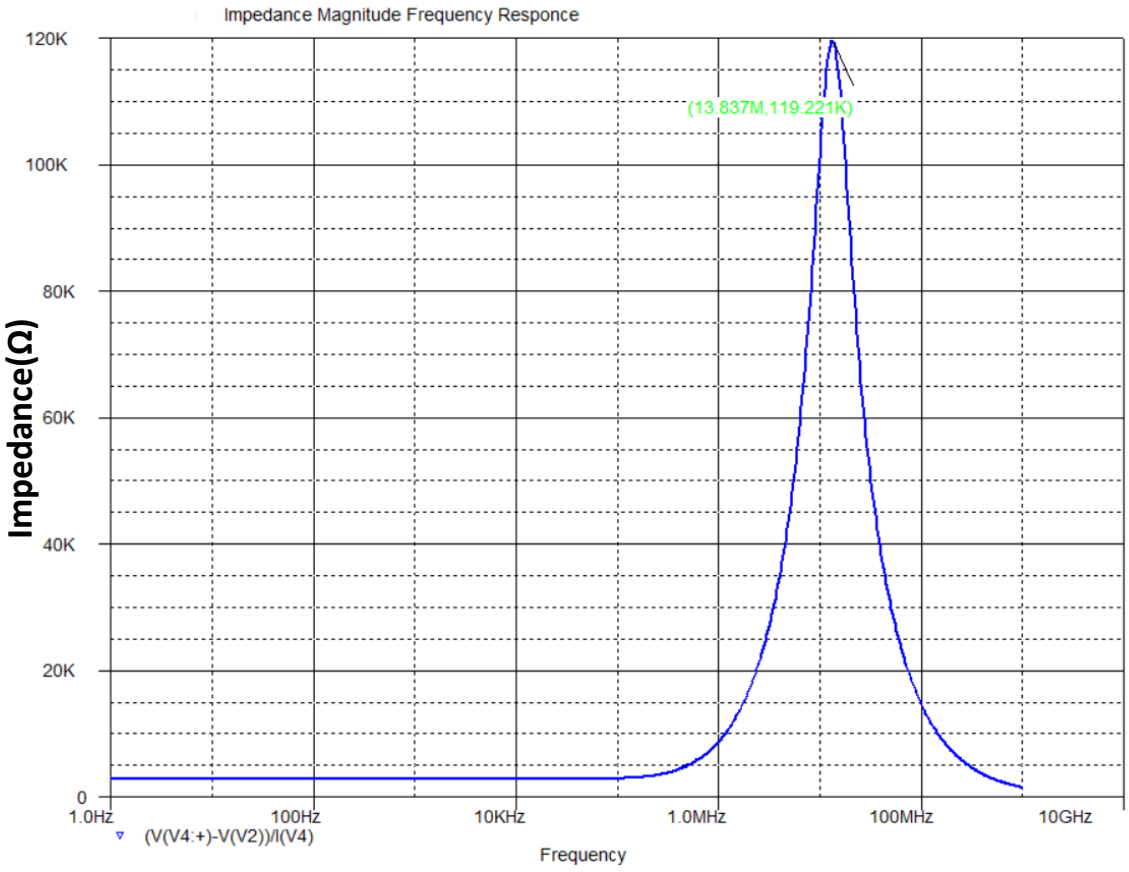

Fig. 4.7 Impedance magnitude–frequency responses of Fig. 3.1 for $I_{bias} = 150\mu A$

From above cases, it is seen that simulated and theoretical results are in close agreement between **1 kHz and 1 MHz** frequency range.

4.3 Workability Example for proposed series Inductor

To check the workability of proposed floating series inductor of Fig. 3.1, it is applied in active RLC second order low pass filter as depicted in Fig 4.8. The corresponding transfer function of the designed filter is given as in Equation (4.2) below:

$$\mathbf{V_2} = \frac{\left(\frac{\mathbf{1}}{\mathbf{L_{eq}C_L}}\right)\mathbf{V_1}}{\mathbf{s^2} + \mathbf{s}\left(\frac{\mathbf{R_{eq}}}{\mathbf{L_{eq}}}\right) + \frac{\mathbf{1}}{\mathbf{L_{eq}C_L}}} \qquad (\mathbf{4.2})$$

Whose cut off frequency is described as:

$$\omega_o = \sqrt{\frac{\mathbf{1}}{\mathbf{L_{eq}C_L}}} \qquad (\mathbf{4.3})$$

and quality factor is denoted as:

$$\mathbf{Q} = \frac{\mathbf{1}}{\mathbf{R_{eq}}}\sqrt{\frac{\mathbf{L_{eq}}}{\mathbf{C_L}}} \qquad (\mathbf{4.4})$$

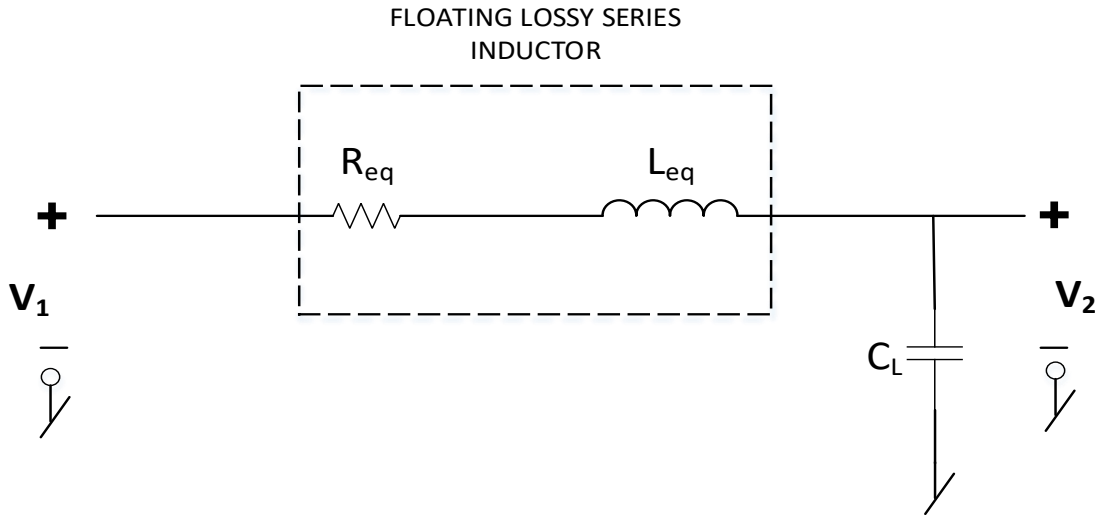

Fig. 4.8 RLC low-pass filter realized with the floating inductor in Fig. 3.1

The component values used for realizing filter are: $C = 150pF$, $R = 3k\Omega$ and $C_L = 265pF$.

- For $I_{bias} = 100\mu A$

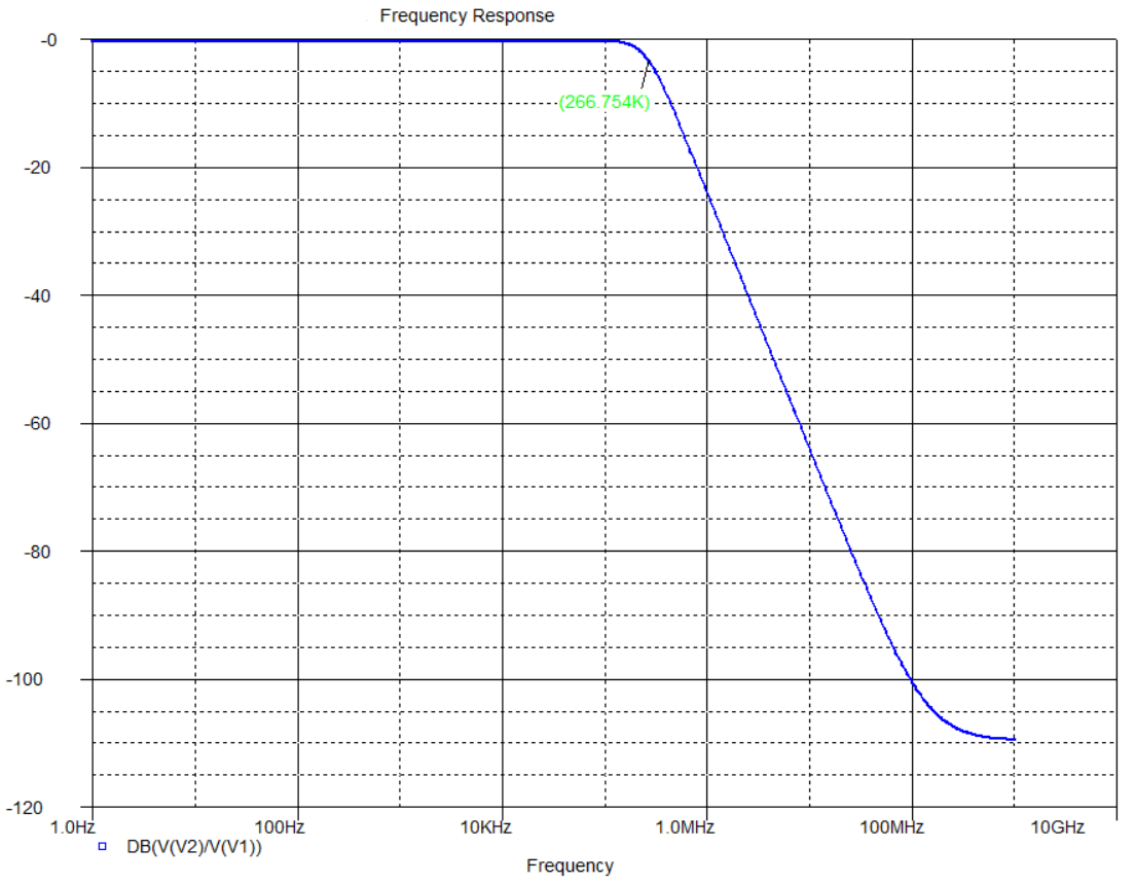

Fig. 4.9 Frequency response of the LPF using proposed floating inductor in Fig. 4.8

Practical Cut off frequency = 266.65 kHz (from simulation)

Theoretical Cut off frequency = 267.2 kHz (from equation (4.3))

- For $I_{bias} = 120\mu A$

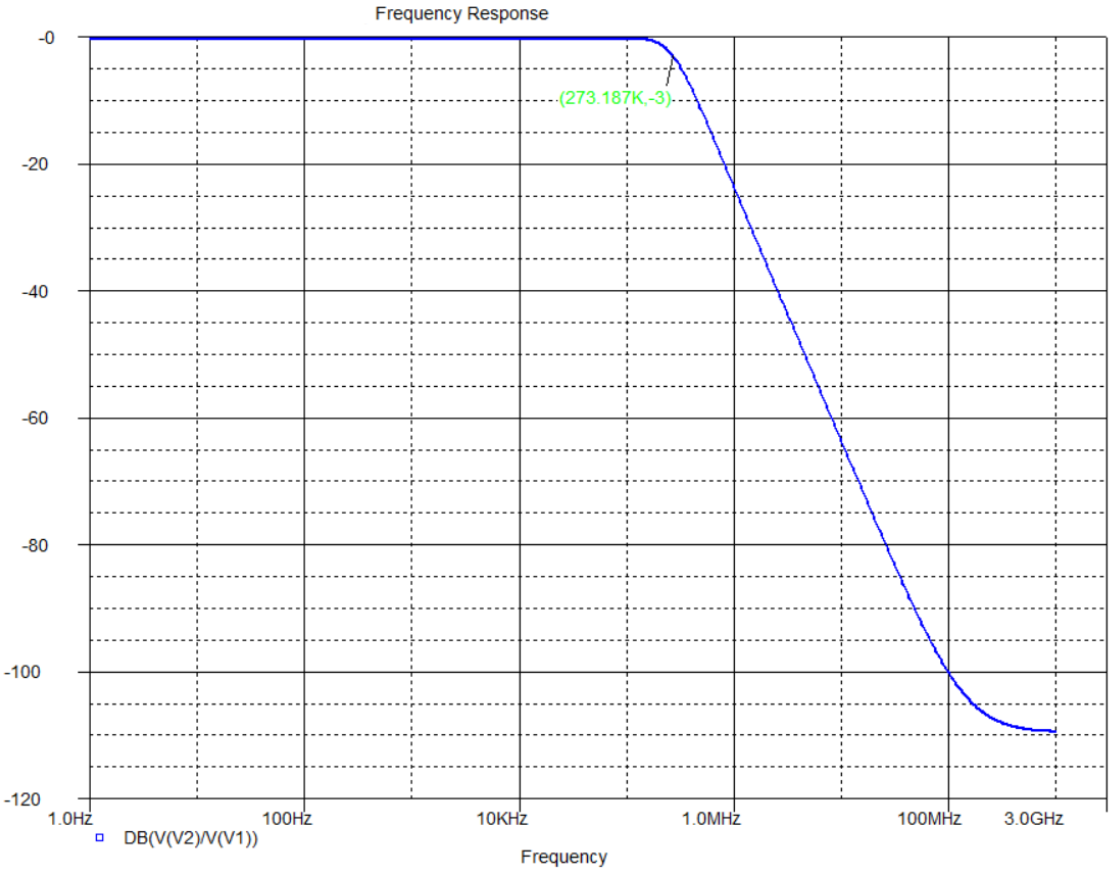

Fig. 4.10 Frequency response of the LPF using proposed floating inductor in Fig. 4.8

Practical Cut off frequency of filter = 273.18 kHz (from simulation)

Theoretical Cut off frequency of filter = 274.5 kHz (from Equation (4.3))

- For $I_{bias} = 150\mu A$

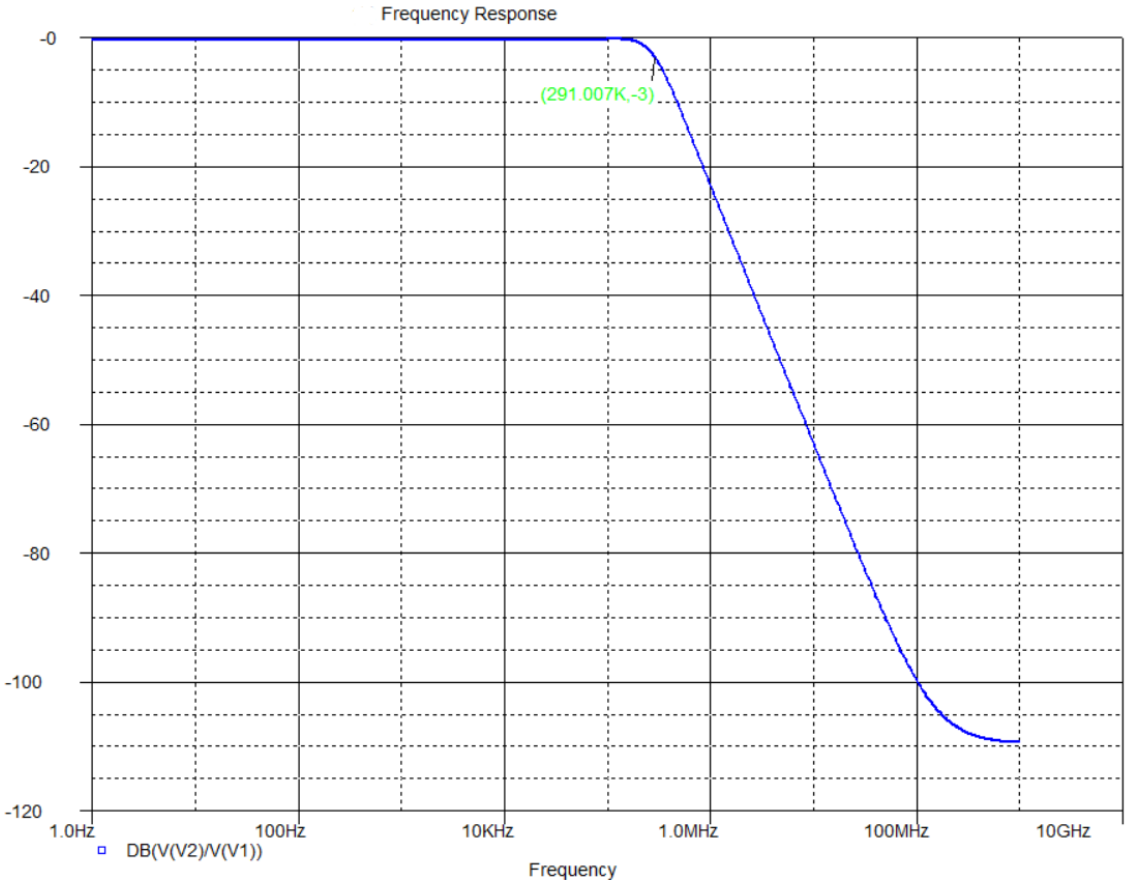

Fig. 4.11 Frequency response of the LPF using proposed floating inductor in Fig. 4.8

Practical Cut off frequency = 291 kHz

Theoretical Cut off frequency = 284 kHz

From above different analysis , we can see see the tunability of cut off frequency with g_m. Thus above analysis verifies the workability of the proposed floating inductor within a relative error range of +- 5%.

4.4 Workability Example for Proposed Parallel Inductor

To confirm the workability, the proposed lossy floating parallel inductor of Fig. 3.3 is used to implement the active resonant circuit depicted in Fig. 4.12 whose angular frequency and the quality factor are given by:

$$\omega_o = \sqrt{\frac{1}{L_{eq}C_L}} \; and \; \mathbf{Q} = \frac{1}{R_{eq}}\sqrt{\frac{L_{eq}}{C_L}} \qquad (4.5)$$

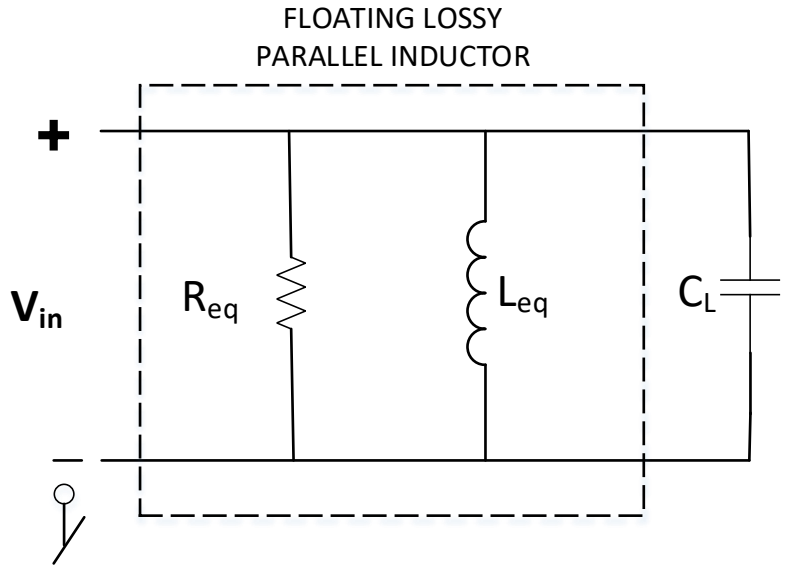

Fig. 4.12 Active Resonant circuit realized with the floating inductor of Fig. 3.3

A) For I_{bias1} = 120mA and I_{bias2} = 100mA and C_L= 50pF

Practical Cut off frequency, $f_o = 537.984kHz$ (from simulation)

Theoretical Cut off frequency, $f_t = 550.646$kHz (from Equation (4.5))

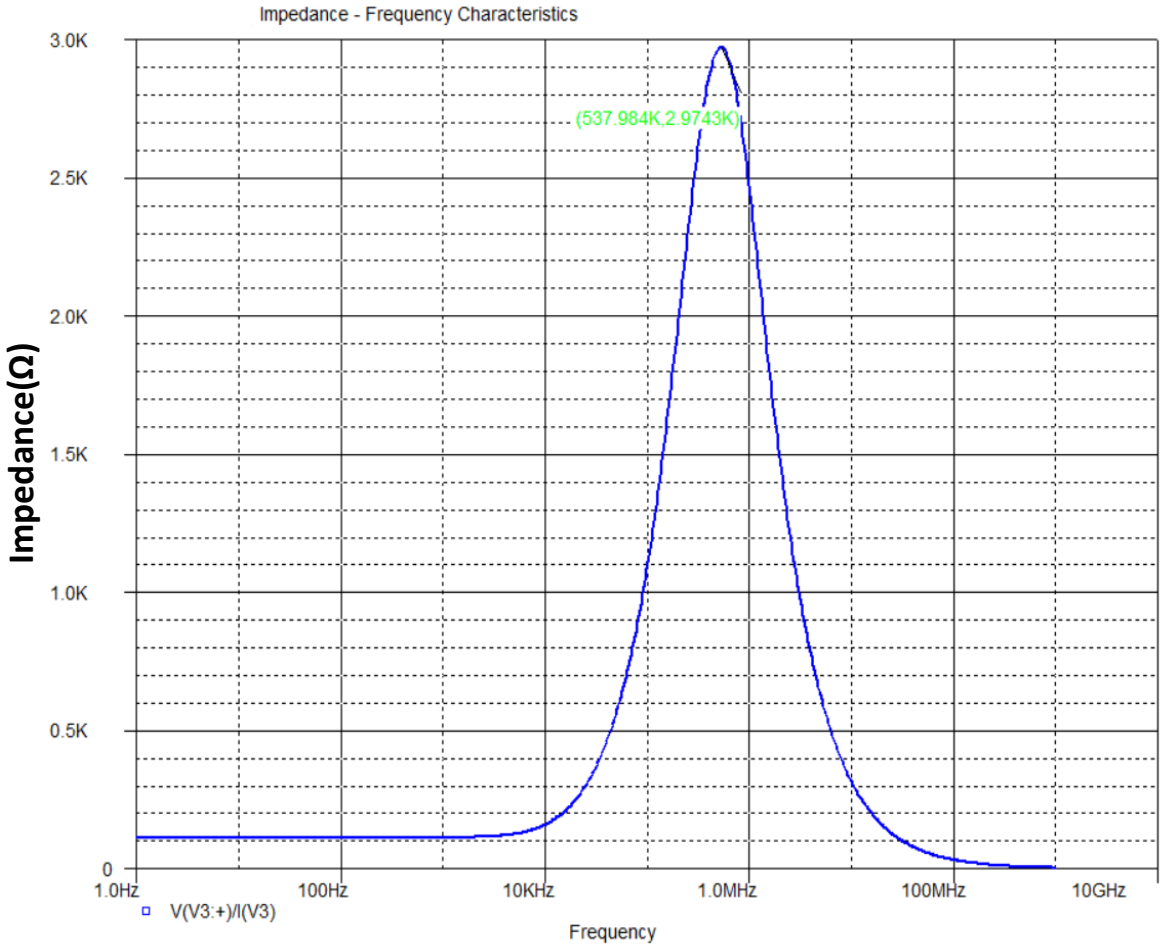

Fig. 4.13 Impedance- Frequency response of the parallel resonance circuit for VDIBA Biasing Currents.

B) For I_{bias1} = 150mA and I_{bias2} = 100mA and C_L= 50pF

Practical Cut off frequency, $f_p = 562.341kHz$ (from simulation)

Theoretical Cut off frequency, $f_t = 566.27$kHz (from equation 4.5)

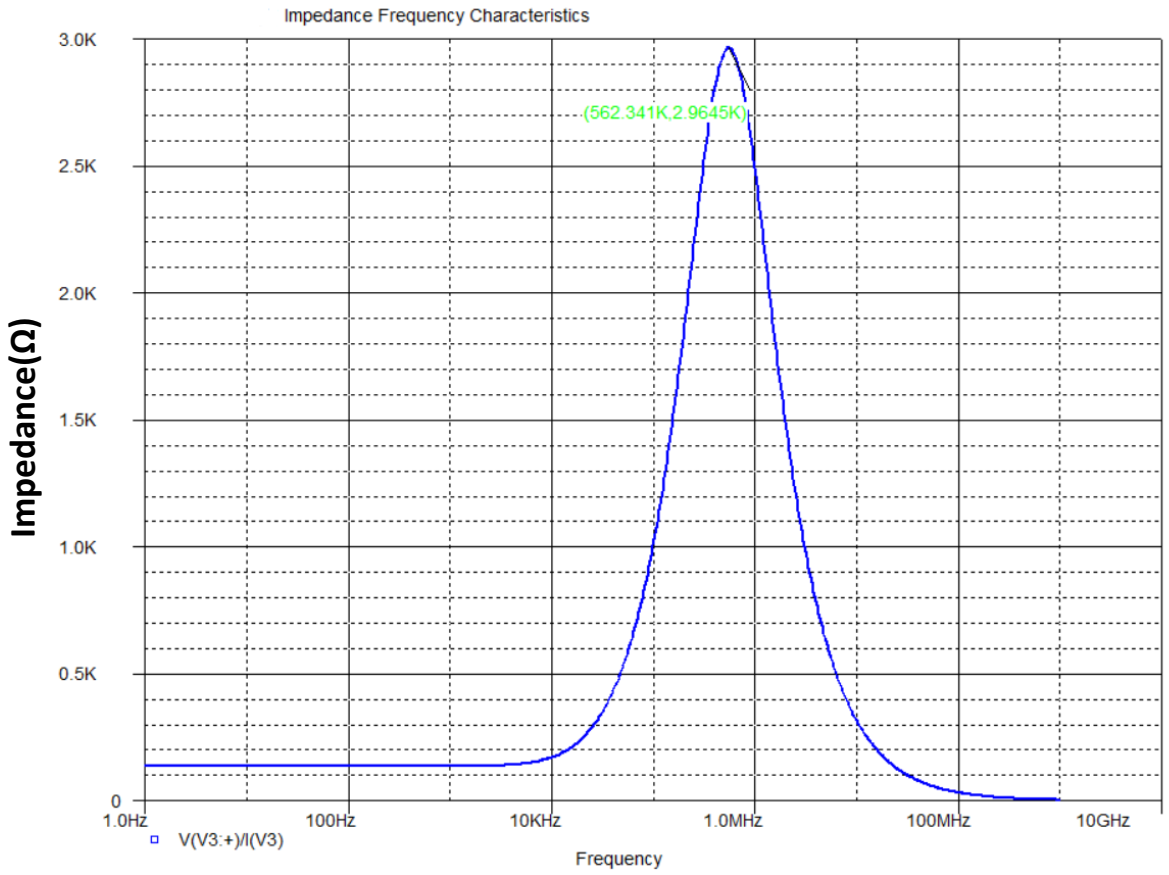

Fig. 4.13 Impedance Frequency response of the parallel resonance circuit for VDIBA Biasing Currents.

Thus, from above analysis, Electronic tuning of cut off frequency through Bias current confirms the workability of the proposed floating inductor parallel circuit.

4.5 Comparison of Proposed Floating Inductors with Previously Published Inductors:

Comparison of various performance parameters of proposed inductance simulator with the previous known simulators in the literature is shown in Table II.

INDUCTOR TERMINAL	REFERENCE	ACTIVE BLOCK COUNT	PASSIVE ELEMENT COUNT	INDUCTOR CONFIGURATION	ELECTRONIC TUNING
Floating	[65]	OTA=1 OTA=1, OA>=2	R=2, C=1	Series RL PARALLEL - RL	No
Floating	[66]	CFOA=2	R=3, C=1	Lossless Parallel-RL	No
Floating	[1]	CFOA=2	R=2, C=1	Series RL, Parallel-RL	No
Floating	[41]	CCII+ =2, CCII- = 1	R=2, C=1	Series RL, Parallel-RL	No
Floating	[67]	DDCC =1	R=2, C=1	Series-RL	No
Grounded	[68]	VDBA=1, MOS=1	C=1	Series RL, Parallel RL	Yes
Floating	[69]	DVCC=2	R=2, C=1	Lossless	No
Floating	[70]	VDBA=2	C=1	Lossless	Yes
Floating	[71]	CCII+=2, CFOA=1	R=2, C=1	Lossless	no
Floating	Proposed Inductors	VDIBA=2	R=1, C=1	Series-RL, ParallelRL	Yes

Table II: Proposed Circuit comparison with other Simulators

From the table it can be seen that inductors configurations in [65], [41] and [72] employ more number of active devices and simulators in [66], [69], [71] employ more number of passive components that the proposed simulator along with no tuning feasibility.

CONCLUSION

Among various modern active building blocks, VDIBA is emerging as quite flexible and versatile building block for analog circuit design. Alternative simple single capacitor based lossy floating inductance circuits (series and parallel) are presented employing two VDIBAs along with one passive resistor and capacitor each.

Inductance value in both floating inductors is electronically controllable in parallel RL circuit whereas it is controllable through resistor in series RL circuit. The synthetic lossy inductor and its application have been evaluated by employing PSPICE simulation for the TSMC 0.25-um CMOS technology. One NMOS transistor (in triode region) can be used which can act as Voltage controlled linear resistor (VCR) by which inductance value can also be tuned electronically.

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