ANALYTICAL MODELING AND TCAD SIMULATION OF In_2O_5Sn TRANSPARENT GATE ELECTRODE RECESSED CHANNEL MOSFET FOR HIGH PERFORMANCE APPLICATIONS

Thesis Submitted by

AJAY KUMAR

In Fulfillment of the Requirements for the Degree of

DOCTOR OF PHILOSOPHY

Under the Supervision of

PROF. M. M. TRIPATHI

&

DR. RISHU CHAUJAR

ELECTRICAL ENGINEERING DEPARTMENT

DELHI TECHNOLOGICAL UNIVERSITY

MARCH 2019

Dedicated to….

My Family

Delhi Technological University

(Govt. of National Capital Territory of Delhi)
Bawana Road, Delhi-110042

CERTIFICATE

This is to certify that the thesis titled "***Analytical Modeling and TCAD Simulation of In_2O_5Sn Transparent Gate Electrode Recessed Channel MOSFET for High Performance Applications***" is being submitted by ***Mr. Ajay Kumar*** with registration number ***2K16/PHD/EE/05*** to the Delhi Technological University for the award of the degree of Doctor of Philosophy in Electrical Engineering Department. The work embodied in this thesis is a record of bonafide research work carried out by him in the Microelectronics Research Lab, Applied Physics Department, Delhi Technological University (Formerly Delhi College of Engineering), New Delhi under the guidance of ***Prof. M. M. Tripathi*** and ***Dr. Rishu Chaujar***. It is further certified that this work is original and has not been submitted in part or fully to any other University or Institute for the award of any degree or diploma.

Ajay Kumar
Roll No.2K16/PHD/EE/05

This is to certify that the above statement made by the candidate is correct to the best of our knowledge.

Prof. Madhusudan Singh
Head & DRC Chairman
Electrical Engineering Department
Delhi Technological University
Delhi, India

Prof. M. M. Tripathi
Supervisor (Professor)
Electrical Engineering Department
Delhi Technological University
Delhi, India

Dr. Rishu Chaujar
Supervisor (Associate Professor)
Department of Applied Physics
Delhi Technological University
Delhi, India

ACKNOWLEDGMENTS

During three years of my research work, several people support with their valuable suggestions and make my research a wonderful journey. I would like to take this opportunity to acknowledge them.

First and foremost, I would like to express my sincere gratitude to my supervisor, mentor ***Dr. Rishu Chaujar*** *and* ***Prof. M.M. Tripathi*** *for their constant encouragement, support, and guidance at every stage of my research time. They provided me every opportunity to present my work at important conferences and in industry. I especially thank for prompt reading and careful review of my thesis.*

I am thankful to ***Prof. Yogesh Singh****, Vice Chancellor, Delhi Technological University,* ***Prof. Madhusudan Singh****, HOD, Electrical Engineering Department, DTU and* ***Prof. S. C. Sharma****, Applied Physics Department, DTU for their generous support and providing ample infrastructure to carry out my research work. I further thanks to SRC and DRC members* ***Prof. Madhusudan Singh (Chairman DRC), Prof. Harsupreet Kaur (External Expert),*** *for taking their decisive time serving in my committee and giving me treasured recommendations on my thesis.*

I wish to express my deepest gratitude to my beloved wife ***Dr. Neha Gupta*** *for her important, perceptive comments and suggestions which enhance the quality of my research work. It was her continuous moral support and encouragement without which this thesis would not have been possible. I also express my gratefulness to* ***Dr. Aditya Jain, Dr. Vinay Kumar, Dr. Rakesh Saroha, Dr. Ratneshwar Kumar Ratnesh, Dr. Lucky Krishnia, and Dr. Ashish Gupta*** *for the various discussions we had, both technical and otherwise.*

My colleagues, associates, and friends continuously influenced me in a positive way and have an important impact on my thinking. I will always remain

grateful to them for their selfless support. I want to thank ***Suryakant Shukla, Dr. Prakash Chittora, Dr. Ravi Gupta, Abhishek Bhardwaj, and Hemant Saxena.***

To each and every one whom I have met during my time at Microelectronics Research Laboratory: ***Anuj Chhabra, Samarth Singh, Balark Tiwari, Anuj Sinha, Pawan Singh, Deepak Singh, Bhavya Kumar, and Ardaman Kaur.***

I would also like to convey my extreme thanks to all the faculty members and technical staff of Department of Electrical Engineering and Department of Applied Physics for their continuous support.

I would like to thank ***University Grant Commission (UGC)****, New Delhi, for providing the financial support to carry out the research work. I would also like to acknowledge the support of* ***Department of Science and Technology (DST)*** *for research work and travel grant.*

*Last but not least, my father (****Ram Sajiwan Verma****), my mother (****Rani Devi****), my brother my ideal (****Sanjay Kumar****), my sister-in-law (****Sheela Verma****), my sisters (****Seema Verma, Sanno Verma and Sudha Verma****), my niece (****Vaishnavi Kumar****), my mother-in-law (****Rajkumari Gupta****), my brother-in-law (****Nikhil Gupta****), my sister-in-law (****Diksha Gupta****), my nephew (****Reyansh Gupta****), all my relatives and well-wishers, have always encouraged me and have been by my side in every challenging and tough situation. I am highly grateful towards my parents who have sacrificed boundlessly to make this thesis a success. Also, I would like to thank* ***Dr. Kunwar Singh*** *(Assistant Professor, NSIT, Delhi),* ***Dr. Sachin Umrao****,* ***Dr. Shubham Sahay*** *and* ***Dr. Amit Kumar Goyal*** *for their constant support and motivation during my research work.*

(Ajay Kumar)

New Delhi, March 2019

ABSTRACT

Analytical Modeling and TCAD Simulation of In_2O_5Sn Transparent Gate Electrode Recessed Channel MOSFET for High Performance Applications

In this era of internet of things (IoT), the scaling of CMOS is playing a vital role. However, scaling of MOSFETs beyond sub-nm regime is extremely challenging for non-planar device architecture owing to rigorous criteria required for the transistor switching. The stringent scaling may lead to static power dissipation due to increase in OFF-state leakage current. Many solutions have been proposed to overcome CMOS scaling bottleneck with different device architectures such as FinFETs, gate all around silicon nanowire (GAA SiNW), recessed channel (RC) MOSFETs and many more. Although many device structures such as GAA SiNW MOSFETs results in suppression of SCEs, it is not easy to fabricate this due to its non-planar architecture. RC MSOFET offers best possible gate control leading to SCEs and fabrication feasibility for IC industries at very low fabrication cost owing to planar architecture. Different gate materials have been used to improve the gate controllability over the channel and among all; indium tin oxide (ITO) is found to be the most suitable gate material. ITO is very feasible for fabrication and has a very low cost. ITO has a very low resistivity (10^{-5} Ω-cm) with higher Hall mobility (53.5 cm^2 $V^{-1}s^{-1}$). Due to these properties, ITO is frequently used in semiconductor devices and more commonly, for silicon-based MOSFET devices having technology less than 30 nm.

In this thesis, Transparent Gate Recessed Channel (TGRC) MOSFET have been critically scrutinized and compared with the conventional structures using device simulations obtained using ATLAS 3D device simulator. The analysis exemplified that TGRC-MOSFET has overcome the drawbacks faced by the conventional structures and improves the device analog and RF performance owing to trench gate

and ITO metal gate. The improved analog performance and architecture of the device makes it suitable for x-ray dosimeter and bio-sensing applications.

In the beginning, the analog and linearity performance of TGRC-MOSFET has been discussed along with the impact of trench depth [Negative Junction Depth (NJD)] and gate length (L_G) with an aim to achieve a reliable and high performance transistor. Proposed device improves the analog performance in terms of transconductance, device efficiency, output resistance, and gain. The improved analog and linearity performance at 5 nm NJD and 20 nm L_G of TGRC-MOSFET makes it suitable for low power linear RF amplifiers as a nano-scaled device.

Further, the reliability issues of the proposed device have been explored by considering the effect of interface trap charges (both polarity and density) in terms of static, linearity and intermodulation distortion FOMs. It is found that with the amalgamation of ITO on conventional recessed channel (CRC) MOSFET, the proposed device exhibits improved immunity against interface trap charges. In addition, the influence of ambient temperature (150-300K) along with trap charges on TGRC MOSFET has also been explored with an aim to analyse at which temperature the device is more stable in the presence of interface defects (trap charges).

Moreover, capacitance-voltage (C-V) analysis and frequency dependent capacitance have been analysed with an aim to examine the effectiveness of In_2O_5Sn as a gate material on parasitic capacitance. The capacitance dependent parameters such as Transconductance Frequency Product (TFP), Energy Delay Product (EDP) and Gain Bandwidth Product (GBP) have also been assessed and found that, TFP increases in comparison to metal gate RC MOSFET owing to a noticeable reduction in parasitic capacitance ($C_{gg}=C_{gs}+C_{gd}$), due to which EDP and GBP also improve considerably. In order to provide detailed insight to RF engineers for microwave applications, the small signal RF model has been studied in terms of microwave parameters such as *S* (scattering) parameters, *Z* (impedance) parameters, *Y* (admittance) parameters, and h (hybrid) parameters with an aim to analyse the behaviour of device at microwave frequency. It has also been observed that the

transit (cut-off) frequency (f_T) and maximum oscillator frequency (f_{MAX}) enhances significantly owing to the remarkable reduction in intrinsic capacitances.

After analysing the enhanced electrical properties of the proposed device, it has been explored for an X-Ray dosimeter as well as a biosensor. In the first application, TGRC-MOSFET has used as an x-ray dosimeter where x-ray radiation in the 0.5k to 10kRad dose range after irradiation has been considered. TCAD simulations for the same have been done to estimate threshold voltage shift in MOSFET with different radiation dosage. Models accounting for electron-hole pair generation and recombination are applied along with trap/de-trap model for insulator as well as interface charging. An improvement in radiation sensitivity has been found on increasing the oxide thickness from 2 nm to 6 nm. Along with signal amplification and processing circuit, this device can find enormous applicability in clinical and space environment. Further, the device applications have been extended and used for bio-sensing application. TGRC-MOSFET comprises a nano-gap cavity for the detection of biomolecules and transparent gate to enhance the overall current efficiency of RC-MOSFET. For the detection of neutral biomolecules, following electrical characteristics were studied: I_{ON}/I_{OFF}, shift in threshold voltage, change in surface potential and hereafter, calculate the sensitivity of the biosensor. In addition, TGRC noise immunity has been evaluated in the presence of biomolecules.

Thus, the high current switching ratio, lower I_{OFF}, lower SS, superior RF performance, temperature robustness, and better reliability in terms of ITCs makes TGRC-MOSFET, a promising candidate for employing in a low power, high switching speed and high performance applications even at wide temperature range.

LIST OF FIGURES

LIST OF TABLES

LIST OF PUBLICATIONS

In International Refereed Journals (9)

1. **A. Kumar,** M. M. Tripathi, and R. Chaujar "Reliability of Indium-Tin-Oxide with Interface Trap Charges on TGRC-MOSFET at Low Temperature" **IEEE Transactions on Electron Devices**, Vol.65, Issue 3, pp 860-866. **(IF: 2.605).**
2. **A. Kumar,** B. Tiwari, S. Singh, M. M. Tripathi, and R. Chaujar "Radiation Analysis of TGRC-MOSFET: An X-Ray Dosimeter for Clinical Applications" **IEEE Transactions on Electron Devices.** Vol.65, pp 5014-5020, 2018. **(IF: 2.605)**
3. **A. Kumar,** M. M. Tripathi, and R. Chaujar "Comprehensive Analysis of Sub-20nm Black Phosphorus Based Junctionless-Recessed Channel MOSFET for Analog/RF Applications" **Superlattices and Microstructures, Elsevier** Vol. 116, April 2018, Pages 171-180. **(IF: 2.123)**
4. **A. Kumar,** M. M. Tripathi, and R. Chaujar "Investigation of Parasitic Capacitances of In_2O_5Sn Gate Electrode Recessed Channel MOSFET for ULSI Switching Applications" **Microsystem Technologies, Springer** Vol 23, Issue 12, pp 5867–5874, 2017. **(IF: 1.581)**
5. **A. Kumar,** M. M. Tripathi, and R. Chaujar "Low Power, Highly Sensitive Nano-gap Embedded Sub-20nm TGRC-MOSFET for the Detection of Neutral Biomolecules" **Journal of computational electronics, Springer.** Vol 1, pp 1807-1815. **(IF: 1.526)**
6. **A. Kumar,** M. M. Tripathi, and R. Chaujar "In_2O_5Sn Based Transparent Gate Recessed Channel MOSFET: RF Small-Signal Model for Microwave Applications" **AEU International Journal of Electronocs and Communication, Elsevier,** Vol 93, Issue 9, pp 233–241**. (IF: 2.115).**
7. **A. Kumar** "Effect of Trench Depth and Gate Length Shrinking Assessment on the Analog and Linearity Performance of TGRC-MOSFET" **Superlattices and Microstructures, Elsevier** Volume 109, September 2017, Pages 626-640. **(IF: 2.123).**
8. **A. Kumar,** M. M. Tripathi, and R. Chaujar, "RF Noise Modeling of Black Phosphorus Junctionless Trench MOSFET in Strong Inversion Region", **Superlattices and Microstructures**, **Elsevier**. Vol. 125, pp. 72-79, 2019. **(IF: 2.123)**.
9. **A. Kumar,** M. M. Tripathi and R. Chaujar "High Sensitivity Assessment of TGRC MOSFET as a Protein Biomarker for Early Stage Diagnostics" **Vacuum, Elsevier**. Vol. 164, pp. 46-52, 2019**. (IF: 2.067).**

In International Conferences (15)

1. **A. Kumar,** M. M. Tripathi, and R. Chaujar "Low Power, Highly Sensitive Nano-gap Embedded TGRC-MOSFET for the Detection of Neutral Biomolecules" 5th International Conference on Bio-Sensing Technology Riva Del Garda, Italy (Elsevier), P-115. 7-10 May 2017.
2. **A. Kumar,** D. Kaur, M. M. Tripathi, and R. Chaujar "Influence of High-k Gate on Transparent Gate Recessed Channel (TGRC) MOSFET: A reliability Study" International Conference on Microelectronics Devices and Systems (ICMDCS), 10th to 12th August 2017, Vellore, India.
3. **A. Kumar,** M. M. Tripathi, and R. Chaujar "Effect of Interface Trap charge density on the reliability issues of TGRC-MOSFET: A reliability Study" International Conference on Microelectronics Devices and Systems (ICMDCS), 10th to 12th August 2017, Vellore, India.
4. **A. Kumar**, S. Singh, B. Tiwari and R. Chaujar, "Twin Gate Rectangular Recessed Channel (TG-RRC) MOSFET for Digital-Logic Applications". International Conference on Microelectronics Devices and Systems (ICMDCS), 10th to 12th August 2017, Vellore, India.
5. **A. Kumar,** M. M. Tripathi, and R. Chaujar "Small-Signal Modeling of In_2O_5Sn Based Transparent Gate Recessed Channel MOSFET for Microwave/RF Applications" IEEE APMC 2017 Kuala Lampur, 16-17 Nov, pp. 976-979.
6. **A. Kumar,** M. M. Tripathi, and R. Chaujar "Sub-20 nm Black Phosphorus Junctionless-Recessed Channel (BP JL-RC) MOSFET: A Low Power Device" 3rd Nanotechnology for Instrumentation and Measurement Workshop (NANOfIM), Gautam Buddha University Noida, India, November 16-17, 2017.
7. **A. Kumar**, S. Singh, B. Tiwari and R. Chaujar, "Junctionless Double Gate Recessed Channel (JL-DGRC) MOSFET for Digital-Logic Applications". 3rd Nanotechnology for Instrumentation and Measurement Workshop (NANOfIM), Gautam Buddha University Noida, India, November 16-17, 2017.
8. **A. Kumar,** M. M. Tripathi, and R. Chaujar, "Investigation of Novel Gate Materials on Recessed Channel (RC) MOSFET for High Performance Applications"pp. 402. ICN3I-2017, 6-8 Dec. IIT Roorkee.
9. **A. Kumar,** M. M. Tripathi, and R. Chaujar, "Sub-20nm In_2O_5Sn Gate Electrode Recessed Channel MOSFET for Bio-sensing Applications" International Symposium on Functional Materials (ISFM), 13-15 April, 2018, Chandigarh, India.

10. **A. Kumar,** M. M. Tripathi, and R. Chaujar, "High-Temperature Reliability of Black Phosphorus Recessed Channel (BPRC) MOSFET" 7th International Conference on Computing, Communication and Sensor Network (CCSN) 2018, 27-28 October, Kolkata India.
11. **A. Kumar,** M. M. Tripathi, and R. Chaujar, "TCAD Analysis of Sub-20 nm Black Phosphorus Trench (BP-T) MOSFET for High Temperature Applications" 7th International Conference on Computing, Communication and Sensor Network (CCSN) 2018, 27-28 October, Kolkata India**.**
12. **A. Kumar,** M. M. Tripathi, and R. Chaujar, "Linearity and Distortion Assessment of Black Phosphorus-Based Junctionless RC-MOSFET" 2018 3rd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT), Sri Venkateshwara College of Engineering, Bengaluru 18-19 May 2018.
13. **A. Kumar,** M. M. Tripathi, and R. Chaujar, "Investigation of Different Gate Materials onto Recessed Channel (RC) MOSFET for Improved Device Performance" 3rd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT), Sri Venkateshwara College of Engineering, Bengaluru 18-19 May 2018.
14. **Ajay Kumar**, S. Singh, B. Tiwari, and R. Chaujar, "Temperature Reliability of Junctionless Twin Gate Recessed Channel (JL-TGRC) MOSFET with Different Gate Material for Low Power Digital-Logic Applications. IEEE Region 10 Conference (TENCON), Jeju Island, Korea, 28-31 October 2018.
15. **A. Kumar,** M. M. Tripathi, and R. Chaujar, "Low-Temperature Reliability of Sub-20nm 4H-SiC Trench MOSFET with Black Phosphorus Gate Material", 5th International Conference on Signal Processing and Communication (ICSC), JIIT Noida, India, 7th to 9th March 2019.

TABLE OF CONTENTS

ACRONYMS

MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
BJT	Bipolar Junction Transistor
ICs	Integrated Circuits
CMOS	Complementary Metal Oxide Semiconductor
VLSI	Very-Large-Scale-Integrated
IT	Information Technology
SCEs	Short Channel Effects
SS	Subthreshold Swing
I_{OFF}	OFF Current
I_{ON}	ON Current
V_{th}	Threshold Voltage
DIBL	Drain Induced Barrier Lowering
V_{DS}	Drain-to-Source Voltage
V_{GS}	Gate-to-Source Voltage
HCEs	Hot Carrier Effects
SOI	Silicon on Insulator
CNTs	Carbon Nanotubes
RC	Recessed Channel
TCOs	Transparent Conducting Oxides
ITO	Indium Tin Oxide
IoT	Internet of Things
TGRC	Transparent Gate Recessed Channel
CRC	Conventional Recessed Channel
RF	Radio Frequency
FOMs	Figure of Merits
NJD	Negative Junction Depth
TFP	Transconductance Frequency Product
EDP	Energy Delay Product
GBP	Gain Bandwidth Product
S	Scattering parameters,

Z	Impedance parameters,
Y	Admittance parameters,
h	Hybrid parameters
f_T	Cut-off frequency
f_{MAX}	Maximum oscillator frequency
SRH	Shockley-Read–Hall
ITRS	International Technology Roadmap for Semiconductor
VIP2	Second order voltage intercept point
VIP3	Third order voltage intercept point
IIP3	Third order current intercept point
IMD3	Third order intermodulation distortion
HD3	Third-order harmonic distortion
HD2	Second order harmonic distortion.
IFM	Integral Function Method
P_{DC}	DC power
P_{AC}	AC power
ITC	Interface Trap Charges
NQS	Non-Quasi-Static
APTES	3-aminoppropyltriethoxysilane
ELISA	Enzyme-Linked Immunosorbent Assay
MDV	Marek's disease virus
C_{gs}	Gate to source capacitance
C_{gd}	Gate to drain capacitance
C_{gg}	Gate capacitance
L_{gap}	Length of cavity gap

1

CHAPTER

Introduction

- *This chapter discusses the brief overview of Nanoscale Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and the scaling of MOSFET.*
- *Various adverse effects arise due to the scaling of dimensions and different engineering schemes to overcome the limitations; have been discussed in this chapter.*
- *Moreover, the chapter describes the reliability issues of CMOS devices. In this respect, the origin of interface trap charges, that are inevitably present in any practical device are discussed and is followed by the discussion of the reliability of TGRC MOSFET.*
- *Further, the chapter describes the research gaps that are found while literature survey and is followed by the several possible solutions to overcome these gaps.*
- *In this regard, the chapter introduces Indium Tin Oxide (In_2O_5Sn) popularly known as ITO as a conducting gate material on to the recessed channel (RC) MOSFET.*
- *Thereafter, the significant merits offered by TGRC MOSFET are discussed that is extended with the major challenges faced by the conventional RC MOSFET.*
- *Thus, the chapter describes the primary objective of this thesis followed by an overview of all the chapters.*

1.1 OVERVIEW OF NANOSCALE MOSFET

Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) and bipolar junction transistor (BJT) are two major types of three-terminal semiconductor devices. Although both transistors offer unique features and areas of application, especially in the design of integrated circuits (ICs), MOSFET has become the most widely used electronic device and using this as the basic component, the entire circuits are fabricated on a single silicon chip. MOSFETs can be made quite small (requiring a small area on the silicon IC chip), and has simple manufacturing process and also requires very low power consumption as compared to BJT. The unrelenting ever increasing demand for high speed and dense ICs is the driving force for scaling down the CMOS technology to nanometer nodes that has resulted into transforming the state of art of designing the IC, by providing the stability of operation, low static power dissipation, and noise immunity to devices (Heyns & Tsai, 2009; Moore, 1975). These properties have made it possible on a single IC chip to implement very sophisticated, very-large-scale-integrated (VLSI) digital circuits.

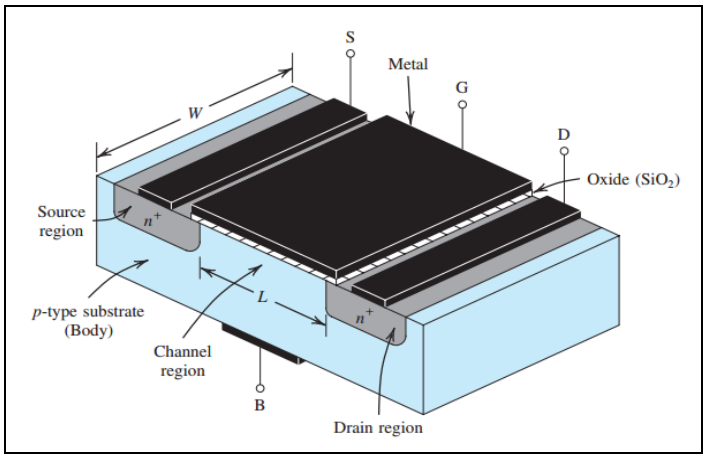


Figure 1.1: Schematic structure of Conventional MOSFET (Arora, 1993).

From past four decades, progress in IC technology has become the driving power in revolution of Information Technology (IT), and marvelously changed the whole world and our lives too. The great triumph of the CMOS devices is necessarily offered by the enhanced drive current and the higher cut off frequency acquired by scaling down the CMOS devices. The scaling of the CMOS devices follows the well-

known Moore's law proposed by Gordon Moore (the co-founder of Intel Corporation) in 1960's which predicts that the number of transistors per IC would double approximately every two years (Moore, 1975). Aggressive scaling of MOSFET down to nanometer regime is administered by the need of higher packing density, low operating power, and high switching speed. The constant scaling of MOSFET enhances its switching speed and also the cut-off frequency to Giga-Hertz regime and thus makes it appropriate for wireless and high-frequency applications.

However, the aggressive scaling of MOSFET fallouts into several critical issues such as various short channel effects (SCEs) (Chaudhry & Kumar, 2004). These SCEs degrades the performance of MOSFET and also increases the subthreshold swing (SS) to a value greater than the fundamental limit of MOSFET, i.e., 60mV/decade. Moreover, the SCEs increases the leakage current, while the supply voltage can no longer be scaled down, both of which result in increased power consumption. Along with various SCEs, and reduced channel length, the passive power density approaches the active power density (in magnitude). To mitigate the standby power dissipation, lower OFF-state current (I_{OFF}) is required. However, the leakage current increases exponentially because the SS of MOSFET has a minimum value of 60mV/decade at room temperature. To overcome these flaws, various novel device architectures and materials engineering have been proposed such as multi-gate architectures of MOSFET, new gate dielectric materials, asymmetric channel doping engineering, and much more (Ferain et al, 2011; Kranti et al, 2004). Since MOSFET is employed as a switch in digital applications; thus, the prime requirement for switching applications is steeper ON/OFF transitions, i.e., lower SS and higher current switching ratio, i.e., I_{ON}/I_{OFF} ratio. The lower SS reduces the static power dissipation whereas, the higher I_{ON}/I_{OFF} ratio determines the performance level of the device. However, the variously reported device architectures for MOSFET successfully enhances the I_{ON}/I_{OFF} ratio, but the fundamental limit of MOSFET put constraints on SS and limit SS to 60mV/decade. Thus, the MOSFET has a fundamental limitation on SS to 60mV/decade at room temperature that is primarily offered by its current switching process, i.e., thermionic (temperature dependent) injection of electrons over the energy barrier. This fundamental limit on SS restricts

further scaling of supply voltage below 1V due to the increased leakage current and various SCEs (Abuelma'atti, 2013; Seabaugh & Zhang, 2010).

1.2 SCALING OF MOSFET

Reduction of cost per logic function and per stored bit, and simultaneously increasing the switching speed of logic gates is the key aim of the entire research and development efforts in VLSI electronics. Further, the aim has been achieved and resulted in new generations of microchips having a higher clock frequency than their predecessor and comprising more transistors.

Scaling was first proposed by Dennard et al (Dennard et al, 1974) with the idea of reducing the device without affecting the voltage-current behavior of large devices. Rules of scaling given by him are known as constant field scaling. In constant field scaling, all the dimensions and voltages are reduced by a scaling factor $\kappa(>1)$, that result constant electric field inside the device as those of an original device (Chatterjee et al, 1980; Majima et al, 2001).

Constant voltage scaling and constant field scaling are the commonly used types of scaling. Constant field scaling requires a reduction in the power supply voltage as one decreases the minimum feature size. However, it yields the largest reduction in the power-delay product of a single transistor. Constant voltage scaling is a preferred scaling method since it provides voltage compatibility with older circuit technologies. Increase in electric field with the reduction in the minimum feature length is the disadvantage of constant voltage scaling and it leads to mobility degradation, velocity saturation, lower breakdown voltages, and increased leakage currents. There is another scaling theory, Brew's scaling theory (Brews, 1979), according to which the channel doping concentration in bulk MOSFET's should be increased to alleviate the short-channel effects. The channel length of the MOSFET was around 10 μm when it developed in 1960. Today most of the ICs utilize CMOS technology with channel length around 30 nm.

Scaling-down has the following advantages:

- *With shorter interconnects and smaller transistors, more circuits can be fabricated on to the each silicon wafer. This leads to reduction in cost of circuits.*
- *Smaller transistors and shorter interconnects also lead to reduction in parasitic capacitances which increases the speed of ICs.*
- *When transistor is scaled down, it leads to reduction in power supply voltages as well as power consumption.*

However, downscaling has its own problem at very short gate length (sub-nm range) (Hu et al, 2010). These are:

- *Static and dynamic power consumption.*
- *Overheating and possible evaporation become major concerns.*
- *Increased electric field within the oxide and increased leakage gate-current.*

1.3 SHORT CHANNEL EFFECTS (SCES)

The channel length and width must be reduced for the future design of ULSI to realize high packing densities and cut-off frequencies. Reducing the channel length leads to SCEs, whereas reduction in current drive is obtained owing to sinking the channel width (Chau et al, 2004). To overcome such scaling limitations and realize high-performance MOS transistors, several techniques have been proposed. MOSFET scaling results in increased SCEs, the most pronounced of which is threshold voltage (V_T) roll-off, DIBL, hot carrier effect, mobility degradation and velocity overshoot.

1.3.1 Threshold Voltage (V_{th}) Roll-off

The key parameter that characterizes SCEs is the degradation of V_{th} with decrease in channel length. The change (decrease) in threshold voltage with change (reduction) in gate length is called the “Threshold voltage roll-off”. When the device is reduced to nanoscale regime, the charge distribution in the channel is influenced by the field originating from the source/drain. Thus, the value of threshold voltage in a short channel device decreases from the constant value maintained in a long channel

device. Mathematically, threshold voltage roll-off is the difference between the threshold voltage of a short channel MOSFET and that of a long channel MOSFET.

1.3.2 Drain Induced Barrier Lowering (DIBL)

In 1988, Kit Man Cham et al. (Cham et al, 2012) reported that drain induced barrier lowering (DIBL) results an increment in the leakage current in short channel devices as the drain to source voltage is increased (as shown in **Figure 1.2**). In a short channel MOSFETs, the potential barrier can be controlled by both the drain-to-source voltage (V_{DS}) and the gate-to-source voltage (V_{GS}). When V_{DS} increases, potential barrier in the channel decreases which leads to DIBL. The reduction in the potential barrier eventually allows electron flow between the source and the drain, even if V_{GS} is lower than the threshold voltage. The channel current that flows under these circumstances ($V_{GS}<V_T$) is called the sub-threshold current (Hu et al, 1985).

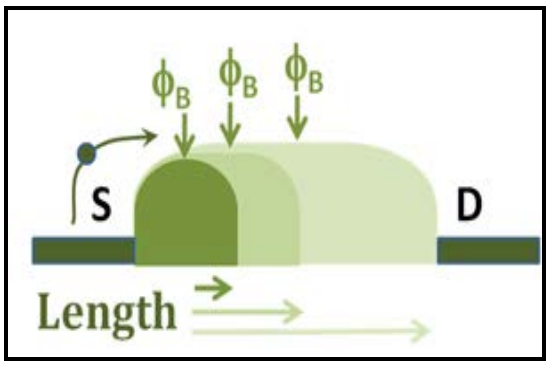


Figure 1.2: Drain Induced Barrier Lowering (Al-Mistarihi et al, 2013).

1.3.3 Hot Carrier Effects (HCEs)

Since device voltages are difficult to scale to arbitrarily small values, electric fields tend to be increased at smaller geometries. Thus, short channel devices reflected various hot carrier effects as shown in **Figure 1.3**, and carrier multiplication and impact ionization may result owing to the reversed biased drain junction. Impact ionization breaks covalent bond and creates holes which contribute to substrate current and some of the holes move to the source, where they lower the source barrier that result in electron injected into p-region from source (Hu et al, 1985).

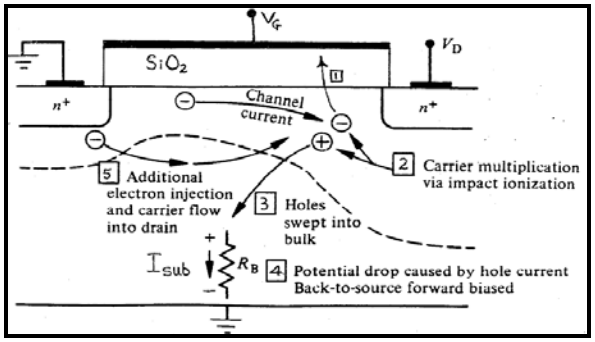


Figure 1.3: Cross-Sectional View of n-channel MOSFET showing Injection of Hot-Carriers due to shortening of channel length (Arora, 1993).

Transport of the energetic electrons over (or tunneling through) the barrier into the oxide is another hot electron effect. These electrons become trapped in the oxide, resulting in the change in the threshold voltage and transfer characteristics of the device (Ogura et al, 1980).

1.4 ENGINEERING SCHEMES TO OVERCOME SCES

Since, SCEs hampered the device operation and reduce device performance; these SCEs should be minimized or eliminated, so that a physical short channel device can preserve the electrical long channel behaviour. There are numerous device engineering schemes (as shown in **Figure 1.4**) that have been reported in literature in last few years to get over these problems.

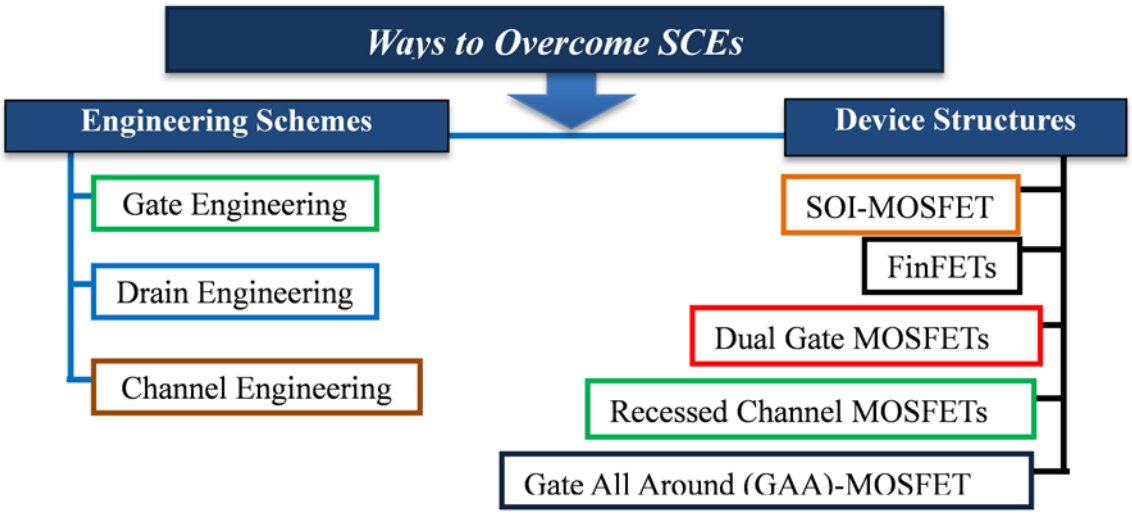


Figure 1.4: Different schemes to alleviate SCEs in nano-scale MOSFET.

1.5 DEVICE CONCEPTS

Continuous increase in the packaging density and the speed of operation of integrated circuits are the major concern for the researchers around the world. Eventually the classical or conventional MOSFET structures have disappeared and new class of devices with new structures using new innovative materials have been introduced. In addition, the recent scaling process has led to arise of novel design concepts for further increase in the integration density.

These concepts span from strained-silicon MOS devices where the silicon channel is replaced by strained silicon to enhance the carrier mobility, to depleted-substrate devices such as FinFETs, single-gate or double-gate silicon on insulator (SOI) devices (Hisamoto et al, 2000), vertical transistors, and even carbon nanotubes (CNTs) (Lin et al, 2011) which represent a completely new device structure.

1.5.1 Silicon on Insulator (SOI)

One can obtain significant reduction of SCEs by sandwiching a fully depleted SOI device (Choi et al, 1999) between the gate electrodes connected together as shown in **Figure 1.5**. The SOI technology dielectrically isolates components and in conjunction with the lateral isolation, reduces various parasitic circuit capacitances, and thus, eliminates the possibility of latch-up failures.

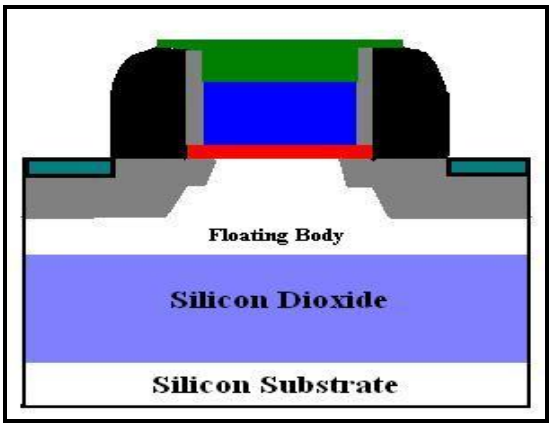


Figure 1.5: Silicon-On-Insulator MOSFET(Choi et al, 1999).

SOI technology offers superior devices with excellent radiation hardness and high device density. In addition, for scaling devices into deep-submicron regime, SOI devices are more suitable with their steeper sub threshold slope which facilitates scaling of the threshold voltage for low-voltage low-power applications.

1.5.2 Dual Gate MOSFET

F. Balestra et.al in 1987 (Balestra et al, 1987) proposed a new structure the "Double-Gate" which appears to be one of the most promising due to the shield-effect played by the double gate (**Figure 1.6**), which strongly reduces drain-induced barrier lowering and minimizes threshold sensitivity to channel length. The main idea of a Double Gate MOSFET is to control the Si channel very efficiently by choosing the Si channel width to be very small and by applying a gate contact to both sides of the channel. This concept helps to suppress short channel effects and leads to higher currents as compared to a MOSFET having only one gate. Main problem with this structure is fabrication, since it requires alignment of the two gates.

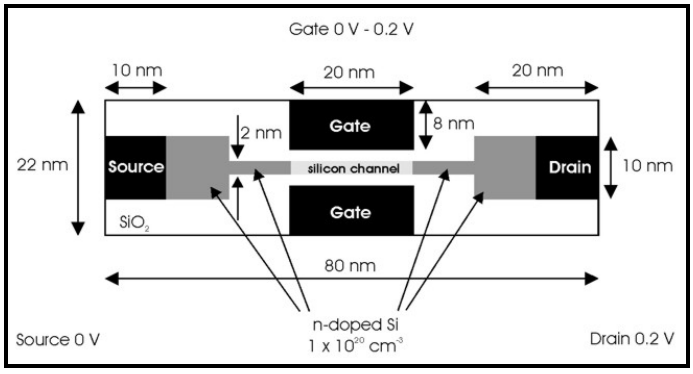


Figure 1.6: Double-Gate MOSFET (Balestra et al, 1987).

1.5.3 Fin FET

FinFET is a three dimensional device in which the channel is built on top of the silicon substrate between the source and drain, called fin. FinFET leads to enhance the current driving capability and reduced leakage current owing to its wrapped channel by gate electrode, so that there can be formed several gate electrodes on each side (Fossum et al, 2003).

Fin-FET offers several advantages such as:

- Low wafer cost
- Low defect density
- No floating body effect
- High heat transfer rate to substrate
- Good process compatibility

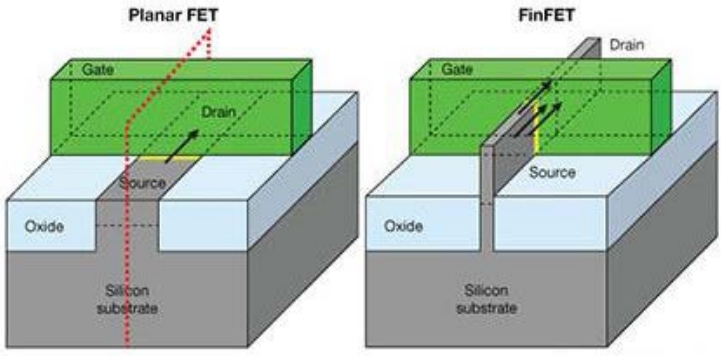


Figure 1.7: Schematic view of both planar MOSFET and FinFETs (Bohr & Mistry, 2011).

1.5.4 Gate-All-Around (GAA) MOSFET

The scaling-down of conventional MOSFET is approaching its limit owing to the SCEs. So, to overcome SCEs, multiple gate MOSFETs were introduced as a replacement. By using more than one gate and creating multiple gate MOSFETs which offers superior control over the channel, results to reduce SCEs and hence leakage current.

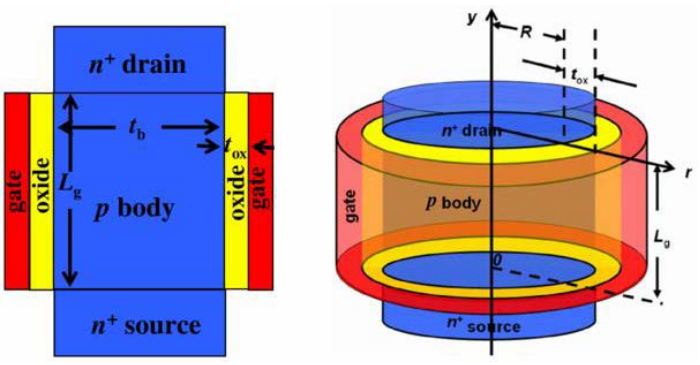


Figure 1.8: Cross-sectional view of cylindrical gate MOSFET with the coordinate system (Jin et al, 2012).

In Gate all around (GAA) structure, channel is surrounded by gate which offers greater controllability over the channel that in turn diminishes the SCEs effectively. Further, GAA MOSFETs offer several advantages such as higher current drivability, mobility enhancement etc., over single gate MOSFET, and other multiple gate MOSFETs. However, GAA MOSFET is difficult to fabricate owing to its non-planar structure which may increase the time and cost. Meanwhile, GAA MOSFETs can be considered as the candidate for future CMOS integration.

1.6 RELIABILITY ISSUES OF CMOS DEVICES

1.6.1 Interface Trap Charges

With strengthening in the complexity and density of VLSI chips, the assessment of the long-term reliability of CMOS devices becomes compulsory. The reliability of MOS devices is very much affected by the quality of interface of semiconductor and oxide. Precisely, the Si-SiO_2 interface may be associated with four types of charges viz. fixed oxide charges, mobile oxide charges, oxide trapped charges and interface states. Moreover, these charges inevitably appear during the fabrication of the MOS devices. Although the number of such charges has been reduced significantly with continuous improvements in fabrication technology, still they cause a substantial degradation in the operation of the device due to the high packing density of transistors in microchips today.

The origin of these interface states are primarily offered by the high electric field present in the channel region for the positive gate and drain bias, that is generated in MOS devices due to scaling of gate length. However, a small fraction of charge carriers gain even large energy (~ 3.2eV for electrons and 4.7eV for holes), that they may surmount the interface of Si-SiO_2 and may penetrate inside the SiO_2 and may constitute the gate leakage current. Among these penetrated charge carriers, few of them may remain trapped in the oxide and if they are still energetic enough, they may subsequently break some of the Si-H or similar weak bonds in the SiO_2. This penetration may translate to a permanent modification of the characteristics of the device and thereby degrades the functioning of integrated circuits. Additionally, the

passage of ionizing radiation in the oxide may also turn to generate the trapped charges in the oxide layer. The electron-hole pair thereby created may recombine or move in the electric field of oxide; such that the generated holes move towards the metallic gate and the electron travels toward the interface of Si and SiO_2. The holes moving towards the metallic gate may be trapped in the oxide and leads to generation of a positive charge in the oxide. Besides, the generation of trapped charges, the ionization radiation may produce new energy levels in the band-gap at Si-SiO_2 interface that may be occupied by the charge carriers depending on the Fermi level position at the interface and the oxide charge will be added/subtracted to the correspondingly charge value (Oldham & McLean, 2003). The most critical factors accountable for the device damage complications are: process induced damage (Poindexter, 1989), radiation-induced damage (Poindexter, 1989), stress-induced damage (Trabzon & Awadelkarim, 1998) and hot carrier induced damage (Naseh et al, 2006).

In the era of sub-100nm, device designing plasma etching used for pattern transfer process may produce electrical and processing damage (falls under the category of stress-induced damage), and thereby damage the Si-oxide interface along with the oxide and consequently degrades the performance, yield, and reliability of the device. Mostly, the interface trap charges are of two types; viz. the acceptor type and donor type interface state. The acceptor type interface state behave as electrically neutral when it is empty, and it comes to be negatively charged when filled with an electron. Whereas, the donor type interface state behave electrically neutral when filled with an electron and turn into positively charged when it is empty (Kumar et al, 2018). Apart from donor/acceptor, a specific interface state is also characterized by (i) the exact energy level in the band-gap i.e. measured in eV from the valence band edge, (ii) its spatial location in the device, for example distance from the source side and (iii) its density i.e. the number of states/cm^2 for discrete states. The position of the Fermi level in the energy band gap accounts for the net charge quantitatively in the respective interface state (Neamen, 2003). It is reported (Neamen, 2003) that the acceptor (donor) states lie in the upper (lower) half of the energy band-gap. Moreover, these interface states act as a fixed positive/negative charge as if in Fermi level and so

the interface state will behave as a negative fixed charge. Similarly, a donor type interface trap acts as a positive fixed charge and thereby in this thesis, these interface traps are accounted as effective positive and negative fixed interface charges.

1.7 RESEARCH GAPS

After learning the literature review, we have found some research gaps that are listed below which we tried to fill through possible solutions.

1. *Ease of fabrication feasibility-a challenging point to obtain using non-planar devices.*

2. *Need of innovative gate material which enhances the overall device performance.*

3. *The fabrication processes may damage the gate oxide as well as the interface of the Si-SiO_2 interface. These defects are the origin of interface trap charges and oxide charges that alters the ideal predicted characteristics. Thus, the device performance must be analyzed in the presence of these default traps to ensure the reliability.*

4. *Design of RF CMOS circuits in real products remains a challenge due to the strong constraints on power consumption. In addition, the issue of noise is still an active area of investigation for amplifiers and receivers for RF communication.*

5. *To run into the perpetual call of transistors with high and low-temperature tolerance desirable in aircraft, space, and automotive technology, temperature affectability over device performance must be analyzed.*

6. *In addition, electronic device especially MOSFETs are used as a sensor, either as a bio-sensor, radiation sensor etc., owing to several advantages. As technology moves towards small devices, new FET based sensor for different specializations are required.*

1.8 POSSIBLE SOLUTIONS

1.8.1 Recessed Channel MOSFET

Recessed Channel (RC) MOSFET is a possible way as it is feasible to fabricate in comparison to non-planar devices.

Recessed Channel (RC) MOSFET is considered as a promising device for suppressing short channel effects (SCEs) and hot carrier effects (HCEs) since the shallow junctions or even negative junctions structure can be fabricated without any increase in the series resistance. These MOSFETs are, hence, good candidates for use in sub-nm regime as shown in **Figure 1.9**. The potential barrier (corner effect) formed at each concave corner, is found to be responsible for suppressing the SCEs, HCEs, and punch-through.

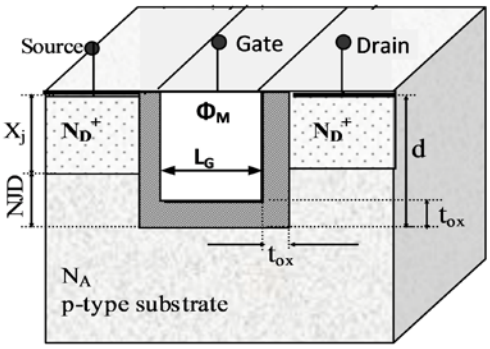


Figure 1.9: Schematic cross-sectional view of Conventional Recessed Channel MOSFET (Chaujar et al, 2008c).

Threshold voltage of the device is increased due to higher potential barriers as the carriers needed high energy to surmount the potential barriers, and results in the carrier velocity degradation with the increase of the concave corner, that will bring about HCE immunity and driving capability degradation. These charge carriers not only surmount the potential barriers, but also have to change their direction when they are travelling from source to drain region and the electric field near the source is smaller in recessed channel. Therefore, the impact ionization generation rate in RC MOSFET is far smaller than that in conventional devices. Low impact ionization rate

brings small substrate and gate current consequentially, which means HCEs immunity in RC MOSFET devices (Chaujar et al, 2008a; b; c) is better than that in planar devices.

Furthermore, it has been also observed that, the hot-carrier effect is strongly suppressed as the concave corner increases (corner effect). When charge carriers surmount the potential barriers, they lose more energy and hence their velocity becomes lower and therefore the HCE diminishes. As the recessed (or trench) depth increases, the potential barriers upsurge, and the channel potential becomes lower. Also, as the recessed depth increases, it shortens the flat portion of the channel. Hence, the path (where the carriers are accelerated) is shortened and the energy gained by the charge carriers is lowered, so the probability of hot carrier becomes smaller and improve HCEs immunity. Studies by Chaujar et.al (Chaujar et al, 2008c), Appenzeller et.al demonstrate that the capability of HCEs immunity in RC MOSFET is intensely influenced by geometric structure. Due to the device structure, corner effect and the electric field distribution in Recessed Channel MOSFETs are influenced strongly, so do the transportation of carriers and the HCEs immunity.

In RC devices, the threshold voltage roll-off is eliminated with the shortness of channel length as of the emergence of corner effect even in sub-nm regions. By taking benefit of the corner effect, threshold voltage shift can be possibly eliminated against channel length variation. To adjust the threshold voltage in RC MOSFET numerous structural parameters, such as junction depths, the concave corner, concave sidewall structure, and the channel doping concentration can be used, while in conventional MOSFETs, only the channel doping concentration can be used. The gate length of the conventional MOSFET is longer than the effective channel length due to the lateral diffusion of the source/drain regions; however, the gate length of the RC MOSFET is shorter than the effective channel length because the junction depths are less than the groove depth. Therefore, RC structure lends itself to higher packing density. This MOSFET design, thus, proves its efficacy for high performance applications where device and hot carrier reliability is a major concern.

The optimization of the structure and technology is, however, important to obtain better gate control and hence, high drain current. The geometry of the device

retained the scaling of MOSFET down to the sub-nm range, should not require too many additional and expensive process steps. This eliminates, for the moment, the novel structures such as gate-all-around transistors, though very good in term of short-channel effects and current drive capabilities.

A. Merits of RC-MOSFET

- ☞ Suppress various SCEs such as Hot-carrier and Punchthrough
- ☞ Less expensive fabrication process

B. Demerits of RC-MOSFET

- ☞ Carriers in the channel now requires more energy to surmount these barriers, which limits its carrier transport efficiency and hence, current driving capability..

1.8.2 Novel Gate Materials

The performance of semiconductor devices such as MOSFET is majorly dependent on its gate controllability over the channel and the gate controllability is dependent on device gate architecture and the material which is deposited on to the gate. Aluminium (Al) is the commonly used gate material in the semiconductor devices and it has some limitations in application perspective.

A. Transparent Conducting Oxides (TCOs)

To enhance the device performance and interdisciplinary applications, conventional gate material is replaced by amorphous transparent conducting oxides (TCOs) and TCOs are electrical conductive materials usually prepared with thin film technology. TCOs are used as transparent electrode for optoelectronic applications in optoelectronic devices such as flat panel display, opto-electrical interfaces, and circuitries. TCO thin films are practically used as transparent electrodes and exhibit average transmittance above 80% in visible region and having resistivity less than of the order of 10^{-3} Ω-cm with higher carrier concentration (in the order of 10^{20} cm^{-3})

and band gap (~3 eV). Most of the TCO are impurity doped ZnOn, In_2O_3 and SnO_2 including some ternary compounds (Minami, 2005). Till now, different TCO thin films consisting of binary compounds (SnO_2, In_2O_3, ZnO, CdO etc.) have been developed with impurity doped ZnO (ZnO:Al and ZnO:Ga), impurity-doped In_2O_3 (In_2O_3:Sn, or ITO) and impurity-doped SnO_2 (SnO_2:Sb and SnO_2:F) films. Some of the reported effective dopants along with their associated binary compound are listed in **Table 1.1** (Minami, 2005).

Table 1.1: TCO for thin film transparent electrodes (Minami, 2005).

Material	Dopant or compound
SnO_2	Sb, F, As, Nb, Ta
In_2O_3	Sn, Ge, Mo, F, Ti, Zr, Hf, Nb, Ta, W, Te
ZnO	Al, Ga, B, In, Y, Sc, F, V, Si, Ge, Ti, Zr, Hf
CdO	In, Sn
$ZnO–SnO_2$	Zn_2SnO_4, $ZnSnO_3$
$ZnO–In_2O_3$	$Zn_2In_2O_5$, $Zn_3In_2O_6$
$In_2O_3–SnO_2$	$In_4Sn_3O_{12}$
$CdO–SnO_2$	Cd_2SnO_4, $CdSnO_3$
$CdO–In_2O_3$	$CdIn_2O_4$
$MgIn_2O_4$	
$GaInO_3$, $(Ga, In)_2O_3$	Sn, Ge
$CdSb_2O_6$	Y
$ZnO–In_2O_3–SnO_2$	$Zn_2In_2O_5–In_4Sn_3O_{12}$
$CdO–In_2O_3–SnO_2$	$CdIn_2O_4–Cd_2SnO_4$
$ZnO–CdO–In_2O_3–SnO_2$	

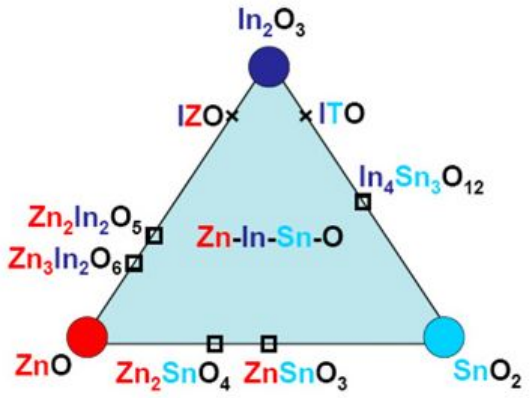


Figure 1.10: TCO semiconductors for thin film transparent electrodes (Minami, 2005).

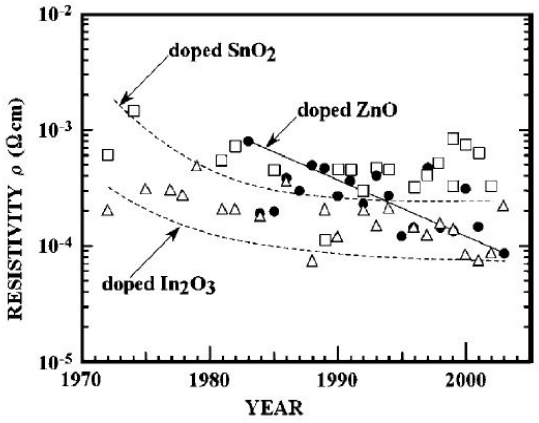


Figure 1.11: Reported resistivity of impurity-doped binary compound TCO films (Minami, 2005).

In addition to binary compounds, ternary compounds such as $CdSnO_3$, Cd_2SnO4, $Zn_2\ SnO_4$, $MgIn_2O_4$, $CdIn_2O_4$, $In_4Sn_3O_{12}$ and $CdSb_2O_6$ have been developed (Chopra et al, 1983; Dawar & Joshi, 1984; Enoki et al, 1992; Minami et al, 1997; Un'no et al, 1993; Yanagawa et al, 1994). These TCO films are easy to design owing to use of multicomponent oxide materials (shown in **Figure 1.10**) for specialized applications and can be controlled by altering the chemical composition (Sato et al, 1993b).

B. Indium Tin Oxide (ITO): In_2O_5Sn

Obtaining lower resistivity of TCO is a major challenge. In recent years, some of the impurity doped binary compound TCO film has been reported with minimum resistivity as shown in **Figure 1.11.** From the reported work as shown in **Figure 1.11,** it is evident that, In_2O_3 doped TCO film i.e., indium tin oxide (ITO) has the lowest resistivity of the order of 10^{-5} Ω-cm as compared to ZnO doped and SnO_2 doped. ITO (In_2O_5Sn) is a solid solution of indium oxide (In_2O_3; 90%) and tin oxide (SnO_2; 10%), transparent and colorless thin film. ITO is the most widely used TCO owing to its electrical conductivity and optical transparency (Stadler, 2012). The electrical properties of ITO with a resistivity of 10^{-5} Ω-cm have been summarized in **Table 1.2**.

Table 1.2: Electrical properties if ITO with a resistivity of 10^{-5} Ω-cm (Minami, 2005).

Resistivity (Ω cm)	Carrier concentration (cm^{-3})	Hall mobility ($cm^2 (V s)^{-1}$)
7.4×10^{-5}	$\sim 1.38 \times 10^{21}$	103
8.9×10^{-5}	1.3×10^{21}	54.1
7.2×10^{-5}	2.5×10^{21}	33.2
9.5×10^{-5}	1.8×10^{21}	40
8.45×10^{-5}	1.38×10^{21}	53.5

ITO and ZnO are the two promising transparent electrodes used in semiconductor devices. ITO is more stable than ZnO for oxidizing atmosphere at high temperature (Sato et al, 1993a). Some characteristics comparison of ITO and ZnO are summarized in **Table 1.3**.

Table 1.3: Comparison of ITO and ZnO (Minami, 2005)

	Doped ZnO	ITO
Low resistivity (Ω cm)	10^{-5}	10^{-5}
Practical resistivity (Ω cm)	$2–3 \times 10^{-4}$	1×10^{-4}
E_g (eV)	3.3	3.7
Index of refraction	2	2
Work function	4.6	4.8–5.0
Cost	Inexpensive	Very expensive
Stability		
Acid solution	<Good (stable)	
Alkali solution	<Good (stable)	
Oxidizing atmosphere at high temperature (or oxygen plasma)	<Good (stable)	
Reducing atmosphere at high temperature (or hydrogen plasma)	Good (stable)>	

1.9 OBJECTIVES OF THESIS

CMOS scaling has been the driving machinery for the ever-increasing number of functionalities and significant miniaturization of the integrated circuits (ICs) enabling

this era of big data and internet of things (IoT). Therefore, there is a need to study comprehensively the physics and applications of new device structure which extend Moore's Law. The present thesis mainly aims to replace the gate metal with transparent conducting material (ITO) that improves device efficiency and reduces short channel effects and hence, it has future in photovoltaic applications such as solar cell, flat panel display etc..

In this thesis, all types of scaling issues mainly HCEs and DIBL of proposed device structure i.e., Transparent Gate Recessed Channel (TGRC) MOSFET have been critically scrutinized and compared with the conventional structures using device simulations obtained using ATLAS 3D device simulator. The analysis exemplified that this device structure has overcome the drawbacks faced by the conventional structures and improves the device performance. Further, a comprehensive examination comprising of RF gain analysis including main FOMs, S-parameters and Noise evaluation, small signal model, linearity and intermodulation, study of device reliability due to trap charges and also at different ambient temperatures. Further the device has been proposed for application as a biosensor and as an x-ray dosimeter.

The entire work in the present thesis is divided into seven chapters based on the following objectives listed below:

1. Analog and linearity performance of the proposed device have been discussed along with the impact of trench depth (Negative Junction Depth (NJD)) and gate length (L_G) shrinking. The improved analog and linearity performance at 5 nm NJD and 20 nm L_G of TGRC-MOSFET makes it suitable for low power linear RF amplifiers as a nano-scaled device.

2. To investigate the reliability issues of the proposed device by considering the effect of interface trap charges (both polarity and density) in terms of static, linearity and intermodulation distortion FOMs. In addition, the influence of ambient temperature (150-300K) along with trap charges on TGRC MOSFET has also been explored with an aim to analyse at which temperature the device is more stable in the presence of interface defects (trap charges).

3. To examine the effectiveness of In_2O_5Sn (ITO) as a gate material on parasitic capacitance which prominently influences the current driving capability and thus, the switching performance? The capacitance dependent parameters such as Transconductance Frequency Product (TFP), Energy Delay Product (EDP) and Gain Bandwidth Product (GBP) are also assessed and reflect its effectiveness in RF amplifiers and receivers.

4. To examine the high frequency performance of the device, the small signal modeling in terms of *S* (scattering) parameters, *Z* (impedance) parameters, *Y* (admittance) parameters, and *h* (hybrid) and to calculate RF FOMs [transit (cut-off) frequency (f_T) and maximum oscillator frequency (f_{MAX})] at microwave frequency has been done. It may provide detailed insight to RF engineers for microwave applications and testing of RF ports.

5. Applications of the proposed device have been explored as an X-Ray dosimeter to detect harmful x-rays and improved its sensitivity in sub-30 nm regime. Thereafter, the device proposed has been used as a biosensor which can sense bio-molecules such as proteins, DNA, glucose or in cancer detection. Also, the main aim is to improve the sensitivity of the sensor compared to previously reported work.

The purpose behind these objectives is to find a new planar device structure with substantially reduced short channel effects that provides an attractive design in view of a system on chip realization, where digital, mixed-signal base band and RF transceiver block would be integrated on a single chip.

1.10 CONTRIBUTION OF THE RESEARCH WORK

The main contribution of the research work listed below:

- First time, In_2O_5Sn (ITO) has been introduced as a gate material on to the Recessed Channel MOSFET at sub-30 nm regime.
- Device reliability has been investigated by considering the effect of interface trap charges (both polarity and density). In addition, the influence of ambient temperature (150-300K) along with trap charges has also been explored.

- Modeling of small signal parameters (*S*, *Z*, *Y*, and *h*) has been performed at microwave frequency.
- First time, the device has been explored as an X-Ray dosimeter to detect harmful x-rays radiation.
- The proposed device has also been explored as a biosensor which can sense bio-molecules such as proteins, DNA, glucose or in cancer detection.

1.11 ORGANIZATION OF THESIS

This thesis is organized into seven chapters to accommodate all the research objectives. Each chapter is organized to be fundamentally self-contained.

Chapter-1 describes the review of the MOSFET basics, scaling issues and short channel effects. The chapter progresses towards need for advanced MOSFET structures such as planer MOSFET and trench MOSFET to extend Moore's and immunity against short channel effects. The architecture of TGRC MOSFET and the device physics considering the advantages of ITO is explained in detail along with the simulation approaches. Further, a detailed description of Gate Electrode Engineering Scheme and fabrication feasibility of RC-MOSFETs with different gate materials is presented and lastly the overall organization of the thesis along with the importance of the research work presented in this thesis.

Chapter-2 explores the analog and linearity performance of Transparent Gate Recessed Channel (TGRC) MOSFET along with the impact of trench depth (Negative Junction Depth (NJD)) and gate length (L_G) shrinking with an aim to achieve a reliable and high performance transistor. Proposed device improves the analog performance in terms of transconductance, device efficiency, output resistance, and gain. Moreover, linearity figure of merits are also enhanced at lower gate bias in TGRC MOSFET in comparison to conventional MOSFET and Conventional Recessed Channel (CRC) MOSFET due to reduced harmonic distortions (g_{m3}). Thus, the improved analog and linearity performance at 5 nm NJD and 20 nm L_G of TGRC-MOSFET makes it suitable for low power linear RF amplifiers as a nano-scaled

device. Thus, these results would serve as a worthy design tool for low power and high performance CMOS circuits.

Chapter-3 explores the reliability issues of the proposed device by considering the effect of interface trap charges (both polarity and density) in terms of static, linearity and intermodulation distortion FOMs. It is found that with the amalgamation of the transparent gate (ITO) on Conventional Recessed Channel (CRC) MOSFET, it exhibits improved immunity against interface trap charges. In addition, the influence of ambient temperature (150-300K) along with trap charges on TGRC MOSFET has also been explored with an aim to analyse at which temperature the device is more stable in the presence of interface defects (trap charges).

Chapter-4 investigates the capacitance-voltage (C-V) analysis and frequency dependent capacitance of In_2O_5Sn (ITO) gate electrode Recessed Channel (TGRC) MOSFET with an aim to examine the effectiveness of In_2O_5Sn as a gate material on parasitic capacitance which prominently influences the current driving capability and thus, the switching performance. Moreover, capacitance dependent parameters such as Transconductance Frequency Product (TFP), Energy Delay Product (EDP) and Gain Bandwidth Product (GBP) are also assessed and found that, TFP increases in comparison to metal gate RC MOSFET owing to a noticeable reduction in parasitic capacitance ($C_{gg}=C_{gs}+C_{gd}$), due to which EDP and GBP also improve considerably and thus reflects its effectiveness in RF amplifiers and receivers. In addition, the effect of parameter variation such as gate length (Lg) and negative junction depth (NJD) of TGRC have also been observed in this chapter, and results reveal that with L_g=20nm and NJD=5nm, TGRC unveils outstanding switching performance which is desirable for low power ULSI applications.

Chapter-5 examines the small signal RF model of Transparent Gate Recessed Channel (TGRC) MOSFET. Small signal model is studied in terms of microwave parameters such as S (scattering) parameters, Z (impedance) parameters, Y (admittance) parameters, and h (hybrid) parameters with an aim to analyse the behaviour of TGRC MOSFET at microwave frequency. It has also been observed that the transit (cut-off) frequency (f_T) and maximum oscillator frequency (f_{MAX}) enhances significantly in TGRC MOSFET owing to the remarkable reduction in

intrinsic capacitances. Results reveal that the proposed device design improves the small signal behaviour and thus, may provide detailed insight to RF engineers for microwave applications and testing of RF ports.

Chapter-6 explores the application of TGRC MOSFET as an X-Ray dosimeter as well as a biosensor. The first part this chapter reports response of N-channel Transparent Gate Recessed Channel (TGRC) MOSFET to X-ray radiation in the 0.5k to 10kRad dose range after irradiation. TCAD simulations for the same have been done to estimate threshold voltage shift in MOSFET with different radiation dosage. An improvement in radiation sensitivity has been found on increasing the oxide thickness from 2nm to 6nm. Results suggest that TGRC-MOSFET can be effectively used as an X-ray dosimeter in the sub 30nm scale. Along with signal amplification and processing circuit, this device can find enormous applicability in clinical and space environment.

In the second part, TGRC MOSFET has been used as a biosensor which comprises a nano-gap cavity for the detection of biomolecules and transparent gate to enhance the overall current efficiency of RC-MOSFET. For the detection of neutral biomolecules, following electrical characteristics were studied: I_{on}/I_{off}, shift in threshold voltage, change in surface potential and hereafter, calculate the sensitivity of the biosensor. In addition, TGRC noise immunity has been evaluated in the presence of biomolecules. Furthermore, the modulation of cavity gap length has also been observed. Overall Analysis reveals that TGRC MOSFET as a bio-sensor exhibits high sensitivity at a very low drain bias. Thus, this proposed biosensor can be used for biosensor applications to diagnose various associated diseases which require lower noise, high speed, low power, and high density.

Chapter-7 summarizes the overall research work illustrated in this thesis along with the concrete conclusions drawn from the results presented. This chapter also discusses about the future scope of the present work and how can be this work extended and used in future for further research directions.

1.12 REFERENCES

Abuelma'atti, M. T. (2013) MOSFET Scaling Crisis and the Evolution of Nanoelectronic Devices: The Need for Paradigm Shift in Electronics Engineering Education. *Procedia-Social and Behavioral Sciences*, 102, 432-437.

Al-Mistarihi, M. F., Rjoub, A. & Al-Taradeh, N. R. (2013) Drain induced barrier lowering (DIBL) accurate model for nanoscale Si-MOSFET transistor, *2013 25th International Conference on Microelectronics (ICM)*. IEEE.

Arora, N. (1993) MOSFET Models for VLSI Circuit Simulation Theory and Practice Springer. *New York*.

Balestra, F., Cristoloveanu, S., Benachir, M., Brini, J. & Elewa, T. (1987) Double-gate silicon-on-insulator transistor with volume inversion: A new device with greatly enhanced performance. *IEEE Electron Device Letters*, 8(9), 410-412.

Bohr, M. & Mistry, K. (2011) Intel's revolutionary 22 nm transistor technology. *Intel website*.

Brews, J. R. (1979) Subthreshold behavior of uniformly and nonuniformly doped long-channel MOSFET. *IEEE Transactions on Electron Devices*, 26(9), 1282-1291.

Cham, K. M., Oh, S.-Y., Moll, J. L., Lee, K. & Vandevoorde, P. (2012) *Computer-aided design and VLSI device development, 53*Springer Science & Business Media.

Chatterjee, P. K., Hunter, W., Holloway, T. & Lin, Y. (1980) The impact of scaling laws on the choice of n-channel or p-channel for MOS VLSI. *IEEE Electron Device Letters*, 1(10), 220-223.

Chau, R., Datta, S., Doczy, M., Doyle, B., Kavalieros, J. & Metz, M. (2004) High-κ/metal-gate stack and its MOSFET characteristics. *IEEE Electron Device Letters*, 25(6), 408-410.

Chaudhry, A. & Kumar, M. J. (2004) Controlling short-channel effects in deep-submicron SOI MOSFETs for improved reliability: a review. *IEEE Transactions on Device and Materials Reliability*, 4(1), 99-109.

Chaujar, R., Kaur, R., Saxena, M., Gupta, M. & Gupta, R. (2008a) On-state and RF performance investigation of sub-50 nm L-DUMGAC MOSFET design for high-speed logic and switching applications. *Semiconductor Science and Technology*, 23(9), 095009.

Chaujar, R., Kaur, R., Saxena, M., Gupta, M. & Gupta, R. (2008b) Solution to CMOS technology for high performance analog applications: GEWE-RC MOSFET, *Advanced Optoelectronic Materials and Devices, 2008. AOMD 2008. 2nd National Workshop on*. IEEE.

Chaujar, R., Kaur, R., Saxena, M., Gupta, M. & Gupta, R. (2008c) TCAD assessment of gate electrode workfunction engineered recessed channel (GEWE-RC) MOSFET and its multilayered gate architecture—part I: hot-carrier-reliability evaluation. *Electron Devices, IEEE Transactions on*, 55(10), 2602-2613.

Choi, Y.-K., Asano, K., Lindert, N., Subramanian, V., King, T.-J., Bokor, J. & Hu, C. (1999) Ultra-thin body SOI MOSFET for deep-sub-tenth micron era, *Electron Devices Meeting, 1999. IEDM'99. Technical Digest. International*. IEEE.

Chopra, K., Major, S. & Pandya, D. (1983) Transparent conductors—a status review. *Thin solid films*, 102(1), 1-46.

Dawar, A. & Joshi, J. (1984) Semiconducting transparent thin films: their properties and applications. *Journal of Materials Science*, 19(1), 1-23.

Dennard, R. H., Gaensslen, F. H., Rideout, V. L., Bassous, E. & LeBlanc, A. R. (1974) Design of ion-implanted MOSFET's with very small physical dimensions. *IEEE Journal of Solid-State Circuits*, 9(5), 256-268.

Enoki, H., Nakayama, T. & Echigoya, J. (1992) The Electrical and Optical Properties of the ZnO-SnO2 Thin Films Prepared by RF Magnetron Sputtering. *physica status solidi (a)*, 129(1), 181-191.

Ferain, I., Colinge, C. A. & Colinge, J.-P. (2011) Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors. *Nature*, 479(7373), 310.

Fossum, J., Chowdhury, M., Trivedi, V., King, T.-J., Choi, Y.-K., An, J. & Yu, B. (2003) Physical insights on design and modeling of nanoscale FinFETs, *Electron Devices Meeting, 2003. IEDM'03 Technical Digest. IEEE International*. IEEE.

Heyns, M. & Tsai, W. (2009) Ultimate scaling of CMOS logic devices with Ge and III–V materials. *Mrs bulletin*, 34(7), 485-492.

Hisamoto, D., Lee, W.-C., Kedzierski, J., Takeuchi, H., Asano, K., Kuo, C., Anderson, E., King, T.-J., Bokor, J. & Hu, C. (2000) FinFET-a self-aligned double-gate MOSFET scalable to 20 nm. *IEEE Transactions on Electron Devices*, 47(12), 2320-2325.

Hu, C., Tam, S. C., Hsu, F.-C., Ko, P.-K., Chan, T.-Y. & Terrill, K. W. (1985) Hot-electron-induced MOSFET degradation—Model, monitor, and improvement. *IEEE Transactions on Electron Devices*, 32(2), 375-385.

Hu, L., Kim, H. S., Lee, J.-Y., Peumans, P. & Cui, Y. (2010) Scalable coating and properties of transparent, flexible, silver nanowire electrodes. *ACS nano*, 4(5), 2955-2963.

Jin, X., Liu, X., Wu, M., Chuai, R., Lee, J.-H. & Lee, J.-H. (2012) A continuous current model of ultra-thin cylindrical surrounding-gate inversion-mode Si nanowire nMOSFETs considering a wide range of body doping concentration. *Semiconductor Science and Technology*, 28(1), 015002.

Kranti, A., Chung, T. M., Flandre, D. & Raskin, J.-P. (2004) Laterally asymmetric channel engineering in fully depleted double gate SOI MOSFETs for high performance analog applications. *Solid-State Electronics*, 48(6), 947-959.

Kumar, A., Tripathi, M. & Chaujar, R. (2018) Reliability Issues of In2O5Sn Gate Electrode Recessed Channel MOSFET: Impact of Interface Trap Charges and Temperature. *IEEE Transactions on Electron Devices*, 65, 860-866.

Lin, S., Kim, Y.-B. & Lombardi, F. (2011) CNTFET-based design of ternary logic gates and arithmetic circuits. *IEEE transactions on nanotechnology*, 10(2), 217-225.

Majima, H., Saito, Y. & Hiramoto, T. (2001) Impact of quantum mechanical effects on design of nano-scale narrow channel n-and p-type MOSFETs, *Electron Devices Meeting, 2001. IEDM'01. Technical Digest. International*. IEEE.

Minami, T. (2005) Transparent conducting oxide semiconductors for transparent electrodes. *Semiconductor Science and Technology*, 20(4), S35-S44.

Minami, T., Takeda, Y., Takata, S. & Kakumu, T. (1997) Preparation of transparent conducting In4Sn3O12 thin films by DC magnetron sputtering. *Thin Solid Films*, 308, 13-18.

Moore, G. E. (1975) Progress in digital integrated electronics, *Electron Devices Meeting*.

Naseh, S., Deen, M. J. & Chen, C.-H. (2006) Hot-carrier reliability of submicron NMOSFETs and integrated NMOS low noise amplifiers. *Microelectronics Reliability*, 46(2-4), 201-212.

Neamen, D. A. (2003) *Semiconductor physics and devices: basic principles*McGraw Hill.

Ogura, S., Tsang, P. J., Walker, W. W., Critchlow, D. L. & Shepard, J. F. (1980) Design and characteristics of the lightly doped drain-source (LDD) insulated gate field-effect transistor. *IEEE Transactions on Electron Devices*, 27(8), 1359-1367.

Oldham, T. R. & McLean, F. (2003) Total ionizing dose effects in MOS oxides and devices. *IEEE Transactions on Nuclear Science*, 50(3), 483-499.

Poindexter, E. H. (1989) MOS interface states: overview and physicochemical perspective. *Semiconductor Science and Technology*, 4(12), 961.

Sato, H., Minami, T., Takata, S., Miyata, T. & Ishii, M. (1993a) Low temperature preparation of transparent conducting ZnO: Al thin films by chemical beam deposition. *Thin Solid Films*, 236(1-2), 14-19.

Sato, H., Minami, T., Takata, S. & Yamada, T. (1993b) Transparent conducting p-type NiO thin films prepared by magnetron sputtering. *Thin solid films*, 236(1-2), 27-31.

Seabaugh, A. C. & Zhang, Q. (2010) Low-voltage tunnel transistors for beyond CMOS logic. *Proceedings of the IEEE*, 98(12), 2095-2110.

Stadler, A. (2012) Transparent conducting oxides—an up-to-date overview. *Materials*, 5(4), 661-683.

Trabzon, L. & Awadelkarim, O. (1998) Damage to n-MOSFETs from electrical stress relationship to processing damage and impact on device reliability. *Microelectronics Reliability*, 38(4), 651-657.

Un'no, H., Hikuma, N., Omata, T., Ueda, N., Hashimoto, T. & Kawazoe, H. (1993) Preparation of MgIn2O4-X thin films on glass substrate by RF sputtering. *Japanese journal of applied physics*, 32(9A), L1260.

Yanagawa, K., Ohki, Y., Omata, T., Hosono, H., Ueda, N. & Kawazoe, H. (1994) Preparation of Cd1− x Y x Sb2O6 thin film on glass substrate by radio frequency sputtering. *Applied physics letters*, 65(4), 406-408.

2

CHAPTER

Analog and Linearity Performance of Transparent Gate Recessed Channel (TGRC) MOSFET for High Performance Applications

- *In this chapter, analog and linearity performance of Transparent Gate Recessed Channel (TGRC) MOSFET have been discussed along with the impact of trench depth (Negative Junction Depth (NJD)) and gate length (L_G) shrinking with an aim to achieve a high performance transistor.*
- *It is found that device enhances the I_{ON} by 38% and thereby improves the analog performance in terms of transconductance, device efficiency, output resistance, and gain.*
- *Moreover, linearity figure of merits are also enhanced at lower gate bias in TGRC MOSFET in comparison to conventional devices due to reduced harmonic distortions (g_{m3}).*
- *Consequently, improved analog and linearity performance at 5 nm NJD and 20 nm L_G of TGRC-MOSFET makes it suitable for low power linear applications. Thus, these results would serve as a worthy design tool for low power and high performance CMOS circuits.*

2.1 INTRODUCTION

Continuous downscaling of MOSFET dimensions into sub-nm regime leads to undesirable effects such as Short channel effects (SCEs), leakage current, parasitic capacitances etc. resulting in poor device performance and loses the control over gate thereby affecting the analog performance of device such as transconductance, device efficiency, gain etc. Moreover, for RFIC designing and high-frequency applications, CMOS devices are required with high gain and low intermodulation distortion to sustain linear operations when working with a weak signal. In modern communication systems, a high linearity is desired so as to exhibit less distortion. Intermodulation (IM) may induce when the system gives nonlinearity performance and generate different frequency signal at outputs compared to input signal frequency. This kind of interference may fall into the band of interest and distorted the desired output (Razavi & Behzad, 1998). However, sub-nm MOSFET exhibit linear relation but short channel effects (SCEs) hinders its linearity.

To overcome such scaling problems, various device engineering schemes (gate, channel and drain engineering, etc.) and numerous device structures such as multi-gate MOSFET by Barsan in 1981 (Barsan, 1981), SOI MOSFET by An et al. in 2003 (An et al, 2003), Conventional Recessed Channel (CRC) MOSFET by Chaujar et al. in 2008 (Chaujar et al, 2008b), GAA MOSFET by Auth et al. in 1997 (Auth & Plummer, 1997), and Silicon Nanowire MOSFET by Gupta et al. in 2015 (Gupta et al, 2015) etc., have already been reported in the literature. Among them, RC-MOSFET is most promising for extending the scaling limit of conventional CMOS technology due to tremendous gate controllability, lessened SCEs and most importantly the ease of fabrication feasibility (Veeraraghavan & Fossum, 1989). In CRC-MOSFET, two potential barrier are created at the two corners (Chaujar et al, 2008a) owing to higher field lines due to which electrons are now required more energy to cross these barriers. Consequently, these barriers bounds device transport efficiency and thus, current driving capability (I_{on}) reduced. Thus, there is a need of integration of engineering schemes onto RC MOSFET to enhance the current driving capability. Hence, gate metal engineering scheme is incorporated by some optically transparent

and electrically conducting oxides (TCO). TCO is used for different applications in electronic devices due to various properties such as conductivity, thermal stability, transparency, mechanical durability, chemical durability, cost and toxicity (D. J. Rogers, 2010). Among all the TCO, indium tin oxide (ITO) has the highest conductivity and very good transparency as well so; it can be used as electrode material in flat panel display.

Therefore, in this work for the first time analog and linearity/harmonic distortions of TGRC-MOSFET has been studied and concurrently compared with CRC MOSFET in terms of I_{on}, transconductance, device efficiency, intrinsic gain and Linearity FOMs such as Voltage Intercept Point (VIP2, VIP3), IIP3, and Distortions (IMD3, HD3) using ATLAS 3D device simulator (SILVACO, 2011). In addition, effectiveness of geometry dependent parameters such as gate length (L_G) and recessed channel length (NJD) are also examined with an aim to optimize the device parameters so that TGRC MOSFET can be used as highly linear amplifiers with low distortions in communication systems.

2.2 DEVICE DESIGN AND ITS DESCRIPTION

Figure 2.1 shows the simulated 3D device structure of TGRC-MOSFET. The source and drain region is highly doped with n-type impurity of 5×10^{19} cm^{-3}, the substrate is

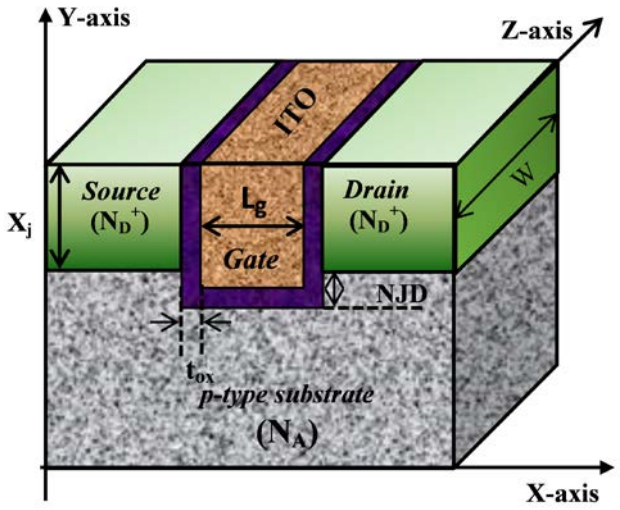


Figure 2.1: 3-D device structure of TGRC-MOSFET (Kumar, 2017; Kumar et al, 2016).

doped with p-type impurity of 1×10^{17} cm^{-3} and thick oxide layer t_{ox} of 2.0 nm is embodied in it as shown in **Figure 2.1**. Negative Junction Depth (NJD) is taken as 10 nm. Gate workfunction of TGRC-MOSFET (Φ_{ITO}) is 4.7eV and for CRC-MOSFET, it is 4.4eV. To equally analyze the device performances, both the devices (CRC and TGRC MOSFET) are optimized to have the similar threshold voltage, i.e., 0.3V by adjusting the substrate doping. For this analysis, all the junctions of the device structure are assumed to be abrupt; the doping profiles are uniform, and the biasing conditions are considered at room temperature (T=300K). Further, to obtain the numerical solutions, two numerical techniques Gummel and Newton have been considered (SILVACO, 2011) to obtain better convergence. Gate bias (V_{gs}) and drain bias is 0.7 V and 0.5V respectively in all cases unless stated otherwise.

2.3 SIMULATION METHODOLOGY AND CALIBRATION

As we were considering a nanoscale MOSFET, the size of mesh nearly 0.003 or 0.004 units in the x and y-direction while 0.02 unit in z direction near the channel and in the active regions has been selected for more precise calculations (Rahimian & Orouji, 2013). The electron and hole currents are calculated by Poisson's equation and the continuity equations. All the simulations are based on the inversion layer Lombardi CVT mobility model to permit one to take account of carrier-carrier scattering, carrier velocity saturation, the influence of the vertical electric field and carrier diffusion at the interface. Auger recombination model and Shockley-Read–Hall (SRH) for minority carrier recombination were used. Further, the hydrodynamic energy transport model comprising of the continuity equations and momentum transport equations have also been used (SILVACO, 2011). The equations (from 2.1 to 2.6) and models utilized are listed below.

1. **Poisson's equation**

$$div(\varepsilon\nabla\varphi) = -\rho \tag{2.1}$$

Where ε is local permittivity; φ is electrostatic potential and ρ is local space charge density.

2. **Current continuity equation**

For Holes,

$$\frac{\partial p}{\partial t} = \frac{1}{q} div\vec{J}_p + G_p - R_p \tag{2.2}$$

For Electrons,

$$\frac{\partial n}{\partial t} = \frac{1}{q} div\vec{J}_n + G_n - R_n \tag{2.3}$$

Where, $\vec{J}_p$ and $\vec{J}_n$ hole and electron current density respectively; G_p and G_n are the generation rate for holes and electrons; R_p and R_n is the recombination rate for holes and electrons respectively.

3. Recombination

3.1 SRH (Shockley Read Hall)

$$R_{SRH} = \frac{pn - n_{ie}^2}{\tau_p\left[n + n_{ie}e^{(-(E_{TRAP}/kT_L))}\right] + \tau_n\left[p + n_{ie}e^{(-(E_{TRAP}/kT_L))}\right]} \tag{2.4}$$

Where, E_{TRAP}, change between the trap energy level and the intrinsic Fermi level; τ_n and τ_p, and are the electron lifetime and hole lifetimes, respectively.

3.2 Auger recombination

$$R_{Auger} = AUGN\left(pn^2 - nn_{ie}^2\right) + AUGP\left(np^2 - pn_{ie}^2\right) \tag{2.5}$$

AUGN and AUGP are user-definable and AUGN=8.3×10^{-32} cm^6/s, AUGP=1.8×10^{-31} cm^6/s.

4. Parallel electric-field-dependent mobility

$$\mu(E) = \mu_0\left[\frac{1}{1+(\mu_0 E/\upsilon_{sat})^{\beta}}\right]^{1/\beta} \tag{2.6}$$

Here, E is the parallel electric field and μ_0 is low-field mobility. The β parameter is user-definable in the mobility statement.

Physical Model parameters which are used in device simulation have been calibrated according to the experimental results (Appenzeller et al, 2002). In order to authenticate the simulations results, the data has been drawn-out (Appenzeller et al, 2002) for 36 nm groove MOSFET and then plotted as shown in **Figure 2.2**. It is evident from the figure that simulated results are in good agreement with the experimental results in sub-40 nm groove MOSFET thus validating the simulation models.

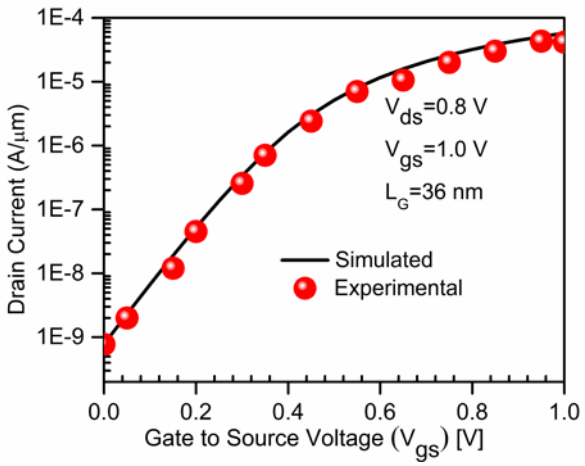


Figure 2.2: Calibrated transfer characteristics of recessed channel MOSFET (36 nm gate length) with experimental (Appenzeller et al, 2002) and simulation data (Kumar, 2017; Kumar et al, 2016).

2.4 FABRICATION FEASIBILITY

The fabrication feasibility of TGRC-MOSFET is shown in **Figure 2.3**. The groove MOSFET has already been fabricated (Appenzeller et al, 2002) with a 36nm groove gate and (Xiao-Hua et al, 2006) fabricated a 140 nm groove gate MOSFET. Thus, the TGRC MOSFET can be fabricated using the above device design schemes, in which the benefits of transparent gate engineering scheme have been combined with groove gate for accomplishing improved characteristics.

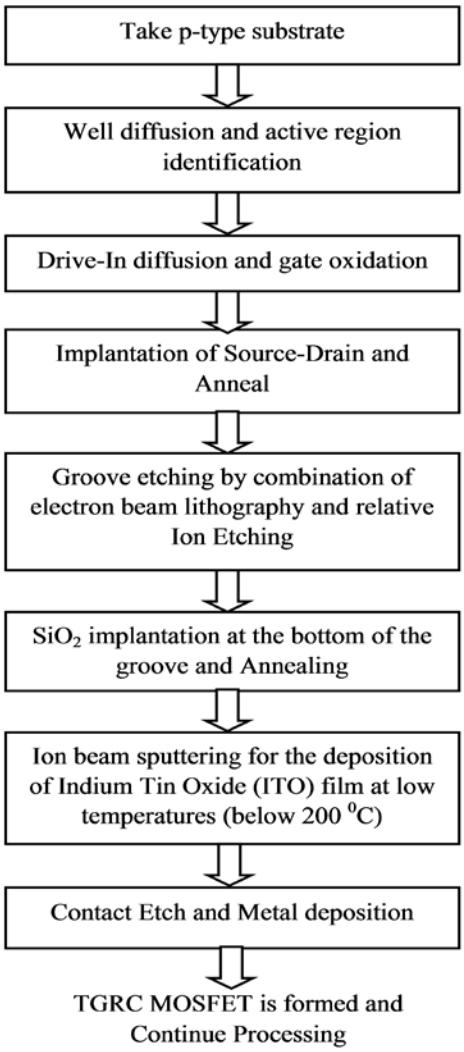


Figure 2.3: Process flow of TGRC MOSFET(Kumar, 2017).

2.5 RESULTS AND DISCUSSION

2.5.1 Analog Performance

This subsection describes and subsequently compared the analog performance of TGRC, CRC, and conventional MOSFET. Performances are studied in terms of transfer characteristics (I_{ds}/V_{gs}), transconductance (g_m), device efficiency (g_m/I_{ds}) and intrinsic gain (g_m/g_d). Transfer characteristics of Conventional, CRC, and TGRC-MOSFET, are shown in **Figure 2.4(a)** and it is depicted that the current driving capability of conventional and CRC-MOSFET is approximately same, but TGRC-MOSFET shows higher current driving capability.

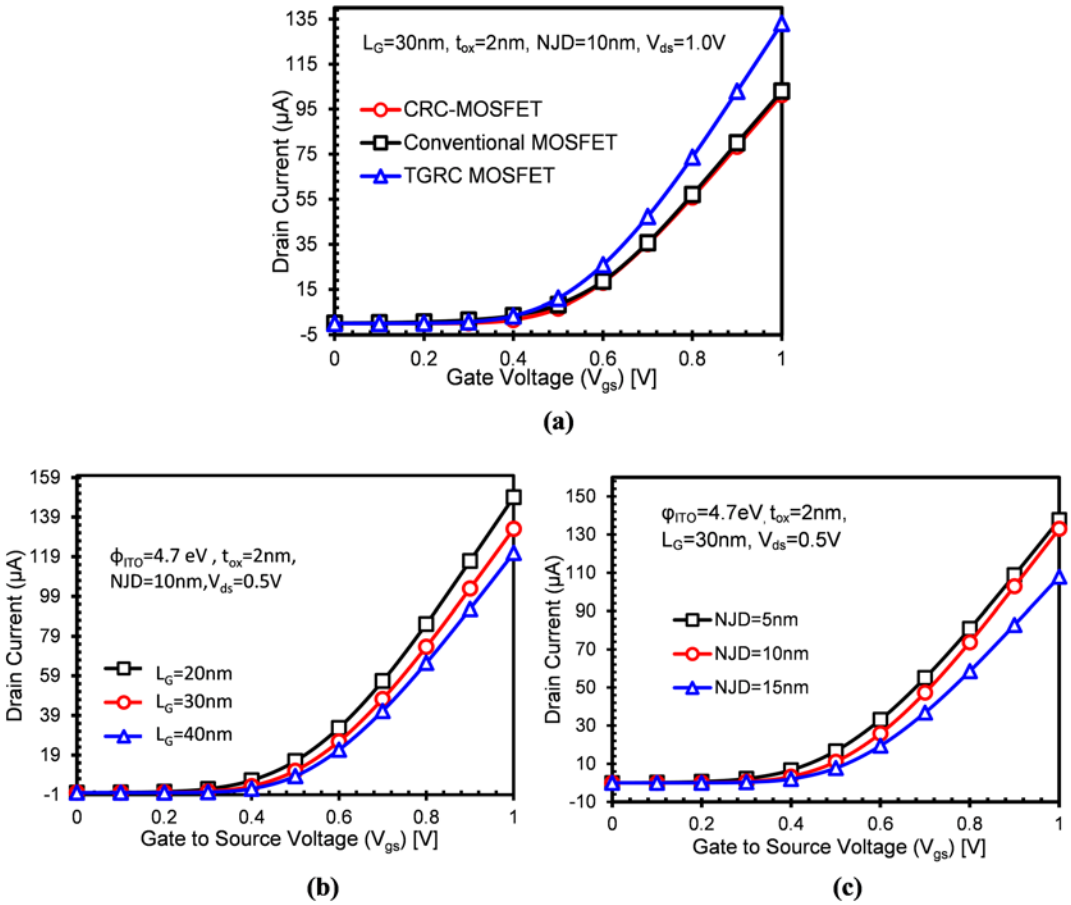


Figure 2.4: (a) Drain current variations for TGRC-MOSFET, CRC-MOSFET, and Conventional MOSFET. (b) Drain current at different L_G. (c) Drain current variations at different NJDs as a function of applied V_{gs} (Kumar, 2017).

This enhancement is due to the incorporation of ITO which reduces electric field near the drain side (Kumar et al, 2015) and thereby improves carrier efficiency resulting in enhancement in drain current by 35%. In addition, the effect of technology variations of TGRC-MOSFET such as L_G and NJD is also observed on transfer characteristics. It is found as the L_G is scaled down from 40 nm to 20 nm, the drain current (I_{ON}) increases significantly as clearly shown in **Figure 2.4(b)**. This increment is due to the reduction of the gate length and hence, now the charge carriers needed less time to reach drain from the source.

Further, by varying the value of NJD, which greatly affects the performance of RC MOSFET (Chaujar et al, 2009), the current driving capability of TGRC is further improved due to the increment of charge carriers travelling from source to drain if

NJD reduces as shown in **Figure 2.4(c)**. There is a limitation in the reduction of NJD and it should not be zero or less; if it is, then SCEs arises. Also, the transconductance increases with increase in gate voltage, and it is more prominent in TGRC-MOSFET as shown in **Figure 2.5(a)** due to TCO at the gate in place of metal which gives high linearity performance and linearity is proportional to transconductance (Kim et al, 2004). The effect gate length variation on transconductance is also observed in TGRC-MOSFET and found that if the gate length shrinks from 40 nm to 30 nm, then

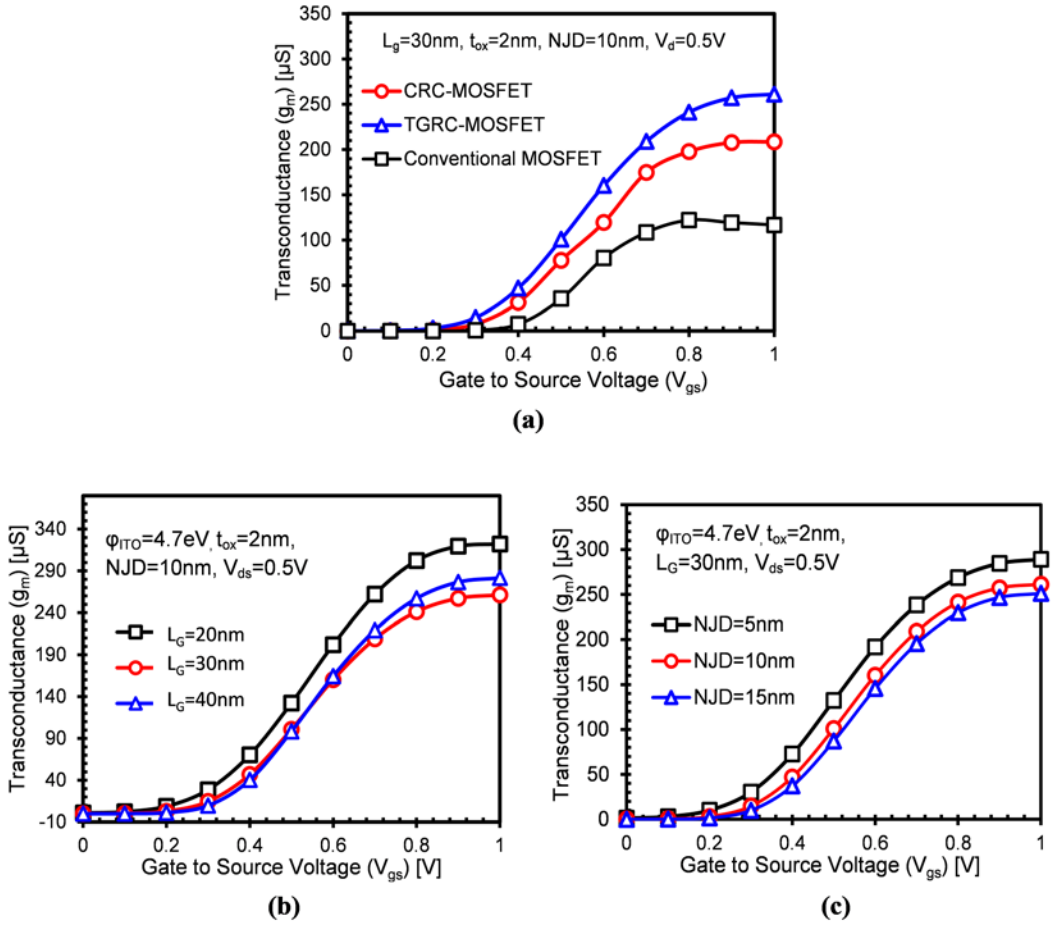


Figure 2.5: (a) Variations of g_m for TGRC-MOSFET, CRC-MOSFET, and Conventional MOSFET, (b) Variation of g_m at different L_G, (c) Variation of g_m at various NJDs as a function of applied V_{gs} (Kumar, 2017).

a very small reduction (by 7.1%) in transconductance is observed while, a major increment (by 23.37%) is observed when gate length reduces from 30 nm to 20 nm as evident from **Figure 2.5(b)**. **Figure 2.5(c)** reflects the effect of technology variation on transconductance in terms of different NJDs and it is found that transconductance

is more prominent which gives high linearity performance at 5nm NJD while it degrades if NJD increases to 10 nm and 15 nm. Thus, improved analog performance of TGRC-MOSFET at scaled dimensions make it suitable for 22 nm node technology (Iwai, 2009) as per ITRS (International Technology Roadmap for Semiconductor) (Jeong & Kahng, 2009).

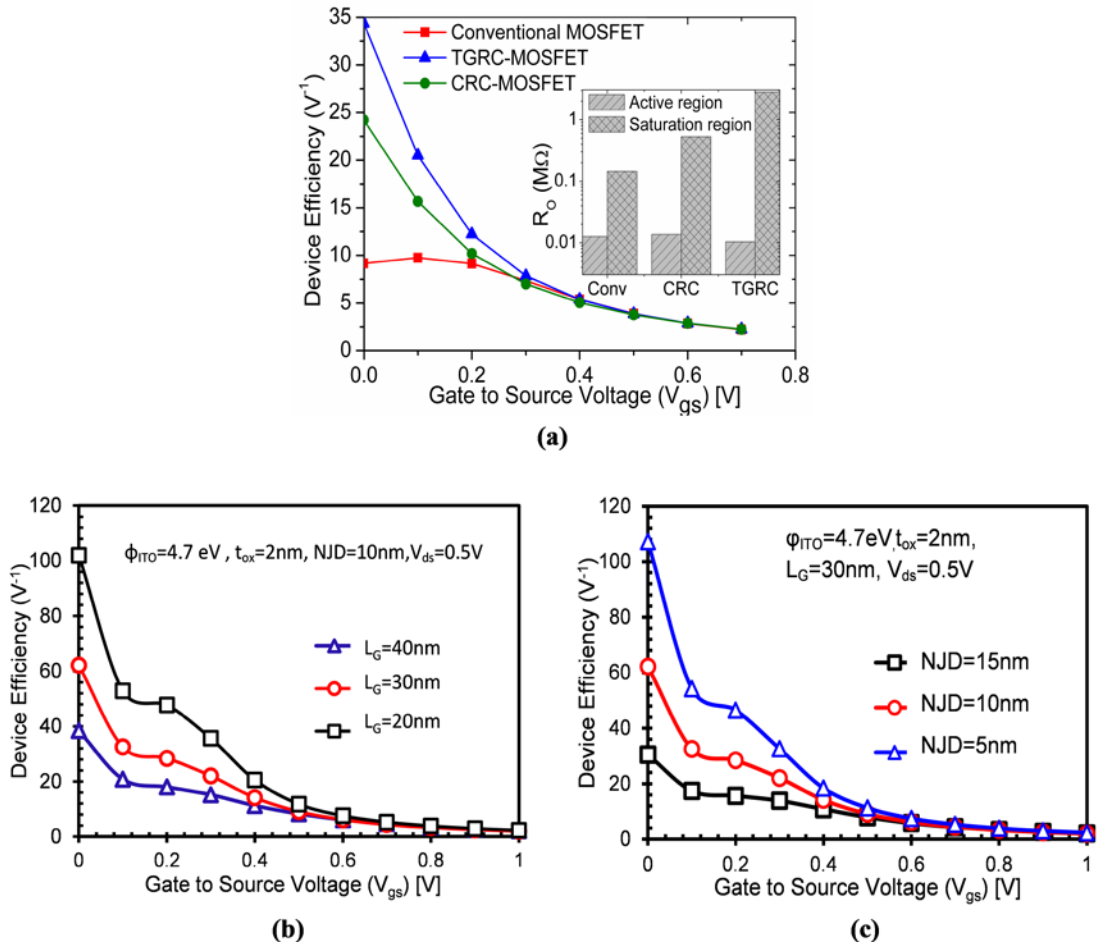


Figure 2.6: (a) Variations of Device Efficiency for TGRC-MOSFET, CRC-MOSFET, and Conventional MOSFET. Inset: Output resistance. (b) Variation of Device Efficiency at different L_G, (c) Variation of Device Efficiency at various NJDs as a function of applied V_{gs} (Kumar, 2017).

The transconductance to the current ratio (g_m/I_d) or device efficiency and output resistance have been evaluated for three different devices (Conventional, CRC, and TGRC MOSFET) as depicted in **Figure 2.6(a)**. Device efficiency is an important parameter in the design of analog circuits, which offers the measure of efficiency to

convert power into speed. It is evident from **Figure 2.6(a)** that the device efficiency is higher in TGRC-MOSFET as compared to conventional and CRC MOSFETs due to increase in g_m in comparison to I_d, which overall enhances g_m/I_d. The output resistance (R_o) of a MOSFET is the inverse of the output conductance. R_o is low in active region while high in the saturation region in TGRC as compared to conventional counterparts (shown in **Figure 2.6(a)** inset). The device efficiency further increases by 63% and 61.29% if the gate length shrinks from 40 nm to 30 nm and 30 nm to 20 nm respectively in TGRC-MOSFET, as shown in **Figure 2.6(b)**. In addition, in technology variation, the effect of NJD variation on device efficiency is also perceived for TGRC-MOSFET (shown in **Figure 2.6(c)**). It is evident from **Figure 2.6(c)** that the reduction in NJD enhances the device efficiency by 78.33% if NJD is scaled to 5 nm.

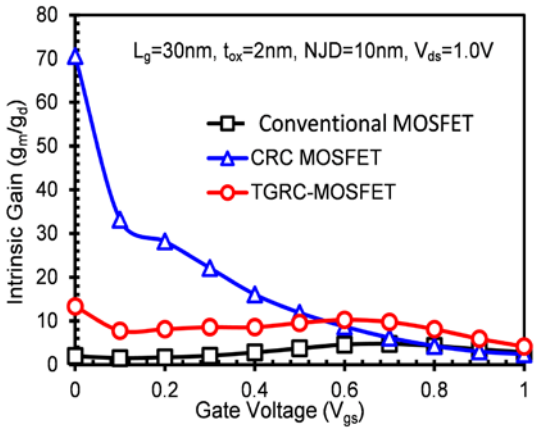


Figure 2.7: Variations of Intrinsic Gain as a function of applied V_{gs} for TGRC-MOSFET, CRC-MOSFET, and Conventional MOSFET (Kumar, 2017).

Further, the intrinsic gain which is one of the important characteristic of MOSFET is defined as the ratio of transconductance (g_m) to output conductance (g_d) (Wang et al, 2007). For better performance, intrinsic gain should be as high as possible and it is evident from **Figure 2.7** that the intrinsic gain is lower in subthreshold region (where device is off) and inactive region, and the intrinsic gain increases in TGRC architecture in comparison to conventional and CRC MOSFET. Thus, TGRC-MOSFET shows promising analog performance for ULSI in comparison to conventional and CRC MOSFET.

2.5.2 Intermodulation and Linearity Performance

A. Linearity Performance

In this sub-section, the linearity of our proposed device is studied and simultaneously compared with its conventional counterparts. Thereafter, technology variations in terms of gate length and NJD have also been studied with an aim to analyze the linearity performance of TGRC at scaled dimensions. The performance metrics used in this analysis are VIP2, VIP3, IIP3, and 1-dB Compression Point. VIP represents the amplitude of the input signal at which the amplitude of the analysed harmonic is equal to the amplitude of the fundamental signal (Cerdeira et al, 2004). VIP2 defined as the extrapolated input voltage at which first and second-order harmonic voltages are equal, and VIP3 defined as the extrapolated input voltage at which first and third-order harmonic voltages are equal. shown in equation (2.7) and (2.8) (Chaujar et al, 2009).

$$VIP2 = 4\frac{g_{m1}}{g_{m2}} \tag{2.7}$$

$$VIP3 = \sqrt{24 \times g_{m1} / g_{m3}} \tag{2.8}$$

Where $g_{m1} = \frac{\partial I_d}{\partial V_{gs}}$ and $g_{m2} = \frac{\partial^2 I_d}{\partial V^2_{gs}} \cdot g_{m3} = \frac{\partial^3 I_d}{\partial V^3_{gs}}$

Figure 2.8(a) reflects the variation of VIP2 w.r.t. the V_{gs} for TGRC-MOSFET and it is also compared with conventional MOSFET and CRC-MOSFET. For higher linearity and lower distortion operation the value of VIP2 should be higher. From **Figure 2.8(a)**, it is analysed that the TGRC device resembles to a higher value of VIP2 by 22.3% and 8.49% as compared to the conventional and CRC designs respectively, which is only due to the incorporation of ITO as a TCO in the TGRC design. The variation of VIP2 w.r.t. applied gate to source voltage for three different gate lengths of TGRC-MOSFET as shown in **Figure 2.8(b)**, and it is found that when the gate length shrinks from 40 nm to 30 nm and from 30 nm to 20 nm, then VIP2 increases which reflect higher value at 20 nm gate lengths. Thus, 20nm TGRC architecture shows higher linearity performance. Similarly, by scaling down the NJD

to 5 nm, TGRC shows the higher value of VIP2 owing to reduce SCEs, improves g_m and thus VIP2 as shown in **Figure 2.8(c)**.

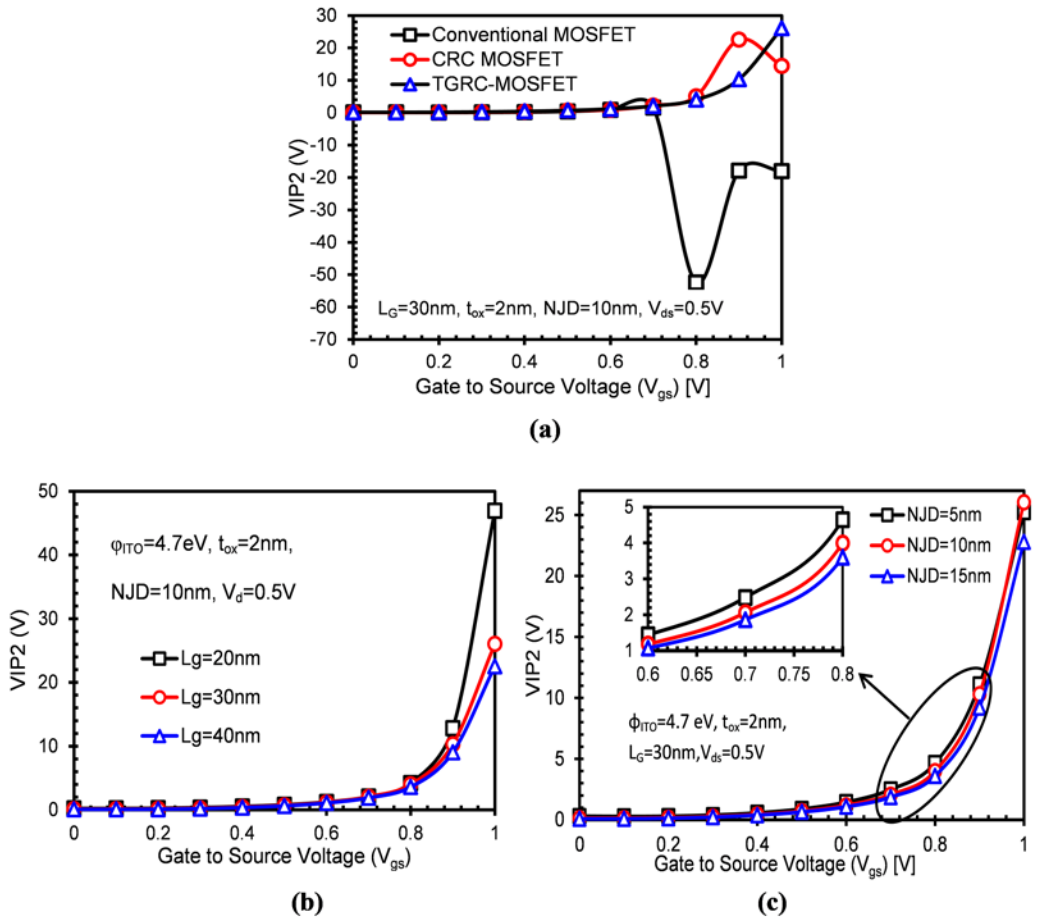


Figure 2.8: (a) Variations of VIP2 for TGRC-MOSFET, CRC-MOSFET, and Conventional MOSFET. (b) Variation of VIP2 at different L_G. (c) Variation of VIP2 at different NJDs as a function of applied V_{gs} (Kumar, 2017).

Figure 2.9(a) reflects the variation of VIP3 w.r.t. the V_{gs} for TGRC, CRC, and conventional MOSFETs. VIP3 peak is perceived at low gate bias (0.45V) in TGRC architecture which is higher by 37.5%, 17.8% compared to conventional and CRC MOSFETs respectively, owing to ITO as a transparent gate design which enhances carrier velocity and thus transconductance. VIP3 peak is further enhanced by scaling down the gate length to 20 nm as clearly evident from **Figure 2.9(b)**. This increase is due to higher g_m (see **Figure 2.5(b)**). Similarly, if NJD is scaled down to 5 nm from 15 nm, VIP3 peak increases significantly as reflected in **Figure 2.9(c)**, thus, it signifies that scaled TGRC-MOSFET exhibit high linearity.

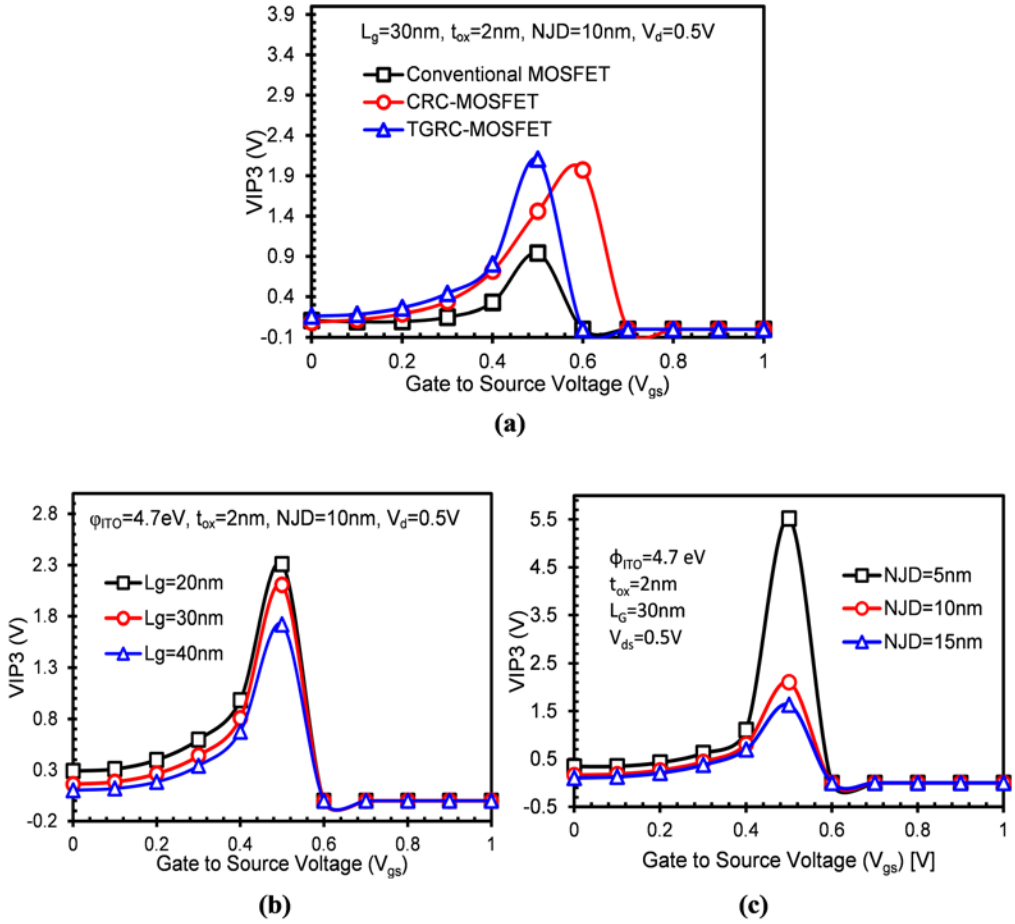


Figure 2.9: (a) Variations of VIP3 for TGRC-MOSFET, CRC-MOSFET, and Conventional MOSFET. (b) Variation of VIP3 at different L_G. (c) Variation of VIP3 at various NJDs as a function of applied V_{gs} (Kumar, 2017).

Figure 2.10(a) evidently reveals an improvement in IIP3 for the TGRC as compared to the conventional and CRC designs. This is due to the integration of the TGRC architecture, which is attributed to high transconductance and lower value of g_{m3}, and thus results increase in the carrier transport efficiency causing an improved gate control over the channel. Moreover, the gate length and NJD variations w.r.t. the applied gate to source voltage are also shown in **Figure 2.10(b)** and **Figure 2.10(c)** which show increase in linearity of the device and, hence, desirable efficiency is observed.

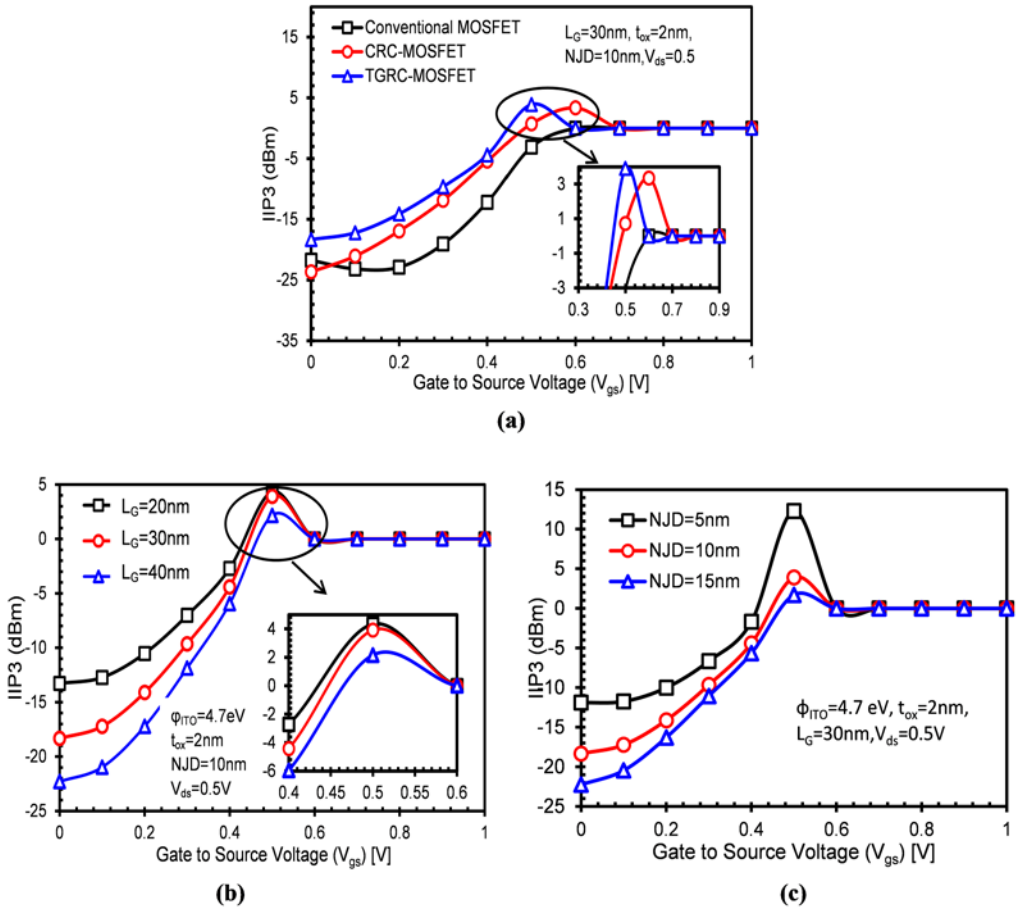


Figure 2.10: (a) Variations of IIP3 for TGRC-MOSFET, CRC-MOSFET, and Conventional MOSFET. (b) Variation of IIP3 at different L_G. (c) Variation of IIP3 at different NJDs as a function of applied V_{gs} (Kumar, 2017).

Moreover, there are two important FOMs which govern amplifier's efficiency and linearity i.e. third-order intercept point (IIP3) and 1-dB compression point (1dB CP). Third-order intercept is a theoretical point at which the third-order distortion signal amplitudes equal the input signals, and it is useful in determining the linearity condition of an amplifier. 1-dB compression point is defined as the input power which causes the gain to drop by 1-dB. These two parameters are evaluated by equations (2.9) and (2.10) (Chaujar et al, 2009; Woerlee et al, 2001).

$$IIP3 = \frac{2}{3}\frac{g_{m1}}{g_{m3} \times Rs} \tag{2.9}$$

$$1-dB\,Compression\ \text{Point} = 0.22 \times \sqrt{\frac{g_{m1}}{g_{m3}}} \tag{2.10}$$

where R_S=50 Ω for analog and RF applications.

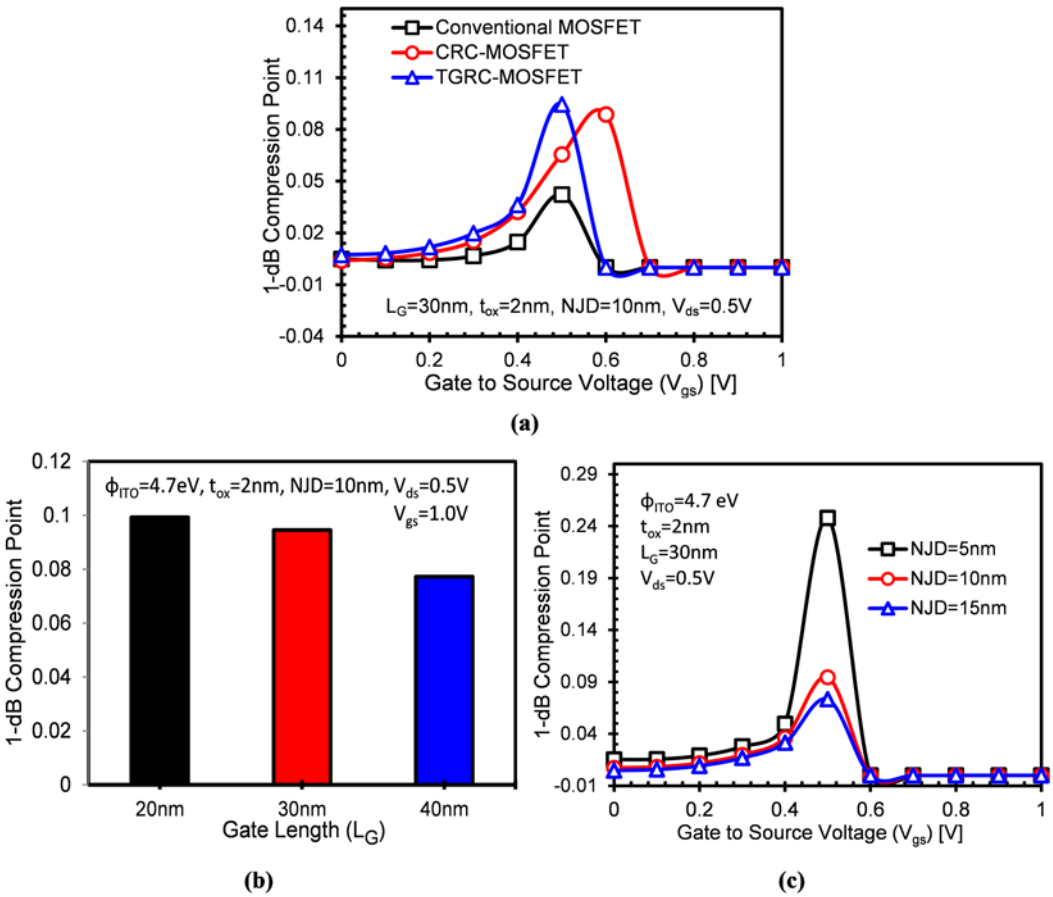


Figure 2.11: (a) Variations of 1-dB Compression point for TGRC-MOSFET, CRC-MOSFET, and Conventional MOSFET. (b) Variation of 1-dB Compression point at different L_G. (c) Variation of 1-dB Compression at different NJDs as a function of applied V_{gs} (Kumar, 2017).

So, IIP3 can be enhanced by reducing the gate length (from 40 nm to 30 nm and from 30 nm to 20 nm) and decreasing the NJD (from 15 nm to 10 nm and from 10 nm to 5 nm). The 1-dB compression point is essential to identify at what point compression occurs so that input levels can be limited to prevent distortion. It is generally the input power that causes the gain to fall by 1 dB from the normal linear gain specification. This parameter signifies the maximum input power that the amplifier circuit can handle by providing a fixed amount of gain, and if the input power surpasses the compression point, the gain starts falling. Hence, it is desirable that a 1-dB compression point should be as high as possible for the highly linear amplifier.

Figure 2.11(a) shows peak value of 1-dB compression point in TGRC-MOSFET rises in comparison to its conventional counterparts. This improvement is due to the enhanced current driving capability of the device owing to high conductivity and transparency of ITO. Further, the gate length variation is observed for TGRC-MOSFET in terms of 1-dB compression point, and it is found that with the tuning of gate length and NJD, 1-dB compression point is significantly improved as shown in **Figure 2.11(b)** and **Figure 2.11(c)** owing to improved current driving capability of TGRC-MOSFET that enhances g_m and thus 1-dB compression point.

B. Intermodulation Distortion

The previous subsection discusses about the linearity of TGRC-MOSFET and how it can be improved if the device parameters scale down. In this subsection, distortion due to high order transconductance is studied to examine its efficacy on the performance of TGRC architecture. **Figure 2.12(a)** reflects the variations of third derivative of transconductance (g_{m3}) w.r.t. the V_{gs} for conventional MOSFET, CRC-MOSFET, and TGRC-MOSFET. It is examined from **Figure 2.12(a)** that the TGRC device has lower g_{m3} as compared to the CRC design; and due to this, lesser distortion is observed.

Figure 2.12(b) displays the variations of g_{m3} w.r.t. the V_{gs} for three different gate lengths (20 nm, 30 nm, and 40 nm). It is found that the DC bias point moves towards higher V_{gs} with increase in L_G as clearly indicated by **Figure 2.12(b)**. This deviation is due to the amalgamation of ITO in TGRC-MOSFET. Further, the variations of g_{m3} w.r.t. V_{gs} for different NJDs have been observed, and it is analysed that, if NJD reduces then g_{m3} also reduces which indicates that when NJD is 5nm, TGRC-MOSFET shows minimum distortion as depicted in **Figure 2.12(c)**. In addition, IMD3 and HD3 (Third-order harmonic distortion) are major issues in linear amplifiers that arise owing to the nonlinearity performance of the device (Gupta & Chaujar, 2016). IMD3 signifies the intermodulation current at which first and third order intermodulation harmonic currents are equal. IMD3 is analyzed considering the effect of the transparent gate.

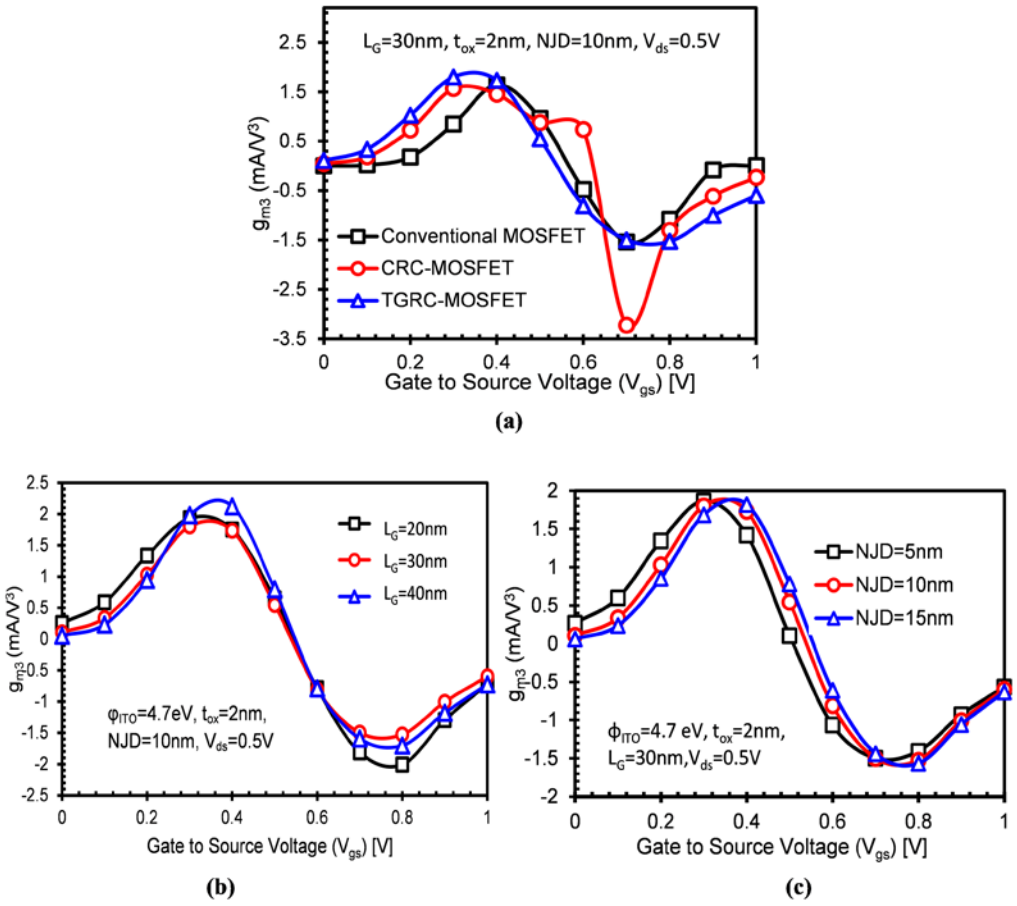


Figure 2.12: (a) Variations of g_{m3} for TGRC-MOSFET, CRC-MOSFET, and Conventional MOSFET. (b) Variation of g_{m3} at different L_G. (c) Variation of g_{m3} at various NJDs as a function of applied V_{gs} (Kumar, 2017).

The distortion has been calculated with the help of integral function method (IFM) since this approach allows the distortion extraction from DC measurements without an AC characterization, dissimilar to Fourier-based methods (Cerdeira et al, 2004; Doria et al, 2008). The approximate analytical expression for IMD3 and HD3 are given as:

$$IMD3 = \left(\frac{9}{2}\times(VIP3)^3\times g_{m3}\right)^2 \times R_S \tag{2.11}$$

$$HD3 = 0.25V_a^2\frac{\left(\frac{d^2 g_{m1}}{dV^2{}_{GT}}\right)}{6g_{m1}} \tag{2.12}$$

Where V_a is the magnitude of AC signal and considered to be very small, of about 50 mV for IFM analysis.

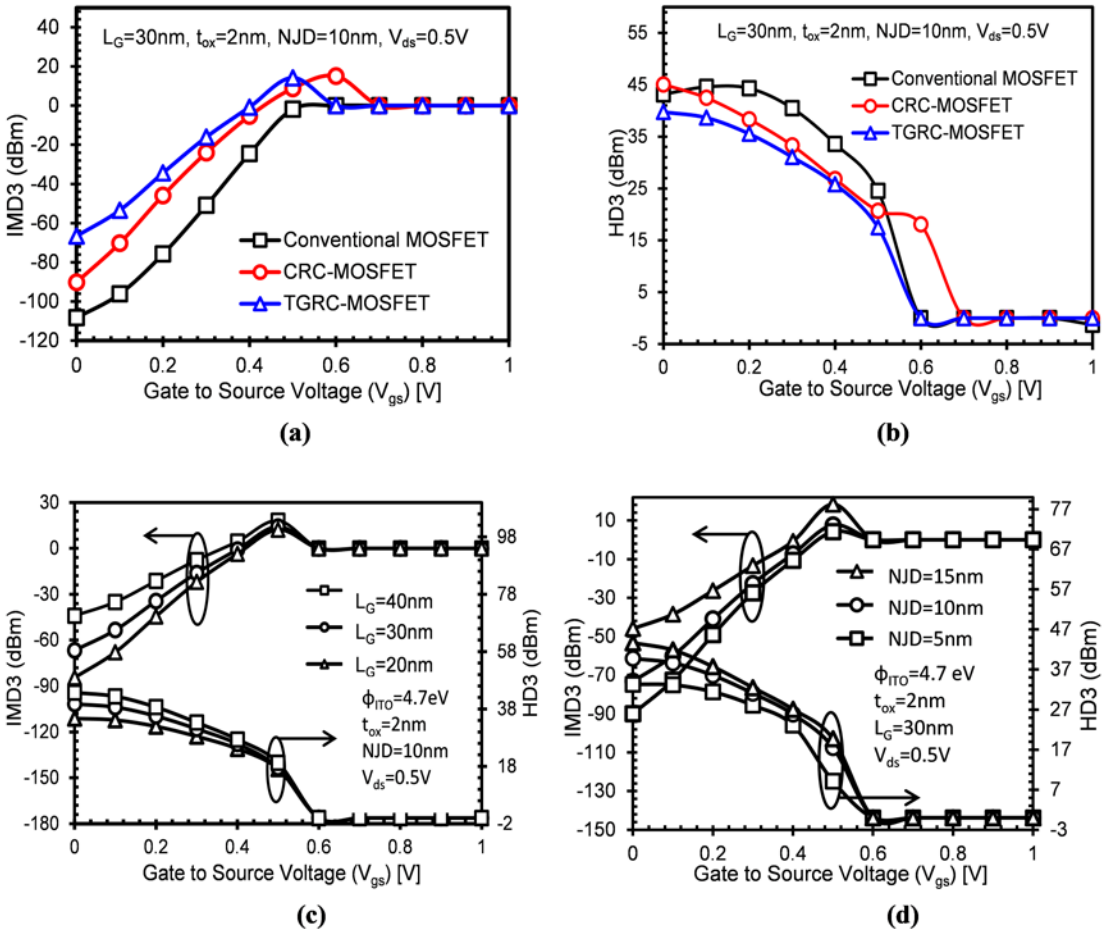


Figure 2.13: (a) Variations of IMD3 for TGRC-MOSFET, CRC-MOSFET and Conventional MOSFET. (b) Variation of HD3 for TGRC-MOSFET, CRC-MOSFET, and Conventional MOSFET. (c) Variations of IMD3 and HD3 at different L_G. (d) Variation of IMD3 and HD3 at various NJDs as a function of applied V_{gs} (Kumar, 2017).

Figure 2.13(a)–(d) shows the variation of IMD3 and HD3 w.r.t. the applied gate to source voltage for the conventional, CRC and TGRC designs, for gate length variation, and for NJD variation, respectively. Degeneracy of signals in a wireless communication system is originated as IMD3 from the nonlinearity shown by the transistor static characteristics. By using a circuit with balanced topologies, even-order harmonics can be reduced by 40–50 dB. Therefore, it is essential to diminish the third-order harmonics for decreasing the signal distortion (Ghosh et al, 2012). **Figure 2.13(a)** shows that the performance of IMD3 degrades in TGRC-MOSFET owing to the high peak value of VIP3 which dominates the value of IMD3 less in comparison to g_{m3} (**Figure 2.12(a)**) as compared to its counterpart conventional and CRC-MOSFET. Meanwhile, HD3 is also reduced in TGRC architecture as compared to its

conventional counterparts as shown in **Figure 2.13(b)**. Further, both the third order distortions have been reduced for TGRC-MOSFET if the gate length is reduced to 20 nm due to the reduction of g_{m3} as shown in **Figure 2.13(c)**. **Figure 2.13(d)** also reflects the reduction in IMD3 and HD3 with reduced NJD. Thus, the scaling of the device architecture reduces the intermodulation and harmonic distortions, hence presenting TGRC-MOSFET as a favorable candidate for RFIC designing.

2.6 SUMMARY

A complete study of the analog, linearity and intermodulation distortion analysis of TGRC-MOSFET has been explored with the impact of trench gate and gate length miniaturization at sub-nano level. From the investigation, it is found that TGRC-MOSFET achieves high current driving capability due to ITO as a gate material in comparison to conventional MOSFETs which results in high transconductance (increased by 32.1% and 35% compared to conventional MOSFET and CRC-MOSFET respectively) and improved device efficiency. Further, it is also observed that TGRC exhibit significant enhancement in peak values of VIP2, VIP3, 1-dB compression point, IIP3 and lesser values of the IMD3 and HD3 in comparison to its counterparts at 5 nm NJD and 20 nm gate length. Therefore, TGRC-MOSFET delivered enriched analog and linearity performance in terms of superior input power and lesser signal distortion. Moreover, it is also analyzed that with the tuning of TGRC's parameters such as L_G and NJD, its analog and linearity performance enhances appreciably owing to enhanced current driving capability and reduced g_{m3} (distortions). Therefore, the proposed TGRC-MOSFET is prominent for high scale integration, which can be developed for RFIC design and it is also a favorable candidate for ultra-low power, analog, and distortion-less application. After considering the analog and linearity behavior of TGRC MOSFET, reliability is of serious concern, owing to various process/stress/radiation damages that induce interface charges at the Si-SiO_2 interface. Thus, to ensure the reliability of the device, it is essential to investigate the characteristics of the device in the presence of various ITCs that is the primary focusing area of the next chapter.

2.7 REFERENCES

An, X., Huang, R., Zhao, B., Zhang, X. & Wang, Y. (2003) Design guideline of an ultra-thin body SOI MOSFET for low-power and high-performance applications. *Semiconductor science and technology*, 19(3), 347.

Appenzeller, J., Martel, R., Avouris, P., Knoch, J., Scholvin, J., del Alamo, J. A., Rice, P. & Solomon, P. (2002) Sub-40 nm SOI V-groove n-MOSFETs. *IEEE Electron Device Letters*, 23(2), 100-102.

Auth, C. P. & Plummer, J. D. (1997) Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET's. *Electron Device Letters, IEEE*, 18(2), 74-76.

Barsan, R. M. (1981) Analysis and modeling of dual-gate MOSFET's. *Electron Devices, IEEE Transactions on*, 28(5), 523-534.

Cerdeira, A., Alemán, M. A., Estrada, M. & Flandre, D. (2004) Integral function method for determination of nonlinear harmonic distortion. *Solid-State Electronics*, 48(12), 2225-2234.

Chaujar, R., Kaur, R., Saxena, M., Gupta, M. & Gupta, R. (2008a) Laterally amalgamated DUal material GAte concave (L-DUMGAC) MOSFET for ULSI. *Microelectronic Engineering*, 85(3), 566-576.

Chaujar, R., Kaur, R., Saxena, M., Gupta, M. & Gupta, R. (2008b) TCAD assessment of gate electrode workfunction engineered recessed channel (GEWE-RC) MOSFET and its multilayered gate architecture—part I: hot-carrier-reliability evaluation. *Electron Devices, IEEE Transactions on*, 55(10), 2602-2613.

Chaujar, R., Kaur, R., Saxena, M., Gupta, M. & Gupta, R. (2009) TCAD assessment of Gate Electrode Workfunction Engineered Recessed Channel (GEWE-RC) MOSFET and its multi-layered gate architecture, Part II: Analog and large signal performance evaluation. *Superlattices and Microstructures*, 46(4), 645-655.

D. J. Rogers, H. T. (2010) Criteria for choosing conductors, 25.

Doria, R. T., Cerdeira, A., Raskin, J.-P., Flandre, D. & Pavanello, M. A. (2008) Harmonic distortion analysis of double gate graded-channel MOSFETs operating in saturation. *Microelectronics Journal*, 39(12), 1663-1670.

Ghosh, P., Haldar, S., Gupta, R. & Gupta, M. (2012) An investigation of linearity performance and intermodulation distortion of GME CGT MOSFET for RFIC design. *IEEE Transactions on Electron Devices*, 59(12), 3263-3268.

Gupta, N. & Chaujar, R. (2016) Optimization of high-k and gate metal workfunction for improved analog and intermodulation performance of Gate Stack (GS)-GEWE-SiNW MOSFET. *Superlattices and Microstructures*.

Gupta, N., Kumar, A. & Chaujar, R. (2015) Impact of device parameter variation on RF performance of gate electrode workfunction engineered (GEWE)-silicon nanowire (SiNW) MOSFET. *Journal of Computational Electronics*, 14(3), 798-810.

Iwai, H. (2009) Roadmap for 22nm and beyond. *Microelectronic Engineering*, 86(7), 1520-1528.

Jeong, K. & Kahng, A. B. (2009) A power-constrained MPU roadmap for the International Technology Roadmap for Semiconductors (ITRS), *SoC Design Conference (ISOCC), 2009 International*. IEEE.

Kim, T. W., Kim, B. & Lee, K. (2004) Highly linear receiver front-end adopting MOSFET transconductance linearization by multiple gated transistors. *IEEE Journal of Solid-State Circuits*, 39(1), 223-229.

Kumar, A. (2017) Effect of Trench Depth and Gate Length Shrinking Assessment on the Analog and Linearity Performance of TGRC-MOSFET. *Superlattices and Microstructures*.

Kumar, A., Gupta, N. & Chaujar, R. (2015) Analysis of novel transparent gate recessed channel (TGRC) MOSFET for improved analog behaviour. *Microsystem Technologies*.

Kumar, A., Gupta, N. & Chaujar, R. (2016) Analysis of novel transparent gate recessed channel (TGRC) MOSFET for improved analog behaviour. *Microsystem Technologies*, 22(11), 2665-2671.

Rahimian, M. & Orouji, A. A. (2013) Investigation of the Electrical and Thermal Performance of SOI MOSFETs with Modified Channel Engineering. *Materials Science in Semiconductor Processing*, 16(5), 1248-1256.

Razavi, B. & Behzad, R. (1998) *RF microelectronics, 1*Prentice Hall New Jersey.

SILVACO, I. (2011) ATLAS User's Manual. *Santa Clara, CA, Ver*, 5.

Veeraraghavan, S. & Fossum, J. G. (1989) Short-channel effects in SOI MOSFETs. *IEEE Transactions on Electron Devices*, 36(3), 522-528.

Wang, R., Zhuge, J., Huang, R., Tian, Y., Xiao, H., Zhang, L., Li, C., Zhang, X. & Wang, Y. (2007) Analog/RF performance of Si nanowire MOSFETs and the impact of process variation. *IEEE transactions on Electron Devices*, 54(6), 1288-1294.

Woerlee, P. H., Knitel, M. J., Van Langevelde, R., Klaassen, D. B., Tiemeijer, L. F., Scholten, A. J. & Zegers-van Duijnhoven, A. T. (2001) RF-CMOS performance trends. *IEEE Transactions on Electron Devices*, 48(8), 1776-1782.

Xiao-Hua, M., Yue, H., Bao-Gang, S., Hai-Xia, G., Hong-Xia, R., Jin-Cheng, Z., Jin-Feng, Z., Xiao-Ju, Z. & Wei-Dong, Z. (2006) Fabrication and characterization of groove-gate MOSFETs based on a self-aligned CMOS process. *Chinese Physics*, 15(1), 195.

3

CHAPTER

Reliability Issues of In_2O_5Sn Gate Electrode Recessed Channel MOSFET: Impact of Interface Trap Charges and Temperature

- *Reliability issues of In_2O_5Sn Gate Recessed Channel MOSFET have been analysed by considering the effect of interface trap charges (both polarity and density) present at the Si/SiO_2 interface.*
- *Device characteristics are studied in terms of Static, Linearity and Intermodulation Distortion FOMs.*
- *It is found that with amalgamation of the transparent gate (ITO) on Conventional Recessed Channel (CRC) MOSFET, it exhibits improved immunity against interface trap charges.*
- *In addition, the influence of ambient temperature (150-300K) along with trap charges on TGRC MOSFET has also been explored with an aim to analyze the impact of temperature on the device stability in the presence of interface defects (trap charges).*
- *Results so obtained revealed that TGRC MOSFET shows improved device performance at low temperature with trap charges being less influenced.*

This study demonstrates that TGRC MOSFET can act as a promising candidate for low-power linear/analog applications where low temperature is desired.

3.1 INTRODUCTION

As discussed in Chapter 1, during fabrication processes, various types of charges or traps are carelessly incorporated into the oxide and thus degrades the performance of the device (Arora, 1993). Four different types of trap charges present in the thermally grown oxide, i.e., 1. Interface Trapped Charges. 2. Field Oxide Charges, 3. Mobile Ionic Charge and 4. Oxide Trapped Charge. Among them, the most important one to study is the interface trap charges owing to the wide-ranging and degrading effect on device characteristics. These charges are due to electronic energy levels situated at the interface of Si/SiO_2 with energy states in the Si band gap that can change their charge state by capturing or emitting electrons (or holes). These electrons arise owing to incomplete bonds (dangling), adsorption of extraneous impurity atoms at the silicon surface, and other defects such as lattice mismatch at the interface, which triggered by either radiation or bond-breaking processes (Jo et al, 2017; Lho & Kim, 2005; Poindexter, 1989; Trabzon & Awadelkarim, 1998). These charges are also known as surface states or interface states (or traps) where the position of Fermi level decides the occupancy of interface trap charges under equilibrium state. In contrast to conduction and valence band, the interface trap charges have energy level situated in the forbidden gap.

The trap charges (both electrons and holes) are present in this gap and cannot move quickly due to large space between the interfacial trivalent silicon atoms. The energy level of an acceptor interface trap charge (or negative trap charges) lies above the valence band and below Fermi energy level while the energy level of donor interface trap charge (or positive trap charges) lie below the conduction band and above the Fermi energy level (Arora, 1993). Moreover, the trap density is very subtle to even small process variation, which subsequently leads to mobility and threshold voltage degradation and thus results in a decrement in device transconductance. Hence, it is essential to examine the consequence of these trap charges on the performance of TGRC-MOSFET.

3.2 DEVICE DESIGN AND ITS DESCRIPTION

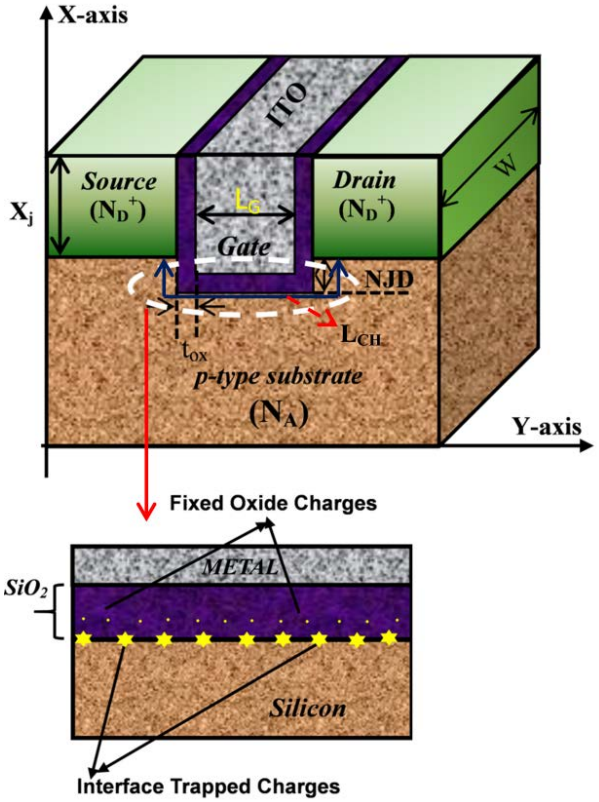


Figure 3.1: Device design of TGRC-MOSFET (3D device) with interface traps charges (Kumar et al, 2017a; 2018).

Figure 3.1 shows the schematic 3D view of TGRC-MOSFET which consists of interfaced trap charges at the interface of Si/SiO_2 interface. The gate length (L_G) is 30nm while channel length (L_{CH}) is 54nm ($L_G+2t_{ox}+2NJD$), oxide thickness (t_{ox}) = 2nm, negative junction depth (NJD) = 10nm, groove depth = 38nm, for both devices (CRC and TGRC MOSFETs). The source/drain region is heavily n+ doped ($5\times10^{20}cm^{-3}$) whereas channel is p-doped ($1\times10^{17}cm^{-3}$) for both CRC and TGRC MOSFETs. The gate material which plays a role in determining the current driving capability of MOSFET is taken In_2O_5Sn in the proposed device (TGRC-MOSFET) having workfunction of 4.7eV whereas, in CRC-MOSFET, aluminium (4.4eV) as gate metal is used.

3.3 SIMULATION METHODOLOGY AND CALIBRATION

ATLAS is a powerful simulation tool which is used for extracting of reliability results and all figure of merits (FOMs) (SILVACO, 2011). Various simulation models have been used during this analysis such as Lombardi CVT model to consider all the mobilities such as scattering mechanism which is caused by the parallel and perpendicular field applied on the device. For carrier generation-recombination, we have used Shockley-Read-Hall (SRH) Recombination. In order to consider the information about the low energy (temperature) of the carriers, we have used Energy Balance Transport (EBT) model (SILVACO, 2011). To validate the simulations results, the statistics have been drawn-out for 36 nm groove MOSFET (Appenzeller et al, 2002) and then plotted as evident in **Figure 3.2**. It is detected from the **Figure 3.2** that simulated results almost matched with the experimental results in 36 nm groove MOSFET thus validating the simulation models. In this analysis, the value of trap charge density at the interface is chosen as 1e12 cm^{-2} with uniform profiles according to previously published work (Chiang, 2011; Shabde et al, 1988).

To explore the effect of trap charges on the sub-nm device, the total gate length is considered as a damaged region due to the high field in the channel region owing to scaling.

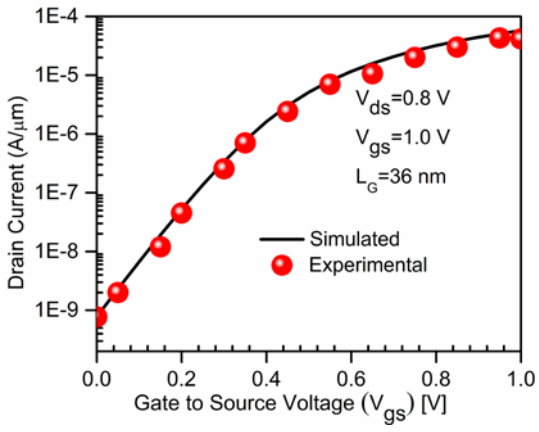


Figure 3.2: Calibrated transfer characteristics of recessed channel MOSFET (36 nm gate length) with experimental (Appenzeller et al, 2002) and simulation data (Kumar et al, 2017a; 2018).

3.4 RESULTS AND DISCUSSION

There are many parameters which influence the performance of a MOSFET. In this section, reliability is examined and calculated in terms of analog and linearity FOMs. In addition, the effect of low temperature is explored on reliability issues of TGRC-MOSFET in the presence of trap charges (i.e., defects).

3.4.1 Impact of Interface Trap Charges on Analog Performance

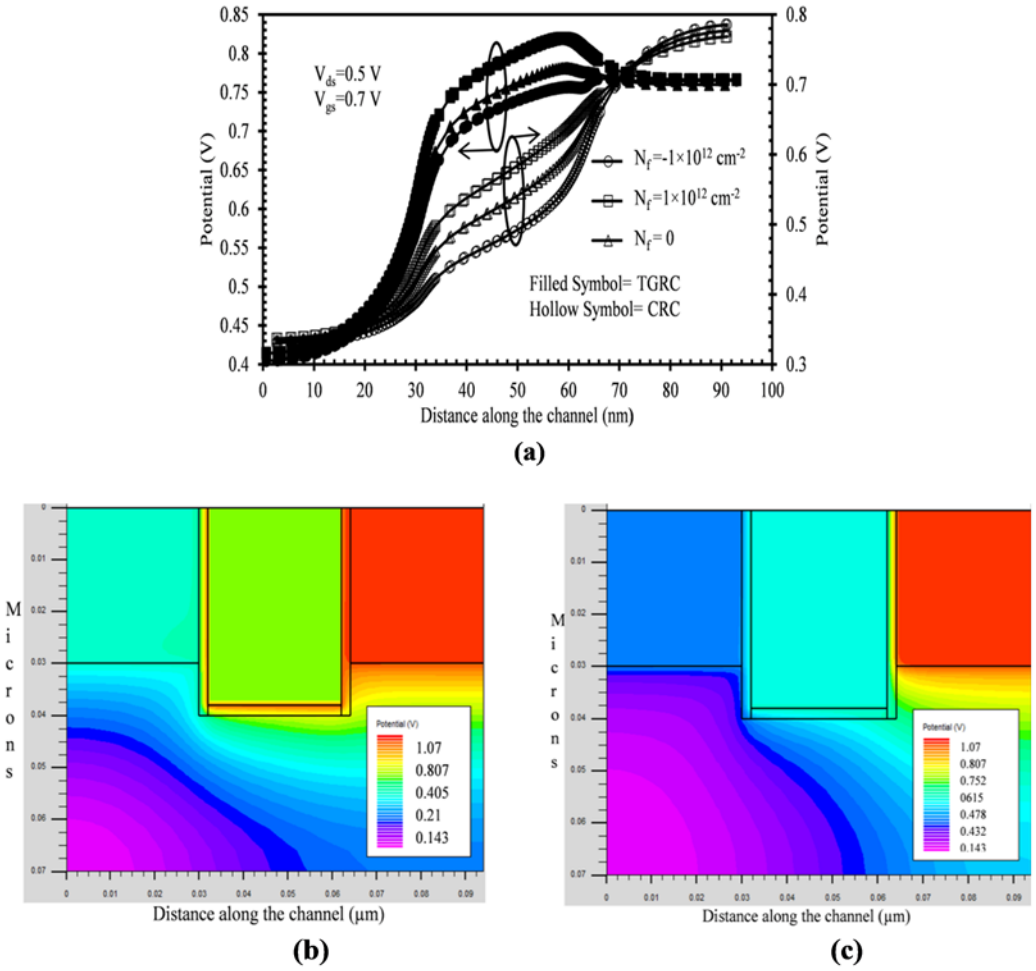


Figure 3.3: (a) Potential, with respect to the distance along the channel for CRC and TGRC MOSFETs. (b) Contour plot CRC-MOSFET with impact of positive interface trap charge (c) Contour plot TGRC-MOSFET with impact of positive interface trap charge (Kumar et al, 2018).

Trap charges (both positive and negative) present beneath the Si/SiO_2 region is responsible for the change in flat band voltage, and it is given by (Chiang, 2011):

$$\Delta V_{fb} = \frac{qN_f}{C_{ox}} \tag{3.1}$$

Where ΔV_{fb} is the change in flat band voltage, N_f is the charge density and C_{ox} is gate oxide capacitance (shown in equation 3.1). **Figure 3.3(a)** shows the impact of interface trap charges (positive and negative) on the surface potential along the channel. The trap charges are considered along with the entire gate length (L_G), and it is revealed from the figure that, the positive trap charges (donor type) enhances the potential while negative trap charges (acceptor type) reduces the potential in TGRC and CRC MOSFET. This enhancement (reduction) in potential is due to lowering (rising) of flat-band voltage which increases (decreases) the gate control over the channel and thus the surface potential. It is also found that surface potential enhances significantly in TGRC-MOSFET in comparison to CRC-MOSFET owing to the high conductivity of transparent gate as clearly reflected through 2D contour plots shown in **Figure 3.3(b-c)**.

It is observed from **Figure 3.4(a)** and **Figure 3.4(b)** that electric field in the channel region enhances appreciably in TGRC-MOSFET due to high surface potential in the channel region and owing to ITO as a gate metal having higher workfunction in comparison to the aluminium metal gate. Electric field near the drain end reduces and enhances near the source side as compared to CRC-MOSFET.

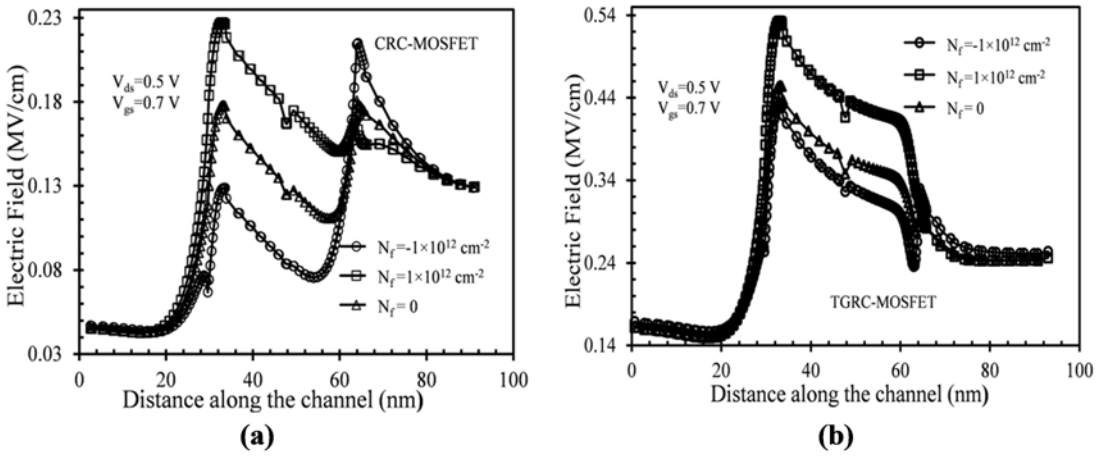


Figure 3.4: (a) Electric field distribution along the channel for CRC-MOSFET and (b) for TGRC-MOSFET (Kumar et al, 2018).

The presence of positive (negative) trap charges increases (decreases) the electric field near the source end in comparison to drain end, owing to the creation of more (less) charges in the channel region and thus leads to more (less) number of charge-carriers being flow. However, from **Figure 3.3** and **Figure 3.4**, it is clearly observed that influence of trap charges is less pronounced in TGRC in comparison to CRC-MOSFET. The impact of trap charges on transfer characteristics (I_{ds}-V_{gs}) and output characteristics are also examined. **Figure 3.5(a-b)** indicates that the effect of trap charges is more prominent in the sub-threshold region than linear region. It is found that in the presence of positive (negative) trap charges, drain current increases (decreases) owing to high (low) field at the source end and enhanced (reduced) gate control. However, TGRC indicates nearly insignificant change in on-current profile due to interface traps/damage region when it worked in inversion region.

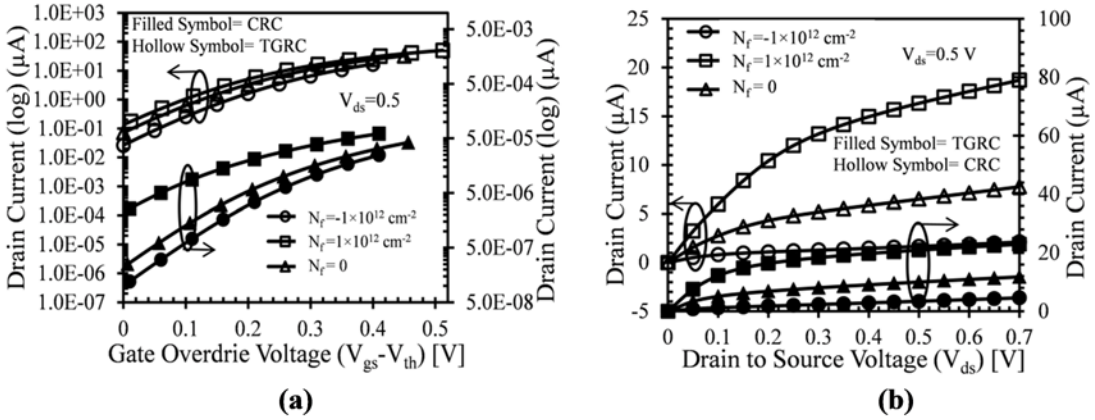


Figure 3.5: (a) Transfer characteristics w.r.t. V_{gs}, (b) Output characteristics w.r.t. V_{ds}; for CRC-MOSFET and TGRC-MOSFET (Kumar et al, 2018).

Electrical power is the "rate" at which energy is being consumed in a circuit. The impact of interface trap charges on the low-power performance parameter such as P_{DC} (DC power) and P_{AC} (AC power) has also been evaluated using the following equations 3.2 and 3.3:

$$P_{DC} = V_{DC} \times I_{DC} \tag{3.2}$$

$$P_{AC} = V_{rms} \times I_{rms} \tag{3.3}$$

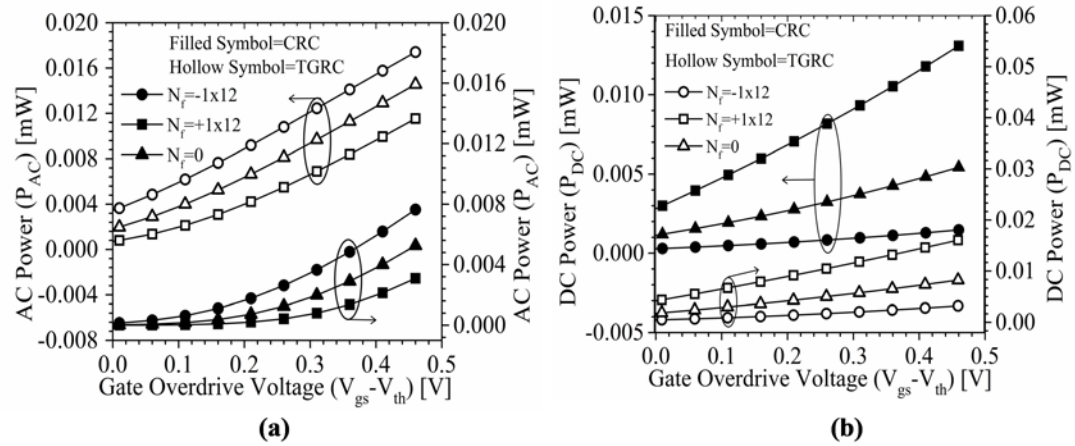


Figure 3.6: (a) DC power (P_{DC}) and (b) AC power (P_{AC}) w.r.t. V_{gs}; for CRC-MOSFET and TGRC-MOSFET (Kumar et al, 2018).

It is found that DC power starts increasing with increase in gate overdrive voltage and its value is numerically smaller in TGRC-MOSFET in comparison to CRC-MOSFET as evidently shown from **Figure 3.6(a)**. Moreover, it is also observed that the effect of trap charges in TGRC-MOSFET shows lesser impact on DC power in comparison to CRC-MOSFET. This improvement is due to lower off current and improved current driving capability. In addition, AC power is also studied and is found that AC power in TGRC-MOSFET is more immune to interface trap charges in comparison to CRC-MOSFET as shown in **Figure 3.6(b)**. Thus, it can be concluded that in the presence of trap charges, TGRC-MOSFET will be suitable for low power applications.

Further, it is also analyzed that with the tuning of TGRC's parameters such as L_G (From 40nm to 20nm) and NJD (from 15nm to 5nm), its linearity performance enhances appreciably (Kumar, 2017) while power (P_{AC}) degrades as clearly reflected in **Table 3.1**. Therefore, depending on the application, we may utilize the trade-off between improved linearity and improved P_{AC} at a given device feature size.

Table 3.1. P_{AC} Variation with L_G (Kumar et al, 2018).

Gate length (L_G) (nm)	20	30	40
P_{AC} (mW)	0.01325	0.015	0.018

Moreover, due to enhancement in drain current, switching ratio (I_{ON}/I_{OFF}) of TGRC enriches significantly as evident from **Figure 3.7(a)** and it is calculated by the

ratio of current at V_{gs}=0.7 V (I_{ON}) and current at V_{gs}=0 V (I_{OFF}). In TGRC, the ratio is increased by 125%, 128%, and 166% for positive, negative, and neutral trap charges respectively as compared to CRC device, shown in **Figure 3.7(a)**.

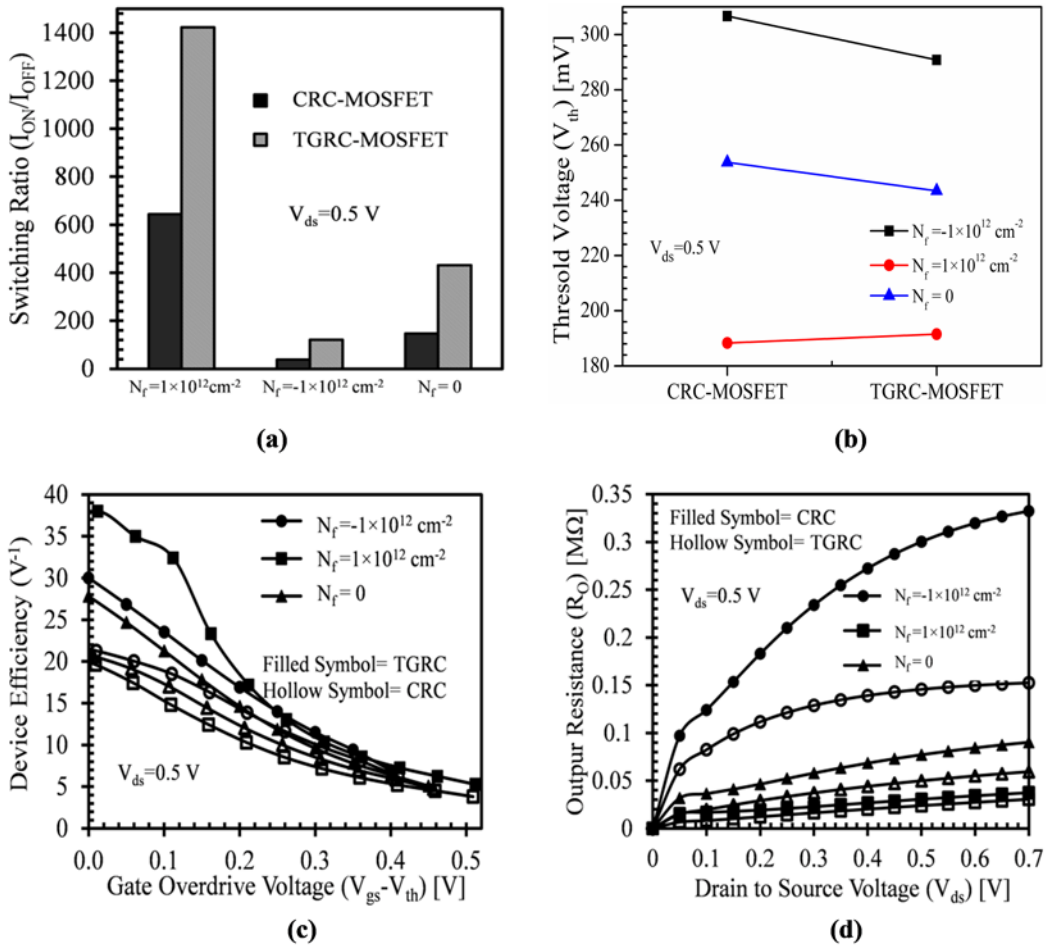


Figure 3.7: Effect of interface trap charges on (a) switching ratio (b) threshold voltage (c) device efficiency and (d) output resistance, for CRC-MOSFET and TGRC-MOSFET (Kumar et al, 2018).

However, CRC-MOSFET shows a more significant influence of interface trap charges for switching ratio than TGRC-MOSFET. In addition, the threshold voltage (V_{th}) which is a significant parameter for analog applications, also improves in TGRC-MOSFET in comparison to CRC-MOSFET as shown in **Figure 3.7(b)**. This increase is due to reduced leakage current owing to the transparent gate which results in reduced SCEs (Hot-carrier and DIBL) (Kumar et al, 2016a).

V_{th} is also affected by trap charges as reflected in **Figure 3.7(b)** but the effect is more in CRC in comparison to TGRC due to less change in flat band voltage. Influence of trap charges on transconductance to the current ratio (g_m/I_d) or device efficiency and output resistance have also been analyzed for both devices as depicted in **Figure 3.7(c)** and **Figure 3.7(d)**. In the design of analog circuits, device efficiency is a vital factor which offers the measure of effectiveness to convert power into speed. It is evident from **Figure 3.7(c)** that the device efficiency is higher (lower) in TGRC-MOSFET when positive (negative) trap charges are present in comparison to CRC-MOSFET. It is also observed in **Figure 3.7(c)** that the impact of interface trap charges on device efficiency is less prominent in TGRC and thus signify superior efficiency in TGRC than CRC. The output resistance (R_o) is the transposed of the output conductance in a MOSFET and for high performance; R_o should be as small as possible. When positive (negative) trap charges have been taken into consideration, R_o is very less (high) while it is less prominent for negative and neutral trap charges in TGRC-MOSFET as compared to conventional counterpart as shown in **Figure 3.7(d)**. Thus, recessed channel MOSFET with transparent gate material (ITO) shows reliable performance in the presence of interface trap charges as compared to CRC device.

3.4.2 Impact of Interface Trap Charges on Linearity and Distortion Performance

High linearity and lower intermodulation distortion are essential requirements for a CMOS device when working with weak signals. Nonlinearity introduces intermodulation distortion (IMD) and generates an undesired distorted signal in the output of different frequency signals compared to an input signal which results in degradation in device behavior (Razavi & Behzad, 1998). For that reason, in this subsection, the influence of interface trap charges on linearity and intermodulation distortion of TGRC device are studied and results so obtained are simultaneously compared with CRC-MOSFET. The performance metrics used in this analysis are g_{m3} (higher order transconductance coefficient), VIP3 (third order voltage intercept point), IIP3 (third order current intercept point), IMD3 (third order intermodulation

distortion), HD2 and HD3 (second and third order harmonic distortion). To assure higher linearity, higher order transconductance coefficient (g_{m3}) must be minimal.

From the dc parameters, VIP3 is used to evaluate the distortion characteristics. IIP3 and VIP3 should be high, but IMD3 and HD3 should be low for lower distortion. The device linearity FOMs are evaluated as shown in Equation (3.4) to (3.7) (Chaujar et al, 2009).

$$VIP3 = \sqrt{24 \times g_{m1} / g_{m3}} \tag{3.4}$$

where $g_{m1} = \frac{\partial I_d}{\partial V_{gs}}$ and $g_{m2} = \frac{\partial^2 I_d}{\partial V^2{}_{gs}}$. $g_{m3} = \frac{\partial^3 I_d}{\partial V^3{}_{gs}}$

$$IIP3 = \frac{2}{3}\frac{g_{m1}}{g_{m3} \times Rs} \tag{3.5}$$

where R_S=50 Ω for analog and RF applications.

$$IMD3 = \left(\frac{9}{2} \times (VIP3)^3 \times g_{m3}\right)^2 \times R_S \tag{3.6}$$

$$HD2 = 0.5 V_a \frac{\left(\frac{dg_{m1}}{dV_{GT}}\right)}{2g_{m1}} \tag{3.7}$$

$$HD3 = 0.25 V_a^2 \frac{\left(\frac{d^2 g_{m1}}{dV^2{}_{GT}}\right)}{6g_{m1}} \tag{3.8}$$

where R_S=50 Ω for analog and RF applications. V_a is the amplitude of AC signal and considered about 50 mV (which is minuscule) for Integral Function Method (IFM) analysis.

Ideally, g_{m3} should be as low as possible because g_{m3} decides the dc bias point for optimal device operation and determines the limits on the distortion. **Figure 3.8(a)**

illustrates the variation of g_{m3} w.r.t. V_{gs} for damaged (positive and negative traps) and undamaged region.

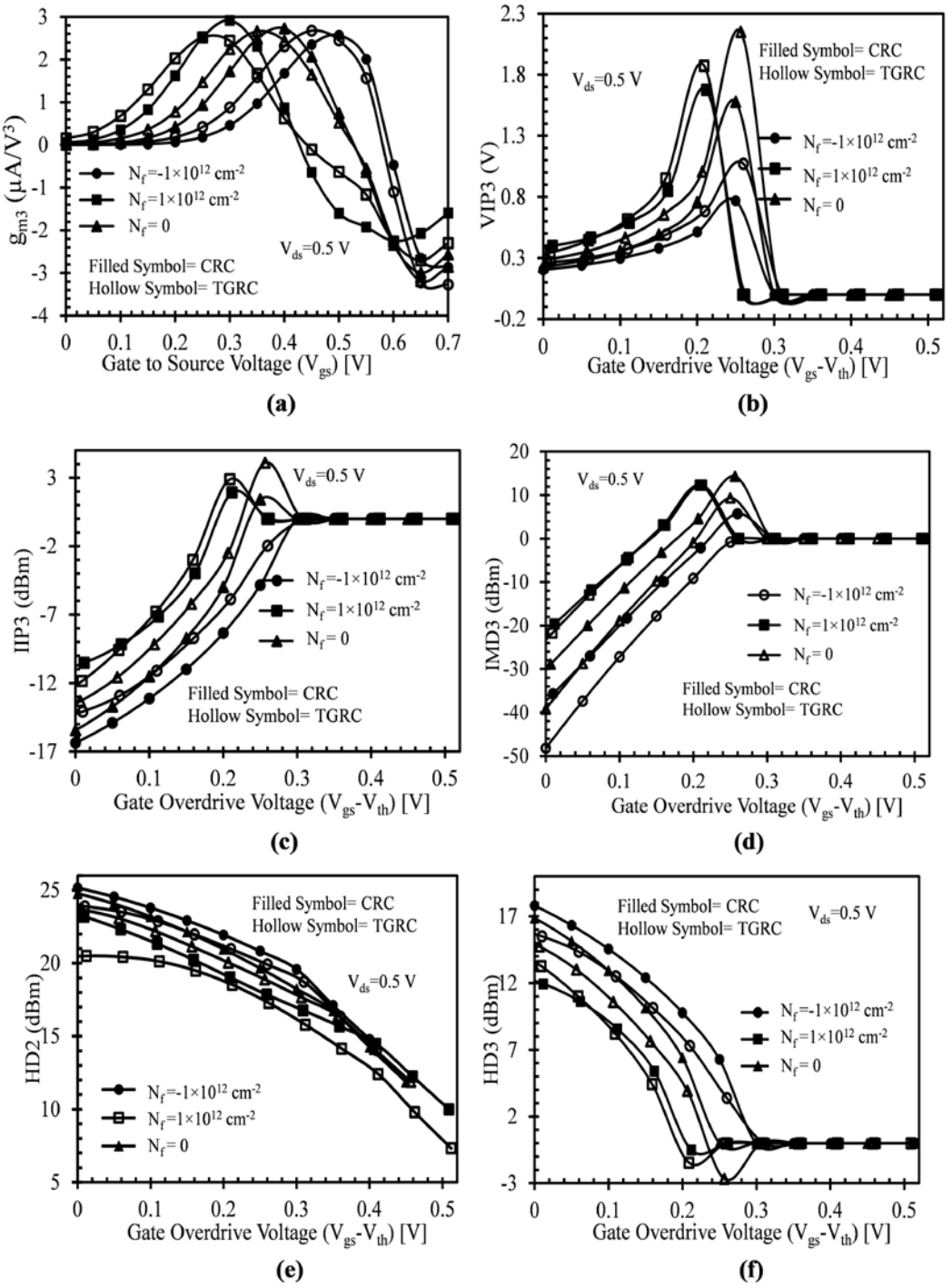


Figure 3.8: : Effect of interface trap charges on (a) g_{m3}, (b) VIP3, (c) IIP3, (d) IMD3, (e) HD2 and (f) HD3 for CRC-MOSFET and TGRC-MOSFET (Kumar et al, 2018).

g_{m3} is a higher-order derivative of transfer characteristics and it is observed that g_{m3} reduces (enhances) in case of TGRC in the presence of positive (negative) trap charges although this variation is very less in comparison to CRC-MOSFET. This is due to less dependency of trap charges on transfer characteristics and transconductance which reflects TGRC is more reliable in the presence of interface trap charges/damage. **Figure 3.8(b)** and **Figure 3.8(c)** reflect the influence of interface trap charges on VIP3 and IIP3 respectively. For low distortion and high linearity, the peak value of IIP3 and VIP3 should be high. VIP3 signifies extrapolated input voltage at which first and third order harmonics of drain current are equal and expressed as in Equation (4) while IIP3 is a theoretical point at which the third-order distortion signal amplitudes equal the input signals, and it is useful in determining the linearity condition of an amplifier (Gupta & Chaujar, 2016b). The amplitude of VIP3 and IIP3 is high for TGRC-MOSFET as compared to CRC-MOSFET, and it also implies that the damaged device (in the presence of trap charges) shows less linearity in comparison with the undamaged device, but TGRC architecture shows better linearity and less distortion in comparison to CRC-MOSFET. This is due to the higher conductivity of ITO as compared to the metal gate that enhances current driving capability (Kumar et al, 2017b) and thus improves linearity performance in the presence of interface traps.

In addition, IMD3, HD2 and HD3 are major issues in linear amplifiers that arise owing to the nonlinearity performance of the device (Gupta & Chaujar, 2016b) and stated in Equation (6) to (8). IMD3 represents the intermodulation current at which the first and the third order intermodulation harmonic currents are same. IMD3 is analyzed considering the influence of interface trap charges on TGRC device. IFM is used for the calculation of the distortion since this approach is an authorizations for the extraction of distortion from DC measurements deprived of an AC characterization, dissimilar to Fourier-based methods (Cerdeira et al, 2004; Doria et al, 2008) as shown in equation (6) to (8). The output conductance of TGRC is negligible. Hence, device gains are improved (Kumar et al, 2016b; Van Langevelde & Klaassen, 1997a). **Figure 3.8(d)** reveals that IMD3 reduces in TGRC-MOSFET owing to the reduced g_{m3} value in comparison to VIP3 which dominates the value of

IMD3 (**Figure 3.8(a)**) as compared to CRC-MOSFET. Meanwhile, it is also observed that TGRC reduces (increase) HD2 and HD3 when positive (negative) trap charges are considered and exhibit a very less effect of trap charges as compared to its conventional counterpart as shown in **Figure 3.8(e)** and **Figure 3.8(f)**. Thus, TGRC exhibits improved linearity and distortion-less performance for ULSI in the presence of interface trap charges.

3.4.3 Effect of Interface Trap Charges at Low Temperature on Analog, Linearity and Intermodulation Distortion

This sub-section describes the effect of temperature on the above-mentioned parameters for TGRC-MOSFET in the occurrence of interface trap charges to analyze the reliability of TGRC-MOSFET at low temperatures (150-300K). Electrical behavior of CMOS devices changes with change- in temperature. As the temperature increase, the carrier mobility (Van Langevelde & Klaassen, 1997b) decreases as:

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-n} \tag{3.9}$$

Where ‘n’ is an exponent, which varies from 1.6 to 2.4 (Sze & Ng, 2006). If mobility is decreased, then the output current also reduces, and hence with the increase in temperature, switching ratio decreases as shown in **Figure 3.9(a)**. Moreover, change in ambient temperature also influences the trap charges created during the fabrication process. It is found that in the presence of positive (negative) trap charges, the number of charge carriers increased (decrease), due to which mobility reduced (enhance) and hence switching ratio and output resistance (inset) reduced (improves) as evident from **Figure 3.9(a)**. Further, the threshold voltage (V_{th}) of the MOSFET is inversely proportional to the temperature (Groeseneken et al, 1990) and it increases at low temperature due to the rise in Fermi potential (ϕ_F) and depletion charges (Elewa et al, 1990). In the absence of trap charges, V_{th} is 0.243V at room temperature. **Figure 3.9(b)** shows the variation of the threshold voltage, and it is observed that as the temperature rises from 150K to 300K, V_{th} reduced and it is higher (lower) for negative (positive) trap charges due to change in flat-band voltage and

mobility. Besides, both mobility and threshold voltage also influenced the drain to source current I_{ds} (Gupta & Chaujar, 2016a) as:

$$I_{ds}(T) \propto \mu(T)[V_{gs} - V_{th}(T)] \tag{3.10}$$

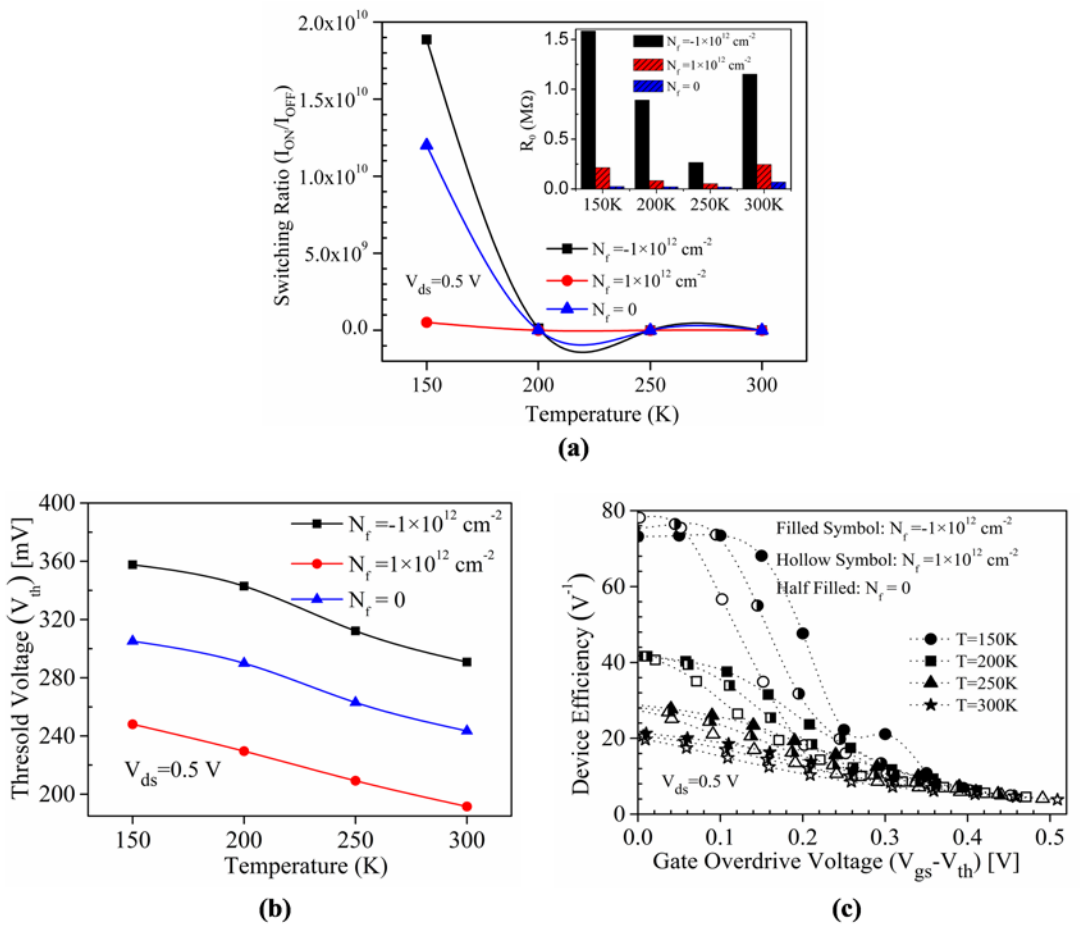


Figure 3.9: Effect of temperature on (a): switching ratio, Inset: output resistance, (b): threshold voltage and (c): device efficiency, in TGRC-MOSFET with interface trap charge density (Kumar et al, 2018).

Figure 3.9(c) illustrates the higher device efficiency at a lower temperature, and in the presence of positive (negative) trap charges, device efficiency is more (less) with respect to neutral trap charges. Hence, TGRC-MOSFET shows better performance at low temperature owing to reduced fluctuations. **Figure 3.10(a)** shows higher order transconductance g_{m3} as a function of the gate to source voltage for different ambient temperatures in the presence of positive (donor), and negative (acceptor) interface trap charges. At T=150 K, positive (negative) trap charges exhibit

low (high) distortion owing to improved transconductance. Furthermore, at high temperature (>150 K), distortion is increased (low peaks are observed in g_{m3}).

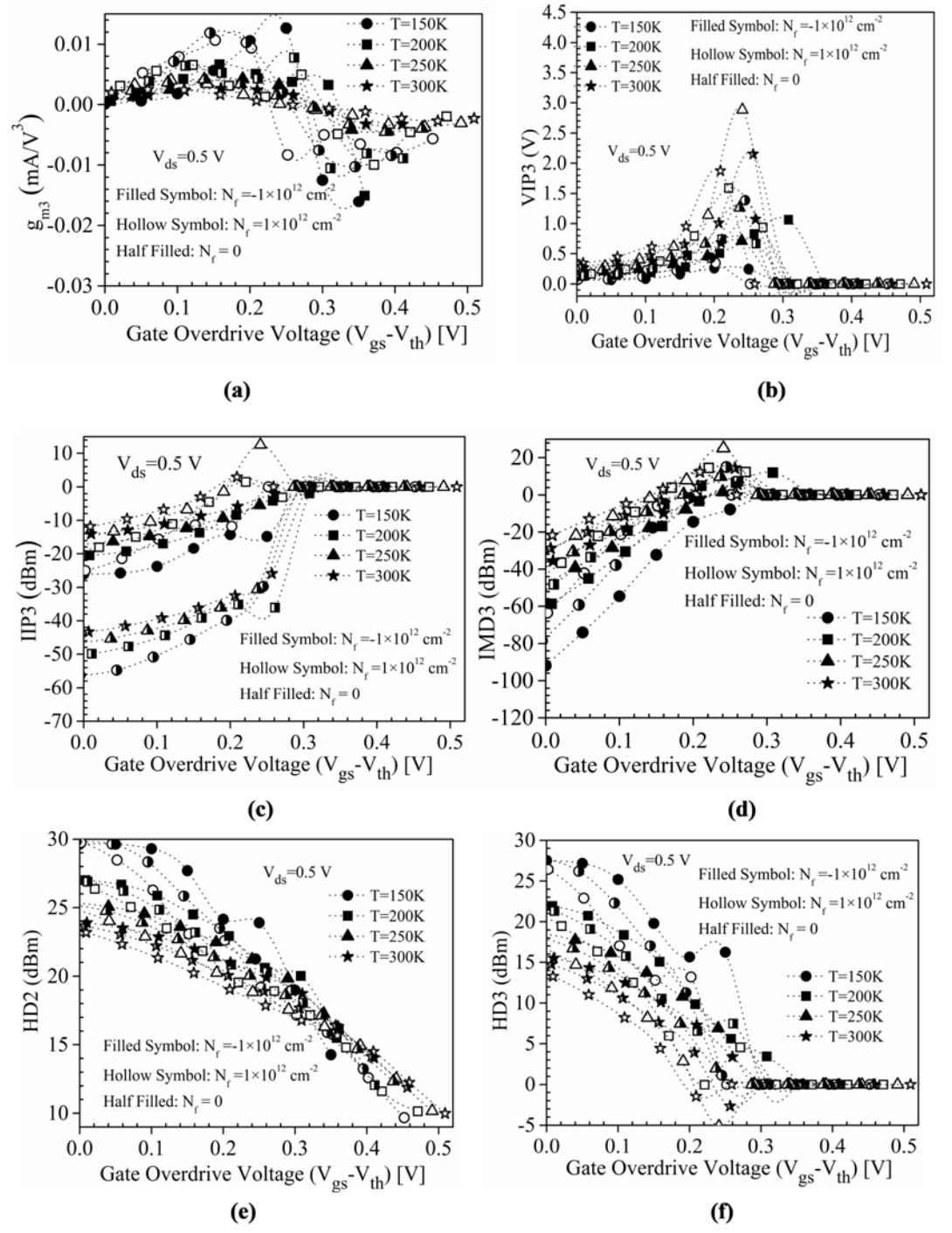


Figure 3.10: Effect of temperature with interface trap charges on (a): g_{m3}, (b): VIP3, (c): IIP3, (d): IMD3, (e): HD2 and (f): HD3 in TGRC-MOSFET (Kumar et al, 2018).

Figure 3.10(b) and **Figure 3.10(c)** reflect the improved performance of TGRC-MOSFET at a lower temperature (< 300 K) in terms of VIP3 and IIP3 respectively in the presence of trap charges. It is found that peak value of VIP3 and IIP3 is enhancing at a low temperature which indicates less distortion and high linearity when the device is working at lower temperatures. Besides, it is also observed that impact of interface trap charges on TGRC's linearity performance at low temperature is less prominent as clearly indicated from **Figure 3.10 (b-c)**. Thus, TGRC-MOSFET acts as a potential candidate for linear amplifiers working at low temperatures in CMOS ULSI. Harmonic distortion is an essential reliability issue which arises due to the non-linear performance of MOSFET. Thus, HD in terms of IMD3, HD2, and HD3 are examined as a function of both temperature and interface trap charges and are illustrated in **Figure 3.10(d)**, **Figure 3.10(e)**, and **Figure 3.10(f)** respectively. Change in ambient temperature plays a major role in amplifiers working in communication systems and sometimes it causes an undesirable change in signals and thus causes distortion in the band of interest. This is due to random motion of electrons which results in thermal noise within the device and thus, degrades the device performance. At low temperatures (<300 K), harmonic distortions (IMD3, HD2 and HD3) is reduced in TGRC-MOSFET as evident from **Figure 3.10(d)**, **Figure 3.10(e)** and **Figure 3.10(f)**. It is also observed that in the presence of positive (negative) trap charges, g_{m3} lowers (increase) owing to improved (reduce) current driving capability and thus lowers (rise) the distortion. This effect is more at low temperatures in TGRC due to enhancement in transconductance and reduction in g_{m3} [see **Figure 3.10(a)**].

3.4.4 Influence of Interface Trap Charge's Polarity and Density

The influence of ITCs polarity and density is observed on TGRC-MOSFET. It is observed From **Figure 3.11(a-b)** that, in the presence of positive trap charges, drain current enhances significantly due to the more (low) control of gate bias voltage. Drain current further increases (decreases) with an increase in positive (negative) trap charge density as shown in **Fig 3.11(a-b)**. It is found that input and output characteristics are more prone to positive charges in comparison to negative charges. **Figure 3.12(a-b)** reflects the effect of trap charges polarity/density on linearity

FOMs. **Figure 3.12(a)** shows that the transconductance (g_m) is high (low) for positive (negative) traps owing to reduced (enhanced) flat band voltage due to more (low) gate bias. To assure higher linearity, higher order transconductance coefficient (g_{m3}) must be minimal because g_{m3} decides the dc bias point for optimal operation of the device and regulates the limits on the distortion. It is apparent from **Figure 3.12(b)** that in the existence of positive (negative) trap charges, g_{m3} peak reduces (enhances) appreciably and the effect of density variation is more (less) observed for positive (negative) trap charge density. Thus, signifies that TGRC-MOSFET is less prone to negative trap density.

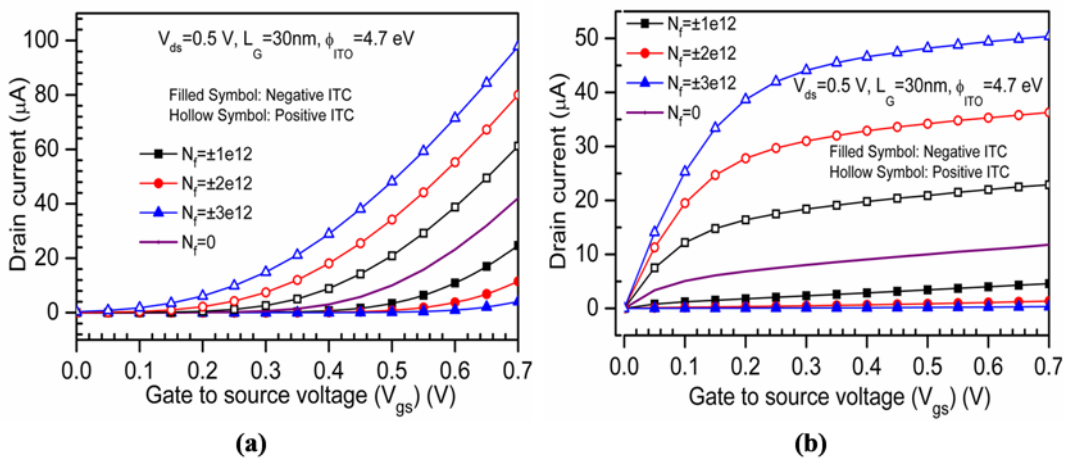


Figure 3.11: (a) Transfer characteristics w.r.t. source voltage (V_{gs}), (b) Output characteristics w.r.t. source voltage (V_{ds}) for TGRC-MOSFET (Kumar et al, 2017a).

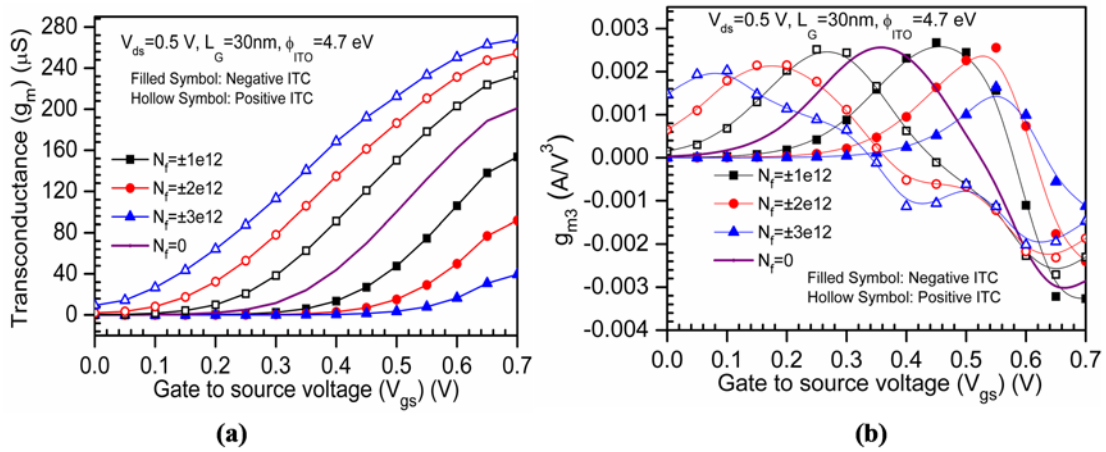


Figure 3.12: Impact of interface trap charges for TGRC-MOSFET on (a) transconductance (g_{m1}) and (b) g_{m3} (Kumar et al, 2017a).

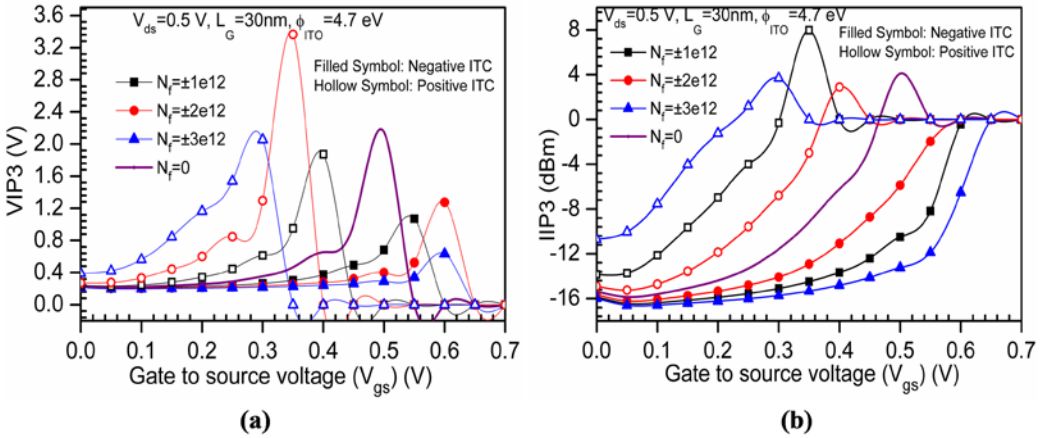


Figure 3.13: Impact of interface trap charges for TGRC-MOSFET on (a) VIP3 and (b) IIP3 (Kumar et al, 2017a).

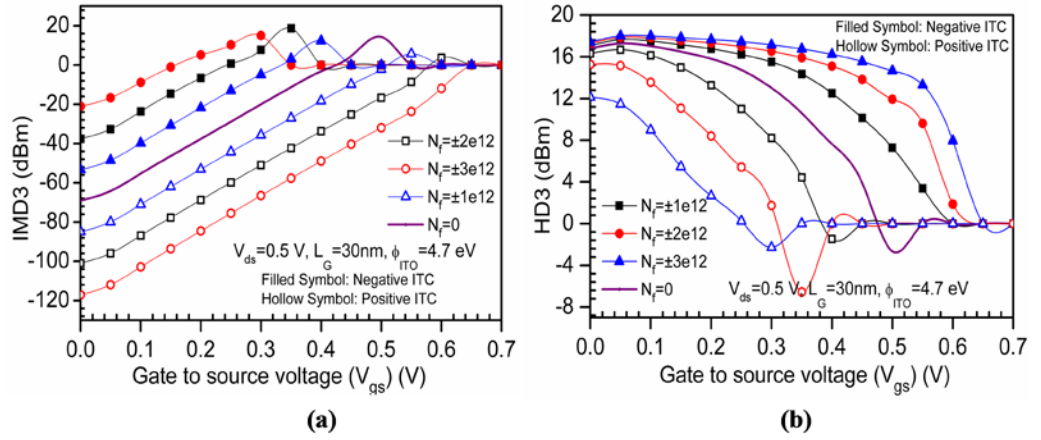


Figure 3.14: Impact of interface trap charges for TGRC-MOSFET on (a) IMD3, and (b) HD3 (Kumar et al, 2017a).

From the dc parameters, VIP3 is used to evaluate the distortion characteristics. Higher VIP3 and IIP3 but lower IMD3 and HD3 are required for lower distortion. The device linearity FOMs are evaluated from Equation (4) and (5) (Chaujar et al, 2009). The peak amplitude of VIP3 and IIP3 is higher for higher trap density as compared to lower trap density, and it is also found that in the presence of positive trap charges, linearity performance improves owing to improved current driving capability but more reliable for negative trap charges as shown in **Figure 3.13(a)** and **3.13(b)**. In addition, IMD3 is also analyzed considering the influence of both interface trap density and polarity. IFM is used for the calculation of the distortion since this approach is an authorization for the extraction of distortion from DC measurements deprived of an AC characterization, dissimilar to Fourier-based methods (Cerdeira et

al, 2004) as shown in Equation (6) and (8). **Figure 3.14(a)** reveals that IMD3 reduces in TGRC-MOSFET owing to the reduced g_{m3} value in comparison to VIP3 which dominates the value of IMD3 (**Figure 3.12(b)**). Meanwhile, it is also observed that TGRC shows reduced (increase) HD3 when positive (negative) trap charges are considered with high density and exhibit a very little effect of traps charges as shown in **Figure 3.14(b)**. TGRC exhibits improved linearity and distortion-less performance in the presence of negative trap charge density. Thus, TGRC is more reliable for negative traps as compared to positive traps.

3.5 SUMMARY

In this chapter, the influence of interface trap charges on the static, linearity, and distortion FOMs have been studied to explore the reliability issues of TGRC-MOSFET. The performance of this device has also been compared with conventional recessed channel (CRC) MOSFET through extensive device simulation. The proposed device is suitable for high switching applications even in the presence of trap charges. It has been shown that the TGRC-MOSFET exhibit superior current driving capability, high linearity (VIP3 and IIP3) with low distortions. It has also been observed that TGRC-MOSFET is more immune to interface trap charges even in the density variation with different polarity (acceptor and donor). Likewise, it is also found that TGRC-MOSFET at low temperature (150K) in the presence of interface trap charges show negligible variation in device behavior in terms of I_{ds}, g_m, VIP3, IIP3, HD2, HD3, and IMD3. Thus, it signifies that TGRC-MOSFET is more reliable at low temperatures and serves as a promising candidate for analog and low power-high linearity applications.

Further, as downscaling of CMOS devices not only promises high integration but must also provide high switching performance with reduced parasitic capacitances. Additionally, the rising interest of high ULSI applications motivates to analyze the stray capacitance of nano scaled MOSFET and is the central point of discussion for the next chapter of this thesis.

3.6 REFERENCES

Appenzeller, J., Martel, R., Avouris, P., Knoch, J., Scholvin, J., del Alamo, J. A., Rice, P. & Solomon, P. (2002) Sub-40 nm SOI V-groove n-MOSFETs. *IEEE Electron Device Letters*, 23(2), 100-102.

Arora, N. (1993) MOSFET Models for VLSI Circuit Simulation Theory and Practice Springer. *New York*.

Cerdeira, A., Alemán, M. A., Estrada, M. & Flandre, D. (2004) Integral function method for determination of nonlinear harmonic distortion. *Solid-State Electronics*, 48(12), 2225-2234.

Chaujar, R., Kaur, R., Saxena, M., Gupta, M. & Gupta, R. (2009) TCAD assessment of Gate Electrode Workfunction Engineered Recessed Channel (GEWE-RC) MOSFET and its multi-layered gate architecture, Part II: Analog and large signal performance evaluation. *Superlattices and Microstructures*, 46(4), 645-655.

Chiang, T.-K. (2011) A compact model for threshold voltage of surrounding-gate MOSFETs with localized interface trapped charges. *IEEE Transactions on Electron Devices*, 58(2), 567-571.

Doria, R. T., Cerdeira, A., Raskin, J.-P., Flandre, D. & Pavanello, M. A. (2008) Harmonic distortion analysis of double gate graded-channel MOSFETs operating in saturation. *Microelectronics Journal*, 39(12), 1663-1670.

Elewa, T., Balestra, F., Cristoloveanu, S., Hafez, I. M., Colinge, J.-P., Auberton-Herve, A.-J. & Davis, J. R. (1990) Performance and physical mechanisms in SIMOX MOS transistors operated at very low temperature. *IEEE Transactions on Electron Devices*, 37(4), 1007-1019.

Groeseneken, G., Colinge, J.-P., Maes, H. E., Alderman, J. & Holt, S. (1990) Temperature dependence of threshold voltage in thin-film SOI MOSFETs. *IEEE Electron Device Letters*, 11(8), 329-331.

Gupta, N. & Chaujar, R. (2016a) Investigation of temperature variations on analog/RF and linearity performance of stacked gate GEWE-SiNW MOSFET for improved device reliability. *Microelectronics Reliability*, 64, 235-241.

Gupta, N. & Chaujar, R. (2016b) Optimization of high-k and gate metal workfunction for improved analog and intermodulation performance of Gate Stack (GS)-GEWE-SiNW MOSFET. *Superlattices and Microstructures*, 97, 630-641.

Jo, H., Choi, S., Rhee, S. & Park, Y. J. (2017) An Analytical Model for the Threshold Voltage of Intrinsic Channel MOSFET Having Bulk Trap Charges. *IEEE Transactions on Electron Devices*, 64(5), 2113-2120.

Kumar, A. (2017) Effect of Trench Depth and Gate Length Shrinking Assessment on the Analog and Linearity Performance of TGRC-MOSFET. *Superlattices and Microstructures*.

Kumar, A., Gupta, N. & Chaujar, R. (2016a) Analysis of novel transparent gate recessed channel (TGRC) MOSFET for improved analog behaviour. *Microsystem Technologies,* 22(11), 2665-2671.

Kumar, A., Gupta, N. & Chaujar, R. (2016b) Power gain assessment of ITO based Transparent Gate Recessed Channel (TGRC) MOSFET for RF/wireless applications. *Superlattices and Microstructures*, 91, 290-301.

Kumar, A., Tripathi, M. & Chaujar, R. (2017a) Influence of interface trap charge density on reliability issues of transparent gate recessed channel (TGRC) MOSFET, *Microelectronic Devices, Circuits and Systems (ICMDCS), 2017 International conference on*. IEEE.

Kumar, A., Tripathi, M. & Chaujar, R. (2017b) Investigation of parasitic capacitances of In2O5Sn gate electrode recessed channel MOSFET for ULSI switching applications. *Microsystem Technologies*, 23(12), 5867-5874.

Kumar, A., Tripathi, M. & Chaujar, R. (2018) Reliability Issues of In2O5Sn Gate Electrode Recessed Channel MOSFET: Impact of Interface Trap Charges and Temperature. *IEEE Transactions on Electron Devices*, 65, 860-866.

Lho, Y. H. & Kim, K. Y. (2005) Radiation effects on the power MOSFET for space applications. *ETRI journal*, 27(4), 449-452.

Poindexter, E. H. (1989) MOS interface states: overview and physicochemical perspective. *Semiconductor Science and Technology*, 4(12), 961.

Razavi, B. & Behzad, R. (1998) *RF microelectronics, 1*Prentice Hall New Jersey.

Shabde, S., Bhattacharyya, A., Kao, R. S. & Muller, R. S. (1988) Analysis of MOSFET degradation due to hot-electron stress in terms of interface-state and fixed-charge generation. *Solid-state electronics*, 31(11), 1603-1610.

SILVACO, I. (2011) ATLAS User's Manual. *Santa Clara, CA, Ver*, 5.

Sze, S. M. & Ng, K. K. (2006) *Physics of semiconductor devices*John wiley & sons.

Trabzon, L. & Awadelkarim, O. (1998) Damage to n-MOSFETs from electrical stress relationship to processing damage and impact on device reliability. *Microelectronics Reliability*, 38(4), 651-657.

Van Langevelde, R. & Klaassen, F. (1997a) Accurate drain conductance modeling for distortion analysis in MOSFETs, *Electron Devices Meeting, 1997. IEDM'97. Technical Digest., International*. IEEE.

Van Langevelde, R. & Klaassen, F. M. (1997b) Effect of gate-field dependent mobility degradation on distortion analysis in MOSFETs. *IEEE Transactions on Electron Devices*, 44(11), 2044-2052.

4

CHAPTER

Investigation of Parasitic Capacitances of In_2O_5Sn Gate Electrode Recessed Channel MOSFET for ULSI Switching Applications

- *This chapter discusses the capacitance-voltage (C-V) analysis and frequency dependent capacitance of In_2O_5Sn gate electrode Recessed Channel (TGRC) MOSFET.*
- *Here our aim is to examine the effectiveness of In_2O_5Sn as a gate material on parasitic capacitance which prominently influences the current driving capability and thus, the switching performance.*
- *Moreover, capacitance dependent parameters such as Transconductance Frequency Product (TFP), Energy Delay Product (EDP) and Gain Bandwidth Product (GBP) are also assessed.*
- *In addition, the effect of parameter variation such as gate length (L_G) and negative junction depth (NJD) of TGRC is also observed.*
- *Results reveal that with L_G=20 nm and NJD=5 nm, TGRC unveils outstanding switching performance which is desirable for low power ULSI applications.*

4.1 INTRODUCTION

As discussed in **Chapter 1**, shrinking of device dimensions is the main driving force towards circuit miniaturization, low cost, and portability (Moore, 1975). As the dimensions of CMOS device reduces, scaling of silicon-based MOSFET devices for barrier potential, critical electric field, oxide thickness, the threshold voltage becomes tougher (Iwai, 2009). To overcome these limitations, numerous techniques are being proposed by researchers. Some of them include modification on the existing structure and technology; and on the other hand, incorporation of some new material instead of prevailing material (Woerlee et al, 2001). These include multi-gate MOSFET proposed by Barsan in 1981 (Barsan, 1981), SOI MOSFET by An et al. in 2003 (An et al, 2003), GAA MOSFET by Auth et al. in 1997 (Auth & Plummer, 1997), and Silicon Nanowire MOSFET by Hu et al. in 2002(Gupta et al, 2015; Hu et al, 2004; Hu et al, 2003) etc., to overcome the scaling problems at nano-regime. However, Recessed Channel (RC) MOSFET (Chaujar et al, 2008) comes in to the existence and appreciably eliminated short channel effects (SCEs) and hot carrier effects (HCEs) due to the existence of trench channel which separates the source and drain regions. Although RC-MOSFET has its own limitations that it hinders the current driving capability, to overcome this limitation, there is a need of integrating some engineering scheme onto RC-MOSFET. Therefore, In_2O_5Sn (Indium tin oxide) as a gate metal is amalgamated onto RC-MOSFET and as a result, TGRC-MOSFET (Kumar et al, 2015; 2016a; b) comes into existence.

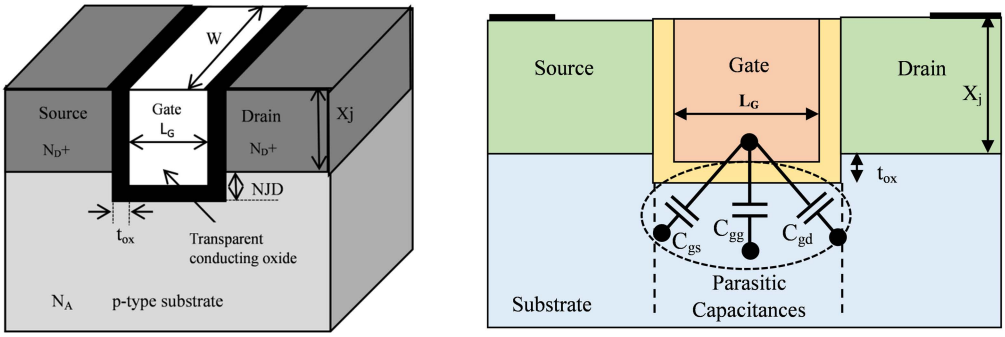
As device dimensions go into sub-30 nm range, the parasitic capacitances become more protruding, which thus affects the device performance and makes the device unsuitable for switching and low power applications. As the channel length scales down, the gate control over the channel gets reduced due to the increased source/drain capacitances (Murali & Meindl, 2007). Therefore, there is a need to perform and study the capacitance-voltage (C-V) analysis which is more advantageous over current-voltage analysis (Steinke et al, 2012) to scrutinize the effects of parasitic capacitances on device performance.

In this work, for the first time, a highly conductive and transparent material

(ITO) is used as a gate electrode in RC-MOSFET to analyse the effect of parasitic capacitances (both bias dependent and frequency dependent). ITO (In_2O_5Sn) is made of indium oxide (In_2O_3) and tin oxide (SnO_2), and it needs lowest deposition temperature (Murali & Meindl, 2007; Singh et al, 2006). ITO has a high concentration of the order of 10^{21} cm^{-3} and a very low resistivity (10^{-5} Ω-cm) with higher Hall mobility (53.5 cm^2 $V^{-1}s^{-1}$) (Minami, 2005). Due to these properties, ITO is frequently used in semiconductor devices, and today silicon-based MOSFET devices having technology less than 30 nm are common.

Further, the bias-dependent parasitic capacitances of TGRC-MOSFET are extracted and found that parasitic capacitances are reduced appreciably due to the amalgamation of ITO as a gate electrode (in trenched gate) as compared to the aluminium electrode (CRC-MOSFET) at THz frequencies. Further, device comparison in terms of parasitic capacitances and figure of merits (FOMs) such as TFP, EDP, and GBP has been examined.

4.2 DEVICE DESIGN AND ITS DESCRIPTION



(a) **(b)**

Figure 4.1: The schematic simulated structure of TGRC-MOSFET. (b). Cross view of TGRC-MOSFET with parasitic capacitances (Kumar et al, 2017).

A schematic simulated device i.e. TGRC-MOSFET is shown in **Figure 4.1(a)**. **Figure 4.1(b)** shows the cross-sectional view of TGRC-MOSFET with parasitic capacitances. The channel is doped uniformly to $1x10^{17}$ cm^{-3} (p-type) in both (TGRC and CRC

MOSFETs) the devices. The doping in the source and drain region is kept at $5x10^{19}$ cm^{-3}. The gate length is 30 nm, with the total channel length of 54 nm ($L_G+2t_{ox}+2NJD$) and thickness of oxide is 2.0 nm as the default device structure parameters of TGRC and CRC MOSFETs are shown in **Table 4.1**. **Figure 4.1(b)** reflects the parasitic capacitances (C_{gs}, $C_{gd,}$ and C_{gg}) at the gate-source interface, gate-drain interface, and gate-gate interface in the cross-sectional view of TGRC-MOSFET.

Table 4.1: Default simulated structure parameters of TGRC and CRC MOSFETs (Kumar et al, 2017).

Device / Parameters	TGRC	CRC
Gate Length (L_G)	30 nm	
Length of the Source and the Drain region	30 nm	
Device Width (W)	200 nm	
Groove Depth	38 nm	
Negative Junction Depth (NJD)	10 nm	
Substrate Doping (N_A)	$1x10^{17}$ cm^{-3}	
Source/Drain Doping (N_D^+)	$5x10^{19}$ cm^{-3}	
Physical Oxide Thickness (t_{ox})	2 nm	
Work function	4.7 eV (ITO)	4.2 eV (Al)

4.3 RESULTS AND DISCUSSION

4.3.1 Impact of In_2O_5Sn on Parasitic Capacitances

Figure 4.2(a) reflects the parasitic capacitances (Kumar et al, 2016b) in terms of gate-source capacitance and gate-drain capacitance. As V_{gs} increases, the accumulation of charge carriers near the gate increases due to which gate-source capacitance and gate-drain capacitance increases. With increase in V_{ds} increases, the pinch-off point moves

towards source side, and it leads to accumulation of charges towards source side resulting in an increment of C_{gs}. To maintain the charge neutrality, the charges near the drain decreases and hence C_{gd} decreases as clearly evident from **Figure 4.2(b)**.

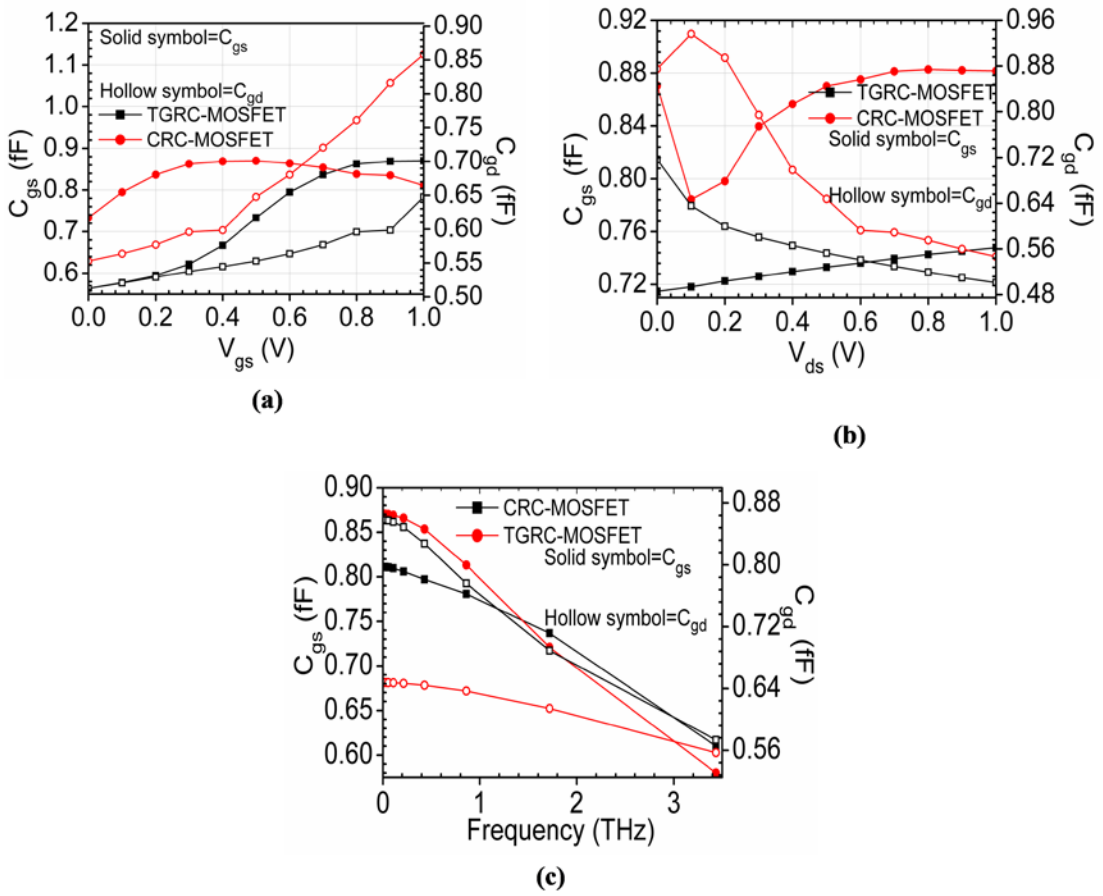


Figure 4.2: C_{gs} and C_{gd} as a function of (a) V_{gs}=1.0V at V_{ds}=0.5V (b) V_{ds}=1.0V at V_{gs}=0.5V (c) frequency at V_{gs}=1.0V, V_{ds}=0.5V; of CRC and TGRC MOSFETs (Kumar et al, 2017).

It is observed that the value of parasitic capacitances in TGRC device is very less as compared to CRC device as shown in **Figure 4.2(a)** due to the high conductivity of ITO which shows that applied voltage is a force to charge carriers in current conduction instead of accumulation near the gate (see **Figure 4.2(a)** and **(b)**) and the same trend follows in ref. (Kundu et al, 2014). So higher switching speed is obtained which also reduces the delay time, making it suitable for the digital applications hence, making TGRC device a promising candidate for switching applications. Further, the variation of C_{gs} and C_{gd} has also been observed with frequency, and it is clearly reflected from **Figure 4.2(c)** that when frequency increases

to the THz range, then both C_{gs} and C_{gd} reduces. The resultant value of C_{gs} and C_{gd} is very less in TGRC as compared to CRC-MOSFET due to the incorporation of ITO as a conducting oxide which indicates the efficacy of transparent material in semiconductor devices for switching applications.

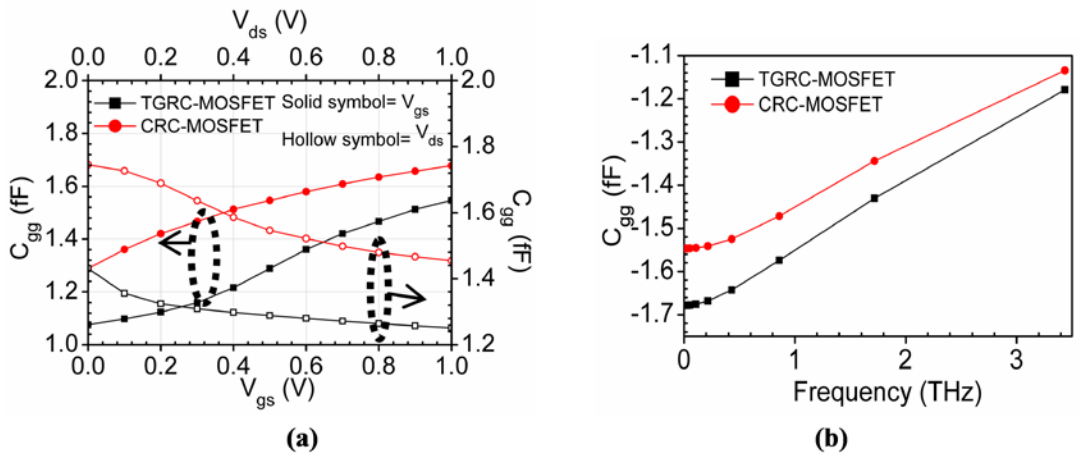


Figure 4.3: Gate Capacitance as a function of (a) V_{gs}=1.0V (V_{ds}=0.5V) and V_{ds}=1.0V (V_{gs}=0.5V) (b) frequency at V_{gs}=1.0V, V_{ds}=0.5V; of CRC and TGRC MOSFETs (Kumar et al, 2017).

Figure 4.3(a) shows the variation of gate capacitance as a function of V_{gs} and V_{ds}. When V_{gs} increases, the accumulation of charges at the gate increases and thus increases the gate capacitance. Moreover, when V_{ds} is increased, the charge carriers near the gate moves towards source side and contributes in drain current thereby lowering the gate capacitance (Marjani & Hosseini, 2014) as can be clearly observed in **Figure 4.3(a)**. It is also noted that, for very high frequency, the gate capacitance is also reduced (3.41%) in TGRC as shown in **Figure 4.3(b)**. Thus, TGRC device is a suitable device for low power switching applications.

A notable capacitance dependent FOM, transconductance frequency product (TFP) for high-frequency performance is given in equation (4.1). TFP is principally the product of device efficiency and f_T (Kumar et al, 2016a). It signifies a trade-off between bandwidth and power and is used for high-speed designs. **Figure 4.4(a)** shows that TFP is increasing as V_{gs} increases in sub-threshold region (below 0.4 V) and in inversion region, TFP attains a peak value of 650 GHz and with further increase in gate bias, i.e., as biasing go in deep inversion region, TFP falls significantly due to increment in C_{gg} [see **Figure 4.3(a)**].

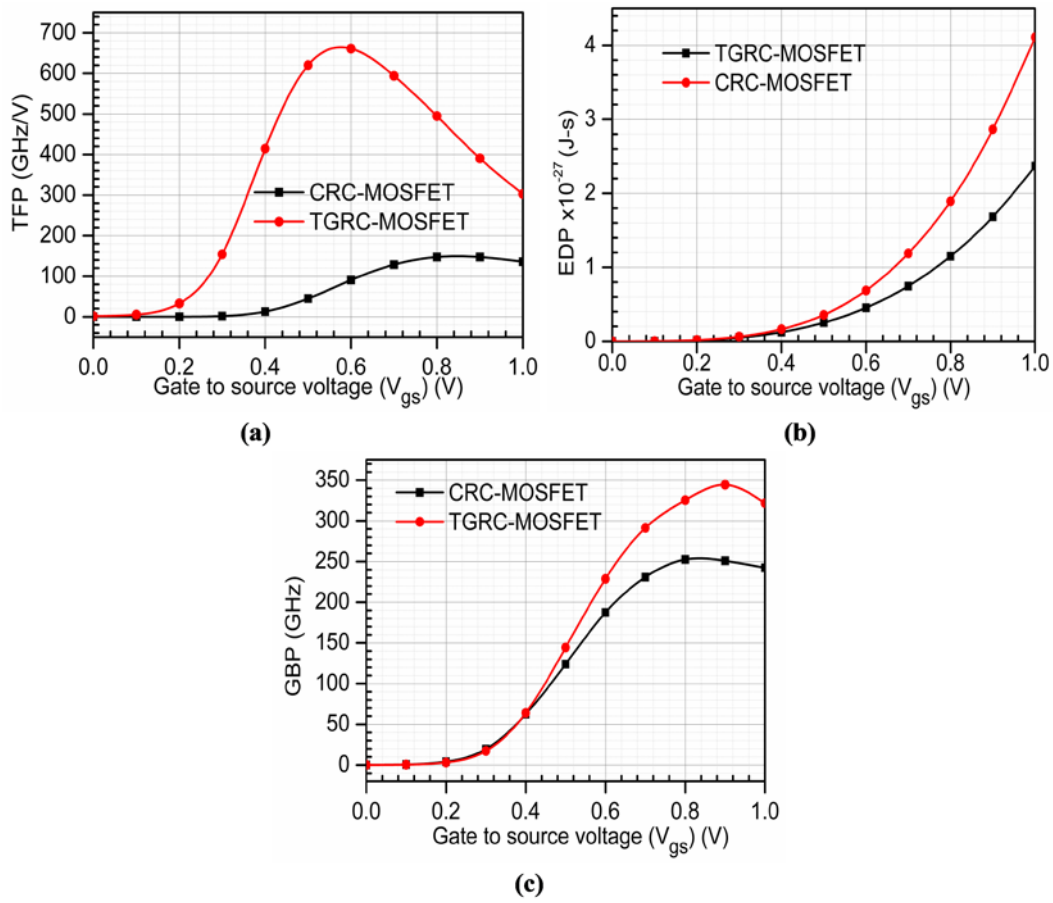


Figure 4.4: (a) TFP, (b) EDP, (c) GBP; at V_{gs}=1.0V, V_{ds}=0.5V as a function of gate to source voltage for CRC and TGRC MOSFETs (Kumar et al, 2017).

It is observed that the peak value of TFP is higher in TGRC-MOSFET due to the high value of transconductance as reported earlier (Kumar et al, 2016b) and reduction in total gate capacitance (which is the sum of C_{gs} and C_{gd}) in the linear region [see **Figure. 4.2(a)**].

$$TFP = \left(\frac{g_m}{I_d}\right) \times \left(\frac{g_m}{2\pi C_{gg}}\right) \tag{4.1}$$

Further, energy-delay product (EDP) [given in equation (4.2)] is a valued parameter as far as circuit applications are concerned. It is a measure of energy and is defined by the product of the average energy (E_{ave}) and the gate delay (τ). It calculates the energy consumed per switching event (such as in logic families). In TGRC, EDP improves at lower drain bias in comparison to CRC-MOSFET as evident from **Figure 4.4(b),** due to a reduction in gate capacitance (C_{gg}) and enhancement in on-current

(Kumar et al, 2015). In addition, **Figure 4.4(c)** shows the Gain Bandwidth Product (GBP) [calculated by equation (4.3)] at different drain bias voltage and is a qualitative measure of both gain and bandwidth of a voltage amplifier. It is perceived that GBP improves at higher drain voltage in TGRC device due to a reduction in C_{gd} [see **Figure 3(a)**]. GBP peak value indicates the frequency at which the device attains maximum gain.

$$EDP = \left(C_{gg} V_d^2\right) \times \left(\frac{C_{gg} V_d}{I_{on}}\right) \tag{4.2}$$

$$GBP = \frac{g_m}{2\pi \times 10 \times C_{gd}} \tag{4.3}$$

4.3.2 Impact of Gate Length (L_G) Miniaturization

Furthermore, the impact of parameter variation on the proposed device is studied in terms of the gate length. As evident from **Figure 4.5(a)** that, when gate length decreases, C_{gs} and C_{gd} decreases as a function of V_{gs}. The similar trend follows in ref. (Cho et al, 2011; Ghosh et al, 2015). When the gate length decreases from 40 nm to 30 nm, C_{gs} decreases by 8.42% and C_{gd} decreases by 3.03%.

Furthermore, when we reduce the gate length from 30 nm to 20 nm, then C_{gs} decreases by 9.31%, and C_{gd} decreases by 3.4%. Thus, shrinking the gate length reduces the parasitic capacitances in TGRC-MOSFET, which leads to increased circuit density in IC fabrication. As we know that, when V_{ds} increases, the pinch-off point moves towards source side and the number of charge carriers accumulates towards source side. Hence C_{gs} increases and C_{gd} decreases as shown in **Figure 4.5(b)**. Thereafter, the gate length variation is observed, and it is clearly evident from the figure that as the gate length reduces C_{gs} and C_{gd} are also reduced. If we reduce the gate length from 40 nm to 30 nm, then 4% and 0.98% decrement is observed in C_{gs} and C_{gd} respectively.

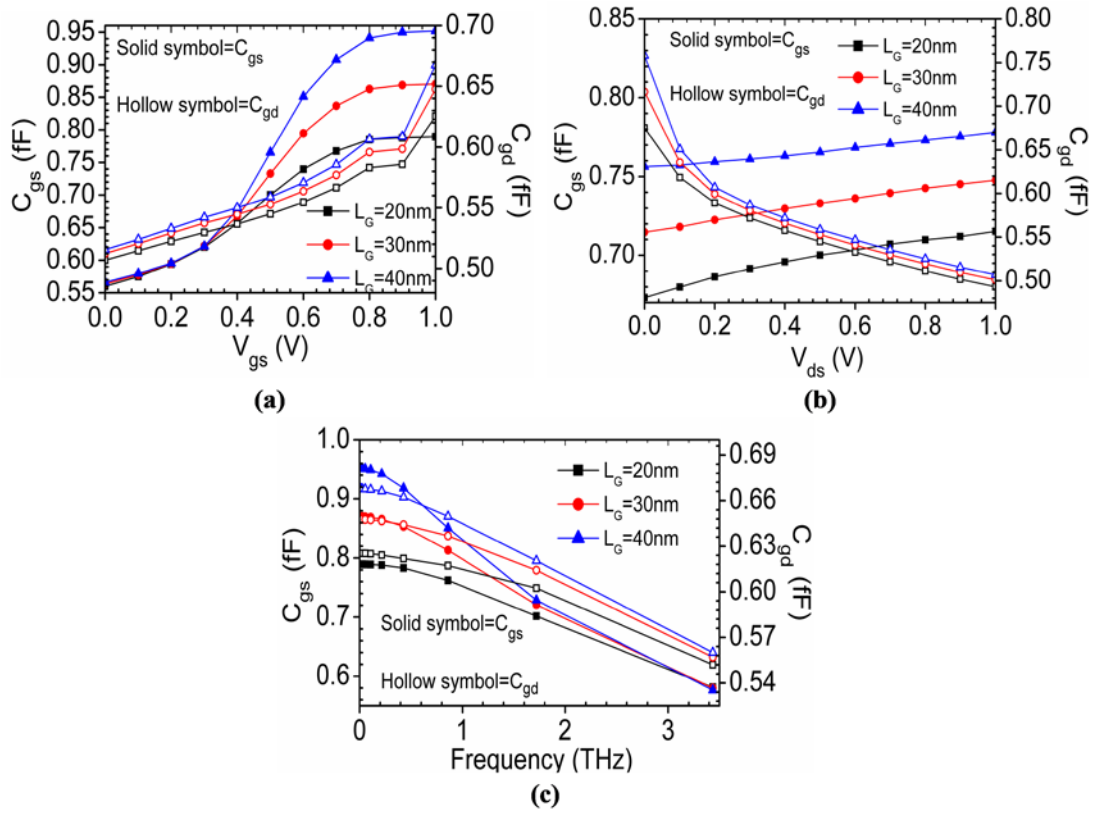


Figure 4.5: C_{gs} and C_{gd} as a function of (a) V_{gs}=1.0V at V_{ds}=0.5V (b) V_{ds}=1.0V at V_{gs}=0.5V (c) frequency at V_{gs}=1.0V, V_{ds}=0.5V; of TGRC-MOSFET for various gate lengths (Kumar et al, 2017).

When gate length further reduces from 30 nm to 20 nm, then 4.28% and 1.59% reduction is observed in C_{gs} and C_{gd} respectively. Further, the impact of gate length variation on parasitic capacitances is observed for very high frequencies (at THz) as shown in **Figure 4.5(c)**. When the frequency is increased in THz range, and gate length reduces from 40 nm to 30 nm, then C_{gs} and C_{gd} are reduced by 7.08% and 2.8% respectively and further 8.2% and 3.5% when gate length varies from 30 nm to 20 nm. Hence, the reduction in parasitic capacitances leads to a device for better switching performances of TGRC-MOSFET, as we scale-down the channel length.

Figure 4.6(a) reflects the parameter variation of TGRC MOSFET in terms of the gate length. It is evident from figure that gate capacitance increases when V_{gs} is increased (Marjani & Hosseini, 2014), and V_{ds} is decreased. As the gate length reduces, and then the gate capacitance is also decreased. If we scale-down the gate length of TGRC MOSFET from 40 nm to 30 nm, then 7.22% and 2.34% decrement is

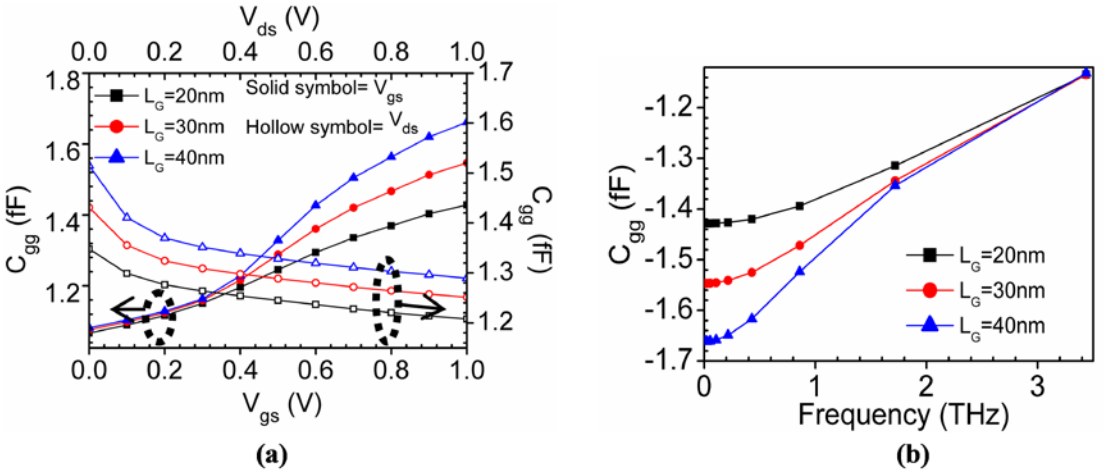


Figure 4.6: Gate Capacitance as a function of (a) V_{gs}=1.0V (V_{ds}=0.5V) and V_{ds}=1.0V (V_{gs}=0.5V) (b) frequency at V_{gs}=1.0V, V_{ds}=0.5V; of TGRC-MOSFET for various gate lengths (Kumar et al, 2017).

-observed in C_{gg} as a function of V_{gs} and V_{ds} respectively. If we further scale-down the gate length from 30 nm to 20 nm, then 7.79% and 4% decrement is reflected in C_{gg} as a function of V_{gs} and V_{ds} respectively.

It is also evident from **Figure 4.6(b)** that, the gate capacitance is also reduced (lower the magnitude) by 6.61% and 7.79% when the gate length scales down from 40 nm to 30 nm and 30 nm to 20 nm respectively at very high frequencies. Therefore, 20 nm gate length device shows that, as we scale-down the device, the parasitic capacitances are reduced, thus making TGRC device a promising device for high-frequency switching applications. Proposed device also leads to increased circuit density in IC fabrication.

Likewise, by scaling down the gate length to 20 nm, TFP and GBP are increased while EDP reduces appreciably as is clear from **Figure 4.7** (Park et al). This enhancement is due to a reduction in gate capacitance and increase in I_{on} [see **Figure 4.2 (a)**]. EDP is further minimized if TGRC is biased in the linear region in comparison to saturation region owing to reduced supply voltage and capacitance coupling, whereas, in cut-off region EDP reduces appreciably as shown in **Figure 4.7(b)**. This is useful in the field of low power switching applications.

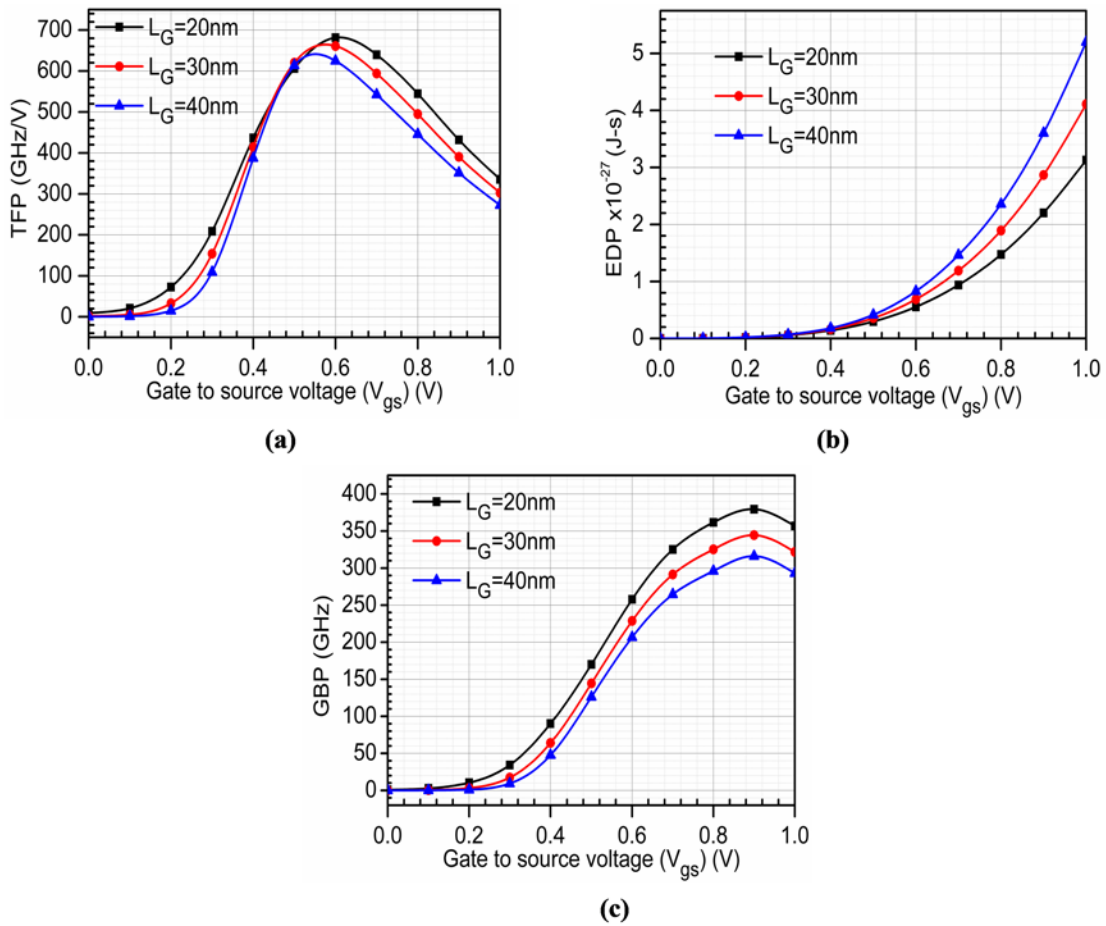


Figure 4.7: (a) TFP, (b) EDP, (c) GBP; as a function of V_{gs}=1.0V (V_{ds}=0.5V) of TGRC-MOSFET for various gate lengths (Kumar et al, 2017).

4.3.3 Impact of Variation of Negative Junction Depth (NJD)

Effects of NJD variation on parasitic capacitances have also been observed in this section of the proposed device. When NJD is reduced, the number of charge carriers move quickly from source to drain because channel length gets reduced with the reduction of NJD and the switching time is also reduced making the device operation faster. **Figure 4.8(a)** shows that the decrease in C_{gs} and C_{gd} is reflected when NJD is reduced from 15 nm to 5 nm, and it is also observed that when V_{gs} increases, the reduction in C_{gs} is increased. If NJD is reduced from 15 nm to 10 nm, C_{gs} and C_{gd} is reduced by 7.27% and 1.6% respectively. Further, reduction in NJD from 10 nm to 5 nm reduces C_{gs} and C_{gd} by 17.21% and 2.22% respectively. Similar kind of reduction in parasitic capacitances is observed when V_{ds} is varied, as evident from **Figure 4.8(b).** When NJD is reduced from 15 nm to 10 nm then, C_{gs} and C_{gd} are reduced by

4.4% and 3.1% respectively. At higher frequencies, C_{gs} and C_{gd} are reduced (by 12.3% and 8.97%) if NJD reduces (from 15 nm to 10 nm) as is reflected from **Figure 4.8(c)**.

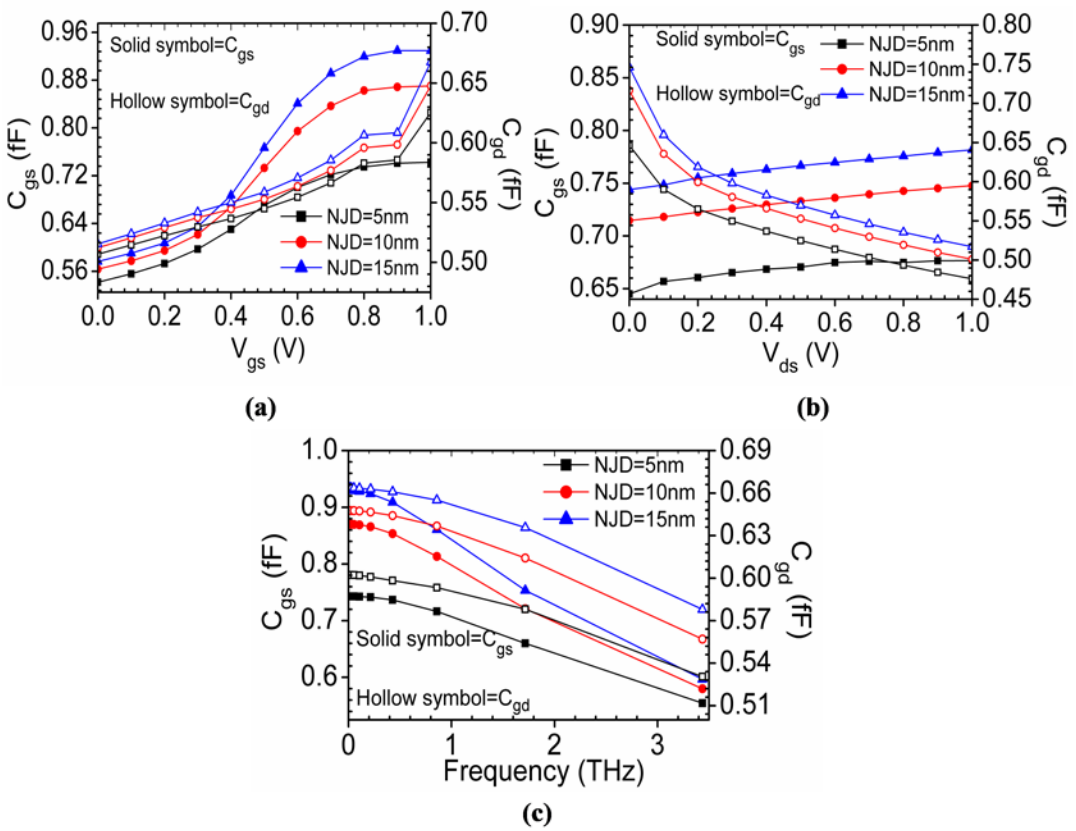


Figure 4.8: C_{gs} and C_{gd} as a function of (a) V_{gs}=1.0V at V_{ds}=0.5V (b) V_{ds}=1.0V at V_{gs}=0.5V (c) frequency at V_{gs}=1.0V, V_{ds}=0.5V; of TGRC-MOSFET at various NJDs (Kumar et al, 2017).

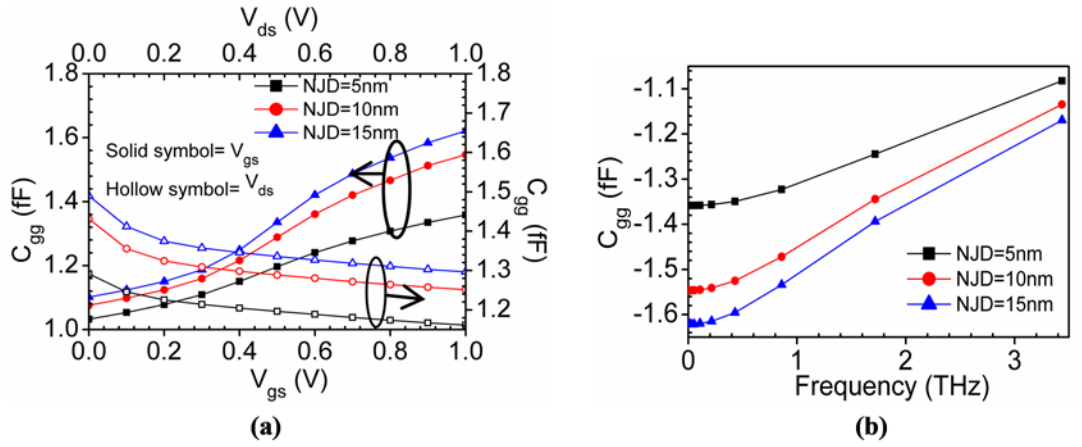


Figure 4.9: Gate Capacitance as a function of (a) V_{gs}=1.0V (V_{ds}=0.5V) and V_{ds}=1.0V (V_{gs}=0.5V) (b) frequency at V_{gs}=1.0V, V_{ds}=0.5V; of TGRC-MOSFET for various NJDs (Kumar et al, 2017).

Moreover, the gate capacitance is investigated at different NJDs, and it is observed when V_{gs} and V_{ds} are applied as shown in **Figure 4.9(a)**. When NJD is reduced from 15 nm to 10 nm then, C_{gg} is reduced by 4.63% and 4.0% w.r.t V_{gs} and V_{ds} respectively. Further, NJD reduction from 10 nm to 5 nm reduces C_{gg} by 13.53% and 8% w.r.t. V_{gs} and V_{ds} respectively as shown in **Figure 4.9(a)**. **Figure 4.9(b)** shows a very high reduction in gate capacitance when NJD scales down at THz frequency range. In addition, a decrease in NJD to 5nm results in an enhancement in TFP and GBP while degrading EDP as shown in **Figure 4.10** (Park et al). From **Figure 4.10(b)**, it is observed that effect of transparent gate scheme strongly affects the EDP. GBP also improves by modulating NJD as is reflected in **Figure 4.10(b)**. It has also been observed that GBP achieve higher value in saturation mode since C_{gd} is lower in saturation mode [see **Figure 4.5** (Park et al)].

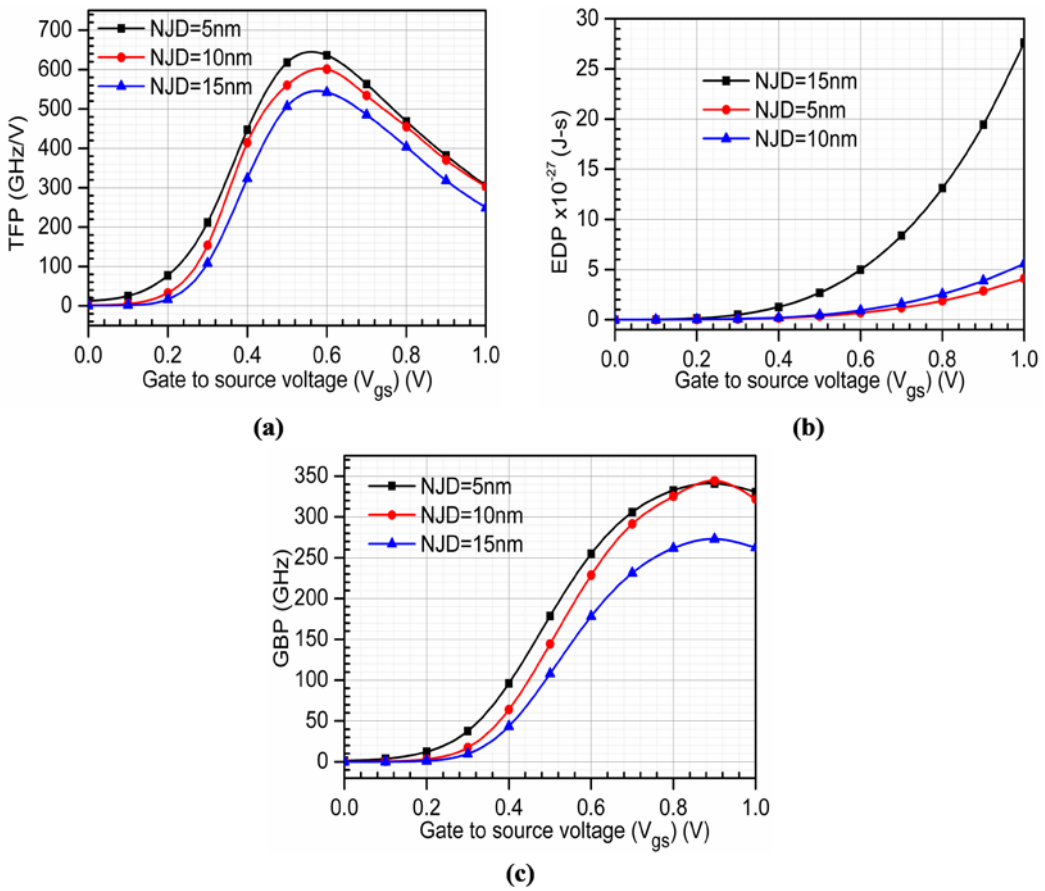


Figure 4.10: (a) Transconductance Frequency Product (TFP), (b) Energy Delay Product (EDP) , (c) Gain Bandwidth Product (GBP); as a function of V_{gs}=1.0V (V_{ds}=0.5V) of TGRC-MOSFET for various NJDs (Kumar et al, 2017).

4.4 SUMMARY

This chapter analyzes the capacitance–voltage characteristics of In_2O_5Sn gate electrode recessed channel MOSFET with 30 nm gate length to examine the parasitic capacitances. The simulated results are then used to isolate the parasitic capacitances. The effect of In_2O_5Sn gate electrode (as a transparent gate electrode) in recessed channel MOSFET has been studied in terms of bias and frequency-dependent parasitic capacitances and capacitance dependent FOMs such as TFP, EDP, and GBP for high switching performance. It is observed that with the amalgamation of In_2O_5Sn with RC MOSFET, parasitic capacitances decrease in comparison to aluminium gate metal (CRC MOSFET). When the gate length reduces to 20 nm, the parasitic capacitances get reduced, and the overall parasitic capacitances reduce in TGRC architecture by ~25%, making the device suitable at sub-20 nm regime. It is also found that with the variation in frequency, parasitic capacitance reduces due to the high current driving capability of TGRC MOSFET; thus, TGRC architecture proves to be a promising contender for high frequency/switching applications in 22 nm node technology.

After achieving the superior switching performance with reduced parasitic capacitances, highly scaled MOSFET that promises the high integration must ensure the excellent RF performance. Thus, to ensure the superior RF/microwave performance and exhaustive understanding, a small signal mathematical modeling has been developed for TGRC-MOSFET, and the developed analytical small signal model is used to analyse various small signal parameters in terms of *S* (scattering) parameters, *Z* (impedance) parameters, *Y* (admittance) parameters, *h* (hybrid) parameters, and RF FOMs which is illustrated in the next chapter**.**

4.5 REFERENCES

An, X., Huang, R., Zhao, B., Zhang, X. & Wang, Y. (2003) Design guideline of an ultra-thin body SOI MOSFET for low-power and high-performance applications. *Semiconductor science and technology*, 19(3), 347.

Auth, C. P. & Plummer, J. D. (1997) Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET's. *Electron Device Letters, IEEE*, 18(2), 74-76.

Barsan, R. M. (1981) Analysis and modeling of dual-gate MOSFET's. *Electron Devices, IEEE Transactions on*, 28(5), 523-534.

Chaujar, R., Kaur, R., Saxena, M., Gupta, M. & Gupta, R. (2008) TCAD assessment of gate electrode workfunction engineered recessed channel (GEWE-RC) MOSFET and its multilayered gate architecture—part I: hot-carrier-reliability evaluation. *Electron Devices, IEEE Transactions on*, 55(10), 2602-2613.

Cho, S., Lee, J. S., Kim, K. R., Park, B.-G., Harris Jr, J. S. & Kang, I. M. (2011) Analyses on small-signal parameters and radio-frequency modeling of gate-all-around tunneling field-effect transistors. *Electron Devices, IEEE Transactions on*, 58(12), 4164-4171.

Ghosh, S., Koley, K. & Sarkar, C. K. (2015) Impact of the lateral straggle on the Analog and RF performance of TFET. *Microelectronics Reliability*, 55(2), 326-331.

Gupta, N., Kumar, A. & Chaujar, R. (2015) Oxide bound impact on hot-carrier degradation for gate electrode workfunction engineered (GEWE) silicon nanowire MOSFET. *Microsystem Technologies*.

Hu, S.-F., Wu, Y.-C., Sung, C.-L., Chang, C.-Y. & Huang, T.-Y. (2004) A dual-gate-controlled single-electron transistor using self-aligned polysilicon sidewall spacer gates on silicon-on-insulator nanowire. *IEEE transactions on nanotechnology*, 3(1), 93-97.

Hu, S., Wu, Y., Sung, C., Chang, C. & Huang, T. (2003) Single-electron transistor using self-aligned sidewall spacer gates on silicon-on-insulator nanowire, *Nanotechnology, 2003. IEEE-NANO 2003. 2003 Third IEEE Conference on*. IEEE.

Iwai, H. (2009) Roadmap for 22nm and beyond. *Microelectronic Engineering*, 86(7), 1520-1528.

Kumar, A., Gupta, N. & Chaujar, R. (2015) Analysis of novel transparent gate recessed channel (TGRC) MOSFET for improved analog behaviour. *Microsystem Technologies*.

Kumar, A., Gupta, N. & Chaujar, R. (2016a) Power gain assessment of ITO based Transparent Gate Recessed Channel (TGRC) MOSFET for RF/wireless applications. *Superlattices and Microstructures*, 91, 290-301.

Kumar, A., Gupta, N. & Chaujar, R. (2016b) TCAD RF performance investigation of Transparent Gate Recessed Channel MOSFET. *Microelectronics Journal*, 49, 36-42.

Kumar, A., Tripathi, M. & Chaujar, R. (2017) Investigation of parasitic capacitances of In2O5Sn gate electrode recessed channel MOSFET for ULSI switching applications. *Microsystem Technologies*, 23(12), 5867-5874.

Kundu, A., Koley, K., Dutta, A. & Sarkar, C. K. (2014) Impact of gate metal work-function engineering for enhancement of subthreshold analog/RF performance of underlap dual material gate DG-FET. *Microelectronics Reliability*, 54(12), 2717-2722.

Marjani, S. & Hosseini, S. E. (2014) Radio-frequency modeling of square-shaped extended source tunneling field-effect transistors. *Superlattices and Microstructures*, 76, 297-314.

Minami, T. (2005) Transparent conducting oxide semiconductors for transparent electrodes. *Semiconductor Science and Technology*, 20(4), S35-S44.

Moore, G. E. (1975) Progress in digital integrated electronics, *Electron Devices Meeting*.

Murali, R. & Meindl, J. D. (2007) Modeling the effect of source/drain junction depth on bulk-MOSFET scaling. *Solid-state electronics*, 51(6), 823-827.

Park, D., King, Y.-c., Lu, Q., King, T.-J., Hu, C., Kalnitsky, A., Tay, S.-P. & Cheng, C.-C. (1998) Transistor characteristics with Ta/sub 2/O/sub 5/gate dielectric. *IEEE Electron Device Letters*, 19(11), 441-443.

Singh, V., Suman, C. & Kumar, S. (2006) Indium Tin Oxide (ITO) films on flexible substrates for organic light emitting diodes, *Proc. of ASID*.

Steinke, D. R., Piccirillo, J., Gausepohl, S. C., Vivekand, S., Rodgers, M. P. & Lee, J. U. (2012) Parasitic capacitance removal of sub-100nm p-MOSFETs using capacitance–voltage measurements. *Solid-State Electronics*, 68, 51-55.

Woerlee, P. H., Knitel, M. J., Van Langevelde, R., Klaassen, D., Tiemeijer, L. F., Scholten, A. J. & Zegers-van Duijnhoven, A. T. (2001) RF-CMOS performance trends. *Electron Devices, IEEE Transactions on*, 48(8), 1776-1782.

5

CHAPTER

RF and Small Signal Behaviour of In_2O_5Sn Gate Electrode Recessed Channel MOSFET

- *This chapter discusses the small signal RF model of Transparent Gate Recessed Channel (TGRC) MOSFET.*
- *Small signal model is studied in terms of microwave parameters such as S (scattering) parameters, Z (impedance) parameters, Y (admittance) parameters, and h (hybrid) parameters with an aim to analyze the behavior of TGRC MOSFET at microwave frequency.*
- *All the results of TGRC-MOSFET have been compared with Conventional Recessed Channel (CRC) MOSFET and modeled results have also been compared with simulation results and found in good agreement with the 3D-simulation results.*
- *Moreover, it is perceived from the results that 99.4% enhancement in the input impedance of TGRC-MOSFET and input admittance is improved by 32.9% in the proposed device in comparison to CRC-MOSFET.*
- *It has also been observed that the transit (cut-off) frequency (f_T) and maximum oscillator frequency (f_{MAX}) enhances significantly by 42.85% and 123% respectively in TGRC MOSFET owing to the remarkable reduction in intrinsic capacitances.*
- *Results reveal that the proposed device design improves the small signal behaviour and thus, may provide detailed insight to RF engineers for microwave applications and testing of RF ports.*

5.1 INTRODUCTION

From past few decades, MOSFETs are commercially used in the field of the microwave, HF applications owing to the fact that highly scaled MOSFETs achieve cut-off frequencies in the range of GHz making CMOS technology appropriate for the application of RF and wireless communications (Adhikari & Singh, 2015b; Kilchytska et al, 2003; Larson, 2003; Saito et al, 1998; Yang et al, 2002). On the contrary, scaling also results in the so-called short channel effects (SCEs), which hampers the device HF performance and make CMOS inapt for Microwave/Wireless applications (Ajayan et al, 2017; Chen, 2013). To overcome this problem, different device schemes have been introduced in recent years which have high immunity against SCEs such as multi-gate MOSFETs, -tapered/recessed channel MOSFET (Adhikari & Singh, 2018), nanowire MOSFET (Gupta & Chaujar, 2016; Gupta et al, 2015a; b), etc. Therefore, there is a need for the new type of device design which overcomes the shortcomings that arise due to downscaling of device dimensions and also simultaneously improves the device's f_T and f_{MAX}.

In our recent work, we have reported that with the incorporation of ITO as a gate electrode onto Recessed Channel MOSFET considerably improves the overall device's electrical performance (Kumar, 2017; Kumar et al, 2016a; b; Kumar et al) and RF performance (Kumar et al, 2016c). Also, the small signal (Adhikari & Singh, 2015a) modeling of TGRC MOSFET has already been studied in our previous work explaining the *Y* and *Z*-parameters (Kumar et al, 2017). Still, there is a need to evaluate all the essential microwave parameters which are essential in understanding the device physics at high frequency. Therefore, in this chapter, detailed explanation and modeling of small signal parameters, i.e., *S*-parameters (Sinnesbichler & Olbrich, 2003; Taher et al, 2006), *Y*-parameters, *Z*-parameters, and *h*-parameters of TGRC-MOSFET are extensively explored and compared with conventional RC MOSFET to study its effectiveness for RF field.

This work is organized as follows: Section 2 describes the 3D device structure of TGRC-MOSFET. Physical transport models invoked during the simulation study (Wei & Lu, 2018) are discussed in Section 3 along with the calibration. Section 4 describes the small signal modeling of TGRC-MOSFET in terms of scattering,

impedance, admittance, hybrid, and transmission parameters. In addition, f_T, f_{MAX} and capacitance is also observed in this section.

5.2 DEVICE DESIGN AND ITS DESCRIPTION

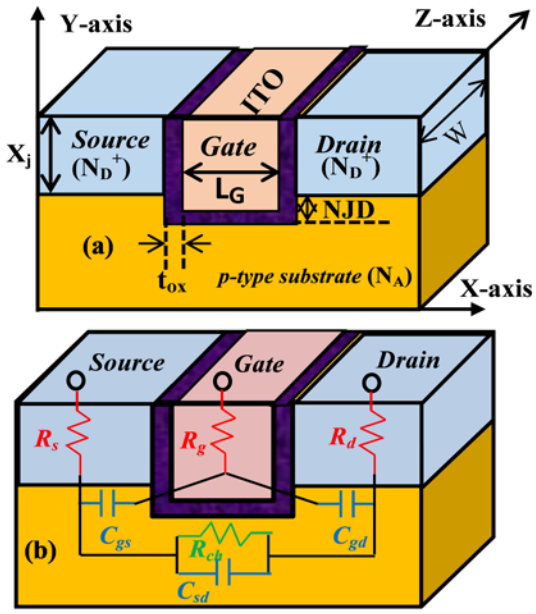


Figure 5.1: (a) Schematic structure and (b) conceptual depiction of the small signal equivalent of TGRC-MOSFET (Kumar et al, 2017; Kumar et al, 2018b).

Figure 5.1(a) and **5.1(b)** reflect the simulated 3D device design and conceptual depiction of the small signal equivalent of TGRC-MOSFET respectively. An n-type impurity of 1×10^{19} cm^{-3} is used in the highly doped Source/Drain region. The substrate is doped with a p-type impurity of 1×10^{17} cm^{-3}, and thick oxide layer t_{ox} of 2.0 nm is embodied in it as shown in **Figure 5.1(a)**. Negative Junction Depth (NJD) is taken as 10 nm, gate bias (V_g) is 0.7 V and drain bias (V_d) is 0.5V. Gate workfunction of TGRC-MOSFET (Φ_{ITO}) is 4.7 eV, and for CRC-MOSFET, it is 4.4eV. All the junctions in the device are assumed as abrupt in the simulation, uniform doping profiles and the biasing conditions are considered at room temperature (T=300K). Further, Gummel and Newton are the two numerical techniques which have been considered to obtain the solutions (SILVACO, 2011).

5.3 SIMULATION METHODOLOGY

All the simulations have been performed using Silvaco TCAD (SILVACO, 2011). The simulation process includes the device structure and functionality. For comparison, we have kept all the parameters of both the devices same such as structural parameters. All simulation models used are same for both the devices. In order to consider the mobilities, scattering mechanism caused by lattice vibrations or phonons, Lombardi CVT model is used. Shockley-Read-Hall (SRH) Recombination model is used to consider all the carrier generation-recombination related phenomenon (SILVACO, 2011). A few other models have also been used to simulate the device precisely.

5.4 RESULTS AND DISCUSSION

5.4.1 Small Signal Behaviour Modeling

For the extraction of RF small signal parameters of TGRC-MOSFET and CRC-MOSFET, Non-quasi-static (NQS) small-signal equivalent circuit (as shown in **Figure 5.2**) of RC MOSFET is used which is operating in strong inversion region (Tsividis & McAndrew, 2011). R_s is the source resistance, R_g is the gate resistance and R_d is the drain resistance, intrinsic gate-to-drain conductance is denoted by g_{ds} whereas g_m denotes transconductance.

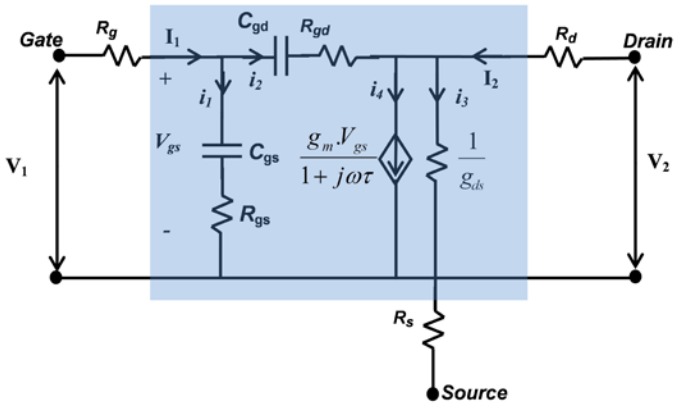


Figure 5.2: Non-quasi-static (NQS) model of the RF MOSFET (RC-MOSFET) (Kumar et al, 2018b).

R_{gs} and R_{gd} have distributed channel resistance; intrinsic gate-to-drain capacitance is denoted by C_{gd} and C_{gs} denotes gate-to-source capacitance. τ is the time constant which represents the charge transport delay (Tsividis & McAndrew, 2011). For those networks which are operating at RF and microwave frequencies, small-signal parameters (*Z*, *Y*, *S*, and *h*) are commonly used, where admittances are more easily computed as compared to voltages and currents, since, at high frequency, it is challenging to estimate currents and voltages.

A. Admittance (Y) Parameters

A small-signal equivalent circuit can describe the transistor at high frequency where MOSFET can be converted in to its *Y*-parameter equivalent circuit consisting of all *Y*-parameters (Y_{11}, Y_{12}, Y_{21} and Y_{22}). *Y*-parameters are defined either at the input end or the output end under ac short-circuit conditions and the values depend on the operating frequency as well as dc bias conditions. AC voltages and currents can be easily measured at low frequencies, but the measurement of these parameters becomes exceptionally difficult at very high frequencies. Then, at such high frequencies, another set of parameters called scattering, or *S*-parameters can be used. However, the device physics and design are more related to *Y*-parameters and so *S*-parameters are again converted in to *Y*-parameters, and hence, the study of *Y*-parameters becomes necessary. By solving the small signal equivalent model (as shown in **Figure 5.2**), *Y*-parameters are calculated as follows:

Total current flowing at the input port,

$$I_1 = i_1 + i_2 \tag{5.1}$$

Total current flowing at the output port,

$$I_2 = i_3 + i_4 - i_1 \tag{5.2}$$

Applying nodal analysis at input node,

$$\frac{V_1}{X_1} + \frac{V_1 - V_2}{X_2} = 0 \tag{5.3}$$

$$\frac{V_2}{X_3} + \frac{V_2 - V_1}{X_2} + \frac{g_m V_{gs}}{1 + j\omega\tau} = 0 \tag{5.4}$$

Where

$$X_1 = \frac{1 + j\omega R_{gs} C_{gs}}{j\omega C_{gs}} \; ; \; X_2 = \frac{1 + j\omega R_{ds} C_{ds}}{j\omega C_{ds}} \; ; \; X_3 = \frac{1}{g_{ds} + j\omega C_{sd}}$$

By solving equation (5.3) and (5.4), and using approximations

$\omega^2 R_{gs}^2 C_{gs}^2 << 1,\ \omega^2 R_{gd}^2 C_{gd}^2 << 1$ and $\omega^2 \tau^2 << 1$

Short circuit input admittance is obtained as

$$Y_{11} \cong \omega^2 (R_{gs} C_{gs}^2 + R_{gd} C_{gd}^2) + j\omega (C_{gs} + C_{gd})$$

$$Y_{11} \cong \omega^2 (\alpha + \beta) + j\omega (C_{gs} + C_{gd}) \tag{5.5}$$

Where, $\alpha = R_{gs} C_{gs}^2, \beta = R_{gd} C_{gd}^2$

Similarly, short circuit output admittance is found to be

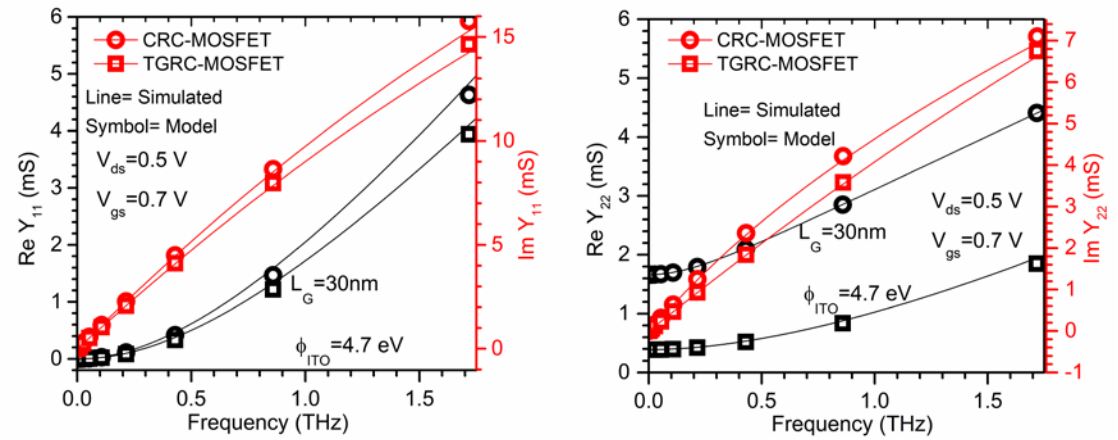
$$Y_{22} \cong g_{ds} + \omega^2 \beta + j\omega (C_{gd} + C_{sd}) \tag{5.6}$$

Short circuit forward transfer admittance is as follows

$$Y_{12} \cong -\omega\beta - j\omega C_{gd} \tag{5.7}$$

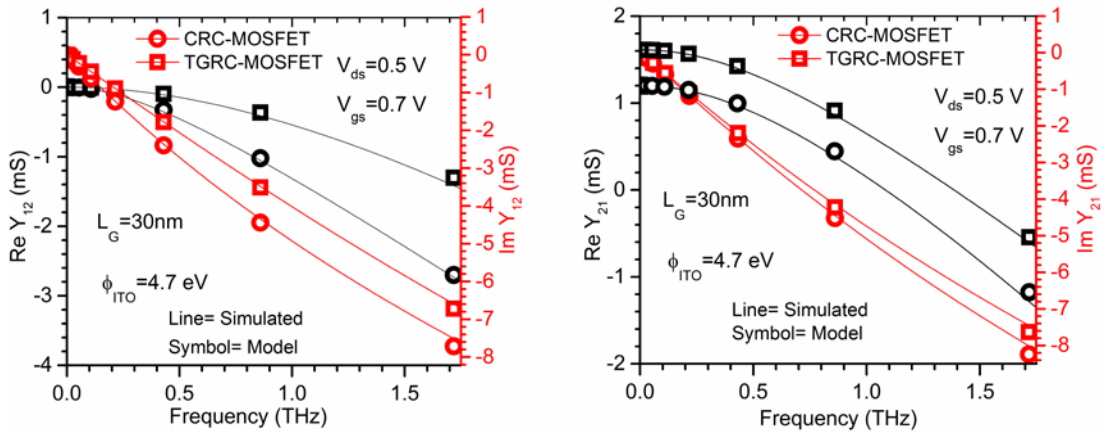
Short circuit reverse transfer admittance is as follows

$$Y_{21} \cong -\omega^2 \beta - j\omega C_{gd} + g_m (1 + \tau) \tag{5.8}$$



(a) **(b)**

Figure 5.3: (a) Y-parameters (Y_{11}) and (b) Y-parameters (Y_{22}), w.r.t. frequency at V_{gs}=0.7 V and V_{ds}=0.5 V for CRC and TGRC-MOSFET (Kumar et al, 2017; Kumar et al, 2018b).



(a) **(b)**

Figure 5.4: (a) Y-parameters (Y_{12}) and (b) Y-parameters (Y_{21}), w.r.t. frequency at V_{gs}=0.7 V and V_{ds}=0.5 V for CRC-MOSFET and TGRC-MOSFET (Kumar et al, 2017; Kumar et al, 2018b).

Y_{11} and Y_{22} are called short-circuit input and output admittance respectively. These parameters have been evaluated for TGRC-MOSFET, and the modeled results are simultaneously compared with CRC-MOSFET. As shown in **Figure 5.3(a)** and **5.3(b)**, Y_{11} and Y_{22} are low in TGRC as a comparison to CRC. Y_{11} and Y_{22} should below for better performance of the device in RF region. Y_{12} is called short-circuit forward transfer admittance, and Y_{21} is called short-circuit reverse transfer admittance. Y_{12} and Y_{21} are both higher in case of TGRC-MOSFET and smaller in CRC-MOSFET as shown in **Figure 5.4(a)** and **5.4(b)**. Enhancement in *Y*-parameters indicates a reduction in parasitic capacitances and enhancement in transconductance (Kumar et al, 2016d; Kumar et al, 2018a).

B. Impedance (Z) Parameters

For the synthesis of electronic filters, Impedance (*Z*) parameters are commonly used. *Z*-parameters can be useful in the design and analysis of power distribution networks and impedance-matching networks. Z_{11} is called open circuit input impedance, and Z_{22} is called open circuit output impedance. These two parameters are basically used for impedance matching. Input impedance should be equal to output impedance for impedance matching, and it is a necessary condition for maximum power transfer from source to load. For high-frequency RF application, Z_{11} (input impedance) should be as high as possible. Input impedance (Z_{11}) must be high and output impedance (Z_{22}) should be low so that no-loading problem occurs in RF receiver.

From the equivalent circuit as shown in **Figure 5.2**, the *Z*-parameters can be analyzed as follows:

Open circuit input impedance (driving point impedance) is found to be

$$Z_{11} \cong \frac{Y_{22}}{\Delta Y} \cong \frac{g_{ds} + \omega^2\beta + j\omega(C_{gd} + C_{sd})}{\begin{aligned} &j\omega(C_{gs}g_{ds} + C_{gd}g_{ds} + C_{gd}g_m + \tau C_{gd}g_m) + \\ &j\omega^3(\alpha C_{gd} + \beta C_{gs} + C_{sd}(\alpha+\beta)) + \alpha\beta\omega^4 \\ &+ \omega^2(\alpha g_{ds} + \beta g_{ds} - C_{gs}C_{sd} - C_{gd}C_{sd} + \beta g_m(1+\tau) + C_{gd}^2) \end{aligned}} \tag{5.9}$$

$$Z_{11} \cong \frac{g_{ds} + \omega^2\beta + j\omega(C_{gd} + C_{sd})}{\chi} \tag{5.10}$$

Open circuit output impedance (driving point impedance):

$$Z_{22} \cong \frac{Y_{11}}{\Delta Y} \cong \frac{\omega^2(\alpha+\beta) + j\omega(C_{gs} + C_{gd})}{\begin{aligned} &j\omega(C_{gs}g_{ds} + C_{gd}g_{ds} + C_{gd}g_m + \tau C_{gd}g_m) + \\ &j\omega^3(\alpha C_{gd} + \beta C_{gs} + C_{sd}(\alpha+\beta)) + \alpha\beta\omega^4 \\ &+ \omega^2(\alpha g_{ds} + \beta g_{ds} - C_{gs}C_{sd} - C_{gd}C_{sd} + \beta g_m(1+\tau) + C_{gd}^2) \end{aligned}} \tag{5.11}$$

$$Z_{22} \cong \frac{\omega^2(\alpha+\beta) + j\omega(C_{gs} + C_{gd})}{\chi} \tag{5.12}$$

Open circuit transfer impedance from input port to output port:

$$Z_{12} \cong \frac{-Y_{12}}{\Delta Y} \cong \frac{\omega\beta + j\omega C_{gd}}{\begin{aligned} &j\omega(C_{gs}g_{ds} + C_{gd}g_{ds} + C_{gd}g_m + \tau C_{gd}g_m) + \\ &j\omega^3(\alpha C_{gd} + \beta C_{gs} + C_{sd}(\alpha+\beta)) + \alpha\beta\omega^4 \\ &+ \omega^2(\alpha g_{ds} + \beta g_{ds} - C_{gs}C_{sd} - C_{gd}C_{sd} + \beta g_m(1+\tau) + C_{gd}^2) \end{aligned}} \tag{5.13}$$

$$Z_{12} \cong \frac{\omega\beta + j\omega C_{gd}}{\chi} \tag{5.14}$$

Open circuit transfer impedance from output to input port:

$$Z_{21} \cong \frac{-Y_{21}}{\Delta Y} \cong \frac{\omega^2\beta + j\omega C_{gd} - g_m(1+\tau)}{\begin{aligned} &j\omega(C_{gs}g_{ds} + C_{gd}g_{ds} + C_{gd}g_m + \tau C_{gd}g_m) + \\ &j\omega^3(\alpha C_{gd} + \beta C_{gs} + C_{sd}(\alpha+\beta)) + \alpha\beta\omega^4 \\ &+ \omega^2(\alpha g_{ds} + \beta g_{ds} - C_{gs}C_{sd} - C_{gd}C_{sd} + \beta g_m(1+\tau) + C_{gd}^2) \end{aligned}} \tag{5.15}$$

$$Z_{21} \cong \frac{\omega^2\beta + j\omega C_{gd} - g_m(1+\tau)}{\chi} \tag{5.16}$$

Where

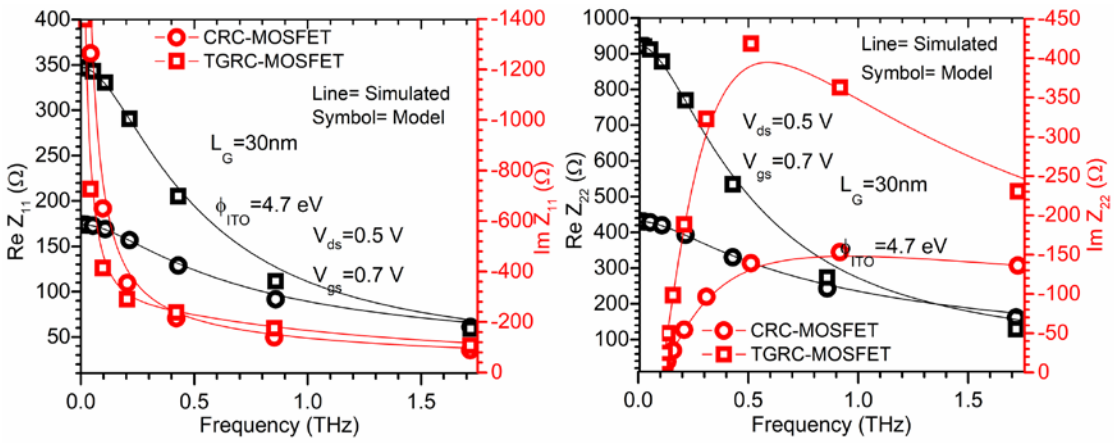
$$\chi = j\omega(C_{gs}g_{ds} + C_{gd}g_{ds} + C_{gd}g_m + \tau C_{gd}g_m) + j\omega^3(\alpha C_{gd} + \beta C_{gs} + C_{sd}(\alpha+\beta)) + \alpha\beta\omega^4$$
$$+ \omega^2(\alpha g_{ds} + \beta g_{ds} - C_{gs}C_{sd} - C_{gd}C_{sd} + \beta g_m(1+\tau) + C_{gd}^2)$$

$$\alpha = R_{gs}C_{gs}^2$$
$$\beta = R_{gd}C_{gd}^2$$

τ = Time constant, represents the charge transport delay

Assume that

$\omega^2 R_{gs}^2 C_{gs}^2 << 1$, $\omega^2 R_{gd}^2 C_{gd}^2 << 1$ and $\omega^2\tau^2 << 1$

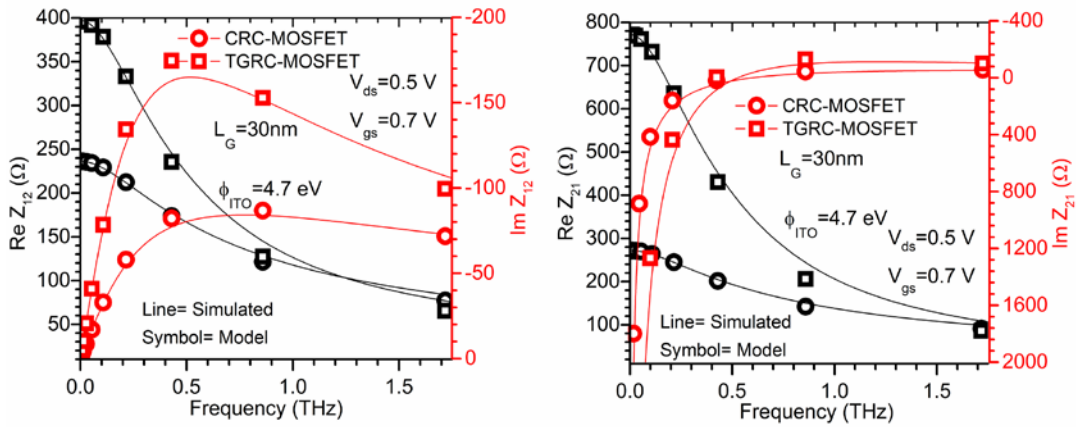


(a) **(b)**

Figure 5.5: (a) Z-parameters (Z_{11}) and (b) Z-parameters (Z_{22}), w.r.t. frequency at V_{gs}=0.7 V and V_{ds}=0.5 V for CRC and TGRC MOSFETs (Kumar et al, 2017; Kumar et al, 2018b).

Figure 5.5(a) and **5.5(b)** reflects the *Z*-parameters Z_{11} and Z_{22} respectively for both CRC and TGRC, and it is observed that Z_{11} and Z_{22} are higher at low frequency and decreases gradually w.r.t. frequency due to the dependency (inversely proportional) of Z_{11} and Z_{22} on ω. The modeled results are well calibrated with the

simulated data for TGRC-MOSFET and its counterpart. **Figure 5.5(a)** shows that input impedance is very high while output impedance is less (as shown in **Figure 5.5(b)**). MOSFET has very high input impedance because of SiO_2, but in TGRC-MOSFET, input impedance also has been increased due to the incorporation of ITO in the grooved gate. If the input impedance of the device is high, it means the device is useful for RF-based receivers in communication systems.



(a) **(b)**

Figure 5.6: (a) Z-parameters (Z_{12}) and 7(b) Z-parameters (Z_{21}), w.r.t. frequency at V_{gs}=0.7 V and V_{ds}=0.5 V for CRC and TGRC MOSFETs (Kumar et al, 2017; Kumar et al, 2018b).

Z_{12} and Z_{21} are called open circuit transfer impedance from the input port to output port and output to input port respectively. Z_{12} and Z_{21} are also called transfer impedances. These two impedance parameters should be high for better RF performance of the device. Z_{12} and Z_{21} both are high in TGRC-MOSFET as compared to its conventional counterpart at hundreds of GHz frequency range, and the modeled data is well calibrated with simulated data as depicted in **Figure 5.6(a)** and **5.6(b)** respectively. Z_{12} and Z_{21} are improved due to the reduction in parasitic capacitances (shown later in **Figure 5.10**) and also due to the incorporation of ITO as a gate metal, which enhances current driving capability, transconductance and hence, gains of the device as reported earlier (Kumar et al, 2016d).

C. Scattering (S) parameters

In order to examine the small signal behavior of MOSFET, extraction of *S*-parameters is the most appropriate method at high frequencies. The behaviour of any microwave

component such as circulator of coupler (3 port network), filter or amplifier (two port network), antenna or oscillator (one port network) etc. are characterised by *S* parameters. **Figure 5.7** shows the modeled and simulated *S*-parameters for the CRC and TGRC-MOSFET and the bias conditions are same as in **Figure 5.2**. Symbols are modeled value and solid lines are simulated ones up to 1.7 THz frequency range. *S*-parameters are calculated using other small signal parameters such as *Y*-parameters and *Z*-parameters (Frickey, 1994). Here we have used *Z*-parameters for the calculation of *S*-parameters as described in equations (5.17) to (5.28).

S-parameters, S_{11} is the input reflection coefficient at port-1 and S_{22} is the output reflection coefficient at port-2. Basically it is the measure of the quality of the match between the port and terminating impedance. These two parameters are obtained using equations (5.17) and (5.20) respectively by using the value of *Z* component from evaluated small signal parameters (from equation (9) to (16)) as required in equation (5.17) and (5.20) and obtained as follows-

$$S_{11} = \frac{(Z_{11} - Z_{01}^{*})(Z_{22} + Z_{02}) - Z_{12}Z_{21}}{(Z_{11} + Z_{01})(Z_{22} + Z_{02}) - Z_{12}Z_{21}} \tag{5.17}$$

$$S_{11} = \frac{\begin{array}{l}(\frac{g_{ds} + \omega^2\beta + j\omega(C_{gd} + C_{sd})}{\chi} - Z_{01}^{*})(\frac{\omega^2(\alpha+\beta) + j\omega(C_{gs} + C_{gd})}{\chi} + Z_{02}) - \\ (\frac{\omega\beta + j\omega C_{gd}}{\chi})(\frac{\omega^2\beta + j\omega C_{gd} - g_m(1+\tau)}{\chi})\end{array}}{\begin{array}{l}(\frac{g_{ds} + \omega^2\beta + j\omega(C_{gd} + C_{sd})}{\chi} + Z_{01})(\frac{\omega^2(\alpha+\beta) + j\omega(C_{gs} + C_{gd})}{\chi} + Z_{02}) - \\ (\frac{\omega\beta + j\omega C_{gd}}{\chi})(\frac{\omega^2\beta + j\omega C_{gd} - g_m(1+\tau)}{\chi})\end{array}} \tag{5.18}$$

$$S_{11} = \frac{\begin{array}{l}(\frac{g_{ds} + \omega^2\beta + j\omega(C_{gd} + C_{sd})}{\chi} - Z_{01}^{*})(\frac{\omega^2(\alpha+\beta) + j\omega(C_{gs} + C_{gd})}{\chi} + Z_{02}) - \\ (\frac{\omega\beta + j\omega C_{gd}}{\chi})(\frac{\omega^2\beta + j\omega C_{gd} - g_m(1+\tau)}{\chi})\end{array}}{\xi} \tag{5.19}$$

$$S_{22} = \frac{(Z_{11} + Z_{01})(Z_{22} - Z_{02}^{*}) - Z_{12}Z_{21}}{(Z_{11} + Z_{01})(Z_{22} + Z_{02}) - Z_{12}Z_{21}} \tag{5.20}$$

$$S_{22} = \frac{\left(\frac{g_{ds}+\omega^2\beta+j\omega(C_{gd}+C_{sd})}{\chi}+Z_{01}\right)\left(\frac{\omega^2(\alpha+\beta)+j\omega(C_{gs}+C_{gd})}{\chi}-Z_{02}^{*}\right)-\left(\frac{\omega\beta+j\omega C_{gd}}{\chi}\right)\left(\frac{\omega^2\beta+j\omega C_{gd}-g_m(1+\tau)}{\chi}\right)}{\left(\frac{g_{ds}+\omega^2\beta+j\omega(C_{gd}+C_{sd})}{\chi}+Z_{01}\right)\left(\frac{\omega^2(\alpha+\beta)+j\omega(C_{gs}+C_{gd})}{\chi}+Z_{02}\right)-\left(\frac{\omega\beta+j\omega C_{gd}}{\chi}\right)\left(\frac{\omega^2\beta+j\omega C_{gd}-g_m(1+\tau)}{\chi}\right)} \quad (5.21)$$

$$S_{22} = \frac{\left(\frac{g_{ds}+\omega^2\beta+j\omega(C_{gd}+C_{sd})}{\chi}+Z_{01}\right)\left(\frac{\omega^2(\alpha+\beta)+j\omega(C_{gs}+C_{gd})}{\chi}-Z_{02}^{*}\right)-\left(\frac{\omega\beta+j\omega C_{gd}}{\chi}\right)\left(\frac{\omega^2\beta+j\omega C_{gd}-g_m(1+\tau)}{\chi}\right)}{\xi} \quad (5.22)$$

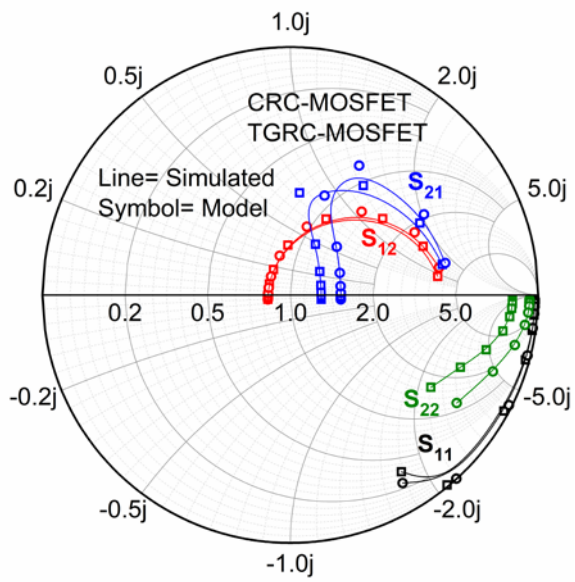


Figure 5.7: Modeled and simulated S-parameters up to 1.7 THz frequency using extracted model parameters and small signal model for CRC and TGRC MOSFETs at V_{gs}=0.7 V and V_{ds}=0.5 V (Kumar et al, 2018b).

Figure 5.7 shows the Smith Chart plot of the real part and imaginary modeled and simulated results of S_{11} and S_{22} for both devices. From **Figure 5.7**, it is clear that both S_{11} and S_{22} reduce the frequency and reduction is more in reflection coefficient in

TGRC device as compared to its counterpart. Modeled and simulated results are matched as evident from **Figure 5.7**. Further, S_{12} (reverse isolation parameter) defines the measure of feedback from the output to the input of an amplifier (Adhikari & Singh, 2017; Pozar, 2009) whereas S_{21} (forward transmission coefficient) is called forward gain of two port device. **Figure 5.7** reflects that S_{12} increases in the proposed device as compared to the conventional device. The enhancement in S_{12} is observed due to the higher value of Z_{12} as shown in **Figure 5.6(a)**. The modeled data and simulated data have been evaluated for S_{21} and plotted in Smith chart up to 1.7 THz frequency for both the devices as shown in **Figure 5.7**.Similarly, S_{12} and S_{21} are evaluated as follows-

$$S_{12} = \frac{2Z_{12}(R_{01}R_{02})^{1/2}}{(Z_{11}+Z_{01})(Z_{22}+Z_{02}) - Z_{12}Z_{21}} \tag{5.23}$$

$$S_{12} = \frac{2(\frac{\omega\beta + j\omega C_{gd}}{\chi})(R_{01}R_{02})^{1/2}}{(\frac{g_{ds}+\omega^2\beta + j\omega(C_{gd}+C_{sd})}{\chi} + Z_{01})(\frac{\omega^2(\alpha+\beta)+j\omega(C_{gs}+C_{gd})}{\chi} + Z_{02}) - (\frac{\omega\beta + j\omega C_{gd}}{\chi})(\frac{\omega^2\beta + j\omega C_{gd} - g_m(1+\tau)}{\chi})} \tag{5.24}$$

$$S_{12} = \frac{2(\frac{\omega\beta + j\omega C_{gd}}{\chi})(R_{01}R_{02})^{1/2}}{\xi} \tag{5.25}$$

$$S_{21} = \frac{2Z_{21}(R_{01}R_{02})^{1/2}}{(Z_{11}+Z_{01})(Z_{22}+Z_{02}) - Z_{12}Z_{21}} \tag{5.26}$$

$$S_{21} = \frac{2(\frac{\omega^2\beta + j\omega C_{gd} - g_m(1+\tau)}{\chi})(R_{01}R_{02})^{1/2}}{(\frac{g_{ds}+\omega^2\beta + j\omega(C_{gd}+C_{sd})}{\chi} + Z_{01})(\frac{\omega^2(\alpha+\beta)+j\omega(C_{gs}+C_{gd})}{\chi} + Z_{02}) - (\frac{\omega\beta + j\omega C_{gd}}{\chi})(\frac{\omega^2\beta + j\omega C_{gd} - g_m(1+\tau)}{\chi})} \tag{5.27}$$

$$S_{21} = \frac{2(\frac{\omega^2\beta + j\omega C_{gd} - g_m(1+\tau)}{\chi})(R_{01}R_{02})^{1/2}}{\xi} \quad (5.28)$$

Where-

$$\xi = (\frac{g_{ds} + \omega^2\beta + j\omega(C_{gd} + C_{sd})}{\chi} + Z_{01})(\frac{\omega^2(\alpha+\beta) + j\omega(C_{gs} + C_{gd})}{\chi} + Z_{02}) -$$
$$(\frac{\omega\beta + j\omega C_{gd}}{\chi})(\frac{\omega^2\beta + j\omega C_{gd} - g_m(1+\tau)}{\chi})$$

and

$$\chi = j\omega(C_{gs}g_{ds} + C_{gd}g_{ds} + C_{gd}g_m + \tau C_{gd}g_m) + j\omega^3(\alpha C_{gd} + \beta C_{gs} + C_{sd}(\alpha+\beta)) + \alpha\beta\omega^4$$
$$+ \omega^2(\alpha g_{ds} + \beta g_{ds} - C_{gs}C_{sd} - C_{gd}C_{sd} + \beta g_m(1+\tau) + C_{gd}^2)$$

D. Hybrid (h) Parameters

Hybrid parameters are based on the dependent variables and are known as so as they are a hybrid combination of current and voltage ratios. Hybrid parameters are very useful for describing transistors using equivalent small signal model. *h*-parameters are much easier than *Z* or *Y* parameters (Alexander & Sadiku, 2013) to measure experimentally for such devices. Further, *h*-parameters have been evaluated in terms of h_{11} (short circuit input impedance), h_{22} (open circuit output admittance), h_{12} (open circuit reverse voltage gain) and h_{21} (short circuit forward current gain); as *h*-parameters deliver a quick estimate of the performance of transistor circuit. Transistor behaves as a linear device for AC small signals because the output AC signal is proportional to the input AC signal. Under such conditions, AC operation of the transistor can be described using *h*-parameters. Using *Y*-parameters, *h*- parameters can also be calculated as described in equations (5.29) to (5.32) (Alexander & Sadiku, 2013).

Short circuit input impedance is obtained from equation (5.5) as follows.

$$h_{11} \cong \frac{1}{Y_{11}} \cong \frac{1}{\omega^2(\alpha+\beta) + j\omega(C_{gs} + C_{gd})} \quad (5.29)$$

Similarly, open circuit output admittance

$$h_{22} \cong \frac{\Delta Y}{Y_{11}} \cong \frac{\begin{matrix} j\omega(C_{gs}g_{ds} + C_{gd}g_{ds} + C_{gd}g_m + \tau C_{gd}g_m) + j\omega^3(\alpha C_{gd} + \beta C_{gs} + C_{sd}(\alpha+\beta)) + \\ \alpha\beta\omega^4 + \omega^2(\alpha g_{ds} + \beta g_{ds} - C_{gs}C_{sd} - C_{gd}C_{sd} + \beta g_m(1+\tau) + C_{gd}^2) \end{matrix}}{\omega^2(\alpha+\beta) + j\omega(C_{gs}+C_{gd})} \quad (5.30)$$

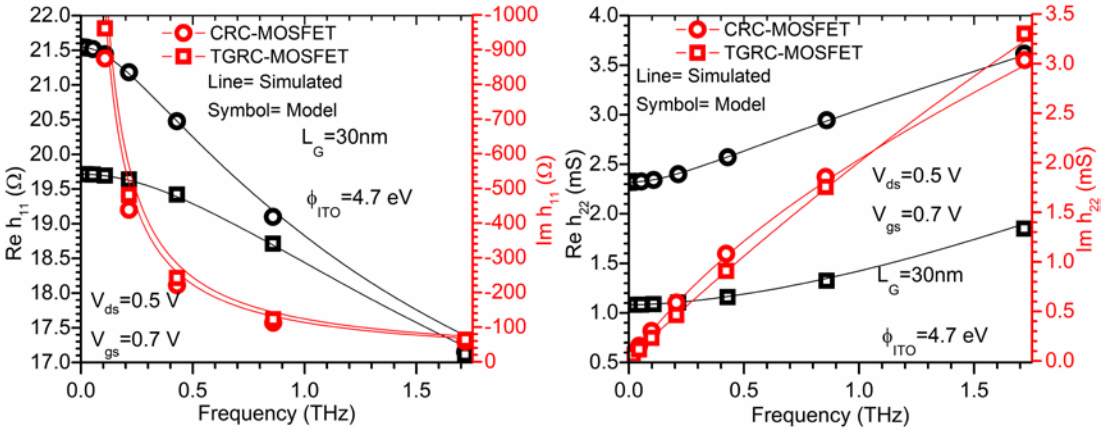
$$h_{22} \cong \frac{\Delta Y}{Y_{11}} \cong \frac{\chi}{\omega^2(\alpha+\beta) + j\omega(C_{gs}+C_{gd})}$$

Open circuit reverse voltage gain

$$h_{12} \cong \frac{-Y_{12}}{Y_{11}} \cong \frac{\omega\beta + j\omega C_{gd}}{\omega^2(\alpha+\beta) + j\omega(C_{gs}+C_{gd})} \quad (5.31)$$

Short circuit forward current gain,

$$h_{21} \cong \frac{Y_{21}}{Y_{11}} \cong \frac{-\omega^2\beta - j\omega C_{gd} + g_m(1+\tau)}{\omega^2(\alpha+\beta) + j\omega(C_{gs}+C_{gd})} \quad (5.32)$$



(a) **(b)**

Figure 5.8: (a) h-parameter (h_{11}) and (b) h-parameter (h_{22}), w.r.t. frequency at V_{gs}=0.7 V and V_{ds}=0.5 V for CRC and TGRC MOSFETs (Kumar et al, 2018b).

The real part of h_{11} and h_{22} of TGRC-MOSFET have been compared with CRC-MOSFET as shown in **Figure 5.8(a)** and **5.8(b)** respectively. It is evident that both h_{11} and h_{22} are less in TGRC as compared to the conventional device. The value of h_{11} is continuously decreased with frequency because h_{11} is inversely proportion to Y_{11} and also to ω^2 as clearly evident from equation (5.29) while h_{22} increases with frequency due to the higher order value of ω as shown in equation (5.30). **Figure 5.9(a)** and **5.9(b)** reflects the real and imaginary part of h_{12} and h_{21} respectively for TGRC-MOSFET and CRC-MOSFET w.r.t. frequency. h_{12} is less in TGRC-MOSFET and increased when the frequency is increased while in CRC-MOSFET, it is reduced

with frequency. For TGRC-MOSFET, h_{21} is lower than CRC-MOSFET and when the frequency is increased, it is reduced due to increase in input impedance [shown in **Figure 5.5(a)**].

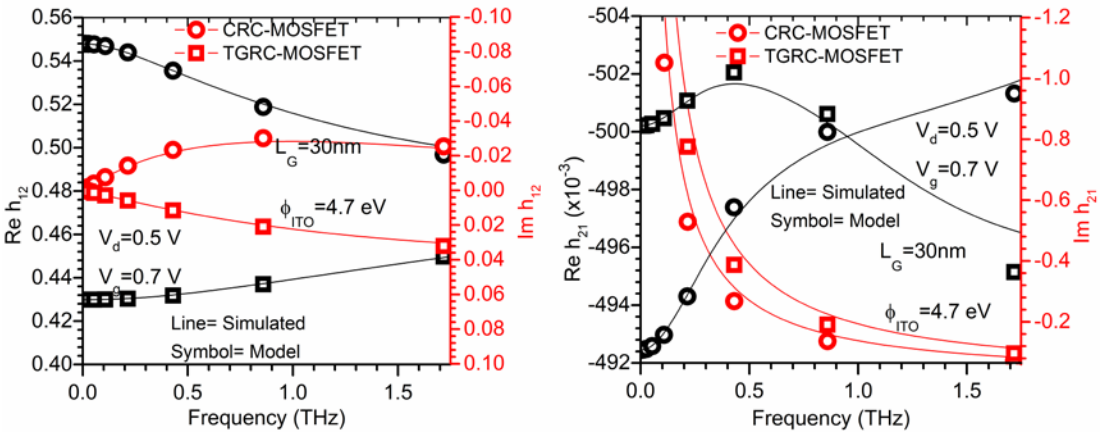


Figure 5.9: (a) h-parameter (h_{12}) and (b) h-parameter (h_{21}), w.r.t. frequency at V_{gs}=0.7 V and V_{ds}=0.5 V for CRC and TGRC MOSFETs (Kumar et al, 2018b).

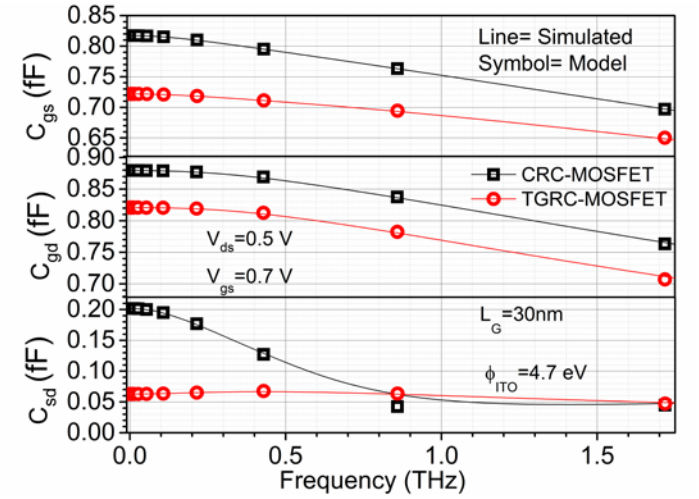


Figure 5.10: RF component (C_{gs}, C_{gd} and C_{sd}) of the small signal equivalent circuit w.r.t. frequency at V_{gs}=0.7 V and V_{ds}=0.5 V for CRC and TGRC MOSFETs (Kumar et al, 2019; Kumar et al, 2018b).

$$C_{gd} = -\mathrm{Im}(Y_{22})/\omega \tag{5.33}$$

$$C_{gs} = (\mathrm{Im}(Y_{11}) + \mathrm{Im}(Y_{12}))/\omega \tag{5.34}$$

$$C_{sd} = (\mathrm{Im}(Y_{22}) + \mathrm{Im}(Y_{12}))/\omega \tag{5.35}$$

Furthermore, with the intensified growth of wireless communication market, CMOS devices must guarantee for the minimum parasitic capacitances and subsequently, the high speed. Thus, to ensure for the superior RF/microwave performance of TGRC-MOSFET, parasitic capacitances have been explored for very high frequency. **Figure 5.10** shows the other bias dependent small signal modeled parameters for TGRC and CRC in terms of C_{gs}, C_{gd} and C_{sd} and compared with simulated data. C_{gs}, C_{gd} and C_{sd} are evaluated by using equations (5.33), (5.34), and (5.35) respectively. From **Figure 5.10**, it is reflected that C_{gs}, C_{gd} and C_{sd} of TGRC-MOSFET turned out to be smaller (in femto-Farad) than that of CRC-MOSFETs. From **Figure 5.10,** it is also found that the modeled data is approximately matched with the simulated data which reveals that the proposed device is suitable for high-frequency (THz) applications.

5.4.2 Extraction of RF FoMs

RF FOMs are essential for basic building blocks of digital RF and analogue circuits. These FOMs do not require equivalent transistor circuit or compact model parameters and can directly be extracted from *Y*-parameters and also can be directly measured without any extrapolation involved (Hurkx et al, 2004). Using the simplified analytical expressions for the *Y*-parameters (from equation (5.5) to (5.8)), we can model analytically different RF FoMs which are very useful for circuit designing.

A. Transit Frequency f_T

Transit frequency (f_T) (Chalkiadaki & Enz, 2015) also called as cut-off frequency (Sarkar & Jana, 2014) is defined as the frequency at which the magnitude of the current gain is equal to unity. It is a measure of maximum useful frequency of a transistor when it is used as an amplifier. f_T of the device is an important design parameter for RF/microwave application, and can be calculate as given in equation (5.36).

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{5.36}$$

where transconductance is denoted by g_m (200 µS for CRC

and 250 µS for TGRC) and parasitic capacitances are denoted by C_{gd} and C_{gs}.

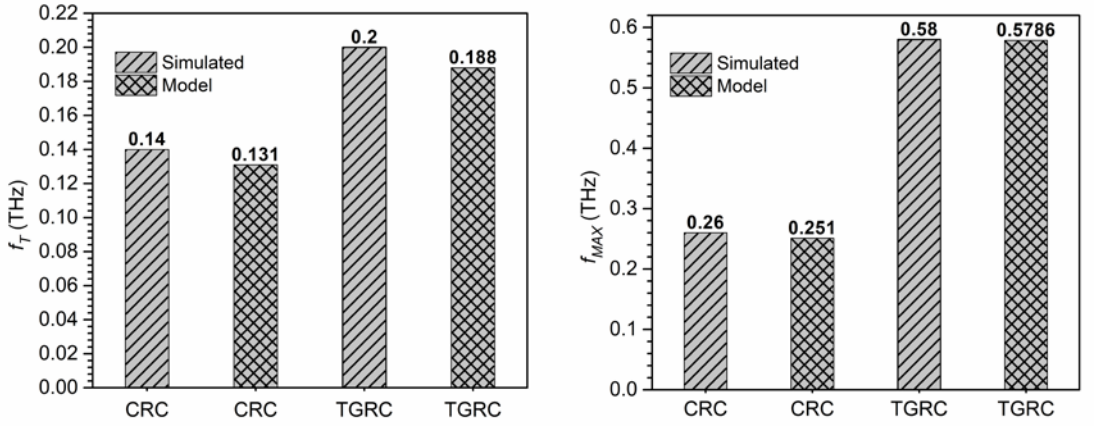


Figure 5.11: (a) Transit frequency. (b) Maximum oscillator frequency at V_{gs}=0.7 V and V_{ds}=0.5 V for CRC-MOSFET and TGRC-MOSFET (Kumar et al, 2019; Kumar et al, 2018b).

Results show that f_T improves 42% in simulated data and 43.5% in modeled data (nearly matched) in TGRC-MOSFET as compared to CRC-MOSFET as reflected in **Figure 5.11(a)** due to reduction in C_{gs} and C_{gd} as reflected in **Figure 5.10**. From equation (5.36), we see that f_T is directly proportion to g_m and hence, higher f_T is obtained due to higher g_m (Kumar, 2017) in TGRC device.

B. Maximum Oscillation Frequency f_{MAX}

For low-current forward transit time, f_T is surely a good indicator. However, it does not include the effects of gate resistance (R_g) as a performance indicator, which is important in determining the transient response of a transistor. Therefore, an indicator called maximum oscillator frequency (f_{MAX}) has been proposed including R_g effects. f_{MAX} is also defined as the frequency at which the unilateral gain become equal to unity (Chalkiadaki & Enz, 2015) and by using small signal components, f_{MAX} is given as in equation (5.37).

$$f_{MAX} = \frac{f_T}{\sqrt{4R_g\left(g_{ds} + 2\pi f_T C_{gd}\right)}} \tag{5.37}$$

In **Figure 5.11(b)** f_{MAX} is displayed with extracted modeled value and compared with the simulated value for CRC and TGRC devices. Results show that

f_{MAX} improves 123% in simulated data and 130% in modeled data (nearly same) in TGRC-MOSFET as compared to CRC-MOSFET as reflected in **Figure 5.11(b)** due to the enhancement of carrier mobility which results in a reduction in gate resistance. From equation (5.37), we see that, since f_{MAX} is directly proportioned to the f_T, for the same reasons as explained for f_T, so higher f_T reflects higher f_{MAX} (Kumar, 2017) in TGRC device than the previous published work (Adhikari & Singh, 2015a; Adhikari & Singh, 2017).

5.5 SUMMARY

This chapter discusses the small signal modeling of TGRC-MOSFET in terms of microwave and electrical parameters, i.e., impedance, admittance, and hybrid parameters. It is found that TGRC-MOSFET shows high input impedance and low output impedance owing to the ITO as a gate material which improves the current driving capability and thus the device HF performance in comparison to conventional RC MOSFET. Further, the transfer impedance also improves in TGRC device as compared to the conventional device due to reduced SCEs and high ON current which enhances the ultimate gain of the device and thus can be useful in wireless/millimeter wave applications. Moreover, the calculated model results of small signal parameters are in good agreement with the simulation results so obtained at the THz range and thereby validating the small signal model. Results show that the proposed device is best suited for superior RF/Microwave applications.

After discussing the high switching and superior RF/Microwave applications, the capability of TGRC MOSFET is explained for sensing applications such as radiation sensor (as a dosimeter) and biosensor in the next chapter with high sensitivity in sub-20 nm regime for use in medical diagnosis.

5.6 REFERENCES

Adhikari, M. & Singh, Y. (2015a) High-performance dual-channel InGaAs MOSFET for small signal RF applications. *Electronics Letters*, 51(15), 1203-1205.

Adhikari, M. S. & Singh, Y. (2015b) A nanoscale dual-channel trench (DCT) MOSFET for analog/RF applications. *Superlattices and Microstructures*, 88, 567-573.

Adhikari, M. S. & Singh, Y. (2017) High performance multi-channel MOSFET on InGaAs for RF amplifiers. *Superlattices and Microstructures*, 102, 79-87.

Adhikari, M. S. & Singh, Y. (2018) Implementation of Trench-based Power LDMOS and Low Voltage MOSFET on InGaAs. *IETE Technical Review*, 1-9.

Ajayan, J., Nirmal, D., Prajoon, P. & Pravin, J. C. (2017) Analysis of nanometer-scale InGaAs/InAs/InGaAs composite channel MOSFETs using high-K dielectrics for high speed applications. *AEU-International Journal of Electronics and Communications*, 79, 151-157.

Alexander, C. K. & Sadiku, M. N. (2013) *Fundamentos de circuitos eléctricos*McGraw Hill Mexico.

Chalkiadaki, M.-A. & Enz, C. C. (2015) RF small-signal and noise modeling including parameter extraction of nanoscale MOSFET from weak to strong inversion. *IEEE Transactions on Microwave Theory and Techniques*, 63(7), 2173-2184.

Chen, Q. B. (2013) Compact modeling of multi-gate MOSFETs for RF designs, *2013 IEEE International Wireless Symposium (IWS)*.

Frickey, D. A. (1994) Conversions between S, Z, Y, H, ABCD, and T parameters which are valid for complex source and load impedances. *IEEE Transactions on microwave theory and techniques*, 42(2), 205-211.

Gupta, N. & Chaujar, R. (2016) Investigation of temperature variations on analog/RF and linearity performance of stacked gate GEWE-SiNW MOSFET for improved device reliability. *Microelectronics Reliability*, 64, 235-241.

Gupta, N., Kumar, A. & Chaujar, R. (2015a) Impact of device parameter variation on RF performance of gate electrode workfunction engineered (GEWE)-silicon

nanowire (SiNW) MOSFET. *Journal of Computational Electronics*, 14(3), 798-810.

Gupta, N., Kumar, A. & Chaujar, R. (2015b) Oxide bound impact on hot-carrier degradation for gate electrode workfunction engineered (GEWE) silicon nanowire MOSFET. *Microsystem Technologies*.

Hurkx, G., Agarwal, P., Dekker, R., van der Heijden, E. & Veenstra, H. (2004) RF figures-of-merit for process optimization. *IEEE Transactions on Electron Devices*, 51(12), 2121-2128.

Kilchytska, V., Nève, A., Vancaillie, L., Levacq, D., Adriaensen, S., Van Meer, H., De Meyer, K., Raynaud, C., Dehan, M. & Raskin, J.-P. (2003) Influence of device engineering on the analog and RF performances of SOI MOSFETs. *Electron Devices, IEEE Transactions on*, 50(3), 577-588.

Kumar, A. (2017) Effect of Trench Depth and Gate Length Shrinking Assessment on the Analog and Linearity Performance of TGRC-MOSFET. *Superlattices and Microstructures*.

Kumar, A., Gupta, N. & Chaujar, R. (2016a) Analysis of novel transparent gate recessed channel (TGRC) MOSFET for improved analog behaviour. *Microsystem Technologies*, 22(11), 2665-2671.

Kumar, A., Gupta, N. & Chaujar, R. (2016b) Effect of structured parameters on the hot-carrier immunity of transparent gate recessed channel (TGRC) MOSFET. *Microsystem Technologies*, 1-8.

Kumar, A., Gupta, N. & Chaujar, R. (2016c) Power gain assessment of ITO based Transparent Gate Recessed Channel (TGRC) MOSFET for RF/wireless applications. *Superlattices and Microstructures*, 91, 290-301.

Kumar, A., Gupta, N. & Chaujar, R. (2016d) TCAD RF performance investigation of Transparent Gate Recessed Channel MOSFET. *Microelectronics Journal*, 49, 36-42.

Kumar, A., Gupta, N., Tripathi, M. & Chaujar, R. (2019) RF noise modeling of Black Phosphorus Junctionless Trench MOSFET in strong inversion region. *Superlattices and Microstructures*, 125, 72-79.

Kumar, A., Tripathi, M. & Chaujar, R. Investigation of parasitic capacitances of In2O5Sn gate electrode recessed channel MOSFET for ULSI switching applications. *Microsystem Technologies*, 1-8.

Kumar, A., Tripathi, M. & Chaujar, R. (2017) Small-signal modeling of In2O5Sn based transparent gate recessed channel MOSFET for microwave/RF applications, *Microwave Conference (APMC), 2017 IEEE Asia Pacific*. IEEE.

Kumar, A., Tripathi, M. & Chaujar, R. (2018a) Reliability Issues of In2O5Sn Gate Electrode Recessed Channel MOSFET: Impact of Interface Trap Charges and Temperature. *IEEE Transactions on Electron Devices*, 65, 860-866.

Kumar, A., Tripathi, M. M. & Chaujar, R. (2018b) In2O5Sn based transparent gate recessed channel MOSFET: RF small-signal model for microwave applications. *AEU - International Journal of Electronics and Communications*, 93, 233-241.

Larson, L. E. (2003) Silicon technology tradeoffs for radio-frequency/mixed-signal" systems-on-a-chip". *Electron Devices, IEEE Transactions on*, 50(3), 683-699.

Pozar, D. M. (2009) *Microwave engineering*John Wiley & Sons.

Saito, M., Ono, M., Fujimoto, R., Tanimoto, H., Ito, N., Yoshitomi, T., Ohguro, T., Momose, H. S. & Iwai, H. (1998) 0.15-μm RF CMOS technology compatible with logic CMOS for low-voltage operation. *Electron Devices, IEEE Transactions on*, 45(3), 737-742.

Sarkar, A. & Jana, R. (2014) The influence of gate underlap on analog and RF performance of III–V heterostructure double gate MOSFET. *Superlattices and Microstructures*, 73, 256-267.

SILVACO, I. (2011) ATLAS User's Manual. *Santa Clara, CA, Ver*, 5.

Sinnesbichler, F. X. & Olbrich, G. R. (2003) Thermal time constant extraction for HBTs from S-parameter measurements. *AEU-International Journal of Electronics and Communications*, 57(3), 181-184.

Taher, H., Schreurs, D. & Nauwelaers, B. (2006) Extraction of small-signal equivalent circuit model parameters for Si/SiGe HBT using S-parameters measurements and one geometrical information. *AEU-International Journal of Electronics and Communications*, 60(8), 567-572.

Tsividis, Y. & McAndrew, C. (2011) *Operation and Modeling of the MOS Transistor*Oxford Univ. Press.

Wei, B. & Lu, C. (2018) Transition metal dichalcogenide MoS2 field-effect transistors for analog circuits: A simulation study. *AEU-International Journal of Electronics and Communications*, 88, 110-119.

Yang, J.-Y., Benaissa, K., Crenshaw, D., Williams, B., Sridhar, S., Ai, J., Boselli, G., Zhao, S., Tang, S.-P. & Mahalingam, N. (2002) 0.1 μm RFCMOS on high resistivity substrates for system on chip (SOC) applications, *IEDm: international electron devices meeting*.

6

CHAPTER

In_2O_5Sn Gate Electrode Recessed Channel MOSFET for an X-Ray Dosimeter and Biosensing Application

- *This chapter reports the applications of In_2O_5Sn Gate Electrode Recessed Channel (TGRC) MOSFET as a dosimeter and biosensor.*
- *In the first part, the response of N-channel TGRC MOSFET to X-ray radiation in the 0.5k to 10kRad dose range after irradiation has been analysed.*
- *TCAD simulations for the same have been done to estimate threshold voltage shift in MOSFET with different radiation dosage.*
- *An improvement of 1.11mVolts/kRad in radiation sensitivity has been found on increasing the oxide thickness from 2nm to 6nm.*
- *In the second part of this chapter, TGRC MOSFET as a biosensor has been proposed and electrical detection of neutral biomolecules has studied in terms of I_{on}/I_{off}, shift in threshold voltage, change in surface potential and hereafter, calculates the sensitivity of the biosensor.*
- *In addition, the noise immunity of TGRC device has been observed when the biomolecules are immobilized.*
- *Furthermore, the modulation of cavity gap length (from 8nm to 20nm), has also been observed.*
- *Thus, TGRC device can be used for biosensor applications to diagnose various associated diseases which require lower noise, high speed, low power, and high density.*

6.1 INTRODUCTION

As discussed in **Chapter 1**, semiconductor devices such as Field Effect Transistor (FET) and Metal Oxide Semiconductor Field Effect Transistor (MOSFET) are the most appropriate devices for sensing applications. MOSFETs are excessively used in radiation rich environments, such as space and military. When electronic circuits are exposed to various radiation environments, it becomes critical to define the behavior of the circuit undergoing irradiation. Various effects such as SEB (Single Event Burnout), SEGR (Single Event Gate Rupture), insulator charging and interface charging degrades the circuit performance and sometimes completely damage the device (Allenspach et al, 1996). To ensure safety and stability of such circuits in a harsh radiation environment, the incoming dose must be monitored to initiate specific repairs or replacement. In medical applications (Villani et al, 2013), an X-ray dose which is intended to kill cancerous cells will probably cause damage to normal tissues and hence, to minimize this damage, extremely precise dose adjustments are required which is facilitated if the sensor can be placed close to the site receiving radiation. MOSFET dosimeters are used to determine total dose absorbed due to their valuable property of linear dependence of threshold voltage on total ionizing dose over a finite range of doses.

TGRC MOSFET has the ability to provide high packing density and hence, miniaturized sensors which are of utmost importance as exposure to ionizing radiation has to be tightly controlled in radiotherapy, nuclear waste management, high-energy physics experiments, and space missions to avoid health or technical safety risks (Seco et al, 2014). Moreover, the increased functionality and reduced cost of large variety of integrated circuits and systems has brought its own benefit to the end users and above all the semiconductor industry.

Scaling of MOSFET leads to hot carrier injection (HCI) which causes excess of charge carriers flowing through gate oxide and thus degrades its performance and therefore to overcome this effect, recessed channel structure is used with 6nm oxide thickness. Also, recessed structure leads to low power dissipation which is of utmost importance for a dosimeter to show improved sensitivity at nano-level. TGRC MOSFET (Kumar, 2017; Kumar et al, 2016a; c; d; 2017a; Kumar et al, 2017b; 2018d)

is therefore preferred as it has ITO (Minami, 2005a) as gate electrode allowing easier energy transfer through the gate electrode thereby maximizing the absorbed dose leading to enhanced sensitivity and hence proving to be an ideal choice for dosimeter (Morgan et al, 1995; Schwank et al, 2008). As a result of the interaction of ionizing x-ray radiation with TGRC MOSFET, holes are trapped inside the oxide-substrate interface layer, which causes a shift in the threshold voltage (Benedetto & Boesch, 1986) of the device. To predict the electrical behavior of MOSFET device under the influence of ionizing radiation, it is necessary to determine the trapped hole density inside the oxide and energy imparted by the radiation to the material.

When high energy photons strike the semiconductor lattice, they provide sufficient energy to generate electron-hole pair directly or indirectly via the lattice vibrations. Generating electron-hole pair in SiO_2 layer requires energy, $E_p = 17 \pm 1$ eV (Ausman Jr & McLean, 1975). Using this value of E_p, we are able to calculate $g_0 = 8.1 \times 10^{12}$ pairs/cm^3-Rad (Oldham & McLean, 2003) which is the theoretical number of electron-hole pairs generated, but this value is greatly reduced due to recombination process. In semiconductor region, as the mobility of electrons and holes doesn't differ significantly, they can recombine very easily. However, in the case of gate oxide, being an insulator, the difference in mobility is significantly large. As a result, electrons move very quickly towards the gate electrode, and holes drift slowly towards the Si-SiO_2 interface and finally getting trapped there. The trapped holes at the Si-SiO_2 interface are relatively immobile causing a negative shift in threshold voltage on the electrical characteristics of MOSFET. Ultimately, the shift in threshold voltage can be used as a dosimetric parameter to evaluate incident radiation dosage.

The second part of this chapter discusses the applicability of TGRC MOSFET for biosensing. With the aid of nanotechnology, various kind of biosensors has been developed for medical applications and disease diagnostics, to address its high performance. According to medical science, prompt detection of any disease mainly cancer is valuable for the survival of patients. Numerous methods have been developed for detection of the biomolecule, such as the enzyme-linked immunosorbent assay (Comini et al), Alzheimer's disease, ovarian cancer, and

coronary artery disease. Though, many of them are complicated and time-consuming due to labeling practices (Lee et al, 2015), FET-based biosensors have gained a lot of attention from past few years owing to high scalability, high sensitivity, rapid electrical detection, low power consumption, direct electrical readouts, low-cost mass production as compared with other devices, including surface Plasmon resonance (Bergveld, 1986), microcantilevers (Sang et al, 2016), and an array of fluorescence sensors (Im et al, 2007). Low-cost, highly sensitive, reliable, user-friendly quick diagnostic bio-sensing devices are essential for different biological and biomedical applications (Vu et al, 2009). For biosensing applications, sensitivity is the key factor for a MOSFET. Time to time different structures such as nanowire Junctionless MOSFET (Ahangari, 2016) and Tunnel FET (Chandan et al, 2018; Kanungo et al, 2016) have been introduced to enhance the sensitivity of FET based biosensor. Nanotechnology-based biosensor devices are used (Ahn et al, 2010; Azmi et al, 2014; Gao et al, 2011) to overcome the difficulties of conventional health diagnostic methods.

Moreover, the development of semiconductor technology for medical applications advanced to shrink the device dimensions for the nanoscale regime in order to provide high packing density with the high-speed integrated circuit. However, in an ultra-scaled device, the influence of short channel effects (SCEs) deeply affect the device performance (Ahangari, 2016). To overcome SCEs, several device engineering schemes and modulation in device structures have been reported in the literature (Barsan, 1981; Chaujar et al, 2008b; Gupta & Chaujar, 2016a; Gupta & Chaujar, 2016b; Gupta & Chaujar, 2016c; Gupta et al, 2015). Recessed Channel (RC) MOSFET, is considered as the most promising one since it overcomes almost all the SCEs and is also feasible with recent CMOS technology (Chaujar et al, 2008a). Nowadays, numerous innovative gate materials have been explored to intensify the current driving capability of CMOS and also to enhance the overall device performance. In this proposed device (TGRC-MOSFET) as a biosensor, ITO has been used as a gate material due to its enhanced electrical properties which have been demonstrated in previous work (Kumar et al, 2016a; b; c; d; Kumar et al, 2018c; d).

ITO enhances significantly the on-current owing to its very low resistivity (10^{-5} Ω-cm) with high mobility (53.5 cm^2 $V^{-1}s^{-1}$) (Minami, 2005b).

Therefore, for the first time, the simulation study of TGRC-MOSFET as a biosensor has been introduced by taking into consideration the electrical properties of biomolecules. A biosensor is basically used to sense biological elements, attaching the sensitivity and binding specificity of biologics such as enzymes, proteins, nucleotides, and antibodies. In this proposed TGRC-MOSFET as a biosensor, the channel potential of the device is influenced by the electrical properties of biomolecules and thus can further be useful for the detection of biomolecules. In conventional MOSFET, the current flows in the channel when gate voltage exceeds the threshold voltage (V_{TH}), and in biosensor, it can be modulated by the dielectric constant which is due to biomolecule immobilization below the gate electrode because threshold voltage depends upon gate capacitance. The electrical characteristics are altered due to absorption of biomolecules and due to which the sensitivity of sensor changes.

6.2 IN_2O_5SN GATE ELECTRODE RECESSED CHANNEL MOSFET: AN X-RAY DOSIMETER

6.2.1 Device Design and its Description

For irradiated TGRC MOSFET device, threshold voltage, hole trap density, maximum on-current are usually the most relevant parameters. The radiation-induced changes are reported in this paper based on these parameters. Our device consists of the transparent gate made of indium tin oxide (ITO) as shown in **Figure 6.1** and the design parameters are given in **Table 6.1** (Kumar et al, 2018a). ITO is a wide band gap material that exhibits the special property of high optical transmittance (~90%) in the visible region of the spectrum combined with a high electrical conductivity (Morgan et al, 1995). As the radiation sensitivity is found to be dependent on the absorbed dose, ITO having high optical transmittance is expected to enhance the overall trapping of the incident radiation dose.

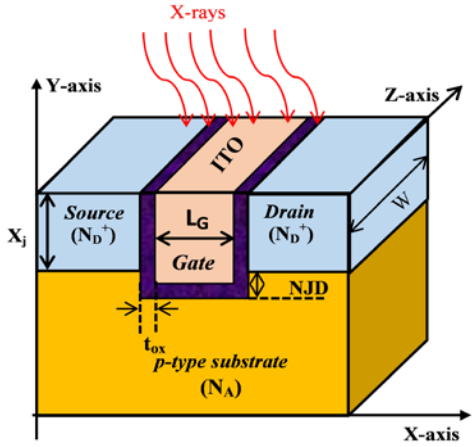


Figure 6.1: Simulated device structure of TGRC-MOSFET (Kumar et al, 2018a).

Table 6.1: Design Parameters of TGRC MOSFET (Kumar et al, 2018a).

Parameter	Unit		
Oxide Thickness (t_{ox})	2 nm	4 nm	6nm
Source/Drain doping (N_D^+)	1×10^{19} cm^{-3}		
Substrate doping (N_A)	1×10^{16} cm^{-3}		
Gate Length (L_G)	30 nm		
Negative junction depth (NJD)	10 nm	12 nm	14 nm
Work function for TGRC-MOSFET	4.7 eV		
Permittivity of SiO_2 (ε_{ox})	3.9		
Gate to Source voltage (V_{gs})	1.5 V		
Drain to Source voltage (V_{ds})	0.05 V		

This work is based on direct incident radiation for very short duration in the simulation process. The values are found immediately after irradiation and continuing irradiation for a long time period has been avoided for the device protection. Strict constraints are applied on the device dimensions as the intended application – implantable clinical dosimeter will require additional space for peripheral electronic components.

Moreover, the power consumption is one of the major issues for a semiconductor device. It is found that DC power starts increasing with increase in gate voltage and its value is smaller in TGRC MOSFET in comparison to conventional MOSFET as shown from **Figure 6.2**. This improvement is due to lower off current and improved current driving capability. In addition, TGRC MOSFET is a

less AC power consumption device as compared to conventional MOSFET as shown in **Figure 6.2**.

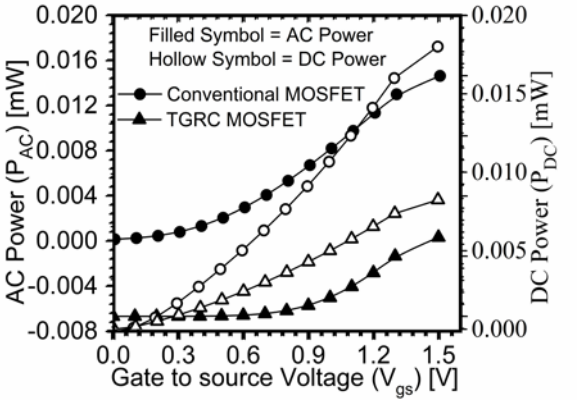


Figure 6.2: AC power (P_{AC}) and DC power (P_{DC}) w.r.t. V_{gs}; for TGRC MOSFET and conventional MOSFET (Kumar et al, 2018a).

6.2.2 Simulation Methodology and Calibration

For TCAD simulations, various models have been taken into effect such as, for mobility of carriers under the influence of changing electric field, we have included Parallel Electric Field Dependence model which takes care of all the parameters affecting the mobility of carriers including velocity saturation effect (SILVACO, 2011). To predict the behavior of the device undergoing radiation, it is extremely crucial to accurately model the movement of carriers so that simulated charge trapping is almost identical to practical device undergoing irradiation. For carrier generation-recombination, we have implemented concentration-dependent Klaassen Shockley-Read-Hall (klasrh) Recombination model as it can include concentration-dependent lifetime of carriers (SILVACO, 2011).

As electron-hole pair generation-recombination is a key phenomenon in predicting the behavior of MOSFET after irradiation, it can be most accurately modeled via klasrh model. To model the trap states of the carrier in oxide and interface region, we have included bound trap model as it allows us to specify energy level requirement of trapped states. The above-selected models account for almost the entire device physics associated with the MOSFET, thereby producing extremely accurate results.

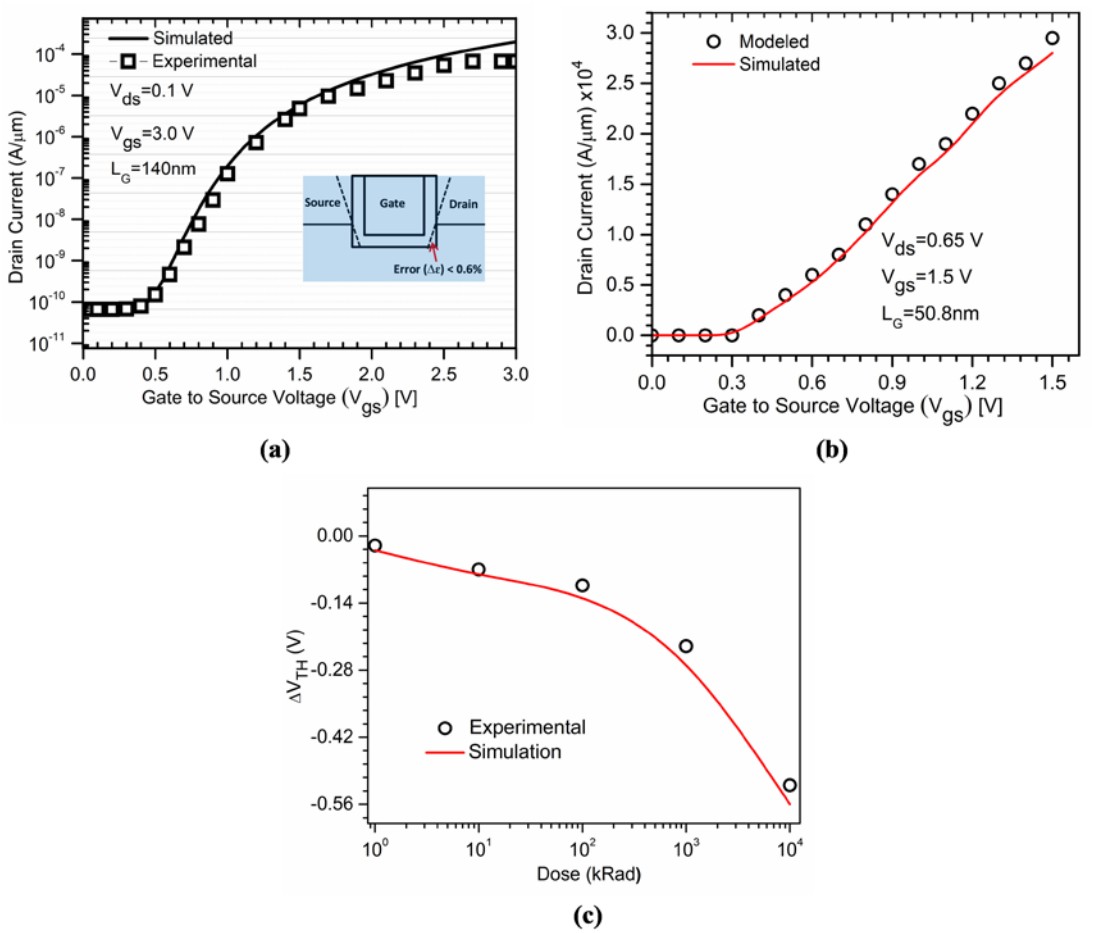


Figure 6.3: (a) Experimental (Xiao-Hua et al, 2006) and simulation of I_{ds}-V_{gs} characteristics of 140 nm gate length grooved gate (recessed channel) MOSFET. (b) Modelled (Sreelal et al, 2002) and simulation of I_{ds}-V_{gs} characteristics of 50.8 nm gate length recessed channel MOSFET. (c) Calibration of experimental (Berland et al, 1991) and simulation results with shift in threshold voltage (ΔV_{TH}) under irradiation up to 10^4 kRad (Kumar et al, 2018b).

To validate the simulation models, both the experimental (Xiao-Hua et al, 2006) and modeled data (Sreelal et al, 2002) have been extracted and calibrated as shown in **Figure 6.3(a)** and **6.3(b)** respectively. The fabricated data (Xiao-Hua et al, 2006) is extracted from a grooved gate trapezoidal like structure of 140 nm gate length which is similar to U-groove gate. The corner effect (error) (Chaujar et al, 2008a) ($\Delta\varepsilon/L_{eff}$) is less than 0.6%, which is almost negligible as depicted in **Figure 6.3(a)**. Further to validate the results the simulated models have also been calibrated with modelled data (Sreelal et al, 2002) for 50.8 nm gate length (channel length (L_G+2(NJD+t_{ox}))=85.8 nm) which is also in good agreement as evident from **Figure 6.3(b)**, thus reflecting the validity of simulation models.

Further, to show simulation validity of radiation dose, we have compared our simulation results [shown in **Figure 6.3(c)**] with those of experimentally obtained parameters by V. Berland, and A. Touboul (Berland et al, 1991). To compare the results, we have scaled our device dimensions similar to that of experimental device, by changing gate length to 20 µm and gate oxide thickness to 23 nm. Additionally buried oxide of thickness 380 nm is introduced to match with the experimental device. Simulations for radiation dose up to 10^4 kRad are done and change in threshold voltage is compared with our device as shown in **Figure 6.3(c)**, which predicts almost similar results with a small margin of error. Thus, it validates the accuracy of simulation models after irradiation.

6.2.3 Results and Discussion

A. Impact of X-Ray Doses

TCAD Simulation of TGRC MOSFET undergoing irradiation shows that a significant number of holes are trapped in the SiO_2 gate oxide layer and the area of gate oxide as $68nm^2$ (2nm × (2+30+2 nm)) is considered. As depicted in **Figure 6.4**, the trapped hole density is maximum (6×10^8 cm^{-2}) near the oxide-substrate interface.

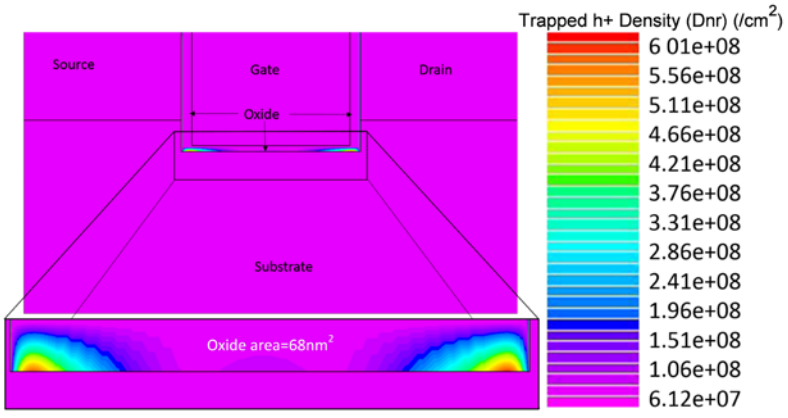


Figure 6.4: Trapped hole density profile along the oxide substrate interface, having oxide thickness 2nm, and oxide area 68 nm^2 (Kumar et al, 2018a).

In our simulation, the maximum hole trap density is found out to be 6×10^8 (Dnr/cm^2) for a total ionizing dose of 10k rads. This accumulation of charge due to trapping of holes accounts for the maximum change in the electrical characteristics of

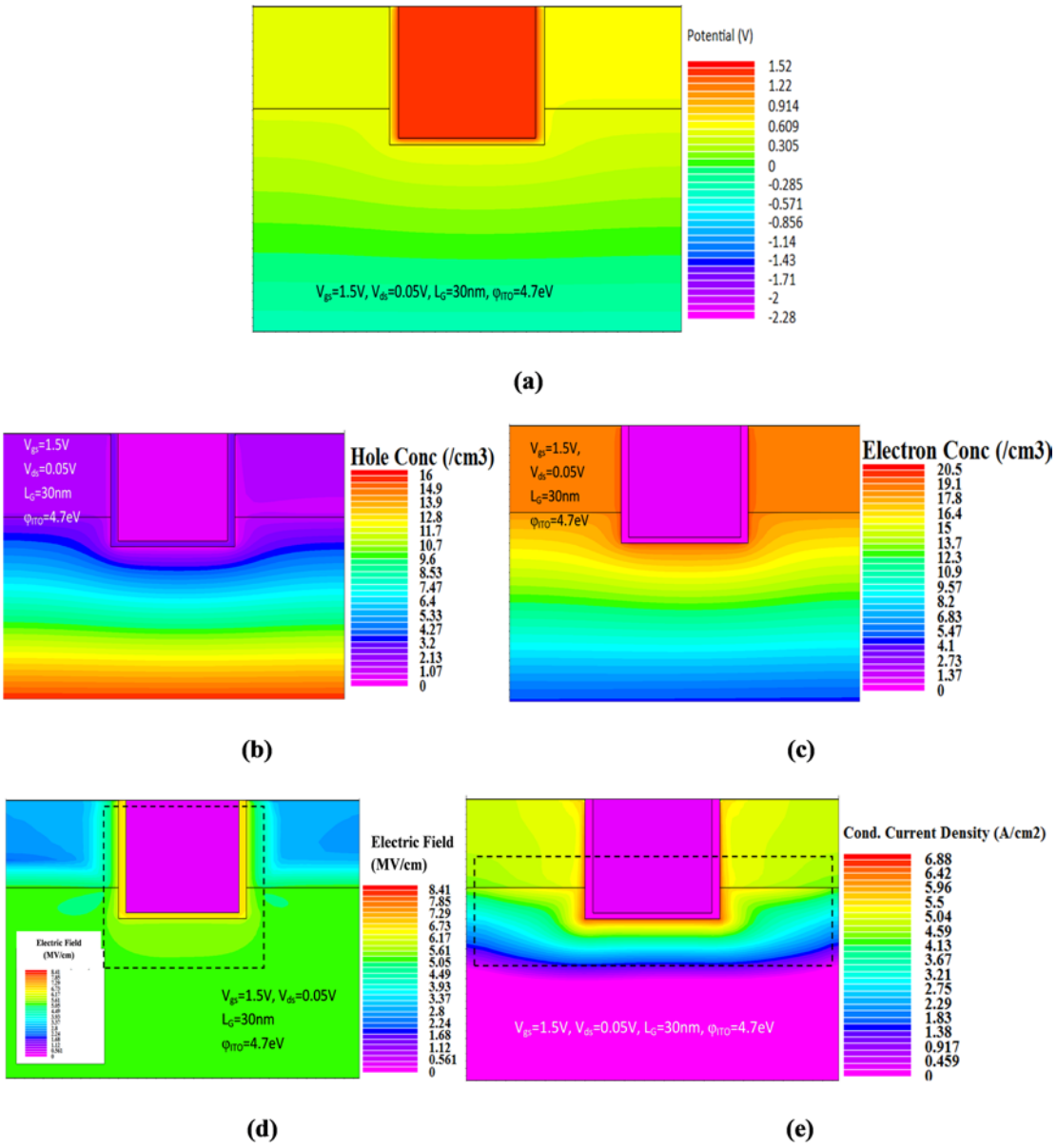


Figure 6.5: Contour plots of (a) Surface potential; (b) Hole concentration; (c) Electron concentration; (d) Electric field and (e) Conduction current density on TGRC-MOSFET (t_{ox}=2nm) with 1000 RadX-ray dose (Kumar et al, 2018a).

-the device. The overall sensitivity of the dosimeter is dependent on trapped hole concentration in the oxide layer, and to maximize this, we needed strong electric field inside the oxide layer which can significantly reduce the electron-hole recombination thereby increasing the trapped hole concentration. This has been achieved with multiple simulations and with hit and trial approach, we were able to generate electric fields as high as 7 MV/cm in the oxide region as shown in **Figure 6.5(d)** and corresponding biasing which allowed such high field is depicted in **Figure 6.5(a)**. To

illustrate the conduction channel which is formed, we've included detailed contours showing the charge carrier concentration in the device as shown in **Figure 6.5(b)** and **6.5(c)**.

In TGRC MOSFET, due to the accumulation of trapped holes near the oxide-substrate interface, there is a negative shift in the threshold voltage of the device as shown in **Figure 6.6**. V_{TH} is obtained using the single derivative method by analyzing the drain to source current (I_{ds}) vs. gate to source voltage (V_{gs}) curve. The evaluated values of threshold voltage show a linear dependence on applied radiation dose and the threshold voltage shift being negative (shown in **Figure 6.6**). The threshold voltage shift ($|V_{TH\text{-}SHIFT}|$) has been evaluated (as $|(V_T\text{-}V_{T0})|$, where V_T is the threshold voltage after irradiation (0.5k-10k Rad) and V_{T0} is the threshold voltage without irradiation and is plotted as shown in **Figure 6.7**. The radiation dose has been considered from 0.5kRad as in radiotherapy, daily doses could range from 50Rad up to 2500Rad. In some specific medical treatments such as lung cancer, specific doses are required for specific patient and it is also more important to analyse which x-ray doses are delivered to the organs (Nakamura et al, 2018).

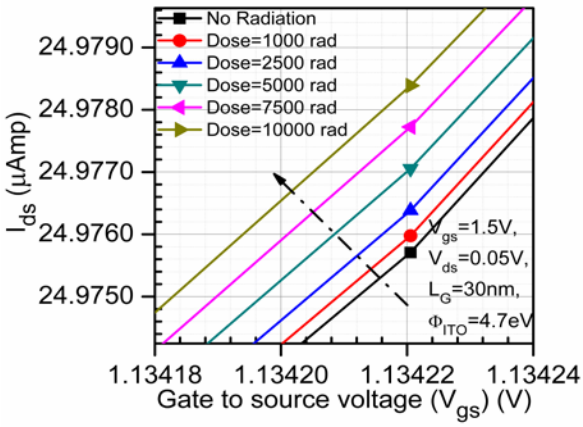
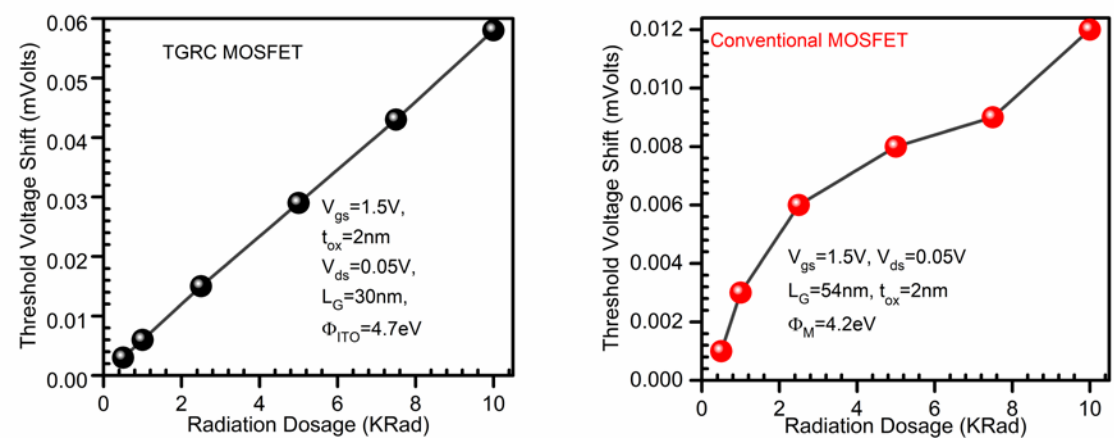


Figure 6.6: The impact of X-ray radiation damage on the current-voltage characteristics of TGRC MOSFET at t_{ox}=2nm (Kumar et al, 2018a).

The proposed device having low operating voltages along with small drain to source current (**Figure 6.8(a)**) has extremely low power consumption (see **Figure 6.2**) which enhances the overall usage time with limited power supply, hence increasing its applicability as an implantable dosimeter. In the conventional

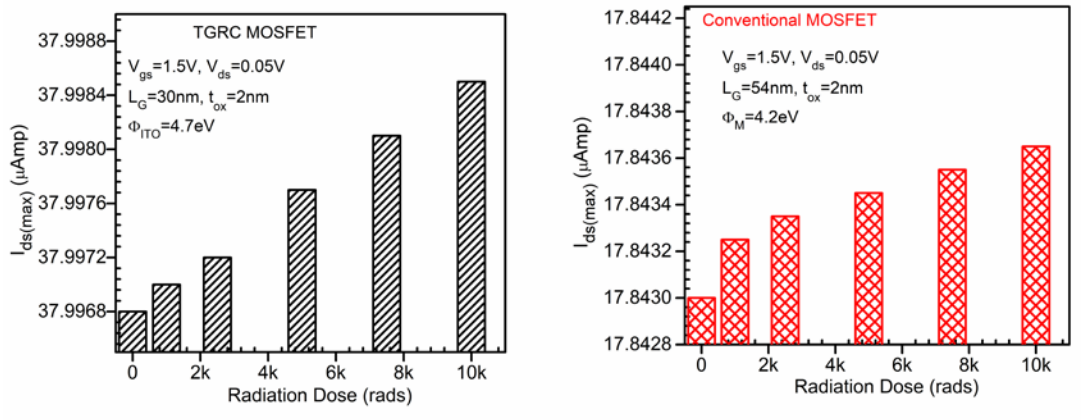
MOSFET, hot carrier injection leads to impact ionization which causes excess of electrons to flow through gate oxide and thus leads to degradation in sensitivity and maximum drain current as shown in **Figure 6.12** and **Figure 6.8(b)** respectively.



(a) **(b)**

Figure 6.7: Threshold Voltage Shift due to radiation on (a): TGRC MOSFET and, (b): Conventional MOSFET (Kumar et al, 2018a).

Trapped hole density is plotted for varying radiation doses along the oxide layer which confirms the theoretical prediction that maximum hole trapping is related linearly to the incident radiating dose (0.5k-10k Rad) as depicted in **Figure 6.9**. Due to increasing radiation dosage, more electron-hole pairs are generated which consequently enhances the number of trapped holes in the oxide-substrate interface region.



(a) **(b)**

Figure 6.8: The impact of radiation dose on the maximum drain to source current for (a): TGRC MOSFET and, (b): Conventional MOSFET (Kumar et al, 2018a).

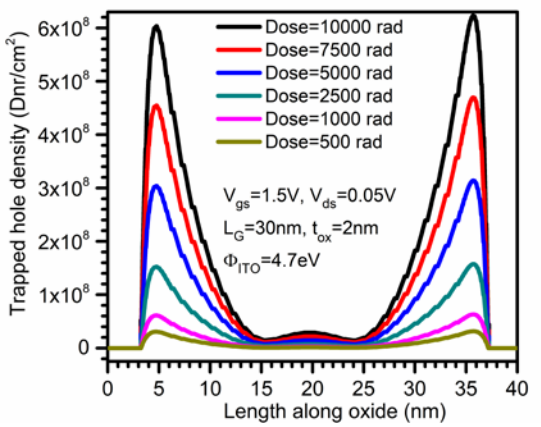


Figure 6.9: Trapped hole density profile along the oxide substrate interface (Kumar et al, 2018a).

By increasing the radiation dosage (0.5k-10k Rad), we are increasing the trapped hole density in the Si/SiO_2 interface region as shown in **Figure 6.9** and **Figure 6.10**, thereby making it abundant in positive charge. Due to the accumulation of charge, the overall channel being formed is enriched with more attracted electrons. Due to increase in the attracted electrons at the surface, V_{TH} decreases ($|V_{TH\text{-}SHIFT}|$ increases) as shown in **Figure 6.7**. Ultimately, there is a significant change in threshold voltage in TGRC MOSFET as compared to conventional MOSFET upon

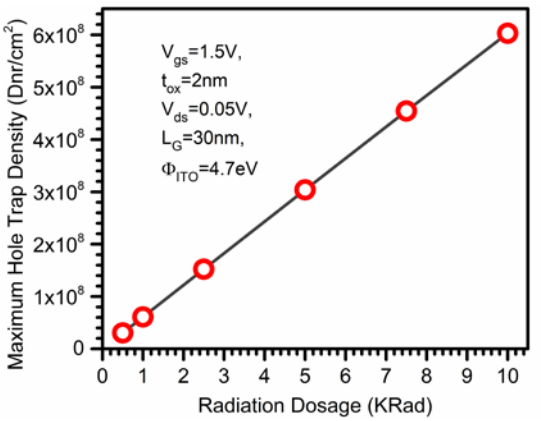


Figure 6.10: The impact of varying radiation dosage on maximum hole trap density (Kumar et al, 2018a).

-application of radiation, and this change is uniform up to 10kRad dose as reflected in **Figure 6.7(a)** and **6.7(b)** respectively. Hence, it can be used as a sensor for detecting X-ray radiation dose up to 10kRads. This particular range of measurement comes close to the amount of radiation being used in X-ray radiation therapy which is approximately few Rad of dose. Thus, the proposed device (TGRC MOSFET) can be

effectively used as a dosimeter in a situation where device dimensions are limited to few nanometers having sensitivity up to 1.11 mV/kRad (at 6 nm oxide thichness).

B. Effects of Varying the Oxide Thickness on Radiation Sensitivity

The electrical behavior of TGRC MOSFET during the process of irradiation is greatly influenced by the thickness of the gate oxide layer. As we increase or decrease the thickness of oxide layer, consequently the channel length ($L_{CH}(=L_G+2(NJD+t_{ox})$) is also modified. Further, to validate TGRC MOSFET as a dosimeter, sensitivity of the device is compared with the conventional MOSFET (as shown in **Figure 6.11**) and it is found that, the conventional MOSFET (where gate length and the channel length is same ($L_G = L_{CH} = 54$ nm)) is less sensitive (0.652 mV/kRad) as compared to TGRC MOSFET (1.11 mV/kRad) owing to reduced current driving capability due to short channel effects which dominates at sub-30 nm gate length. These results show that TGRC MOSFET provides improved performance than conventional MOSFET.

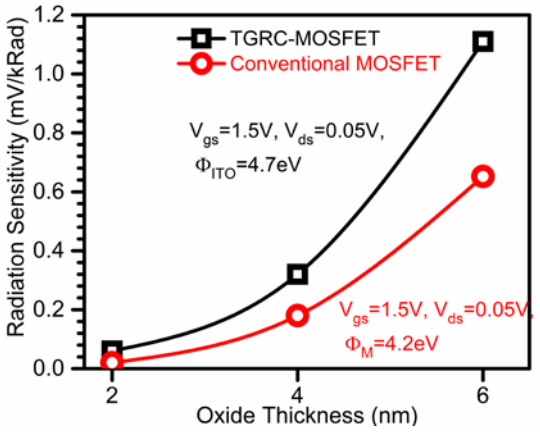


Figure 6.11: Dependency of Radiation Sensitivity on Oxide Thickness in TGRC MOSFET and, Conventional MOSFET (Kumar et al, 2018a).

The effect of increasing the oxide thickness in our device has also been simulated, and observed this increase in oxide thickness, leading to increased threshold voltage V_{TH} and decreased ON-current of the device as shown in **Figure 6.12** and **Figure 6.13**. As we gradually increase the oxide thickness from 2nm to 6nm, the overall volume of SiO_2 receiving total ionization dose is greatly enhanced leading to greater number of electron-hole pair generation-recombination and ultimately increased trapped hole states in the oxide-substrate interface.

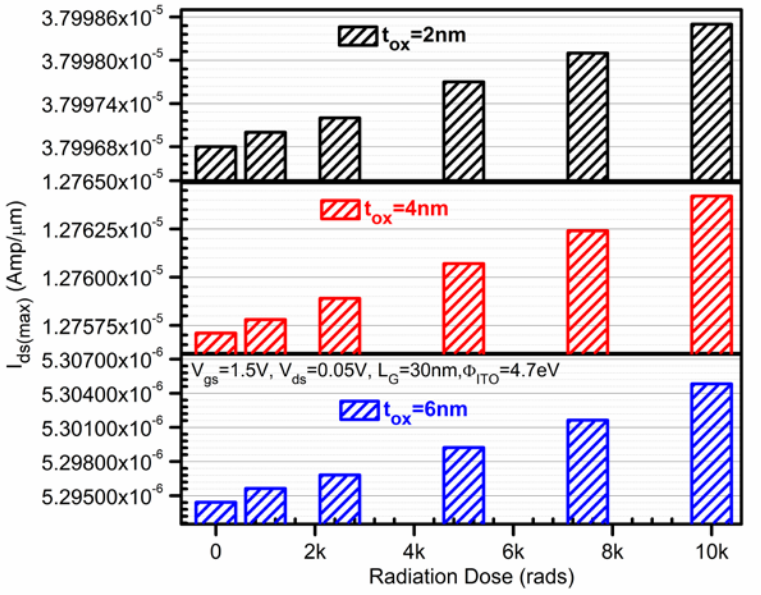


Figure 6.12: Variation of ON current with radiation dosage for different oxide thickness (Kumar et al, 2018a).

To evaluate the radiation sensitivity of the device, we used the slope of the graph from **Figure 6.6**. With the decrease in thickness of gate oxide, radiation hardness improves (Benedetto & Boesch, 1986; Schwank et al, 2008). Thus, the shift in threshold voltage is more substantial in thicker oxide as depicted in **Figure 6.13**, which in turn points out that if we want to design highly sensitive dosimeter, thicker oxide is essential, but under dimensional constraints or space critical application, as in case of clinical dosimeter this reduced sensitivity can be mitigated by external amplifier circuits.

Saks et al. (Saks et al, 1984) predicted that for oxide layer, the threshold voltage changes with radiation dose as the square of the oxide thickness (Radiation Sensitivity α (Oxide Thickness)^2), suggesting the uniform distribution of generated electron-hole pair and trapped states throughout the oxide-substrate interface. For comparatively thinner oxides (less than 20nm), threshold voltage shifts show slightly less $(t_{ox})^2$ thickness dependence which can be easily inferred from the results shown in **Figure 6.11** (sensitivity up to 1.11 mV/kRad at 6 nm oxide thichness) and **Figure 6.13**. As the proposed device is optimized to generate threshold voltage shift which depends linearly on applied radiation dose, the simulations confirm that TGRC

MOSFET will generate almost linear results within 2 to 6 nm oxide thickness range. Thus, 6nm oxide thickness is the optimal oxide thickness for the TGRC as dosimeter.

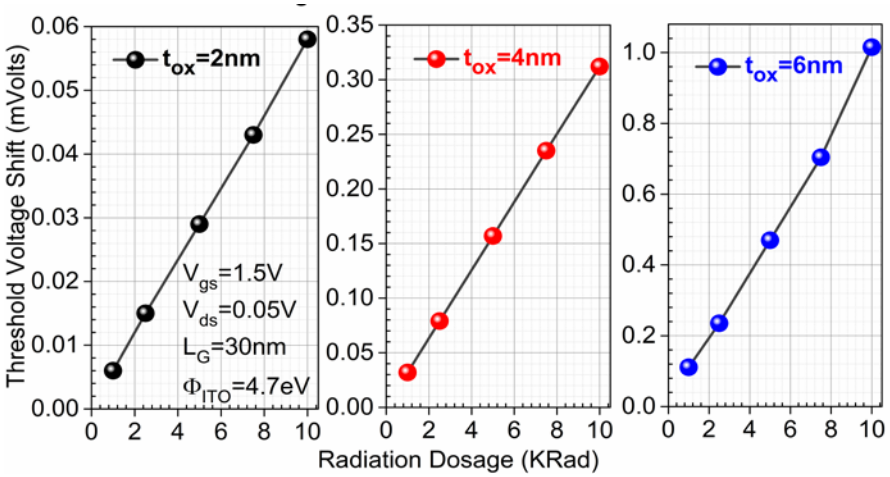


Figure 6.13: Threshold voltage shift with variation in radiation dosage for various oxide thicknesses (Kumar et al, 2018a).

6.3 Ultra-Low Power Dielectric Modulated Nano-gap Embedded In_2O_5Sn Gate Electrode Recessed Channel MOSFET for Biosensing Application

6.3.1 Device Structure

The 3D device structure of biosensor considered in this work is shown in **Figure 6.14**. For immobilization of biomolecules, a small nano-cavity is created in the gate insulator region, since it is the most important region in determining the behavior and characteristics of CMOS. Here, L_{gap} is the length of Nano-gap cavity (8 nm), t_{ox} is the oxide thickness (2 nm), and L_G, the gate length is taken 20 nm. The source and drain regions are highly doped with an n-type impurity of 5×10^{19} cm^{-3}, and the substrate is doped with a p-type impurity of 1×10^{17} cm^{-3} as shown in **Figure 6.14**. Negative Junction Depth (NJD) is taken as 10 nm, Gate workfunction of ITO (Φ_{ITO}) is 4.7eV.

Gate bias (V_{gs}) is 0.7 V and Drain bias (V_{ds}) is 0.2 V throughout the analysis unless stated otherwise.

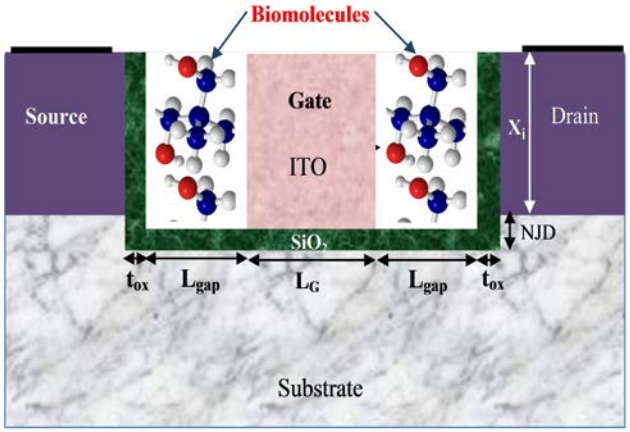


Figure 6.14: Schematic structure of TGRC-MOSFET as a biosensor (Kumar et al, 2018e).

The absorption of different biomolecules is modeled by introducing insulator with dielectric constant same as that of a particular biomolecule in the Nano-gap cavity. The unfilled cavity (i.e. no bio-molecules is present) is modelled by using an insulator having dielectric constant k=1 and dielectric constant of different biomolecules as: streptavidin (k=2.1) (Busse et al, 2002), biotin (k=2.63) (Densmore et al, 2008), 3-aminoppropyltriethoxysilane (APTES) (k=3.57) and protein (k=8) (Kim et al, 2012). Streptavidin-biotin is used to detect Marek's disease virus (MDV) using enzyme-linked immunosorbent assay (ELISA) method (Davidson et al, 1986) while APTES functions as a facilitator to immobilize biomolecules on the surface in the detection process of dengue virus (Zhang et al, 2010).

6.3.2 Results and Discussion

It can be observed from the transfer characteristics of a biosensor (**Figure 6.15(a)**), that when the neutral biomolecules are immobilized (k>1) in the cavity, ON-current enhances significantly in comparison to the absence of biomolecule (k=1) owing to increased value of dielectric constant which increases the transconductance as well (shown in **Figure 6.15(b)**). For the different biomolecules, ammeter indicates the different value of current by which the biomolecule can be identified (Im et al, 2007).

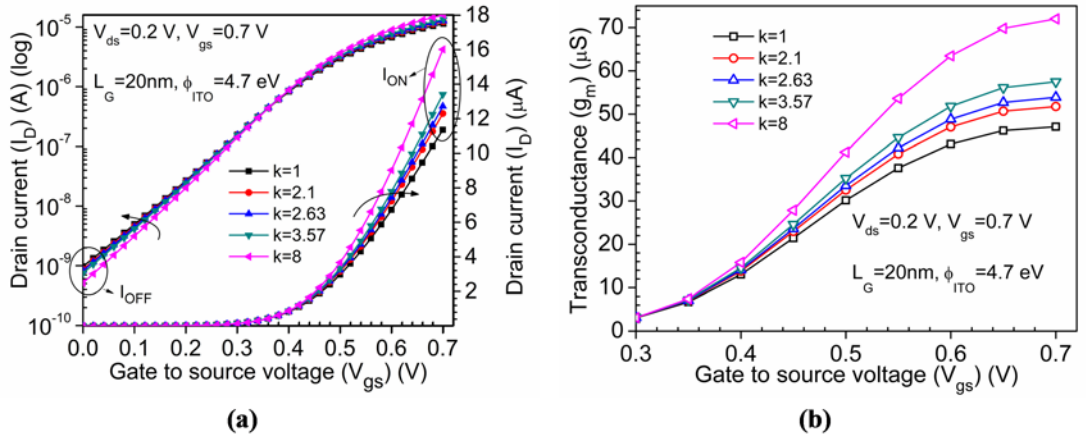


Figure 6.15: (a) Transfer characteristics and (b) Transconductance (g_m); of Nano-gap embedded TGRC-MOSFET in the presence of biomolecules (Kumar et al, 2018e).

Due to increase in ON-current, the switching ratio (I_{ON}/I_{OFF}) also increases with a dielectric value as shown in **Figure 6.16(a)**. Thus, the change in drain current, enhancement in I_{ON} and switching ratio for a particular biomolecule can be used as a key parameter to detect/sense the specific biomolecule. Further, sensitivity is one of the critical parameters for the proposal of a device as a biosensor. In this work, sensitivity (S) is defined as given in equation (6.1)-

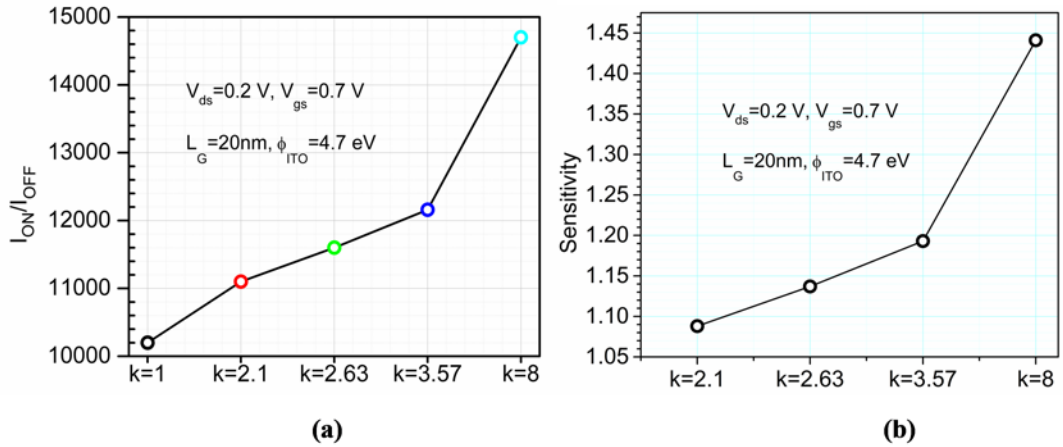


Figure 6.16: (a) Switching ratio (I_{ON}/I_{OFF}) and (b) Impact on sensitivity variation of the various biomolecules at 0.2V drain voltages for TGRC-MOSFET (Kumar et al, 2018e).

$$S = \frac{I_{ON}(k>1)}{I_{ON}(k=1)} \tag{6.1}$$

Figure 6.16(b) reflects the sensitivity of different biomolecules and it is clearly evident that the sensitivity of protein biomolecules (k=8) is higher as

compared to streptavidin, biotin, and APTES (2.1, 2.63, and 3.57 respectively) as the uniform dielectric indicates a specific biomolecule with 100% filled cavity.

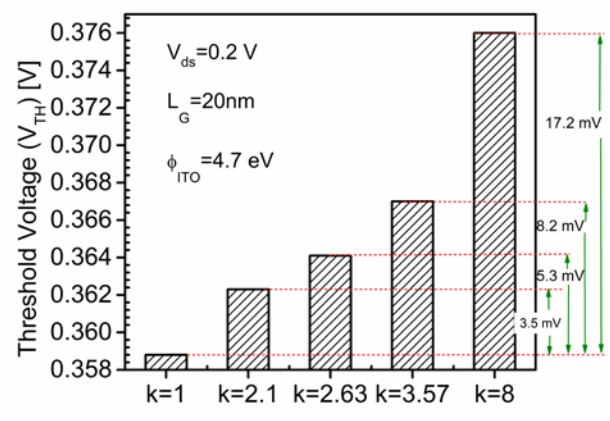
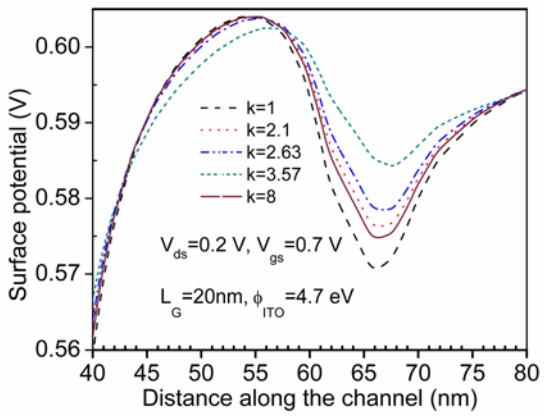


Figure 6.17: Threshold voltage shifts for different biomolecules in TGRC-MOSFET (Kumar et al, 2018e).

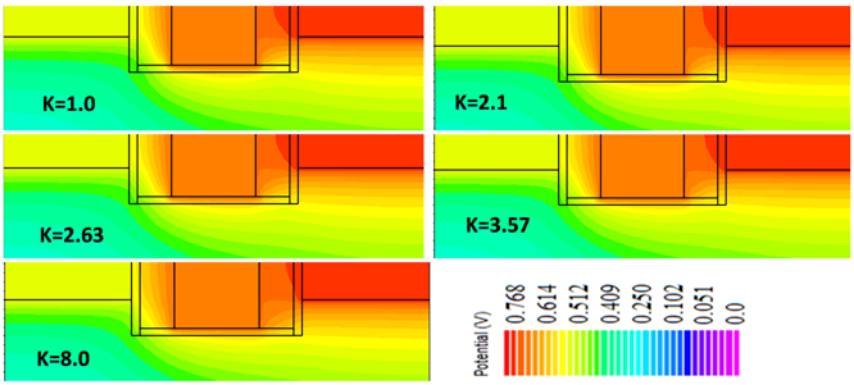
The threshold voltage is used for detection purpose as a sensing parameter, and it is directly related to the dielectric constant. Threshold voltage defines the specific gate voltage at which drain current is equal to 10^{-7} (A/μm) in this work. The threshold voltage enhances as the related dielectric constant of the biomolecule is increased, and the same results are observed for TGRC-MOSFET in which threshold voltage increases with dielectric constant, as shown in **Figure 6.17**. The threshold voltage shift (ΔV_{TH}) of 3.5 mV, 5.3 mV, 8.2 mV and 17.2 mV is observed when dielectric constant changes from the unfilled cavity to the filled cavity with k=2.1, 2.63, 3.57, and 8; as reflected in **Figure 6.17**.

Sometimes threshold voltage shift (ΔV_{TH}) is also called the sensitivity of the biosensor, and it is defined as $\Delta V_{TH} = V_{TH}$ (after absorption of the molecule) - V_{TH} (air-filled cavity) (Choi et al, 2010; Kannan & Kumar, 2013). Threshold voltage shift is directly proportional to the permittivity of the absorbed neutral biomolecule and is given in equation (6.2).

$$\Delta V_{TH} \propto k_{bio} \tag{6.2}$$



(a)



(b)

Figure 6.18: (a) Effect on surface potential in the presence of biomolecules along the channel from source to drain in TGRC-MOSFET. (b) Contour plot of surface potential in the presence of biomolecules (for k=1, 2.1, 2.63, 3.57 and 8) along the channel from source to drain in TGRC-MOSFET (Kumar et al, 2018e).

Thus, it can be said that higher the absolute value of ΔV_{TH}, the better the sensitivity of biosensor as ΔV_{TH} also represented the sensitivity of the device and the threshold voltage shift towards the higher gate voltage in the presence of biomolecule in the nano-gap cavity (Ahangari, 2016). In addition, the electrical performance of TGRC-MOSFET biosensor is also examined in terms of surface potential as shown in **Figure 6.18(a)**. Under the cavity region, the deformation of potential appears (effectively at drain end). When biomolecules are immobilized in the cavity, the change in potential is observed due to change in dielectric constant of bio-molecules. Hence, the shift in potential can detect the presence of biomolecules in the cavity region. Contour plots of surface potential clearly show the change in potential when biomolecules are immobilized in the Nano-cavity as shown in **Figure 6.18(b)**.

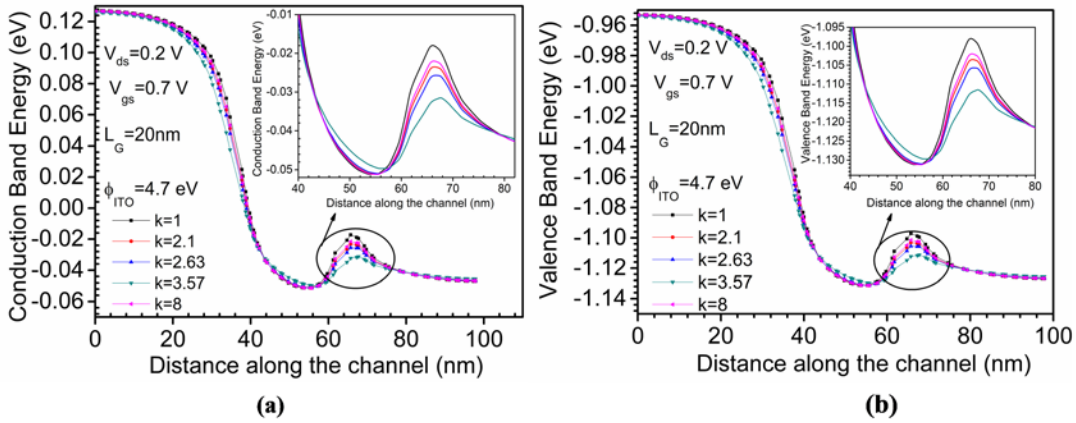


Figure 6.19: Effect on energy bands: (a) Conduction band and (b) Valence band along the channel in the presence of biomolecules in TGRC-MOSFET (Kumar et al, 2018e).

Figure 6.19(a) and **Figure 6.19(b)** reflects the energy band profile (Abdi & Kumar, 2015) in terms of conduction band energy. When the biomolecules are immobilized in the Nano-gap cavity then, change in conduction band energy and valence band energy is clearly evident as shown in **Figure 6.19(a)** and **6.19(b)**. The shift in energy band is more prominent for those biomolecules having dielectric constant 3.57 while less prominent for protein, streptavidin and biotin molecules biomolecules in comparison to the case of absence (Kranti & Armstrong) of biomolecules as reflected in **Figure 6.19(a)** and **6.19(b)**. Thus, TGRC can also be used as a low power sensing device due to effective change in energy band profiles at low drain bias (0.2 V) for different biomolecules.

Moreover, it is also observed from **Figure 6.20(a)** that, in the presence of various biomolecules (k=2.1 to k=8) the electron temperature decreases (~510K) due to high-k (biomolecules) dielectric in the nano cavity-gap, due to which the leakage currents such as hot electron injected gate current and impact ionization substrate current are almost eliminated, and thus I_{ON} (shown in **Figure 6.15(a)**) and sensitivity of the device enhances. Contours plot clearly represent how the temperature varies when the biomolecules come into the Nano-gap cavity, as shown in the **Figure 6.20(b)**. With the change in temperature, change in dielectric constant can detect/sense about which biomolecules are present.

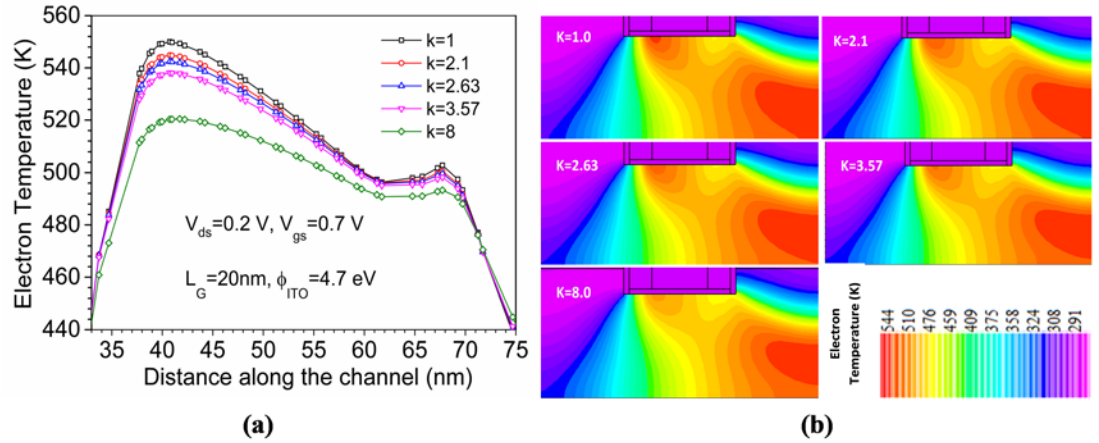


Figure 6.20: (a) Effect on electron temperature along the channel from source to drain and (b) contour plot of electron temperature, in the presence of biomolecules in TGRC-MOSFET (Kumar et al, 2018e).

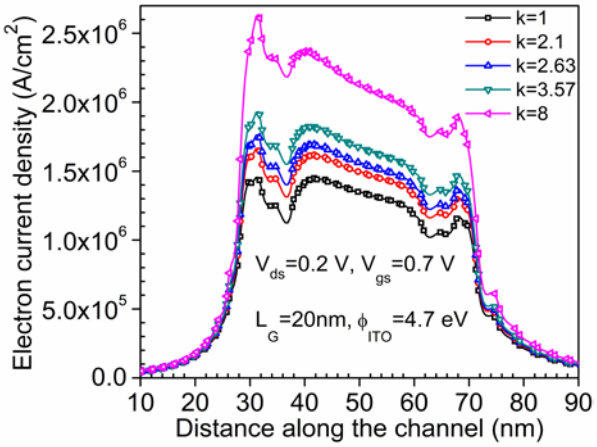


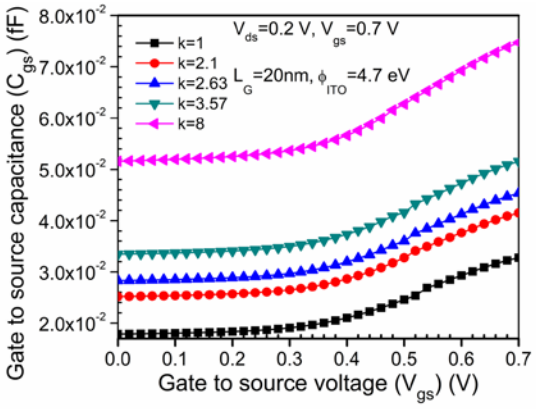
Figure 6.21: Electron current density along the channel from source to drain in the presence of biomolecules in TGRC-MOSFET (Kumar et al, 2018e).

Furthermore, electron current density (Stern et al, 2008) has been observed in the presence and absence of different biomolecules in the nano cavity-gap as shown in **Figure 6.21**. In the proposed biosensor, it is evident that the electron current density is very low when the nano cavity-gap is unfilled (for air, k=1) and when the nano cavity-gap is filled with the different biomolecules in increasing order of dielectric constant then, the electron current density is also increased. For higher current density, I_{ON} will be high due to which the switching ratio is also higher. Thus, the device will be more sensitive when the nano cavity-gap is filled with biomolecules and the sensitivity is higher for higher dielectric constant (as shown in **Figure**

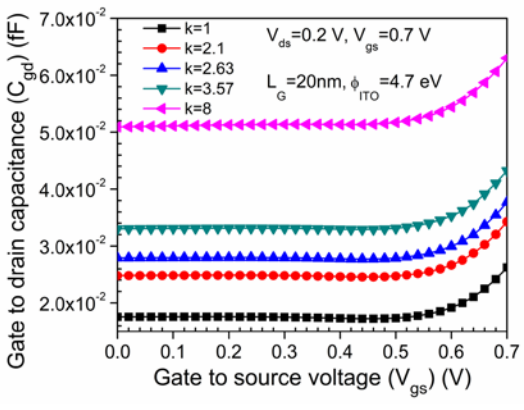
6.16(b)). It has also been observed from **Figure 6.21** that, electron current density is higher just below the nano cavity-gap due to higher gate controllability of TGRC-MOSFET owing to ITO as a gate material.

A. Effect on Parasitic Capacitances

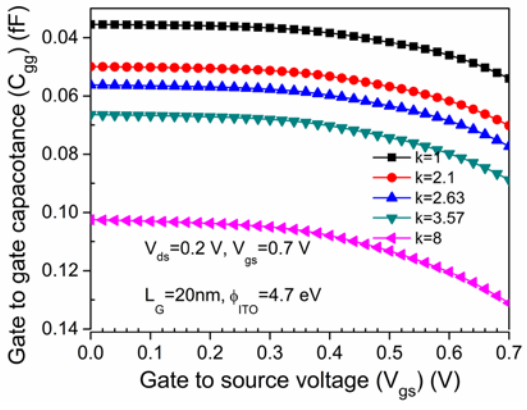
The presence of biomolecule can be easily observed with the change in stray capacitances because the stray (parasitic) capacitances of a field effect transistor are altered by changing the dielectric constant of gate oxide. From **Figure 6.22(a)** and **Figure 6.22(b)**, it is observed that the gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) is altered (increased) by changing (increasing) the corresponding dielectric constant of k=2.1, 2.63, 3.57 and 8 in comparison to unfilled cavity gap.



(a)



(b)



(c)

Figure 6.22: (a) Effect on parasitic capacitances (a) C_{gs} (b) C_{gd} (c) C_{gg}; in the presence of biomolecules in TGRC-MOSFET (Kumar et al, 2018e).

When V_{gs} increases, the accumulation of charge carriers near the gate increases (Kumar et al) and as a result, gate-source capacitance and gate-drain capacitance increases. Similarly, gate capacitance (C_{gg}) is altered in the presence different dielectric constant and when V_{gs} increases, the accumulation of charges at the gate increases and thus increases the gate capacitance (Kumar et al) as shown in **Figure 6.22(c)**. When the molecules having higher dielectric constant are immobilized, then the change in the capacitances is more prominent while less prominent for lower dielectric constant as evident from **Figure 6.22(a)**, **(b)** and **(c)**. Parasitic capacitances must be as low as possible in a semiconductor device for high-performance applications. Here, all the parasitic capacitances (C_{gs}, C_{gd} and C_{gg}) which have been evaluated in the presence of different biomolecules, are quite low in the femtofarad scale.

B. Noise Assessment

In the presence of any external agent/biomolecules in the channel region of CMOS, the electrical behavior in terms of I-V characteristics gets altered. This shift in I-V characteristics and other electrical behavior used as a key parameter for the detection of biomolecules is clearly observed in previous sections. But on the contrary, these carriers or biomolecules sometimes leads to noise which also degrades the biosensor performance. Therefore, to examine the noise immunity of proposed biosensor, noise FOMs such as minimum noise figure, noise conductance, etc. has also been studied w.r.t. frequency (Gupta & Chaujar, 2016a).

It is evidently shown in **Figure 6.23(a)** and **Figure 6.23(b)**, as biomolecules are immobilized in the cavity, all the noise parameters (noise conductance and min noise figure respectively) improve significantly at high frequency. This observation is mainly attributed to the transparent conducting material (ITO) in the TGRC-MOSFET architecture because, in a transparent material, random motion of free electrons decreases. In transparent conducting material, the temperature rise is not much significant [shown in **Figure 6.20(a)**] when the concentration of charge carriers is increased, due to which noise immunity of TGRC biosensor in the presence of biomolecules improves.

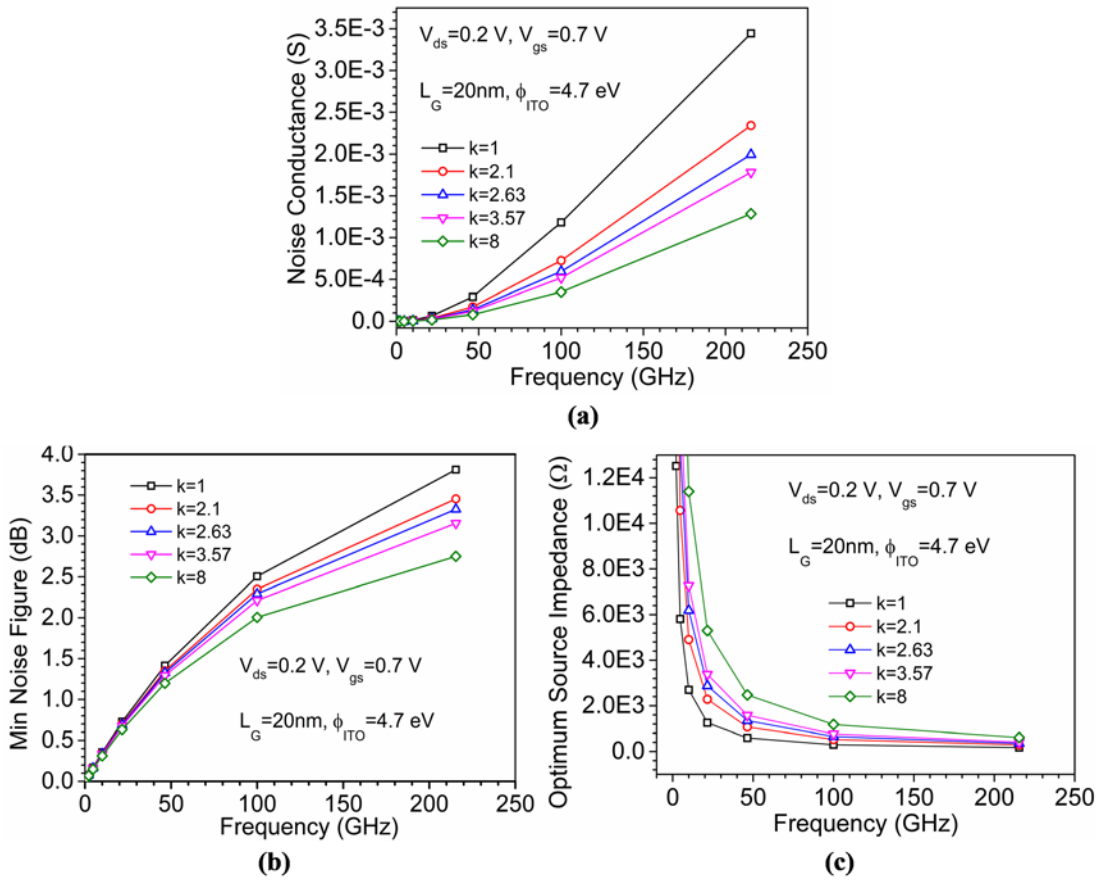


Figure 6.23: (a) Noise conductance, (b) Minimum noise figure, and (c) Optimum source impedance; in the presence of biomolecules in TGRC-MOSFET at GHz frequency range (Kumar et al, 2018e).

Furthermore, **Figure 6.23(c)** reflects another noise parameter called optimum source impedance ($Z_{OPT}=R_{OPT}+jX_{OPT}$) with respect to frequency for different biomolecules and it is observed that optimum source impedance is nearly zero for higher frequency when the nano cavity-gap is empty and further, it is increased when the dielectric constant of the biomolecule is increased which reflects that the device exhibits less noise in the presence of biomolecules and thus the device is suitable for the bio-sensing applications.

C. Effect of Nano-gap Cavity Length

Moreover, the effect of cavity length (L_{gap}) (Abdi & Kumar, 2015) has also been observed in this work with an aim to investigate how much the sensitivity and thus the performance of biosensor vary with change in gap length.

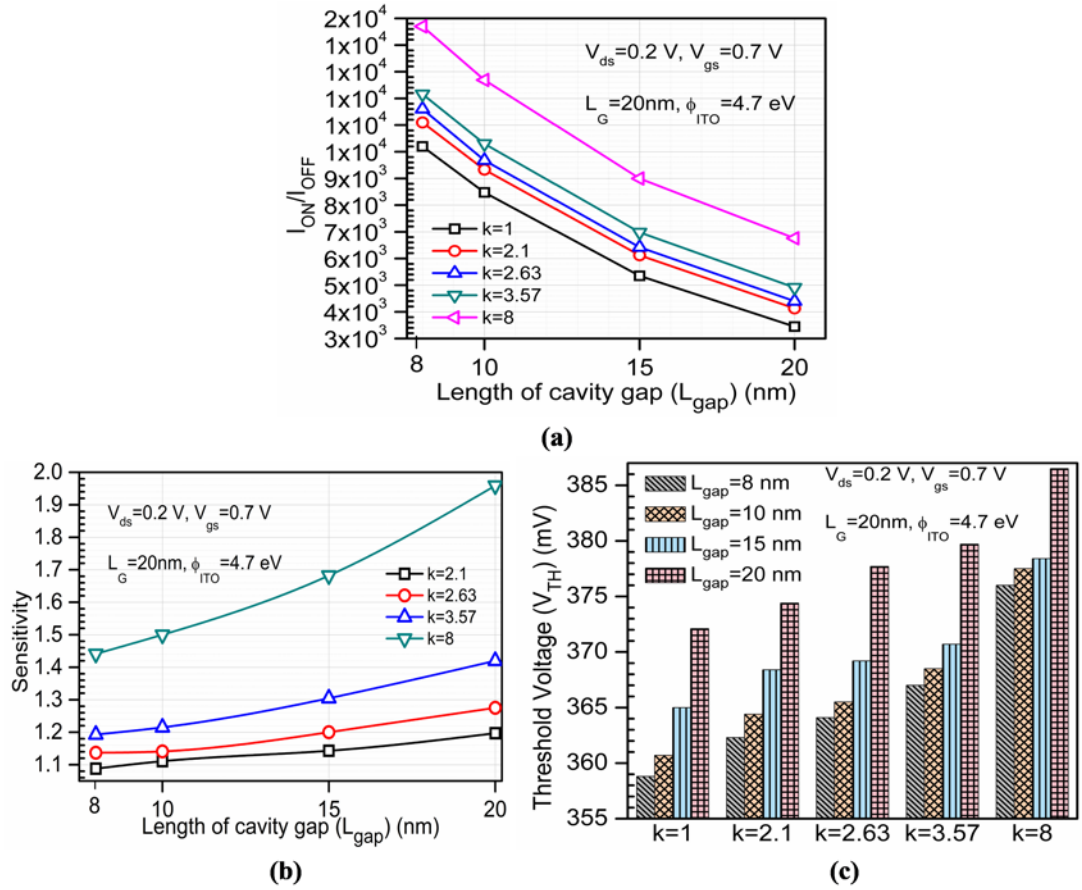


Figure 6.24: (a) The impact of length of cavity gap variation on switching ratio, (b) The impact of length of cavity gap variation on Sensitivity, and (c) The impact of length of cavity gap variation on Threshold voltage; for different biomolecules in TGRC-MOSFET (Kumar et al, 2018e).

Figure 6.24(a) shows with an increase in cavity gap length, I_{ON}/I_{OFF} ratio reduce evidently due to increase in OFF current owing to higher capacitance. Moreover, the sensitivity of TGRC-biosensor is also observed at different cavity gap length and it is found that sensitivity increases significantly with the increase in L_{gap} as shown in **Figure 6.24(b)**. From the figure, it is also observed that the sensitivity increases from a lower value of k to a higher value of k (for each L_{gap}). Thus, with L_{gap}=20nm, nano-gap embedded TGRC-biosensor shows better sensitivity at k=8 (protein) biomolecules in comparison to other biomolecules. **Figure 6.24(c)** displays the change in threshold voltage due to change in L_{gap} (from 8 nm to 20 nm) for different biomolecules and it is observed that more noticeable change in threshold voltage (due to change in dielectric constant) is used as one of the sensing parameters for detection of biomolecules. Thus, 20nm cavity-gap length of TGRC MOSFET

show optimum performance and hence, can be employed as a low power, high sensitive biosensor to diagnose various associated diseases.

6.4 SUMMARY

The first part of this chapter propopsed an x-ray dosimeter which is able to achieve radiation sensitivity up to 1.11 mV/kRad in TGRC MOSFET. In 1k to 10kRad dose range, the electrical characteristics of the MOSFET have shown an almost linear trend. Threshold voltage showed a linear negative shift and ON current, a linear positive shift. We further investigated the effects of varying the oxide thickness on radiation sensitivity, as oxide thickness is one of the most important factors responsible for threshold voltage shift, our dosimetric parameter. An increment of 246% in sensitivity was observed when we increased oxide thickness from 4nm to 6nm and decrement of 81 %, when we reduced oxide thickness from 4nm to 2nm. Hence, for TGRC MOSFET to be used as a dosimeter, thicker oxide is recommended, but under dimensional constraints: 2nm, 4nm, 6nm, oxide thickness generated acceptable threshold voltage shift, thus can be effectively used as a dosimeter. In future medical applications, the proposed device can be used as implantable dosimeter due to extremely small form factor (nano-scale dimensions) leading to accurate dose determination which is of utmost requirement in medical dosimetry.

The second part of this chapter explores nano-gap embedded; ITO gated Recessed Channel MOSFET as a biosensor. For the detection of various biomolecules, electrical behavior was studied in terms of threshold voltage shift, sensitivity, switching ratio, surface potential, capacitance and noise FOMs. Results so obtained clearly revealed that due to ITO gate in the nano-gap cavity, the electrical performance of the TGRC biosensor enhances significantly and sensitivity of a biosensor is higher in case the high dielectric value of biomolecule. It is found that with protein biomolecule ($k\approx8$), sensitivity is higher amongst the rest with higher noise immunity. Thus, TGRC-MOSFET biosensor proves to be a favorable device for the sensing applications owing to its high sensitivity and low power electrical detection property of different biomolecules. Further, the efficacy of cavity gap length is also examined for switching ratio, V_{TH}, and sensitivity of proposed biosensor and

found that sensitivity increases with increase in cavity length but overall biosensor performance slightly degrades. Therefore, there is need to optimize the value of cavity gap length for better performance. As sub-20nm TGRC-MOSFET can be, thus employed at a low noise, high speed and high sensitive biosensor for the detection of various associated diseases.

6.5 REFERENCES

Abdi, D. B. & Kumar, M. J. (2015) Dielectric modulated overlapping gate-on-drain tunnel-FET as a label-free biosensor. *Superlattices and Microstructures*, 86, 198-202.

Ahangari, Z. (2016) Performance assessment of dual material gate dielectric modulated nanowire junctionless MOSFET for ultrasensitive detection of biomolecules. *RSC Advances*, 6(92), 89185-89191.

Ahn, J.-H., Choi, S.-J., Han, J.-W., Park, T. J., Lee, S. Y. & Choi, Y.-K. (2010) Double-gate nanowire field effect transistor for a biosensor. *Nano letters*, 10(8), 2934-2938.

Allenspach, M., Dachs, C., Johnson, G., Schrimpf, R., Lorfevre, E., Palau, J., Brews, J., Galloway, K., Titus, J. & Wheatley, C. (1996) SEGR and SEB in n-channel power MOSFETs. *IEEE Transactions on Nuclear Science*, 43(6), 2927-2931.

Ausman Jr, G. A. & McLean, F. B. (1975) Electron− hole pair creation energy in SiO2. *Applied Physics Letters*, 26(4), 173-175.

Azmi, M. M., Tehrani, Z., Lewis, R., Walker, K.-A., Jones, D., Daniels, D., Doak, S. & Guy, O. (2014) Highly sensitive covalently functionalised integrated silicon nanowire biosensor devices for detection of cancer risk biomarker. *Biosensors and Bioelectronics*, 52, 216-224.

Barsan, R. M. (1981) Analysis and modeling of dual-gate MOSFET's. *Electron Devices, IEEE Transactions on*, 28(5), 523-534.

Benedetto, J. M. & Boesch, H. (1986) The relationship between 60co and 10-kev x-ray damage in mos devices. *IEEE Transactions on Nuclear Science*, 33(6), 1317-1323.

Bergveld, P. (1986) The development and application of FET-based biosensors. *Biosensors*, 2(1), 15-33.

Berland, V., Touboul, A., Dupont-Nivet, E. & Leray, J.-L. (1991) Effect of x-ray radiation on MOSFET's (SIMOX) LF excess noise, *Radiation and its Effects on Devices and Systems, 1991. RADECS 91., First European Conference on*. IEEE.

Busse, S., Scheumann, V., Menges, B. & Mittler, S. (2002) Sensitivity studies for specific binding reactions using the biotin/streptavidin system by evanescent optical methods. *Biosensors and Bioelectronics*, 17(8), 704-710.

Chandan, B. V., Nigam, K. & Sharma, D. (2018) Junctionless based dielectric modulated electrically doped tunnel FET based biosensor for label-free detection. *Micro & Nano Letters*, 13(4), 452-456.

Chaujar, R., Kaur, R., Saxena, M., Gupta, M. & Gupta, R. (2008a) Laterally amalgamated DUal material GAte concave (L-DUMGAC) MOSFET for ULSI. *Microelectronic Engineering*, 85(3), 566-576.

Chaujar, R., Kaur, R., Saxena, M., Gupta, M. & Gupta, R. (2008b) TCAD assessment of gate electrode workfunction engineered recessed channel (GEWE-RC) MOSFET and its multilayered gate architecture—part I: hot-carrier-reliability evaluation. *Electron Devices, IEEE Transactions on*, 55(10), 2602-2613.

Choi, J.-M., Han, J.-W., Choi, S.-J. & Choi, Y.-K. (2010) Analytical modeling of a nanogap-embedded FET for application as a biosensor. *IEEE Transactions on Electron Devices*, 57(12), 3477-3484.

Comini, E., Baratto, C., Concina, I., Faglia, G., Falasconi, M., Ferroni, M., Galstyan, V., Gobbi, E., Ponzoni, A., Vomiero, A., Zappa, D., Sberveglieri, V. & Sberveglieri, G. (2013) Metal oxide nanoscience and nanotechnology for chemical sensors. *Sensors and Actuators B: Chemical*, 179, 3-20.

Davidson, I., Malkinson, M., Strenger, C. & Becker, Y. (1986) An improved ELISA method, using a streptavidin-biotin complex, for detecting Marek's disease virus antigens in feather-tips of infected chickens. *Journal of virological methods*, 14(3-4), 237-241.

Densmore, A., Xu, D.-X., Janz, S., Waldron, P., Mischki, T., Lopinski, G., Delâge, A., Lapointe, J., Cheben, P. & Lamontagne, B. (2008) Spiral-path high-sensitivity silicon photonic wire molecular sensor with temperature-independent response. *Optics letters*, 33(6), 596-598.

Gao, A., Lu, N., Dai, P., Li, T., Pei, H., Gao, X., Gong, Y., Wang, Y. & Fan, C. (2011) Silicon-nanowire-based CMOS-compatible field-effect transistor

nanosensors for ultrasensitive electrical detection of nucleic acids. *Nano letters*, 11(9), 3974-3978.

Gupta, N. & Chaujar, R. (2016a) Influence of gate metal engineering on small-signal and noise behaviour of silicon nanowire MOSFET for low-noise amplifiers. *Applied Physics A*, 122(8), 1-9.

Gupta, N. & Chaujar, R. (2016b) Investigation of temperature variations on analog/RF and linearity performance of stacked gate GEWE-SiNW MOSFET for improved device reliability. *Microelectronics Reliability*, 64, 235-241.

Gupta, N. & Chaujar, R. (2016c) Optimization of high-k and gate metal workfunction for improved analog and intermodulation performance of Gate Stack (GS)-GEWE-SiNW MOSFET. *Superlattices and Microstructures*.

Gupta, N., Kumar, A. & Chaujar, R. (2015) Oxide bound impact on hot-carrier degradation for gate electrode workfunction engineered (GEWE) silicon nanowire MOSFET. *Microsystem Technologies*.

Im, H., Huang, X.-J., Gu, B. & Choi, Y.-K. (2007) A dielectric-modulated field-effect transistor for biosensing. *Nature nanotechnology*, 2(7), 430-434.

Kannan, N. & Kumar, M. J. (2013) Dielectric-modulated impact-ionization MOS transistor as a label-free biosensor. *IEEE Electron Device Letters*, 34(12), 1575-1577.

Kanungo, S., Chattopadhyay, S., Gupta, P. S., Sinha, K. & Rahaman, H. (2016) Study and analysis of the effects of SiGe source and pocket-doped channel on sensing performance of dielectrically modulated tunnel FET-based biosensors. *IEEE Transactions on Electron Devices*, 63(6), 2589-2596.

Kim, S., Baek, D., Kim, J.-Y., Choi, S.-J., Seol, M.-L. & Choi, Y.-K. (2012) A transistor-based biosensor for the extraction of physical properties from biomolecules. *Applied Physics Letters*, 101(7), 073703.

Kranti, A. & Armstrong, G. A. (2006) Engineering source/drain extension regions in nanoscale double gate (DG) SOI MOSFETs: Analytical model and design considerations. *Solid-state electronics*, 50(3), 437-447.

Kumar, A. (2017) Effect of Trench Depth and Gate Length Shrinking Assessment on the Analog and Linearity Performance of TGRC-MOSFET. *Superlattices and Microstructures*.

Kumar, A., Gupta, N. & Chaujar, R. (2016a) Analysis of novel transparent gate recessed channel (TGRC) MOSFET for improved analog behaviour. *Microsystem Technologies*, 22(11), 2665-2671.

Kumar, A., Gupta, N. & Chaujar, R. (2016b) Effect of structured parameters on the hot-carrier immunity of transparent gate recessed channel (TGRC) MOSFET. *Microsystem Technologies*, 1-8.

Kumar, A., Gupta, N. & Chaujar, R. (2016c) Power gain assessment of ITO based Transparent Gate Recessed Channel (TGRC) MOSFET for RF/wireless applications. *Superlattices and Microstructures*, 91, 290-301.

Kumar, A., Gupta, N. & Chaujar, R. (2016d) TCAD RF performance investigation of Transparent Gate Recessed Channel MOSFET. *Microelectronics Journal*, 49, 36-42.

Kumar, A., Gupta, N. & Chaujar, R. (2017a) Effect of structured parameters on the hot-carrier immunity of transparent gate recessed channel (TGRC) MOSFET. *Microsystem Technologies*, 23(9), 4057-4064.

Kumar, A., Tiwari, B., Singh, S., Tripathi, M. M. & Chaujar, R. (2018a) Radiation Analysis of N-Channel TGRC-MOSFET: An X-Ray Dosimeter. *IEEE Transactions on Electron Devices*, 65(11), 5014-5020.

Kumar, A., Tiwari, B., Singh, S., Tripathi, M. M. & Chaujar, R. (2018b) Radiation Analysis of N-Channel TGRC-MOSFET: An X-Ray Dosimeter. *IEEE Transactions on Electron Devices*, 1-7.

Kumar, A., Tripathi, M. & Chaujar, R. Investigation of parasitic capacitances of In2O5Sn gate electrode recessed channel MOSFET for ULSI switching applications. *Microsystem Technologies*, 1-8.

Kumar, A., Tripathi, M. & Chaujar, R. (2017b) Investigation of parasitic capacitances of In2O5Sn gate electrode recessed channel MOSFET for ULSI switching applications. *Microsystem Technologies*, 23(12), 5867-5874.

Kumar, A., Tripathi, M. & Chaujar, R. (2018c) In 2 O 5 Sn Based Transparent Gate Recessed Channel MOSFET: RF Small-Signal Model for Microwave

Applications. *AEU-International Journal of Electronics and Communications*.

Kumar, A., Tripathi, M. & Chaujar, R. (2018d) Reliability Issues of In2O5Sn Gate Electrode Recessed Channel MOSFET: Impact of Interface Trap Charges and Temperature. *IEEE Transactions on Electron Devices*, 65, 860-866.

Kumar, A., Tripathi, M. M. & Chaujar, R. (2018e) Ultralow-power dielectric-modulated nanogap-embedded sub-20-nm TGRC-MOSFET for biosensing applications. *Journal of Computational Electronics*, 17(4), 1807-1815.

Lee, J., Jang, J., Choi, B., Yoon, J., Kim, J.-Y., Choi, Y.-K., Kim, D. M., Kim, D. H. & Choi, S.-J. (2015) A Highly Responsive Silicon Nanowire/Amplifier MOSFET Hybrid Biosensor. *Scientific reports*, 5.

Minami, T. (2005a) Transparent conducting oxide semiconductors for transparent electrodes. *Semiconductor Science and Technology*, 20(4), S35-S44.

Minami, T. (2005b) Transparent conducting oxide semiconductors for transparent electrodes. *Semiconductor Science and Technology*, 20(4), S35.

Morgan, D., Salehi, A., Aliyu, Y., Bunce, R. & Diskett, D. (1995) Radiation damage in indium tin oxide (ITO) layers. *Thin Solid Films*, 258(1-2), 283-285.

Nakamura, M., Ishihara, Y., Matsuo, Y., Iizuka, Y., Ueki, N., Iramina, H., Hirashima, H. & Mizowaki, T. (2018) Quantification of the kV X-ray imaging dose during real-time tumor tracking and from three-and four-dimensional cone-beam computed tomography in lung cancer patients using a Monte Carlo simulation. *Journal of radiation research*, 59(2), 173-181.

Oldham, T. R. & McLean, F. (2003) Total ionizing dose effects in MOS oxides and devices. *IEEE Transactions on Nuclear Science*, 50(3), 483-499.

Saks, N., Ancona, M. & Modolo, J. (1984) Radiation effects in MOS capacitors with very thin oxides at 80 K. *IEEE Transactions on Nuclear Science*, 31(6), 1249-1255.

Sang, S., Wang, Y., Feng, Q., Wei, Y., Ji, J. & Zhang, W. (2016) Progress of new label-free techniques for biosensors: a review. *Critical reviews in biotechnology*, 36(3), 465-481.

Schwank, J. R., Shaneyfelt, M. R., Fleetwood, D. M., Felix, J. A., Dodd, P. E., Paillet, P. & Ferlet-Cavrois, V. (2008) Radiation effects in MOS oxides. *IEEE Transactions on Nuclear Science*, 55(4), 1833-1853.

Seco, J., Clasie, B. & Partridge, M. (2014) Review on the characteristics of radiation detectors for dosimetry and imaging. *Physics in Medicine & Biology*, 59(20), R303.

SILVACO, I. (2011) ATLAS User's Manual. *Santa Clara, CA, Ver*, 5.

Sreelal, S., Lau, C. & Samudra, G. (2002) Parasitic capacitance characteristics of deep submicrometre grooved gate MOSFETs. *Semiconductor science and technology*, 17(3), 179.

Stern, E., Vacic, A. & Reed, M. A. (2008) Semiconducting nanowire field-effect transistor biomolecular sensors. *IEEE Transactions on Electron Devices*, 55(11), 3119-3130.

Villani, E., Gabrielli, A., Khan, A., Pikhay, E., Roizin, Y. & Zhang, Z. (2013) Monolithic 180 nm CMOS dosimeter for in vivo medical applications. *IEEE Transactions on Nuclear Science*, 60(2), 843-849.

Vu, X. T., Eschermann, J. F., Stockmann, R., GhoshMoulick, R., Offenhäusser, A. & Ingebrandt, S. (2009) Top-down processed silicon nanowire transistor arrays for biosensing. *physica status solidi (a)*, 206(3), 426-434.

Xiao-Hua, M., Yue, H., Bao-Gang, S., Hai-Xia, G., Hong-Xia, R., Jin-Cheng, Z., Jin-Feng, Z., Xiao-Ju, Z. & Wei-Dong, Z. (2006) Fabrication and characterization of groove-gate MOSFETs based on a self-aligned CMOS process. *Chinese Physics*, 15(1), 195.

Zhang, G.-J., Zhang, L., Huang, M. J., Luo, Z. H. H., Tay, G. K. I., Lim, E.-J. A., Kang, T. G. & Chen, Y. (2010) Silicon nanowire biosensor for highly sensitive and rapid detection of Dengue virus. *Sensors and Actuators B: Chemical*, 146(1), 138-144.

7

CHAPTER

Conclusion and Future Scope

- *This chapter recapitulates the overall work carried out in this thesis.*
- *In addition, the concrete conclusion drawn from the results obtained are also briefly highlighted.*
- *Thereafter, this chapter describes the possible future scope of the work that could be done in future to extend the research.*

7.1 CONCLUSION

CMOS scaling has been the driving machinery for the ever-increasing number of functionalities and significant miniaturization of the integrated circuits (ICs) enabling this era of big data and internet of things (IoT). Therefore, there is a need to explore new device structure with innovative material which extends Moore's Law. In this regard, a planar device structure called transparent gate recessed channel (TGRC) MOSFET has been proposed with In_2O_5Sn, a transparent conducting material which improves device efficiency and reduces short channel effects that could assist next-generation logic transistor operational at less than 0.2 V. In this thesis, all types of scaling issues of proposed device structure, i.e., TGRC MOSFET have been critically scrutinized and compared with the conventional structures. The analysis exemplified that this device structure has overcome the drawbacks faced by conventional structures and provides an extremely high packing density with improved device performance. Moreover, to overcome various challenges during the fabrication of non-planar devices, In_2O_5Sn has been integrated on recessed channel MOSFET to acquire lower SS, higher I_{ON}, along with low leakage current. Furthermore, for the comprehensive study of the analog, linearity, and intermodulation distortion analysis of TGRC MOSFET has been explored in **Chapter 2** with the impact of trench gate and gate length miniaturization at sub-30 nm regime. From the investigation, it has been found that TGRC MOSFET achieves high current driving capability due to ITO as a gate material in comparison to conventional MOSFETs which results in high transconductance (increased by 32.1% and 35% compared to conventional MOSFET and CRC-MOSFET respectively) and improved device efficiency. Further, it is also observed that TGRC exhibit a significant enhancement in peak values of VIP2, VIP3, 1-dB compression point, IIP3 and lesser values of the IMD3 and HD3 in comparison to its counterparts at 5 nm NJD and 20 nm gate length. Therefore, TGRC-MOSFET delivered enriched analog and linearity performance in terms of superior input power and lesser signal distortion. Moreover, it is also analyzed that with the tuning of TGRC's parameters such as L_G and NJD, its analog and linearity performance enhances appreciably owing to enhanced current driving capability and reduced g_{m3} (distortions). Therefore, the proposed TGRC-MOSFET is prominent for high scale

integration, which can be developed for RFIC design and it is also a favorable candidate for ultra-low power, analog, and distortion-less application.

In addition, for sub-nm devices, reliability is of serious concern, owing to various process/stress/radiation damages that induce interface charges at the Si-SiO_2 interface. Ideally, the impact of interface defect along the Si-SiO_2 interface is neglected in almost all the research articles. However, practically a large number of positive/negative charges are present along the Si-SiO_2 interface and also ionic charges may be found within the SiO_2 layer. These interface trap charges (ITC) may be reduced significantly by advanced fabrication techniques but can never be uprooted, and thus they appear inevitably in any fabricated transistor. Thus, to ensure the reliability of the device, it is essential to investigate the characteristics of the device in the presence of various ITCs that is a primary focus area in **Chapter 3**.

Along with the influence of ITCs on the static, linearity, and distortion FOMs, low-temperature reliability has also been explored in the proposed device structure and has also been compared with conventional recessed channel (CRC) MOSFET through extensive device simulations. The proposed device is suitable for high switching applications even in the presence of trap charges. It has been shown that the TGRC MOSFET exhibit superior current driving capability, high linearity (VIP3 and IIP3) with low distortions. It has also been observed that TGRC MOSFET is more immune to ITC even in the density variation with different polarity (acceptor and donor). Likewise, it is also found that TGRC-MOSFET at low temperature (150K) in the presence of ITCs show negligible variation in device behavior in terms of I_{ds}, g_m, VIP3, IIP3, HD2, HD3, and IMD3. Thus, it signifies that TGRC-MOSFET is more reliable at low temperatures and serves as a promising candidate for analog and low power-high linearity applications.

Moreover, highly scaled TGRC MOSFET that promises the high integration must ensure the excellent switching performance and must guarantee for the minimum parasitic capacitances. Thus, to ensure for the superior switching performance of the proposed device, i.e., TGRC MOSFET has been explored for various capacitance dependent Figure of Merits (FOMs) and is the central point of

discussion in **Chapter 4**. Thus, **Chapter 4** analyzes the capacitance-voltage characteristics of In_2O_5Sn gate electrode recessed channel MOSFET with 30 nm gate length to examine the parasitic capacitances. The simulated results are then used to isolate the parasitic capacitances. The effect of In_2O_5Sn gate electrode (as a transparent gate electrode) in recessed channel MOSFET has been studied in terms of bias and frequency-dependent parasitic capacitances and capacitance dependent FOMs such as TFP, EDP, and GBP for high switching performance. It is observed that with the amalgamation of In_2O_5Sn with RC MOSFET, parasitic capacitances decrease in comparison to aluminium gate metal (CRC MOSFET). When the gate length reduces to 20 nm, then the parasitic capacitances get reduced, and the overall parasitic capacitances reduce in TGRC architecture by ~25%. Hence, the device is more suitable at the sub-20 nm regime. It is also found that with the variation in frequency, parasitic capacitance reduces due to the high current driving capability of TGRC MOSFET; thus, TGRC architecture proves to be a promising contender for high frequency/switching applications in 22 nm node technology.

In addition to superior switching performance with reduced parasitic capacitances, highly scaled MOSFET that promises the high integration must ensure the excellent RF performance. Thus, to ensure for the superior RF/microwave performance, TGRC MOSFET has been explored in terms of small signal modeling and RF Figure of Merits (FOMs) in **Chapter 5**. **Chapter 5** discusses the non-quasi-static (NQS) small signal modeling of TGRC-MOSFET in terms of microwave and electrical parameters, i.e., impedance, admittance, and hybrid parameters. It is found that TGRC-MOSFET shows high input impedance and low output impedance owing to the transparent gate which improves the current driving capability and thus the device HF performance in comparison to conventional RC MOSFET. Further, the transfer impedance also improves in TGRC device as compared to the conventional device due to reduced SCEs and high ON current which enhances the ultimate gain of the device and thus can be useful in wireless/millimeter wave applications. Moreover, the calculated model results of small signal parameters are in good agreement with the simulation results so obtained at the THz range and thus validated the small signal

model. Results show that the proposed device is best suited for superior RF/Microwave applications.

After discussing the high switching and superior RF performance of TGRC device, it is further used for sensing application such as radiation sensor (as a dosimeter) and biosensor in **Chapter 6** with higher sensitivity in sub-20 nm regime. **Chapter 6** is primarily divided into two parts; the first part of the chapter proposes the application of TGRC-MOSFET as an x-ray dosimeter which is able to achieve radiation sensitivity up to 1.11 mV/kRad. In 1k to 10kRad dose range, the electrical characteristics of the MOSFET have shown an almost linear trend. Threshold voltage showed a linear negative shift and ON current a linear positive shift. We further investigated the effects of varying the oxide thickness on radiation sensitivity, as oxide thickness is one of the most important factors responsible for threshold voltage shift, a dosimetric parameter. An increment of 246% in sensitivity was observed when we increased oxide thickness from 4 nm to 6 nm and decrement of 81 % when we reduced oxide thickness from 4 nm to 2 nm. Hence for TGRC MOSFET to be used as a dosimeter, the thicker oxide is recommended, but under dimensional constraints: 2nm, 4nm, 6nm, oxide thickness generated acceptable threshold voltage shift. Thus it can be effectively used as a dosimeter. In future medical applications, the proposed device can be used as an implantable dosimeter due to extremely small form factor (nano-scale dimensions) leading to accurate dose determination which is the utmost requirement in medical dosimetry.

The second part of this chapter explores nano-gap embedded; ITO gated Recessed Channel MOSFET as a biosensor. For the detection of various biomolecules, electrical behavior was studied in terms of threshold voltage shift, sensitivity, switching ratio, surface potential, capacitance, and noise FOMs. Results so obtained clearly revealed that due to ITO gate in the nano-gap cavity, the electrical performance of the TGRC biosensor enhances significantly and sensitivity of a biosensor is higher in case of high dielectric value of biomolecule. It is found that with protein biomolecule ($k \approx 8$), sensitivity is higher amongst the rest with higher noise immunity. Thus, TGRC-MOSFET biosensor proves to be a favorable device for

the sensing applications owing to its high sensitivity and low power electrical detection property of different biomolecules.

Further, the efficacy of cavity gap length is also examined for switching ratio, V_{TH}, and sensitivity of proposed biosensor and found that sensitivity increases with an increase in cavity length, but overall biosensor performance slightly degrades. Therefore, there is a need to optimize the value of cavity gap length for better performance. Hence, sub-20nm TGRC-MOSFET can be employed at low noise, high speed and high sensitive biosensor for the detection of various associated diseases.

By achieving these research objectives, we can give the design of an optimum device which can be used efficiently in analog/digital and sensing applications. Also, results so obtained can be served as a worthy design tool for design and process engineers in medical applications.

7.2 FUTURE SCOPE

The key encompassing objective of this thesis is to design an In_2O_5Sn gated recessed channel MOSFET which can overwhelm the major shortcomings of conventional MOSFET. Further, the proposed device design is also investigated for their reliability in terms of interface trap charges that are inevitably present along the interface of Si-SiO_2 in any practical device. Another objective of this research work is to examine the proposed device under a wide temperature range to check the temperature robustness while employing the device under a temperature sensitive environment. Additionally, the applicability of the device as an X-ray dosimeter and biosensor has also been investigated. Some of the objectives are accomplished through analytical modeling and extensive numerical simulations. However, given the above work, it would be interesting to explore and extend the following aspects as future aspects.

1. This work can be further extended by performing quantum analytical modeling of TGRC MOSFET considering the effect of SCEs in terms of the threshold voltage, drain current, etc, to verify the simulated results.

2. The work done in this thesis accounts for only the fixed ITC, and the impact of mobile charges are ignored. Thus, to comprehend the reliability aspects in terms of defects, it is needed to analyze the device under both mobile and fixed ITC, and hence it could be taken up as future work.

3. The work done has been accounted for only Si as a source, channel and drain material and chiefly the numerous engineering schemes have been explored for defeating the challenges faced by conventional MOSFETs. Thus, the device must be analyzed by employing various materials that essentially deals with the material engineering and could be addressed in the future.

4. Further, the effect of the fringing field becomes prominent when gate stacking is used. Therefore, there is a need to consider this effect to accurately depict the device behavior at the sub-nm regime.

5. The circuit response of the proposed TGRC MOSFET can also be done to employ it for digital circuit applications such as for CMOS inverters, RAM, and other gated logic designs.

6. Moreover, the device design can be utilized as a gas sensor which can sense harmful gases.

Reliability Issues of In_2O_5Sn Gate Electrode Recessed Channel MOSFET: Impact of Interface Trap Charges and Temperature

Ajay Kumar, *Student Member, IEEE*, M. M. Tripathi, *Senior Member, IEEE*, and Rishu Chaujar, *Senior Member, IEEE*

***Abstract*— In this paper, reliability issues of In_2O_5Sn (indium–tin oxide: a transparent material) transparent gate recessed channel (TGRC)-MOSFET has been analyzed by considering the effect of interface trap charges (both positive and negative) present at the Si/SiO_2 interface. Following device, characteristics are studied in terms of static, linearity, and intermodulation figure of merits. It is found that with the amalgamation of the transparent gate indium tin oxide on conventional recesses channel (CRC) MOSFET, it exhibits improved immunity against interface trap charges in comparison to CRC-MOSFET. In addition, the influence of ambient temperature (150–300 K) along with trap charges on TGRC-MOSFET has also been explored with an aim to analyze at which temperature of the device is more stable in the presence of interface defects (trap charges). Results obtained reveal that TGRC shows improved device performance at low temperature with trap charges being less influenced. Thus, this paper demonstrates that TGRC MOSFET can act as a promising candidate for low-power linear analog applications, where low temperature is required.**

***Index Terms*— Conventional recesses channel (CRC)-MOSFET, interface trap charges, indium tin oxide (ITO), temperature, transparent gate recessed channel (TGRC)-MOSFET.**

I. Introduction

TODAY, most of the IC applications are based on CMOS technology and subsequently it goes to subnanometer node technology to enhance its performance in terms of density, speediness, lower power ingesting, and cost. From past few years, the high interest has been rising on device reliability as it is always a major issue. This paper discusses the reliability issues by considering the defects/impurities arise due to oxide charges. During fabrication processes, various types of charges or traps being carelessly incorporated into the oxide, and thus degrades the performance of the device [1]. Four different types of trap charges are present in the thermally grown oxide, i.e., 1) interface trapped charges; 2) field oxide charges; 3) mobile ionic charge; and 4) oxide trapped charge. Among them, the most important one to study is the interface trap charges owing to the wide-ranging and degrading effect on device characteristics. These charges are due to the electronic energy-levels situated at the interface of Si/SiO_2 with energy states in the Si band gap that can change their charge state by capturing or emitting electrons (or holes). These electrons arise owing to incomplete bonds (dangling), adsorption of extraneous impurity atoms at the silicon surface, and other defects, such as lattice mismatch at the interface, which is triggered by either radiation or bond-breaking processes [2]–[5]. These charges are also known as surface states or interface states (or traps) and the position of Fermi level decides the occupancy of interface trap charges under equilibrium state. In contrast to conduction and valence bands, the interface trap charges have energy level situated in the forbidden gap. The trap charges (both electrons and holes) are present in this gap and cannot move quickly due to large space between the interfacial trivalent silicon atoms. The energy level of an acceptor interface trap charge (or negative trap charges) lies above the valence band and below Fermi energy level, while the energy level of donor interface trap charge (or positive trap charges) lies below the conduction band and above the Fermi energy level [1]. Moreover, the trap density is very subtle to even small process variation, which subsequently leads to mobility and threshold voltage degradation, and thus results in a decrement in device transconductance. Hence, there is essential to examine the consequence of these trap charges on the analog behavior of the device.

From past few years, various innovative MOS structures and gate materials have been emerged to overcome the scaling limitations, i.e., short-channel effects (SCEs). It has been found that trench gate (recessed channel) MOSFET prominently overcome the SCEs [6] and also it is one of the promising planar structure as it is extending the scaling limit of conventional MOSFET. However, its carrier transport efficiency is limited by two potential barriers created at two corners due to which carriers need more energy to cross these high barriers, and thus limits the current driving capability. Thus, In_2Sn_5O

Manuscript received December 4, 2017; accepted January 10, 2018. Date of publication January 31, 2018; date of current version February 22, 2018. This work was supported by the University Grants Commission. The work of A. Kumar was supported in part by the Delhi Technological and University Grants Commission. The review of this paper was arranged by Editor W. Tsai. *(Corresponding author: Rishu Chaujar.)*

The authors are with the Electrical Engineering Department, Delhi Technological University, New Delhi 110042, India, and also with the Applied Physics Department, Delhi Technological University, New Delhi 110042, India (e-mail: ajaykumar@dtu.ac.in; mmtripathi@dce.ac.in; chaujar.rishu@dtu.ac.in).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2018.2793853

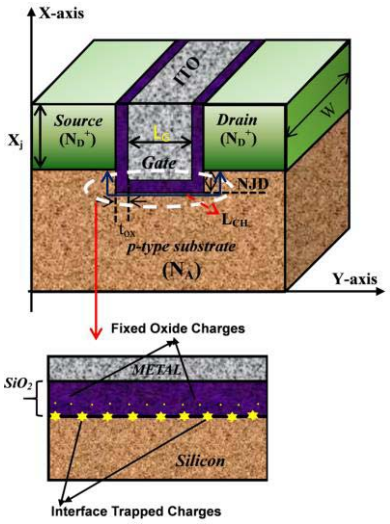


Fig. 1. Device design of TGRC-MOSFET (3-D device) with interface traps charges.

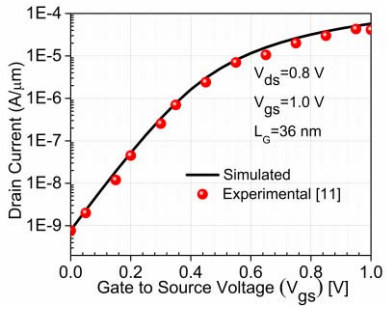


Fig. 2. Calibrated transfer characteristics of recessed channel MOSFET (36-nm gate length) with experimental and simulation data.

(indium–tin oxide) is used as gate material instead of conventional metal gate owing to its high conductivity, thermal stability, cost, and durability [7]–[9].

In this paper for the first time, the reliability issues of indium tin oxide (ITO) gate recessed channel MOSFET in the presence of uniform interface trap charges has been examined. In addition, the influence of low temperature (150–300 K) is also studied to find out at which temperature the device shows improved reliability in the presence of defects.

II. Device Design and It's Description

Fig. 1 shows the schematic 3-D view of transparent gate recessed channel (TGRC)-MOSFET consists of interfaced trap charges at the Si/SiO_2 interface. The gate length (L_G) is 30 nm while channel length (L_{CH}) is 54 nm [$L_G + 2t_{ox} + 2$ negative junction depth (NJD)], oxide thickness (t_{ox}) = 2 nm, NJD = 10 nm, and groove depth = 38 nm, for both devices [conventional recesses channel (CRC)- and TGRC-MOSFETs]. The source/drain region is heavily n+-doped (5×10^{20} cm^{-3}) whereas channel is p-doped (1×10^{17} cm^{-3}) for both CRC- and TGRC-MOSFETs. The gate material which plays a role in determining the current driving capability of MOSFET is taken In_2O_5Sn in the proposed device (TGRC-MOSFET) having workfunction of 4.7 eV, whereas, in CRC-MOSFET, aluminum (4.4 eV) is used as gate metal.

III. Simulation Methodology and Calibration

ATLAS is a powerful simulation tool, which is used for the extracting of reliability results and all figure of merits (FOMs) [10]. Various simulation models have been used, such as the Lombardi CVT model is used to consider all the mobilities such as scattering mechanism that is caused by the parallel and perpendicular fields applied on the device. For carrier generation-recombination, we have used Shockley–Read–Hall (SRH) recombination. Fermi–Dirac statistics is used in the case of very highly doped material. In order to consider the information about the low energy (temperature) of the carriers, we have used energy balance transport model [10]. The calibration of physical model parameters of the simulated device with the experimental results, by Appenzeller *et al.* in 2002 [11], is shown in Fig. 2. So as to validate the simulations results, the statistics have been drawn-out [11] for 36-nm groove MOSFET and then plotted as evident in Fig. 2. It is detected from Fig. 2 that simulated results almost matched with the experimental results in sub-40-nm groove MOSFET thus validating the simulation models. In this analysis, the value of trap charge density at the interface is chosen $1e^{12}$ cm^{-2} with uniform profiles according to previously published work [12], [13].

To explore the effect of trap charges on the subnanometer device, the total gate length is considered as the damaged region due to the high field in the channel region owing to scaling.

IV. Results and Discussion

There are many parameters which influence the performance of a MOSFET. In this section, reliability is examined and calculated in terms of analog and linearity FOMs. In addition, the effect of low temperature is explored on reliability issues of TGRC-MOSFET in the presence of trap charges (i.e., defects).

A. Impact of Interface Trap Charges on Analog Performance

Trap charges (both positive and negative) present beneath the Si/SiO_2 region are responsible for the change in flat-band voltage, and it is given by [12]

$$\Delta V_{\text{fb}} = \frac{qN_f}{C_{\text{ox}}} \tag{1}$$

where ΔV_{fb} is the change in flat-band voltage, N_f is the charge density, and C_{ox} is gate oxide capacitance. Fig. 3(a) shows the impact of interface trap charges (positive and negative) on the surface potential along the channel.

The trap charges are considered along with the entire gate length (L_G), and it is revealed from the figure that, the positive trap charges (donor type) enhances the potential while negative trap charges (acceptor type) reduces the potential in TGRC- and CRC-MOSFETs. This enhancement (reduction) in

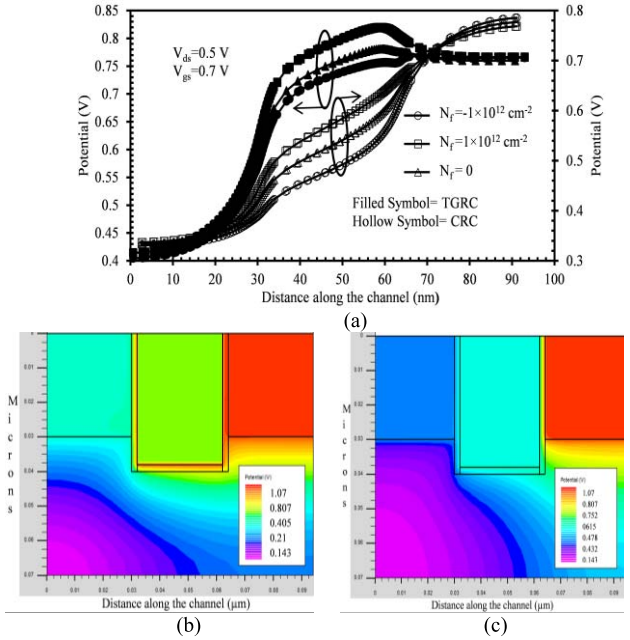


Fig. 3. (a) Potential with respect to the distance along the channel for CRC- and TGRC-MOSFETs. (b) Contour plot CRC-MOSFET with the impact of positive interface trap charge. (c) Contour plot TGRC-MOSFET with the impact of positive interface trap charge.

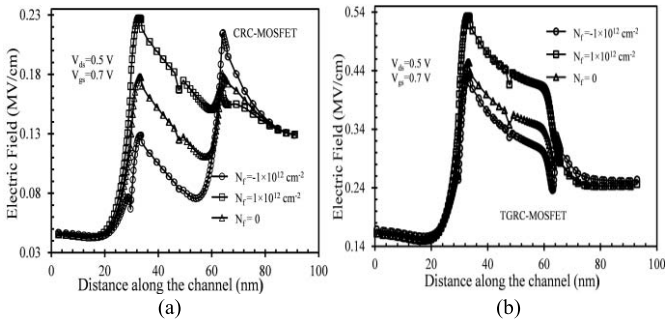


Fig. 4. Electric field distribution along the channel for (a) CRC-MOSFET and (b) TGRC-MOSFET.

potential is due to lowering (rising) of flat-band voltage which increases (decreases) the gate control over the channel and thus the surface potential. It is also found that surface potential enhances significantly in TGRC-MOSFET in comparison to CRC-MOSFET owing to the high conductivity of transparent gate as clearly reflected through 2-D contour plots shown in Fig. 3(b) and (c). It is observed from Fig. 4(a) and (b) that electric field in the channel region enhances appreciably in TGRC-MOSFET due to high surface potential in the channel region and owing to transparent gate metal having higher workfunction in comparison to the aluminum metal gate. Electric field near the drain end reduces and enhances near the source side as compared with CRC-MOSFET. The presence of positive (negative) trap charges increases (decreases) the electric field near the source end in comparison to drain end, owing to the creation of more (less) charges in the channel region, and thus leads to more (less) number of charge carriers being flow. However, from Figs. 3 and 4, it is clearly observed that the influence of trap charges is less pronounced in TGRC in comparison with CRC-MOSFET.

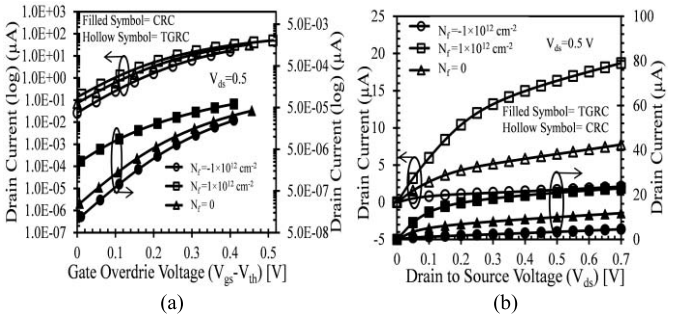


Fig. 5. (a) Transfer characteristics with respect to V_{gs} and (b) output characteristics with respect to V_{ds}, for CRC- and TGRC-MOSFETs.

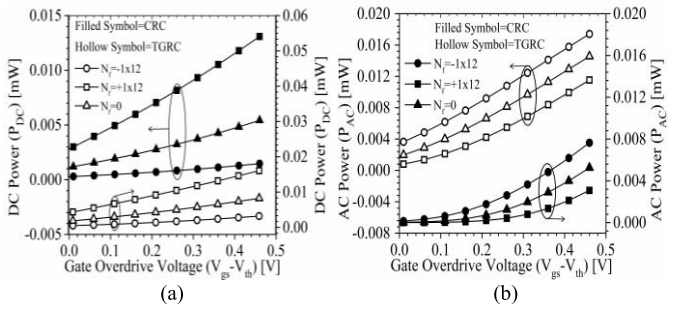


Fig. 6. (a) dc power (P_{dc}) and (b) ac power (P_{ac}) with respect to V_{gs}, for CRC- and TGRC MOSFETs.

The impact of trap charges on transfer characteristics (I_{ds}–V_{gs}) and output characteristics is also examined. Fig. 5(a) and (b) indicates that the effect of trap charges is more prominent in the subthreshold region than linear region. It is found that in the presence of positive (negative) trap charges, drain current increases (decreases) owing to high (low) field at the source end, and enhance (reduce) gate control. However, TGRC indicates nearly insignificant change in ON-current due to interface traps/damage region when it worked in inversion region.

Electrical power is the "rate" at which energy is being consumed in a circuit. The impact of interface trap charges on the low-power performance parameter, such as P_{dc} (dc power) and P_{ac} (ac power), has also been evaluated using the following:

$$P_{DC} = V_{DC} \times I_{DC} \tag{2}$$

$$P_{AC} = V_{rms} \times I_{rms}. \tag{3}$$

It is found that dc power starts increasing with increase in gate overdrive voltage and its value is numerically smaller in TGRC-MOSFET in comparison to CRC-MOSFET, as evidently shown from Fig. 6(a). Moreover, it is also observed that the effect of trap charges in TGRC-MOSFET shows lesser impact on dc power in comparison to CRC-MOSFET. This improvement is due to lower OFF-current and improved current driving capability. In addition, ac power is also studied and is found that ac power in TGRC-MOSFET is more immune to interface trap charges in comparison to CRC-MOSFET, as shown in Fig. 6(b). Thus, it can be concluded that in the presence of trap charges, TGRC-MOSFET will be suitable for low-power applications.

TABLE I
P_{AC} VARIATION WITH L_G

Gate length (L_G) (nm)	20	30	40
P_{AC} (mW)	0.01325	0.015	0.018

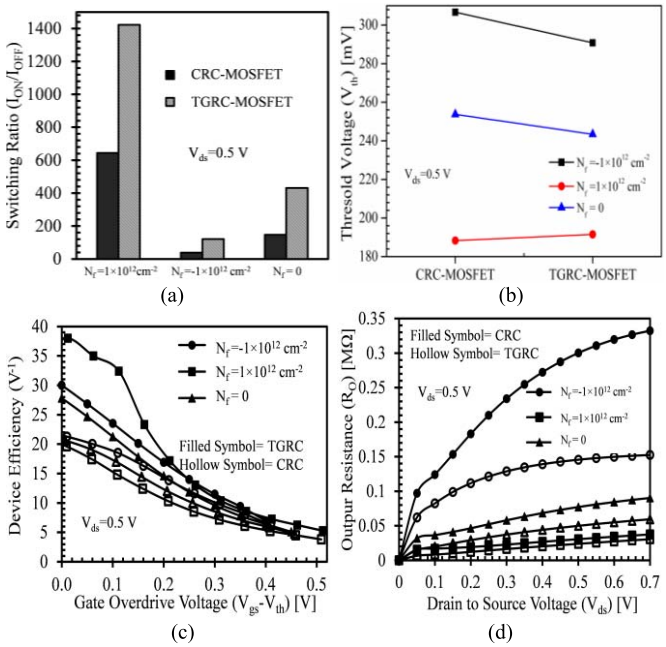


Fig. 7. Effect of interface trap charges on (a) switching ratio, (b) threshold voltage, (c) device efficiency, and (d) output resistance, for CRC- and TGRC MOSFETs.

Furthermore, it is also analyzed that with the tuning of TGRC's parameters, such as L_G(from 40 to 20 nm) and NJD (from 15 to 5 nm), its linearity performance enhances appreciably [14] while power (P_{ac}) degrades, as clearly reflected in Table I. Therefore, depending on the application, we may utilize the tradeoff between improved linearity or improved P_{ac} at a given device feature size.

Moreover, due to enhancement in drain current, switching ratio (I_{ON}/I_{OFF}) of TGRC enriches significantly as evident from Fig. 7(a) and it is calculated by the ratio of current at $V_{gs} = 0.7$ V (I_{ON}) and $V_{gs} = 0$ V (I_{OFF}). In TGRC, the ratio is enhanced by 125%, 128%, and 166% for positive, negative, and neutral trap charges, respectively, as compared with CRC device, shown in Fig. 7(a). However, CRC-MOSFET shows a more significant influence of interface traps charges for switching ratio than TGRC-MOSFET. In addition, the threshold voltage (V_{th}) which is a significant parameter for analog applications, also improves in TGRC-MOSFET in comparison to CRC-MOSFET, as shown in Fig. 7(b). This improvement is due to reduced leakage current owing to the transparent gate, which results in reduced SCEs (hot-carrier and drain induced barrier lowering) [15].

V_{th} is also affected by trap charges, as reflected in Fig. 7(b), but the effect is more in CRC in comparison to TGRC due to less change in flat-band voltage. Influence of trap charges on transconductance to the current ratio (g_m/I_d) or device efficiency and output resistance have also been analyzed for both devices, as shown in Fig. 7(c) and (d). In the design of analog circuits, device efficiency is a vital factor, which offers the measure of effectiveness to convert power into speed. It is evident from Fig. 7(c) that the device efficiency is higher (lower) in TGRC-MOSFET when positive (negative) trap charges are present in comparison to CRC-MOSFET. It is also observed in Fig. 7(c) that the impact of interface trap charges on device efficiency is less prominent in TGRC, and thus signify superior efficiency in TGRC than CRC. The output resistance (R_o) is the transposed of the output conductance in a MOSFET and for high performance; R_o should be as small as possible. When positive (negative) trap charges have been taken into consideration, R_o is very less (high) while it is less prominent for negative and neutral trap charges in TGRC-MOSFET as compared with conventional counterpart, as shown in Fig. 7(d). Thus, recessed channel MOSFET with transparent gate material (ITO) shows reliable performance in the presence of interface trap charges as compared with CRC device.

B. Impact of Interface Trap Charges on Linearity and Distortion Performance

High linearity and lower intermodulation distortions (IMDs) are essential requirements for a CMOS device when working with weak signals. Nonlinearity introduces IMD and generates an undesired distorted signal in the output of different frequency signals compared with an input signal, which results in degradation in device behavior [16]. For that reason, in this subsection, the influence of interface trap charges on linearity and IMD of TGRC device are studied and results obtained are simultaneously compared with CRC-MOSFET. The performance metrics used in this analysis are g_{m3} (higher order transconductance coefficient), third-order voltage intercept point (VIP3), third-order current intercept point (IIP3), third-order IMD (IMD3), and second- and third-order harmonic distortions (HD2 and HD3). To assure higher linearity, higher order transconductance coefficient (g_{m3}) must be minimal.

From the dc parameters, VIP3 is used to evaluate the distortion characteristics. IIP3 and VIP3 should be high, but IMD3 and HD3 should be low for lower distortion. The device linearity FOMs are evaluated, as shown in (4)–(7) [17]

$$\text{VIP3} = \sqrt{24 \times g_{m1}/g_{m3}} \tag{4}$$

where $g_{m1} = (\partial I_d/\partial V_{gs})$ and $g_{m2} = (\partial^2 I_d/\partial V_{gs}^2)$. $g_{m3} = (\partial^3 I_d/\partial V_{gs}^3)$

$$\text{IIP3} = \frac{2}{3}\frac{g_{m1}}{g_{m3} \times Rs} \tag{5}$$

where $R_S = 50\ \Omega$ for analog and RF applications

$$\text{IMD3} = \left(\frac{9}{2} \times (VIP3)^3 \times g_{m3}\right)^2 \times R_S \tag{6}$$

$$\text{HD2} = 0.5V_a\frac{\left(\frac{dg_{m1}}{dV_{GT}}\right)}{2g_{m1}} \tag{7}$$

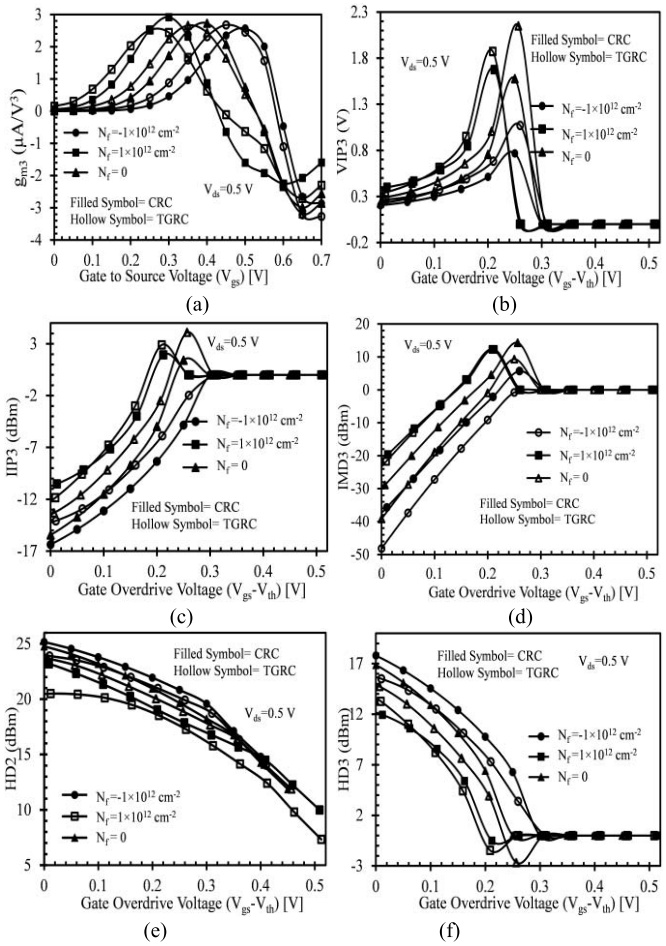


Fig. 8. Effect of interface trap charges on (a) g_{m3}, (b) VIP3, (c) IIP3, (d) IMD3, (e) HD2, and (f) HD3, for CRC- and TGRC MOSFETs.

$$\mathrm{HD3} = 0.25V_a^2 \frac{\left(\frac{d^2 g_{m1}}{dV_{GT}^2}\right)}{6g_{m1}} \tag{8}$$

where $R_S = 50\ \Omega$ for analog and RF applications. V_a is the amplitude of ac signal and considered about 50 mV (which is minuscule) for integral function method (IFM) analysis.

Ideally, g_{m3} should be as low as possible because g_{m3} decides the dc bias point for optimal device operation and determines the limits on the distortion. Fig. 8(a) illustrates the variation of g_{m3} with respect to V_{gs} for damaged (positive and negative traps) and undamaged region. g_{m3} is a higher order derivative of transfer characteristics and it is observed that g_{m3} reduces (enhances) in case of TGRC in the presence of positive (negative) trap charges although this variation is very less in comparison to CRC-MOSFET. This is due to less dependence on trap charges on transfer characteristics and transconductance, which reflects TGRC, is more reliable in the presence of interface trap charges/damage. Fig. 8(b) and (c) reflects the influence of interface trap charges on VIP3 and IIP3, respectively. For low distortion and high linearity, the peak value of IIP3 and VIP3 should be high. VIP3 signifies extrapolated input voltage at which first- and third-order harmonics of drain current are equal and expressed as in (4), while IIP3 is a theoretical point at which the third-order distortion signal amplitudes equal the input signals, and it is useful in determining the linearity condition of an amplifier [18]. The amplitude of VIP3 and IIP3 is high for TGRC-MOSFET as compared with CRC-MOSFET, and it also implies that the damaged device (in the presence of trap charges) shows less linearity in comparison with the undamaged device, but TGRC architecture shows better linearity and less distortion in comparison to CRC-MOSFET. This is due to the higher conductivity of ITO as compared with the metal gate that enhances current driving capability [19], and thus improves linearity performance in the presence of interface traps. In addition, IMD3, HD2, and HD3 are major issues in linear amplifiers that arise owing to the nonlinearity performance of the device [18] and stated in (6)–(8). IMD3 represents the intermodulation current at which the first- and third-order intermodulation harmonic currents are the same. IMD3 is analyzed considering the influence of interface trap charges on TGRC device. IFM is used for the calculation of the distortion since this approach authorizations for the extraction of distortion from dc measurements deprived of an ac characterization, dissimilar to Fourier-based methods [20], [21] as shown in (6)–(8). The output conductance of TGRC is negligible. Hence, the device gains are improved [22], [23]. Fig. 8(d) reveals that IMD3 reduces in TGRC-MOSFET owing to the reduced g_{m3} value in comparison to VIP3, which dominates the value of IMD3 [Fig. 8(a)] as compared with CRC-MOSFET. Meanwhile, it is also observed that TGRC reduces (increase) HD2 and HD3 when positive (negative) trap charges are considered and exhibit the very less effect of traps charges as compared with its conventional counterpart, as shown in Fig. 8(e) and (f). Thus, TGRC exhibits improved linearity and distortion-less performance for ultra large scale integration (ULSI) in the presence of interface trap charges.

C. Effect of Interface Trap Charges at Low Temperature on Analog, Linearity, and Intermodulation Distortion

This subsection describes the effect of temperature on the above-mentioned parameters for TGRC-MOSFET in the occurrence of interface trap charges to analyze the reliability of TGRC-MOSFET at low temperatures (150–300 K). Electrical behavior of CMOS devices changes with change in temperature. As the temperature increases, the carrier mobility [24] decreases as

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-n} \tag{9}$$

where "n" is an exponent, which varies from 1.6 to 2.4 [25]. If mobility is decreased, then the output current also reduces, and hence with the increase in temperature, switching ratio decreases, as shown in Fig. 9(a). Moreover, change in ambient temperature also influences the traps charges created during the fabrication process. It is found that in the presence of positive (negative) trap charges, the number of charge carriers increased (decrease), due to which mobility reduced (enhance) and hence switching ratio and output resistance (inset) reduced (improves), as evident from Fig. 9(a). Furthermore, the threshold voltage (V_{th}) of the MOSFET is inversely proportional to the temperature [26] and it increases at low temperature due

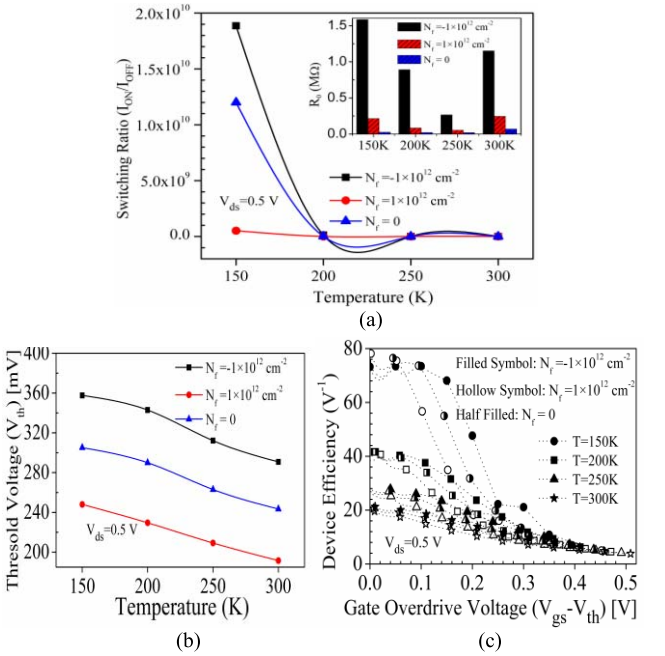


Fig. 9. Effect of temperature on (a) switching ratio, inset: output resistance, (b) threshold voltage, and (c) device efficiency, in TGRC-MOSFET with interface trap charge density.

to the rise in Fermi potential (ϕ_F) and depletion charges [27]. In the absence of trap charges V_{th} is 0.243 V at room temperature. Fig. 9(b) shows the variation of the threshold voltage, and it is observed that as the temperature rises from 150 to 300 K, V_{th} reduced and it is higher (lower) for negative (positive) trap charges due to the change in flat-band voltage and mobility. Besides, both mobility and threshold voltage also influenced the drain to source current I_{ds} [28] as

$$I_{\text{ds}}(T) \propto \mu(T)[V_{\text{gs}} - V_{\text{th}}(T)] \tag{10}$$

Fig. 9(c) illustrates the higher device efficiency at a lower temperature, and in the presence of positive (negative) trap charges, device efficiency is more (less) with respect to neutral trap charges. Hence, TGRC-MOSFET shows better performance at low temperature owing to reduced fluctuations. Fig. 10(a) shows higher order transconductance (g_{m3}) as a function of the gate to source voltage for different ambient temperatures in the presence of positive (donor), and negative (acceptor) interface trap charges. At $T = 150$ K, positive (negative) trap charges exhibit low (high) distortion owing to improved transconductance. Furthermore, at high temperature (>150 K), distortion is increased (low peaks are observed in g_{m3}). Fig. 10(b) and (c) reflects the improved performance of TGRC-MOSFET at a lower temperature (<300 K) in terms of VIP3 and IIP3, respectively, in the presence of trap charges. It is found that peak value of VIP3 and IIP3 is enhancing at a low temperature which indicates less distortion and high linearity, when the device is working at low temperature. Besides, it is also observed that impact of interface trap charges on TGRC's linearity performance at low temperature is less prominent, as clearly indicated from Fig.10(b) and (c). Thus, TGRC-MOSFET acts as a potential candidate for linear amplifiers working at low temperatures in CMOS ULSI. Harmonic distortion is an essential reliability issue which

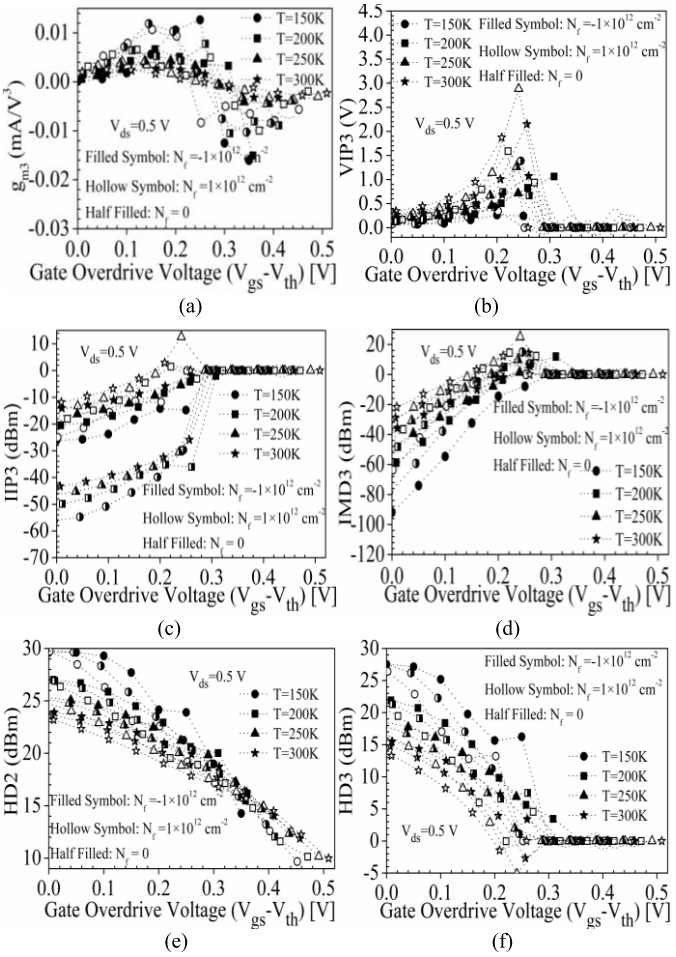


Fig. 10. Effect of temperature with interface trap charges on (a) g_{m3}, (b) VIP3, (c) IIP3, (d) IMD3, (e) HD2, and (f) HD3 in TGRC-MOSFET.

arises due to the nonlinear performance of MOSFET. Thus, HD in terms of IMD3, HD2, and HD3 are examined as a function of both temperature and interface trap charges and are illustrated in Fig. 10(d)–(f), respectively. Change in ambient temperature plays a major role in amplifiers working in communication systems and sometimes it causes an undesirable change in signals and thus causes distortion in the band of interest. This is due to the random motion of electrons which results in thermal noise within the device, and thus degrades the device performance. At low temperatures (<300 K), harmonic distortions (IMD3, HD2, and HD3) are reduced in TGRC-MOSFET, as evident from Fig. 10 (d)–(f). It is also observed that in the presence of positive (negative) trap charges, g_{m3} lowers (increase) owing to improved (reduce) current driving capability, and thus lowers (rise) the distortion. This effect is more at low temperatures in TGRC due to enhancement in transconductance and reduction in g_{m3} [see Fig. 10(a)].

V. Conclusion

This paper studies the influence of interface trap charges on the static, linearity, and distortion FOMs to explore the reliability issues of TGRC-MOSFET. The performance of this device has also been compared with CRC-MOSFET through extensive device simulation. The proposed device is

suitable for high switching applications even in the presence of trap charges. It has been shown that the TGRC-MOSFET exhibits superior current driving capability, and high linearity (VIP3 and IIP3) with low distortions. It has also been observed that TGRC-MOSFET is more immune to interface trap charges than CRC-MOSFET. Likewise, it is also found that TGRC-MOSFET at low temperature (150 K) in the presence of interface trap charges show negligible variation in device behavior in terms of I_{ds}, g_m, VIP3, IIP3, HD2, HD3, and IMD3. Thus, the TGRC-MOSFET is more reliable at low temperatures and serves as a promising candidate for analog and low-power high-linearity applications.

REFERENCES

[1] N. D. Arora, *MOSFET Models for VLSI Circuit Simulation: Theory and Practice*. New York, NY, USA: Springer, 1993.

[2] H. Jo, S. Choi, S. Rhee, and Y. J. Park, "An analytical model for the threshold voltage of intrinsic channel MOSFET having bulk trap charges," *IEEE Trans. Electron Devices*, vol. 64, no. 5, pp. 2113–2120, May 2017.

[3] Y. H. Lho and K. Y. Kim, "Radiation effects on the power MOSFET for space applications," *ETRI J.*, vol. 27, no. 4, pp. 449–452, 2005.

[4] L. Trabzon and O. O. Awadelkarim, "Damage to n-MOSFETs from electrical stress relationship to processing damage and impact on device reliability," *Microelectron. Rel.*, vol. 38, no. 4, pp. 651–657, 1998.

[5] E. H. Poindexter, "MOS interface states: Overview and physicochemical perspective," *Semicond. Sci. Technol.*, vol. 4, no. 12, p. 961, 1989.

[6] S. Veeraraghavan and J. G. Fossum, "Short-channel effects in SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 36, no. 3, pp. 522–528, Mar. 1989.

[7] R. G. Gordon, "Criteria for choosing transparent conductors," *MRS Bull.*, vol. 25, pp. 52–57, Aug. 2000.

[8] V. Singh, C. K. Suman, and S. Kumar, "Indium Tin Oxide (ITO) films on flexible substrates for organic light emitting diodes," in *Proc. ASID*, 2006, pp. 388–391.

[9] R. Murali and J. D. Meindl, "Modeling the effect of source/drain junction depth on bulk-MOSFET scaling," *Solid-State Electron.*, vol. 51, no. 6, pp. 823–827, 2007.

[10] *ATLAS User's Manual*, SILVACO, Santa Clara, CA, USA, 2011.

[11] J. Appenzeller *et al.*, "Sub-40 nm SOI V-groove n-MOSFETs," *IEEE Electron Device Lett.*, vol. 23, no. 2, pp. 100–102, Feb. 2002.

[12] T.-K. Chiang, "A compact model for threshold voltage of surrounding-gate MOSFETs with localized interface trapped charges," *IEEE Trans. Electron Devices*, vol. 58, no. 2, pp. 567–571, Feb. 2011.

[13] S. Shabde, A. Bhattacharyya, R. S. Kao, and R. S. Müller, "Analysis of MOSFET degradation due to hot-electron stress in terms of interface-state and fixed-charge generation," *Solid-State Electron.*, vol. 31, no. 11, pp. 1603–1610, 1988.

[14] A. Kumar, "Effect of trench depth and gate length shrinking assessment on the analog and linearity performance of TGRC-MOSFET," *Superlattices Microstruct.*, vol. 109, pp. 626–640, Sep. 2017.

[15] A. Kumar, N. Gupta, and R. Chaujar, "Analysis of novel transparent gate recessed channel (TGRC) MOSFET for improved analog behaviour," *Microsyst. Technol.*, vol. 22, no. 11, pp. 2665–2671, 2016.

[16] B. Razavi and R. Behzad, *RF Microelectronics*, vol. 1. Englewood Cliffs, NJ, USA: Prentice-Hall, 1998.

[17] R. Chaujar, R. Kaur, M. Saxena, M. Gupta, and R. S. Gupta, "TCAD assessment of Gate Electrode Workfunction Engineered Recessed Channel (GEWE-RC) MOSFET and its multi-layered gate architecture, Part II: Analog and large signal performance evaluation," *Superlattices Microstruct.*, vol. 46, no. 4, pp. 645–655, 2009.

[18] N. Gupta and R. Chaujar, "Optimization of high-k and gate metal workfunction for improved analog and intermodulation performance of Gate Stack (GS)-GEWE-SiNW MOSFET," *Superlattices Microstruct.*, vol. 97, pp. 630–641, Sep. 2016.

[19] A. Kumar, M. M. Tripathi, and R. Chaujar, "Investigation of parasitic capacitances of In_2O_5Sn gate electrode recessed channel MOSFET for ULSI switching applications," *Microsyst. Technol.*, vol. 23, no. 12, pp. 5867–5874, 2017.

[20] A. Cerdeira, M. A. Alemán, M. Estrada, and D. Flandre, "Integral function method for determination of nonlinear harmonic distortion," *Solid-State Electron.*, vol. 48, no. 12, pp. 2225–2234, 2004.

[21] R. T. Doria, A. Cerdeira, J.-P. Raskin, D. Flandre, and M. A. Pavanello, "Harmonic distortion analysis of double gate graded-channel MOSFETs operating in saturation," *Microelectron. J.*, vol. 39, no. 12, pp. 1663–1670, 2008.

[22] A. Kumar, N. Gupta, and R. Chaujar, "Power gain assessment of ITO based Transparent Gate Recessed Channel (TGRC) MOSFET for RF/wireless applications," *Superlattices Microstruct.*, vol. 91, pp. 290–301, Mar. 2016.

[23] R. van Langevelde and F. M. Klaassen, "Accurate drain conductance modeling for distortion analysis in MOSFETs," in *IEDM Tech. Dig.*, Dec. 1997, pp. 313–316.

[24] R. van Langevelde and F. M. Klaassen, "Effect of gate-field dependent mobility degradation on distortion analysis in MOSFETs," *IEEE Trans. Electron Devices*, vol. 44, no. 11, pp. 2044–2052, Nov. 1997.

[25] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*. New York, NY, USA: Wiley, 2006.

[26] G. Groeseneken, J. Colinge, H. E. Maes, J. C. Alderman, and S. Holt, "Temperature dependence of threshold voltage in thin-film SOI MOSFETs," *IEEE Electron Device Lett.*, vol. 11, no. 8, pp. 329–331, Aug. 1990.

[27] T. Elewa *et al.*, "Performance and physical mechanisms in SIMOX MOS transistors operated at very low temperature," *IEEE Trans. Electron Devices*, vol. 37, no. 4, pp. 1007–1019, Apr. 1990.

[28] N. Gupta and R. Chaujar, "Investigation of temperature variations on analog/RF and linearity performance of stacked gate GEWE-SiNW MOSFET for improved device reliability," *Microelectron. Rel.*, vol. 64, pp. 235–241, Sep. 2016.

Ajay Kumar (S'15) received the B.Tech. degree in electronics and communication from Uttar Pradesh Technical University, Lucknow, India, in 2009, and the M.Tech. degree in nanoscience and technology from Delhi Technological University, New Delhi, India, in 2014, where he is currently pursuing the Ph.D. degree with Electrical Engineering Department.

M. M. Tripathi (SM'16) received the B.Tech. degree from the Madan Mohan Malaviya Engineering College, Gorakhpur, India, in 1994, and the Ph.D. degree from Gautam Buddh Technical University, Lucknow, India, in 2010.

He is currently a Professor with the Electrical Engineering Department, Delhi Technological University, New Delhi, India.

Rishu Chaujar (SM'16) received the B.Sc. (H), M.Sc., and Ph.D. degrees in electronics from the University of Delhi, New Delhi, India, in 2003, 2005, 2009 respectively.

She is currently an Assistant Professor with the Department of Applied Physics, Delhi Technological University, New Delhi.

Radiation Analysis of N-Channel TGRC-MOSFET: An X-Ray Dosimeter

Ajay Kumar, *Student Member, IEEE*, Balark Tiwari, Samarth Singh, Madan Mohan Tripathi, *Senior Member, IEEE*, and Rishu Chaujar, *Senior Member, IEEE*

***Abstract*— This paper reports the response of an N-channel transparent gate recessed channel (TGRC) metal–oxide–semiconductor field-effect transistor (MOSFET) to X-ray radiation in the 0.5-k–10-krad dose range after irradiation. TCAD simulations for the same have been done to estimate the threshold voltage shift in MOSFET with different radiation dosages. Models accounting for electron–hole pair generation and recombination are applied along with the trap/detrap model for an insulator as well as interface charging. An improvement of 1.11 mV/krad in radiation sensitivity has been found in increasing the oxide thickness from 2 to 6 nm. The results suggest that TGRC-MOSFET can be effectively used as an X-ray dosimeter in the sub-30-nm scale. Along with a signal amplification and processing circuit, this device can find an enormous applicability in clinical and space environments.**

***Index Terms*— Dose, dosimeter, radiation, total ionizing dose (TID), transparent gate recessed channel (TGRC) metal–oxide–semiconductor field-effect transistor (MOSFET).**

I. Introduction

METAL–OXIDE–SEMICONDUCTOR field-effect transistors (MOSFETs) are excessively used in radiation rich environments, such as space and military. When electronic circuits are exposed to various radiation environments, it becomes critical to define the behavior of the circuit undergoing irradiation. Various effects such as single-event burnout, single-event gate rupture, insulator charging, and interface charging degrade the circuit performance and sometimes completely damage the device [1]. To ensure safety and stability of such circuits in a harsh radiation environment, the incoming dose must be monitored to initiate specific repairs or replacement. In medical applications [2], an X-ray dose which is intended to kill cancerous cells will probably cause damage to normal tissue, to minimize this damage, extremely precise dose adjustments are required which are facilitated if the sensor can be placed close to the site receiving radiation. MOSFET dosimeters are used to determine total dose absorbed due to their valuable property of linear dependence of the threshold voltage on total ionizing dose (TID) over a finite range of doses.

Transparent gate recessed channel (TGRC) MOSFET has the ability to provide the high packing density, and hence, miniaturized sensors that are of utmost importance as exposure to an ionizing radiation has to be tightly controlled in radiotherapy, nuclear waste management, high-energy physics experiments, and space missions to avoid health or technical safety risks [3]. Moreover, the increased functionality and reduced cost of a large variety of integrated circuits and systems have brought its own benefit to the end users and above all the semiconductor industry.

Scaling of MOSFET leads to hot-carrier injection (HCI) which causes an excess of charge carriers flowing through gate oxide and thus degrades its performance, and therefore, to overcome this effect, a recessed channel structure is used with the 6-nm oxide thickness. Also, the recessed structure leads to low power dissipation which is of utmost importance for a dosimeter to show an improved sensitivity at the nano level. TGRC-MOSFET [4]–[10] is therefore preferred as it has indium tin oxide (ITO) [11] as the gate electrode allowing easier energy transfer through the gate electrode, thereby maximizing the absorbed dose leading to enhanced sensitivity and, hence, proving to be an ideal choice for a dosimeter [12], [13]. As a result of the interaction of ionizing X-ray radiation with TGRC-MOSFET, holes are trapped inside the oxide–substrate interface layer, which causes a shift in the threshold voltage [14] of the device. To predict the electrical behavior of the MOSFET device under the influence of ionizing radiation, it is necessary to determine the trapped hole density inside the oxide and energy imparted by the radiation to the material.

When high-energy photons strike the semiconductor lattice, they provide sufficient energy to generate an electron–hole pair directly or indirectly via the lattice vibrations. Generating an electron–hole pair in a SiO_2 layer requires energy, $E_p = 17 \pm 1$ eV [15]. Using this value of E_p, we are able to calculate $g_0 = 8.1 \times 10^{12}$ pairs/cm^3 $\cdot$ rad [16] which is the theoretical number of electron–hole pairs generated, but this value is greatly reduced due to the recombination process. In the semiconductor region as the mobility of electrons and holes does not differ significantly, they can recombine very easily. However, in the case of gate oxide, being an insulator, the difference in mobility is significantly large.

Manuscript received July 12, 2018; revised September 1, 2018; accepted September 6, 2018. Date of publication September 24, 2018; date of current version October 22, 2018. This work was supported by the University Grants Commission. The work of A. Kumar was supported by the Delhi Technological University. The review of this paper was arranged by Editor B. Kaczer. *(Corresponding author: Rishu Chaujar.)*

The authors are with the Electrical Engineering Department, Delhi Technological University, New Delhi 110042, India, and also with the Applied Physics Department, Delhi Technological University, New Delhi 110042, India (e-mail: ajaykumar@dtu.ac.in; balarktiwari_2k14@dtu.ac.in; samarthsingh_2k14@dtu.ac.in; mmtripathi@dce.ac.in; chaujar.rishu@dtu.ac.in).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2018.2869536

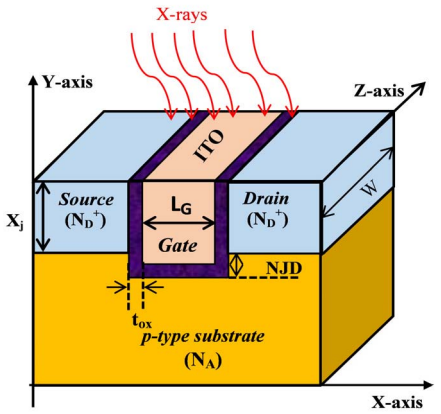


Fig. 1. Simulated device structure of TGRC-MOSFET.

TABLE I
DESIGN PARAMETERS OF TGRC-MOSFET

Parameter	Unit		
Oxide Thickness (t_{ox})	2 nm	4 nm	6nm
Source/Drain doping (N_D^+)	1×10^{19} cm^{-3}		
Substrate doping (N_A)	1×10^{16} cm^{-3}		
Gate Length (L_G)	30 nm		
Negative junction depth (NJD)	10 nm	12 nm	14 nm
Work function for TGRC-MOSFET	4.7 eV		
Permittivity of SiO_2 (ε_{ox})	3.9		
Gate to Source voltage (V_{gs})	1.5 V		
Drain to Source voltage (V_{ds})	0.05 V		

As a result, electrons move very quickly toward the gate electrode, and holes drift slowly toward the Si–SiO_2 interface and finally getting trapped there. The trapped holes at the Si–SiO_2 interface are relatively immobile causing a negative shift in the threshold voltage on the electrical characteristics of the MOSFET device. Ultimately, the shift in the threshold voltage can be used as a dosimetric parameter to evaluate an incident radiation dosage.

II. TGRC-MOSFET Device Structure

For an irradiated TGRC-MOSFET device, the threshold voltage, hole trap density, and maximum ON-current are usually the most relevant parameters. The radiation-induced changes are reported in this paper based on these parameters.

Our device consists of the transparent gate made of ITO as shown in Fig. 1 and the design parameters are given in Table I. ITO is a wide bandgap material that exhibits the special property of high optical transmittance (~90%) in the visible region of the spectrum combined with a high electrical conductivity [12]. As the radiation sensitivity is found to be dependent on the absorbed dose, ITO having high optical transmittance is expected to enhance the overall trapping of the incident radiation dose. This paper is based on the direct incident radiation for the very short duration in the simulation process. The values that are found immediately after

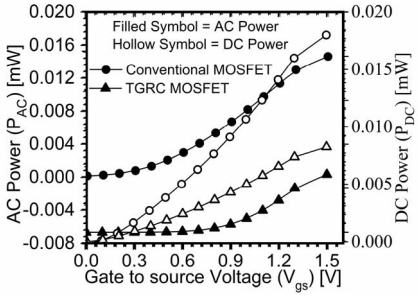


Fig. 2. AC power (P_{ac}) and dc power (P_{dc}) with respect to V_{gs} for TGRC-MOSFET and the conventional MOSFET.

irradiation and continuing irradiation for a long-time period have been avoided for the device protection. Strict constraints are applied to the device dimensions as the intended application—implantable clinical dosimeter will require an additional space for peripheral electronic components.

Moreover, the power consumption is one of the major issues for a semiconductor device. It is found that dc power starts increasing with an increase in the gate voltage and its value is smaller in TGRC-MOSFET in comparison to the conventional MOSFET as shown in Fig. 2. This improvement is due to the lower OFF-current and improved current driving capability. In addition, TGRC-MOSFET is less ac power consumed device compared to the conventional MOSFET as shown in Fig. 2. Thus, it can be concluded that TGRC-MOSFET is a low power device.

III. Simulation Methodology and Calibration

For TCAD simulations, various models have been taken into effect such as, for mobility of carriers under the influence of changing the electric field, we have included the parallel electric field dependence model that takes care of all the parameters affecting the mobility of carriers including the velocity saturation effect [17]. To predict the behavior of the device undergoing radiation, it is extremely crucial to accurately model the movement of carriers so that simulated charge trapping is almost identical to practical device undergoing irradiation. For carrier generation–recombination, we have implemented the concentration-dependent Klaassen Shockley–Read–Hall (KLASRH) Recombination model as it can include the concentration-dependent lifetime of carriers [17].

As electron–hole pair generation–recombination is a key phenomenon in predicting the behavior of MOSFET after irradiation, it can be most accurately modeled via the KLASRH model. To model the trap states of the carrier in the oxide and interface region, we have included the bound trap model as it allows us to specify the energy level requirement of trapped states.

The above-selected models account for almost the entire device physics associated with the MOSFET, thereby producing extremely accurate results.

To validate the simulation models, both the experimental [18] and modeled data [19] have been extracted and calibrated as shown in Fig. 3(a) and (b), respectively. The fabricated data [18] are extracted from a grooved gate trapezoidal-like structure of 140-nm gate length which is

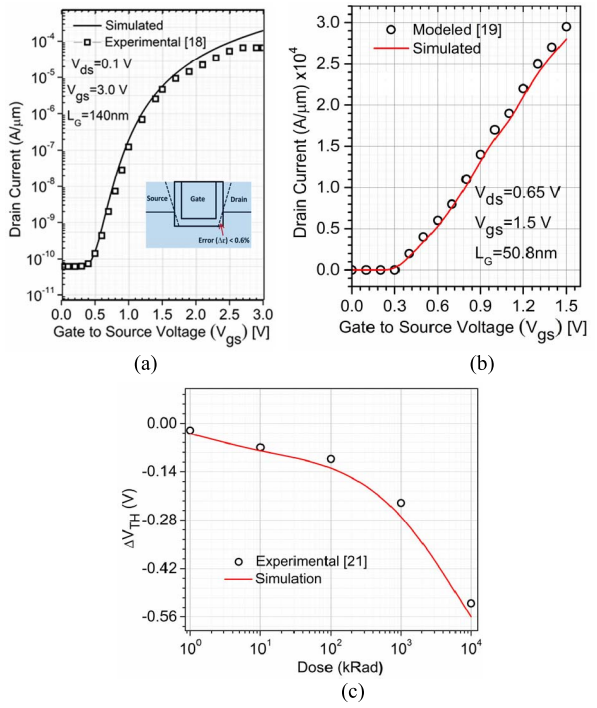


Fig. 3. (a) Experimental and simulation of I_{ds}–V_{gs} characteristics of 140-nm gate length grooved gate (recessed channel) MOSFET. (b) Modeled and simulation of I_{ds}–V_{gs} characteristics of 50.8-nm gate length recessed channel MOSFET. (c) Calibration of experimental and simulation results with shift in threshold voltage (ΔV_{TH}) under irradiation up to 10^4krad.

similar to U-groove gate. The corner effect (error) [20] $(\Delta\varepsilon/L_{\text{eff}}) < 0.6\%$, which is almost negligible as depicted in Fig. 3(a). Further to validate the results, the simulated models have also been calibrated with the modeled data [19] for 50.8-nm gate length [channel length $(L_G + 2(\text{NJD} + t_{ox})) = 85.8$ nm] which is also in good agreement as evident from Fig. 3(b), thus reflecting the validity of simulation models.

Furthermore, to show the simulation validity of radiation dose, we have compared our simulation results [shown in Fig. 3(c)] with those of experimentally obtained parameters by Berland *et al.* [21]. To compare the results, we have scaled our device dimensions similar to that of the experimental device, by changing the gate length to 20 μm and gate oxide thickness to 23 nm. In addition, the buried oxide of thickness 380 nm is introduced to match with the experimental device. Simulations for radiation dose up to 10^4 krad are done and change in the threshold voltage is compared with our device as shown in Fig. 3(c), which predicts almost similar results with a small margin of the error. Thus, it validates the accuracy of simulation models after irradiation.

IV. Fabrication Process of TGRC-MOSFET

In the process of fabrication (shown in Fig. 4), first of all, a silicon wafer (substrate) is taken, and then the diffusion process is used for the creation of n-well region. Before drive-in diffusion and gate oxidation process, the active region is identified. Source–drain implantation and anneal process are implemented before groove etching by the combination of reactive ion etching and electron beam lithography, and then

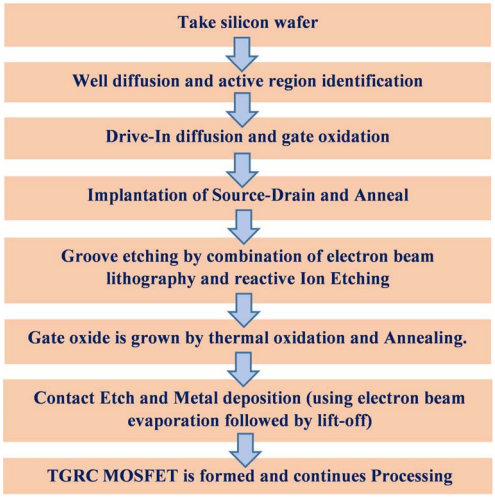


Fig. 4. Fabrication process of TGRC-MOSFET.

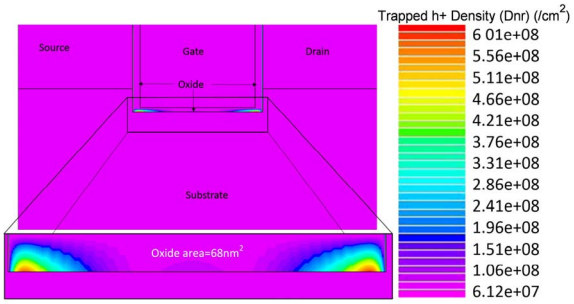


Fig. 5. Trapped hole density profile along the oxide–substrate interface, having oxide thickness 2 nm and oxide area 68 nm^2.

the gate oxide is grown by thermal oxidation at the bottom of the groove. Different oxide thicknesses will result in different channel lengths $[L_{CH} = L_G + 2(\text{NJD} + t_{ox})]$. Contact etches and metal deposition (using electron beam evaporation followed by liftoff) process is done in the last fabrication process.

Thus, the fabrication of TGRC-MOSFET can be done by using the process flow of device design schemes. The proposed device is the aids of the transparent gate engineering scheme which has been combined with the groove gate for accomplishing the improved characteristics.

V. Results and Discussion

A. Impact of X-Ray Doses

TCAD simulation of TGRC-MOSFET undergoing irradiation shows that a significant number of holes are trapped in the SiO_2 gate oxide layer and the area of gate oxide as 68 nm^2 [2 nm $\times$ (2 + 30 + 2 nm)] is considered. As depicted in Fig. 5, the trapped hole density is maximum (6×10^8cm^{-2}) near the oxide–substrate interface.

In our simulation, the maximum hole trap density is found out to be 6×10^8 (dnr/cm^2) for a TID of 10 krads. This accumulation of charge due to trapping of holes accounts for the maximum change in the electrical characteristics of the device. The overall sensitivity of the dosimeter is dependent on the trapped hole concentration in the oxide layer, and to maximize this, we needed a strong electric field inside the

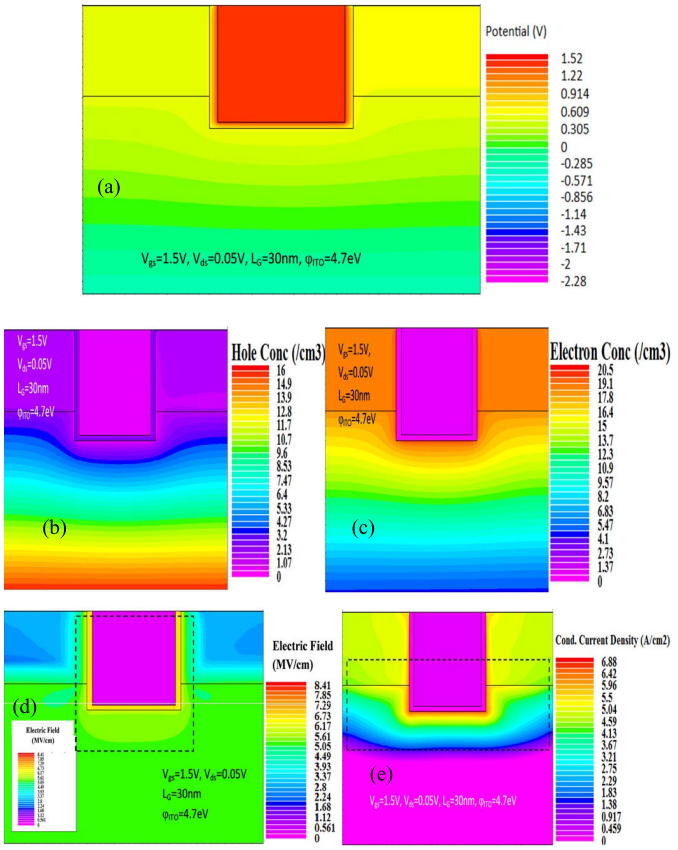


Fig. 6. Contour plots of (a) surface potential, (b) hole concentration, (c) electron concentration, (d) electric field, and (e) conduction current density on TGRC-MOSFET (t_{ox} = 2 nm) with 1000-rad X-ray dose.

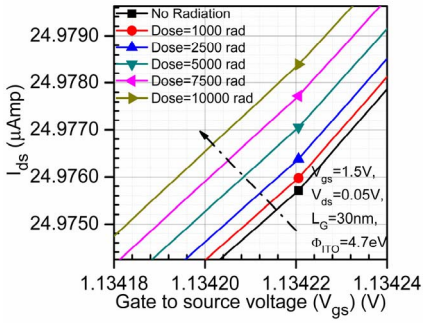


Fig. 7. Impact of an X-ray radiation damage on the current–voltage characteristics of TGRC-MOSFET at t_{ox} = 2 nm.

oxide layer which can significantly reduce the electron–hole recombination, thereby increasing the trapped hole concentration. This has been achieved with multiple simulations and with hit and trial approach, we were able to generate electric fields as high as 7 MV/cm in the oxide region as shown in Fig. 6(d) and the corresponding biasing which allowed such high field is depicted in Fig. 6(a). To illustrate the conduction channel which is formed, we have included detailed contours showing the charge carrier concentration in the device as shown in Fig. 6(b) and (c).

In TGRC-MOSFET, due to the accumulation of trapped holes near the oxide–substrate interface, there is a negative shift in the threshold voltage of the device as shown in Fig. 7. V_{TH} is obtained using the single derivative method

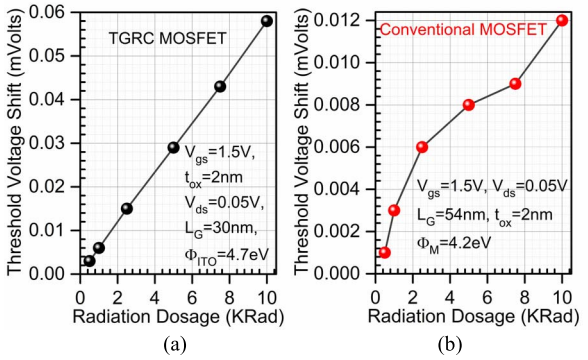


Fig. 8. Threshold voltage shift due to radiation on (a) TGRC-MOSFET and (b) conventional MOSFET.

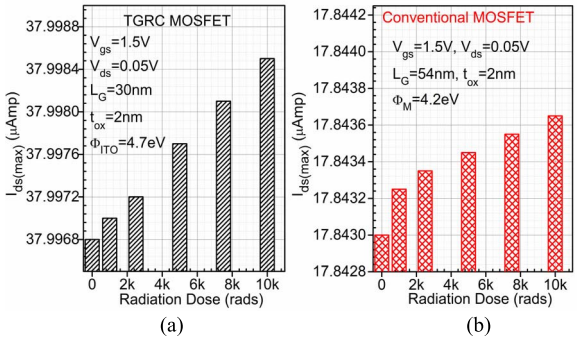


Fig. 9. Impact of radiation dose on the maximum drain-to-source current for (a) TGRC-MOSFET and (b) conventional MOSFET.

by analyzing the drain-to-source current (I_{ds}) versus gate-to-source voltage (V_{gs}) curve. The evaluated values of the threshold voltage show a linear dependence on applied radiation dose and the threshold voltage shift is negative (shown in Fig. 7). The threshold voltage shift ($|V_{TH-SHIFT}|$) has been evaluated [by $|(V_T - V_{T0})|$, where V_T is the threshold voltage after irradiation (0.5 k–10 krad) and V_{T0} is the threshold voltage without irradiation] and plotted as shown in Fig. 8. The radiation dose has been considered from 0.5 krad as in radiotherapy, daily doses could range from 50 up to 2500 rad. In some specific medical treatments such as lung cancer, specific doses are required for a specific patient and it is also more important to analyze which X-ray doses are delivered to the organs [22].

The proposed device having low operating voltages along with small drain-to-source current [Fig. 9(a)] has extremely low power consumption (see Fig. 2) which enhances the overall usage time with the limited power supply, hence increasing its applicability as an implantable dosimeter. In the conventional MOSFET, HCI leads to impact ionization which causes an excess of electrons to flow through gate oxide and thus leads to degradation in sensitivity and the maximum drain current as shown in Fig. 9(b).

The trapped hole density is plotted for varying radiation doses along the oxide layer which confirms the theoretical prediction that the maximum hole trapping is related linearly to the incident radiating dose (0.5 k–10 krad) as depicted in Fig. 10. Due to increasing radiation dosage, more electron–hole pairs are generated which consequently

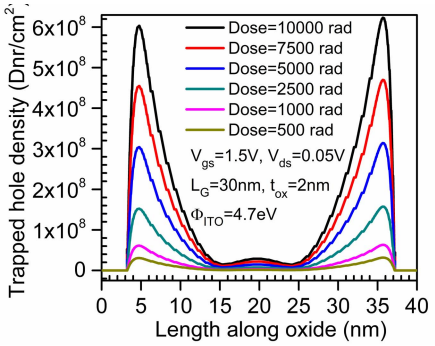


Fig. 10. Trapped hole density profile along the oxide–substrate interface.

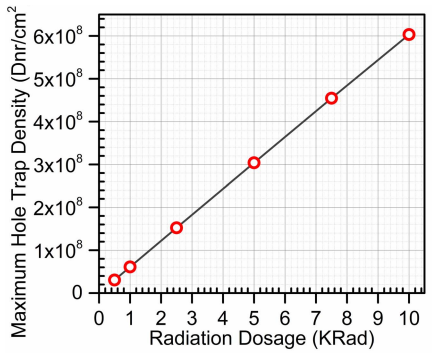


Fig. 11. Impact of varying radiation dosage on maximum hole trap density.

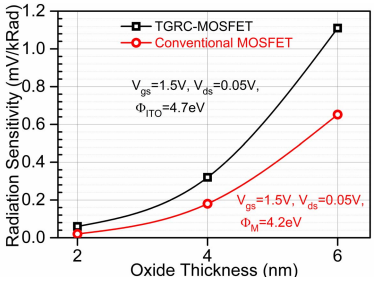


Fig. 12. Dependence of radiation sensitivity on oxide thickness in TGRC-MOSFET and conventional MOSFET.

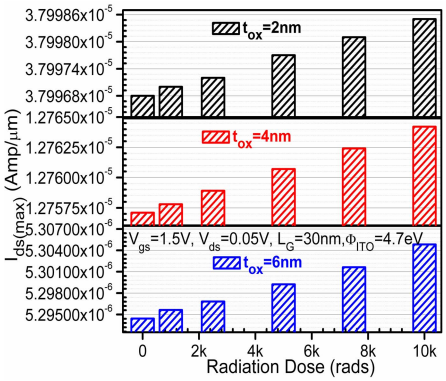


Fig. 13. Variation of ON-current with radiation dosage for different oxide thicknesses.

enhances the number of trapped holes in the oxide–substrate interface region.

By increasing the radiation dosage (0.5 k–10 krad), we are increasing the trapped hole density in the Si–SiO_2 interface region as shown in Figs. 10 and 11, thereby making it abundant in the positive charge. Due to the accumulation of charge, the overall channel being formed is enriched with more attracted electrons. Due to an increase in the attracted electrons at the surface, V_{TH} decreases ($|V_{TH-SHIFT}|$ increases) as shown in Fig. 8. Ultimately, there is a significant change in the threshold voltage in TGRC-MOSFET compared to the conventional MOSFET upon application of radiation, and this change is uniform up to 10-krad dose as reflected in Fig. 8(a) and (b), respectively. Hence, it can be used as a sensor for detecting the X-ray radiation dose up to 10 krad. This particular range of measurement comes close to the amount of radiation being used in X-ray radiation therapy which is approximately few rads of dose. Thus, the proposed device (TGRC-MOSFET) can be effectively used as a dosimeter in a situation where device dimensions are limited to few nanometers having sensitivity up to 1.11 mV/krad (at 6-nm oxide thickness).

B. Effects of Varying the Oxide Thickness on Radiation Sensitivity

The electrical behavior of TGRC-MOSFET during the process of irradiation is greatly influenced by the thickness of the gate oxide layer. As we increase or decrease the thickness of the oxide layer, consequently the channel length [$L_{CH}(= L_G + 2(NJD + t_{ox})$] is also modified. Furthermore, to validate TGRC-MOSFET as a dosimeter, sensitivity of the device is compared with the conventional MOSFET (as shown in Fig. 12) and it is found that the conventional MOSFET (where gate length and the channel length is the same [$L_G = L_{CH} = 54$ nm)] is less sensitive (0.652 mV/krad) compared to TGRC-MOSFET (1.11 mV/krad) owing to the reduced current driving capability due to short-channel effects which dominates at sub-30-nm gate length. These results show that TGRC-MOSFET provides improved performance than the conventional MOSFET. We have also simulated the effects of increasing the oxide thickness in our device, and observed this increase in oxide thickness, leading to decrease in ON current of the device and increase in threshold voltage shift, as shown in Figs. 13 and 14 respectively. As we gradually increase the oxide thickness from 2 to 6 nm, the overall volume of SiO_2 receiving total ionization dose is greatly enhanced leading to a greater number of electron–hole pair generation–recombination and, ultimately, increased trapped hole states in the oxide–substrate interface. To evaluate the radiation sensitivity of the device, we used the slope of the graph from Fig. 7. With the decrease in the thickness of the gate oxide, radiation hardness improves [13], [14]. Thus, the shift in the threshold voltage is more substantial in the thicker oxide as depicted in Fig. 14, which in turn points out that if we want to design highly sensitive dosimeter, a thicker oxide is essential, but under dimensional constraints or space critical application, as in the case of the clinical dosimeter, this reduced sensitivity can be mitigated by external amplifier circuits.

Saks *et al.* [23] predicted that for an oxide layer, the threshold voltage changes with radiation dose as the square of the oxide thickness [radiation sensitivity α (oxide thickness)^2], suggesting the uniform distribution of generated electron–hole

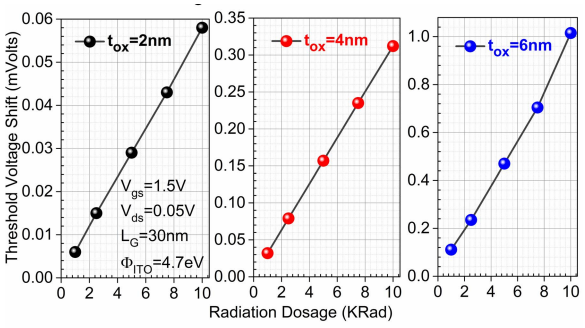


Fig. 14. Threshold voltage shift with variation in radiation dosage for various oxide thicknesses.

pair and trapped states throughout the oxide–substrate interface. For comparatively thinner oxides (less than 20 nm), threshold voltage shifts show slightly less than $(t_{ox})^2$ thickness dependence which can be easily inferred from the results shown in Fig. 12 (sensitivity up to 1.11 mV/krad at 6-nm oxide thickness) and Fig. 14. As the proposed device is optimized to generate the threshold voltage shift which depends linearly on applied radiation dose, the simulations confirm that TGRC-MOSFET will generate almost linear results within the 2–6-nm oxide thickness range. Thus, the 6-nm oxide thickness is the optimal oxide thickness for the TGRC as a dosimeter.

VI. Conclusion

We were able to achieve radiation sensitivity up to 1.11 mV/krad with our device. In 1–10-krad dose range, the electrical characteristics of the MOSFET have shown an almost linear trend. The Threshold voltage showed a linear negative shift and an ON-current linear positive shift. We further investigated the effects of varying the oxide thickness on radiation sensitivity, as oxide thickness is one of the most important factors responsible for the threshold voltage shift, our dosimetric parameter. An increment of 246% in sensitivity was observed when we increased oxide thickness from 4 to 6 nm and decrement of 81% when we reduced oxide thickness from 4 to 2 nm. Hence, for TGRC-MOSFET to be used as a dosimeter, a thicker oxide is recommended, but under dimensional constraints: 2, 4, and 6 nm, oxide thickness generated acceptable threshold voltage shift, thus can be effectively used as a dosimeter. In future medical applications, the proposed device can be used as an implantable dosimeter due to extremely small form factor (nanoscale dimensions) leading to an accurate dose determination which is the utmost requirement in medical dosimetry.

References

[1] M. Allenspach *et al.*, "SEGR and SEB in n-channel power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 6, pp. 2927–2931, Dec. 1996, doi: 10.1109/23.556887.

[2] E. G. Villani, A. Gabrielli, A. Khan, E. Pikhay, Y. Roizin, and Z. Zhang, "Monolithic 180 nm CMOS dosimeter for *in vivo* medical applications," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 2, pp. 843–849, Apr. 2013, doi: 10.1109/TNS.2013.2251472.

[3] J. Seco, B. Clasie, and M. Partridge, "Review on the characteristics of radiation detectors for dosimetry and imaging," *Phys. Med. Biol.*, vol. 59, no. 20, p. R303, 2014, doi: 10.1088/0031-9155/59/20/R303.

[4] A. Kumar, "Effect of trench depth and gate length shrinking assessment on the analog and linearity performance of TGRC-MOSFET," *Superlattices Microstruct.*, vol. 109, pp. 626–640, Sep. 2017, doi: 10.1016/j.spmi.2017.05.045.

[5] A. Kumar, N. Gupta, and R. Chaujar, "Power gain assessment of ITO based transparent gate recessed channel (TGRC) MOSFET for RF/wireless applications," *Superlattices Microstruct.*, vol. 91, pp. 290–301, Mar. 2016, doi: 10.1016/j.spmi.2016.01.027.

[6] A. Kumar, N. Gupta, and R. Chaujar, "TCAD RF performance investigation of transparent gate recessed channel MOSFET," *Microelectron. J.*, vol. 49, pp. 36–42, Mar. 2016, doi: 10.1016/j.mejo.2015.12.007.

[7] A. Kumar, N. Gupta, and R. Chaujar, "Analysis of novel transparent gate recessed channel (TGRC) MOSFET for improved analog behaviour," *Microsyst. Technol.*, vol. 22, no. 11, pp. 2665–2671, 2016, doi: 10.1007/s00542-015-2554-z.

[8] A. Kumar, N. Gupta, and R. Chaujar, "Effect of structured parameters on the hot-carrier immunity of transparent gate recessed channel (TGRC) MOSFET," *Microsyst. Technol.*, vol. 23, no. 9, pp. 4057–4064, 2017, doi: 10.1007/s00542-016-2918-z.

[9] A. Kumar, M. M. Tripathi, and R. Chaujar, "Reliability issues of In_2O_5Sn gate electrode recessed channel MOSFET: Impact of interface trap charges and temperature," *IEEE Trans. Electron Devices*, vol. 65, no. 3, pp. 860–866, Mar. 2018, doi: 10.1109/TED.2018.2793853.

[10] A. Kumar, M. M. Tripathi, and R. Chaujar, "Investigation of parasitic capacitances of In_2O_5Sn gate electrode recessed channel MOSFET for ULSI switching applications," *Microsyst. Technol.*, vol. 23, no. 12, pp. 5867–5874, 2017, doi: 10.1007/s00542-017-3348-2.

[11] T. Minami, "Transparent conducting oxide semiconductors for transparent electrodes," *Semicond. Sci. Technol.*, vol. 20, no. 4, pp. S35–S44, 2005, doi: 10.1088/0268-1242/20/4/004.

[12] D. V. Morgan, A. Salehi, Y. H. Aliyu, R. W. Bunce, and D. Diskett, "Radiation damage in indium tin oxide (ITO) layers," *Thin Solid Films*, vol. 258, nos. 1–2, pp. 283–285, 1995, doi: 10.1016/0040-6090(94)06420-2.

[13] J. R. Schwank *et al.*, "Radiation effects in MOS oxides," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 4, pp. 1833–1853, Aug. 2008, doi: 10.1109/TNS.2008.2001040.

[14] J. M. Benedetto and H. E. Boesch, "The relationship between 60Co and 10-keV X-ray damage in MOS devices," *IEEE Trans. Nucl. Sci.*, vol. 33, no. 6, pp. 1317–1323, Dec. 1986, doi: 10.1109/TNS.1986.4334599.

[15] G. A. Ausman, Jr. and F. B. McLean, "Electron–hole pair creation energy in SiO_2," *Appl. Phys. Lett.*, vol. 26, no. 4, pp. 173–175, 1975, doi: doi.org/10.1063/1.88104.

[16] T. R. Oldham and F. B. McLean, "Total ionizing dose effects in MOS oxides and devices," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 483–499, Jun. 2003, doi: 10.1109/TNS.2003.812927.

[17] *ATLAS User's Manual, Vertion 5*, SILVACO International, Santa Clara, CA, USA, 2016.

[18] M. Xiao-Hua *et al.*, "Fabrication and characterization of groove-gate MOSFETs based on a self-aligned CMOS process," *Chin. Phys.*, vol. 15, no. 1, p. 195, 2006, doi: 1009-1963/15/1/031.

[19] S. Sreelal, C. K. Lau, and G. S. Samudra, "Parasitic capacitance characteristics of deep submicrometre grooved gate MOSFETs," *Semicond. Sci. Technol.*, vol. 17, no. 3, p. 179, 2002, [Online]. Available: http://iopscience.iop.org/0268-1242/17/3/301

[20] R. Chaujar, R. Kaur, M. Saxena, M. Gupta, and R. Gupta, "Laterally amalgamated DUal material GAte concave (L-DUMGAC) MOSFET for ULSI," *Microelectron. Eng.*, vol. 85, no. 3, pp. 566–576, 2008, doi: 10.1016/j.mee.2007.10.002.

[21] V. Berland, A. Touboul, E. Dupont-Nivet, and J.-L. Leray, "Effect of X-ray radiation on MOSFET's (SIMOX) LF excess noise," in *Proc. 1st Eur. Conf. Radiat. Effects Devices Syst.*, Sep. 1991, pp. 159–163, doi: 10.1109/RADECS.1991.213639.

[22] M. Nakamura *et al.*, "Quantification of the kV X-ray imaging dose during real-time tumor tracking and from three- and four-dimensional cone-beam computed tomography in lung cancer patients using a Monte Carlo simulation," *J. Radiat. Res.*, vol. 59, no. 2, pp. 173–181, 2018, doi: 10.1093/jrr/rrx098.

[23] N. S. Saks, M. G. Ancona, and J. A. Modolo, "Radiation effects in MOS capacitors with very thin oxides at 80 °K," *IEEE Trans. Nucl. Sci.*, vol. NS-31, no. 6, pp. 1249–1255, Dec. 1984, doi: 10.1109/TNS.1984.4333491.

Ajay Kumar (S'15) received the B.Tech. degree in electronics and communication from UPTU, Lucknow, India, in 2009, and the M.Tech. degree in nanoscience and technology from Delhi Technological University (formerly the Delhi College of Engineering), New Delhi, India, in 2014, where he is currently pursuing the Ph.D. degree with the Electrical Engineering Department.

Balark Tiwari is currently pursuing the B.Tech. degree in engineering physics (major in electronics) from Delhi Technological University (formerly the Delhi College of Engineering), New Delhi, India.

Samarth Singh is currently pursuing the B.Tech. degree in engineering physics (major in electronics) from Delhi Technological University (formerly the Delhi College of Engineering), New Delhi, India.

Madan Mohan Tripathi (SM'16) received the B.Tech. degree from the Madan Mohan Malaviya Engineering College, Gorakhpur, India, in 1994, and the Ph.D. degree from Gautam Buddh Technical University, Lucknow, India, in 2010.

He is currently a Professor with the Electrical Engineering Department, Delhi Technological University (formerly the Delhi College of Engineering), New Delhi, India.

Rishu Chaujar (SM'16) is currently working as an Associate Professor with the Department of Applied Physics, Delhi Technological University (formerly the Delhi College of Engineering), New Delhi, India. She has authored or co-authored over 200 papers in various reputed international and national journals and conferences.

Dr. Chaujar is a Fellow of IETE and a Life Member of NASI.

Int. J. Electron. Commun. (AEÜ) 93 (2018) 233–241

Contents lists available at ScienceDirect

Int. J. Electron. Commun. (AEÜ)

journal homepage: www.elsevier.com/locate/aeue

Regular paper

In_2O_5Sn based transparent gate recessed channel MOSFET: RF small-signal model for microwave applications

Ajay Kumar[a], M.M. Tripathi[a], Rishu Chaujar[b,*]

[a] Department of Electrical Engineering, Delhi Technological University, Delhi 110042, India
[b] Department of Applied Physics, Delhi Technological University, Delhi 110042, India

ARTICLE INFO

Keywords:
CRC
h-parameters
ITO
S-parameters TGRC-MOSFET
Y-parameters
Z-parameters

ABSTRACT

This paper discusses the small signal RF model of Transparent Gate Recessed Channel (TGRC) MOSFET using a 3D TCAD device simulator. Small signal model is studied in terms of microwave parameters such as S (scattering) parameters, *Z* (impedance) parameters, *Y* (admittance) parameters, and *h* (hybrid) parameters with an aim to analyze the behavior of TGRC MOSFET at microwave frequency. All the results of TGRC-MOSFET have been compared with Conventional Recessed Channel (CRC) MOSFET having aluminum as gate metal electrode. Modeled results have also been compared with simulation results and found good agreement with the 3D-simulation results. Moreover, it is perceived from the results that 99.4% enhancement in the input impedance of TGRC-MOSFET and input admittance is improved by 32.9% in the proposed device (TGRC-MOSFET) in comparison to CRC-MOSFET. It has also been observed that the transit (cut-off) frequency (f_T) and maximum oscillator frequency (f_{MAX}) enhances significantly by 42.85% and 123% respectively in TGRC MOSFET owing to the remarkable reduction in intrinsic capacitances. Results reveal that the proposed device design improves the small signal behavior thus, may provide detailed insight to RF engineers for microwave applications and testing of RF ports.

1. Introduction

From past few decades, MOSFETs are commercially used in the field of the microwave, HF applications owing to the fact that highly scaled MOSFETs achieve cut-off frequencies in the range of GHz making CMOS technology appropriate for the application of RF and wireless communications [1–5]. On the contrary, scaling also results in the so-called short channel effects (SCEs), which hampers the device HF performance and make CMOS inapt for Microwave/Wireless applications [6,7]. To overcome this problem, different device schemes have been introduced in recent years which have high immunity against SCEs such as multi-gate MOSFETs, -tapered/recessed channel MOSFET [8], nanowire MOSFET [9–11], etc. Therefore, there is a need for the new type of device design which overcomes the shortcomings that arise due to downscaling of device dimensions and also simultaneously improves the device's f_T and f_{MAX}.

In our recent work, we have reported that with the incorporation of ITO as a gate electrode onto Recessed channel MOSFET considerably improves the overall device's electrical performance [12–15] and RF performance [16]. Also, the small signal [17] modeling of TGRC MOSFET has already being studied in our previous work explaining the *Y* and *Z*-parameters [18]. Still, there is a need to evaluate all the essential microwave parameters which are essential to understanding the device physics at high frequency. Therefore, in this paper, detailed explanation and modeling of small signal parameters, i.e., *S*-parameters [19,20], *Y*-parameters, *Z*-parameters, and *h*-parameters of TGRC-MOSFET are extensively explored and compared with conventional RC MOSFET to study its effectiveness for RF field.

This work is organized as follows: Section 2 describes the 3D device structure of TGRC-MOSFET. Physical transport models invoked during the simulation study [21] are discussed in Section 3 along with the calibration. Section 4 describes the small signal modeling of TGRC-MOSFET in terms of scattering, impedance, admittance, hybrid and transmission parameters. In addition, f_T, f_{MAX} and capacitance is also observed in this section. At the end conclusion is discussed in Section 5.

2. Device design and it's description

Fig. 1(a) and (b) reflect the simulated 3D device design and conceptual depiction of the small signal equivalent of TGRC-MOSFET respectively. An n-type impurity of 1×10^{19} cm^{-3} is used in the highly doped Source/Drain region. The substrate is doped with a p-type

* Corresponding author.
E-mail addresses: ajaykumar@dtu.ac.in (A. Kumar), mmtripathi@dce.ac.in (M.M. Tripathi), chaujar.rishu@dtu.ac.in (R. Chaujar).

https://doi.org/10.1016/j.aeue.2018.06.014
Received 14 April 2018; Accepted 6 June 2018

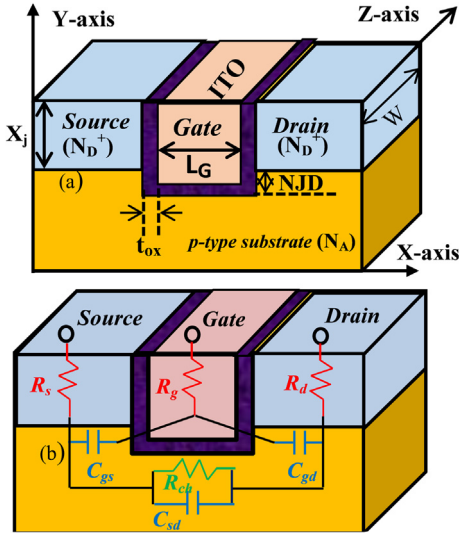


Fig. 1. (a) Schematic structure and (b) conceptual depiction of the small signal equivalent of TGRC-MOSFET.

impurity of 1×10^{17} cm^{-3}, and thick oxide layer t_{ox} of 2.0 nm is embodied in it as shown in Fig. 1(a). Negative Junction Depth (NJD) is taken as 10 nm, gate bias (V_g) is 0.7 V and drain bias (V_d) is 0.5 V. Gate workfunction of TGRC-MOSFET (Φ_{ITO}) is 4.7 eV, and for CRC-MOSFET, it is 4.4 eV. All the junctions in the device are assumed as abrupt in the simulation, uniform doping profiles and the biasing conditions are considered at room temperature (T = 300 K). Further, Gummel and Newton are the two numerical techniques which have been considered to obtain the solutions [22].

3. Calibration and simulation methodology

To validate the simulation models of sub-40 nm groove MOSFET, the experimental statistics have been drawn-out from Joerg Appenzeller et al. in 2002 [23]. Joerg Appenzeller has fabricated a grooved MOSFET [23] for 36 nm. Thus, the experimental data and simulated data is calibrated and plotted as evident in Fig. 2. For 36 nm gate length, the simulated data almost matched with the experimental data as evident from Fig. 2, thereby validating the simulation models.

All the simulations have been performed using Silvaco TCAD [22]. The simulation process includes the device structure and functionality. For comparison, we have kept all the parameters of both the devices same such as structural parameters. All simulation models used are same for both the devices. In order to consider the mobilities, scattering mechanism caused by lattice vibrations or phonons, Lombardi CVT

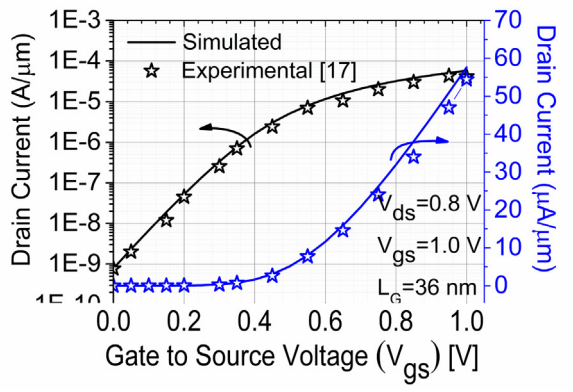


Fig. 2. Calibrated transfer characteristics of recessed channel MOSFET (36 nm gate length) with experimental [23] and simulation data.

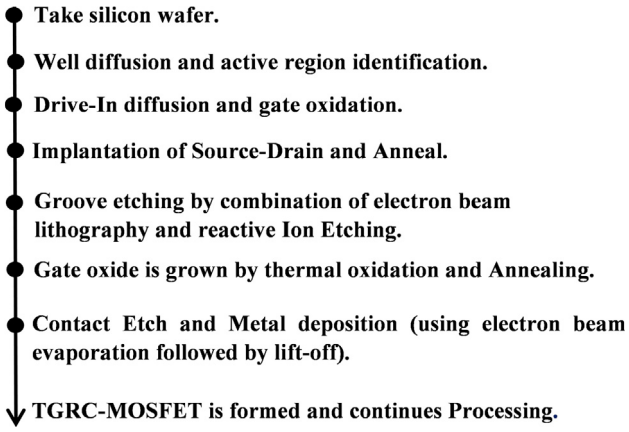


Fig. 3. Fabrication process flow of TGRC-MOSFET.

model is used. Shockley-Read-Hall (SRH) Recombination model is used to consider all the carrier generation-recombination related phenomenon [22]. A few other models have also been used to simulate the device precisely.

4. Fabrication process

In the process of fabrication (see Fig. 3), first of all, a silicon wafer (substrate) is taken, and then the diffusion process is used for the creation of n-well region. Before Drive-In diffusion and gate oxidation process, active region is identified. Source-drain implantation and anneal process are implemented before groove etching by the combination of reactive ion etching and electron beam lithography, and then the gate oxide is grown by thermal oxidation at the bottom of the groove. Contact etches, and metal deposition (using electron beam evaporation followed by lift-off) process is done in the last fabrication process. Thus, the fabrication of TGRC-MOSFET can do by using the process flow of device design schemes. The proposed device is the aids of the transparent gate engineering scheme which has been combined with groove gate for accomplishing the improved characteristics.

5. Small signal behavior modeling

For the extraction of RF small signal parameters of TGRC-MOSFET and CRC-MOSFET, Non-quasi-static (NQS) small-signal equivalent circuit (as shown in Fig. 4) of RC MOSFET is used which is operating in strong inversion region [24]. R_s is the source resistance, and R_d is the drain resistance, intrinsic gate-to-drain conductance is denoted by g_{ds} whereas g_m denotes transconductance. R_{gs} and R_{gd} have distributed channel resistance; intrinsic gate-to-drain capacitance is denoted by C_{gd} and C_{gs} denotes gate-to-source capacitance. τ is the time constant which represents the charge transport delay [24]. For those networks which

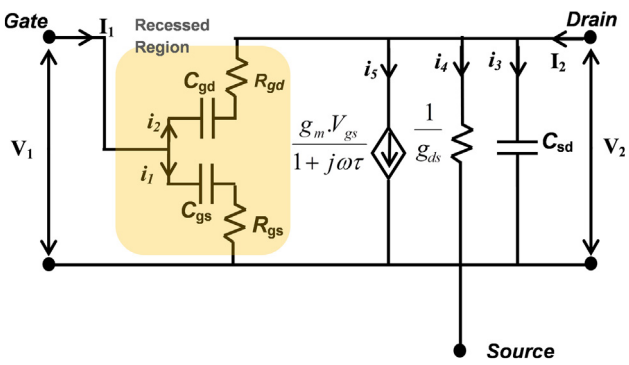


Fig. 4. Non-quasi-static (NQS) model of the RF MOSFET (RC-MOSFET).

are operating at RF and microwave frequencies, small-signal parameters (*Z*, *Y*, *S*, and *h*) are commonly used, where admittances are more easily computed as compared to voltages and currents, since, at high frequency, it is challenging to estimate currents and voltages.

5.1. Admittance (Y) parameters

A small-signal equivalent circuit can describe the transistor at high frequency where MOSFET can be converted in to its *Y*-parameter equivalent circuit consisting of all *Y*-parameters (Y_{11}, Y_{12}, Y_{21} and Y_{22}). *Y*-parameters are defined either at the input end or the output end under ac short-circuit conditions and the values depend on the operating frequency as well as dc bias conditions. AC voltages and currents can be easily measured at low frequencies, but the measurement of these parameters becomes exceptionally difficult at very high frequencies. Then, at such high frequencies, another set of parameters called scattering, or *S*-parameters can be used. However, the device physics and design are more related to *Y*-parameters and so *S*-parameters are again converted in to *Y*-parameters, and hence, the study of *Y*-parameters becomes necessary. By solving the small signal equivalent model (as shown in Fig. 4), *Y*-parameters are calculated as follows:

Total current flowing at the input port,

$$I_1 = i_1 + i_2 \tag{1}$$

Total current flowing at the output port,

$$I_2 = i_3 + i_4 + i_5 - i_1 \tag{2}$$

Applying nodal analysis at input node,

$$\frac{V_1}{X_1} + \frac{V_1 - V_2}{X_2} = 0 \tag{3}$$

$$\frac{V_2}{X_3} + \frac{V_2 - V_1}{X_2} + \frac{g_m V_{gs}}{1 + j\omega\tau} = 0 \tag{4}$$

where

$$X_1 = \frac{1 + j\omega R_{gs} C_{gs}}{j\omega C_{gs}};\ X_2 = \frac{1 + j\omega R_{ds} C_{ds}}{j\omega C_{ds}};\ X_3 = \frac{1}{g_{ds} + j\omega C_{sd}}$$

By solving Eqs. (3) and (4), and using approximations

$$\omega^2 R_{gs}^2 C_{gs}^2 << 1,\ \ \omega^2 R_{gd}^2 C_{gd}^2 << 1 \text{ and } \omega^2\tau^2 << 1$$

We get

Short circuit input admittance

$$Y_{11} \cong \omega^2 (R_{gs} C_{gs}^2 + R_{gd} C_{gd}^2) + j\omega (C_{gs} + C_{gd})$$

$$Y_{11} \cong \omega^2 (\alpha + \beta) + j\omega (C_{gs} + C_{gd}) \tag{5}$$

where, $\alpha = R_{gs} C_{gs}^2$, $\beta = R_{gd} C_{gd}^2$

Similarly, short circuit output admittance is found to be

$$Y_{22} \cong g_{ds} + \omega^2\beta + j\omega (C_{gd} + C_{sd}) \tag{6}$$

Short circuit forward transfer admittance is as follows

$$Y_{12} \cong -\omega\beta - j\omega C_{gd} \tag{7}$$

Short circuit reverse transfer admittance is as follows

$$Y_{21} \cong -\omega^2\beta - j\omega C_{gd} + g_m(1 + \tau) \tag{8}$$

Y_{11} and Y_{22} are called short-circuit input and output admittance respectively. These parameters have been evaluated for TGRC-MOSFET, and the modeled results are simultaneously compared with CRC-MOSFET. As shown in Fig. 5(a) and (b), Y_{11} and Y_{22} are low in TGRC as a comparison to CRC. Y_{11} and Y_{22} should be low for better performance of the device in RF region. Y_{12} is called short-circuit forward transfer admittance, and Y_{21} is called short-circuit reverse transfer admittance. Y_{12} and Y_{21} are both higher in case of TGRC-MOSFET and smaller in CRC-MOSFET as shown in Fig. 6(a) and (b). Improvement in *Y*-parameters indicates a reduction in parasitic capacitances and improvement in transconductance [25,26].

5.2. Impedance (Z) parameters

For the synthesis of electronic filters, Impedance (*Z*) parameters are commonly used. Z-parameters can be useful in the design and analysis of power distribution networks and impedance-matching networks. Z_{11} is called open circuit input impedance, and Z_{22} is called open circuit output impedance. These two parameters are basically used for impedance matching. Input impedance should be equal to output impedance for impedance matching, and it is necessary to condition for maximum power transfer from source to load. For high-frequency RF application, Z_{11} (input impedance) should be as high as possible. Input impedance (Z_{11}) must be high and output impedance (Z_{22}) should be low so that no-loading problem occurs in RF receiver.

From the equivalent circuit as shown in Fig. 4, the Z-parameters can be analyzed as follows:

Open circuit input impedance (driving point impedance) is found to be

$$Z_{11} \cong \frac{Y_{22}}{\Delta Y} \cong \frac{g_{ds} + \omega^2\beta + j\omega(C_{gd} + C_{sd})}{\begin{aligned} &j\omega(C_{gs}g_{ds} + C_{gd}g_{ds} + C_{gd}g_m + \tau C_{gd}g_m) \\ &+ j\omega^3(\alpha C_{gd} + \beta C_{gs} + C_{sd}(\alpha + \beta)) + \alpha\beta\omega^4 \\ &+ \omega^2(\alpha g_{ds} + \beta g_{ds} - C_{gs}C_{sd} - C_{gd}C_{sd} + \beta g_m(1 + \tau) + C_{gd}^2) \end{aligned}} \tag{9}$$

$$Z_{11} \cong \frac{g_{ds} + \omega^2\beta + j\omega(C_{gd} + C_{sd})}{\chi} \tag{10}$$

Open circuit output impedance (driving point impedance):

$$Z_{22} \cong \frac{Y_{11}}{\Delta Y} \cong \frac{\omega^2(\alpha + \beta) + j\omega(C_{gs} + C_{gd})}{\begin{aligned} &j\omega(C_{gs}g_{ds} + C_{gd}g_{ds} + C_{gd}g_m + \tau C_{gd}g_m) \\ &+ j\omega^3(\alpha C_{gd} + \beta C_{gs} + C_{sd}(\alpha + \beta)) + \alpha\beta\omega^4 \\ &+ \omega^2(\alpha g_{ds} + \beta g_{ds} - C_{gs}C_{sd} - C_{gd}C_{sd} + \beta g_m(1 + \tau) + C_{gd}^2) \end{aligned}} \tag{11}$$

$$Z_{22} \cong \frac{\omega^2(\alpha + \beta) + j\omega(C_{gs} + C_{gd})}{\chi} \tag{12}$$

Open circuit transfer impedance from input port to output port:

$$Z_{12} \cong \frac{-Y_{12}}{\Delta Y} \cong \frac{\omega\beta + j\omega C_{gd}}{\begin{aligned} &j\omega(C_{gs}g_{ds} + C_{gd}g_{ds} + C_{gd}g_m + \tau C_{gd}g_m) \\ &+ j\omega^3(\alpha C_{gd} + \beta C_{gs} + C_{sd}(\alpha + \beta)) + \alpha\beta\omega^4 \\ &+ \omega^2(\alpha g_{ds} + \beta g_{ds} - C_{gs}C_{sd} - C_{gd}C_{sd} + \beta g_m(1 + \tau) + C_{gd}^2) \end{aligned}} \tag{13}$$

$$Z_{12} \cong \frac{\omega\beta + j\omega C_{gd}}{\chi} \tag{14}$$

Open circuit transfer impedance from output to input port:

$$Z_{21} \cong \frac{-Y_{21}}{\Delta Y} \cong \frac{\omega^2\beta + j\omega C_{gd} - g_m(1 + \tau)}{\begin{aligned} &j\omega(C_{gs}g_{ds} + C_{gd}g_{ds} + C_{gd}g_m + \tau C_{gd}g_m) \\ &+ j\omega^3(\alpha C_{gd} + \beta C_{gs} + C_{sd}(\alpha + \beta)) + \alpha\beta\omega^4 \\ &+ \omega^2(\alpha g_{ds} + \beta g_{ds} - C_{gs}C_{sd} - C_{gd}C_{sd} + \beta g_m(1 + \tau) + C_{gd}^2) \end{aligned}} \tag{15}$$

$$Z_{21} \cong \frac{\omega^2\beta + j\omega C_{gd} - g_m(1 + \tau)}{\chi} \tag{16}$$

where

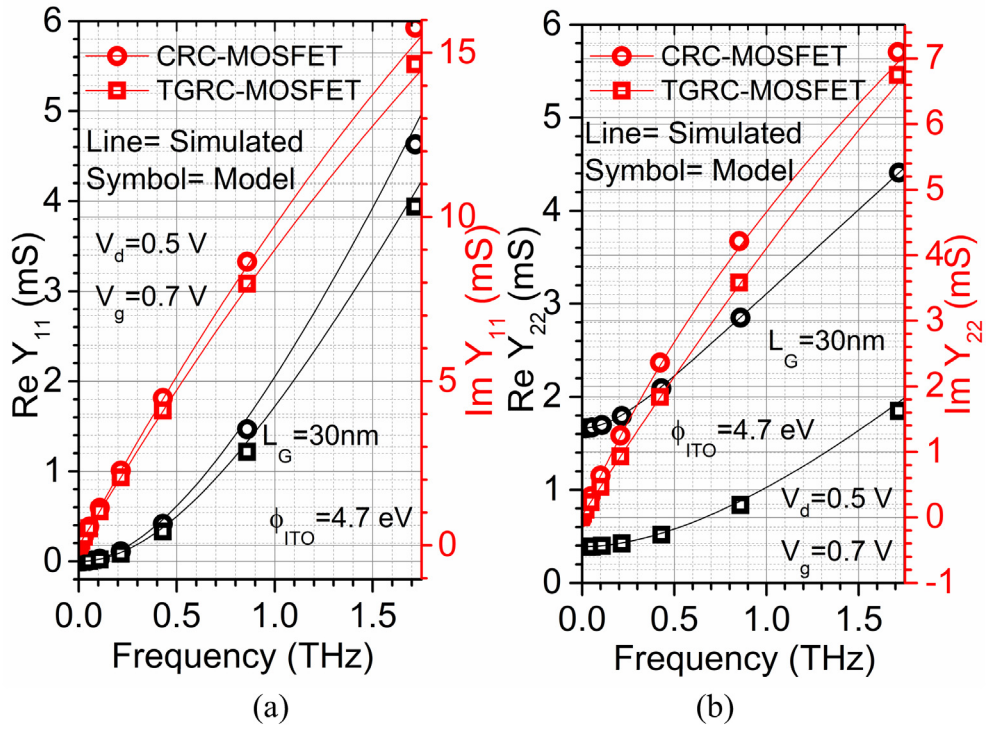


Fig. 5. (a) *Y*-parameters (Y_{11}) and (b) *Y*-parameters (Y_{22}), w.r.t. frequency at V_g = 0.7 V and V_d = 0.5 V for CRC and TGRC-MOSFET.

$$\chi = j\omega(C_{gs}g_{ds} + C_{gd}g_{ds} + C_{gd}g_m + \tau C_{gd}g_m) + j\omega^3(\alpha C_{gd} + \beta C_{gs} + C_{sd}(\alpha + \beta)) + \alpha\beta\omega^4 + \omega^2(\alpha g_{ds} + \beta g_{ds} - C_{gs}C_{sd} - C_{gd}C_{sd} + \beta g_m(1 + \tau) + C_{gd}^2)$$

$$\alpha = R_{gs}C_{gs}^2$$

$$\beta = R_{gd}C_{gd}^2$$

τ = Time constant, represents the charge transport delay

Assume that

$\omega^2 R_{gs}^2 C_{gs}^2 << 1$, $\omega^2 R_{gd}^2 C_{gd}^2 << 1$ and $\omega^2\tau^2 << 1$

Fig. 7(a) and (b) reflects the *Z*-parameters Z_{11} and Z_{22} respectively for both CRC and TGRC, and it is observed that Z_{11} and Z_{22} are higher at low frequency and decreases gradually w.r.t. frequency due to the dependency (inversely proportional) of Z_{11} and Z_{22} on ω. The modeled results are well calibrated with the simulated data for TGRC-MOSFET and its counterpart. Fig. 7(a) shows that input impedance is very high while output impedance is less (as shown in Fig. 7(b)). MOSFET has very high input impedance because of SiO_2, but in TGRC-MOSFET, input impedance also has been enhanced due to the incorporation of ITO in the grooved gate. If the input impedance of the device is high, it means the device is useful for RF-based receivers in communication systems.

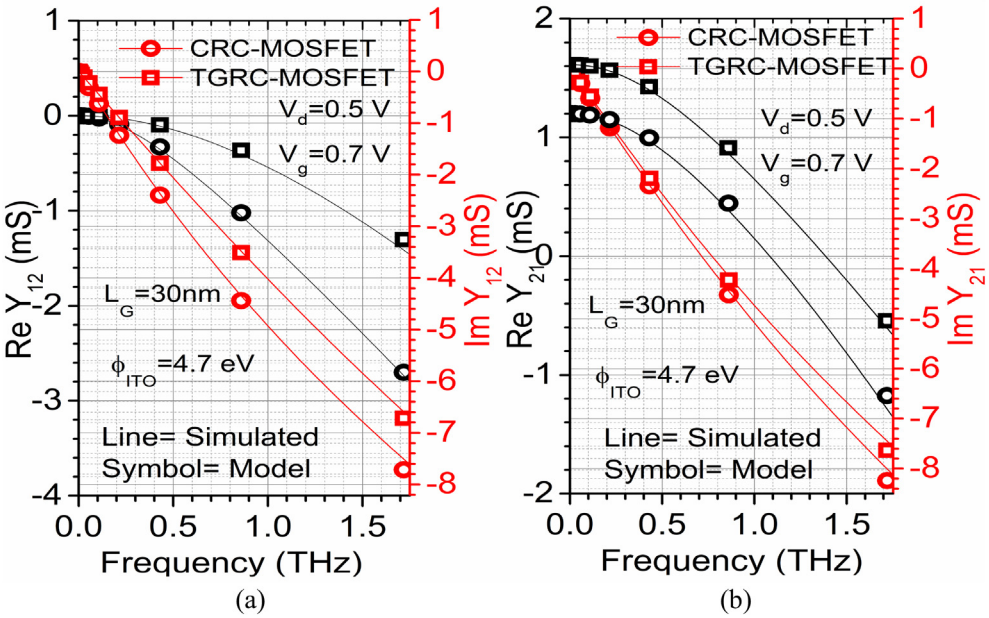


Fig. 6. (a) *Y*-parameters (Y_{12}) and (b) *Y*-parameters (Y_{21}), w.r.t. frequency at V_g = 0.7 V and V_d = 0.5 V for CRC-MOSFET and TGRC-MOSFET.

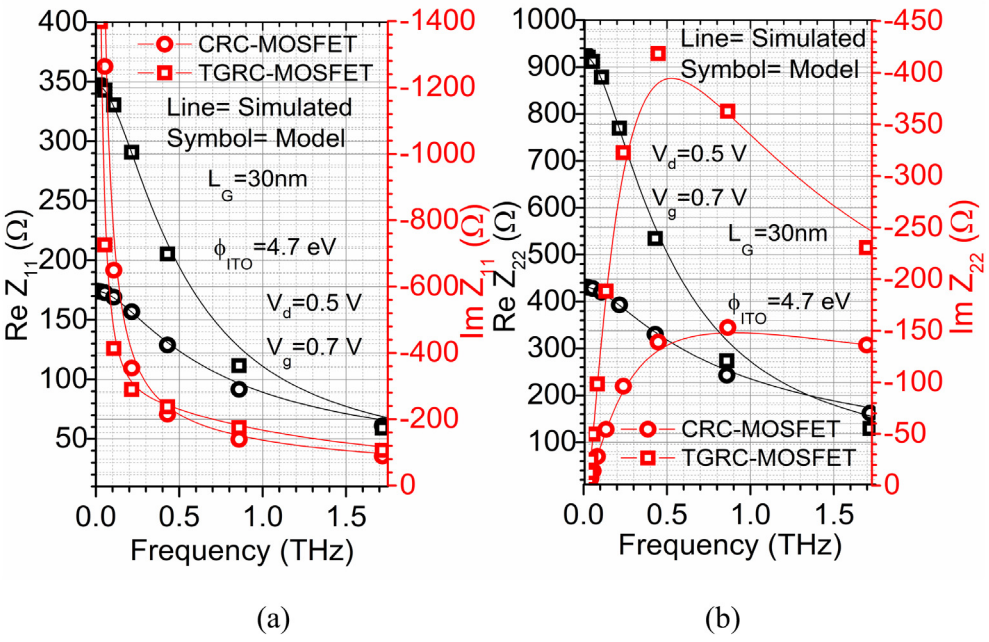


Fig. 7. (a) *Z*-parameters (Z_{11}) and (b) *Z*-parameters (Z_{22}), w.r.t. frequency at V_g = 0.7 V and V_d = 0.5 V for CRC and TGRC-MOSFET.

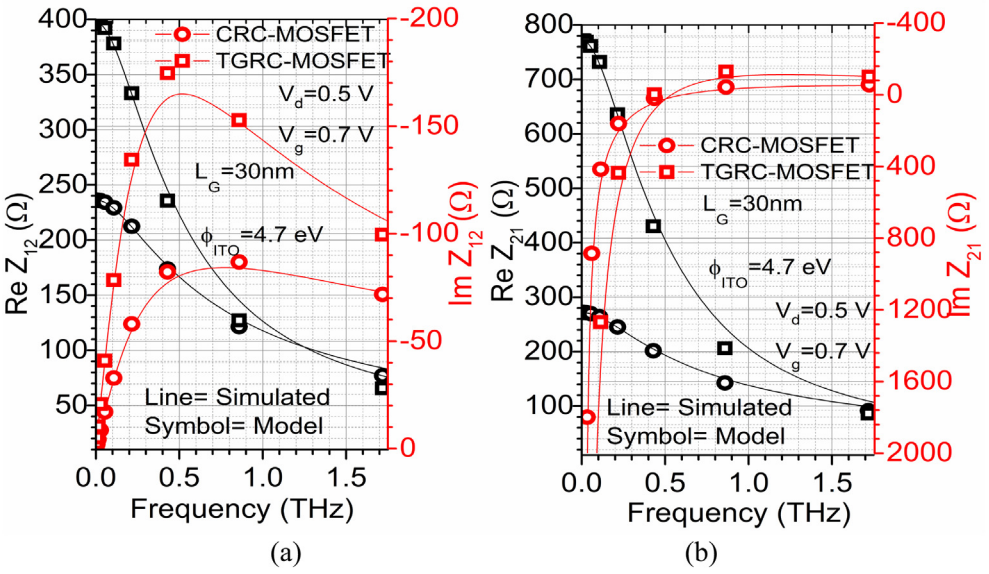


Fig. 8. (a) *Z*-parameters (Z_{12}) and 7(b) *Z*-parameters (Z_{21}), w.r.t. frequency at V_g = 0.7 V and V_d = 0.5 V for CRC and TGRC-MOSFET.

Z_{12} and Z_{21} are called open circuit transfer impedance from the input port to output port and output to input port respectively. Z_{12} and Z_{21} are also called transfer impedances. These two impedance parameters should be high for better RF performance of the device. Z_{12} and Z_{21} both are high in TGRC-MOSFET as compared to its conventional counterpart at hundreds of GHz frequency range, and the modeled data is well calibrated with simulated data as depicted in Fig. 8(a) and (b) respectively. Z_{12} and Z_{21} are improved due to the reduction in parasitic capacitances (shown later in Fig. 12) and also due to the incorporation of ITO as a gate metal, which enhances current driving capability, transconductance and hence gains of the device as reported earlier [25].

5.3. Scattering (S) parameters

In order to examine the small signal behavior of MOSFET, extraction of *S*-parameters is the most appropriate method at high frequencies. Fig. 9 shows the modeled and simulated *S*-parameters for the CRC and TGRC-MOSFET and the bias conditions are same as in Fig. 4. Symbols are modeled value and solid lines are simulated ones up to 1.7 THz frequency range. *S*-parameters are calculated using other small signal parameters such as *Y*-parameters and *Z*-parameters [27]. Here we have used *Z*-parameters for the calculation of *S*-parameters as described in Eqs. (17)–(28).

S-parameters, S_{11} is the input reflection coefficient at port-1 and S_{22} is the output reflection coefficient at port-2. Basically it is the measure of the quality of the match between the port and terminating impedance. These two parameters are obtained using Eqs. (17) and (20) respectively by using the value of *Z* component from evaluated small signal parameters (from Eqs. (9)–(16)) as required in Eqs. (17) and (20) and obtained as follows-

Fig. 9 shows the Smith Chart plot of the real part and imaginary modeled and simulated results of S_{11} and S_{22} for both devices. From Fig. 9 it is clear that both S_{11} and S_{22} reduce the frequency and

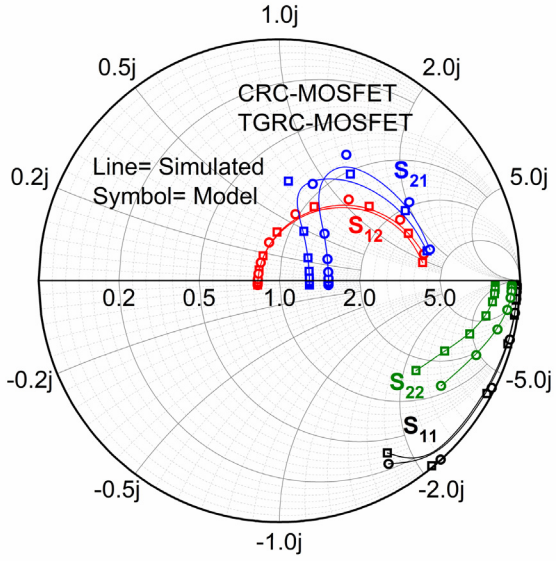


Fig. 9. Modeled and simulated *S*-parameters up to 1.7 THz frequency using extracted model parameters and small signal model for CRC and TGRC-MOSFET at $V_g = 0.7$ V and $V_d = 0.5$ V.

reduction is more in reflection coefficient in TGRC device as compared to its counterpart. Modeled and simulated results are matched as evident from Fig. 9.

$$S_{11} = \frac{(Z_{11}-Z_{01}^*)(Z_{22}+Z_{02})-Z_{12}Z_{21}}{(Z_{11}+Z_{01})(Z_{22}+Z_{02})-Z_{12}Z_{21}} \tag{17}$$

$$S_{11} = \frac{\left(\frac{g_{ds}+\omega^2\beta+j\omega(C_{gd}+C_{sd})}{\chi}-Z_{01}^*\right)\left(\frac{\omega^2(\alpha+\beta)+j\omega(C_{gs}+C_{gd})}{\chi}+Z_{02}\right)}{-\left(\frac{\omega\beta+j\omega C_{gd}}{\chi}\right)\left(\frac{\omega^2\beta+j\omega C_{gd}-g_m(1+\tau)}{\chi}\right)} \\ \frac{\left(\frac{g_{ds}+\omega^2\beta+j\omega(C_{gd}+C_{sd})}{\chi}+Z_{01}\right)\left(\frac{\omega^2(\alpha+\beta)+j\omega(C_{gs}+C_{gd})}{\chi}+Z_{02}\right)}{-\left(\frac{\omega\beta+j\omega C_{gd}}{\chi}\right)\left(\frac{\omega^2\beta+j\omega C_{gd}-g_m(1+\tau)}{\chi}\right)} \tag{18}$$

$$S_{11} = \frac{\left(\frac{g_{ds}+\omega^2\beta+j\omega(C_{gd}+C_{sd})}{\chi}-Z_{01}^*\right)\left(\frac{\omega^2(\alpha+\beta)+j\omega(C_{gs}+C_{gd})}{\chi}+Z_{02}\right)}{-\left(\frac{\omega\beta+j\omega C_{gd}}{\chi}\right)\left(\frac{\omega^2\beta+j\omega C_{gd}-g_m(1+\tau)}{\chi}\right)} \\ \frac{}{\xi} \tag{19}$$

$$S_{22} = \frac{(Z_{11}+Z_{01})(Z_{22}-Z_{02}^*)-Z_{12}Z_{21}}{(Z_{11}+Z_{01})(Z_{22}+Z_{02})-Z_{12}Z_{21}} \tag{20}$$

$$S_{22} = \frac{\left(\frac{g_{ds}+\omega^2\beta+j\omega(C_{gd}+C_{sd})}{\chi}+Z_{01}\right)\left(\frac{\omega^2(\alpha+\beta)+j\omega(C_{gs}+C_{gd})}{\chi}-Z_{02}^*\right)}{-\left(\frac{\omega\beta+j\omega C_{gd}}{\chi}\right)\left(\frac{\omega^2\beta+j\omega C_{gd}-g_m(1+\tau)}{\chi}\right)} \\ \frac{\left(\frac{g_{ds}+\omega^2\beta+j\omega(C_{gd}+C_{sd})}{\chi}+Z_{01}\right)\left(\frac{\omega^2(\alpha+\beta)+j\omega(C_{gs}+C_{gd})}{\chi}+Z_{02}\right)}{-\left(\frac{\omega\beta+j\omega C_{gd}}{\chi}\right)\left(\frac{\omega^2\beta+j\omega C_{gd}-g_m(1+\tau)}{\chi}\right)} \tag{21}$$

$$S_{22} = \frac{\left(\frac{g_{ds}+\omega^2\beta+j\omega(C_{gd}+C_{sd})}{\chi}+Z_{01}\right)\left(\frac{\omega^2(\alpha+\beta)+j\omega(C_{gs}+C_{gd})}{\chi}-Z_{02}^*\right)}{-\left(\frac{\omega\beta+j\omega C_{gd}}{\chi}\right)\left(\frac{\omega^2\beta+j\omega C_{gd}-g_m(1+\tau)}{\chi}\right)} \\ \frac{}{\xi} \tag{22}$$

S_{12} (reverse isolation parameter) defines the measure of feedback from the output to the input of an amplifier [28,29] whereas S_{21} (forward transmission coefficient) is called forward gain of two port device. Fig. 9 reflects that S_{12} increases in the proposed device as compared to the conventional device. The enhancement in S_{12} is observed due to the higher value of Z_{12} as shown in Fig. 8(a). The modeled data and simulated data have been evaluated for S_{21} and plotted in Smith chart up to 1.7 THz frequency for both the devices as shown in Fig. 9.

Similarly, S_{12} and S_{21} are evaluated as follows-

$$S_{12} = \frac{2Z_{12}(R_{01}R_{02})^{1/2}}{(Z_{11}+Z_{01})(Z_{22}+Z_{02})-Z_{12}Z_{21}} \tag{23}$$

$$S_{12} = \frac{2\left(\frac{\omega\beta+j\omega C_{gd}}{\chi}\right)(R_{01}R_{02})^{1/2}}{\left(\frac{g_{ds}+\omega^2\beta+j\omega(C_{gd}+C_{sd})}{\chi}+Z_{01}\right)\left(\frac{\omega^2(\alpha+\beta)+j\omega(C_{gs}+C_{gd})}{\chi}+Z_{02}\right)} \\ -\left(\frac{\omega\beta+j\omega C_{gd}}{\chi}\right)\left(\frac{\omega^2\beta+j\omega C_{gd}-g_m(1+\tau)}{\chi}\right) \tag{24}$$

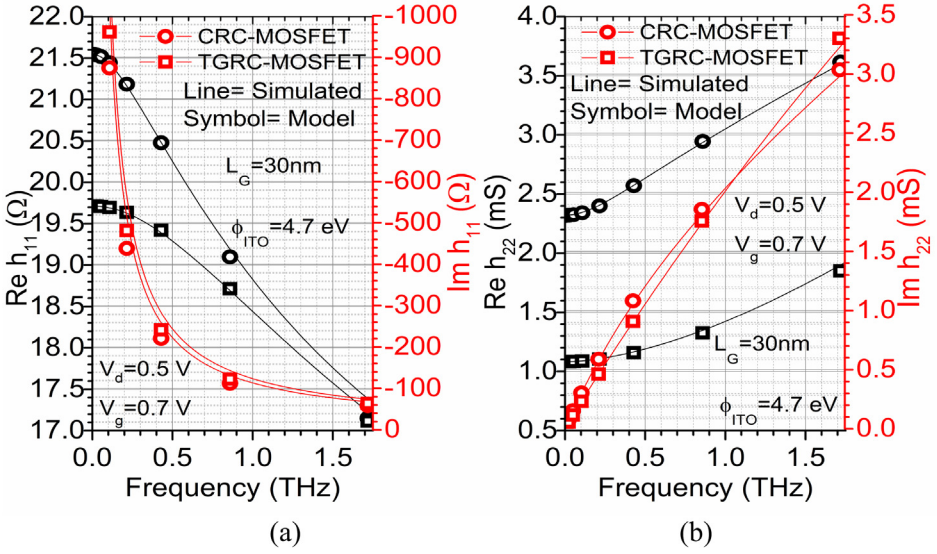


Fig. 10. (a) *h*-parameter (h_{11}) and (b) *h*-parameter (h_{22}), w.r.t. frequency at $V_g = 0.7$ V and $V_d = 0.5$ V for CRC and TGRC-MOSFET.

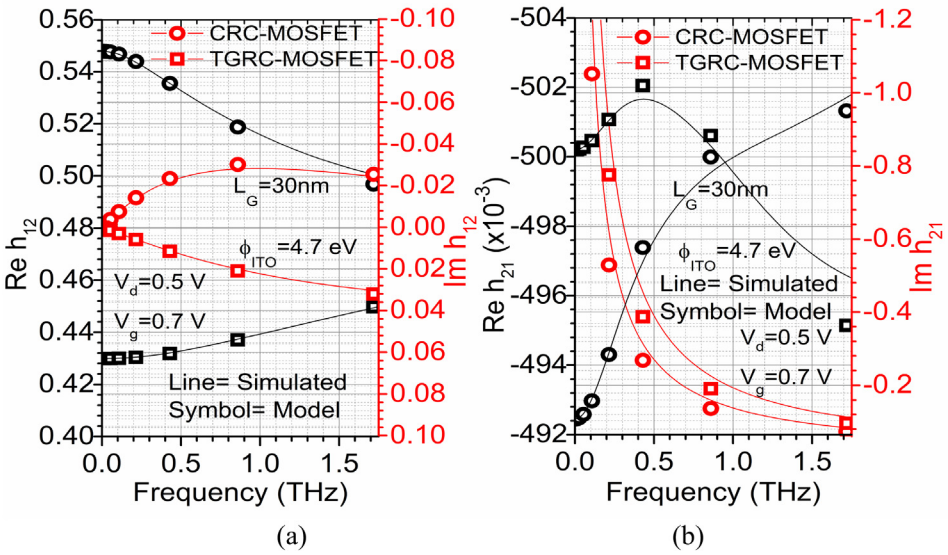


Fig. 11. (a) *h*-parameter (h_{12}) and (b) *h*-parameter (h_{21}), w.r.t. frequency at V_g = 0.7 V and V_d = 0.5 V for CRC and TGRC-MOSFET.

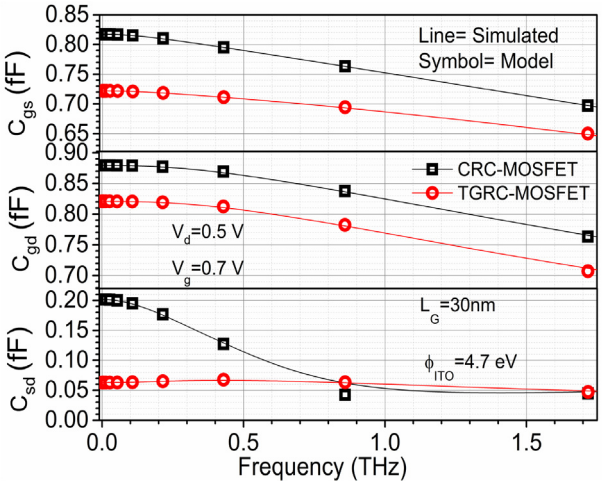


Fig. 12. RF component (C_{gs}, C_{gd} and C_{sd}) of the small signal equivalent circuit w.r.t. frequency at V_g = 0.7 V and V_d = 0.5 V for CRC and TGRC-MOSFET.

$$S_{12} = \frac{2\left(\frac{\omega\beta + j\omega C_{gd}}{\chi}\right)(R_{01}R_{02})^{1/2}}{\xi} \tag{25}$$

$$S_{21} = \frac{2Z_{21}(R_{01}R_{02})^{1/2}}{(Z_{11}+Z_{01})(Z_{22}+Z_{02}) - Z_{12}Z_{21}} \tag{26}$$

$$S_{21} = \frac{2\left(\frac{\omega^2\beta + j\omega C_{gd} - g_m(1+\tau)}{\chi}\right)(R_{01}R_{02})^{1/2}}{\left(\frac{g_{ds}+\omega^2\beta+j\omega(C_{gd}+C_{sd})}{\chi}+Z_{01}\right)\left(\frac{\omega^2(\alpha+\beta)+j\omega(C_{gs}+C_{gd})}{\chi}+Z_{02}\right) - \left(\frac{\omega\beta+j\omega C_{gd}}{\chi}\right)\left(\frac{\omega^2\beta+j\omega C_{gd}-g_m(1+\tau)}{\chi}\right)} \tag{27}$$

$$S_{21} = \frac{2\left(\frac{\omega^2\beta + j\omega C_{gd} - g_m(1+\tau)}{\chi}\right)(R_{01}R_{02})^{1/2}}{\xi} \tag{28}$$

where

$$\xi = \left(\frac{g_{ds}+\omega^2\beta+j\omega(C_{gd}+C_{sd})}{\chi}+Z_{01}\right)\left(\frac{\omega^2(\alpha+\beta)+j\omega(C_{gs}+C_{gd})}{\chi}+Z_{02}\right) - \left(\frac{\omega\beta+j\omega C_{gd}}{\chi}\right)\left(\frac{\omega^2\beta+j\omega C_{gd}-g_m(1+\tau)}{\chi}\right)$$

and

$$\chi = j\omega(C_{gs}g_{ds} + C_{gd}g_{ds} + C_{gd}g_m + \tau C_{gd}g_m) + j\omega^3(\alpha C_{gd} + \beta C_{gs} + C_{sd}(\alpha+\beta)) + \alpha\beta\omega^4 + \omega^2(\alpha g_{ds} + \beta g_{ds} - C_{gs}C_{sd} - C_{gd}C_{sd} + \beta g_m(1+\tau) + C_{gd}^2)$$

5.4. Hybrid (h) parameters

Hybrid parameters are based on the dependent variables and are known as so as they are a hybrid combination of current and voltage ratios. Hybrid parameters are very useful for describing transistors using equivalent small signal model. *h*-parameters are much easier than *Z* or *Y* parameters [30] to measure experimentally for such devices. Further, *h*-parameters have been evaluated in terms of h_{11} (short circuit input impedance), h_{22} (open circuit output admittance), h_{12} (open circuit reverse voltage gain) and h_{21} (short circuit forward current gain); as *h*-parameters deliver a quick estimate of the performance of transistor circuit. Transistor behaves as a linear device for AC small signals because the output AC signal is proportional to the input AC signal. Under such conditions, AC operation of the transistor can be described using *h*-parameters. Using *Y*-parameters, *h*- parameters can also be calculated as described in Eqs. (29)–(32) [30].

Short circuit input impedance is obtained from Eq. (5) as follows.

$$h_{11} \cong \frac{1}{Y_{11}} \cong \frac{1}{\omega^2(\alpha+\beta)+j\omega(C_{gs}+C_{gd})} \tag{29}$$

Similarly, open circuit output admittance

$$h_{22} \cong \frac{\Delta Y}{Y_{11}} \cong \frac{j\omega(C_{gs}g_{ds} + C_{gd}g_{ds} + C_{gd}g_m + \tau C_{gd}g_m) + j\omega^3(\alpha C_{gd} + \beta C_{gs} + C_{sd}(\alpha+\beta)) + \alpha\beta\omega^4 + \omega^2(\alpha g_{ds} + \beta g_{ds} - C_{gs}C_{sd} - C_{gd}C_{sd} + \beta g_m(1+\tau) + C_{gd}^2)}{\omega^2(\alpha+\beta)+j\omega(C_{gs}+C_{gd})} \tag{30}$$

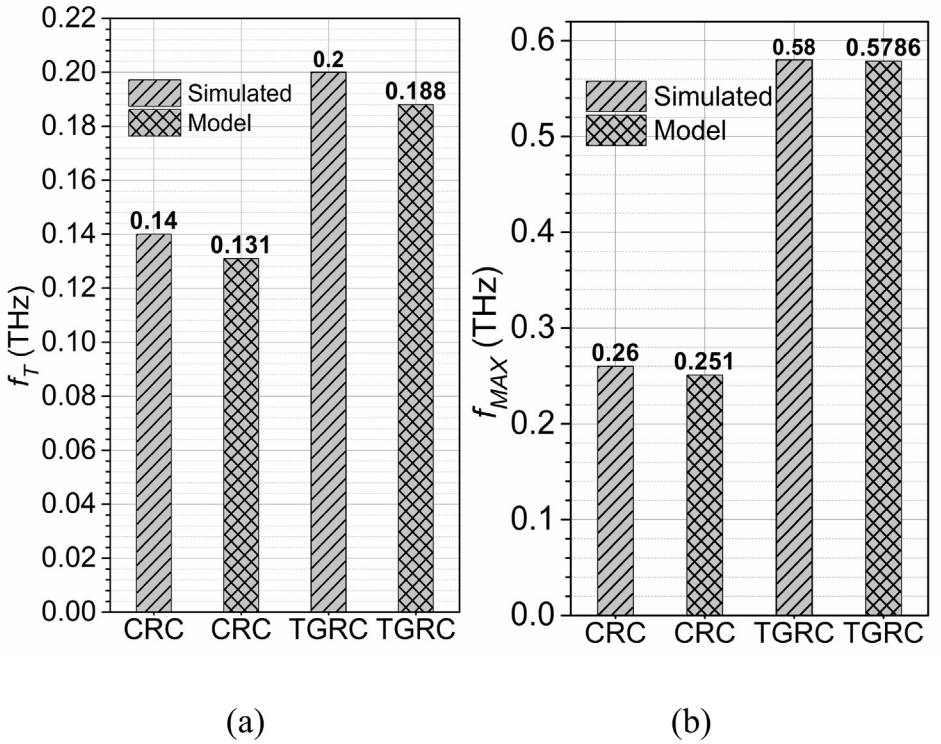


Fig. 13. (a) Transit frequency. (b) Maximum oscillator frequency at $V_g = 0.7$ V and $V_d = 0.5$ V for CRC-MOSFET and TGRC-MOSFET.

$$h_{22} \cong \frac{\Delta Y}{Y_{11}} \cong \frac{\chi}{\omega^2(\alpha+\beta)+j\omega(C_{gs}+C_{gd})}$$

Open circuit reverse voltage gain

$$h_{12} \cong \frac{-Y_{12}}{Y_{11}} \cong \frac{\omega\beta + j\omega C_{gd}}{\omega^2(\alpha+\beta)+j\omega(C_{gs}+C_{gd})} \quad (31)$$

Short circuit forward current gain,

$$h_{21} \cong \frac{Y_{21}}{Y_{11}} \cong \frac{-\omega^2\beta - j\omega C_{gd} + g_m(1+\tau)}{\omega^2(\alpha+\beta)+j\omega(C_{gs}+C_{gd})} \quad (32)$$

The real part of h_{11} and h_{22} of TGRC-MOSFET have been compared with CRC-MOSFET as shown in Fig. 10(a) and (b) respectively. It is evident that both h_{11} and h_{22} are less in TGRC as compared to the conventional device. The value of h_{11} is continuously decreased with frequency because h_{11} is inversely proportion to the Y_{11} and also to the ω^2 as clearly evident from Eq. (29) while h_{22} increases with frequency due to the higher order value of ω as shown in Eq. (30). Fig. 11(a) and (b) reflects the real and imaginary part of h_{12} and h_{21} respectively for TGRC-MOSFET and CRC-MOSFET w.r.t. frequency. h_{12} is less in TGRC-MOSFET and increased when the frequency is increased while in CRC-MOSFET, it is reduced with frequency. For TGRC-MOSFET, h_{21} is lower than CRC-MOSFET and when the frequency is increased, it is reduced due to increase in input impedance (shown in Fig. 7(a)).

Furthermore, Fig. 12 shows the other bias dependent small signal modeled parameters for TGRC and CRC in terms of C_{gs}, C_{gd} and C_{sd} and compared with simulated data. C_{gs}, C_{gd} and C_{sd} are evaluated by using Eqs. (33), (34) and (35) respectively. From Fig. 12, it is reflected that C_{gs}, C_{gd} and C_{sd} of TGRC-MOSFET turned out to be smaller (in femto-Farad) than that of CRC-MOSFETs. From Fig. 12 it is also found that the modeled data is approximately matched with the simulated data which reveals that the proposed device is suitable for high-frequency (THz) applications.

$$C_{gd} = -\mathrm{Im}(Y_{22})/\omega \quad (33)$$

$$C_{gs} = (\mathrm{Im}(Y_{11}) + \mathrm{Im}(Y_{12}))/\omega \quad (34)$$

$$C_{sd} = (\mathrm{Im}(Y_{22}) + \mathrm{Im}(Y_{12}))/\omega \quad (35)$$

5.5. Extraction of RF FoMs

Using the simplified analytical expressions for the Y-parameters (from Eqs. (5)–(8)), we can model analytically different RF FoMs which are very useful for circuit designing.

5.5.1. Transit frequency f_T

Transit frequency (f_T) [31] also called cut-off frequency [32] is defined as the frequency at which the magnitude of the current gain is equal to unity and we can calculate f_T as given in Eq. (36).

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \quad (36)$$

where transconductance is denoted by g_m (200μS for CRC and 250 μS for TGRC) and parasitic capacitances are denoted by C_{gd} and C_{gs}. Results show that f_T improves 42% in simulated data and 43.5% in modeled data (nearly matched) in TGRC-MOSFET as compared to CRC-MOSFET as reflected in Fig. 13(a) due to reduction C_{gs} and C_{gd} as reflected in Fig. 12. From Eq. (36), we see that f_T is directly proportion to the g_m so higher f_T reflects due to higher g_m [12] in TGRC device.

5.5.2. Maximum oscillation frequency f_{MAX}

Further, the extraction of modeled maximum oscillator frequency (f_{MAX}) is shown in Fig. 13(b). f_{MAX} is defined as the frequency at which the unilateral gain become equal to unity [31] and by using small signal components, f_{MAX} is given as in Eq. (37).

$$f_{MAX} = \frac{f_T}{\sqrt{4R_g(g_{ds}+2\pi f_T C_{gd})}} \quad (37)$$

In Fig. 13(b) f_{MAX} is displayed with modeled value and compared with the simulated value for CRC and TGRC devices. Results show that

f_{MAX} improves 123% in simulated data and 130% in modeled data (nearly same) in TGRC-MOSFET as compared to CRC-MOSFET as reflected in Fig. 13(b) due to the enhancement of carrier mobility which results in a reduction in gate resistance. From Eq. (37), we see that, since f_{MAX} is directly proportioned to the f_T, for the same reasons as explained for f_T, so higher f_T reflects higher f_{MAX} [12] in TGRC device than the previous published work [17,29].

6. Conclusion

This paper discusses the small signal modeling of TGRC-MOSFET in terms of microwave and electrical parameters, i.e., impedance, admittance, and hybrid parameters. It is found that TGRC-MOSFET shows high input impedance and low output impedance owing to the transparent gate which improves the current driving capability and thus the device HF performance in comparison to conventional RC MOSFET. Further, the transfer impedance also improves in TGRC device as compared to the conventional device due to reduced SCEs and high ON current which enhances the ultimate gain of the device and thus can be useful in wireless/millimeter wave applications. Moreover, the calculated model results of small signal parameters are in good agreement with the simulation results so obtained at the THz range and thus validated the small signal model. Results show that the proposed device is best suited for superior RF/Microwave applications.

Acknowledgments

The authors are gratified to University Grants Commission (UGC), Applied Physics Department, Electrical Engineering Department, Microelectronics Research Lab, and Delhi Technological to supporting this work.

Appendix A. Supplementary material

Supplementary data associated with this article can be found, in the online version, at https://doi.org/10.1016/j.aeue.2018.06.014.

References

[1] Saito M, Ono M, Fujimoto R, Tanimoto H, Ito N, Yoshitomi T, et al. 0.15-μm RF CMOS technology compatible with logic CMOS for low-voltage operation. Electron Dev, IEEE Trans 1998;45:737–42.
[2] Larson LE. Silicon technology tradeoffs for radio-frequency/mixed-signal "systems-on-a-chip". Electron Dev, IEEE Trans 2003;50:683–99.
[3] Kilchytska V, Nève A, Vancaillie L, Levacq D, Adriaensen S, Van Meer H, et al. Influence of device engineering on the analog and RF performances of SOI MOSFETs. Electron Dev, IEEE Trans 2003;50:577–88.
[4] Yang J-Y, Benaissa K, Crenshaw D, Williams B, Sridhar S, Ai J, et al. 0.1 μm RFCMOS on high resistivity substrates for system on chip (SOC) applications. In: IEDm: international electron devices meeting; 2002. p. 667–70.
[5] Adhikari MS, Singh Y. A nanoscale dual-channel trench (DCT) MOSFET for analog/RF applications. Superlattices Microstruct 2015;88:567–73.
[6] Chen QB. Compact modeling of multi-gate MOSFETs for RF designs. In: 2013 IEEE international wireless symposium (IWS); 2013.
[7] Ajayan J, Nirmal D, Prajoon P, Pravin JC. Analysis of nanometer-scale InGaAs/InAs/InGaAs composite channel MOSFETs using high-K dielectrics for high speed applications. AEU-Int J Electron Commun 2017;79:151–7.
[8] Adhikari MS, Singh Y. Implementation of trench-based power LDMOS and low voltage MOSFET on InGaAs. IETE Tech Rev 2018:1–9.
[9] Gupta N, Kumar A, Chaujar R. Oxide bound impact on hot-carrier degradation for gate electrode workfunction engineered (GEWE) silicon nanowire MOSFET. Microsyst Technol 2015.
[10] Gupta N, Kumar A, Chaujar R. Impact of device parameter variation on RF performance of gate electrode workfunction engineered (GEWE)-silicon nanowire (SiNW) MOSFET. J Comput Electron 2015;14:798–810.
[11] Gupta N, Chaujar R. Investigation of temperature variations on analog/RF and linearity performance of stacked gate GEWE-SiNW MOSFET for improved device reliability. Microelectron Reliab 2016;64:235–41.
[12] Kumar A. Effect of trench depth and gate length shrinking assessment on the analog and linearity performance of TGRC-MOSFET. Superlattices Microstruct 2017.
[13] Kumar A, Gupta N, Chaujar R. Analysis of novel transparent gate recessed channel (TGRC) MOSFET for improved analog behaviour. Microsyst Technol 2016;22:2665–71.
[14] Kumar A, Gupta N, Chaujar R. Effect of structured parameters on the hot-carrier immunity of transparent gate recessed channel (TGRC) MOSFET. Microsyst Technol 2016:1–8.
[15] Kumar A, Tripathi M, Chaujar R. Investigation of parasitic capacitances of In2O5Sn gate electrode recessed channel MOSFET for ULSI switching applications. Microsyst Technol 2017:1–8.
[16] Kumar A, Gupta N, Chaujar R. Power gain assessment of ITO based Transparent Gate Recessed Channel (TGRC) MOSFET for RF/wireless applications. Superlattices Microstruct 2016;91:290–301.
[17] Adhikari M, Singh Y. High-performance dual-channel InGaAs MOSFET for small signal RF applications. Electron Lett 2015;51:1203–5.
[18] Kumar A, Tripathi M, Chaujar R. Small-signal modeling of In2O5Sn based transparent gate recessed channel MOSFET for microwave/RF applications. In: Microwave conference (APMC), 2017 IEEE Asia Pacific. (IEEE, 2017). p. 976–9.
[19] Taher H, Schreurs D, Nauwelaers B. Extraction of small-signal equivalent circuit model parameters for Si/SiGe HBT using S-parameters measurements and one geometrical information. AEU-Int J Electron Commun 2006;60:567–72.
[20] Sinnesbichler FX, Olbrich GR. Thermal time constant extraction for HBTs from S-parameter measurements. AEU-Int J Electron Commun 2003;57:181–4.
[21] Wei B, Lu C. Transition metal dichalcogenide MoS2 field-effect transistors for analog circuits: a simulation study. AEU-Int J Electron Commun 2018;88:110–9.
[22] Silvaco I. ATLAS user's manual, Santa Clara, CA, Ver 2011;5.
[23] Appenzeller J, Martel R, Avouris P, Knoch J, Scholvin J, del Alamo JA, Rice P, Solomon P. Sub-40 nm SOI V-groove n-MOSFETs. IEEE Electron Dev Lett 2002;23:100–2.
[24] Tsividis Y, McAndrew C. Operation and modeling of the MOS transistor. Oxford Univ Press; 2011.
[25] Kumar A, Gupta N, Chaujar R. TCAD RF performance investigation of transparent gate recessed channel MOSFET. Microelectron J 2016;49:36–42.
[26] Kumar A, Tripathi M, Chaujar R. Reliability issues of In2O5Sn gate electrode recessed channel MOSFET: impact of interface trap charges and temperature. IEEE Trans Electron Dev 2018;65:860–6.
[27] Frickey DA. Conversions between S, Z, Y, H, ABCD, and T parameters which are valid for complex source and load impedances. IEEE Trans Microw Theory Tech 1994;42:205–11.
[28] Pozar DM. Microwave engineering. John Wiley & Sons; 2009.
[29] Adhikari MS, Singh Y. High performance multi-channel MOSFET on InGaAs for RF amplifiers. Superlattices Microstruct 2017;102:79–87.
[30] Alexander CK, Sadiku MN, editors. Fundamentos de circuitos eléctricos. McGraw Hill Mexico; 2013.
[31] Chalkiadaki M-A, Enz CC. RF small-signal and noise modeling including parameter extraction of nanoscale MOSFET from weak to strong inversion. IEEE Trans Microw Theory Tech 2015;63:2173–84.
[32] Sarkar A, Jana R. The influence of gate underlap on analog and RF performance of III–V heterostructure double gate MOSFET. Superlattices Microstruct 2014;73:256–67.

Journal of Computational Electronics
https://doi.org/10.1007/s10825-018-1237-2

Ultralow-power dielectric-modulated nanogap-embedded sub-20-nm TGRC-MOSFET for biosensing applications

Ajay Kumar[1] · **M. M. Tripathi**[1] · **Rishu Chaujar**[2]

Abstract
This work examines a transparent gate recessed channel (TGRC) metal–oxide–semiconductor field-effect transistor (MOSFET) for biosensing, including a nanogap cavity for detection of biomolecules and a transparent gate to enhance the overall current efficiency of the RC-MOSFET. For the detection of neutral biomolecules, electrical characteristics such as I_{ON}/I_{OFF}, shift in threshold voltage and change in surface potential have been studied and thereafter, sensitivity of has been evaluated. The biosensor showed enhanced sensitivity for biomolecules with increase in their dielectric value, due to greater on-current owing to the change in capacitances. The capacitances were therefore also evaluated. In addition, immobilization of biomolecules degrades the noise immunity of MOSFET and thereby their overall biosensing performance, while the noise immunity of the TGRC device was very high even in the presence of biomolecules. Furthermore, modulation of the cavity gap length was also investigated, revealing that its increase (from 8 to 20 nm) significantly enhanced the sensitivity of the proposed biosensor. Overall, the results of this analysis reveal that such TGRC-MOSFET biosensors can exhibit high sensitivity (1.45) at very low drain bias (0.2 V), enabling their use for biosensor applications to diagnose various diseases which require lower noise, high speed, low power, and high density.

Keywords Biosensor · Dielectric constant · ITO · Nanogap · Sensitivity · TGRC-MOSFET

1 Introduction

With the aid of nanotechnology, various kinds of biosensor have been developed for use in medical applications and disease diagnostics, which require high performance. According to medical science, prompt detection of any disease, mainly cancer, favors patient survival. Numerous methods have been developed for detection of biomolecules, e.g., the enzyme-linked immunosorbent assay [1], for Alzheimer's disease, ovarian cancer, and coronary artery disease. However, many of these approaches are complicated and time-consuming due to the requirement for labeling techniques [2]. Field-effect transistor (FET)-based biosensors have attracted much attention over recent years owing to their good scalability, high sensitivity, rapid electrical detection, low power consumption, direct electrical readout, and low-cost mass production in comparison with other methods such as surface plasmon resonance devices [3], microcantilevers [4], and arrays of fluorescence sensors [5]. Low-cost, highly sensitive, reliable, user-friendly, and quick diagnostic biosensing devices are essential for different biological and biomedical applications [6]. For biosensing applications, sensitivity is the key factor for a MOSFET. Over time, various structures such as the nanowire junctionless MOSFET [7] and tunnel FET [8, 9] have been introduced to enhance the sensitivity of FET-based biosensors. Nanotechnology-based biosensor devices have also been used [10–12] to overcome the difficulties of conventional health diagnostic methods.

Moreover, advanced development of semiconductor technology for medical applications has shrunk device dimensions to the nanoscale regime to provide high packing density for high-speed integrated circuits. However, in such ultra-scaled device, the influence of short-channel effects (SCEs)

✉ Rishu Chaujar
chaujar.rishu@dtu.ac.in

Ajay Kumar
ajaykumar@dtu.ac.in

M. M. Tripathi
mmtripathi@dce.ac.in

[1] Department of Electrical Engineering, Delhi Technological University, Delhi 110042, India

[2] Department of Applied Physics, Delhi Technological University, Delhi 110042, India

Published online: 11 September 2018

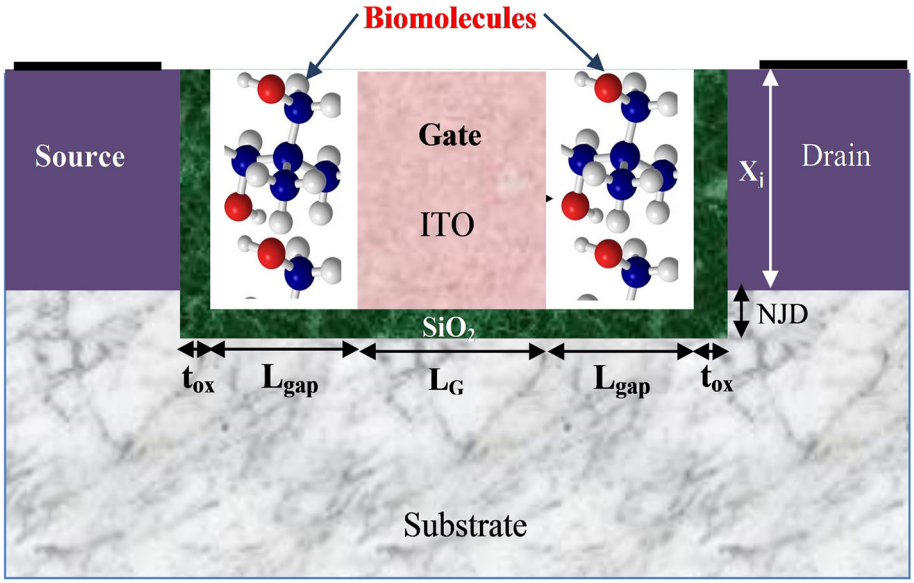


Fig. 1 Schematic structure of the TGRC-MOSFET biosensor

deeply affects device performance [7]. To overcome SCEs, several device engineering schemes and alternative device structures have been reported in literature [13–18]. Among these, the recessed channel (RC) MOSFET is considered to be the most promising, since it overcomes almost all the SCEs and is also compatible with recent complementary metal–oxide–semiconductor (CMOS) technology [19]. Numerous innovative gate materials have been explored recently to enhance the current driving capability of CMOS devices while enhancing their overall performance. In the proposed (TGRC-MOSFET) biosensor device, indium-doped tin oxide (ITO) has been used as a gate material, due to its enhanced electrical properties, as demonstrated in previous work [20–25]. Use of ITO significantly enhances the on-current, due to its very low resistivity (10^{-5} Ω cm) and high mobility (53.5 $cm^2\ V^{-1}\ s^{-1}$) [26].

In the work presented herein, a TGRC-MOSFET for use as a biosensor was simulated, considering the electrical properties of various biomolecules. The main use of biosensors is to sense biological elements, based on their sensitivity to and binding specificity of biological species such as enzymes, proteins, nucleotides, or antibodies. In the proposed TGRC-MOSFET biosensor, the channel potential of the device is influenced by the electrical properties of the biomolecules, enabling their detection. In a conventional MOSFET, current flows in the channel when the gate voltage exceeds a threshold voltage (V_{TH}). In a biosensor, this effect is modulated by the dielectric constant due to immobilization of biomolecules below the gate electrode, because the threshold voltage depends upon the gate capacitance. Absorption of biomolecules therefore affects the electrical characteristics of the sensor, changing its sensitivity.

2 Device structure, simulation methodology, and calibration

The three-dimensional (3D) structure of the considered biosensor device is shown in Fig. 1. For immobilization of biomolecules, a small nanocavity is created in the gate insulator region, since this is the most important region determining the behavior and characteristics of a CMOS device. Here, L_{gap} is the length of the nanogap cavity (8 nm), t_{ox} is the oxide thickness (2 nm), and the gate length L_G is taken to be 20 nm. The source and drain regions are highly doped with n-type impurity to 5×10^{19} cm^{-3}, while the substrate is doped with p-type impurity to 1×10^{17} cm^{-3}, as shown in Fig. 1. The negative junction depth (NJD) is taken to be 10 nm, while the gate workfunction of ITO (Φ_{ITO}) is 4.7 eV. The gate bias (V_{gs}) is 0.7 V and the drain bias (V_{ds}) is 0.2 V throughout the analysis, unless otherwise stated. Absorption of different biomolecules is modeled by introduction of an insulator having the same dielectric constant as a particular biomolecule into the nanogap cavity. The unfilled cavity (i.e., with no biomolecules present) is modeled by using an insulator with dielectric constant $k = 1$, while the dielectric constant of the different considered biomolecules is as follows: streptavidin ($k = 2.1$) [27], biotin ($k = 2.63$) [28], 3-aminopropyltriethoxysilane (APTES) ($k = 3.57$), and protein ($k = 8$) [29]. Streptavidin–biotin is used to detect Marek's disease virus (MDV) using an enzyme-linked immunosorbent assay (ELISA) method [30], while APTES facilitates immobilization of biomolecules onto the surface for detection of dengue virus [31].

ATLAS is a powerful simulation tool that can be used for extraction of reliability results and figures of merit (FOMs) [32]. Various simulation models were applied in this work, including the Lombardi constant voltage and temperature

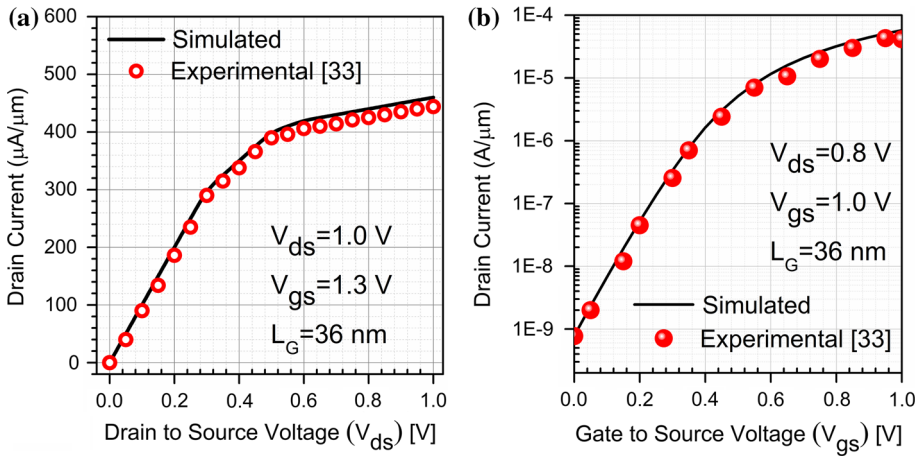


Fig. 2 Calibrated **a** output and **b** transfer characteristics of experimental and simulation data for a recessed channel MOSFET (with 36 nm gate length)

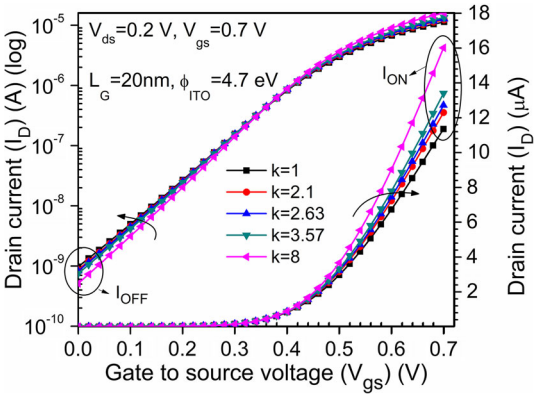


Fig. 3 Transfer characteristics of the nanogap-embedded TGRC-MOSFET in the presence of different biomolecules

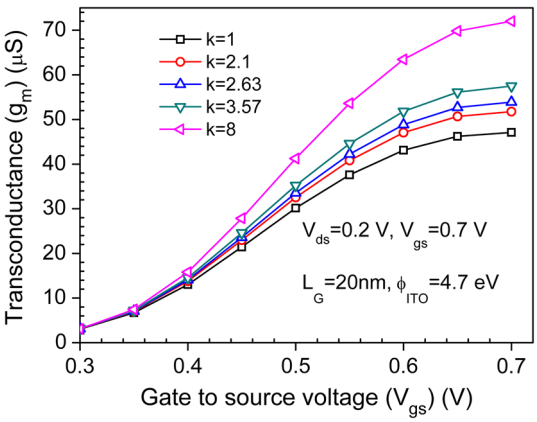


Fig. 4 Transconductance (g_m) of the nanogap-embedded TGRC-MOSFET in the presence of different biomolecules

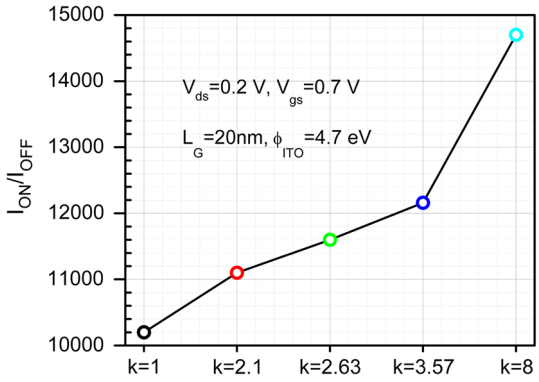


Fig. 5 Switching ratio (I_{on}/I_{off}) of the TGRC-MOSFET at drain voltage of 0.2 V in the presence of different biomolecules

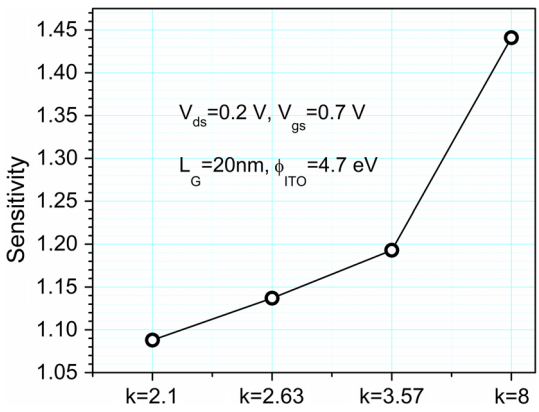


Fig. 6 Sensitivity of the TGRC-MOSFET at drain voltage of 0.2 V to different biomolecules

(CVT) model to consider all the mobilities, e.g., due to scattering caused by the parallel and perpendicular fields applied on the device. For carrier generation–recombination, we used Shockley–Read–Hall (SRH) recombination. Fermi–Dirac statistics were used in case of very highly doped material. To include information about the low energy (temperature) of the carriers, we used the energy balance transport (EBT) model [32]. Calibration of the physical model parameters of the simulated device against experimental results by Appenzeller et al. [33] is shown in Fig. 2. To validate the simulation results, output and transfer characteristic statistics were extracted [33] for a 36-nm RC-MOSFET, as shown in Fig. 2a and b, respectively. The simulation results in Fig. 2a, b almost match with the experimental data for a sub-40-nm RC MOSFET, thus validating the simulation model.

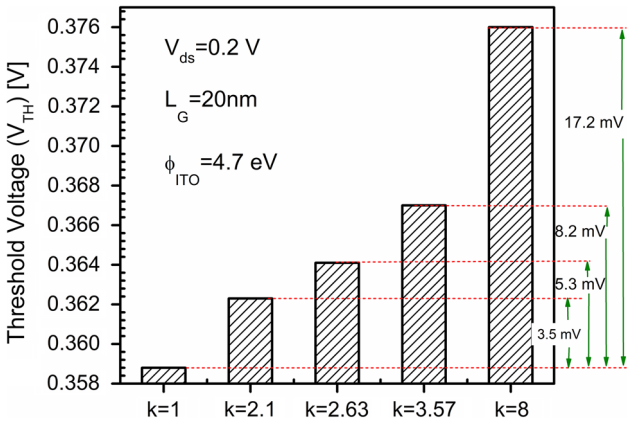


Fig. 7 Threshold voltage shifts for the TGRC-MOSFET in the presence of different biomolecules

3 Results and discussion

It can be observed from the transfer characteristics of the biosensor (Fig. 3) that, when neutral biomolecules are immobilized ($k > 1$) in the cavity, the on-current is significantly enhanced compared with in their absence ($k = 1$), owing to the increase in the dielectric constant and thus transconductance (Fig. 4). Different biomolecules can be detected based on the measured current [5]. Due to the increase in the on-current, the switching ratio (I_{on}/I_{off}) also increases with the dielectric value, as shown in Fig. 5. Thus, the change in the drain current or the enhancement in I_{on} and the switching ratio for a particular biomolecule could be used as key parameters for their detection/sensing. Furthermore, sensitivity is one of the critical parameters for the proposed biosensor device. In this work, the sensitivity (S) is defined as

$$S = \frac{I_{on}(k > 1)}{I_{on}(k = 1)}. \quad (1)$$

Figure 6 presents the sensitivity for the different biomolecules, clearly showing a higher value for protein biomolecules ($k = 8$) compared with streptavidin, biotin, and APTES (2.1, 2.63, and 3.57, respectively); note that the use of a uniform dielectric value implies that the cavity is completely filled by the specific biomolecule.

The threshold voltage was used as a sensing parameter for detection, being directly related to the dielectric constant; in this work, the threshold voltage is defined as the gate voltage at which the drain current is equal to 10^{-7} A/μm. The threshold voltage increases as the dielectric constant of the biomolecule is increased, as shown for the TGRC-MOSFET in Fig. 7. Threshold voltage shifts (ΔV_{TH}) of 3.5 mV, 5.3 mV, 8.2 mV, and 17.2 mV are observed when the dielectric constant changes from the unfilled cavity to a cavity filled with

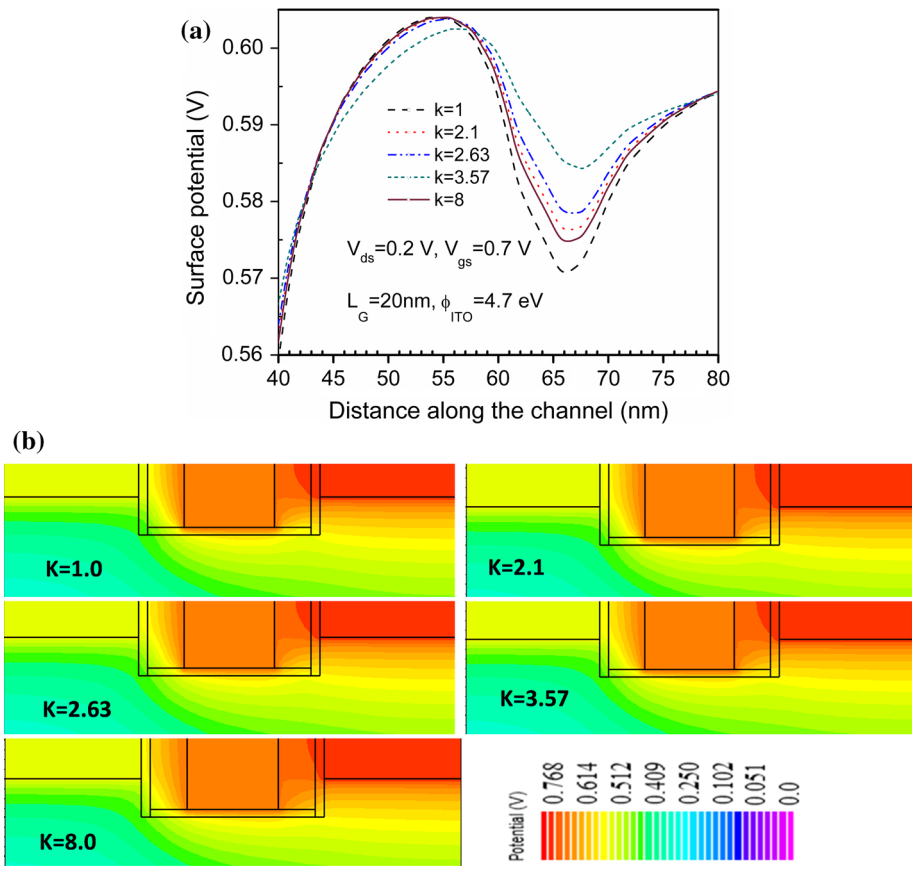


Fig. 8 **a** Surface potential along the channel from the source to drain and **b** corresponding contour plots of the TGRC-MOSFET in the presence of different biomolecules with $k = 1$, 2.1, 2.63, 3.57, and 8

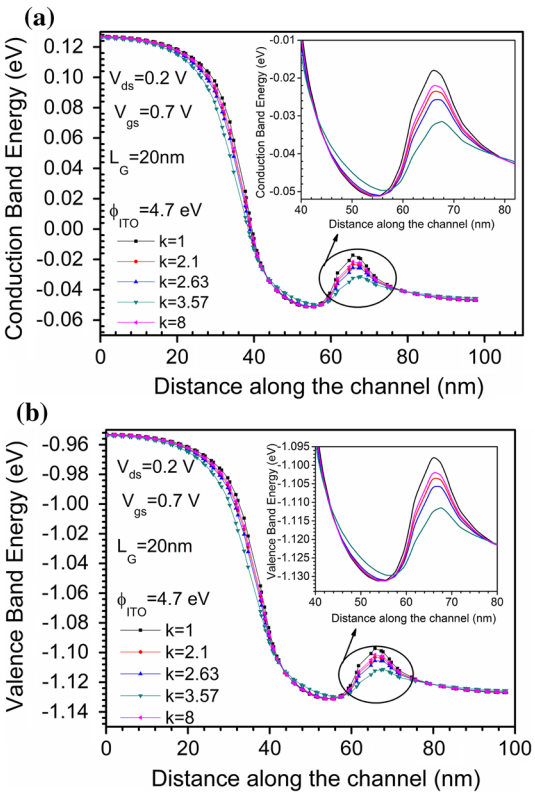


Fig. 9 Effect on **a** conduction band and **b** valence band along the channel of the TGRC-MOSFET in the presence of different biomolecules

biomolecules having $k = 2.1$, 2.63, 3.57, and 8 (Fig. 7). The threshold voltage shift (ΔV_{TH}) can also be used to define the sensitivity of the biosensor as $\Delta V_{TH} = V_{TH}$(after absorption of the molecule) $- V_{TH}$(air-filled cavity) [34, 35]. The threshold voltage shift is directly proportional to the permittivity of the absorbed neutral biomolecule, i.e.,

$$\Delta V_{TH} \propto k_{bio}. \tag{2}$$

Thus, it can be said that, the higher the absolute value of ΔV_{TH}, the better the sensitivity of the biosensor, as ΔV_{TH} also represents the sensitivity of the device and the threshold voltage shifts toward higher gate voltage in the presence of biomolecules in the nanogap cavity [7].

In addition, the electrical performance of the TGRC-MOSFET biosensor was also examined in terms of the surface potential (Fig. 8a). Under the cavity region, deformation of the potential occurs (especially at the drain end). When biomolecules are immobilized in the cavity, a change in potential is observed due to the change in the dielectric constant due to the biomolecules. This shift in potential can also be used to detect the presence of biomolecules in the cavity region. The contour plots of the surface potential in Fig. 8b clearly reveal the change in potential when biomolecules are immobilized in the nanocavity.

Figure 9a, b shows the energy band profile [36] in terms of the conduction- and valence-band energies. When biomolecules are immobilized in the nanogap cavity, these values clearly change. The shift in the energy band is more prominent for the biomolecule with dielectric constant of 3.57 but less prominent for protein, streptavidin, and biotin, in comparison with the case of no biomolecules [37], as reflected in Fig. 9a, b. Thus, the TGRC device can also be used as a low-power sensing device due to this effective change in the energy band profiles at low drain bias (0.2 V) for different biomolecules. Moreover, it is also observed from Fig. 10a that, in the presence of various biomolecules ($k =$

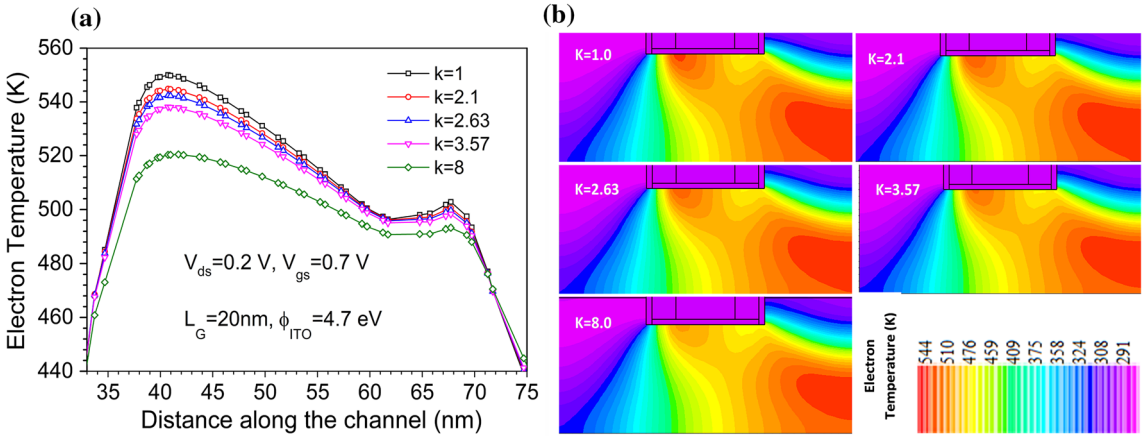


Fig. 10 **a** Electron temperature along the channel from the source to drain and **b** corresponding contour plots for the TGRC-MOSFET in the presence of different biomolecules

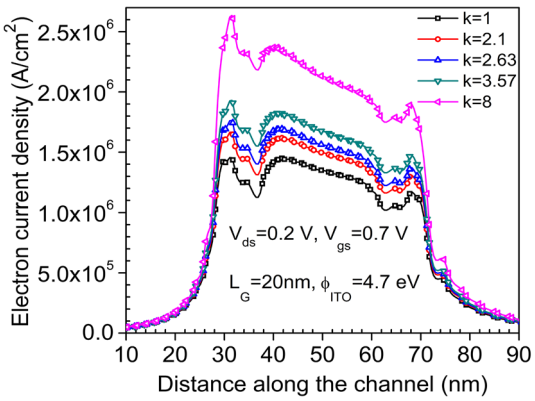


Fig. 11 Electron current density along the channel from the source to drain of the TGRC-MOSFET in the presence of different biomolecules

2.1 to $k = 8$), the electron temperature decreases (~510 K) due to the high-k dielectric (biomolecules) in the nanocavity gap, due to which leakage currents such as hot-electron injected gate current and impact-ionization substrate current are almost eliminated, thereby enhancing the I_{on} (shown in Fig. 2) and sensitivity of the device. The contour plots in Fig. 10b clearly show how the temperature varies when biomolecules are introduced into the nanogap cavity. This change in temperature with the dielectric constant can also be used to detect/sense which biomolecules are present.

Furthermore, the electron current density [38] in the presence and absence of different biomolecules in the nanocavity gap was also investigated (Fig. 11). For the proposed biosensor, it is evident that the electron current density is very low when the nanocavity gap is unfilled (for air, $k = 1$) but increases when the nanocavity gap is filled with different biomolecules, in increasing order of dielectric constant. For higher current density, I_{on} will also be high, due to which the switching ratio is increased. Thus, the device will be more sensitive when the nanocavity gap is filled with biomolecules, and this effect will increase with their dielectric constant (as shown in Fig. 6). It is also observed from Fig. 11 that the electron current density is higher just below the nanocavity gap.

3.1 Effect on parasitic capacitances

The presence of biomolecules can easily be observed via the change in stray capacitances, as the stray (parasitic) capaci-

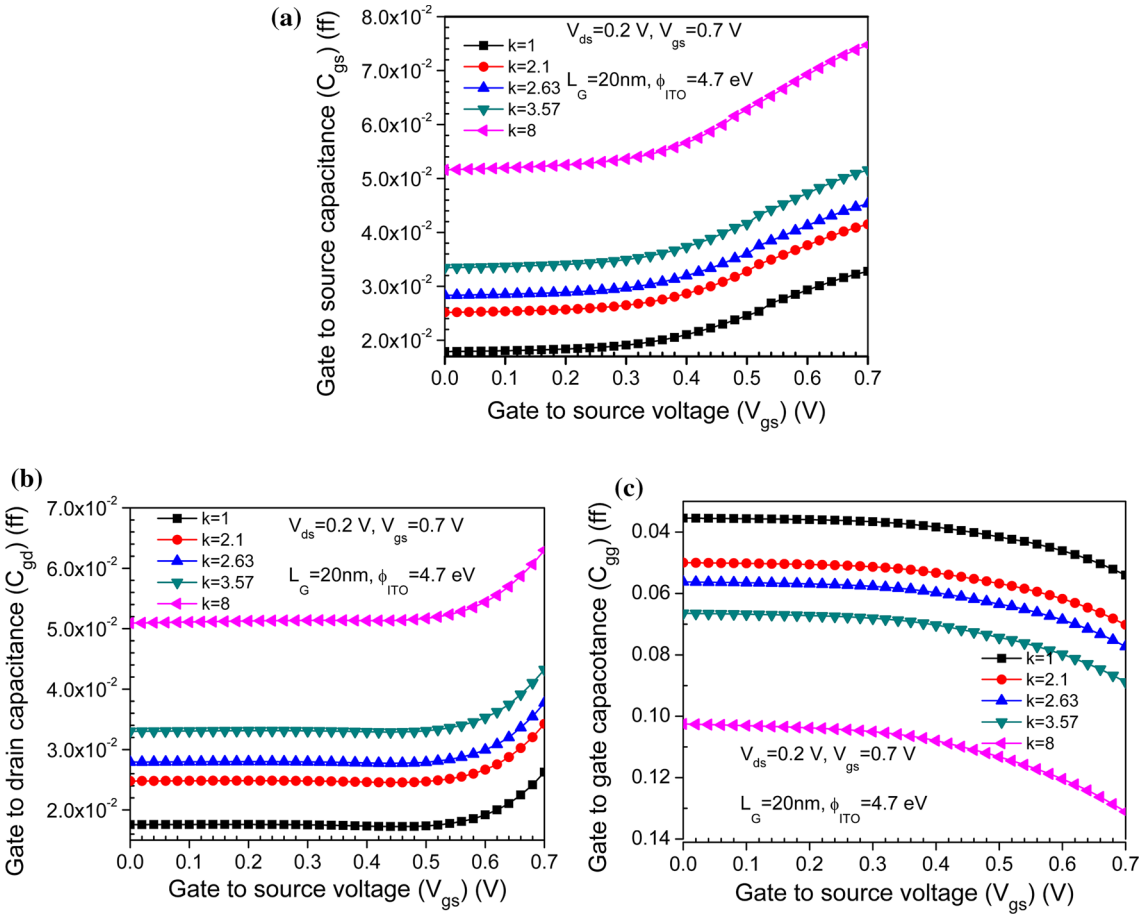


Fig. 12 Effect of different biomolecules on the parasitic capacitances **a** C_{gs}, **b** C_{gd}, and **c** C_{gg} of the TGRC-MOSFET

tances of a field-effect transistor are altered when changing the dielectric constant of the gate oxide. Figure 12a shows that the gate-to-source capacitance (C_{gs}) and gate-to-drain capacitance (C_{gd}) are altered (increased) when changing (increasing) the dielectric constant to $k = 2.1$, 2.63, 3.57, and 8, in comparison with the unfilled nanogap. When V_{gs} increases, the accumulation of charge carriers near the gate increases [39], and as a result, the gate-to-source capacitance and gate-to-drain capacitance also increase. Similarly, the gate capacitance (C_{gg}) is altered in the presence of biomolecules with different dielectric constants, and when V_{gs} increases, the accumulation of charges at the gate increases, and thus so does the gate capacitance [39], as shown in Fig. 12c. When molecules with higher dielectric constant are immobilized, these changes in the capacitances become more prominent, as is evident from Fig. 12a–c. These parasitic capacitances must be as low as possible in semiconductor devices for use in high-performance applications. According to these results, all the parasitic capacitances (C_{gs}, C_{gd}, and C_{gg}) evaluated in the presence of different biomolecules were very low (on femtofarad scale).

3.2 Noise assessment

In the presence of any external agent (e.g., biomolecules) in the channel region of a CMOS device, the electrical behavior in terms of the I–V characteristics is altered. Such shifts in the I–V characteristics and other electrical behaviors can be used as key parameters for detection of biomolecules, as clearly shown above. However, the presence of such agents can also sometimes lead to noise, which degrades biosensor performance. Therefore, to examine the noise immunity of the proposed biosensor, noise FOMs such as the minimum noise figure, noise conductance, etc. were also evaluated w.r.t. frequency [14]. As is clear from Figs. 13, 14, and 15, when biomolecules are immobilized in the cavity, all the noise parameters improved significantly at high frequency. This observation can mainly be attributed to the transparent conducting material (ITO) used in the TGRC-MOSFET architecture, because the random motion of free electrons is decreased in such materials. In a transparent conducting material, the temperature (Fig. 10) does not increase significantly when the concentration of charge carriers is increased, thereby improving the noise immunity of the TGRC biosensor in the presence of biomolecules. Furthermore, Fig. 15 shows another noise parameter, called the optimum source impedance ($Z_{OPT} = R_{OPT} + jX_{OPT}$), with respect to frequency for the different biomolecules, being nearly zero at higher frequencies when the nanocavity gap is empty but increasing with the dielectric constant of the biomolecule. This indicates that the device exhibits very low noise in the presence of biomolecules and is thus suitable for use in biosensing applications.

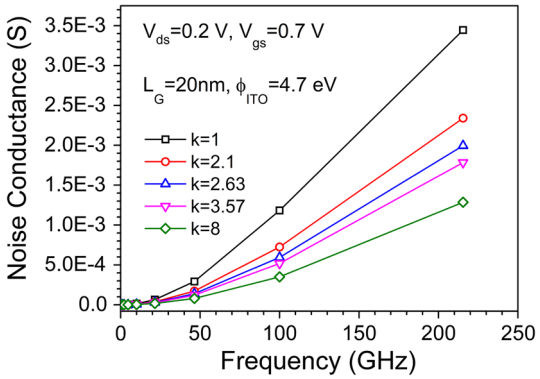


Fig. 13 Noise conductance in the GHz frequency range for the TGRC-MOSFET in the presence of different biomolecules

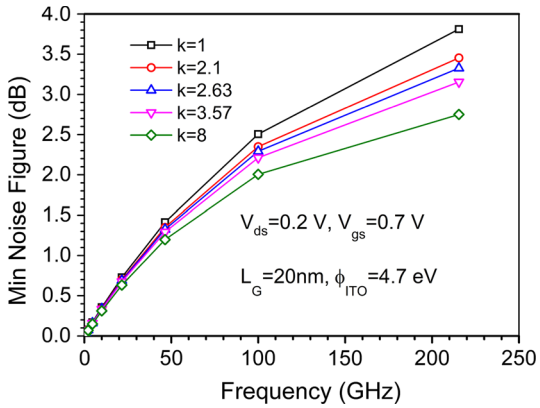


Fig. 14 Minimum noise figure in the GHz frequency range for the TGRC-MOSFET in the presence of different biomolecules

3.3 Effect of the nanogap cavity length

Moreover, the length of the cavity (L_{gap}) [36] was also varied, with the aim of determining its effect on the sensitivity and thereby the performance of the biosensor. Figure 16 shows that, with increase in the cavity gap length, the on/off ratio was evidently reduced due to an increase in the off-current

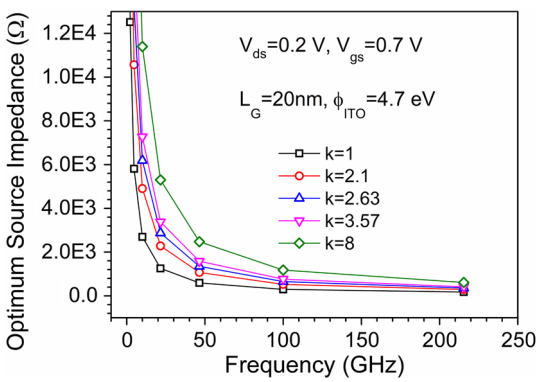


Fig. 15 Optimum source impedance in the GHz frequency range for the TGRC-MOSFET in the presence of different biomolecules

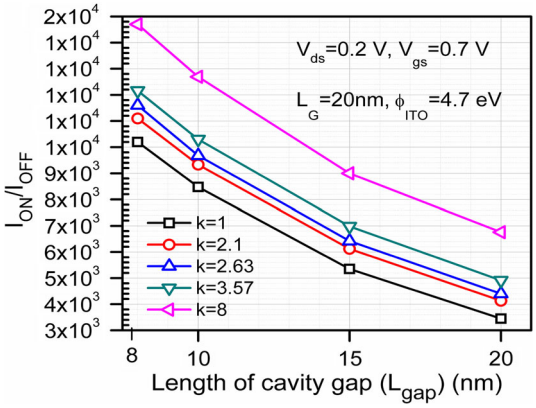


Fig. 16 Effect of varying the cavity gap length in the TGRC-MOSFET on the switching ratio for different biomolecules

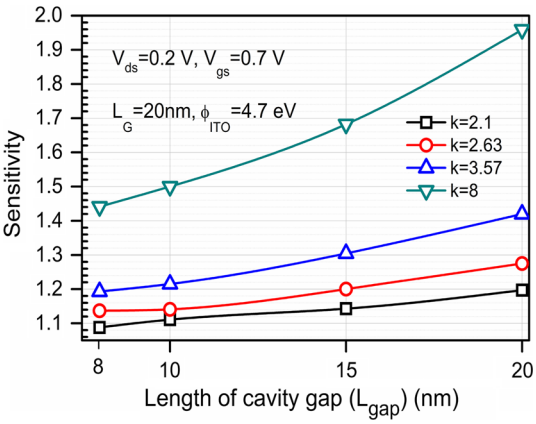


Fig. 17 Effect of varying the cavity gap length in the TGRC-MOSFET on the sensitivity for different biomolecules

resulting from higher capacitance. Moreover, the sensitivity of the TGRC biosensor with different cavity gap lengths was also evaluated, revealing that it increased significantly with increase in L_{gap} (Fig. 17). From this figure, it is observed that the sensitivity increased with k for given L_{gap}. Thus, for $L_{gap} = 20$ nm, the nanogap-embedded TGRC biosensor showed better sensitivity for protein ($k = 8$) in comparison with the other biomolecules. Figure 18 shows the change in the threshold voltage with L_{gap} (from 8 to 20 nm) for the different biomolecules; this noticeable change in the threshold voltage with the dielectric constant can be used as one of the sensing parameters for detection of biomolecules. Thus, the TGRC-MOSFET with cavity gap length of 20 nm showed optimum performance and hence could be employed as a low-power, high-sensitivity biosensor for diagnosis of various associated diseases.

4 Conclusions

The applicability of a nanogap-embedded ITO-gated recessed channel MOSFET as a biosensor was investigated.

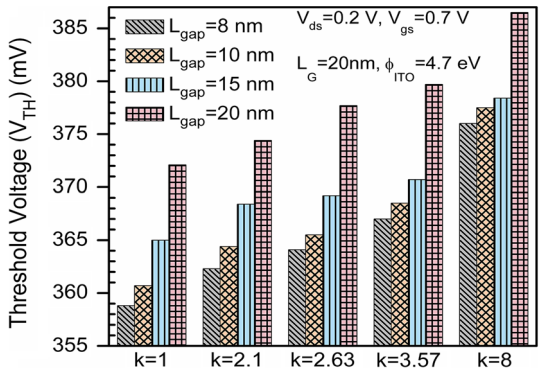


Fig. 18 Effect of varying the cavity gap length in the TGRC-MOSFET on the threshold voltage for different biomolecules

For detection of various biomolecules, the electrical behavior was studied in terms of the threshold voltage shift, sensitivity, switching ratio, surface potential, capacitance, and noise FOMs. The results obtained clearly show that, due to the ITO gate in the nanogap cavity, the electrical performance of the TGRC biosensor was significantly enhanced, showing higher sensitivity for biomolecules with high dielectric value. It was found that the sensitivity was higher for detection of protein ($k \approx 8$) in comparison with the other biomolecules, with higher noise immunity. Such TGRC-MOSFET biosensors are therefore proved to be favorable devices for use in sensing applications, due to their high sensitivity and low-power electrical detection of different biomolecules. Furthermore, the effects of the cavity gap length on the switching ratio, V_{TH}, and sensitivity of the proposed biosensor were also examined, revealing that the sensitivity increased with increase in the cavity length while the overall biosensor performance was slightly degraded. Therefore, the cavity gap length must be optimized for better performance, which will enable use of such sub-20-nm TGRC-MOSFETs as low-noise, high-speed, high-sensitivity biosensors for detection of various associated diseases.

Acknowledgements The authors are grateful to the University Grants Commission (UGC) for provision of financial assistance to carry out this work.

References

1. Comini, E., Baratto, C., Concina, I., Faglia, G., Falasconi, M., Ferroni, M., Galstyan, V., Gobbi, E., Ponzoni, A., Vomiero, A., Zappa, D., Sberveglieri, V., Sberveglieri, G.: Metal oxide nanoscience and nanotechnology for chemical sensors. Sens. Actuators B Chem. **179**, 3–20 (2013)
2. Lee, J., Jang, J., Choi, B., Yoon, J., Kim, J.-Y., Choi, Y.-K., Kim, D.M., Kim, D.H., Choi, S.-J.: A highly responsive silicon nanowire/amplifier MOSFET hybrid biosensor. Sci. Rep. **5**, 12286 (2015)

3. Bergveld, P.: The development and application of FET-based biosensors. Biosensors **2**(1), 15–33 (1986)
4. Sang, S., Wang, Y., Feng, Q., Wei, Y., Ji, J., Zhang, W.: Progress of new label-free techniques for biosensors: a review. Crit. Rev. Biotechnol. **36**(3), 465–481 (2016)
5. Im, H., Huang, X.-J., Gu, B., Choi, Y.-K.: A dielectric-modulated field-effect transistor for biosensing. Nat. Nanotechnol. **2**(7), 430–434 (2007)
6. Vu, X.T., Eschermann, J.F., Stockmann, R., GhoshMoulick, R., Offenhäusser, A., Ingebrandt, S.: Top-down processed silicon nanowire transistor arrays for biosensing. Phys. Status Solidi **206**(3), 426–434 (2009)
7. Ahangari, Z.: Performance assessment of dual material gate dielectric modulated nanowire junctionless MOSFET for ultrasensitive detection of biomolecules. RSC Adv. **6**(92), 89185–89191 (2016)
8. Chandan, B.V., Nigam, K., Sharma, D.: Junctionless based dielectric modulated electrically doped tunnel FET based biosensor for label-free detection. Micro Nano Lett. **13**(4), 452–456 (2018)
9. Kanungo, S., Chattopadhyay, S., Gupta, P.S., Sinha, K., Rahaman, H.: Study and analysis of the effects of SiGe source and pocket-doped channel on sensing performance of dielectrically modulated tunnel FET-based biosensors. IEEE Trans. Electron Devices **63**(6), 2589–2596 (2016)
10. Azmi, M.M., Tehrani, Z., Lewis, R., Walker, K.-A., Jones, D., Daniels, D., Doak, S., Guy, O.: Highly sensitive covalently functionalised integrated silicon nanowire biosensor devices for detection of cancer risk biomarker. Biosens. Bioelectron. **52**, 216–224 (2014)
11. Ahn, J.-H., Choi, S.-J., Han, J.-W., Park, T.J., Lee, S.Y., Choi, Y.-K.: Double-gate nanowire field effect transistor for a biosensor. Nano Lett. **10**(8), 2934–2938 (2010)
12. Gao, A., Lu, N., Dai, P., Li, T., Pei, H., Gao, X., Gong, Y., Wang, Y., Fan, C.: Silicon-nanowire-based CMOS-compatible field-effect transistor nanosensors for ultrasensitive electrical detection of nucleic acids. Nano Lett. **11**(9), 3974–3978 (2011)
13. Barsan, R.M.: Analysis and modeling of dual-gate MOSFET's. IEEE Trans. Electron Devices **28**(5), 523–534 (1981)
14. Gupta, N., Chaujar, R.: Influence of gate metal engineering on small-signal and noise behaviour of silicon nanowire MOSFET for low-noise amplifiers. Appl. Phys. A **122**(8), 1–9 (2016)
15. Gupta, N., Chaujar, R.: Optimization of high-k and gate metal workfunction for improved analog and intermodulation performance of gate stack (GS)-GEWE-SiNW MOSFET. Superlattices Microstruct. **97**, 630–641 (2016)
16. Gupta, N., Chaujar, R.: Investigation of temperature variations on analog/RF and linearity performance of stacked gate GEWE-SiNW MOSFET for improved device reliability. Microelectron. Reliab. **64**, 235–241 (2016)
17. Gupta, N., Kumar, A., Chaujar, R.: Oxide bound impact on hot-carrier degradation for gate electrode workfunction engineered (GEWE) silicon nanowire MOSFET. Microsyst. Technol. **22**, 2655–2664 (2015)
18. Chaujar, R., Kaur, R., Saxena, M., Gupta, M., Gupta, R.: TCAD assessment of gate electrode workfunction engineered recessed channel (GEWE-RC) MOSFET and its multilayered gate architecture—part I: hot-carrier-reliability evaluation. IEEE Trans. Electron Devices **55**(10), 2602–2613 (2008)
19. Chaujar, R., Kaur, R., Saxena, M., Gupta, M., Gupta, R.: Laterally amalgamated DUal material GAte concave (L-DUMGAC) MOSFET for ULSI. Microelectron. Eng. **85**(3), 566–576 (2008)
20. Kumar, A., Gupta, N., Chaujar, R.: Analysis of novel transparent gate recessed channel (TGRC) MOSFET for improved analog behaviour. Microsyst. Technol. **22**(11), 2665–2671 (2016)
21. Kumar, A., Gupta, N., Chaujar, R.: Power gain assessment of ITO based transparent gate recessed channel (TGRC) MOSFET for RF/wireless applications. Superlattices Microstruct. **91**, 290–301 (2016)
22. Kumar, A., Gupta, N., Chaujar, R.: TCAD RF performance investigation of transparent gate recessed channel MOSFET. Microelectron. J. **49**, 36–42 (2016)
23. Kumar, A., Gupta, N., Chaujar, R.: Effect of structured parameters on the hot-carrier immunity of transparent gate recessed channel (TGRC) MOSFET. Microsyst. Technol. **23**, 4057–4064 (2017)
24. Kumar, A., Tripathi, M., Chaujar, R.: Reliability issues of In_2O_5Sn gate electrode recessed channel MOSFET: impact of interface trap charges and temperature. IEEE Trans. Electron Devices **65**, 860–866 (2018)
25. Kumar, A., Tripathi, M., Chaujar, R.: In_2O_5 Sn based transparent gate recessed channel MOSFET: RF small-signal model for microwave applications. AEU-Int. J. Electron. Commun. (2018)
26. Minami, T.: Transparent conducting oxide semiconductors for transparent electrodes. Semicond. Sci. Technol. **20**(4), S35 (2005)
27. Busse, S., Scheumann, V., Menges, B., Mittler, S.: Sensitivity studies for specific binding reactions using the biotin/streptavidin system by evanescent optical methods. Biosens. Bioelectron. **17**(8), 704–710 (2002)
28. Densmore, A., Xu, D.-X., Janz, S., Waldron, P., Mischki, T., Lopinski, G., Delâge, A., Lapointe, J., Cheben, P., Lamontagne, B.: Spiral-path high-sensitivity silicon photonic wire molecular sensor with temperature-independent response. Opt. Lett. **33**(6), 596–598 (2008)
29. Kim, S., Baek, D., Kim, J.-Y., Choi, S.-J., Seol, M.-L., Choi, Y.-K.: A transistor-based biosensor for the extraction of physical properties from biomolecules. Appl. Phys. Lett. **101**(7), 073703 (2012)
30. Davidson, I., Malkinson, M., Strenger, C., Becker, Y.: An improved ELISA method, using a streptavidin-biotin complex, for detecting Marek's disease virus antigens in feather-tips of infected chickens. J. Virol. Methods **14**(3–4), 237–241 (1986)
31. Zhang, G.-J., Zhang, L., Huang, M.J., Luo, Z.H.H., Tay, G.K.I., Lim, E.-J.A., Kang, T.G., Chen, Y.: Silicon nanowire biosensor for highly sensitive and rapid detection of Dengue virus. Sens. Actuators B Chem. **146**(1), 138–144 (2010)
32. Silvaco, I.: ATLAS User's Manual, Santa Clara, CA, Ver 5 (2011)
33. Appenzeller, J., Martel, R., Avouris, P., Knoch, J., Scholvin, J., del Alamo, J.A., Rice, P., Solomon, P.: Sub-40 nm SOI V-groove n-MOSFETs. IEEE Electron Device Lett. **23**(2), 100–102 (2002)
34. Kannan, N., Kumar, M.J.: Dielectric-modulated impact-ionization MOS transistor as a label-free biosensor. IEEE Electron Device Lett. **34**(12), 1575–1577 (2013)
35. Choi, J.-M., Han, J.-W., Choi, S.-J., Choi, Y.-K.: Analytical modeling of a nanogap-embedded FET for application as a biosensor. IEEE Trans. Electron Devices **57**(12), 3477–3484 (2010)
36. Abdi, D.B., Kumar, M.J.: Dielectric modulated overlapping gate-on-drain tunnel-FET as a label-free biosensor. Superlattices Microstruct. **86**, 198–202 (2015)
37. Kranti, A., Armstrong, G.A.: Engineering source/drain extension regions in nanoscale double gate (DG) SOI MOSFETs: analytical model and design considerations. Solid-State Electron. **50**(3), 437–447 (2006)
38. Stern, E., Vacic, A., Reed, M.A.: Semiconducting nanowire field-effect transistor biomolecular sensors. IEEE Trans. Electron Devices **55**(11), 3119–3130 (2008)
39. Kumar, A., Tripathi, M., Chaujar, R.: Investigation of parasitic capacitances of In_2O_5Sn gate electrode recessed channel MOSFET for ULSI switching applications. Microsyst. Technol. **23**, 5867–5874 (2017)

Vacuum 164 (2019) 46–52

Contents lists available at ScienceDirect

Vacuum

journal homepage: www.elsevier.com/locate/vacuum

Sub-30nm In_2O_5Sn gate electrode recessed channel MOSFET: A biosensor for early stage diagnostics

Ajay Kumar[a], M.M. Tripathi[a], Rishu Chaujar[b,*]

[a] Department of Electrical Engineering, Delhi Technological University, Delhi, 110042, India
[b] Department of Applied Physics, Delhi Technological University, Delhi, 110042, India

ARTICLE INFO

Keywords:
APTES
Biosensor
Sensitivity
Indium Tin Oxide (ITO)
Protein
Streptavidin
TGRC-MOSFET

ABSTRACT

This paper presents a technology computer-aided design (TCAD) analysis of an ultrasensitive In_2O_5Sn gate (transparent gate) recessed channel (TGRC) metal-oxide-semiconductor field effect transistor (MOSFET) as a biosensor for early-stage disease diagnostics. The key parameters such as sensitivity, switching ratio, and threshold voltage shift have been compared with the conventional MOSFET. For immobilizing the protein molecules, a cavity has been embedded in the gate insulator region due to which gate capacitance changes owing to the accumulation of protein molecules which reflects the deviation in threshold voltage. Higher sensitivity (1.542) is achieved for protein at a very low drain bias (0.2 V) in comparison to streptavidin and APTES ((3-Aminopropyl) triethoxysilane). Moreover, the cavity gap variation (from 8 to 15 nm) and oxide thickness limitation has also been observed for the device as a biosensor. All the results pave way for early detection techniques of protein-related diseases such as Alzheimer's diseases, ovarian cancer and coronary artery disease with the existing complementary metal oxide semiconductor (CMOS) technology.

1. Introduction

According to medical science, prompt detection of any disease mainly cancer is valuable for the survival of patients. Numerous methods have developed for detection of the biomolecule, such as the enzyme-linked immunosorbent assay [1], Alzheimer's disease, ovarian cancer, type 2 diabetes, and coronary artery disease. Though, many of them are complicated and time-consuming due to labeling practices [2]. Field effect transistor (FET) based biosensors have gained a lot of attention since past few years owing to high-scalability, high sensitivity, rapid electrical detection, low power consumption, direct electrical readouts, low-cost mass production as compared with other devices, including surface Plasmon resonance [3], microcantilevers [4], and an array of fluorescence sensors [5]. Low-cost, highly sensitive, reliable, user-friendly quick diagnostic bio-sensing devices are essential for different biological and biomedical applications [6]. To overcome the difficulties of conventional health diagnostic methods, nanotechnology-based biosensor devices are used [7–9].

Moreover, the development of semiconductor technology advanced to shrink the MOSFET dimensions for the nanoscale regime to provide high packing density with the high-speed integrated circuit. However, in an ultra-scaled device, the influence of short channel effects (SCEs) deeply affects the device performance [10]. Several device engineering schemes and device structures have been reported in the literature [11–13] to overcome SCEs. Recessed Channel (RC) MOSFET is considered as the most promising one since it overcomes almost all of the SCEs and is also feasible with CMOS technology. It has been demonstrated in previous work [14,15] when ITO (Indium Tin Oxide) [16,17] is amalgamated onto RC MOSFET; gate controllability enhances significantly owing to a very low resistivity (10^{-5} Ω-cm) with high mobility (53.5 $cm^2 V^{-1}s^{-1}$) [17].

Therefore, in this paper, for the first time, TGRC-MOSFET is introduced as a biosensor. A biosensor is used to sense biological elements, attaching the sensitivity and binding specificity of biologics such as enzymes, proteins, nucleotides, and antibodies. In this proposed TGRC-MOSFET as a protein biosensor, the channel potential of the device is influenced by the electrical properties of biomolecules. The proposed biosensor can also be used as APTES based sensor owing to high sensitivity to diagnose early stage type 2 diabetes using alpha-hydroxybutyrate (α-HB or ABH) detection [18]. In conventional MOSFET, the current flows in the channel when gate voltage exceeds the threshold voltage (VTH), and it can be modulated by the dielectric constant which is due to biomolecule immobilization below the gate electrode because threshold voltage depends upon gate capacitance. In TGRC-MOSFET, in the gate insulator region, a nano-cavity is embedded for immobilizing the biomolecules. The electrical characteristics are

* Corresponding author.
E-mail addresses: ajaykumar@dtu.ac.in (A. Kumar), mmtripathi@dce.ac.in (M.M. Tripathi), chaujar.rishu@dtu.ac.in (R. Chaujar).

https://doi.org/10.1016/j.vacuum.2019.02.054
Received 10 July 2018; Received in revised form 18 February 2019; Accepted 28 February 2019
Available online 05 March 2019
0042-207X/

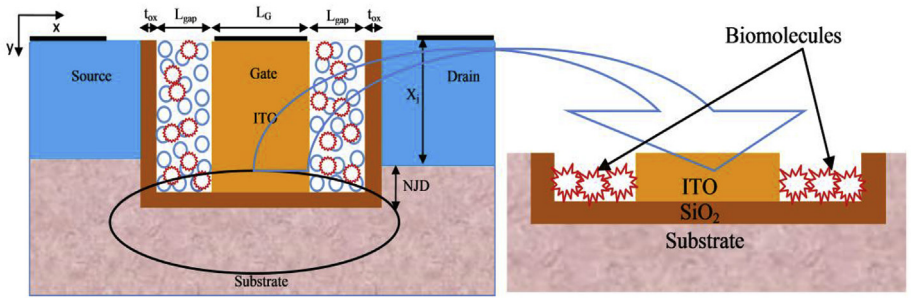


Fig. 1. Schematic structure of TGRC-MOSFET as a biosensor.

altered due to the absorption of biomolecules and due to which the sensitivity of sensor changes. The biomolecules which are absorbed in the Nano-cavity gap changes the dielectric constant (k) of the gap which alters VTH of the device which then serves as a key parameter to estimate the sensitivity of marker.

2. Device structure and its parameters

The device structure for TGRC-MOSFET considered in this work is shown in Fig. 1. The difference between nano cavity-gap implanted TGRC-MOSFET and TGRC-MOSFET involves the nano cavity-gap (L_{gap}) at the edge of the gate dielectric where the biomolecules are accumulating. Here, L_{gap} is the length of the Nano-gap cavity (8 nm), t_{ox} is the oxide thickness (2 nm), and L_G is the gate length (30 nm). The source and drain regions are highly doped with an n-type impurity of $5 \times 10^{19}\,cm^{-3,}$ and the substrate is doped with a p-type impurity of $1 \times 10^{17}\,cm^{-3}$ as shown in Fig. 1. Negative Junction Depth (NJD) is taken as 10 nm, gate bias (V_{gs}) is 0.7 V and drain bias (V_{ds}) is 0.2 V. Gate workfunction of TGRC-MOSFET (Φ_{ITO}) is 4.7eV, and the thickness of ITO is 38 nm. The absorption of different biomolecules is modeled by introducing insulator with dielectric constant same as that of a particular biomolecule in the Nano-gap cavity. In this work, we have studied the behavioural change in MOSFET's electrical characteristics when biomolecule is absorbed in nanogap cavity. Since this analysis is based on simulation, we have chosen dielectric constant without any impurity same as that of particular biomolecule in real time environment. Hence, any signal produced by the impurity of same dielectric constant as the biomolecule theoretically has been ignored. Moreover, when this device is used in medical applications, then the actual biomolecule is taken instead of dielectric constant. Therefore, the signal produced would be only due to absorption of biomolecules. This is the reason for not using complex dielectric constant. Further, the unfilled cavity (i.e. no biomolecules is present) is modeled by using an insulator having dielectric constant k = 1 and dielectric constant is taken greater than unity for the detection of different biomolecules such as streptavidin (k = 2.1) [19], biotin (k = 2.63) [20], 3-aminoppropyltriethoxysilane (APTES) (k = 3.57) [18] and protein (His61) (k = 8) [21,22]. Streptavidin-biotin is used to detect Marek's disease virus (MDV) using enzyme-linked immunosorbent assay (ELISA) method [23] while APTES functions as a facilitator to immobilize biomolecules on the surface in the detection process of dengue virus [24].

3. Simulation methodology and calibration

For TCAD simulations, various models have been taken into effect such as, for mobility of carriers under the influence of changing electric field, we have included Parallel Electric Field Dependence (fldmob model) [25]. The model takes care of all the parameters affecting the mobility of carriers including velocity saturation effect. To predict the behavior of the device undergoing immobilization, it is crucial to model the movement of carriers accurately. For carrier generation-recombination, we have implemented (klasrh model) [25] concentration-dependent Klaassen Shockley-Read-Hall Recombination model as it can include a concentration-dependent lifetime of carriers [25]. The above-selected models account for almost the entire device physics associated with the MOSFET, thereby producing precise results. During the measurement, gate bias is swept from 0 to 0.7 V.

To validate the simulation models, both the experimental statistics [26] and modeled data [27] have been drawn-out. Thus, the experimental data [26] and simulated data is calibrated and plotted as evident in Fig. 3(a) for 140 nm gate length. Hence, we have approximated the corner effect [28] and find out that the error ($\Delta\varepsilon/L_{eff}$) < 0.6% which is negligible as depicted in Fig. 2(a). Moreover, the simulated models have been calibrated with modeled data [27] which is almost matched as evident from Fig. 2(b), thus reflecting the validity of simulation models.

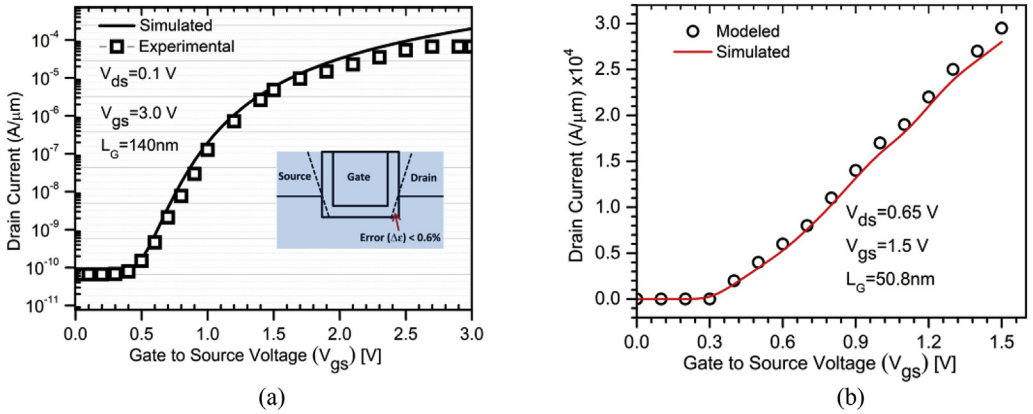


Fig. 2. (a) Experimental and simulation of I_{ds}-V_{gs} characteristics of 140 nm gate length grooved gate (recessed channel) MOSFET. (b) Modeled and simulation of I_{ds}-V_{gs} characteristics of 50.8 nm gate length recessed channel MOSFET.

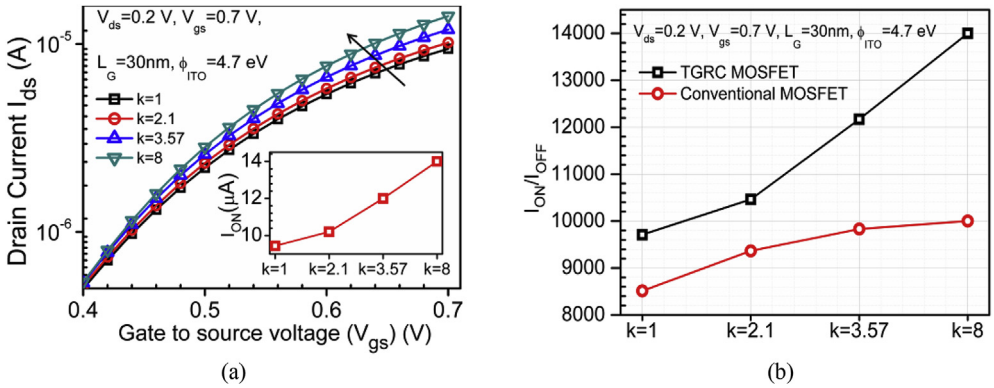


Fig. 3. (a) Transfer characteristics, Inset: ON-current of Nano-gap embedded TGRC-MOSFET and (b) Switching ratio (I_{ON}/I_{OFF}) of Nano-gap embedded TGRC-MOSFET and conventional MOSFET in the presence of biomolecules.

4. Results and discussion

It can be observed from Fig. 3(a), when the biomolecules are immobilized (k > 1) in the Nano-gap cavity, ON-current (shown in inset) rises significantly (at V_{gs} = 0.7 V) in comparison to the absence of biomolecule (k = 1) owing to an increased dielectric constant which increases the gate control. Therefore, the switching ratio (I_{ON}/I_{OFF}) also increases with a dielectric constant (streptavidin, APTES, and protein respectively) as compared to air (unfilled) in the proposed device as compared to conventional MOSFET due to amalgamation of ITO as a gate material (shown in Fig. 3(b)). Thus, the change in drain current, enhancement in I_{ON} and switching ratio for a particular biomolecule can be used as a key parameter to detect/sense the specific biomolecule. The threshold voltage is used for detection purpose as a sensing parameter, and it is directly related to the dielectric constant. Threshold voltage defines the specific gate voltage at which drain current is equal to 10^{-7} (A/μm) in this work. The threshold voltage enhances as the related dielectric constant of the biomolecule is increased, and the same results are observed for TGRC-MOSFET in which threshold voltage increases with dielectric constant, as shown in Fig. 4.

High threshold voltage shift (ΔV_{TH}) of 9.7 mV, 21.3 mV, and 34.1 mV is observed in TGRC device while low ΔV_{TH}; 2 mV, 5 mV, and 9 mV is observed in conventional MOSFET when streptavidin, APTES, and protein respectively are immobilized in the Nano-gap cavity in comparison to unfilled Nano-gap cavity as reflected in Fig. 4.

In this work, the sensitivity (S) parameter is defined as the ration of I_{ON} when the biomolecule is present to the I_{ON} when biomolecule is absent-

$$S = \frac{I_{ON}(k > 1)}{I_{ON}(k = 1)} \quad (1)$$

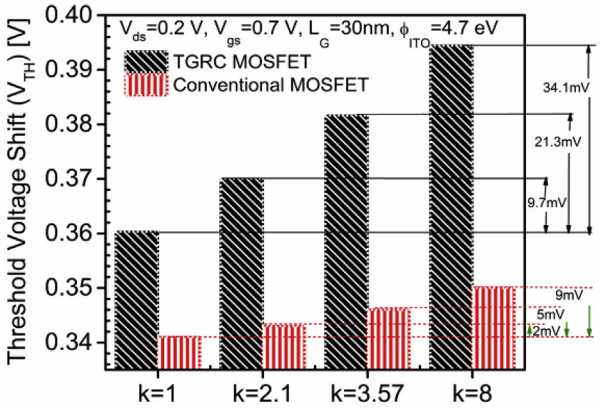


Fig. 4. Threshold voltage shifts for different biomolecules in TGRC-MOSFET and conventional MOSFET.

Fig. 5(a) shows the sensitivity [29] of TGRC-MOSFET and conventional MOSFET. It is evaluated that the sensitivity of TGRC-MOSFET enhanced by 19.85%, 27.9% and 32.93% for streptavidin, APTES, and protein respectively as compared to conventional MOSFET. The enhancement in sensitivity is due to the increment in ON current as well as switching ratio (shown in Fig. 3(a) and (b)).

Fig. 5(b) showed the sensitivity of protein and compared with streptavidin and APTES on different drain bias in TGRC-MOSFET biosensor. It is indicated in Fig. 5 that this device is highly sensitive to low drain bias and less sensitive to higher drain bias. From the figure, it is also evident that the sensitivity is comparatively higher for the protein biomolecules owing to a high dielectric constant at lower drain bias (0.2 V at constant V_{gs} = 0.7 V) as compared to streptavidin and APTES. Thus, TGRC-MOSFET is also applicable for low power ultra-sensing applications in Alzheimer's disease, ovarian cancer, and coronary artery disease diagnosis.

Also, the electrical performance of TGRC-MOSFET biosensor is also examined in terms of surface potential as shown in Fig. 6(a). Under the cavity region, the deformation of potential appears (effectively at drain end). When biomolecules are immobilized in the cavity, the change in potential is observed due to the change in dielectric constant of biomolecules. Hence, the shift in potential can detect the presence of biomolecules in the cavity region. Contour plots of surface potential clearly show the change in potential when biomolecules are immobilized in the Nano-cavity as shown in Fig. 6(b).

Fig. 7 reflects the energy band profile in terms of conduction band energy, valence band energy and electron Quasi-Fermi level (QFL). When the biomolecules are immobilized in the Nano-gap cavity, then the change in conduction band energy and valence band energy is evident as shown in Fig. 7(a) and (b). The shift in energy band is more prominent for protein (k = 8) while less prominent for streptavidin and biotin biomolecules in comparison to the case of absence [30] of biomolecules as reflected in Fig. 7(a) and (b). Contour plots of QFL in the presence of biomolecule are shown in Fig. 7(c). The change in QFL can be observed in the contours plot, by which it can be detected the kind of biomolecule present in the Nano-gap cavity of TGRC-MOSFET. Thus, TGRC can also be used as a low power sensing device due to effective change in energy band profiles at low drain bias (0.2 V) for protein biosensor to diagnose the Alzheimer's disease, ovarian cancer, and coronary artery diseases.

Moreover, it is also observed in Fig. 8(a) that, the electron temperature is high when the protein molecules are immobilizing, and the change in temperature is more prominent for protein while less prominent for streptavidin and APTES molecules as evident from Fig. 6(a). Contours plot represent how the temperature varies when the biomolecules come into the Nano-gap cavity, as shown in Fig. 8(b). With the

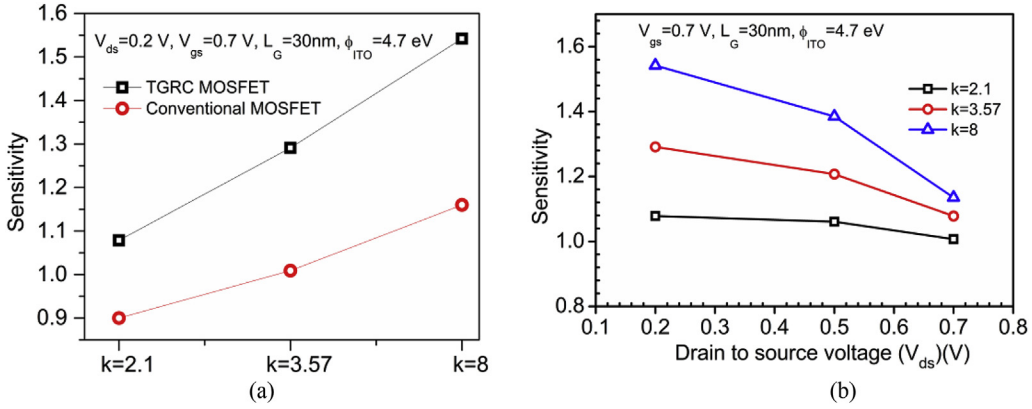


Fig. 5. (a) Comparative study of sensitivity between TGRC-MOSFET and conventional MOSFET for various biomolecules. (b) Impact on sensitivity variation of the various biomolecules at different drain voltages for TGRC-MOSFET.

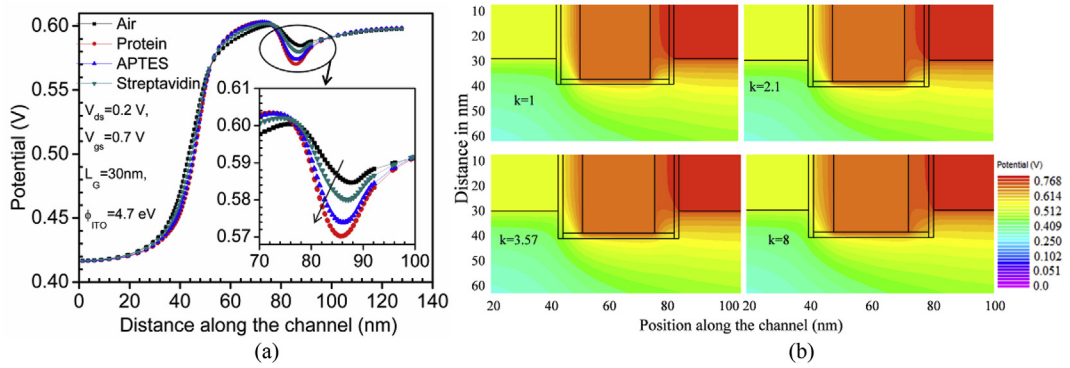


Fig. 6. (a) Effect on surface potential in the presence of biomolecules along the channel from source to drain in TGRC-MOSFET. (b) Contour plot of surface potential in the presence of biomolecules (for k = 1, 2.1, 3.57 and 8) along the channel from source to drain in TGRC-MOSFET.

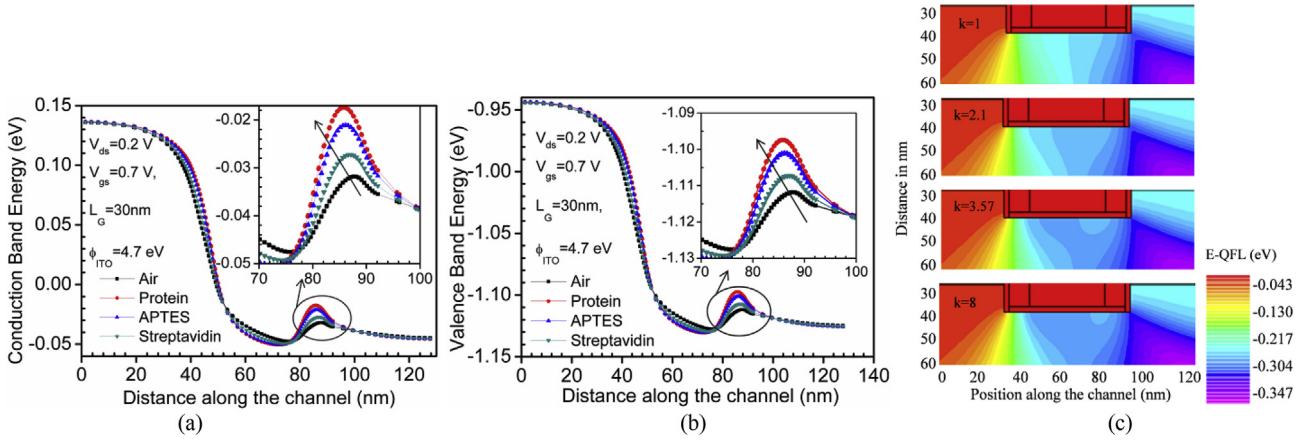


Fig. 7. Effect on energy bands: (a) Conduction band, (b) Valence band and (c) contour plot of electron Quasi-Fermi Level (QFL) in eV, along with the channel in the presence of biomolecules in TGRC-MOSFET.

change in temperature, change in dielectric constant can detect/sense about which biomolecules are present. Thus, TGRC-MOSFET is a promising candidate as a protein biosensor which can be detect the associated protein diseases and provides more efficient therapies (such as Alzheimer and ovarian cancer therapy).

4.1. Effect of parasitic capacitances

The presence of biomolecule can be easily observed by the change in stray capacitances because the stray (parasitic) capacitances of a field effect transistor are altered by changing the dielectric constant. From Fig. 9(a), it is observed that the gate to source capacitance (C_{gs}) is altered (increased) by altering (increasing) the corresponding dielectric constant of streptavidin, APTES, and protein in comparison to air. Similarly, the gate to drain capacitance (C_{gd}) and gate capacitance (C_{gg}) are altered in the presence of air, streptavidin, APTES, and protein as shown in Fig. 9(b) and (c). When the protein molecules are immobilizing, then the change in capacitance is more prominent for protein while less prominent for streptavidin and APTES molecules as compared to air as evident from Fig. 9(a), (b) and (c).

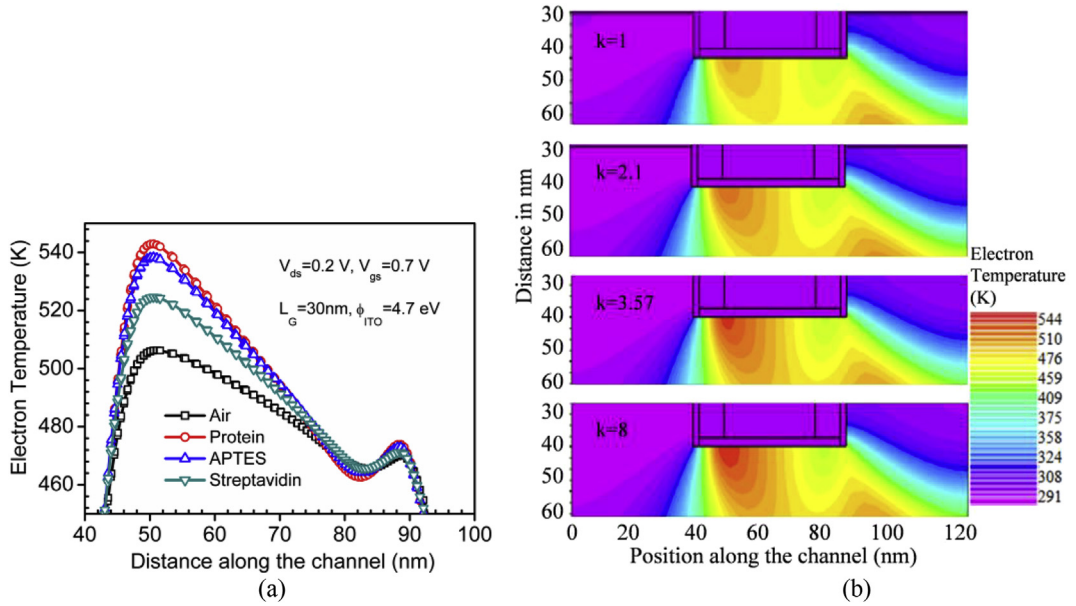


Fig. 8. (a) Effect on electron temperature along the channel from source to drain and (b) contour plot of electron temperature, in the presence of biomolecules in TGRC-MOSFET.

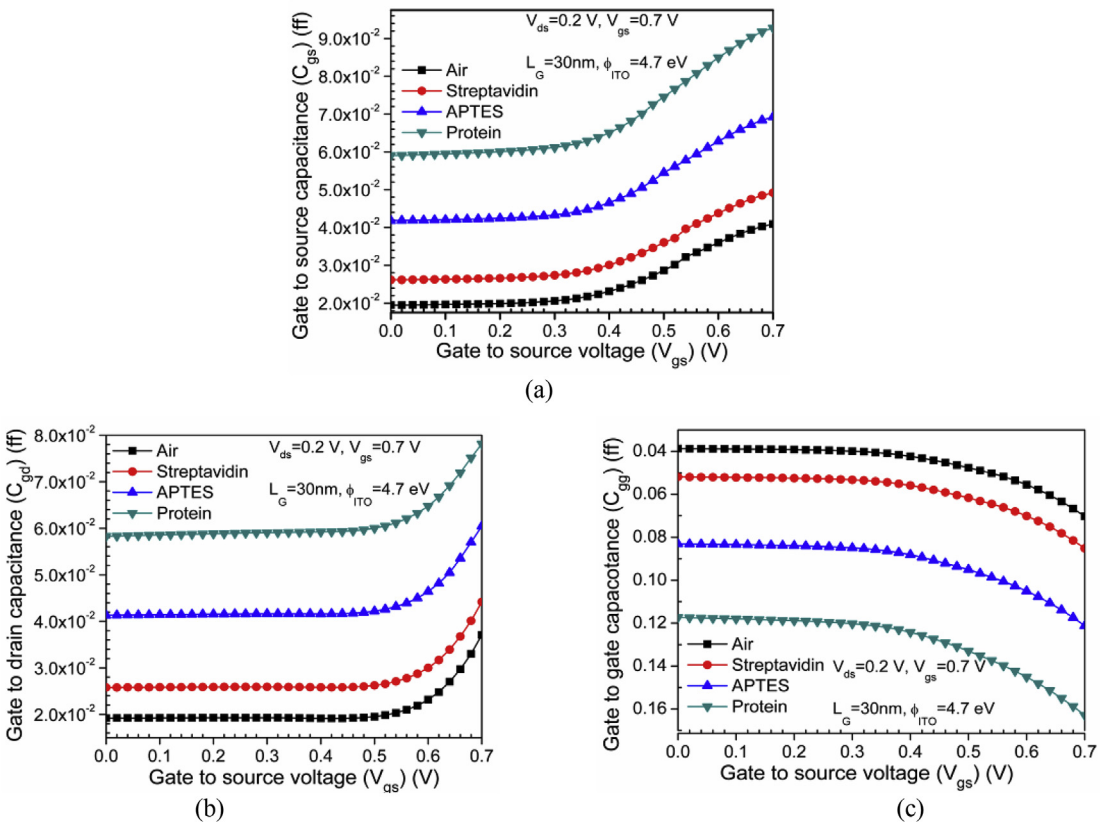


Fig. 9. (a) Effect on parasitic capacitances (a) C_{gs} (b) C_{gd} (c) C_{gg}; in the presence of biomolecules in TGRC-MOSFET.

4.2. Effect of nano-gap cavity length

Moreover, the effect of cavity length (L_{gap}) has also been observed in this work with an aim to investigate the sensitivity at different L_{gap} of the biosensor. Fig. 10(a) shows the impact of L_{gap} variation on I_{ON}, and it is observed that I_{ON} increases for streptavidin, APTES, and protein as compared to air for a particular L_{gap} (8 nm, 10 nm, and 15 nm) but I_{ON} reduces when L_{gap} increases from 8 nm to 15 nm.

Similarly, the switching ratio is increased for streptavidin, APTES, and protein respectively as compared to air for a particular L_{gap} reflected in Fig. 10(b). Fig. 10(c) shows the change (reduces) in threshold voltage due to change in L_{gap} (from 8 nm to 15 nm) for air, streptavidin, APTES, and protein respectively. Thus, more prominent change in threshold voltage (due to change in dielectric constant) is used as a sensing parameter for detection of protein molecules. Moreover, the sensitivity of TGRC-MOSFET is also observed with change in L_{gap}, and it

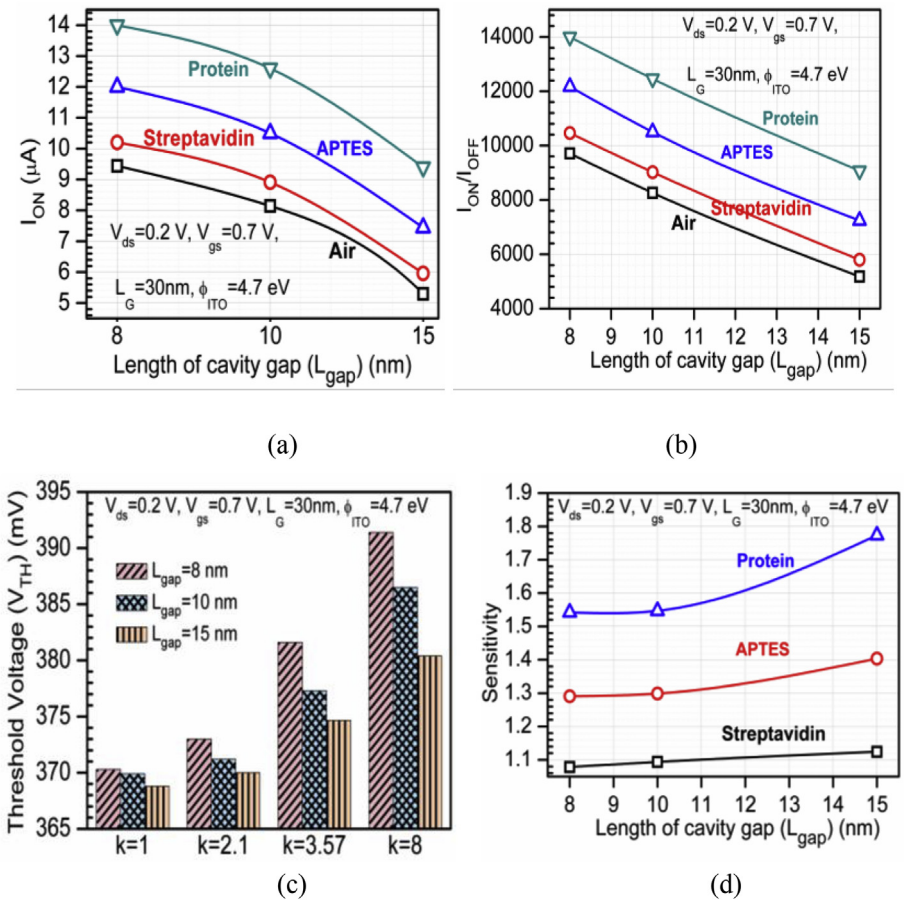


Fig. 10. The impact of length of cavity gap variation on (a) I_{ON}, (b) I_{ON}/I_{OFF}, (c) Threshold voltage, and (d) Sensitivity, for different biomolecules in TGRC-MOSFET.

is found that sensitivity of the device is enhanced significantly with the increase in L_{gap} as shown in Fig. 10(d). From the figure, it is also observed that the sensitivity increases from streptavidin to APTES and APTES to protein (for each L_{gap}). Thus, with L_{gap} = 15 nm, Nano-gap embedded TGRC-MOSFET shows better sensitivity for protein biomolecules in comparison to other biomolecules. Thus, 15 nm cavity-gap length of TGRC MOSFET show optimum performance and hence can be used as a low power, high sensitive biosensor to diagnose various associated diseases.

4.3. Impact of Oxide-thickness: Limit of Detection

In this section, the impact of oxide-thickness (t_{ox}) variation in order to determine the limit of detection has been observed in terms of on-current, switching ratio, threshold voltage and sensitivity in TGRC-MOSFET. In this section, the cavity gap is fixed at 8 nm because; the device gives high performance at 8 nm L_{gap} as a biosensor. Fig. 11(a) shows the impact of t_{ox} variation on $I_{ON,}$ and it is observed that I_{ON} increases for streptavidin, APTES, and protein as compared to air for a particular t_{ox} (2 nm, 4 nm, and 6 nm) but I_{ON} reduces when t_{ox} increases from 2 nm to 6 nm due to higher t_{ox}, gate capacitance (stray capacitance) will be high and thus I_{ON} is reduced.

In the same way, the switching ratio is increased for streptavidin, APTES, and protein respectively as compared to air for a particular t_{ox} reflected in Fig. 11(b). Fig. 11(c) shows the change (reduced) in threshold voltage due to change in t_{ox} (from 2 nm to 6 nm) for air, streptavidin, APTES, and protein respectively. Thus, more prominent change in threshold voltage (due to change in dielectric constant) is used as a sensing parameter for detection of biomolecules. Moreover, the sensitivity of the proposed device is also observed for different $t_{ox,}$ and it is observed that the sensitivity of the device is reduced with the increase in t_{ox} as shown in Fig. 11(d) and maximum at 2 nm t_{ox} due to higher I_{ON}. Thus, 2 nm oxide-thickness of TGRC device show optimum performance and hence can be used as a low power, high sensitive biosensor. From the results, it is also concluded that there is a detection limit of up to 4 nm oxide thickness; and beyond this limit, the device is not suitable for bio-sensing applications due to higher reduction in I_{ON} and sensitivity.

5. Conclusion

This work investigated the performance metric of highly sensitive ultra-low power TGRC-MOSFET as a biosensor. The working principle of TGRC-MOSFET based biosensor for electrical detection of biomolecules has also been investigated in terms of energy band, threshold voltage, electron-QFL, electric field, surface potential, and drain current. The sensitivity factor is improved by 32.93% as compared to conventional MOSFET at low drain bias voltage (0.2 V). Due to higher sensitivity at low drain bias, all the parameters have been investigated at 0.2 V drain voltage for protein molecules and simultaneously compared with other biomolecules such as streptavidin, APTES and also in the absence of molecules (air). Further, the efficacy of cavity gap length and oxide thickness variation is also examined in terms of $I_{ON,}$ switching ratio, $V_{TH,}$ and sensitivity of the proposed biosensor. Thus, TGRC-MOSFET biosensor proves to be a favorable device for the sensing applications as compared to conventional MOSFET based biosensor owing to its high sensitivity and low power electrical detection property which is useful for early diagnosis of deadly diseases and could improve the health of at-risk populations worldwide.

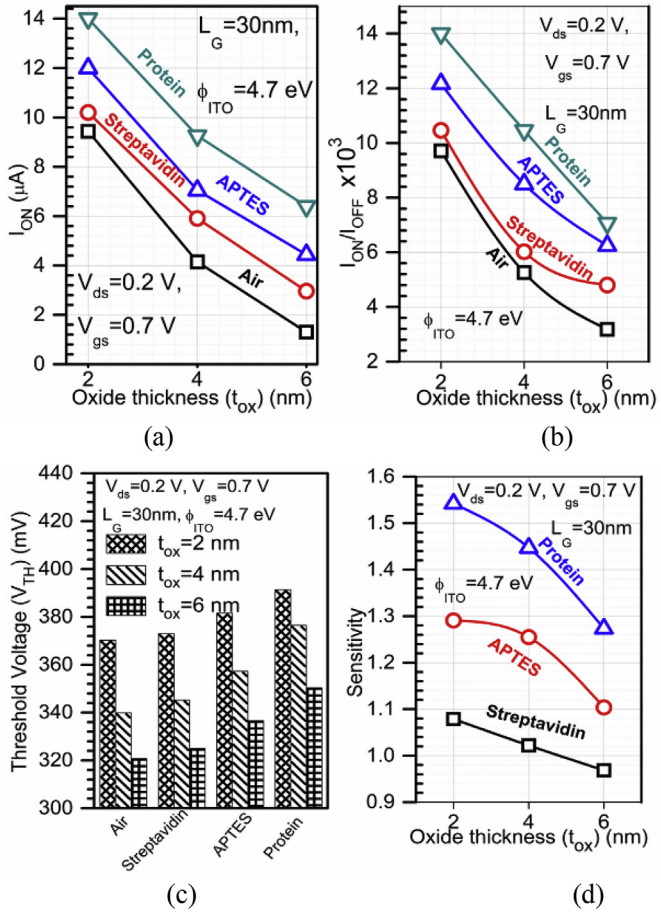


Fig. 11. The impact of oxide-thickness variation on (a) I_{ON}, (b) I_{ON}/I_{OFF}, (c) Threshold voltage, and (d) Sensitivity, for different biomolecules in TGRC-MOSFET.

Acknowledgment

The authors are thankful to Delhi Technological University and Jaypee Institute of Information Technology to carry out this work.

References

[1] E. Comini, C. Baratto, I. Concina, G. Faglia, M. Falasconi, M. Ferroni, V. Galstyan, E. Gobbi, A. Ponzoni, A. Vomiero, D. Zappa, V. Sberveglieri, G. Sberveglieri, Metal oxide nanoscience and nanotechnology for chemical sensors, Sensor. Actuator. B Chem. 179 (2013) 3–20.

[2] J. Lee, J. Jang, B. Choi, J. Yoon, J.-Y. Kim, Y.-K. Choi, D.M. Kim, D.H. Kim, S.-J. Choi, A highly responsive silicon nanowire/amplifier MOSFET hybrid biosensor, Sci. Rep. 5 (2015).

[3] P. Bergveld, The development and application of FET-based biosensors, Biosensors 2 (1) (1986) 15–33.

[4] S. Sang, Y. Wang, Q. Feng, Y. Wei, J. Ji, W. Zhang, Progress of new label-free techniques for biosensors: a review, Crit. Rev. Biotechnol. 36 (3) (2016) 465–481.

[5] H. Im, X.-J. Huang, B. Gu, Y.-K. Choi, A dielectric-modulated field-effect transistor for biosensing, Nat. Nanotechnol. 2 (7) (2007) 430–434.

[6] X.T. Vu, J.F. Eschermann, R. Stockmann, R. GhoshMoulick, A. Offenhäusser, S. Ingebrandt, "Top-down processed silicon nanowire transistor arrays for biosensing, Phys. Status Solidi 206 (3) (2009) 426–434.

[7] M.M. Azmi, Z. Tehrani, R. Lewis, K.-A. Walker, D. Jones, D. Daniels, S. Doak, O. Guy, Highly sensitive covalently functionalised integrated silicon nanowire biosensor devices for detection of cancer risk biomarker, Biosens. Bioelectron. 52 (2014) 216–224.

[8] J.-H. Ahn, S.-J. Choi, J.-W. Han, T.J. Park, S.Y. Lee, Y.-K. Choi, Double-gate nanowire field effect transistor for a biosensor, Nano Lett. 10 (8) (2010) 2934–2938.

[9] A. Gao, N. Lu, P. Dai, T. Li, H. Pei, X. Gao, Y. Gong, Y. Wang, C. Fan, Silicon-nanowire-based CMOS-compatible field-effect transistor nanosensors for ultra-sensitive electrical detection of nucleic acids, Nano Lett. 11 (9) (2011) 3974–3978.

[10] Z. Ahangari, Performance assessment of dual material gate dielectric modulated nanowire junctionless MOSFET for ultrasensitive detection of biomolecules, RSC Adv. 6 (92) (2016) 89185–89191.

[11] R.M. Barsan, "Analysis and modeling of dual-gate MOSFET's," *Electron Devices*, IEEE Transactions on 28 (5) (1981) 523–534.

[12] N. Gupta, R. Chaujar, Optimization of high-k and gate metal workfunction for improved analog and intermodulation performance of Gate Stack (GS)-GEWE-SiNW MOSFET, Superlattice. Microst 97 (2016) 630–641.

[13] N. Gupta, A. Kumar, R. Chaujar, Impact of Channel Doping and Gate Length on Small Signal Behaviour of Gate Electrode Workfunction Engineered Silicon Nanowire MOSFET at THz Frequency, (2014), pp. 192–196.

[14] A. Kumar, M. Tripathi, R. Chaujar, Reliability issues of In2O5Sn gate electrode recessed channel MOSFET: impact of interface trap charges and temperature, IEEE Trans. Electron Devices 65 (2018) 860–866.

[15] A. Kumar, N. Gupta, R. Chaujar, Analysis of novel transparent gate recessed channel (TGRC) MOSFET for improved analog behaviour, Microsyst. Technol. 22 (11) (2016) 2665–2671.

[16] T. Minami, Y. Takeda, S. Takata, T. Kakumu, Preparation of transparent conducting In4Sn3O12 thin films by DC magnetron sputtering, Thin Solid Films 308 (1997) 13–18.

[17] T. Minami, Transparent conducting oxide semiconductors for transparent electrodes, Semicond. Sci. Technol. 20 (4) (2005) S35.

[18] P.K. Sarswat, Y.K. Mishra, M.L. Free, Fabrication and response of alpha-hydroxybutyrate sensors for rapid assessment of cardiometabolic disease risk, Biosens. Bioelectron. 89 (2017) 334–342.

[19] S. Busse, V. Scheumann, B. Menges, S. Mittler, Sensitivity studies for specific binding reactions using the biotin/streptavidin system by evanescent optical methods, Biosens. Bioelectron. 17 (8) (2002) 704–710.

[20] A. Densmore, D.-X. Xu, S. Janz, P. Waldron, T. Mischki, G. Lopinski, A. Delâge, J. Lapointe, P. Cheben, B. Lamontagne, Spiral-path high-sensitivity silicon photonic wire molecular sensor with temperature-independent response, Opt. Lett. 33 (6) (2008) 596–598.

[21] P. Kukic, D. Farrell, L.P. McIntosh, B. García-Moreno E, K.S. Jensen, Z. Toleikis, K. Teilum, J.E. Nielsen, Protein dielectric constants determined from NMR chemical shift perturbations, J. Am. Chem. Soc. 135 (45) (2013) 16968–16976.

[22] S. Kim, D. Baek, J.-Y. Kim, S.-J. Choi, M.-L. Seol, Y.-K. Choi, A transistor-based biosensor for the extraction of physical properties from biomolecules, Appl. Phys. Lett. 101 (7) (2012) 073703.

[23] I. Davidson, M. Malkinson, C. Strenger, Y. Becker, An improved ELISA method, using a streptavidin-biotin complex, for detecting Marek's disease virus antigens in feather-tips of infected chickens, J. Virol Methods 14 (3–4) (1986) 237–241.

[24] G.-J. Zhang, L. Zhang, M.J. Huang, Z.H.H. Luo, G.K.I. Tay, E.-J.A. Lim, T.G. Kang, Y. Chen, Silicon nanowire biosensor for highly sensitive and rapid detection of Dengue virus, Sensor. Actuator. B Chem. 146 (1) (2010) 138–144.

[25] I. SILVACO, ATLAS User's Manual vol. 5, (2011) Santa Clara, CA, Ver.

[26] M. Xiao-Hua, H. Yue, S. Bao-Gang, G. Hai-Xia, R. Hong-Xia, Z. Jin-Cheng, Z. Jin-Feng, Z. Xiao-Ju, Z. Wei-Dong, Fabrication and characterization of groove-gate MOSFETs based on a self-aligned CMOS process, Chin. Phys. 15 (1) (2006) 195.

[27] S. Sreelal, C. Lau, G. Samudra, Parasitic capacitance characteristics of deep sub-micrometre grooved gate MOSFETs, Semicond. Sci. Technol. 17 (3) (2002) 179.

[28] R. Chaujar, R. Kaur, M. Saxena, M. Gupta, R. Gupta, Laterally amalgamated DUal material GAte concave (L-DUMGAC) MOSFET for ULSI, Microelectron. Eng. 85 (3) (2008) 566–576.

[29] A. Kumar, M.M. Tripathi, R. Chaujar, Ultralow-power dielectric-modulated nanogap-embedded sub-20-nm TGRC-MOSFET for biosensing applications, J. Comput. Electron. 17 (4) (December 01, 2018) 1807–1815.

[30] A. Kranti, G.A. Armstrong, Engineering source/drain extension regions in nanoscale double gate (DG) SOI MOSFETs: analytical model and design considerations, Solid State Electron. 50 (3) (2006) 437–447.

Microsyst Technol (2017) 23:5867–5874
DOI 10.1007/s00542-017-3348-2

TECHNICAL PAPER

Investigation of parasitic capacitances of In_2O_5Sn gate electrode recessed channel MOSFET for ULSI switching applications

Ajay Kumar[1] · M. M. Tripathi[1] · Rishu Chaujar[2]

Received: 28 February 2017 / Accepted: 28 February 2017 / Published online: 7 March 2017

Abstract This work discusses the capacitance–voltage (C–V) analysis and frequency dependent capacitance of In_2O_5Sn (Tin Oxide) gate electrode Recessed Channel (TGRC) MOSFET with an aim to examine the effectiveness of In_2O_5Sn (Transparent) as a gate material on parasitic capacitance which prominently influences the current driving capability and thus, the switching performance. Moreover, capacitance dependent parameters such as Transconductance Frequency Product (TFP), Energy Delay Product (EDP) and Gain Bandwidth Product (GBP) are also assessed and found that, TFP increases to 6.33 times in comparison to metal gate RC MOSFET owing to a noticeable reduction in parasitic capacitance ($C_{gg} = C_{gs} + C_{gd}$), due to which EDP and GBP also improve considerably and thus reflects its effectiveness in RF amplifiers and receivers. In addition, the effect of parameter variation such as gate length (L_g) and negative junction depth (NJD) of TGRC is also observed, and results reveal that with $L_g = 20$ nm and NJD = 5 nm, TGRC unveils outstanding switching performance which is desirable for low power ULSI applications.

✉ Rishu Chaujar
rishu.phy@dce.edu

Ajay Kumar
ajaykumar@dtu.ac.in

M. M. Tripathi
mmtripathi@dce.ac.in

[1] Electrical Engineering Department, Delhi Technological University, Delhi, India

[2] Engineering Physics Department, Delhi Technological University, Delhi, India

1 Introduction

From past few periods, shrinking of device dimensions is the main driving force towards circuit miniaturization, low cost, and portability (Moore 1975). As the dimensions of CMOS device reduces, scaling of silicon-based MOSFET devices for barrier potential, critical electric field, oxide thickness, the threshold voltage becomes tougher (Iwai 2009). To overcome these limitations, numerous techniques are being proposed by researchers. Some of them include modification on the existing structure and technology; and on the other hand, incorporation of some new material instead of prevailing material (Woerlee et al. 2001). These includes multi-gate MOSFET proposed by (Barsan 1981), SOI MOSFET by (An et al. 2003), GAA MOSFET by (Auth and Plummer 1997), and Silicon Nanowire MOSFET by (Hu et al. 2003, 2004; Gupta et al. 2016) etc., to overcome the scaling problems at nano-regime. However, Recessed Channel (RC) MOSFET (Chaujar et al. 2008) comes into the existence and appreciably eliminated SCEs and HCEs due to the existence of trench channel which separates the source and drain regions. Although RC MOSFET has its own limitations that it hinders the current driving capability, to overcome this limitation, there is need of integrating some engineering scheme onto RC MOSFET. Therefore, In_2O_5Sn (Indium tin oxide) as a gate metal is amalgamated onto RC MOSFET and then TGRC MOSFET (Kumar et al. 2016a, b, c) comes into existence.

As device dimensions go into sub-30 nm range, the parasitic capacitances become more protruding, which thus affects the device performance and makes the device unsuitable for switching and low power applications. As the channel length scales down, the gate control over the channel gets reduced due to the increased source/drain

capacitances (Murali and Meindl 2007). Therefore, there is a need to perform and study the capacitance–voltage (C–V) analysis which is more advantageous over current–voltage analysis (Steinke et al. 2012) to scrutinize the effects of parasitic capacitances on device performance. In this work, for the first time, a highly conducive and transparent material (ITO) is used as a gate electrode in RC MOSFET to analyses the effect of parasitic capacitances (both bias dependent and frequency dependent). ITO (In_2O_5Sn) is made of indium oxide (In_2O_3) and tin oxide (SnO_2), and it needs lowest deposition temperature (Murali and Meindl 2007; Singh et al. 2006). ITO has a high concentration in the order of 10^{21} cm^{-3} and a very low resistivity (10^{-5} Ω-cm) with higher Hall mobility (53.5 $cm^2\ V^{-1}\ s^{-1}$) (Minami 2005). Due to these properties, ITO is frequently used in semiconductor devices, and today silicon-based MOSFET devices having technology less than 30 nm are common. In this work, the bias-dependent parasitic capacitances of TGRC MOSFET are extracted and found that parasitic capacitances are reduced appreciably due to the amalgamation of ITO as a gate electrode (in trenched gate) as compared to the aluminum electrode (CRC MOSFET) at THz frequencies.

Furthermore, the impact of gate length variation and NJD variation has also been observed. The paper is organized as follows: Sect. 2 describes the 3D device structure; and briefs about the simulation models. In Sect. 3, simulation methodology is discussed along with calibration of simulated models. Further, Sect. 4 focused on device comparison in terms of parasitic capacitances and FOMs such as TFP, EDP, and GBP. Also, the effect of gate length and NJD variation on parasitic capacitances of TGRC-MOSFET is examined. Finally, Sect. 5 presents conclusion and its application.

2 Device design and its description

A schematic simulated device i.e. TGRC MOSFET is shown in Fig. 1a. Figure 1b shows the cross-sectional view of TGRC MOSFET with parasitic capacitances. The channel is doped uniformly to 1×10^{17} cm^{-3} (p-type) in both (TGRC and CRC) the devices. The doping in the source and drain region is kept at 5×10^{19} cm^{-3}. The gate length is 30 nm, although total channel length is 54 nm ($L_G + 2t_{ox} + 2NJD$) and thickness of oxide is 2.0 nm as the default device structure parameters of TGRC and CRC MOSFET is shown in Table 1. Figure 1b reflects the parasitic capacitances (C_{gs}, C_{gd}, and C_{gg}) at the gate-source interface, gate-drain interface, and gate–gate interface in the cross-sectional view of TGRC MOSFET.

3 Simulation methodology and calibration

All the results and figure of merits (FOMs) are extracted using ATLAS, a device simulation tool from (Silvaco 2011). The electron and hole currents are calculated by Poisson's equation and the continuity equations. For the simulations, inversion layer Lombardi CVT mobility model has been used due to consideration of temperature variation with accurate results and to allow one to take into account the carrier–carrier scattering, carrier velocity saturation, the influence of the vertical electric field and carrier diffusion at the interface. For minority carrier, Auger recombination model and Shockley–Read–Hall (SRH) recombination are used. In addition, the hydrodynamic energy transport model comprising of the continuity equations and energy balance transport (EBT) model are used to account for non-local transport effects such as

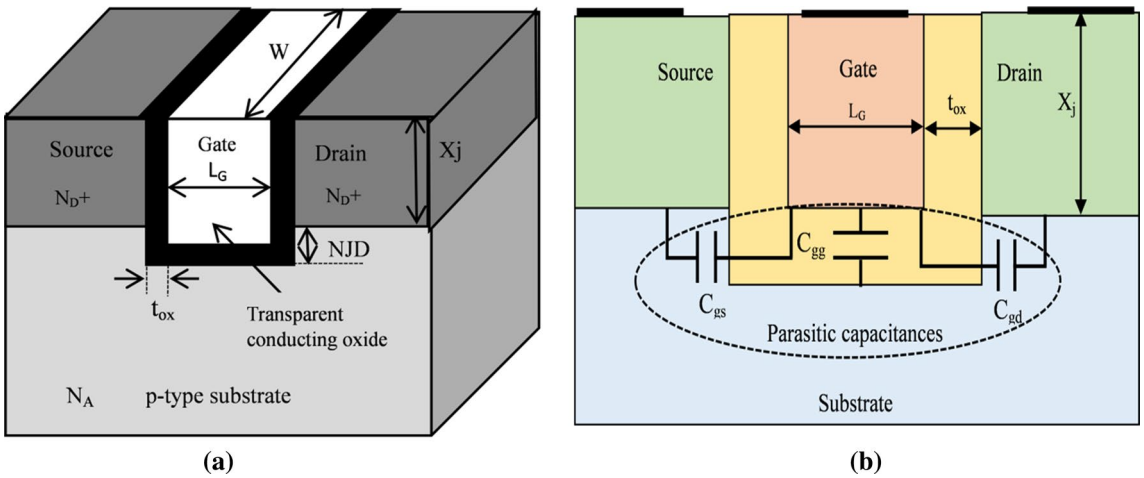


Fig. 1 **a** The schematic simulated structure of TGRC MOSFET. **b** Cross view of THRC MOSFET with parasitic capacitances

Table 1 Default simulated structure parameters of TGRC and CRC MOSFE

Device	TGRC	CRC
Parameters		
Gate length (L_G)	30 nm	
Length of the source and the drain region	30 nm	
Device width (W)	200 nm	
Groove depth	38 nm	
Negative junction depth (NJD)	10 nm	
Substrate doping (N_A)	1×10^{17} cm^{-3}	
Source/drain doping (N_D^+)	5×10^{19} cm^{-3}	
Physical oxide thickness (t_{ox})	2 nm	
Work function	4.7 eV (ITO)	4.2 eV (Al)

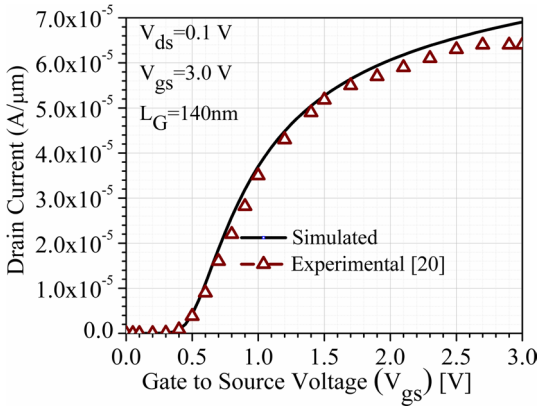


Fig. 2 Experimental and simulation of I_d–V_{gs} characteristics of 140 nm gate length recessed channel MOSFET

diffusion associated with the carrier temperature, velocity overshoot, and the dependence of impact ionization rates on carrier energy distributions (Silvaco 2011). Equations and models used are shown in Table 2.

Where ε = local permittivity; Φ = electrostatic potential; $\rho_{\rightarrow}$ = local space charge density. p = hole concentration; J_p and J_n hole and electron current density respectively. G_p and G_n, are the generation rate for holes and electrons respectively. R_n and R_p are the recombination rate for electrons and holes respectively. q, is the magnitude of the charge on an electron. n/p is the electron/hole concentration. E_{TRAP} is the difference between the trap energy level and the intrinsic Fermi level. τ_n and τ_p, and are the electron and hole lifetimes, respectively. AUGN = 8.3×10^{-32} cm^6/s AUGP = 1.8×10^{-31} cm^6/s. μ_0 is the low-field mobility; υ_{sat}, is the saturation velocity.

In order to authenticate the simulations, the data has been extended (Xiao-Hua et al. 2006) and then plotted as shown in Fig. 2. Model parameters which are used in the simulation have been calibrated according to the experimental results by (Xiao-Hua et al. 2006).

4 Results and discussion

4.1 Impact of In_2O_5Sn on parasitic capacitances

Figure 3a reflects the parasitic capacitances (Kumar et al. 2016c) in terms of gate-source capacitance and gate-drain capacitance. When V_{gs} increases, the accumulation of charge carriers near the gate increases. As a result, the gate-source capacitance and gate-drain capacitance increases. As V_{ds} increases, the pinch-off point moves towards source side, and it leads to accumulation of charges towards source side resulting in an increment of C_{gs}. To maintain the charge neutrality, the charges near the drain decreases and hence C_{gd} decreases as clearly evident from Fig. 3b. It is observed that the value of parasitic capacitances in TGRC device is very less as compared to CRC device as shown in Fig. 3a due to the high conductivity of ITO which shows that applied voltage is a force to charge carriers in current conduction instead of accumulation near the gate (see Fig. 3a, b) and the same trend follows in ref. (Kundu et al. 2014). So higher switching speed is obtained which

Table 2 Used model parameters and equations in simulation (Silvaco 2011; Rahimian and Orouji 2013)

Model	Equation
Poisson's equation	$div(\varepsilon \nabla \phi) = -\rho$
Hole current continuity equation	$\frac{\partial p}{\partial t} = \frac{1}{q} div \vec{J}_p + G_p - R_p$
Electron current continuity equation	$\frac{\partial n}{\partial t} = \frac{1}{q} div \vec{J}_n + G_n - R_n$
SRH recombination	$R_{SRH} = \frac{pn - n_{ie}^2}{\tau_p[n + n_{ie} e^{(-(E_{TRAP}/kT_L))}] + \tau_n[p + n_{ie} e^{(-(E_{TRAP}/kT_L))}]}$
Auger recombination	$R_{Auger} = AUGN(pn^2 - nn_{ie}^2) + AUGP(np^2 - pn_{ie}^2)$
Parallel electric-field-dependent mobility	$\mu(E) = \mu_0 \left[\frac{1}{1 + (\mu_0 E/\upsilon_{sat})^{\beta}}\right]^{1/\beta}$

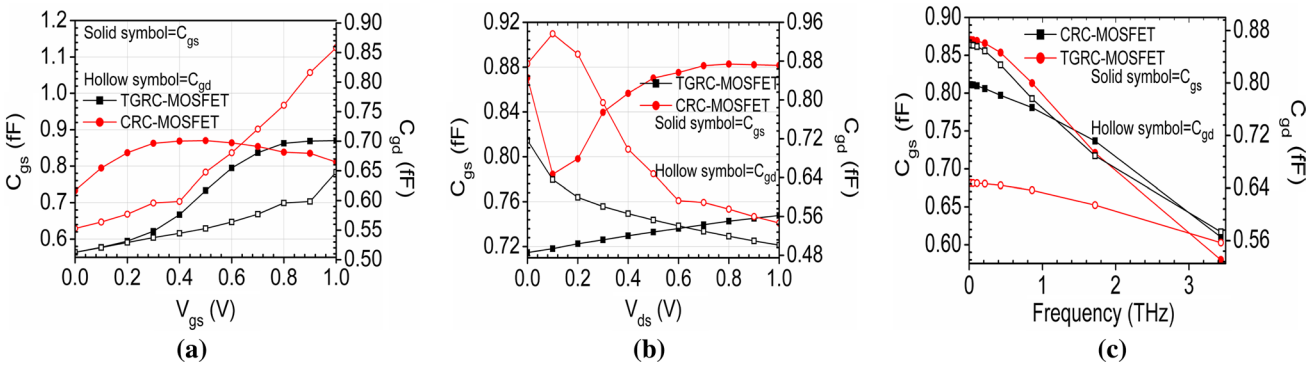


Fig. 3 C_{gs} and C_{gd} as a function of **a** $V_{gs} = 1.0$ V at $V_{ds} = 0.5$ V **b** $V_{ds} = 1.0$ V at $V_{gs} = 0.5$ V **c** frequency at $V_{gs} = 1.0$ V, $V_{ds} = 0.5$ V; of CRC and TGRC MOSFET

also reduces the delay time, making it suitable for the digital applications hence, making TGRC device a promising candidate for switching applications.

Further, the variation of C_{gs} and C_{gd} has also been observed with frequency, and it is clearly reflected from Fig. 3c that when frequency increases to the THz range, then both C_{gs} and C_{gd} reduces. The resultant value of C_{gs} and C_{gd} is very less in TGRC as compared to CRC MOSFET due to the incorporation of ITO as a conducting oxide which indicates the efficacy of transparent material in semiconductor devices for switching applications.

Figure 4a shows the variation of gate capacitance as a function of V_{gs} and V_{ds}. When V_{gs} increases, the accumulation of charges at the gate increases and thus increases the gate capacitance. Moreover, when V_{ds} is increased, the charge carriers near the gate moves towards source side and contributes in drain current thereby lowering the gate capacitance (Marjani and Hosseini 2014) as can be clearly observed in Fig. 4a. It is also noted that, for very high frequency, the gate capacitance is also reduced (3.41%) in TGRC as shown in Fig. 4b. Thus, TGRC device is a suitable device for low power switching applications.

A notable capacitance dependent FOM, transconductance frequency product (TFP) for high-frequency performance is given in Eq. (1). TFP is principally the product of device efficiency and f_T (Kumar et al. 2016b). It signifies a trade-off between bandwidth and power and is used for high-speed designs. Figure 5a shows that TFP is increasing as V_{gs} increases in sub-threshold region (below 0.4 V) and in inversion region, TFP attains a peak value of 650 GHz and with further increase in gate bias, i.e., as biasing go in deep inversion region, TFP falls significantly due to increment in C_{gg} (see Fig. 4a). It is observed that the peak value of TFP is higher in TGRC MOSFET due to the high value of transconductance as reported earlier (Kumar et al. 2016c) and reduction in total gate capacitance (which is the sum of C_{gs} and C_{gd}) in the linear region (see Fig. 3a).

$$TFP = \left(\frac{g_m}{I_d}\right) \times \left(\frac{g_m}{2\pi C_{gg}}\right). \quad (1)$$

Further, energy-delay product (EDP) [given in Eq. (2)] is a valued parameter as far as circuit applications are concerned. It is a measure of energy and is defined by the product of the average energy (E_{ave}) and the gate delay

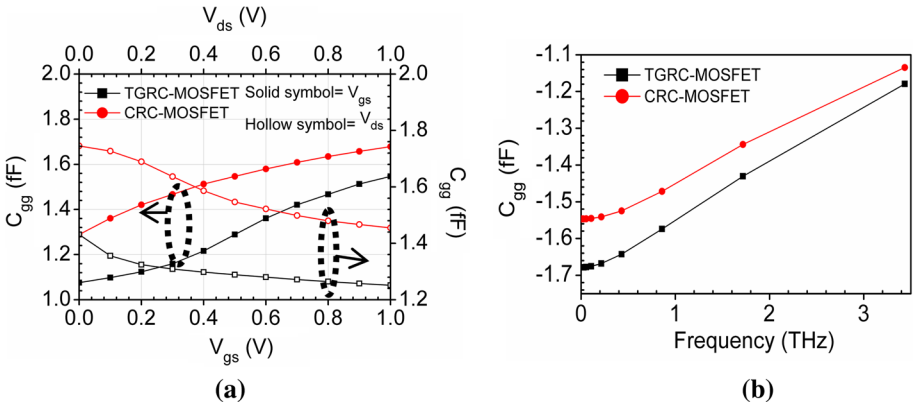


Fig. 4 Gate Capacitance as a function of **a** $V_{gs} = 1.0$ V ($V_{ds} = 0.5$ V) and $V_{ds} = 1.0$ V ($V_{gs} = 0.5$ V) **b** frequency at $V_{gs} = 1.0$ V, $V_{ds} = 0.5$ V; of CRC and TGRC MOSFET

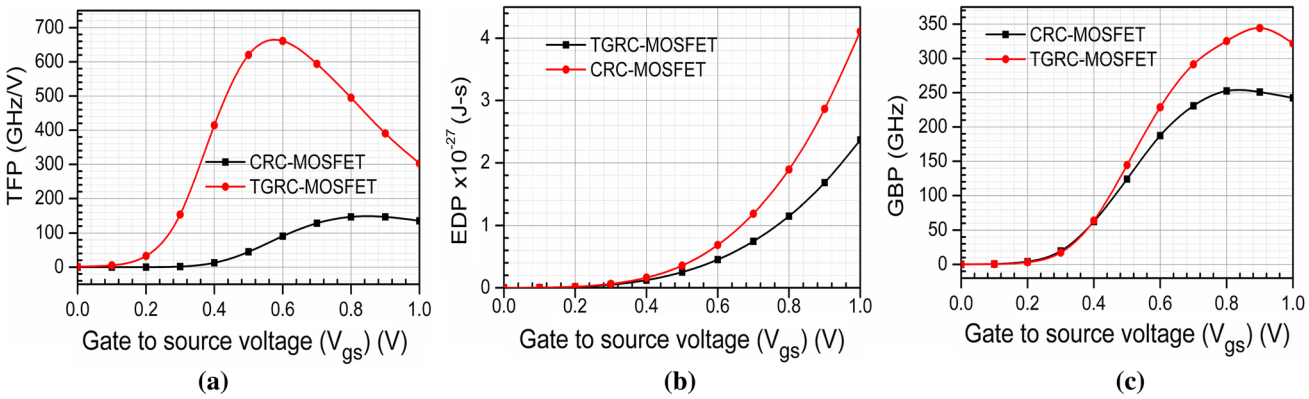


Fig. 5 **a** TFP, **b** EDP, **c** GBP; at $V_{gs} = 1.0$ V, $V_{ds} = 0.5$ V as a function of gate to source voltage for CRC and TGRC MOSFET

(τ). It calculates the energy consumed per switching event (such as in logic families). In TGRC, EDP improves at lower drain bias in comparison to CRC MOSFET as evident from Fig. 5b, due to a reduction in gate capacitance (C_{gg}) and improvement in on-current (Kumar et al. 2016a). In addition, Fig. 5c shows the Gain Bandwidth Product (GBP) [calculated by Eq. (3)] at different drain bias voltage and is a qualitative measure of both gain and bandwidth of a voltage amplifier. It is perceived that GBP improves at higher drain voltage in TGRC device due to a reduction in C_{gd} (see Fig. 3a). GBP peak value indicates the frequency at which the device attains maximum gain.

$$EDP = \left(C_{gg}V_d^2\right) \times \left(\frac{C_{gg}V_d}{I_{on}}\right) \tag{2}$$

$$GBP = \frac{g_m}{2\pi \times 10 \times C_{gd}}. \tag{3}$$

4.2 Impact of gate length (L_G) miniaturization

Furthermore, the impact of parameter variation on the proposed device is studied in terms of the gate length. As evident from Fig. 6a that, when gate length decreases, C_{gs} and C_{gd} decreases as a function of V_{gs}. The similar trend follows in ref. (Cho et al. 2011; Ghosh et al. 2015). When the gate length decreases from 40 to 30 nm, C_{gs} decreases by 8.42% and C_{gd} decreases by 3.03%.

Furthermore, when we reduce the gate length from 30 to 20 nm, then C_{gs} decreases by 9.31%, and C_{gd} decreases by 3.4%. Thus, shrinking the gate length reduces the parasitic capacitances in TGRC MOSFET, which leads to increased circuit density in IC fabrication. As we know that, when V_{ds} increases, the pinch-off point moves towards source side and the number of charge carriers accumulates towards source side. Hence C_{gs} increases and C_{gd} decreases as shown in Fig. 6b. Thereafter, the gate length variation is observed, and it is clearly evident from the figure that as the gate length reduces then, C_{gs} and C_{gd} are also reduced. If we reduce the gate length from 40 to 30 nm, then 4 and 0.98% decrement is observed in C_{gs} and C_{gd}, respectively.

When gate length further reduces from 30 to 20 nm, then 4.28 and 1.59% reduction is observed in C_{gs} and C_{gd}, respectively. Further, the impact of gate length variation on parasitic capacitances is observed for very high frequencies

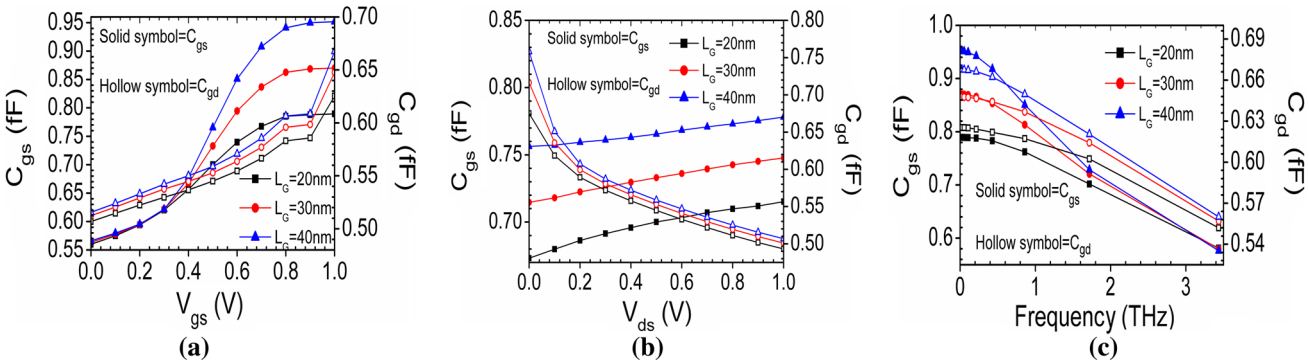


Fig. 6 C_{gs} and C_{gd} as a function of **a** $V_{gs} = 1.0$ V at $V_{ds} = 0.5$ V **b** $V_{ds} = 1.0$ V at $V_{gs} = 0.5$ V **c** frequency at $V_{gs} = 1.0$ V, $V_{ds} = 0.5$ V; of TGRC MOSFET for various gate lengths

(at THz) as shown in Fig. 6c. When the frequency is increased in THz range, and gate length reduces from 40 to 30 nm, then C_{gs} and C_{gd} are reduced by 7.08 and 2.8%, respectively and further 8.2 and 3.5% when gate length varies from 30 to 20 nm. So it is that reduction in parasitic capacitances leads to a device for better switching performances of TGRC MOSFET, as we scale-down the channel length.

Figure 7a reflects the parameter variation of TGRC MOSFET in terms of the gate length. It is evident from figure that gate capacitance increases when V_{gs} is increased (Marjani and Hosseini 2014), and V_{ds} is decreased. As the gate length reduces, and then the gate capacitance is also decreased. If we scale-down the gate length of TGRC MOSFET from 40 to 30 nm, then 7.22 and 2.34% decrement is observed in C_{gg} as a function of V_{gs} and V_{ds}, respectively. If we further scale-down the gate length from 30 to 20 nm, then 7.79 and 4% decrement is reflected in C_{gg} as a function of V_{gs} and V_{ds} respectively. It is also evident from Fig. 7b that, the gate capacitance is also reduced (lower the magnitude) by 6.61 and 7.79% when the gate length scales down from 40 to 30 nm and 30 to 20 nm, respectively at very high frequencies. Therefore, 20 nm gate length device shows that, as we scale-down the device, the parasitic capacitances are reduced, thus making TGRC device a promising device for high-frequency switching applications. Hence, proposed device also leads to increased circuit density in IC fabrication.

Likewise, by scaling down the gate length to 20 nm, TFP and GBP are enhanced while EDP reduces appreciably as is clear from Fig. 8 (Park et al. 1998). This enhancement is due to a reduction in gate capacitance and improvement in I_{on} (see Fig. 3a). EDP is further minimized if TGRC is biased in the linear region in comparison to saturation region owing to reduced supply voltage and capacitance coupling. Whereas in cut-off region, EDP reduces appreciably, as shown in Fig. 8b. This is useful in the field of low power switching applications.

4.3 Impact of variation of negative junction depth (NJD)

Effects of NJD variation on parasitic capacitances have been observed in this section of the proposed device. When NJD is reduced, the number of charge carriers move quickly from source to drain because channel length gets reduced

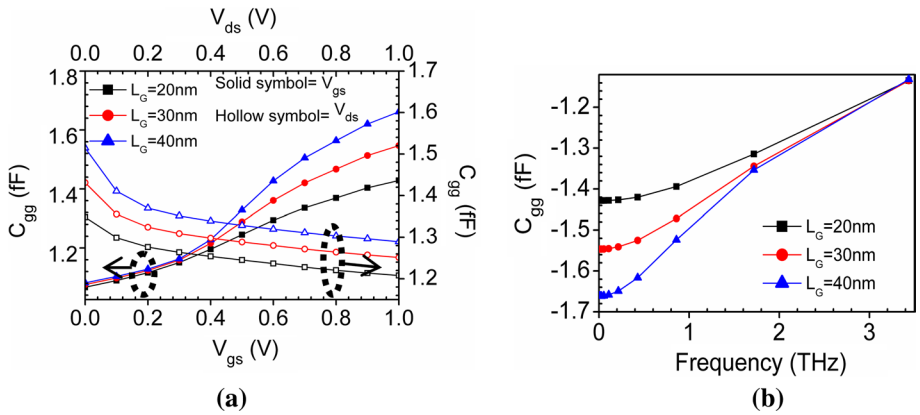


Fig. 7 Gate Capacitance as a function of **a** $V_{gs} = 1.0$ V ($V_{ds} = 0.5$ V) and $V_{ds} = 1.0$ V ($V_{gs} = 0.5$ V) **b** frequency at $V_{gs} = 1.0$ V, $V_{ds} = 0.5$ V; of TGRC MOSFET for various gate lengths

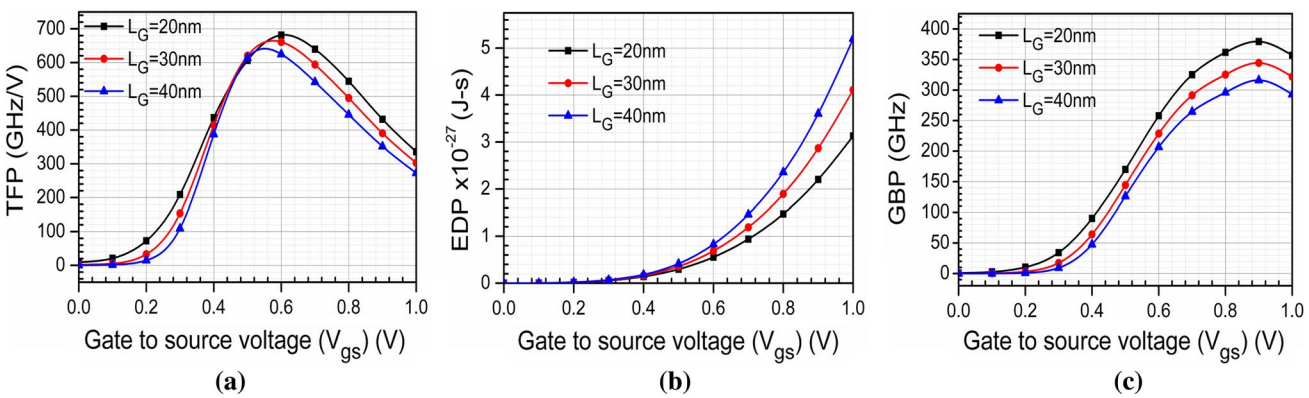


Fig. 8 **a** TFP, **b** EDP, **c** GBP; as a function of $V_{gs} = 1.0$ V ($V_{ds} = 0.5$ V) of TGRC MOSFET for various gate lengths

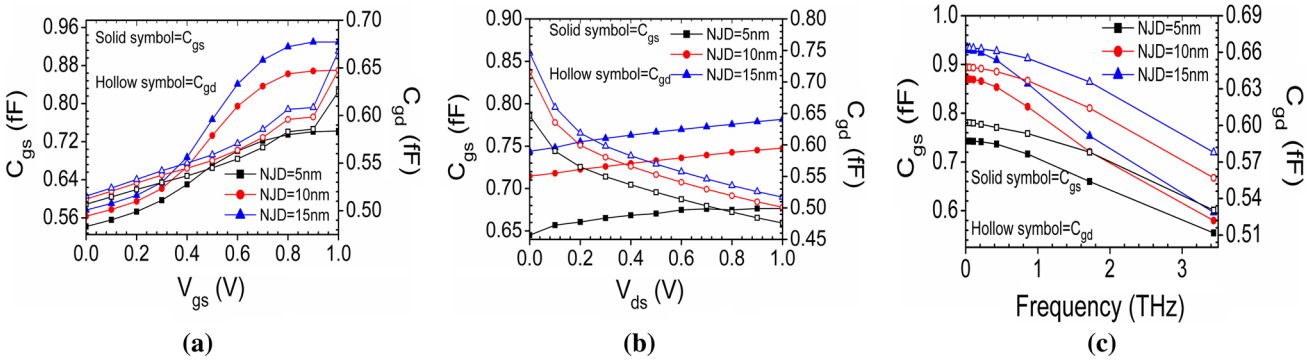


Fig. 9 C_{gs} and C_{gd} as a function of **a** $V_{gs} = 1.0$ V at $V_{ds} = 0.5$ V **b** $V_{ds} = 1.0$ V at $V_{gs} = 0.5$ V **c** frequency at $V_{gs} = 1.0$ V, $V_{ds} = 0.5$ V; of TGRC MOSFET at various NJDs

with the reduction of NJD and the switching time is also reduced making the device operation faster. Figure 9a shows that the decrease in C_{gs} and C_{gd} is reflected when NJD is reduced from 15 to 5 nm, and it is also observed that when V_{gs} increases, the reduction in C_{gs} is enhanced. If NJD is reduced from 15 nm to 10 nm, C_{gs} and C_{gd} is reduced by 7.27 and 1.6%, respectively. Further, reduction in NJD from 10 to 5 nm reduces C_{gs} and C_{gd} by 17.21 and 2.22%, respectively. Similar kind of reduction in parasitic capacitances is observed when V_{ds} is applied, as evident from Fig. 9b. When NJD is reduced from 15 to 10 nm then, C_{gs} and C_{gd} are reduced by 4.4 and 3.1%, respectively. At higher frequencies, C_{gs} and C_{gd} are reduced (by 12.3 and 8.97%) if NJD reduces (from 15 to 10 nm) as reflected from Fig. 9c.

Moreover, the gate capacitance is investigated at different NJDs, and it is observed when V_{gs} and V_{ds} are applied as shown in Fig. 10a. When NJD is reduced from 15 to 10 nm then, C_{gg} is reduced by 4.63 and 4.0% w.r.t V_{gs} and V_{ds}, respectively. Further, NJD reduction from 10 to 5 nm reduces C_{gg} by 13.53 and 8% w.r.t. V_{gs} and V_{ds}, respectively as shown in Fig. 10a. Figure 10b shows a very high reduction in gate capacitance when NJD scales down at THz frequency range. In addition, a decrease in NJD to 5 nm results in an enhancement in TFP and GBP while degrading EDP as shown in Fig. 11 (Park et al. 1998). From Fig. 11b, it is observed that effect of transparent gate scheme strongly affects the EDP. GBP also improves by modulating NJD as reflected in Fig. 11b. It is also found that GBP achieve higher value in saturation mode since C_{gd} is lower in saturation mode [see Fig. 6 (Park et al. 1998)].

5 Conclusion

This work analyzes the capacitance–voltage characteristics of In_2O_5Sn gate electrode recessed channel MOSFET with 30 nm gate length to examine the parasitic capacitances. The simulated results are then used to isolate the parasitic capacitances. The effect of In_2O_5Sn gate electrode (as a transparent gate electrode) in recessed channel MOSFET has been studied in terms of bias and frequency-dependent parasitic capacitances and capacitance dependent FOMs such as TFP, EDP, and GBP for high switching performance. It is observed that with the amalgamation of In_2O_5Sn with RC MOSFET, parasitic capacitances decrease in comparison to aluminum gate metal (CRC MOSFET). When the gate length reduces to 20 nm, then the parasitic capacitances gets reduced, and the overall parasitic capacitances reduce in TGRC architecture by ~25%. Hence, the device is more suitable at sub-20 nm regime. It is also

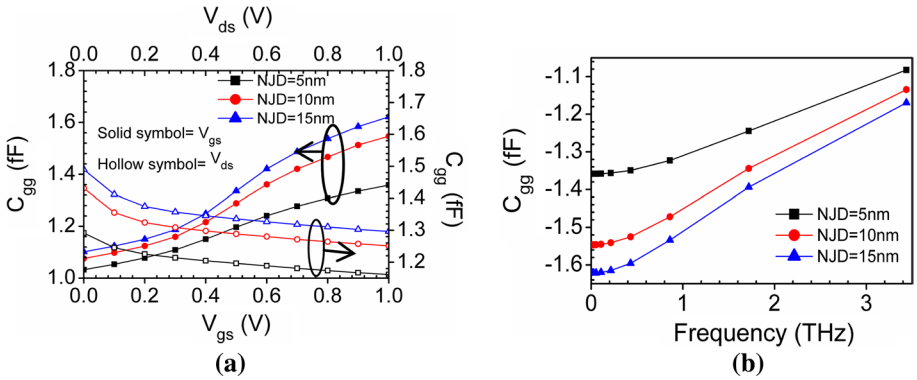


Fig. 10 Gate Capacitance as a function of **a** $V_{gs} = 1.0$ V ($V_{ds} = 0.5$ V) and $V_{ds} = 1.0$ V ($V_{gs} = 0.5$ V) **b** frequency at $V_{gs} = 1.0$ V, $V_{ds} = 0.5$ V; of TGRC MOSFET for various NJDs

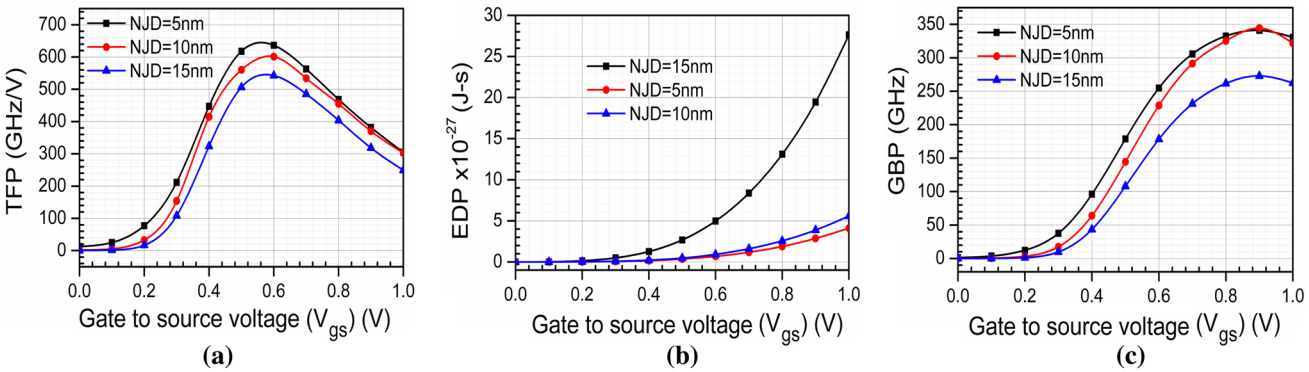


Fig. 11 **a** Transconductance Frequency Product (TFP), **b** Energy Delay Product (EDP), **c** Gain Bandwidth Product (GBP); as a function of $V_{gs} = 1.0$ V ($V_{ds} = 0.5$ V) of TGRC MOSFET for various NJDs

found that with the variation in frequency, parasitic capacitance reduces due to the high current driving capability of TGRC MOSFET; thus, TGRC architecture proves a promising contender for high frequency/switching applications in 22 nm node technology.

Acknowledgements The authors would like to express thankfulness to Microelectronics Research Lab, Department of Engineering Physics and Electrical Engineering Department Delhi Technological University to carry out this work.

References

An X, Huang R, Zhao B, Zhang X, Wang Y (2003) Design guideline of an ultra-thin body SOI MOSFET for low-power and high-performance applications. Semicond Sci Technol 19:347

Auth CP, Plummer JD (1997) Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET's. Electron Device Lett IEEE 18:74–76

Barsan RM (1981) Analysis and modeling of dual-gate MOSFET's. Electron Devices IEEE Trans 28:523–534

Chaujar R, Kaur R, Saxena M, Gupta M, Gupta R (2008) TCAD assessment of gate electrode workfunction engineered recessed channel (GEWE-RC) MOSFET and its multilayered gate architecture—part I: hot-carrier-reliability evaluation. Electron Devices IEEE Trans 55:2602–2613

Cho S, Lee JS, Kim KR, Park B-G, Harris JS Jr, Kang IM (2011) Analyses on small-signal parameters and radio-frequency modeling of gate-all-around tunneling field-effect transistors. Electron Devices IEEE Trans 58:4164–4171

Ghosh S, Koley K, Sarkar CK (2015) Impact of the lateral straggle on the Analog and RF performance of TFET. Microelectron Reliab 55:326–331

Gupta N, Kumar A, Chaujar R (2016) Oxide bound impact on hot-carrier degradation for gate electrode workfunction engineered (GEWE) silicon nanowire MOSFET. Microsyst Technol 22(11):2665–2671

Hu S, Wu Y, Sung C, Chang C, Huang T (2003) Single-electron transistor using self-aligned sidewall spacer gates on silicon-on-insulator nanowire. In: Nanotechnology, 2003. IEEE-NANO 2003. 2003 Third IEEE Conference on. (IEEE, 2003), pp 573–576

Hu S-F, Wu Y-C, Sung C-L, Chang C-Y, Huang T-Y (2004) A dual-gate-controlled single-electron transistor using self-aligned polysilicon sidewall spacer gates on silicon-on-insulator nanowire. IEEE Trans Nanotechnol 3:93–97

Iwai H (2009) Roadmap for 22 nm and beyond. Microelectron Eng 86:1520–1528

Kumar A, Gupta N, Chaujar R (2016a) Analysis of novel transparent gate recessed channel (TGRC) MOSFET for improved analog behaviour. Microsyst Technol 22(11):2665–2671

Kumar A, Gupta N, Chaujar R (2016b) Power gain assessment of ITO based transparent gate recessed channel (TGRC) MOSFET for RF/wireless applications. Superlattices Microstruct 91:290–301

Kumar A, Gupta N, Chaujar R (2016c) TCAD RF performance investigation of transparent gate recessed channel MOSFET. Microelectron J 49:36–42

Kundu A, Koley K, Dutta A, Sarkar CK (2014) Impact of gate metal work-function engineering for enhancement of subthreshold analog/RF performance of underlap dual material gate DG-FET. Microelectron Reliab 54:2717–2722

Marjani S, Hosseini SE (2014) Radio-frequency modeling of square-shaped extended source tunneling field-effect transistors. Superlattices Microstruct 76:297–314

Minami T (2005) Transparent conducting oxide semiconductors for transparent electrodes. Semicond Sci Technol 20:S35–S44

Moore GE (1975) Progress in digital integrated electronics. In: Electron Devices Meeting, pp 11–13

Murali R, Meindl JD (2007) Modeling the effect of source/drain junction depth on bulk-MOSFET scaling. Solid State Electron 51:823–827

Park D, King Y-C, Lu Q, King T-J, Hu C, Kalnitsky A, Tay S-P, Cheng C-C (1998) Transistor characteristics with Ta/sub 2/O/sub 5/gate dielectric. IEEE Electron Device Lett 19:441–443

Rahimian M, Orouji AA (2013) Investigation of the electrical and thermal performance of SOI MOSFETs with modified channel engineering. Mater Sci Semicond Process 16:1248–1256

Silvaco Int. (2016) ATLAS user's manual, ver 5. Santa Clara, CA

Singh V, Suman C, Kumar S (2006) Indium Tin Oxide (ITO) films on flexible substrates for organic light emitting diodes. In: Proc. of ASID, p 388

Steinke DR, Piccirillo J, Gausepohl SC, Vivekand S, Rodgers MP, Lee JU (2012) Parasitic capacitance removal of sub-100 nm p-MOSFETs using capacitance–voltage measurements. Solid State Electron 68:51–55

Woerlee PH, Knitel MJ, Van Langevelde R, Klaassen D, Tiemeijer LF, Scholten AJ, Zegers-van Duijnhoven AT (2001) RF-CMOS performance trends. Electron Devices IEEE Trans 48:1776–1782

Xiao-Hua M, Yue H, Bao-Gang S, Hai-Xia G, Hong-Xia R, Jin-Cheng Z, Jin-Feng Z, Xiao-Ju Z, Wei-Dong Z (2006) Fabrication and characterization of groove-gate MOSFETs based on a self-aligned CMOS process. Chin Phys 15:195

Superlattices and Microstructures 109 (2017) 626–640

Contents lists available at ScienceDirect

Superlattices and Microstructures

journal homepage: www.elsevier.com/locate/superlattices

Effect of trench depth and gate length shrinking assessment on the analog and linearity performance of TGRC-MOSFET

Ajay Kumar

Electrical Engineering Department, Delhi Technological University, Delhi India

ARTICLE INFO

Article history:
Received 21 January 2017
Received in revised form 18 April 2017
Accepted 20 May 2017
Available online 22 May 2017

Keywords:
Analog
Distortions
Linearity
TGRC-MOSFET
Trench gate
Transconductance coefficients

ABSTRACT

This paper discusses the impact of trench depth (Negative Junction Depth (NJD)) and gate length (L_G) shrinking on analog and linearity performance of Transparent Gate Recessed Channel (TGRC) MOSFET with an aim to achieve a reliable and high performance transistor. It is found that device enhances the I_{ON} by 38% and thereby improves the analog performance in terms of transconductance, device efficiency, output resistance, and gain. Moreover, linearity figure of merits are also enhanced at lower gate bias in TGRC MOSFET in comparison to conventional and Conventional Recessed Channel (CRC) MOSFET due to reduced harmonic distortions (g_{m3}). Thus, the improved analog and linearity performance at 5 nm NJD and 20 nm L_G of TGRC-MOSFET makes it suitable for low power linear RF amplifiers as a nano-scaled device. Thus, these results would serve as a worthy design tool for low power and high performance CMOS circuits.

1. Introduction

For RFIC designing and high-frequency applications, CMOS devices are required with low intermodulation distortion to sustain linear operations when working with a weak signal. In modern communication systems, a high linearity is desired so as to exhibit less distortion. Intermodulation (IM) may induce when the system gives nonlinearity performance and generate different frequency signal at outputs compared to input signal frequency. This kind of interference may fall into the band of interest and distorted the desired output [1]. However, sub-nm MOSFET exhibit linear relation but short channel effects (SCEs) hinders its linearity. As the dimensions of the device are reduced, scaling the silicon-based MOSFET devices for barrier potential, critical electric field, oxide thickness, threshold voltage, etc., are becoming hardly increased [2]. To overwhelmed such scaling problems, various device engineering schemes (gate, channel and drain engineering, etc.) and numerous device structures such as multi-gate MOSFET by Barsan in 1981 [3], SOI MOSFET by An et al., in 2003 [4], Conventional Recessed Channel (CRC) MOSFET by Chaujar et al., in 2008 [5], GAA MOSFET by Auth et al., in 1997 [6], and Silicon Nanowire MOSFET by Gupta et al., in 2015 [7] etc., have already been reported in the literature. Among them, RC-MOSFET is most promising for extending the scaling limit of conventional CMOS technology due to tremendous gate controllability, lessened SCEs and ease of fabrication feasibility of RC MOSFET [8]. In CRC-MOSFET, two potential barrier are created at the two corners [9] owing to higher field lines due to which electrons are now required more energy to cross these barriers. Consequently, these barriers bounds device transport efficiency and thus, current driving capability (Ion) reduced. To overwhelm this limitation, there is a need of integration of engineering schemes onto RC MOSFET. Therefore, to enhance the current driving capability and

E-mail address: ajaykumar@dtu.ac.in.

http://dx.doi.org/10.1016/j.spmi.2017.05.045
0749-6036/

improve the device performance for ULSI industry, gate metal engineering scheme is incorporated by some optically transparent and electrically conducting oxides (TCO). TCO is used for different applications in electronic devices due to various properties such as conductivity, thermal stability, transparency, mechanical durability, chemical durability, cost and toxicity [10]. Among all the TCO, indium tin oxide (ITO) has the highest conductivity and very good transparency as well so; it can be used as electrode material in flat panel display. ITO is a compound of In_2O_3 and SnO_2 and it needs lowest deposition temperature as well [11,12]. ITO has a high concentration in the order of 10^{21} cm^{-3} and a very low resistivity (10^{-5} Ω-cm) with higher Hall mobility (53.5 cm^2 $V^{-1}s^{-1}$) [13]. Due to these properties, ITO is frequently used in semiconductor devices and today silicon-based MOSFET devices having technology less than 30 nm are common. Shrinking the device sizes is the driving force towards circuit reduction, low cost, and portability [14]. It is found that the proposed design enhances the device performance in terms of electrical [15,16] and RF performances [17,18].

Therefore, in this work for the first time linearity and harmonic distortions of TGRC-MOSFET has been studied and concurrently compared with CRC MOSFET in terms of Voltage Intercept Point (VIP2, VIP3), IIP3, Distortions (IMD3, HD3) and transconductance and its higher order term (g_{m1}, g_{m3}) using ATLAS 3D device simulator [19]. In addition, effectiveness of geometry dependent parameters such as gate length (L_G) and recessed channel length (NJD) are also examined with an aim to optimize the device parameters so that TGRC MOSFET can be used as highly linear amplifiers with low distortions in communication systems.

2. Device designing and its description

Fig. 1 shows the simulated 3D device structure of TGRC-MOSFET. The source and drain region is highly doped with an n-type impurity of 5×10^{19} cm^{-3} and the substrate is doped with p-type impurity of 1×10^{17} cm^{-3} and thick oxide layer t_{ox} of 2.0 nm is embodied in it as shown in Fig. 1. Negative Junction Depth (NJD) is taken as 10 nm, gate bias (V_{gs}) is 0.7 V and drain bias (V_{ds}) is 0.5 V. Gate workfunction of TGRC-MOSFET (Φ_{ITO}) is 4.7eV and for CRC-MOSFET, it is 4.4eV. To equally analyze the device performances, both the devices (CRC and TGRC MOSFET) are optimized to have the similar threshold voltage, i.e., 0.3 V by adjusting the substrate doping. For this analysis, all the junctions of the device structure are assumed to be abrupt; the doping profiles are uniform, and the biasing conditions are considered at room temperature (T = 300 K). Further, to obtain the numerical solutions two numerical techniques Gummel and Newton have been considered [19] to obtain better convergence.

3. Simulation methodology and calibration

As we were considering a nanoscale MOSFET, the size of mesh nearly 0.003 or 0.004 units in the x and y-direction while 0.02 unit in z direction near the channel and in the active regions has been selected for more precise calculations [20]. The electron and hole currents are calculated by Poisson's equation and the continuity equations. All the simulations are based on the inversion layer Lombardi CVT mobility model to permit one to take account of carrier-carrier scattering, carrier velocity saturation, the influence of the vertical electric field and carrier diffusion at the interface. Auger recombination model and Shockley-Read–Hall (SRH) for minority carrier recombination were used. Further, the hydrodynamic energy transport model comprising of the continuity equations and momentum transport equations have also been used [19]. The equations and models utilized are listed below.

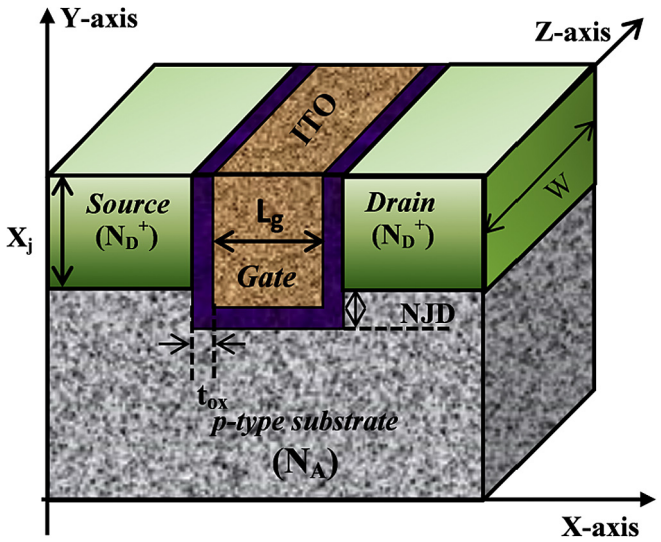


Fig. 1. 3-D device structure of TGRC-MOSFET.

1. Poisson's equation

$$div(\varepsilon \nabla \phi) = -\rho \tag{1}$$

Where ε is local permittivity; φ is electrostatic potential and ρ is local space charge density.

2. Current continuity equation

For Holes,

$$\frac{\partial p}{\partial t} = \frac{1}{q} div \vec{J}_p + G_p - R_p \tag{2}$$

For Electrons,

$$\frac{\partial n}{\partial t} = \frac{1}{q} div \vec{J}_n + G_n - R_n \tag{3}$$

Where, $\vec{J}_p$ and $\vec{J}_n$ hole and electron current density respectively; G_p and G_n are the generation rate for holes and electrons;R_p andR_n is the recombination rate for holes and electrons respectively.

3 Recombination

3.1 SRH (Shockley Read Hall)

$$R_{SRH} = \frac{pn - n_{ie}^2}{\tau_p \left[n + n_{ie} e^{(-(E_{TRAP}/kT_L))}\right] + \tau_n \left[p + n_{ie} e^{(-(E_{TRAP}/kT_L))}\right]} \tag{4}$$

Where, E_{TRAP}, change between the trap energy level and the intrinsic Fermi level; τ_n and τ_p, and are the electron lifetime and hole lifetimes, respectively.

3.2 Auger recombination

$$R_{Auger} = AUGN\left(pn^2 - nn_{ie}^2\right) + AUGP\left(np^2 - pn_{ie}^2\right) \tag{5}$$

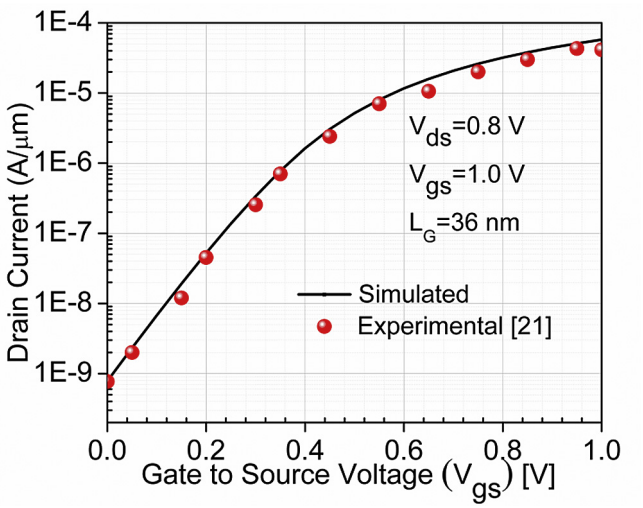
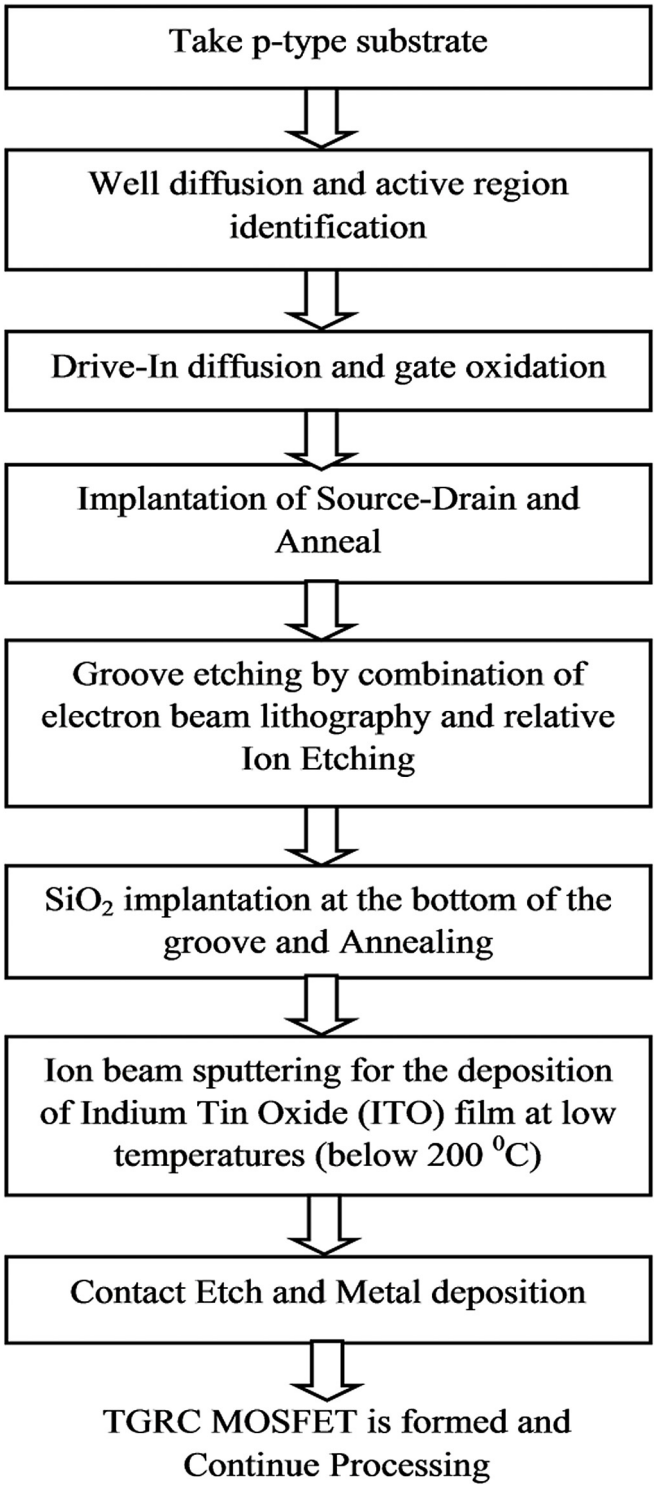


Fig. 2. Experimental and simulation of I_d-V_{gs} characteristics of 36 nm gate length recessed channel MOSFET.

Table 1
Process flow [21,22,32] of TGRC MOSFET.



AUGN and AUGP are user-definable and AUGN = 8.3×10^{-32} cm^6/s, AUGP = 1.8×10^{-31} cm^6/s.

4 Parallel electric-field-dependent mobility

$$\mu(E) = \mu_0 \left[\frac{1}{1 + (\mu_0 E / v_{sat})^{\beta}} \right]^{1/\beta} \tag{6}$$

Physical Model parameters which are used in device simulation have been calibrated according to the experimental results by Joerg Appenzeller et al., in 2002 [21]. In order to authenticate the simulations results, the data has been drawn-out [21] for 36 nm groove MOSFET and then plotted as shown in Fig. 2. It is evident from the figure that simulated results are in good agreement with the experimental results in sub-40 nm groove MOSFET thus validating the simulation models.

4. Fabrication feasibility of TGRC-MOSFET

The fabrication feasibility of TGRC-MOSFET is shown in Table 1. Moreover, the groove MOSFET has already been fabricated by different researchers such as Joerg Appenzeller et al., in 2002 [21] fabricated 36 nm groove gate and M. Xiao-Hua et al., in 2006 [22] fabricated 140 nm groove gate MOSFET. Thus, the TGRC MOSFET can be fabricated using the above device design schemes, in which the benefits of transparent gate engineering scheme have been combined with groove gate for accomplishing improved characteristics.

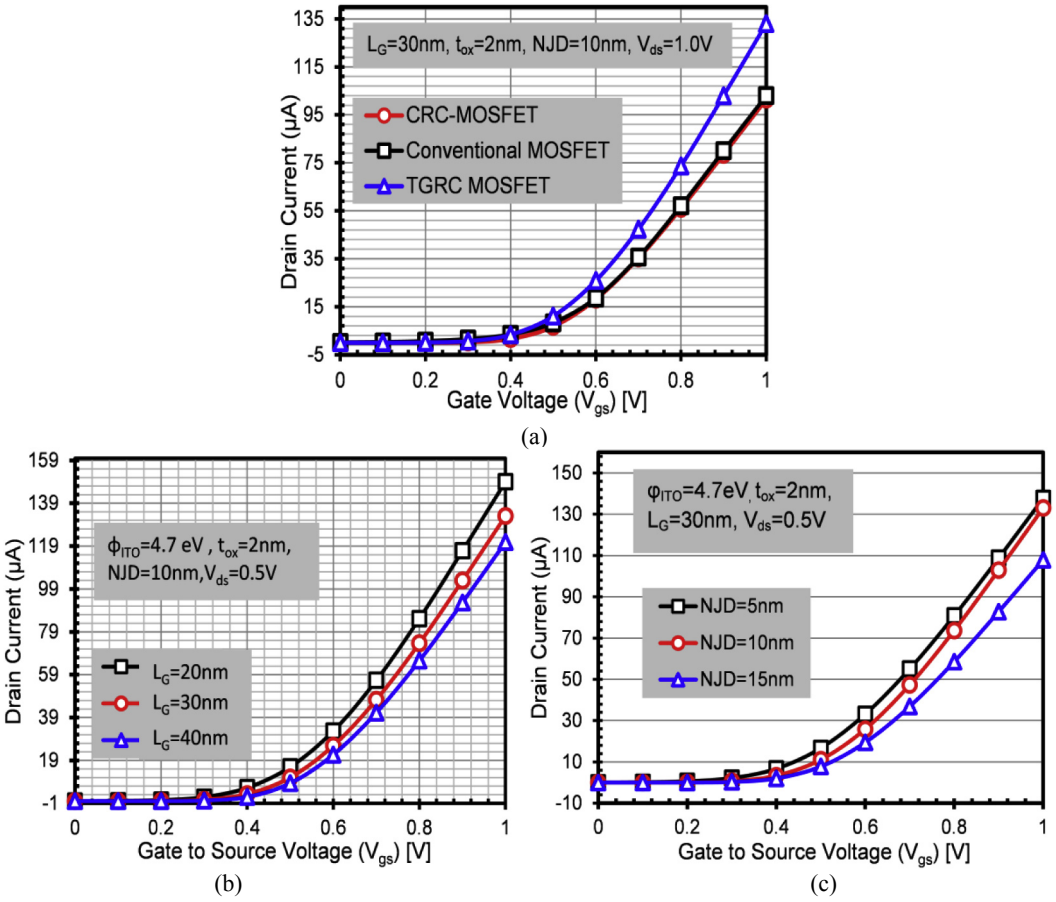


Fig. 3. (a) Drain current variations for TGRC-MOSFET, CRC-MOSFET, and Conventional MOSFET. (b) Drain current at different L_G. (c) Drain current variations at different NJDs as a function of applied V_{gs}.

5. Results and discussion

5.1. Analog performance

This subsection describes and subsequently compared the analog performance of TGRC, CRC, and conventional MOSFET. Performances are studied in terms of transfer characteristics (I_{ds}/V_{gs}), transconductance (g_m), device efficiency (g_m/I_{ds}) and intrinsic gain (g_m/g_d). Transfer characteristics of Conventional, CRC, and TGRC-MOSFET, are shown in Fig. 3(a) and it is depicted that the current driving capability of conventional and CRC-MOSFET is approximately same, but TGRC-MOSFET shows higher current driving capability. This improvement is due to the incorporation of ITO which reduces electric field in drain side [15] and thereby improves carrier efficiency resulting in improvement in drain current (by 35%).

In addition, the effect of technology variations of TGRC-MOSFET such as L_G and NJD is also observed in the transfer characteristics. It is found as the L_G is scaled down from 40 nm to 20 nm, the drain current (I_{ON}) enhances as clearly shown in Fig. 3(b). This enhancement is due to the reduction of the gate length. Hence, charge carriers needed less time to reach drain from the source. Further, by varying the value of NJD, which greatly affects the performance of RC MOSFET [23], the current driving capability of TGRC is further improved due to the increment of charge carriers travelling from source to drain if NJD reduces as shown in Fig. 3(c). There is a limitation in the reduction of NJD and it should not be zero or less; if it is, then SCEs arises. Also, the transconductance increases with increase in gate voltage, and it is more prominent in TGRC-MOSFET as shown in Fig. 4(a) due to TCO at the gate in place of metal which gives high linearity performance because linearity is proportional to transconductance [24]. Further, the effect of variation of gate length on transconductance is observed in TGRC-MOSFET and found that if the gate length shrinks from 40 nm to 30 nm, then very small reduction (by 7.1%) in transconductance is observed while, major enhancement (by 23.37%) is observed when gate length reduces from 30 nm to 20 nm as evident from Fig. 4(b). Fig. 4(c) reflects the effect of technology variation on transconductance in terms of different NJDs

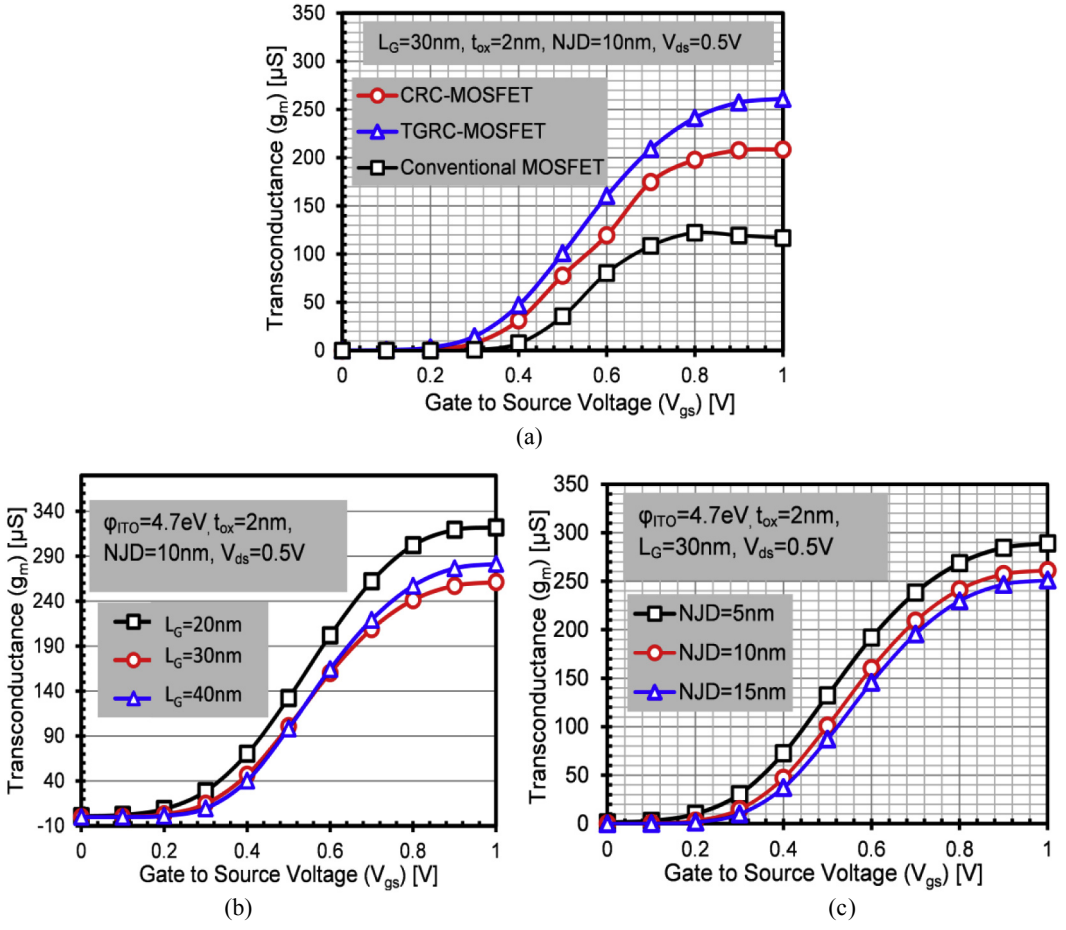


Fig. 4. (a) Variations of g_m for TGRC-MOSFET, CRC-MOSFET, and Conventional MOSFET, (b) Variation of g_m at different L_G, (c) Variation of g_m at various NJDs as a function of applied V_{gs}.

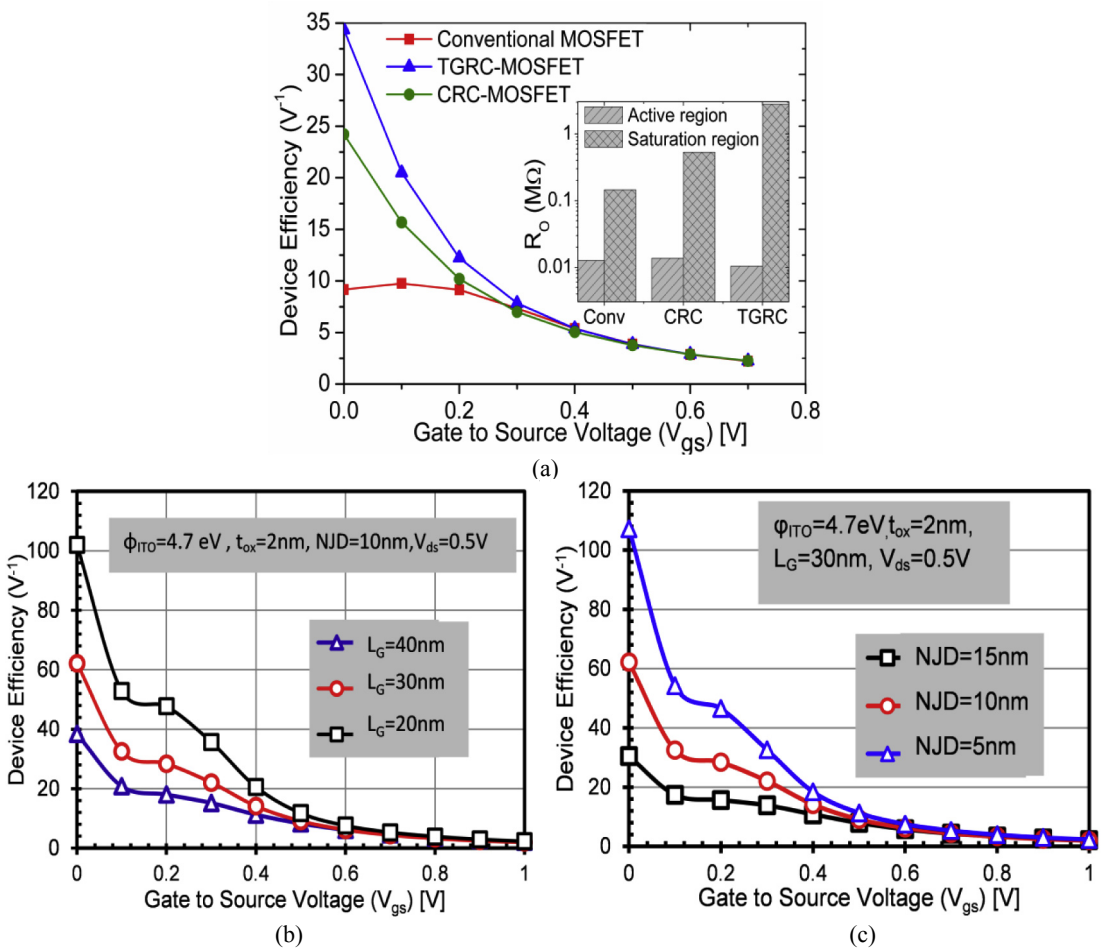


Fig. 5. (a) Variations of Device Efficiency for TGRC-MOSFET, CRC-MOSFET, and Conventional MOSFET. Inset: Output resistance. (b) Variation of Device Efficiency at different L_G, (c) Variation of Device Efficiency at various NJDs as a function of applied V_{gs}.

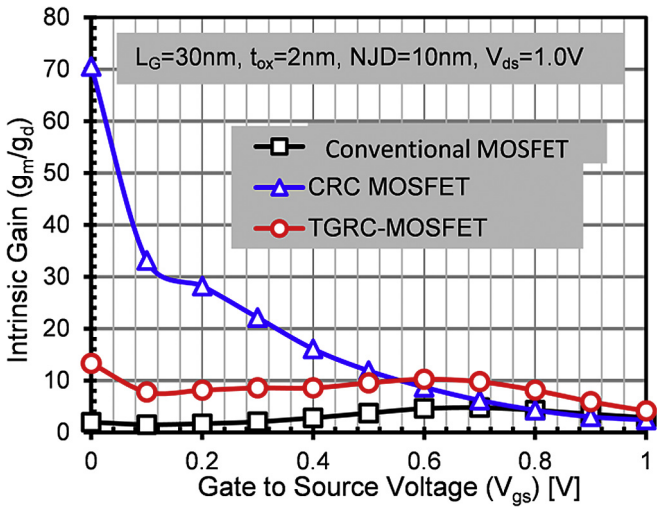


Fig. 6. Variations of Intrinsic Gain as a function of applied V_{gs} for TGRC-MOSFET, CRC-MOSFET, and Conventional MOSFET.

and it is found that transconductance is more prominent which gives high linearity performance at 5 nm NJD while it degrades if NJD increases to 10 nm and 15 nm. Thus, improved analog performance of TGRC-MOSFET as such scaled dimensions make it suitable for 22 nm node technology [2] as per ITRS (International Technology Roadmap for Semiconductor) [25].

The transconductance to the current ratio (g_m/I_d) or device efficiency and output resistance have been evaluated for three different devices (Conventional, CRC, and TGRC MOSFET) as depicted in Fig. 5(a). Device efficiency is an important parameter in the design of analog circuits, which offers the measure of efficiency to convert power into speed. It is evident from Fig. 5(a) that the device efficiency is higher in TGRC-MOSFET as compared to conventional MOSFET and CRC-MOSFET due to improvement in g_m in comparison to I_d, which overall enhances g_m/I_d. The output resistance (R_o) of a MOSFET is the inverse of the output conductance. The most important characteristics of R_o in the circuit design is maximum R_o which decides the maximum available power gain for the device. R_o is low in active region while high in the saturation region in TGRC-MOSFET as compared to conventional counterparts (shown in Fig. 5(a) inset). The device efficiency further increases by 63% and 61.29% if the gate length shrinks from 40 nm to 30 nm and 30 nm–20 nm respectively in TGRC-MOSFET, as shown in Fig. 5(b).

In addition, in technology variation, the effect of NJD variation on device efficiency is also perceived for TGRC-MOSFET (shown in Fig. 5(c)). It is evident from Fig. 5(c) that the reduction in NJD enhances the device efficiency by 78.33% if NJD is scaled to 5 nm. Intrinsic gain one of the important characteristic of MOSFET which is defined as the ratio of transconductance (g_m) to output conductance (g_d) [26]. For better performance, intrinsic gain should be as high as possible and it is evident from Fig. 6 that the intrinsic gain is lower in subthreshold region (where device is off) and inactive region, and the intrinsic gain increases in TGRC architecture in comparison to conventional and CRC MOSFET. Thus TGRC-MOSFET shows promising analog performance for ULSI in comparison to conventional and CRC MOSFET.

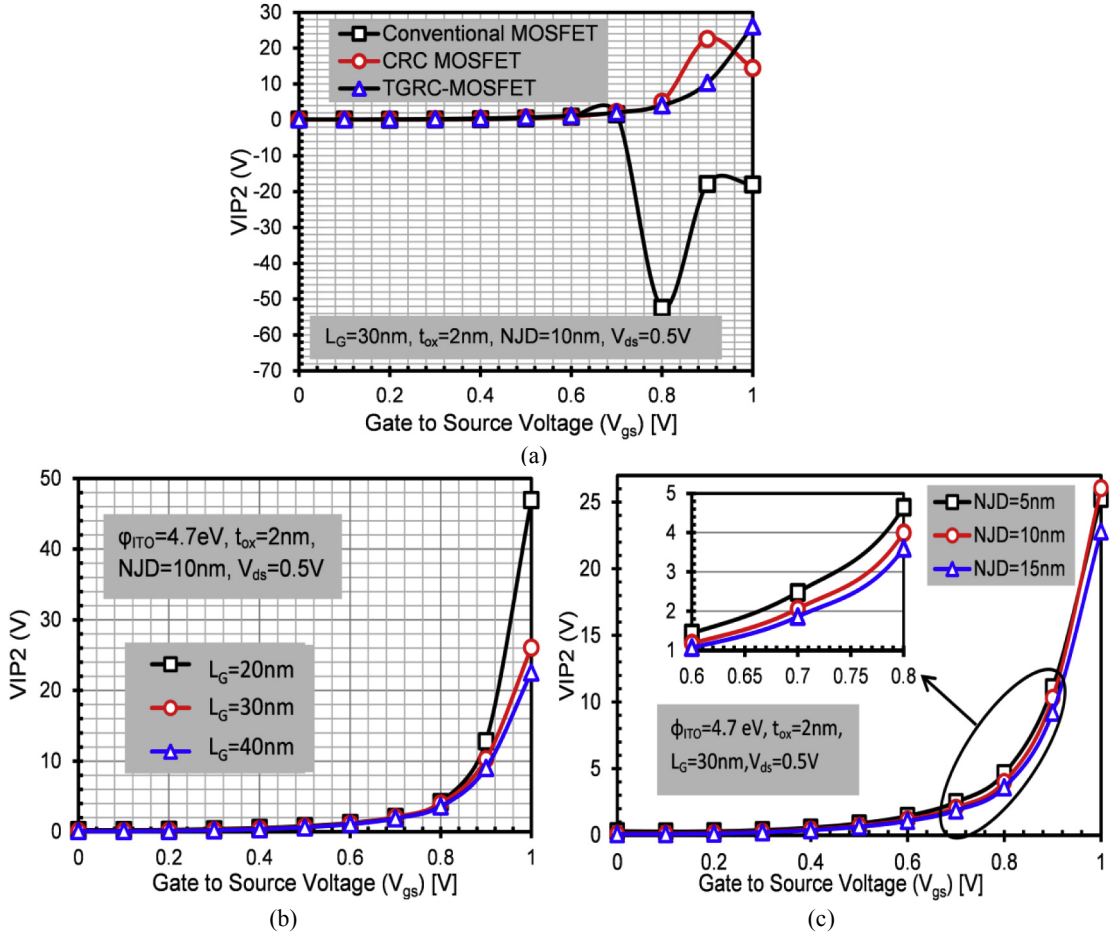


Fig. 7. (a) Variations of VIP2 for TGRC-MOSFET, CRC-MOSFET, and Conventional MOSFET. (b) Variation of VIP2 at different L_G. (c) Variation of VIP2 at different NJDs as a function of applied V_{gs}.

5.2. Intermodulation and linearity performance

5.2.1. Linearity performance

In this sub-section, the linearity of our proposed device is studied and simultaneously compared with its conventional counterparts. Thereafter, technology variations in terms of gate length and NJD have also been studied with an aim to analyze the linearity performance of TGRC at scaled dimensions. The performance metrics used in this analysis are VIP2, VIP3, IIP3 and 1-dB Compression Point. The generalized input voltage (VIP2 and VIP3) represents input voltage at which first order harmonics and third order harmonics are same as shown in equations (7) and (8) [23].

$$VIP2 = 4\frac{g_{m1}}{g_{m2}} \tag{7}$$

$$VIP3 = \sqrt{24 \times g_{m1}/g_{m3}} \tag{8}$$

Where $g_{m1} = \frac{\partial I_d}{\partial V_{gs}}$ and$g_{m2} = \frac{\partial^2 I_d}{\partial V_{gs}^2}$,$g_{m3} = \frac{\partial^3 I_d}{\partial V_{gs}^3}$

Fig. 7(a) reflects the variation of VIP2 w.r.t. the V_{gs} for TGRC-MOSFET and it is also compared with conventional MOSFET and CRC-MOSFET. For higher linearity and lower distortion operation the value of VIP2 should be higher. From Fig. 7(a), it is analyzed that the TGRC device resembles to a higher value of VIP2 by 22.3% and 8.49% as compared to the conventional and CRC designs respectively, which is only due to the incorporation of ITO as a TCO in the TGRC design. The variation of VIP2 w.r.t. applied gate to source voltage for three different gate lengths of TGRC-MOSFET as shown in Fig. 7(b), and it is found that when the gate length shrinks from 40 nm to 30 nm and from 30 nm to 20 nm, then VIP2 increases which reflect higher value at

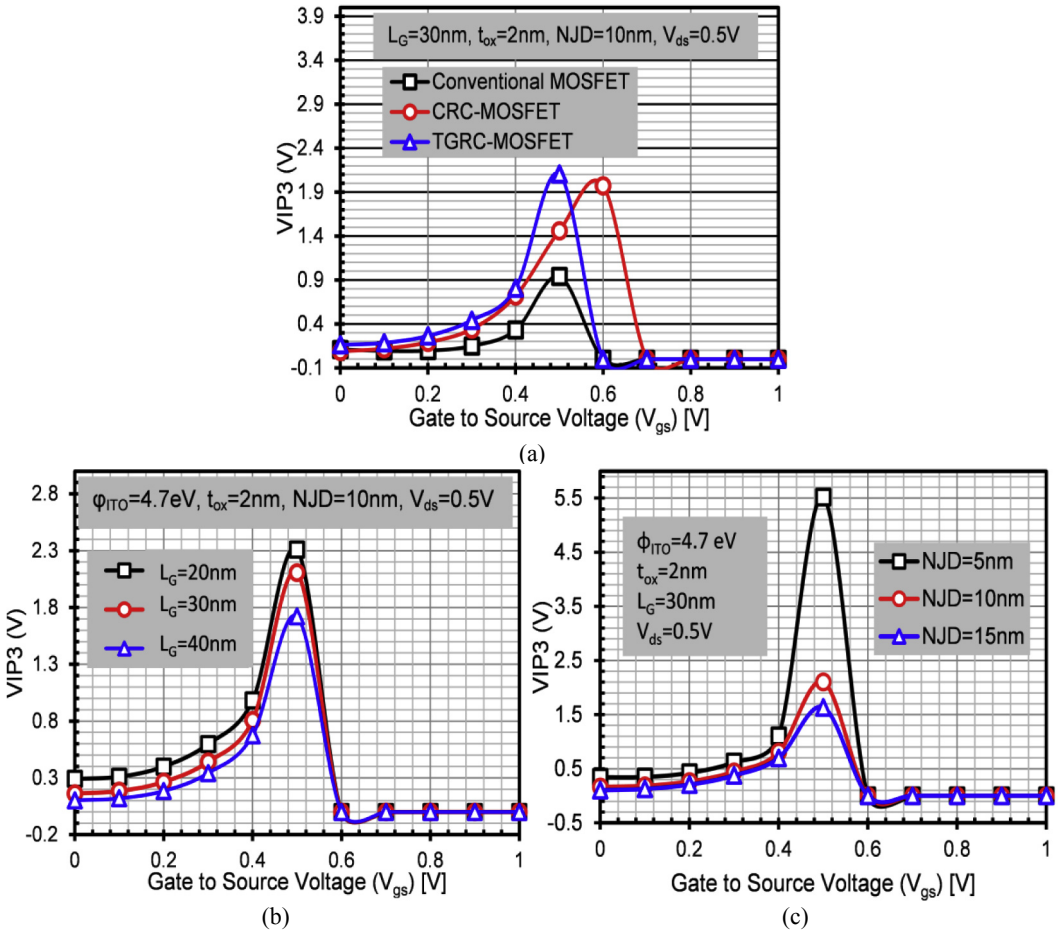


Fig. 8. (a) Variations of VIP3 for TGRC-MOSFET, CRC-MOSFET, and Conventional MOSFET. (b) Variation of VIP3 at different L_G. (c) Variation of VIP3 at various NJDs as a function of applied V_{gs}.

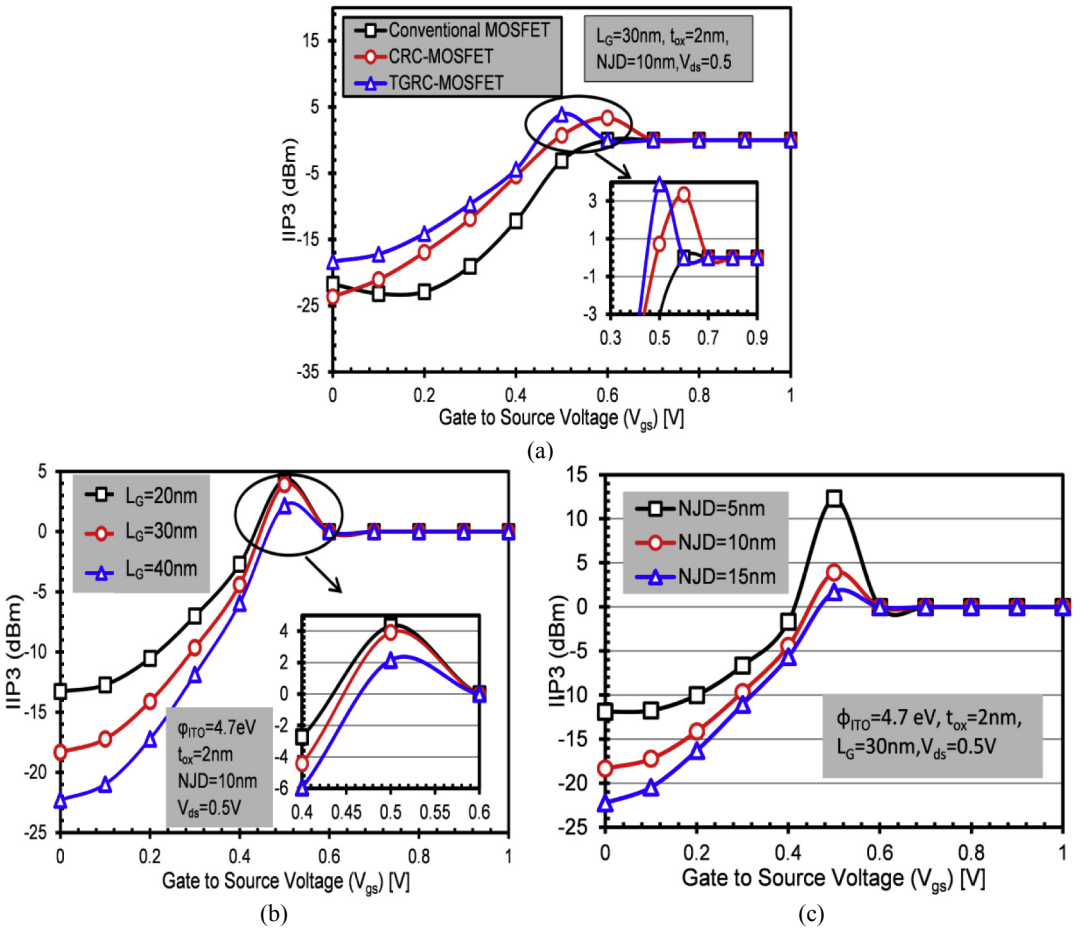


Fig. 9. (a) Variations of IIP3 for TGRC-MOSFET, CRC-MOSFET, and Conventional MOSFET. (b) Variation of IIP3 at different L_G. (c) Variation of IIP3 at different NJDs as a function of applied V_{gs}.

20 nm gate length. Thus, 20 nm TGRC architecture shows higher linearity performance. Similarly, by scaling down the NJD to 5 nm, TGRC shows the higher value of VIP2 owing to reduce SCEs, improves g_m and thus VIP2 as shown in Fig. 7(c).

Fig. 8(a) reflects the variation of VIP3 w.r.t. the V_{gs} for TGRC-MOSFET, CRC-MOSFET, and conventional MOSFET. VIP3 peak is perceived at low gate bias (i.e., 0.45 V) in TGRC architecture which is higher by 37.5%, 17.8% compared to conventional MOSFET and CRC MOSFET respectively, owing to ITO as a transparent gate design which enhances carrier velocity and thus transconductance. VIP3 peak is further enhanced by scaling down the gate length to 20 nm as clearly evident from Fig. 8(b). This enhancement is due to higher g_m (see Fig. 4(b)). Similarly, if NJD is scaled down to 5 nm from 15 nm, VIP3 peak increases significantly, reflected in Fig. 8(c), thus, signifies that scaled TGRC-MOSFET exhibit high linearity.

Moreover, there are two important FOMs which govern amplifier's efficiency and linearity i.e. third-order intercept point (IIP3) and 1-dB compression point (1 dB CP). In general for MOS based amplifiers, higher the output at the intercept, better the linearity. Third-order intercept is a theoretical point at which the third-order distortion signal amplitudes equal the input signals, and it is useful in determining the linearity condition of an amplifier. These two parameters are evaluated by equations (9) and (10) [23,27].

$$IIP3 = \frac{2}{3}\frac{g_{m1}}{g_{m3} \times Rs} \tag{9}$$

$$1 - dB\ Compression\ \text{Point} = 0.22 \times \sqrt{\frac{g_{m1}}{g_{m3}}} \tag{10}$$

where $R_S = 50\ \Omega$ for analog and RF applications.

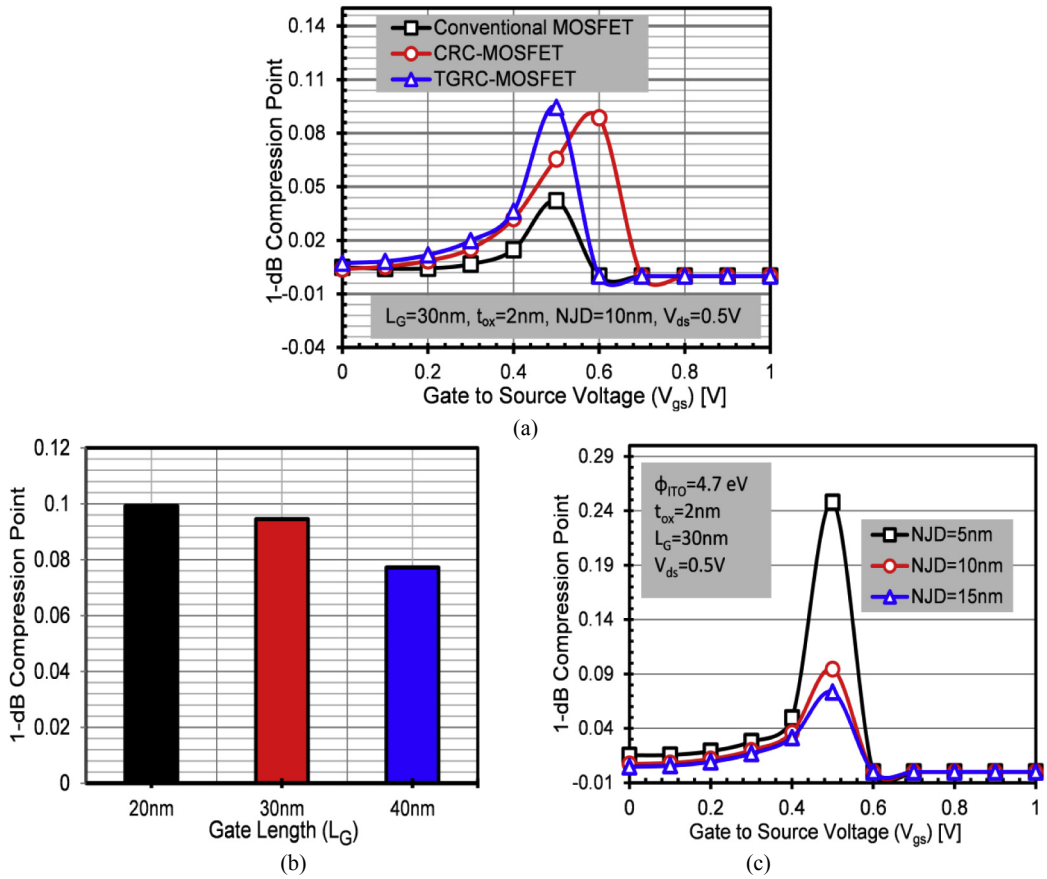


Fig. 10. (a) Variations of 1-dB Compression point for TGRC-MOSFET, CRC-MOSFET, and Conventional MOSFET. (b) Variation of 1-dB Compression point at different L_G. (c) Variation of 1-dB Compression at different NJDs as a function of applied V_{gs}.

Fig. 9(a) evidently reveals an improvement in IIP3 for the TGRC as compared to the conventional and CRC designs; this is due to the integration of the TGRC architecture, which is attributed to the high transconductance and lower value of g_{m3}, thus results in an enhancement in the carrier transport efficiency for well gate control over the channel. Moreover, the gate length and NJD variations w.r.t. the applied gate to source voltage are also shown in Fig. 9(b) and (c) and show enhancement in linearity of the device and, hence, desirable efficiency is observed. So, IIP3 can be enhanced by reducing the gate length (from 40 nm to 30 nm and from 30 nm to 20 nm) and decreasing the NJD (from 15 nm to 10 nm and from 10 nm to 5 nm). The 1-dB compression point is essential to identify at what point compression occurs so that input levels can be limited to prevent distortion. It is generally the input power that causes the gain to fall by 1 dB from the normal linear gain specification. This parameter signifies the maximum input power that the amplifier circuit can handle by providing a fixed amount of gain, and if the input power surpasses the compression point, the gain starts falling. Hence, it is desirable that a 1-dB compression point should be as high as possible for the high linear amplifier.

Fig. 10(a) shows peak value of 1-dB compression point in TGRC-MOSFET rises in comparison to its conventional counterparts. This improvement is due to the enhanced current driving capability of the device owing to high conductivity and transparency of ITO. Further, the gate length variation is observed for TGRC-MOSFET in terms of 1-dB compression point, and it is found that with the tuning of gate length and NJD, 1-dB compression point is significantly improved as shown in Fig. 10(b) and (c) owing to improved current driving capability of TGRC-MOSFET that enhances g_m and thus 1-dB compression point.

5.2.2. Intermodulation distortion

The previous subsection discusses linearity of TGRC-MOSFET and how its linearity improves if the device parameters scale down. In this subsection, distortion due to high order transconductance is studied to examine its efficacy on the performance of TGRC architecture. Fig. 11(a) reflects the variations of third derivative of transconductance (g_{m3}) w.r.t. the V_{gs} for conventional MOSFET, CRC-MOSFET, and TGRC-MOSFET. It is examined from Fig. 11(a) that the TGRC device has lower g_{m3} as compared to the CRC design; due to this lesser distortion is observed. Fig. 11(b) displays the variations of g_{m3}

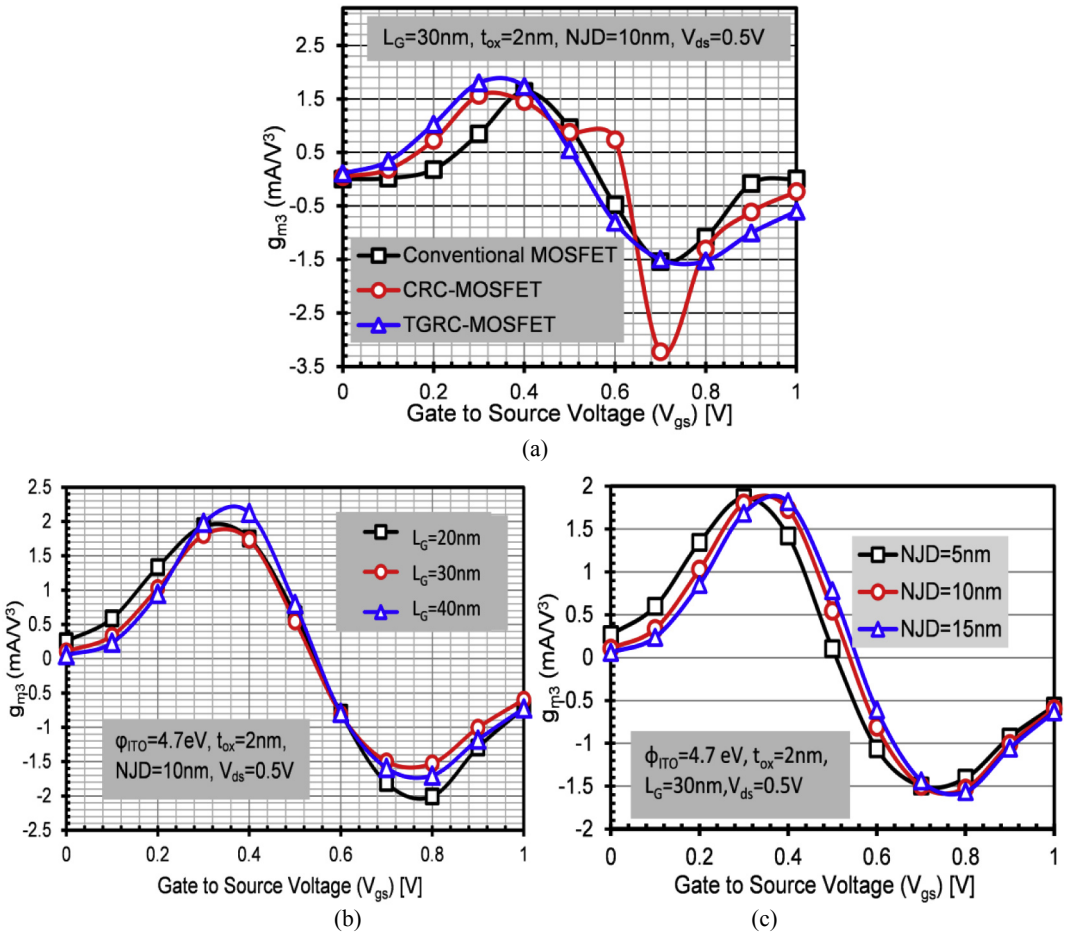


Fig. 11. (a) Variations of g_{m3} for TGRC-MOSFET, CRC-MOSFET, and Conventional MOSFET. (b) Variation of g_{m3} at different L_G. (c) Variation of g_{m3} at various NJDs as a function of applied V_{gs}.

w.r.t. the V_{gs} for three different gate lengths (20 nm, 30 nm, and 40 nm). It is found that the DC bias point moves towards higher V_{gs} with increase in L_G as clearly indicated by Fig. 11(b). This deviation is due to the amalgamation of ITO in TGRC-MOSFET.

Further, the variations of g_{m3} w.r.t. V_{gs} for different NJDs have been observed, and it is analyzed that, if NJD reduces then g_{m3} also reduces which indicates that when NJD is 5 nm, TGRC-MOSFET shows minimum distortion as depicted in Fig. 11(c).

In addition, IMD3 and HD3 (Third-order harmonic distortion) are major issues in linear amplifiers that arise owing to the nonlinearity performance of the device [28]. IMD3 signifies the intermodulation current at which first and third order intermodulation harmonic currents are equal. IMD3 is analyzed considering the effect of the transparent gate. The distortion has been calculated with the help of integral function method (IFM) since this approach allows the distortion extraction from DC measurements without an AC characterization, dissimilar to Fourier-based methods [29,30]. The approximate analytical expression for IMD3 and HD3 are given as:

$$IMD3 = \left(\frac{9}{2} \times (VIP)^3 \times g_{m3}\right)^2 \times R_s \tag{11}$$

$$HD3 = 0.25V_a^2 \frac{\left(\frac{d^2 g_{m1}}{dV_{GT}^2}\right)}{6g_{m1}} \tag{12}$$

Where V_a is the magnitude of AC signal and considered to be very small, of about 50 mV for IFM analysis. Fig. 12(a)–(d) shows the variation of IMD3 and HD3 w.r.t. the applied gate to source voltage for the conventional, CRC and TGRC

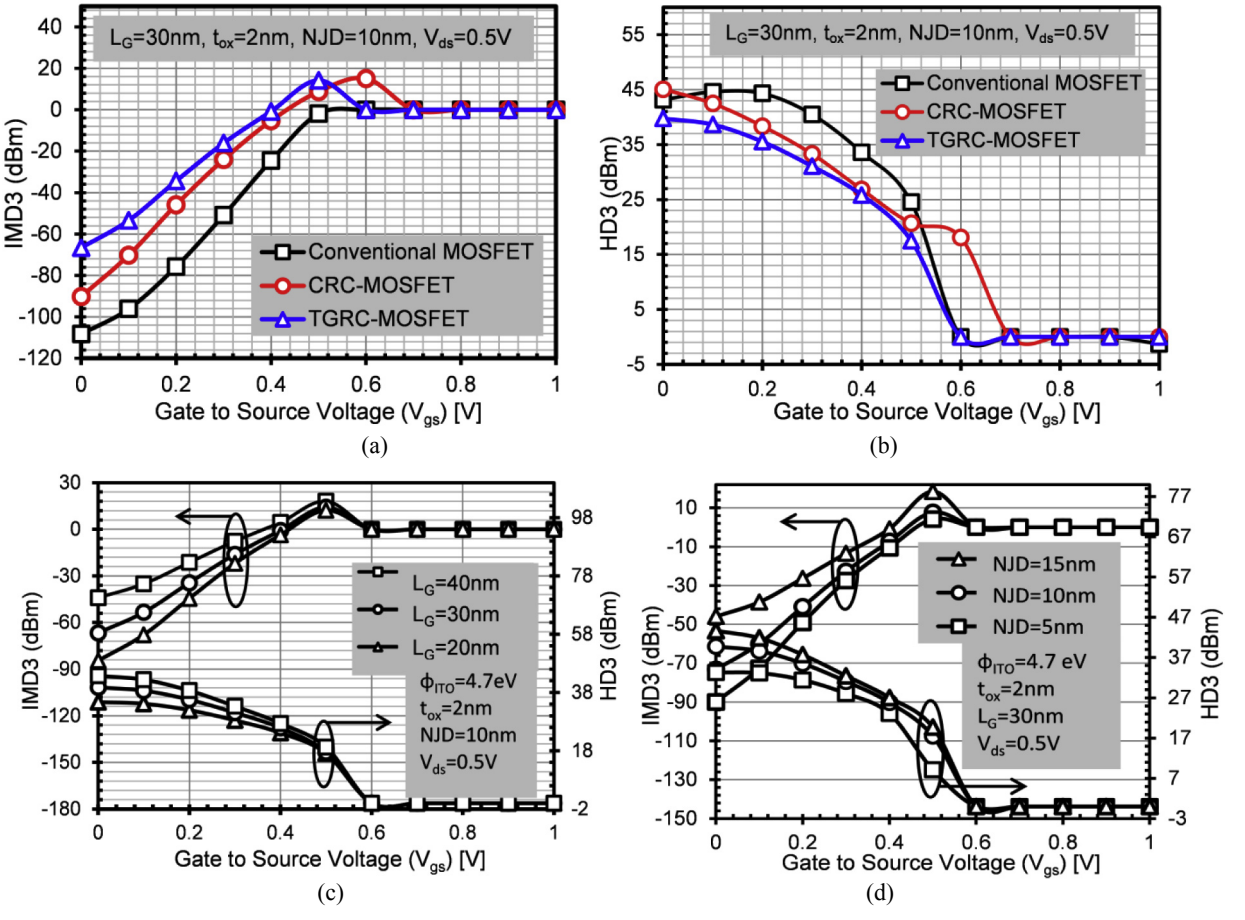


Fig. 12. (a) Variations of IMD3 for TGRC-MOSFET, CRC-MOSFET and Conventional MOSFET. (b) Variation of HD3 for TGRC-MOSFET, CRC-MOSFET, and Conventional MOSFET. (c) Variations of IMD3 and HD3 at different L_G. (d) Variation of IMD3 and HD3 at various NJDs as a function of applied V_{gs}.

designs, for gate length variation, and for NJD variation, respectively. Degeneracy of signals in a wireless communication system is originated as IMD3 from the nonlinearity shown by the transistor static characteristics. By using a circuit with balanced topologies even-order harmonics can be reduced by 40–50 dB. Therefore, it is essential to diminish the third-order harmonics for decreasing the signal distortion [31]. Fig. 12(a) shows that the performance of IMD3 degrades in TGRC-MOSFET owing to the high peak value of VIP3 which dominates the value of IMD3 less in comparison to g_{m3} (Fig. 11(a)) as compared to its counterpart conventional and CRC-MOSFET. Meanwhile, HD3 is also reduced in TGRC architecture as compared to its conventional counterparts as shown in Fig. 12(b). Further, both the third order distortions have been reduced for TGRC-MOSFET if the gate length is reduced to 20 nm due to the reduction of g_{m3} as shown in Fig. 12(c). Fig. 12(d) also reflects the reduction in IMD3 and HD3 with reduced NJD. Thus, the scaling of the device architecture reduces the intermodulation and harmonic distortions, hence presenting TGRC-MOSFET as a favorable candidate for RFIC designing.

6. Conclusion

A complete study of the analog, linearity and intermodulation distortion analysis of TGRC-MOSFET has been explored with the impact of trench gate and gate length miniaturization at sub-nano level. From the investigation, it is found that TGRC-MOSFET is more linear device than its counterparts conventional MOSFET and CRC-MOSFET, due to the incorporation of the ITO as a transparent gate in TGRC design. It is found that TGRC-MOSFET reveals greater values of g_m (enhanced by 32.1% and 35% compared to conventional MOSFET and CRC-MOSFET respectively), lower g_{m3}, improved device efficiency and noteworthy improvement in peak values of VIP2, VIP3, 1-dB compression point, IIP3 and lesser values of the IMD3 and HD3 in comparison to its counterparts at 5 nm NJD and 20 nm gate length. Thus, TGRC-MOSFET delivered enriched analog and linearity performance in terms of superior input power and lesser signal distortion. Moreover, it is also analyzed that with the tuning of TGRC's parameters such as L_G and NJD, its linearity performance enhances appreciably owing to enhanced current driving capability and reduced g_{m3} (distortions). Therefore, the proposed TGRC-MOSFET is prominent for high scale integration, which can be developed for RFIC design and it is also a favorable candidate for ultra-low power, analog, and distortion-less application.

Acknowledgement

This work was supported by Microelectronics Research Lab, Department of Engineering Physics and Electrical Engineering Department Delhi Technological University (3507/(OBC)(NET-DEC.2015)).

References

[1] B. Razavi, R. Behzad, RF Microelectronics, Prentice Hall, New Jersey, 1998.
[2] H. Iwai, Roadmap for 22nm and beyond, Microelectron. Eng. 86 (2009) 1520–1528.
[3] R.M. Barsan, Analysis and modeling of dual-gate MOSFET's, Electron Devices IEEE Trans. 28 (1981) 523–534.
[4] X. An, R. Huang, B. Zhao, X. Zhang, Y. Wang, Design guideline of an ultra-thin body SOI MOSFET for low-power and high-performance applications, Semicond. Sci. Technol. 19 (2003) 347.
[5] R. Chaujar, R. Kaur, M. Saxena, M. Gupta, R. Gupta, TCAD assessment of gate electrode workfunction engineered recessed channel (GEWE-RC) MOSFET and its multilayered gate architecture—part I: hot-carrier-reliability evaluation, Electron Devices IEEE Trans. 55 (2008) 2602–2613.
[6] C.P. Auth, J.D. Plummer, Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET's, Electron Device Lett. IEEE 18 (1997) 74–76.
[7] N. Gupta, A. Kumar, R. Chaujar, Impact of device parameter variation on RF performance of gate electrode workfunction engineered (GEWE)-silicon nanowire (SiNW) MOSFET, J. Comput. Electron. 14 (2015) 798–810.
[8] S. Veeraraghavan, J.G. Fossum, Short-channel effects in SOI MOSFETs, IEEE Trans. Electron Devices 36 (1989) 522–528.
[9] R. Chaujar, R. Kaur, M. Saxena, M. Gupta, R. Gupta, Laterally amalgamated DUal material GAte concave (L-DUMGAC) MOSFET for ULSI, Microelectron. Eng. 85 (2008) 566–576.
[10] H.T.D.J. Rogers, Criteria Choos. Conduct. 25 (2010).
[11] V. Singh, C. Suman, S. Kumar, Indium Tin Oxide (ITO) films on flexible substrates for organic light emitting diodes, Proc. ASID (2006) 388.
[12] R. Murali, J.D. Meindl, Modeling the effect of source/drain junction depth on bulk-MOSFET scaling, Solid-state Electron. 51 (2007) 823–827.
[13] T. Minami, Transparent conducting oxide semiconductors for transparent electrodes, Semicond. Sci. Technol. 20 (2005) S35–S44.
[14] G.E. Moore, Progress in digital integrated electronics, in: Electron Devices Meeting, 1975, pp. 11–13.
[15] A. Kumar, N. Gupta, R. Chaujar, Analysis of novel transparent gate recessed channel (TGRC) MOSFET for improved analog behaviour, Microsyst. Technol. 22 (11) (2015) 2665–2671.
[16] A. Kumar, N. Gupta, R. Chaujar, Effect of structured parameters on the hot-carrier immunity of transparent gate recessed channel (TGRC) MOSFET, Microsyst. Technol. (2016) 1–8.
[17] A. Kumar, N. Gupta, R. Chaujar, Power gain assessment of ITO based Transparent Gate Recessed Channel (TGRC) MOSFET for RF/wireless applications, Superlattices Microstruct. 91 (2016) 290–301.
[18] A. Kumar, N. Gupta, R. Chaujar, TCAD RF performance investigation of transparent gate recessed channel MOSFET, Microelectron. J. 49 (2016) 36–42.
[19] I. SILVACO, ATLAS User's Manual, Santa Clara, CA, Ver, 5, 2011.
[20] M. Rahimian, A.A. Orouji, Investigation of the electrical and thermal performance of SOI MOSFETs with modified channel engineering, Mater. Sci. Semicond. Process. 16 (2013) 1248–1256.
[21] J. Appenzeller, R. Martel, P. Avouris, J. Knoch, J. Scholvin, J.A. del Alamo, P. Rice, P. Solomon, Sub-40 nm SOI V-groove n-MOSFETs, IEEE Electron Device Lett. 23 (2002) 100–102.
[22] M. Xiao-Hua, H. Yue, S. Bao-Gang, G. Hai-Xia, R. Hong-Xia, Z. Jin-Cheng, Z. Jin-Feng, Z. Xiao-Ju, Z. Wei-Dong, Fabrication and characterization of groove-gate MOSFETs based on a self-aligned CMOS process, Chin. Phys. 15 (2006) 195.
[23] R. Chaujar, R. Kaur, M. Saxena, M. Gupta, R. Gupta, TCAD assessment of Gate Electrode Workfunction Engineered Recessed Channel (GEWE-RC) MOSFET and its multi-layered gate architecture, Part II: analog and large signal performance evaluation, Superlattices Microstruct. 46 (2009) 645–655.

[24] T.W. Kim, B. Kim, K. Lee, Highly linear receiver front-end adopting MOSFET transconductance linearization by multiple gated transistors, IEEE J. Solid-State Circuits 39 (2004) 223–229.
[25] K. Jeong, A.B. Kahng, A power-constrained MPU roadmap for the International Technology Roadmap for Semiconductors (ITRS), in: SoC Design Conference (ISOCC), 2009 International, IEEE, 2009, pp. 49–52.
[26] R. Wang, J. Zhuge, R. Huang, Y. Tian, H. Xiao, L. Zhang, C. Li, X. Zhang, Y. Wang, Analog/RF performance of Si nanowire MOSFETs and the impact of process variation, IEEE Trans. Electron Devices 54 (2007) 1288–1294.
[27] P.H. Woerlee, M.J. Knitel, R. Van Langevelde, D.B. Klaassen, L.F. Tiemeijer, A.J. Scholten, A.T. Zegers-van Duijnhoven, RF-CMOS performance trends, IEEE Trans. Electron Devices 48 (2001) 1776–1782.
[28] N. Gupta, R. Chaujar, Optimization of high-k and gate metal workfunction for improved analog and intermodulation performance of Gate Stack (GS)-GEWE-SiNW MOSFET, Superlattices Microstruct. 97 (2016) 631–641.
[29] A. Cerdeira, M.A. Alemán, M. Estrada, D. Flandre, Integral function method for determination of nonlinear harmonic distortion, Solid-State Electron. 48 (2004) 2225–2234.
[30] R.T. Doria, A. Cerdeira, J.-P. Raskin, D. Flandre, M.A. Pavanello, Harmonic distortion analysis of double gate graded-channel MOSFETs operating in saturation, Microelectron. J. 39 (2008) 1663–1670.
[31] P. Ghosh, S. Haldar, R. Gupta, M. Gupta, An investigation of linearity performance and intermodulation distortion of GME CGT MOSFET for RFIC design, IEEE Trans. Electron Devices 59 (2012) 3263–3268.
[32] D. Kim, Y. Han, J.-S. Cho, S.-K. Koh, Low temperature deposition of ITO thin films by ion beam sputtering, Thin Solid Films 377 (2000) 81–86.

Superlattices and Microstructures 125 (2019) 72–79

Contents lists available at ScienceDirect

Superlattices and Microstructures

journal homepage: www.elsevier.com/locate/superlattices

RF noise modeling of Black Phosphorus Junctionless Trench MOSFET in strong inversion region

Ajay Kumar[a], Neha Gupta[b], M.M. Tripathi[a], Rishu Chaujar[c,*]

[a] Electrical Engineering Department, Delhi Technological University, Delhi, India
[b] Department of Applied Science and Humanities, Northern India Engineering College, New Delhi, India
[c] Applied Physics Department, Delhi Technological University, Delhi, India

ARTICLE INFO

Keywords:
BP-JL-T-MOSFET
CT-MOSFET
Noise
RF

ABSTRACT

In this paper, RF noise modeling of Black Phosphorus Junctionless Trench (BP-JL-T) MOSFET has been investigated in strong inversion region. The simulated and modeled results are simultaneously compared with Conventional Trench (CT) MOSFET at THz frequency range. By using analytical expressions from RF equivalent schematic, few RF figure-of-merits (FOMs) have been evaluated. It is found that RF noise parameters such as noise resistance (R_n), minimum noise figure (NF_{min}), optimum source susceptance (B_{opt}) and conductance (G_{opt}) are reduced to more than 200%. Modeled results reveal that BP-JL-T-MOSFET minimizes RF noise thus, providing the detailed insight to RF engineers for microwave applications/RFIC design.

1. Introduction

Low power wireless applications such as the Internet of Things (IoT) and wireless sensor network are setting severe constrain on power consumption [1] at RF. Highly scaled CMOS may enhance RF FOMs, along with a higher cut-off frequency (THz range) which makes it appropriate for microwave and RF applications [2–5] in the sub-20 nm regime. Material plays the vital role in deciding how long the device RF performance enhances in THz frequency range [3,4,6,7]. For high-performance transistor application, black phosphorus is frequently used due to higher mobility at room temperature ($\sim$1000 $cm^2V^{-1}s^{-1}$) and its layered structure. BP has tunable band gap from 0.3 eV (bulk) to 1.0–1.5 eV (a single layer) [8–11]. Due to many more electrical properties, it is the most appropriate material for transistor applications [12,13]. To augment the RF performance of the CT-MOSFET, the gate material is replaced by black phosphorus, the junctions are eliminated from the device, and thus a low power, less noisy and highly RF efficient BP-JL-T-MOSFET is proposed in this work. RF noise is the major concern to make a MOS device for microwave, and RF applications. The RF model should be capable enough to predict the RF noise characteristics for a realistic RF design [1]. For higher frequencies (THz range), the channel generated thermal noise is the dominant noise source. The random motion of charge carriers is responsible for thermal noise in the channel and the induced gate noise generated due to potential fluctuations in the channel owing to the coupling of the gate through gate-oxide capacitance.

This work presents a timely and desirous RF noise modeling of a nanoscale MOSFET in strong inversion region. In Section 2, device design has been explored with the respective design parameters. In Section 3, simulation methodology and model calibration has been explained with used equations. In Section 4, we show the equivalent small signal model of a nanoscale MOSFET for RF noise evaluation where we have extracted RF FOM such as f_T, f_{MAX}, $H_{21,}$ and U and then RF noise analysis has been performed step by step

* Corresponding author.
E-mail addresses: ajaykumar@dtu.ac.in (A. Kumar), gupta.neha@niecdelhi.ac.in (N. Gupta), mmtripathi@dce.ac.in (M.M. Tripathi), chaujar.rishu@dtu.ac.in (R. Chaujar).

https://doi.org/10.1016/j.spmi.2018.10.025
Received 7 September 2018; Received in revised form 24 October 2018; Accepted 25 October 2018
Available online 26 October 2018
0749-6036/

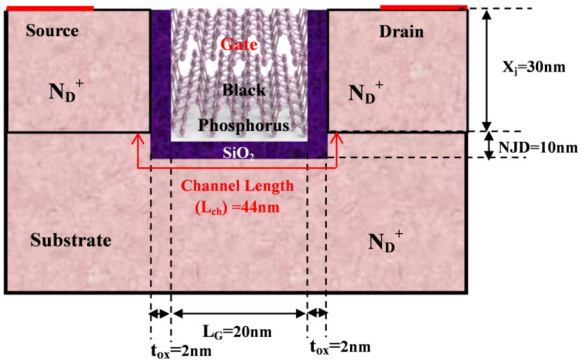


Fig. 1. The device structure of the proposed device (BP-JL-T-MOSFET).

in terms of R_n, NF_{min}, G_{opt} and B_{opt} with derived analytical expressions.

2. Device design of BP-JL-T-MOSFET

The BP-JL-T-MOSFET device structure is shown in Fig. 1 and its parameters are indicated in Table 1. In this proposed device; black phosphorus is amalgamated in the trench region. Source and drain regions are heavily doped while the substrate is lightly doped. The device has 20 nm gate length (Channel Length ($L_g + 2(t_{ox} + NJD)) = 44$ nm), and sub-20 nm gate length improves the density of ICs (Integrated Circuits).

3. Methodology and calibration

For the RF noise and RF FOMs extraction, the direct extraction methodology is used by the small signal model. For TCAD simulations, we have included Parallel Electric Field Dependence (fldmob model). This model takes care of all the parameters affecting the mobility of carriers including velocity saturation effect. For carrier generation-recombination, we have implemented (klasrh model) concentration-dependent Klaassen Shockley-Read-Hall Recombination model as it can include a concentration-dependent lifetime of carriers [14]. The following equations [14] and models are used in the simulation.

1. Poisson's equation

$$div(\varepsilon \nabla \phi) = -\rho \tag{1}$$

Where ε, φ and ρ represents the permittivity, potential, and space charge density respectively.

2. Continuity equations of current

For Holes,

$$\frac{\partial p}{\partial t} = \frac{1}{q} div \vec{J_p} + G_p - R_p \tag{2}$$

For Electrons,

Table 1
BP-JL-T and CT MOSFETs design parameters.

Device Parameters	BP-JL-T-MOSFET	CT-MOSFET
Gate Length (L_g)	20 nm	20 nm
Channel Length (L_{ch})	44 nm	44 nm
Source and the Drain region Length	30 nm	30 nm
Width of the Device (W)	200 nm	200 nm
Groove Depth	38 nm	38 nm
Negative Junction Depth (NJD)	10 nm	10 nm
Substrate Doping	5×10^{16} cm^{-3} (N_D^+)	1×10^{17} cm^{-3} (N_A)
Source/Drain Doping (N_D^+)	5×10^{16} cm^{-3} (N_D^+)	1×10^{19} cm^{-3} (N_A)
Physical Oxide Thickness (t_{ox})	2 nm	2 nm
Metal work function (Φ)	5.16 eV	4.4 eV
Gate to source voltage (V_{gs})	1.5 V	1.5 V
Drain to source voltage (V_{ds})	0.2 V	0.2 V

$$\frac{\partial n}{\partial t} = \frac{1}{q} div\vec{J_n} + G_n - R_n \tag{3}$$

Where, $\vec{J_p}$and $\vec{J_n}$ are current density; the generation rate represented by G_p andG_n; recombination rate R_p and R_n for holes and electrons respectively.

3 Recombination

(a) SRH (Shockley Read Hall)

$$R_{SRH} = \frac{pn - n_{ie}^2}{\tau_p \left[n + n_{ie} e^{(-(E_{TRAP}/kT_L))}\right] + \tau_n \left[p + n_{ie} e^{(-(E_{TRAP}/kT_L))}\right]} \tag{4}$$

Where, E_{TRAP} is a change in the intrinsic Fermi level and the trap energy level; τ_n and τ_p, are the electron and hole lifetimes, respectively.

(b) Auger recombination

$$R_{Auger} = AUGN(pn^2 - nn_{ie}^2) + AUGP(np^2 - pn_{ie}^2) \tag{5}$$

AUGN $= 8.3 \times 10^{-32}$ cm^6/s, AUGP $= 1.8 \times 10^{-31}$ cm^6/s (user-definable).

4.Parallel electric-field-dependent mobility

$$\mu(E) = \mu_0 [\frac{1}{1 + (\mu_0 E/\upsilon_{sat})^{\beta}}]^{1/\beta} \tag{6}$$

Further, the simulation models have been validated and calibrated with experimental data [15]. The experimental data is drawn out from fabricated grooved MOSFET of 36 nm [15] and plotted against simulated results for same device dimensions as reflected in Fig. 2(a) and (b). Fig. 2(a) reflects the calibrated output characteristics and (b) represents calibrated transfer characteristics. It is evident from Fig. 2 that the simulated result nearly matched with the experimental results which signify the validation of simulation models.

4. Small signal RF MOSFET modeling

Fig. 3(a) reflects the equivalent circuit which used BP-JL-T-MOSFET device and has good accuracy and computing efficiency. The circuit consists of an intrinsic and parasitic component that affects the device behavior at RF, namely, the substrate resistance R_B, gate resistance R_G, the source/drain resistance R_S, R_D, and the extrinsic capacitances C_{GSe}, C_{GDe}, and C_{GBe}. For RF measurement, source and bulk are grounded ($V_S = V_B = 0$ V) in the two-port configuration of MOSFET. In the saturation region, MOSFET usually operates for RF applications. Here, the small signal parameters are evaluated from Fig. 3(b) for the calculation of RF FOMs [16] and noise parameters. Voltage control-voltage sources (VCVSs) generated the currents and calculated by Ref. [17]:

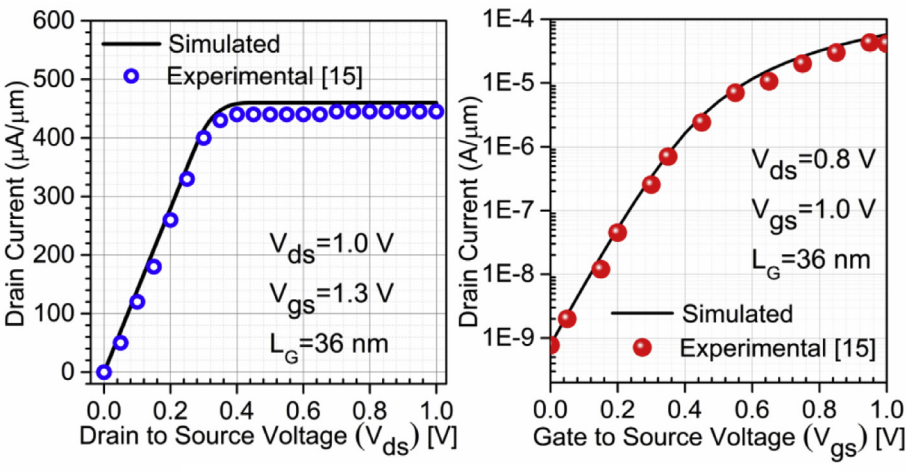


Fig. 2. Calibration of simulated and experimental data: (a) Output characteristics and (b) Transfer characteristics; of 36 nm Trench MOSFET.

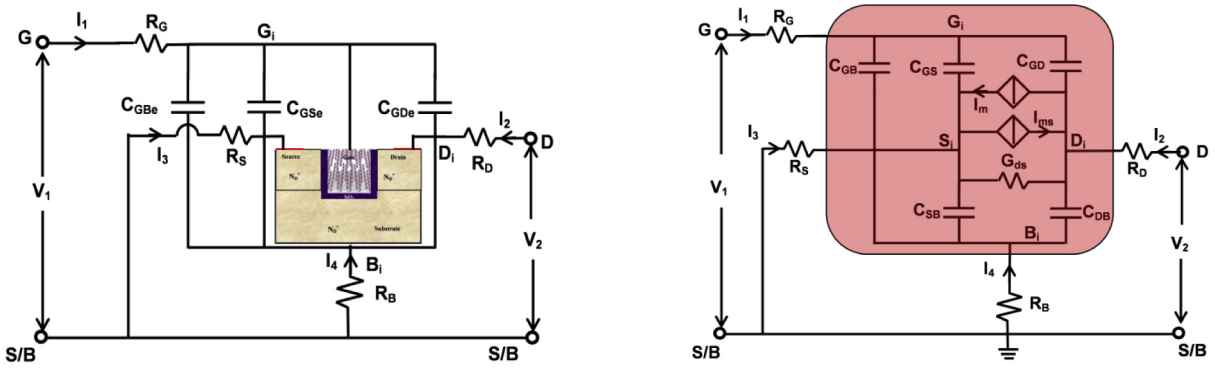


Fig. 3. (a) RF equivalent sub-circuit with BP-JL-T-MOSFET, and (b) Small-signal equivalent circuit in strong inversion region of an RF BP-JL-MOSFET.

$$I_m = Y_m.\,[V(Gi) - V(Bi)] \tag{7}$$

$$I_{ms} = Y_{ms}.\,[V(Si) - V(Bi)] \tag{8}$$

Where $Y_m = G_m. -j\omega C_m$is the gate transmittance and $Y_{ms} = G_{ms}. -j\omega C_{ms}$ is the source transmittance. G_m and G_{ms} are the gate and source transmittance while C_m and C_{ms} are transcapacitances (for gate and source respectively) [17]. For RF analysis from equivalent circuit (Fig. 3(b)), using the assumption (equation (9)) the higher order terms are neglected

$$\omega^2(C_{BB}^2R_B^2 + R_G(2C_{GB}^2R_B + C_{GG}^2R_G)) + \omega^4R_G^2(C_{GB}^2 - C_{BB}^2C_{GG}^2)^2 << 1 \tag{9}$$

and it is valid for few THz operating frequency. In the saturation region, Y-parameters can be derived as

$$Y_{11} \cong \omega^2(R_BC_{GB}^2 + R_GC_{GG}^2) + j\omega C_{GG} \tag{10}$$

$$Y_{22} \cong G_{GS} + \omega^2(C_{DB}R_B(C_{DB} - C_m + C_{ms}) + C_{GD}R_G(C_{GD} + C_m)) + j\omega(C_{DB} + C_{GD}) \tag{11}$$

$$Y_{12} \cong \omega^2(R_BC_{GB}C_{DB} - R_GC_{GG}C_{GD}) - j\omega C_{GD} \tag{12}$$

$$Y_{21} \cong G_{m,eff} + \omega^2(C_{GB}R_B(C_{DB} - C_m + C_{ms}) - C_{GG}R_G(C_{GD} + C_m)) - j\omega(C_{GD} + C_m) \tag{13}$$

with total capacitance C_{GG} (C_{GS} + C_{GD} + C_{GB}). The capacitances are calculated using equation (14)–(17) as

$$C_{GS} = (\mathrm{Im}(Y_{11}) + \mathrm{Im}(Y_{12}))/\omega \tag{14}$$

$$C_{GD} = -\mathrm{Im}(Y_{12})/\omega \tag{15}$$

$$G_{DS} = \mathrm{Re}(Y_{22})|_{\omega=0} \tag{16}$$

$$C_{DB(SD)} = (\mathrm{Im}(Y_{22}) + \mathrm{Im}(Y_{12}))/\omega \tag{17}$$

In the calculation of Y-parametrs, R_S and R_D can be neglected for higher frequencies [18] and the effective gate and source transconductance (in saturation) [17] are $G_{m,eff} = G_m/D$ and $G_{ms,eff} = (G_{ms} + G_{DS})/D$ with $D \approx 1 + G_{ms}R_S$.

4.1. Extraction of RF FoMs

RF FoMs (useful for circuit designing) is analytically modeled with the help of methodical expressions of Y-parameters and expressed from equation (10)–(13).

4.1.1. Transit frequency f_T and maximum oscillation frequency f_{MAX}

f_T is also known as cut-off frequency [5]. f_T can be calculated at unity magnitude of current gain and represented as given in equation (18). However, maximum oscillator frequency (f_{MAX}) is calculated when unilateral gain becomes unity [1,19,20], and with the help of small signal components, f_{MAX} can be represented as given in equation (19). Results show that f_T and f_{MAX} improve four times and eight times respectively in simulated data and similar improvement is observed in modeled data (which are nearly matched) in BP-JL-T device as compared to CT device as reflected in Fig. 4(a) and (b) respectively. f_T enhances due to a reduction in stray capacitances and f_{MAX} improves due to improved f_T (shown in equation (19)).

$$f_T = \frac{G_{m,eff}}{2\pi(C_{GS} + C_{GD})} \tag{18}$$

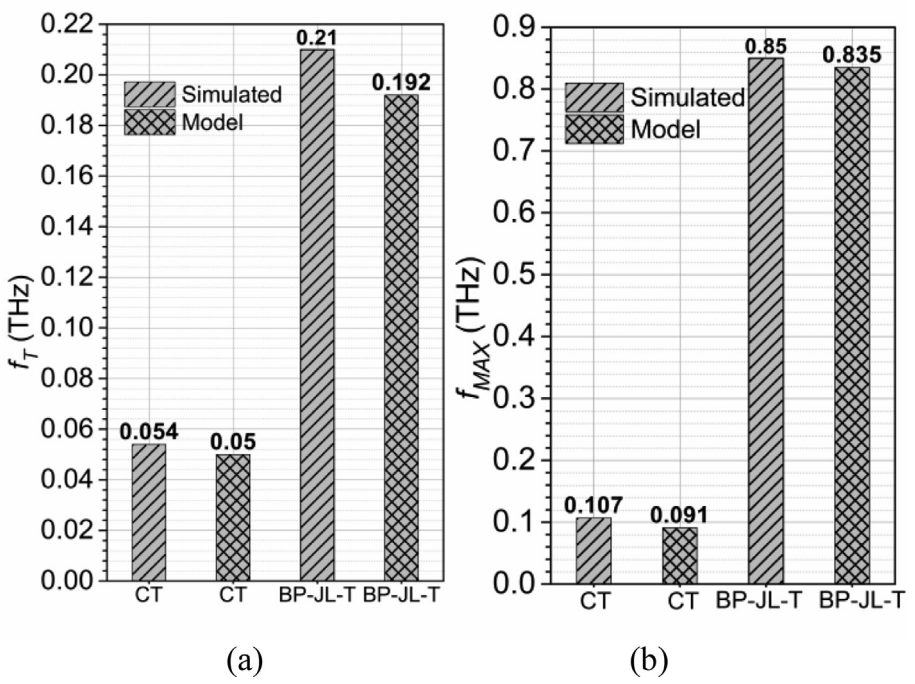


Fig. 4. (a) f_T and (b) f_{MAX}, at V_{ds} = 0.2 V and V_{gs} = 1.5 V for CT and BP-JL-T-MOSFETs.

$$f_{MAX} = \frac{f_T}{\sqrt{4R_G(G_{DS} + 2\pi f_T C_{GD})}} \tag{19}$$

4.1.2. Current gain (H_{21}) and unilateral gain (U)

The current gain is defined as equation (20)

$$H_{21} = \frac{I_2}{I_1} = \frac{Y_{21}}{Y_{11}} \tag{20}$$

Using equations (10) and (13), the complex expression for H_{21} is calculated and found as

$$H_{21} \approx \frac{G_{m,eff} - j\omega(C_{GD} - C_m)}{j\omega C_{GG}} \tag{21}$$

Unilateral gain, also called Mason's gain, is calculated by equation (22)

$$U = \frac{|Y_{21} - Y_{12}|^2}{4.(\mathrm{Re}\{Y_{11}\}\mathrm{Re}\{Y_{22}\} - \mathrm{Re}\{Y_{12}\}\mathrm{Re}\{Y_{21}\})} \tag{22}$$

Fig. 5(a) and (b) reflects that H_{21} and U enhance by 7.5% and 20% respectively in BP-JL-T as compared to CT device owing to lower stray capacitances, and the simulated data is matched with modeled data at THz frequency range.

4.2. RF noise analysis

Noise sources of a MOSFET are shown in Fig. 6 where the noise current sources are parallel to the resistance generated thermal noise. In the device, thermal noise and induced gate noise is modeled by noise current sources I_{nD} and I_{nG} respectively. All the noise parameters are derived using the RF equivalent circuit (shown in Fig. 6) and the expressions are obtained as shown in equations (23)–(25). From the simplified expressions, it is observed that R_n only depends (through the parameter χ_{nD}) on channel thermal noise, however, $F_{\min}$ and Y_{opt} depends on channel thermal noise and induced gate noise [21]. Fig. 7(a) and (b) reflected that NF_{min} and R_n reduce by four and five times respectively in BP-JL-T device as compared to CT device and the modeled results have good agreement with the simulated results. Further, for the extraction of a_N and b_N from B_{opt} and G_{opt} (for Y_{opt}), two intermediate steps (equation (32) and (33)) are required, and $F_{\min}$ can also be used for direct extraction of b_N, but sometimes it has more complexity. χ_{nD} is the thermal noise access and represents how much noise is generated at the drain and is given in equation (29).

Moreover, optimum source susceptance (B_{opt}) and optimum source conductance (G_{opt}) are determined by differentiating equation (24) and expressed as noise [20] paramters which is reflected in Fig. 8(a) and (b) respectively for BP-JL-T and CT MOSFETs. It is observed that G_{opt} and B_{opt} are reduced owing to BP as a gate material, which in turn reduces χ_{nD} and stray capacitances in BP-JL-T

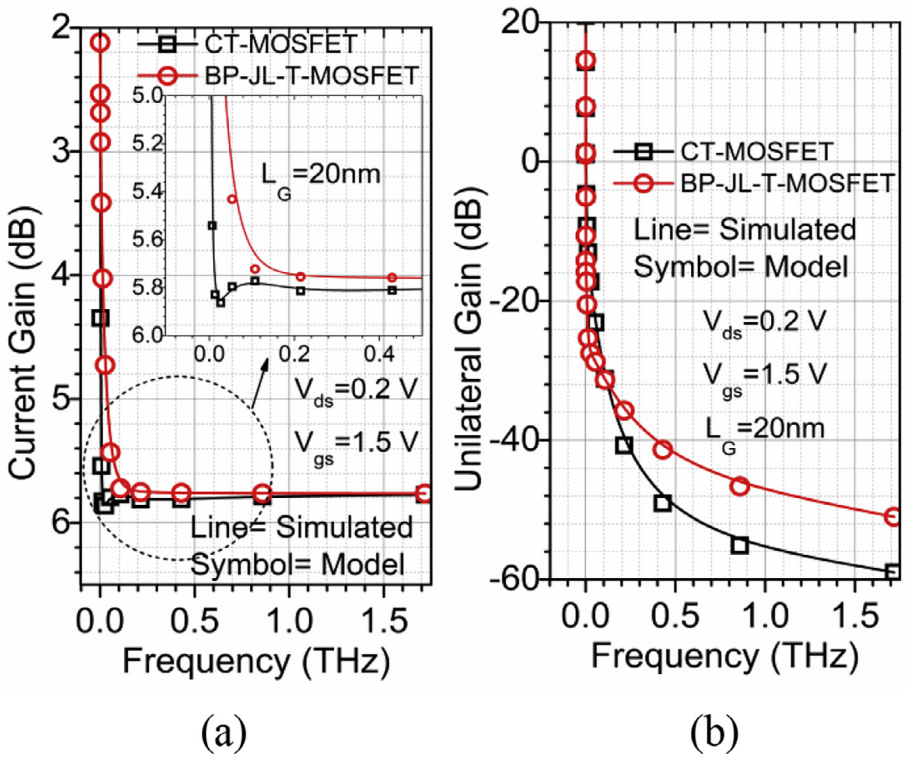


Fig. 5. (a) Current gain and (b) Unilateral gain at V_{ds} = 0.2 V and V_{gs} = 1.5 V for CT and BP-JL-T-MOSFETs.

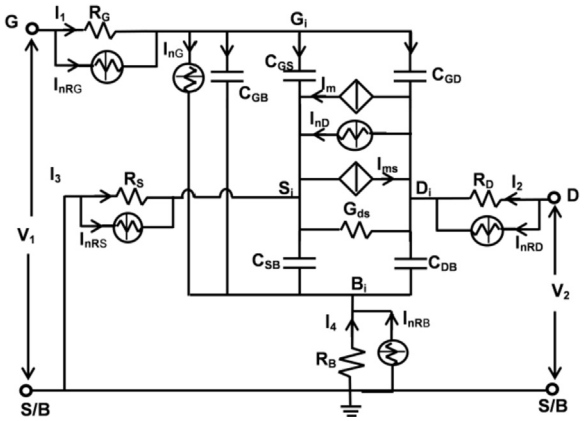


Fig. 6. Small-signal equivalent circuit with the noise sources of a MOSFET.

device as compared to CT device by three times and two times respectively and the modeled results are matched with the simulated results.

$$R_n = \frac{\chi_{nD}}{G_{m,eff}} + R_G \tag{23}$$

$$Y_{opt} = G_{opt} + jB_{opt} = \frac{\omega(b_N + jc_N G_{m,eff})}{2(d_N + \omega^2 R_B (C_{BD} + C_{GD})^2)} \tag{24}$$

$$F_{\min} = 1 + \omega \frac{b_N}{|Y_{21,\text{int}}|^2} + \omega^2 \frac{2R_B(G_{m,eff} C_{GD}(C_{BD} + C_{GD} + G_{m,eff} R_G C_{GD})) + \omega^2 e_N R_G}{G_{m,eff}^2} \tag{25}$$

$$a_N = c_g \sqrt{2C_{GG} C_m \delta_{nG} \chi_{nD}} \tag{26}$$

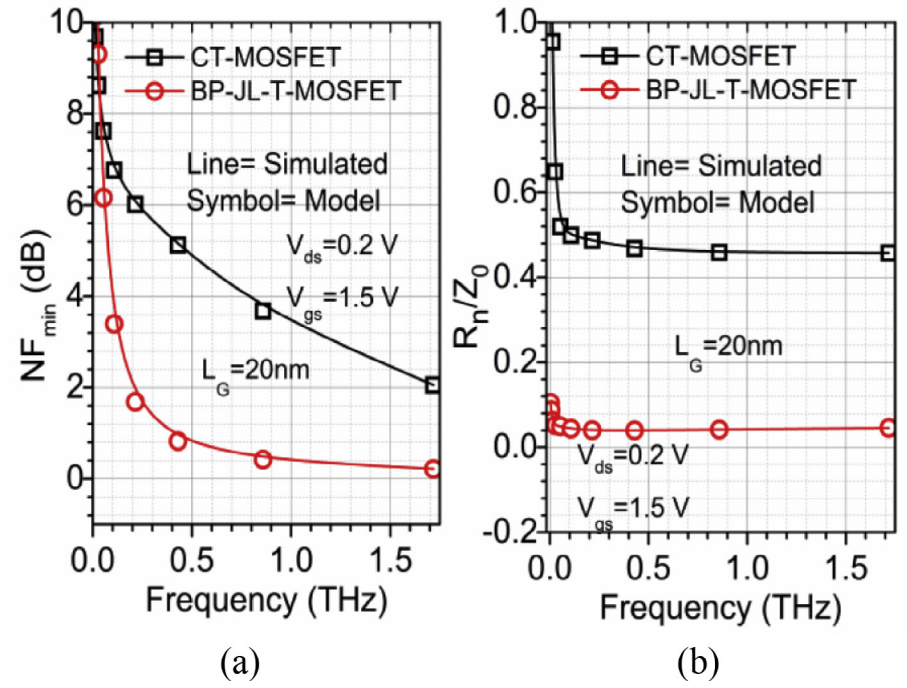


Fig. 7. (a) NF_{min} and (b) R_n, at V_{ds} = 0.2 V and V_{gs} = 1.5 V for CT and BP-JL-T-MOSFETs.

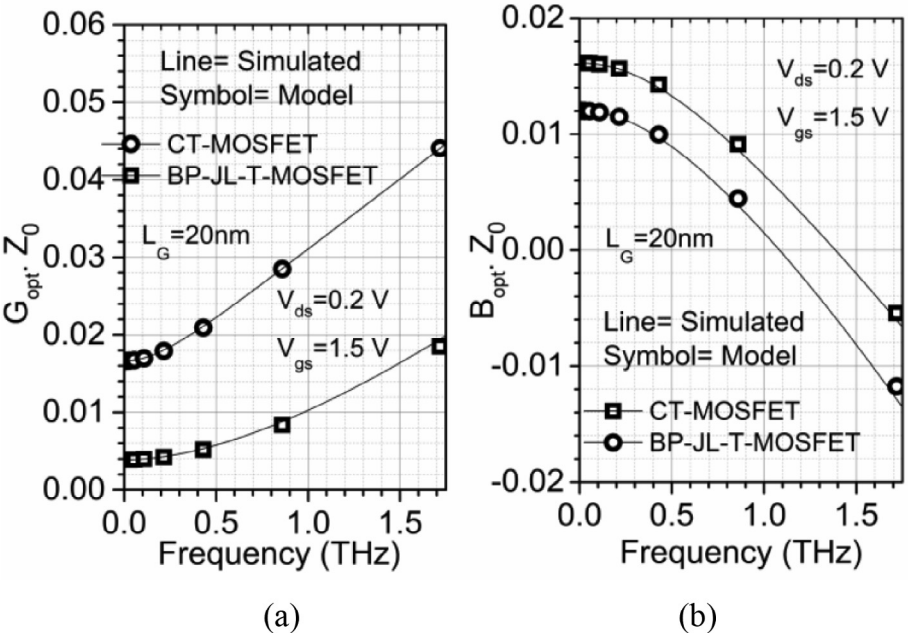


Fig. 8. (a) G_{opt}, and (b) B_{opt} at V_{ds} = 0.2 V and V_{gs} = 1.5 V for CT and BP-JL-T-MOSFETs.

$$b_N = \sqrt{\frac{2d_N\left[2G_{m,eff}\left(\omega^2 e_N R_B + C_{GG}G_{m,eff}\left(C_{GG}\chi_{nD} - a_N\right)\right) + C_{GG}C_m\left|Y_{21,\text{int}}\right|^2\delta_{nG}\right] - c_N^2 G_{m,eff}^3}{G_{m,eff}}} \tag{27}$$

$$c_N = a_N - 2\chi_{nD}C_{GG},\ d_N = G_{m,eff}\chi_{nD} + \left|Y_{21,\text{int}}\right|^2 R_G,\ e_N = \left(C_{BD}C_{GG} - C_{GD}\left(C_{GD} - C_{GG} + C_m\right)\right)^2 \tag{28}$$

$$\chi_{nD} = G_{m,eff}\left(R_n - R_G\right) \tag{29}$$

$$a_N = \frac{2[B_{opt}(|Y_{21,\text{int}}|^2 R_G + \omega^2 R_B (C_{BD} + C_{GD})^2) + G_{m,eff}\chi_{nD}(B_{opt} + \omega C_{GG})]}{\omega G_{m,eff}} \tag{30}$$

$$b_N = \frac{2G_{opt}(G_{m,eff}\chi_{nD} + |Y_{21,\text{int}}|^2 R_G + \omega^2 R_B (C_{BD} + C_{GD})^2)}{\omega} \tag{31}$$

$$\chi_{nD} = \frac{G_{m,eff}[b_N^2 + C_N^2 G_{m,eff}^2 - 4d_N(\omega^2 e_N R_B + C_{GG} G_{m,eff}(C_{GG}\chi_{nD} - a_N))]}{2d_N C_{GG} C_m |Y_{21,\text{int}}|^2} \tag{32}$$

$$c_g = \frac{a_N}{\sqrt{2C_{GG} C_m \delta_{nG}\chi_{nD}}\, a_N} \tag{33}$$

5. Conclusion

This paper discusses the RF noise analytical modeling of the RF FOMs and noise parameters of a nanoscale BP-JL-T-MOSFET in strong inversion region. Simple and generic RF small signal equivalent circuit is demonstrated, and the results show a fine calibration of modeled and simulated data. It is found that RF FOMs such as H_{21}, U, f_T and f_{MAX} improved by 7.4%, 20%, four times and eight times respectively for BP-JL-T MOSFET. Further, a significant reduction in the RF noise parameters such as NF_{min}, R_n, G_{opt} and B_{opt} is obtained in BP-JL-T-MOSFET edifying its effectiveness in RFIC and LNA design.

Acknowledgement

The authors are thankful to University Grants Commission (UGC), Electrical Engineering Department, Microelectronics Research Lab, and Delhi Technological to carry out this work.

References

[1] M.-A. Chalkiadaki, C.C. Enz, RF small-signal and noise modeling including parameter extraction of nanoscale MOSFET from weak to strong inversion, IEEE Trans. Microw. Theor. Tech. 63 (7) (2015) 2173–2184.
[2] M. Saito, M. Ono, R. Fujimoto, H. Tanimoto, N. Ito, T. Yoshitomi, T. Ohguro, H.S. Momose, H. Iwai, 0.15-μm RF CMOS technology compatible with logic CMOS for low-voltage operation, Electron Devices, IEEE Trans. 45 (3) (1998) 737–742.
[3] A. Kumar, M. Tripathi, and R. Chaujar, "Small-signal Modeling of In2O5Sn Based Transparent Gate Recessed Channel MOSFET for Microwave/RF Applications." pp. 976-979..
[4] A. Kumar, M. Tripathi, R. Chaujar, In 2 O 5 Sn based transparent gate recessed channel MOSFET: RF small-signal model for microwave applications, AEU-Int. J. Electron. Commun. 93 (2018) 233–241.
[5] A. Kumar, N. Gupta, R. Chaujar, Power gain assessment of ITO based Transparent Gate Recessed Channel (TGRC) MOSFET for RF/wireless applications, Superlattice. Microst. 91 (2016) 290–301.
[6] A. Kumar, N. Gupta, R. Chaujar, TCAD RF performance investigation of transparent gate recessed channel MOSFET, Microelectron. J. 49 (2016) 36–42.
[7] A. Kumar, M. Tripathi, R. Chaujar, Investigation of parasitic capacitances of In_2O_5Sn gate electrode recessed channel MOSFET for ULSI switching applications, Microsyst. Technol. 23 (12) (2017) 5867–5874.
[8] S. Das, W. Zhang, M. Demarteau, A. Hoffmann, M. Dubey, A. Roelofs, Tunable transport gap in phosphorene, Nano Lett. 14 (10) (2014) 5733–5739.
[9] A. Kumar, M. Tripathi, R. Chaujar, Comprehensive analysis of sub-20nm black phosphorus based junctionless-recessed channel MOSFET for analog/RF applications, Superlattice. Microst. 116 (2018) 171–180.
[10] H. Liu, A.T. Neal, Z. Zhu, Z. Luo, X. Xu, D. Tománek, D.Y. Peide, Phosphorene: an Unexplored 2D Semiconductor with a High Hole Mobility, (2014).
[11] A. Castellanos-Gomez, L. Vicarelli, E. Prada, J.O. Island, K. Narasimha-Acharya, S.I. Blanter, D.J. Groenendijk, M. Buscema, G.A. Steele, J. Alvarez, Isolation and characterization of few-layer black phosphorus, 2D Mater. 1 (2) (2014) 025001.
[12] M.C. Robbins, S.J. Koester, Black phosphorus p-and n-mosfets with electrostatically doped contacts, IEEE Electron. Device Lett. 38 (2) (2017) 285–288.
[13] N. Haratipour, S.J. Koester, Ambipolar black phosphorus MOSFETs with record n-channel transconductance, IEEE Electron. Device Lett. 37 (1) (2016) 103–106.
[14] I. SILVACO, ATLAS User's Manual vol. 5, Ver, *Santa Clara, CA*, 2011.
[15] J. Appenzeller, R. Martel, P. Avouris, J. Knoch, J. Scholvin, J.A. del Alamo, P. Rice, P. Solomon, Sub-40 nm SOI V-groove n-MOSFETs, IEEE Electron. Device Lett. 23 (2) (2002) 100–102.
[16] N. Gupta, A. Kumar, R. Chaujar, Impact of device parameter variation on RF performance of gate electrode workfunction engineered (GEWE)-silicon nanowire (SiNW) MOSFET, J. Comput. Electron. 14 (3) (2015) 798–810.
[17] C.C. Enz, E.A. Vittoz, Charge-based MOS Transistor Modeling: the EKV Model for Low-power and RF IC Design, John Wiley & Sons, 2006.
[18] C. Enz, An MOS transistor model for RF IC design valid in all regions of operation, IEEE Trans. Microw. Theor. Tech. 50 (1) (2002) 342–359.
[19] N. Gupta, R. Chaujar, Investigation of temperature variations on analog/RF and linearity performance of stacked gate GEWE-SiNW MOSFET for improved device reliability, Microelectron. Reliab. 64 (2016) 235–241.
[20] N. Gupta, R. Chaujar, Influence of gate metal engineering on small-signal and noise behaviour of silicon nanowire MOSFET for low-noise amplifiers, Appl. Phys. A 122 (8) (2016) 1–9.
[21] Y. Cheng, M.J. Deen, C.-H. Chen, MOSFET modeling for RF IC design, IEEE Trans. Electron. Dev. 52 (7) (2005) 1286–1303.

Superlattices and Microstructures 116 (2018) 171–180

Contents lists available at ScienceDirect

Superlattices and Microstructures

journal homepage: www.elsevier.com/locate/superlattices

Comprehensive analysis of sub-20 nm black phosphorus based junctionless-recessed channel MOSFET for analog/RF applications

Ajay Kumar [a], M.M. Tripathi [a], Rishu Chaujar [b, *]

[a] Electrical Engineering Department, Delhi Technological University, Delhi, India
[b] Applied Physics Department, Delhi Technological University, Delhi, India

ARTICLE INFO

Article history:
Available online 16 February 2018

Keywords:
Analog
CRC-MOSFET
Frequency
Gain
Parasitic capacitance
RF
BP-JL-RC-MOSFET

ABSTRACT

In this work, a comprehensive analog and RF performance of a novel Black Phosphorus-Junctionless-Recessed Channel (BP-JL-RC) MOSFET has been explored at 45 nm technology node (Gate length = 20 nm). The integration of black phosphorus with junctionless recessed channel MOSFET, leads to higher drain current of about 0.3 mA and excellent switching ratio (of the order of 10^{11}) due to reduced off-current which leads to improvement in sub-threshold slope (SS) (67mV/dec). Further, RF performance metrics have also been studied with an aim to analyze high-frequency performance. The following FOMs have been evaluated: cut-off frequency (f_T), maximum oscillator frequency (f_{MAX}), stern stability factor, various power gains and parasitic capacitances at THz frequency range. Thus, in addition to the high packing density offered by RC MOSFET, the proposed design finds numerous application at THz frequency making it a promising candidate at wafer scale integration level.

1. Introduction

Continuous scaling of MOSFET in sub-20 nm gate length develops opportunities for high speed and low power applications. Several THz cut-off frequencies can be achieved in highly scaled MOSFETs, making CMOS technology appropriate for RF application [1–4]. In sub-20 nm gate length, source/drain capacitances called parasitic capacitances increases and hence, gate control over the channel reduces [5]. Short channel effects (SCEs) also arises due to the scaling down of device dimensions which is not suitable for analog and RF applications [6]. The problems associated with SCEs are threshold voltage roll-off [7], hot carrier effects (HCEs) [8], drain induced barrier lowering (DIBL) [9,10], punch through and gate tunneling current [11]. These effects can be eliminated (reduced) by changing the gate material as well as doping profile of the MOSFET. To reduce these effects and for high-performance transistor application, a new class of material called black phosphorus is used in a recessed structure [12]. Black phosphorus is one of the promising material due to very high mobility (~1000 $cm^2V^{-1}s^{-1}$ at room temperature) and a layered structure which can be realized at sub-1nm thick channel [13]. From bulk (0.3 eV) to single layer (1.0–1.5 eV), black phosphorus has tunable band gap [14–16]. Due to these properties, black phosphorus is the most suitable 2D material in comparison to graphene and transition metal dichalcogenides while graphene has high mobility but

* Corresponding author.
E-mail addresses: ajaykumar@dtu.ac.in (A. Kumar), mmtripathi@dce.ac.in (M.M. Tripathi), chaujar.rishu@dtu.ac.in (R. Chaujar).

https://doi.org/10.1016/j.spmi.2018.02.018
0749-6036/

band gap is zero [17], and transition metal dichalcogenides have low mobility (~10–250 $cm^2V^{-1}s^{-1}$) but large band gap (1–2 eV) [18–20]. Black phosphorus is frequently used in MOSFET for high-performance transistor applications [21,22], but SCEs [23] are the main disadvantages of conventional MOSFET at sub-20 nm gate length. To enhance the performance of the recessed channel MOSFET, black phosphorus is used as a 2D gate material, and the doping profile of source, drain, and channel is uniform to make it as a junctionless transistor. The physics and basic properties of the junctionless transistor are introduced by JP Colinge [24], and it is observed that the sub-threshold swing, DIBL and switching ratio is improved due to the junctionless phenomenon.

For high-performance analog and RF applications, we have combined two techniques, namely recessed gate technique and junctionless technique in this work. In the recessed gate, few layers of black phosphorus are amalgamated as black phosphorus is a most attractive 2D material and the symmetric doping is done to eliminate the junction from the device. BP-JL-RC-MOSFET is a novel device in which the electrical characteristics of a transistor are enhanced due to the tremendous value of switching ratio (due to the lower value of I_{OFF}). Such a high I_{ON} and low I_{OFF} makes black phosphorus a promising material for digital electronics applications [17]. BP JL-RC MOSFET is a highly scaled device, and the gate length is 20 nm which increases the packing density of the integrated circuits (ICs).

2. Device design and its parameters

Fig. 1 shows the simulated 20 nm device structure of BP JL-RC MOSFET. All the design parameters are given in Table 1, and the biasings are applied at room temperature (T = 300 K).

3. Simulation methodology and calibration

ATLAS is a powerful simulation tool which is used for the extraction of reliability results and all Figure of Merits (FOM) [25]. Various simulation models have been used such as Lombardi CVT model to consider all the mobilities such as scattering mechanism which is caused by the parallel and perpendicular field applied on the device. For carrier generation-recombination, we have used Shockley-Read-Hall (SRH) Recombination. Fermi-Dirac statistics is used in case of very highly doped material. To consider the information about the low energy (temperature) of the carriers, we have used Energy Balance Transport (EBT) model [25]. Further, to obtain the numerical solutions, two numerical techniques such as Gummel and Newton have been considered [25] to obtain better convergence.

The calibration of Physical Model parameters of the simulated device with the experimental data by Joerg Appenzeller et al. in 2002 [26] is shown in Fig. 2. To validate the simulation results, the statistics have been drawn-out [26] for 36 nm groove MOSFET and then plotted as evident in Fig. 2. It is detected from Fig. 2 that simulated results almost matched with the experimental data in sub-40 nm groove MOSFET, thus validating the simulation models.

4. Fabrication feasibility of BP-JL-RC-MOSFET

The fabrication feasibility of BP-JL-RC-MOSFET is shown in Fig. 3. Moreover, the groove MOSFET has been fabricated by different researchers such as Joerg Appenzeller et al., in 2002 [26], fabricated 36 nm groove gate and M. Xiao-Hua et al., in 2006 [27], fabricated 140 nm groove gate MOSFET. First of all, a p-type silicon substrate wafer is taken and then n-well region is created by a diffusion process. The active region is then identified and Drive-In diffusion and gate oxidation process is carried out.

Source-drain implantation and anneal process are done before groove etching by a combination of electron beam lithography and reactive ion etching; and then SiO_2 implant at the bottom of the groove is done. In the groove region, black

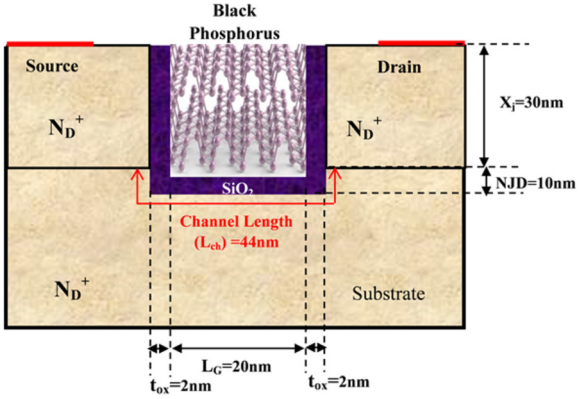


Fig. 1. Schematic structure of BP-JL-RC-MOSFET.

Table 1
Design parameters of BP-JL-RC-MOSFET and CRC-MOSFET.

Device Parameters	BP-JL-RC-MOSFET	CRC-MOSFET
Gate Length (L_g)	20 nm	20 nm
Channel Length (L_{ch})	44 nm	44 nm
Source and the Drain region	30 nm	30 nm
Length Width of the Device (W)	200 nm	200 nm
Groove Depth	38 nm	38 nm
Negative Junction Depth (NJD)	10 nm	10 nm
Substrate Doping	5×10^{16} cm^{-3} (N_D^+)	1×10^{17} cm^{-3} (N_A)
Source/Drain Doping (N_D^+)	5×10^{16} cm^{-3} (N_D^+)	1×10^{19} cm^{-3} (N_D^+)
Physical Oxide Thickness (t_{ox})	2 nm	2 nm
Metal work function (Φ)	5.16 eV	4.4 eV
Gate to source voltage (V_{gs})	1.5 V	1.5 V
Drain to source voltage (V_{ds})	0.2 V	0.2 V

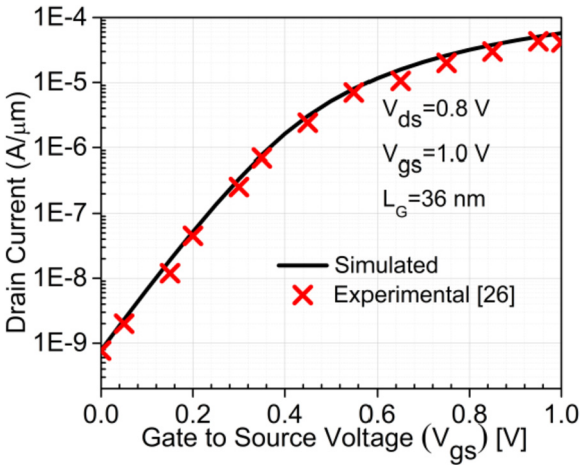


Fig. 2. Experimental and simulation of I_{ds}-V_{gs} characteristics of 36 nm gate length recessed channel MOSFET.

phosphorus is exfoliated, then aligned and transferred to the gate using a PDMS (polydimethylsiloxane) stamping method (PDMS stamps are pieces of polydimethylsiloxane, a silicone, that have usually been patterned against a master to form a relief pattern used in soft lithography) [21]. PMMA (Poly (methyl methacrylate)) was immediately spin-coated (acting as a temporary passivation layer) to minimize the black phosphorus degradation. At last, contact etches and metal deposition (using electron beam evaporation followed by lift-off) process is done. Thus, the BP-JL-RC-MOSFET can be fabricated using the above device design schemes, in which the benefits of the transparent gate engineering scheme have been combined with groove gate for accomplishing improved characteristics.

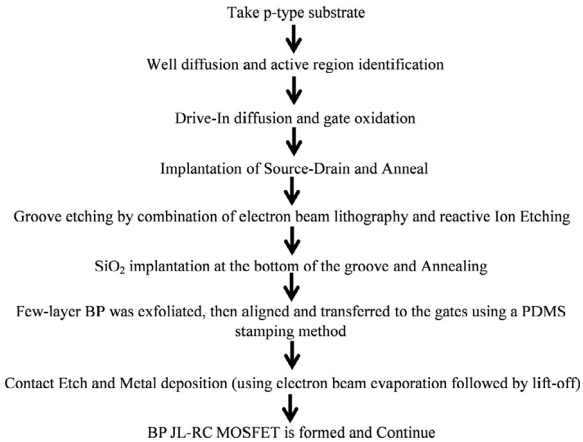


Fig. 3. Fabrication flowchart of BP-JL-RC-MOSFET.

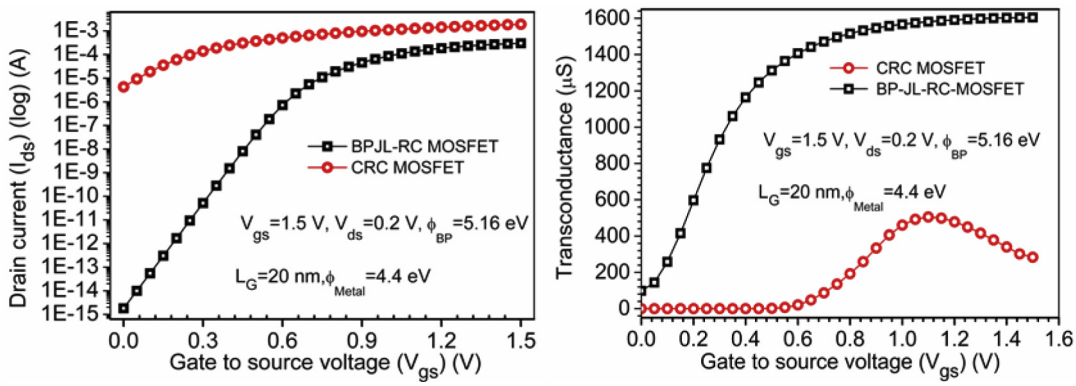


Fig. 4. (a): Transfer characteristics and (b): Transconductance; of CRC-MOSFET and BP-JL-RC-MOSFET.

5. Results and discussions

5.1. Analysis of analog performance

In order to investigate the impact of the Junctionless phenomenon in which black phosphorus is used as gate material on drain current, CRC and BP-JL-RC-MOSFET were simulated using ATLAS 3D device simulator [25]. Fig. 4(a–b) reflects the transfer characteristics and transconductance profile respectively, for BP-JL-RC and CRC devices. Drain current improves in the proposed device as shown in Fig. 4(a) and due to the improvement in drain current, Fig. 4(b) reflects the enhanced transconductance in BP-JL-RC-MOSFET as compared to CRC-MOSFET. It is clearly observed that large difference in off-currents (10^{-6} A and 10^{-11} A) is observed while on-currents (1.89×10^{-3} A and 3×10^{-4} A) are nearly equal between CRC and BP-JL-RC devices due to which the switching ratio of the proposed device is much higher than conventional one as shown in Fig. 5. Reduction in off-current is observed due to the presence of Junctionless phenomenon as well as amalgamation of black phosphorus in the groove (recessed) gate of BP-JL-RC-MOSFET. Black phosphorus improves the gate controllability and hence, shrinks HCEs and SCEs in BP-JL-RC-MOSFET. The switching capability and gate controllability in BP-JL-RC-MOSFET are achieved at a very low drain bias (0.2 V), and gate biasing is ramped from 0 to 1.5 V due to which BP-JL-RC device emerged as an ultra-low power device for analog applications. Fig. 5 also reflects the reduced sub-threshold slope in BP-JL-RC-MOSFET (67.2 mV/dec) as compared to the conventional device (151 mV/dec). The low sub-threshold slope is also responsible for higher switching performance of the device.

Fig. 6(a) and (b) shows the potential and contour plot along the channel for CRC and BP-JL-RC-MOSFET, and it is observed that the potential is higher in the channel region for BP-JL-RC-MOSFET as compared to the conventional device due to the incorporation of black phosphorus on to the recessed gate. Proposed device reflects the lowering of barrier potential at source side which indicates a reduction in DIBL and more pronounced in conventional MOSFET mainly due to the absence of junction in the BP-JL-RC-MOSFET. To evaluate analog parameters in BP-JL-RC-MOSFET and CRC-MOSFET, electric field and electron mobility are two important parameters. It is evident from Fig. 7(a) that, the channel electric field is enhanced by three-times in BP-JL-RC-MOSFET (9×10^5 V/cm) as compared to CRC-MOSFET (3×10^5 V/cm). Enhancement in channel electric field is due to the higher electron mobility of black phosphorus (shown in Fig. 7(b)) as well as junctionless profile of the BP-JL-RC-MOSFET

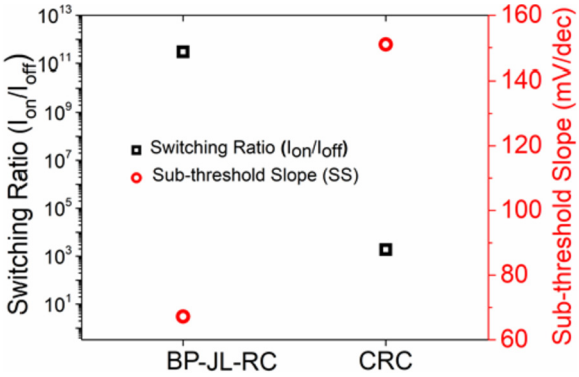


Fig. 5. Switching ratio and sub-threshold slope of BP-JL-RC-MOSFET and CRC-MOSFET.

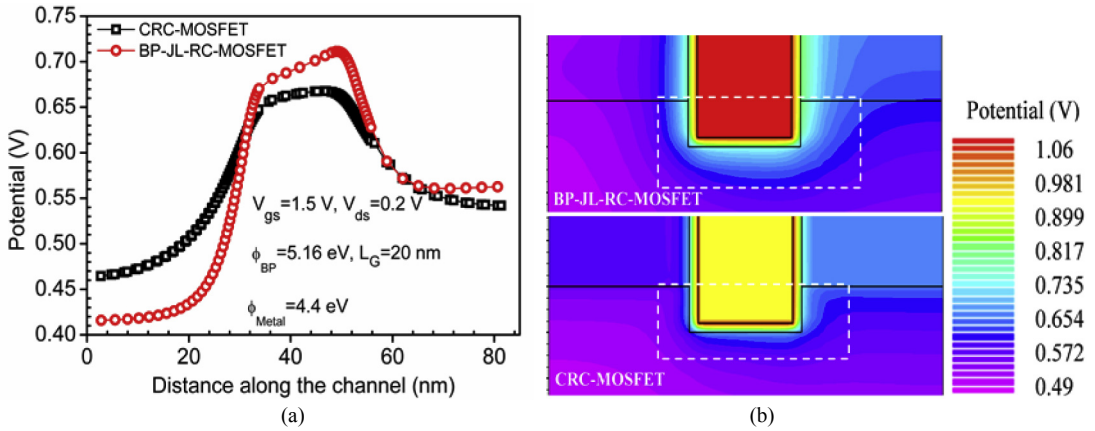


Fig. 6. (a) Potential, with respect to the distance along the channel for CRC and BP-JL-RC-MOSFET. (b) Contour plot CRC and BP-JL-RC-MOSFET.

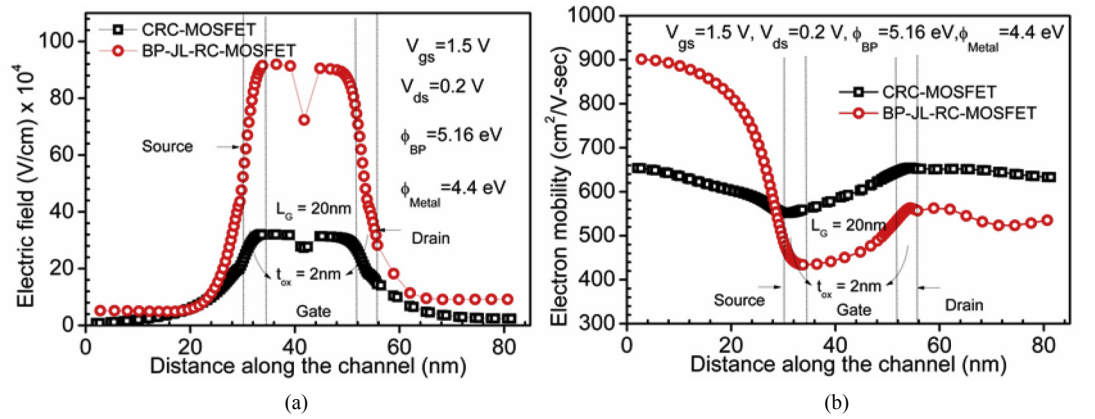


Fig. 7. (a) Electric field and (b) Electron mobility; with respect to the distance along the channel for CRC and BP-JL-RC-MOSFET.

in which electrons feel negligible resistance to reach from drain to source and hence, mobility of the charge carriers (present in channel region) is more at the source side as compared to drain side as shown in Fig. 7(b). Higher electron mobility is also one of the reason due to which the switching ratio is very high in BP-JL-RC-MOSFET (shown in Fig. 5).

Further, electron velocity and electron temperature have been evaluated for both the devices and it is found that electron velocity (shown in Fig. 8(a)) has enhanced significantly for BP-JL-RC-MOSFET as compared to the conventional device due to the enhancement in electric field as the electric field has a direct impact on the electron velocity. Due to the higher electron velocity, which is doubled in BP-JL-RC-MOSFET as compared to CRC-MOSFET, switching ratio is also high thus; BP-JL-RC device is a suitable candidate for higher switching applications. Fig. 8(b) reflects the variation of electron temperature for BP-JL-RC-MOSFET and CRC-MOSFET along the channel, and it is evident that electron temperature is varied from source to drain. First, the electron temperature of BP-JL-RC is high (470 K) as compared to CRC (350 K) at the source side but reduces in the channel region for BP-JL-RC (550 K) as compared to CRC (680 K) and it is very low (less varying) throughout the channel for BP-JL-RC-MOSFET. The electron temperature should be as low as possible for eliminating (minimizing) the leakage currents such as hot electron injected gate current and impact ionization substrate current for building it suitable for switching and ultra-low power applications. Low electron temperature is observed for BP-JL-RC due to Junctionless phenomenon and higher electron mobility of the device as well as gate material (black phosphorus) used in the recessed region.

5.2. Analysis of RF performance

Moreover, power gains are significant in the designing of RF amplifiers, but for the designing of low-noise amplifiers (LNA), stability is one of the primary standards. For the designing of an amplifier for very high frequency, oscillation should be avoided. Stability of an amplifier, also evaluated as Stern stability factor (K), ia found to have a value of K usually greater than one at high frequency and less than one at low frequency [28,29]. By using equation (1) [30,31], K can be defined as-

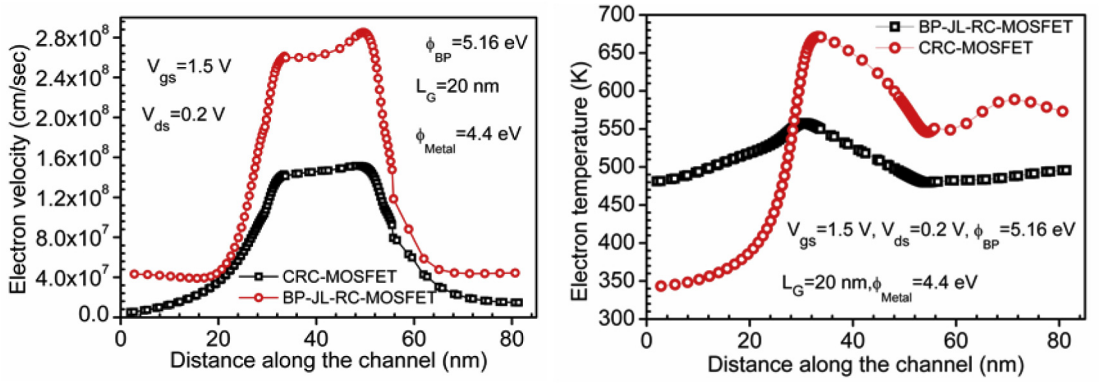


Fig. 8. (a) Electron temperature and (b) Electron velocity; with respect to the distance along the channel for CRC and BP-JL-RC-MOSFET.

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2.|S_{12.} \cdot S_{21}|} \tag{1}$$

where S_{11} and S_{22} represent the reflection coefficients and S_{12} and S_{21} are transmission coefficients, and s-matrix Δ is defined as

$$\Delta = S_{11} \times S_{22} - S_{12} \times S_{21} \tag{2}$$

K has been evaluated for both the devices as shown in Fig. 9. At high frequency, *K* is greater than one for the conventional device, and at very low frequencies, it is less than one while for the proposed device, it is ~1 (slightly > 1 at a higher frequency and <1 at low frequency) which is suitable for designing of RF amplifiers as shown in Fig. 9.

For RF applications, cut-off frequency, f_T [32] is considered when comparing transistors. f_T is a measurement of speed and swing for high-speed digital applications, and it is defined as given in equation (3) [33–35]:

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{3}$$

where transconductance is denoted by g_m and parasitic capacitances are denoted by C_{gd} and C_{gs}. f_T is evaluated when the current gain is unity [36]. Results show that f_T improves 3.88 times in BP-JL-RC-MOSFET as compared to CRC-MOSFET which is reflected in Fig. 9 due to enhanced ON current and transconductance (shown in Fig. 4(a) and (b)). Further, the analysis of maximum oscillator frequency (f_{MAX}) is more important for high switching and high speed of CMOS device. f_{MAX} should be as high as possible, and it is defined as given in equation (4) [36,37]:

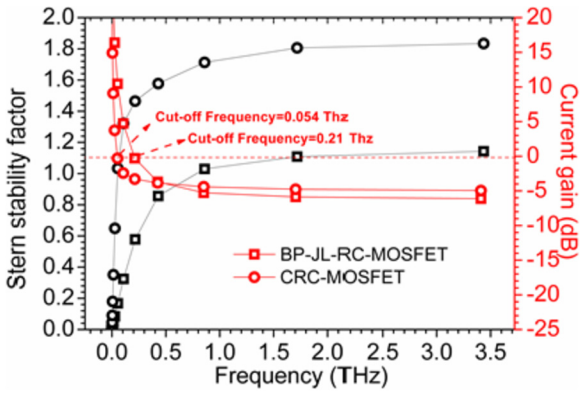


Fig. 9. Stern stability factor and Current gain (to find cut-off frequency) for CRC and BP-JL-RC-MOSFET.

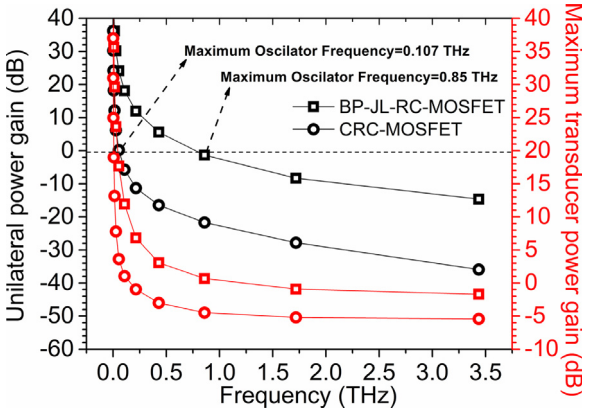


Fig. 10. Unilateral power gain (to find maximum oscillator frequency) and Maximum transducer power gain for CRC and BP-JL-RC-MOSFET.

$$f_{MAX} = \frac{f_T}{\sqrt{4R_g\left(g_{ds} + 2\pi f_T C_{gd}\right)}} \tag{4}$$

Sometimes f_{MAX} is also evaluated when the unilateral power gain is unity [32]. Fig. 10 reflects ~8 times higher f_{MAX} in BP-JL-RC-MOSFET due to the enhancement in carrier mobility (shown in Fig. 7(b)) which reduces gate resistance and hence improves f_{MAX}, as f_{MAX} is directly proportional to transconductance and inversely related to gate resistance [32]. A higher value of f_T and f_{MAX} show the ability of BP-JL-RC-MOSFET for RF applications.

Moreover, the device comparison of BP-JL-RC and CRC-MOSFET have been performed in terms of other RF metrics such as Gma (maximum available power gain) and Gms (maximum stable power gain). Fig. 11 shows the improved maximum theoretical power gain in BP-JL-RC-MOSFET as compared to the conventional device as required for high-frequency applications. In a two-port network, Gma is defined by the ratio of maximum power available at load to the maximum power available at the source, and it is given as in equation (5). For high frequency (THz) applications, Gma and Gms should be large for the device and thus; BP-JL-RC device shows a significant enhancement due to the useful electrical property of black phosphorus.

$$G_{ma} = \frac{P_{load,\max}}{P_{source,\max}} \tag{5}$$

Further, the parasitic capacitances have been evaluated as for the high performance of the device; parasitic capacitances should be as small as possible due to the dependency of speed of a transistor on parasitic capacitances [38,39], which causes a delay in logic-cell. Rise and fall times of a digital device may increase at the input and output side due to the parasitic capacitances as we know that, the maximum speed of a digital switching circuit mainly affects the rise time and fall time [40].

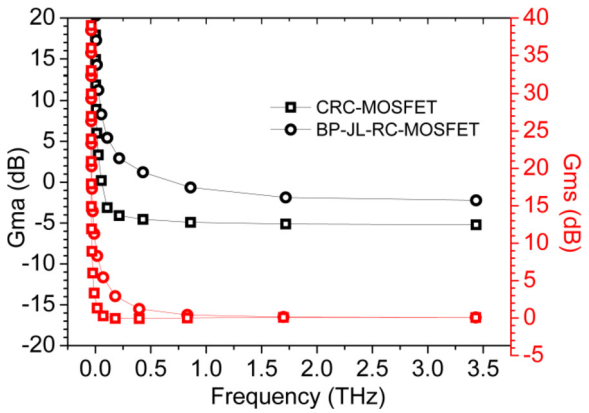


Fig. 11. Gma (Maximum Available Power Gain) and Gms (Maximum Stable Power Gain) for CRC and BP-JL-RC-MOSFET.

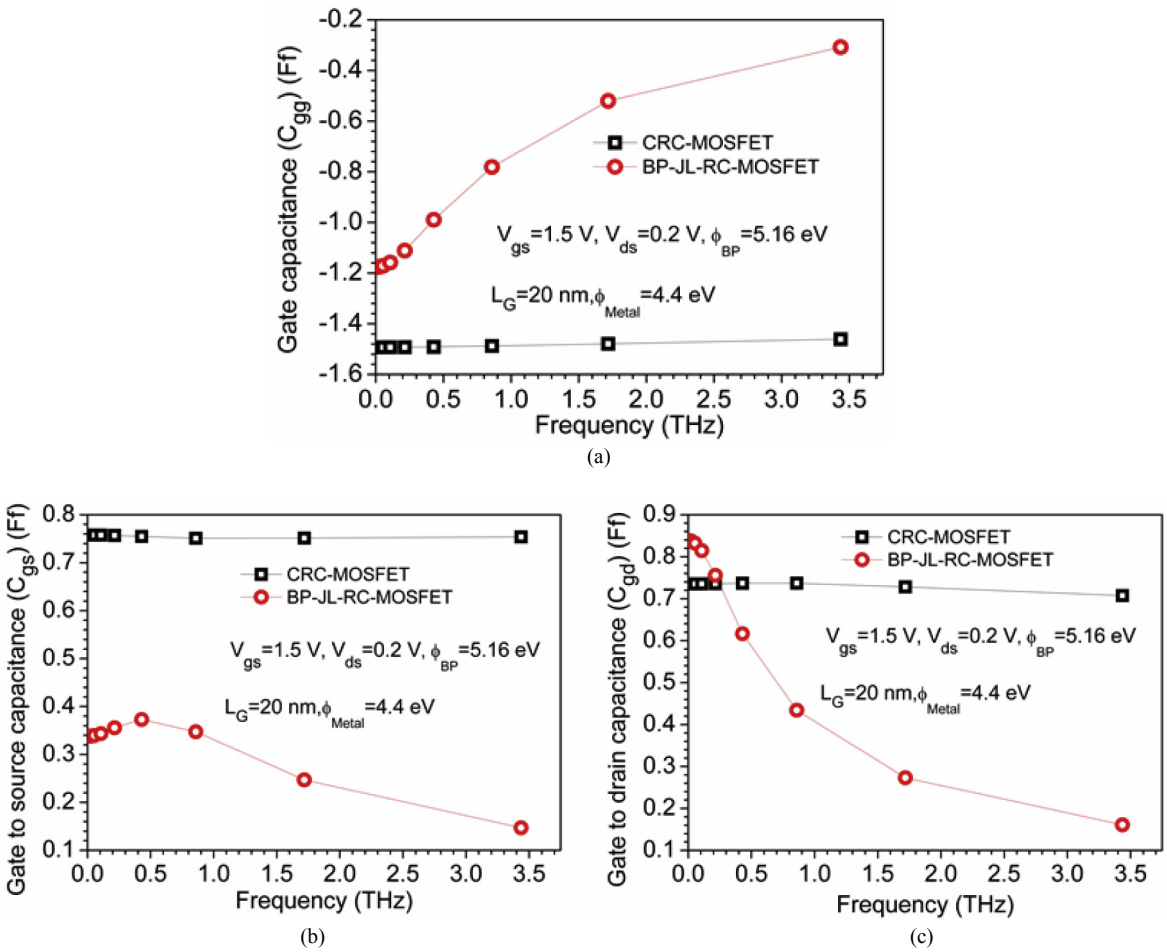


Fig. 12. (a): C_{gg}, (b) C_{gs} and (c) C_{gd} for CRC and BP-JL-RC-MOSFET.

Thus, for RF applications, the investigation of parasitic capacitances is necessary. Many RF amplifiers may have low gain, and sometimes oscillation occurs in the amplifier due to these parasitic losses (parasitic capacitances). In this section, parasitic capacitances have been evaluated in terms of gate capacitance (C_{gg}), the gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) shown in Fig. 12(a), (b) and (c) respectively for BP-JL-RC and CRC-MOSFET. Results show that BP-JL-RC-MOSFET exhibits very small C_{gg}, C_{gs} and C_{gd} as compared to CRC-MOSFET when frequency increases from few Hz to THz range due to the high carrier mobility across the channel (shown in Fig .7(b)) and junctionless phenomenon in BP-JL-RC-MOSFET. Thus, BP-JL-RC-MOSFET shows enhanced analog and RF FOMs as compared to CRC-MOSFET (see Table 2) which makes it for low power analog and RF applications.

Table 2
Summary of analog and RF FOMs.

Device/Parameters	BP-JL-RC-MOSFET	CRC-MOSFET
g_m (μS)	1600	500
I_{on}/I_{off}	3×10^{11}	1.9×10^{3}
Subthreshold slope (mV/dec)	67.2	151
Electric field (V/cm)	9×10^{5}	3×10^{5}
Electron mobility ($cm^2V^{-1}s^{-1}$)	900	650
Electron temperature (K)	550	680
f_T (THz)	0.21	0.0536
f_{MAX} (THz)	0.85	0.107
C_{gs} (ff)	0.15	0.75
C_{gd} (ff)	0.15	0.7
C_{gg} (ff)	0.3	1.5

6. Conclusion

This analysis examines the effectiveness of black phosphorus, a new class of material as a gate metal and a junctionless technology on to the RC MOSFET. This study is done in terms of analog and RF FOMs at room temperature (300 K). Results so obtained reveals that black phosphorus significantly enhances the ON-current, whereas junctionless scheme reduces OFF-current remarkably which thus improves the switching ratio and thus, the analog performance of RC MOSFET at a low bias voltage. Moreover, it is observed that parasitic capacitances which hamper the device performance at high frequency are greatly reduced in BP-JL-RC-MOSFET in comparison to the conventional counterpart. Also, f_T (3.88 times) and f_{MAX} (~8 times) is enhanced significantly, which makes BP-JL-RC-MOSFET a potential candidate for low power analog and RF applications.

Acknowledgement

The authors are thankful to University Grants Commission (UGC), Electrical Engineering Department, Microelectronics Research Lab, and Delhi Technological to carry out this work.

References

[1] M. Saito, M. Ono, R. Fujimoto, H. Tanimoto, N. Ito, T. Yoshitomi, T. Ohguro, H.S. Momose, H. Iwai, 0.15-μm RF CMOS technology compatible with logic CMOS for low-voltage operation, IEEE Trans. Electron. Dev. 45 (3) (1998) 737–742.
[2] L.E. Larson, Silicon technology tradeoffs for radio-frequency/mixed-signal "systems-on-a-chip", IEEE Trans. Electron. Dev. 50 (3) (2003) 683–699.
[3] V. Kilchytska, A. Nève, L. Vancaillie, D. Levacq, S. Adriaensen, H. Van Meer, K. De Meyer, C. Raynaud, M. Dehan, J.-P. Raskin, Influence of device engineering on the analog and RF performances of SOI MOSFETs, IEEE Trans. Electron. Dev. 50 (3) (2003) 577–588.
[4] J.-Y. Yang, K. Benaissa, D. Crenshaw, B. Williams, S. Sridhar, J. Ai, G. Boselli, S. Zhao, S.-P. Tang, N. Mahalingam, 0.1 μm RFCMOS on high resistivity substrates for system on chip (SOC) applications, in: IEDm: International Electron Devices Meeting, 2002, pp. 667–670.
[5] R. Murali, J.D. Meindl, Modeling the effect of source/drain junction depth on bulk-MOSFET scaling, Solid State Electron. 51 (6) (2007) 823–827.
[6] Q.B. Chen, Compact modeling of multi-gate MOSFETs for RF designs, in: 2013 IEEE International Wireless Symposium (IWS), 2013.
[7] Z.-H. Liu, C. Hu, J.-H. Huang, T.-Y. Chan, M.-C. Jeng, P.K. Ko, Y.C. Cheng, Threshold voltage model for deep-submicrometer MOSFETs, IEEE Trans. Electron. Dev. 40 (1) (1993) 86–95.
[8] E. Takeda, C.Y.-W. Yang, A. Miura-Hamada, Hot-Carrier Effects in MOS Devices, Academic Press, 1995.
[9] C.V. Mouli, SOI Device with Reduced Drain Induced Barrier Lowering, 2009. Google Patents.
[10] A. Kumar, N. Gupta, R. Chaujar, Analysis of novel transparent gate recessed channel (TGRC) MOSFET for improved analog behaviour, Microsyst. Technol. 22 (11) (2016) 2665–2671.
[11] J.-i. Nishizawa, T. Ohmi, Short Channel MOSFET with Buried Anti-punch through Region, 1995. Google Patents.
[12] R. Chaujar, R. Kaur, M. Saxena, M. Gupta, R. Gupta, TCAD assessment of gate electrode workfunction engineered recessed channel (GEWE-RC) MOSFET and its multilayered gate architecture—part I: hot-carrier-reliability evaluation, IEEE Trans. Electron. Dev. 55 (10) (2008) 2602–2613.
[13] K.-T. Lam, Z. Dong, J. Guo, Performance limits projection of black phosphorous field-effect transistors, IEEE Electron. Device Lett. 35 (9) (2014) 963–965.
[14] H. Liu, A.T. Neal, Z. Zhu, Z. Luo, X. Xu, D. Tománek, D.Y. Peide, Phosphorene: an Unexplored 2D Semiconductor with a High Hole Mobility, 2014.
[15] A. Castellanos-Gomez, L. Vicarelli, E. Prada, J.O. Island, K. Narasimha-Acharya, S.I. Blanter, D.J. Groenendijk, M. Buscema, G.A. Steele, J. Alvarez, Isolation and characterization of few-layer black phosphorus, 2D Mater. 1 (2) (2014), 025001.
[16] S. Das, W. Zhang, M. Demarteau, A. Hoffmann, M. Dubey, A. Roelofs, Tunable transport gap in phosphorene, Nano Lett. 14 (10) (2014) 5733–5739.
[17] F. Schwierz, Graphene transistors, Nat. Nanotechnol. 5 (7) (2010) 487–496.
[18] C. Gong, H. Zhang, W. Wang, L. Colombo, R.M. Wallace, K. Cho, Band alignment of two-dimensional transition metal dichalcogenides: application in tunnel field effect transistors, Appl. Phys. Lett. 103 (5) (2013), 053513.
[19] H. Fang, S. Chuang, T.C. Chang, K. Takei, T. Takahashi, A. Javey, High-performance single layered WSe2 p-FETs with chemically doped contacts, Nano Lett. 12 (7) (2012) 3788–3792.
[20] N.R. Pradhan, D. Rhodes, S. Feng, Y. Xin, S. Memaran, B.-H. Moon, H. Terrones, M. Terrones, L. Balicas, Field-effect transistors based on few-layered α-MoTe2, ACS Nano 8 (6) (2014) 5911–5920.
[21] M.C. Robbins, S.J. Koester, Black phosphorus p-and n-MOSFETs with electrostatically doped contacts, IEEE Electron. Device Lett. 38 (2) (2017) 285–288.
[22] N. Haratipour, S.J. Koester, Ambipolar black phosphorus MOSFETs with record n-channel transconductance, IEEE Electron. Device Lett. 37 (1) (2016) 103–106.
[23] F. D'Agostino, D. Quercia, Short-channel Effects in MOSFETs, Introduction to VLSI Design (EECS 467), 2000.
[24] J. Colinge, C. Lee, N.D. Akhavan, R. Yan, I. Ferain, P. Razavi, A. Kranti, R. Yu, Junctionless Transistors: Physics and Properties, Semiconductor-on-insulator Materials for Nanoelectronics Applications, Springer, 2011, pp. 187–200.
[25] I. Silvaco, ATLAS User's Manual, 2011. Santa Clara, CA, Ver 5.
[26] J. Appenzeller, R. Martel, P. Avouris, J. Knoch, J. Scholvin, J.A. del Alamo, P. Rice, P. Solomon, Sub-40 nm SOI V-groove n-MOSFETs, IEEE Electron. Device Lett. 23 (2) (2002) 100–102.
[27] M. Xiao-Hua, H. Yue, S. Bao-Gang, G. Hai-Xia, R. Hong-Xia, Z. Jin-Cheng, Z. Jin-Feng, Z. Xiao-Ju, Z. Wei-Dong, Fabrication and characterization of groove-gate MOSFETs based on a self-aligned CMOS process, Chin. Phys. 15 (1) (2006) 195.
[28] S.K. Pati, K. Koley, A. Dutta, N. Mohankumar, C.K. Sarkar, Study of body and oxide thickness variation on analog and RF performance of underlap DG-MOSFETs, Microelectron. Reliab. 54 (6–7) (2014) 1137–1142.
[29] E. Dastjerdy, R. Ghayour, H. Sarvari, Simulation and analysis of the frequency performance of a new silicon nanowire MOSFET structure, Phys. E Low-dimens. Syst. Nanostruct. 45 (2012) 66–71.
[30] A. Kumar, N. Gupta, R. Chaujar, Power gain assessment of ITO based Transparent Gate Recessed Channel (TGRC) MOSFET for RF/wireless applications, Superlattice. Microst. 91 (2016) 290–301.
[31] N. Gupta, A. Kumar, R. Chaujar, Impact of device parameter variation on RF performance of gate electrode workfunction engineered (GEWE)-silicon nanowire (SiNW) MOSFET, J. Comput. Electron. 14 (3) (2015) 798–810.
[32] A. Sarkar, R. Jana, The influence of gate underlap on analog and RF performance of III–V heterostructure double gate MOSFET, Superlattice. Microst. 73 (2014) 256–267.
[33] A. Kumar, N. Gupta, R. Chaujar, TCAD RF performance investigation of transparent gate recessed channel MOSFET, Microelectron. J. 49 (2016) 36–42.
[34] A. Kumar, M. Tripathi, R. Chaujar, Reliability issues of In2O5Sn gate electrode recessed channel MOSFET: impact of interface trap charges and temperature, IEEE Trans. Electron. Dev. 99 (3) (2018) 1–7.
[35] A. Kumar, Effect of trench depth and gate length shrinking assessment on the analog and linearity performance of TGRC-MOSFET, Superlattice. Microst. 109 (2017) 626–640.

[36] B. Nae, A. Lazaro, B. Iniguez, High frequency and noise model of gate-all-around MOSFETs, in: Electron Devices, 2009. CDE 2009. Spanish Conference on, IEEE, 2009, pp. 112–115.
[37] N. Gupta, R. Chaujar, Investigation of temperature variations on analog/RF and linearity performance of stacked gate GEWE-SiNW MOSFET for improved device reliability, Microelectron. Reliab. 64 (2016) 235–241.
[38] N.R. Mohapatra, M.P. Desai, S.G. Narendra, V.R. Rao, Modeling of parasitic capacitances in deep submicrometer conventional and high-K dielectric MOS transistors, IEEE Trans. Electron. Dev. 50 (4) (2003) 959–966.
[39] A. Kumar, M. Tripathi, R. Chaujar, Investigation of parasitic capacitances of In2O5Sn gate electrode recessed channel MOSFET for ULSI switching applications, Microsyst. Technol. 23 (12) (2017) 5867–5874.
[40] P. Malik, R.S. Gupta, R. Chaujar, M. Gupta, AC analysis of nanoscale GME-TRC MOSFET for microwave and RF applications, Microelectron. Reliab. 52 (1) (2012) 151–158.