M. Tech (VLSI Design & Embedded System) HARPREET KAUR 2018

IMPLEMENTATION OF ANALOG CIRCUITS USING CD-DITA

A PROJECT REPORT

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE AWARD OF THE DEGREE
OF

MASTER OF TECHNOLOGY
IN
VLSI Design &Embedded System

Submitted by:

HARPREET KAUR

2K16/VLS/10

Under the supervision of

Mr. A. K. SINGH
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Electronics & Communication Engineering
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CANDIDATE'S DECLARATION

I, Harpreet Kaur, Roll No. 2K16/VLS/10, student of M. Tech. (VLSI DESIGN AND EMBEDDED SYSTEM), hereby declare that the project Dissertation titled "IMPLEMENTATION OF ANALOG CIRCUITS USING CD-DITA" which is submitted by me to the Department of ELECTRONICS AND COMMUNICATION ENGINEERING, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associate ship, Fellowship or other similar title or recognition.

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CERTIFICATE

I hereby certify that the Project Dissertation titled "IMPLEMENTATION OF ANALOG CIRCUITS USING CD-DITA" which is submitted by HARPREET KAUR, Roll No 2K16/VLS/10 Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the students under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ACKNOWLEDGEMENT

I express my deepest gratitude to my project guide Associate Prof. A. K. SINGH, Department of Electronics and Communication Engineering, Delhi Technological University whose encouragement, guidance and support from the initial to the final level enabled me to develop an understanding of the subject. His suggestions and ways of summarizing the things made me to go for independent studying and trying my best to get the maximum in my topic, this made my circle of knowledge very vast. I am highly thankful to him for guiding me in this project.

I also wish to express my gratitude to Prof. S. Indu (HOD, ECE Dept.), Prof. D. R. Bhaskar, Prof. Neeta Pandey and Prof. Rajeshwari Pandey for their constant support and guidance.

Finally, I take this opportunity to extend my deep appreciation to my family and friends, for all that they meant to me during the crucial times of the completion of my project.

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M. Tech. (VLSI)

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LIST OF ABBREVIATIONS

Abbreviation	Full Form
IC	Integrated Circuit
CMOS	Complementary Metal Oxide Semiconductor
DSP	Digital Signal Processing
ADC	Analog to Digital Convertor
DAC	Digital to Analog Convertor
DC	Direct Current
AC	Alternating Current
VLSI	Very Large Scale Integration
CM	Current Mode
VM	Voltage Mode
MM	Mixed Mode
Op-Amp	Operational Amplifier
SR	Slew Rate
ASP	Analog Signal Processing
ABBs	Active Building Blocks
MOS	Metal Oxide Semiconductor
CC	Current Conveyor
CCII	2^{nd} generation Current Conveyor
CFOA	Current Feedback Operational Amplifier
BJT	Bipolar Junction Transistor
TA	Transconductance Amplifier
LPF	Low Pass Filter
BPF	Band Pass Filter

HPF	High Pass Filter
BRF	Band Reject Filter
APF	All Pass Filter
MIMO	Multiple Input Multiple Output
SIMO	Single Input Multiple Output
CDTA	Current Differencing Transconductance Amplifier
CD-DITA	Current Differencing Differential Input Transconductance Amplifier
VCCS	Voltage Controlled Current Source
DVCCS	Differential Voltage Controlled Current Source
DCCCS	Differential Current Controlled Current Source
CDU	Current Differencing Unit
FVF	Flip Voltage Follower
OTA	Operational Transconductance Amplifier
DO-OTA	Dual Output OTA
FVFCS.	Flip Voltage Follower Current Source
B.W	Bandwidth
CDBA	Current Differencing Buffered Amplifier
DDCC	Differential Difference Current Conveyor
OTRA	Operational Transresistance Amplifier
DVCC	Differential Voltage Current Conveyor
DVCCII	2nd Generation Differential Voltage Current Conveyor
FBVDBA	Full- Balanced Voltage Differencing Buffered Amplifier
TIM	Trans Impedance Mode
TAM	Trans Admittance Mode
CCCII	2nd generation Current Controlled Current Conveyor

CCCDTA	Current Control CDTA
DDCC	Differential Difference Current Conveyor
OTRA	Operational Transresistance Amplifier
VD-DIBA	Voltage Differencing – Differential input Buffered Amplifier

ABSTRACT

CD-DITA based basic filtering applications such as first order APF and current mode SIMO-type universal biquad filter have been implemented and CD-DITA based grounded inductor and mixed mode filter have been proposed. CD-DITA is an extension of CDTA having extra voltage input than CDTA increasing its usability of differential inputs. For a suitable CMOS based implementation of CD-DITA, several CDTA realizations are studied and the suitable one is modified to implement the proposed CD-DITA block. A FVF based CD-DITA is characterized and its applications in analog signal processing circuits such as basic current amplifier, adder subtractor and integrator are also studied. The proposed CD-DITA based grounded inductor is realized with one resistors and one capacitor and further using proposed inductor band pass filter has been simulated. The proposed CD-DITA based mixed mode filter using two resistors and two capacitors with independent tuning of natural frequency and quality factor is simulated. The proposed filter also offers low active and passive sensitivities. In addition, the effects of parasitics and errors on the proposed filter are also investigated. The characteristics of CD-DITA and its applications are verified by PSPICE simulations using TSMC 0.25μm CMOS technology. The characteristics of CD-DITA and validity of proposed biquad filter is verified by SPICE simulation using TSMC 180nm technology.

Chapter 1

Introduction

The efficient and compact implementation of various types of digital and analog signal processing algorithms is possible on silicon chip due to the evolution of integrated circuit (IC) technology. Simulation of any block or function indigital domain has been easier due to the evolution of CMOS technology to lower technology nodes. Using CMOS technique,more efficient and smaller in size circuits can be designed.

Although the functions can be implemented and handled efficiently, digital signal processing (DSP) also faces some issues such as:

- **Additional complexity:** Every signal is analogue in nature. So Analog to Digital Converter (ADC) and Digital to Analog Converter (DAC) have to be used before processing any analogue information into digital. Also the reconstruction filters contribute to system complexity.
- **Limited bandwidth:** Wireless transmission of digital signals is not possible and transmission of digital signals for long distance using cables causes distortion and attenuation. Hence repeaters should be used to regenerate these signals and thus bandwidth is limited for digital signals
- **Clock skew:** Clock skew is also called timing skew and occurs in synchronous digital circuits. It's a phenomenon in which the sourced clock will arrive at different times at different components in the same circuit, thus causing skew between any two clocks**.** Thus clock skew arises due to the distribution of a large amount of data and timing of clock over a large chip.
- **Trade-off:** A trade-off is there between operating frequency, power dissipation, cost, noise and level of the interferer.

However, there are many analogue domain functions for example signal rectification, signal amplification, conversion of signals from analog to digital and digital to analog, continuous time filtering that cannot be performed by digital circuits [1].

Hence to implement the above functions, analogue circuits holding high speed of operation with high precision are needed. As the technology is shifting to lower technology nodes,

analogue circuits should also attain features of low power dissipation and operate on low supplies [2].

1.1 Development of technologies:

Since the establishment of the integrated circuits, the operational amplifiers (Op-Amp) have been used as the main and basic building block in analogue circuit design applications. Since then, new analogue applications have been found and the performance conditions for analogue circuits have been changed.

In Voltage mode (VM) Op-Amp blocks very high closed loop gains trade off with bandwidth is present. It means op-amp have limited bandwidth due to the constant gain-bandwidth product at high closed-loop gains. Further, op-amps also suffer from the limited slew rate that in turn affects the large signal operation and also high frequency operation.

When any application demands wide bandwidth, low-voltage and low power operations simultaneously, the VM op-amp becomes very complex and also their characteristics are not needed e.g. DC accuracy. Similarly on the other hand, the circuit techniques that are used in radio or high frequency applications are usually simple so that required accuracy can be achieved. Therefore there is always a growing need for new circuit techniques.

1.2. Voltage and current mode signal processing :-

Since the last two decades in VLSI design, the development of the latest analogue applications have been following the lead of the so called current mode techniques due to the advantages it offers over the VM. Any application is said to be processed in Current Mode (CM), when the information processed is in the form of currents instead of the conventional VM.

Another important advantage of CM over VM is use of the low supply voltages because the design of CM blocks deals with the processing of current signals that can be achieved with lower voltage swings .Also the mixed mode (MM) blocks are also synthesized and analyzed along with developing the CM blocks. From the literature survey its known that CM blocks or techniques always provide a large number of important analogue signal processing (ASP) and signal generator applications. Due to large growth in IC technology in last two decades, the

circuit designers have exploited the CM analogue techniques to provide the efficient solutions to many circuit design problems. As a result, the CM approach for many analogue signal processing applications offers many advantages like as

- High Operating Frequency Range.
- High Slew Rate(SR)
- High Precision
- Better Linearity
- Accuracy
- Low Power Dissipation.

While comparing VM and CM blocks, we should consider that here is no perfect or precise definition for any block to be current mode or voltage mode. Some authors say that signals are represented through currents in CM blocks and by voltages in VM blocks. But in every circuit a node has associated voltage and each branch has a current.

In spite of this, CM approach has a large impact on IC design**.** Our procedure is basically finding circuit realizations that are alternative of the exited circuits but are simple. So for this, the procedure is basically using current signals rather than voltage signals for signal processing applications.

1.3. Motivation for CM design circuit:

One method for finding the substitute of these VM circuit techniques is to go for current signals instead of voltage signals for ASP. Circuits with MOS transistors are highly simplified with the usage of current signals for processing in-stead of voltage signals. Also CM integrated circuit realizations are more immediate to transistor level design than the conventional VM realizations and thus results in simpler systems and circuits. Where in the circuits, wide distribution of signals as voltages and the parasitic effects are more in the form of more capacitances which are discharged and charged with full dynamic voltage swing which results in limited speed and increase in dynamic consumption of power in VM circuits.

In CM circuits, it is difficult to avoid nodes having higher voltage swing but the positive side is these nodes usually come with relatively less parasitic capacitances [3]. Thus it results in higher speed and very low power dissipation.

When the current input signal is applied to a MOS transistor, the voltage developed will be directly proportional to square root of the input current, if all the transistors are assumed to be operating in saturation region. In the similar way, in BJT circuits voltage are logarithmic functions of input signal. Therefore, the voltage swing compression also results in reduction of voltage supply in CM blocks. This very feature is used in many applications such as log filters [4], switched current filters [5], and nonlinear applications of CM usually. But unfortunately, due to the result of mismatching of the devices, this nonlinearity can cause an enormous distortion for the applications which need high linearity specifications or conditions. Therefore, many CM circuits need to utilize more techniques to provide linearity in the circuits.

1.4. Evolvement of CM blocks:

The very first building block meant for current signal processing was published in 1968 [6], and was named as current-conveyor (CC). And the enhanced version of the first generation of CC appeared in 1970 and named as the 2ndgeneration CCII [7] but due to the introduction of the integrated voltage mode operational amplifier none of these CC got popular at that time.

In 1980's, First fast pnp transistors were introduced in the bipolar ICs. In the mean while, the research institutes started noticing problems in the analogue design using the VM Op-Amp and hence it was not clearly the optimal solution to all analogue applications. New researches on CM signal processing with various applications using CC were presented. Furthermore, a new block was available i.e. Current Feedback Op-Amp (CFOA) [8]. The main advantages that CFOA offered over Op-Amp were high bandwidth and high SR due to which it gained popularity in video applications.

Mostly used CCs and the CFOAs relied on the complementary BJT technology. In order to realize the CM circuits with cheap circuit technologies, various kinds of circuit topologies and operational principles were needed. Therefore, in 1988 current mirror using MOS was presented [9].

The primary set of the active building blocks (ABBs) for analogue applications and signal processing applications is developing basically in two modes i.e. the first way that basic blocks that are already presented should be modified to new active blocks such as current mirrors, trans-conductance amplifiers (TA), CCs, voltage feedback amplifiers and also CFOA. The requirement for these modified blocks is that these should have simple structure so that high speed operation is achieved and also low power dissipation. The 2nd way is to characterize these ABBs with new elements.

For novel ABBs, some factors that one should seek are:

- Universality of ABB should be increased
- Electronic control of parameters
- Reduction or elimination of parasitics
- Design circuit application with minimum no. of ABBs and also minimum no of Passive components
- To find the solutions for trading off between the accuracy and speed

Current-differencing differential-input transconductance-amplifier (abbreviated CD-DITA) i.e. is an extension to Current-Differencing Transconductance-Amplifier (CDTA) is one among these ABBs. This block has been characterized by high output and low input impedances and thus making it suitable for the implementation of various ASP applications in CM. The universality of the CD-DITA block leads to the applications using less active and passive components and leading to simpler circuits.

1.5. Objective:

In accordance with the above discussion, the work in this thesis has mainly concentrated its attention on the objectives that has to be achieved for CD-DITA and these objectives are given as:-

- Design of the CD-DITA block
- Development of CD-DITA block
- Design of various applications employing single CD-DITA block

Objectives of this thesis is to modify the existing applications and also to implement new applications such as realizing CD-DITA based proposed grounded inductor and employing its BPF application, implementing CD-DITA based CM universal filter of single-input multi-output (SIMO)-type configuration, implementing first order all pass filter (APF) using CD-DITA, designing and implementing one CD-DITA based proposed MM filter of multi-input multi-output (MIMO)-type configuration. To meet the objective of this work, the existing and the proposed designs have been simulated by using the PSPICE software in 0.250um TSMC technology node i.e. for grounded inductance simulation and 180nm TSMC technology node i.e. for filter applications. Also, the simulated results have been compared with the theoretical results.

1.6. Organization of Thesis:

Chapter 1: Presents the brief introduction of the current mode signal processing in analogue circuit design. In this chapter the motivation for CM blocks and also the objective of the work in thesis have been discussed.

Chapter 2: A brief survey of both CDTA and CD-DITA literature and the survey of several grounded inductor circuits, CM biquad filter circuits employing CM ABBs and MM filter are presented.

Chapter 3: FVF based and Translinear Loop Based CD-DITA has been realized and its non-idealities are studied and simulated. It's DC and AC responses have been characterized and various performance parameters have been extracted through simulations.

Chapter 4: Some basic mathematical signal processing applications and filtering applications has been implemented using FVF based and TL based CD-DITA respectively.

Chapter 5: Proposed grounded inductor and CD-DITA based Proposed MM-MIMO filter has been implemented.

Chapter 7: This chapter presents summary of the work presented in this thesis and the future work has been discussed.

Chapter 2

Literature Survey

2.1 Introduction:

In the past few years, the CM analogue signal processing blocks have received a considerable amount of interest due to its advantages over VM blocks which have been explained briefly in this chapter. As a result of this CM analogue blocks have been emerged, CDTA and CD-DITA are among of these blocks. D. Biolek [10] . The basic block diagram of the CDTA and CD-DITA block is shown in Fig. 2.1(a)

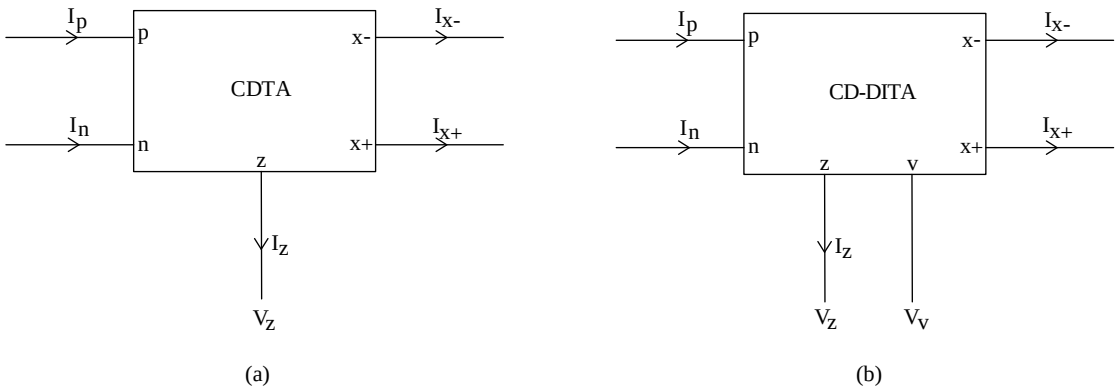


Fig. 2.1 Block diagrams (a) CDTA (b) CD-DITA

CDTA can be seen as a cascading of current differencing unit (CDU) and an operational transconductance amplifier (OTA). CDTA has two low-impedance input terminals n and p, CDU takes the difference of the input signals and then transfer this difference to the intermediate terminal z, and this current is converted into voltage via external impedance connected at the z- terminal. This voltage is again converted back into balanced currents I_{x+} and I_{x-} at $x\pm$ terminal with the gain of OTA i.e. g_m.

CDTA finds many applications in the circuits which are highly sensitive to the stray capacitances because CDTA have input terminals with low-impedance nodes. Thus this advantage makes CDTA a very useful and right choice for the high frequency applications.

CDTA block has been referred to as a true CM block in the literature because it is a current input and current output block.

CD-DITA is an improved version of CDTA. CD-DITA employs one differential-input OTA instead of using a single-input OTA which has been used in the traditional CDTA as shown in the Fig 2.1(b). This active element can provide various applications with advance features and characteristics such as employing minimum passive elements, providing the electronic tenability and controllability of various parameters like gain and quality factor and also realizing MM operation.

A very vast literature is offered on CDTA block which specifically includes realization of CDTA [11] using various techniques and a large variety of the CDTA based signal generation and processing applications [12-13]. However it is obvious from the literature survey, that the CD-DITA has found only single application, i.e. VM first-order APF presented in [14]. This work offers the development of CD-DITA block and its applications in CM and MM filtering area.

2.2 Review of CD-DITA Implementations:

CD-DITA has been derived from CDTA with opening v terminal which was initially grounded; the basic internal circuitry of CD-DITA remains same as of CDTA except the v terminal. So, let's proceed with the review of the Wide-ranging literature of CDTA which suggests that the both bipolar [11], and CMOS [12-13] technologies have been used for implementing CDTA block.

CDTA realization using bipolar technology is presented in [17]. The advantages of BJT based CDTA is its large overall gain when compared to the CMOS based implementations.BJT based CDTA suffers from high power dissipation due to the leakages in BJT.

CMOS technology based CDTA structures have also been presented in the literature [18]. These circuits hold an advantage of very high impedance at z -terminal. A low power CMOS realization of CDTA has been presented in [19]. In this structure, flipped voltage follower (FVF) has been used to construct the input stages, because FVF based CDTA offers very low resistances at input terminals. One more CMOS based CDTA structure is given in [20]. This structure exhibits very low impedance at the inputs and high output impedance (typically in $G\Omega$).

A comparison of all the available CDTA structures in terms of technology, supply voltage, gain and number of transistors, terminal impedances and power dissipation is shown in the table 2.1

Table 2.1 Comparison of several CDTA structures

Ref	Technology used	Supply Voltage	Bias current	Transconductance gain (g_m)	Power dissipation	Impedances at p, n and z
[11]	Bipolar	±3V	100 μA	2 mS	-	-
[17]	Bipolar	±2.5V	50 μA	0.96 mS	-	-
[22]	Bipolar	±1.5V	100 μA	-	8.11 mW	
[18]	0.25 μ CMOS	±1.2V	150 μA	624.9 μS	-	-
[19]	0.35 μ CMOS	±0.75V	54 μA	210 μS	0.37 mW	-
[23]	0.35 μ CMOS	±1.5V	100 μA	673 μS	3.61 mW	812 Ω, 348 Ω, 1.08 MΩ
[20]	0.5 μ CMOS	±2.5V	125 μA	670 μS	1.4 mW	654 Ω, 506 Ω, 1GΩ

2.3 Review of CM universal filters:

Analogue active filter is commonly used block for ASP. This block finds various applications in many fields, such as control systems, wireless communications and instrumentation signal measurement [25]. The synthesis and design of the analogue active filter circuits using electronically controllable blocks i.e. ABBs, taking several measures into account, for example minimum number of the active and passive elements used for implementing any circuit or others, has been receiving significant attention now a days.

Such ABBs provides convenience, versatility, flexibility for analogue circuit designer. Recently, the filters namely the universal or multifunction biquadratic filters, that can perform several functions using only single topology have been receiving significant attention from designers. The most popular universal analogue filters topology among all these filter topologies is a SIMO type CM filters. By simply just applying one current input signal, basic

filter applications such as LPF, BPF and HPF can be realized simultaneously and then by connecting various current outputs the remaining two filter functions such as BRF and APF can be realized simultaneously.

Many universal biquadratic filter configurations employing different ABBs, holding CM-SIMO type topology, have been designed and also implemented in past two decades. The main comparison of various active blocks is given in table 2.2. The CD-DITA based CM-SIMO filter is also compared with these filters and its advantages and disadvantages are also discussed in the coming chapters.

Table 2.2 Comparison of various CM-SIMO universal filters

Reference	**No. of ABBs**	**No. of Resistors used**	**No. of Capacitors Used**	**Electronic Tunability**	**All 5 filter responses realized**
[26]	1	4	2	NO	NO
[27]	1	4	3	NO	NO
[28]	1	2	2	NO	NO
[29]	1	2	2	NO	NO
[17]	1	1	2	YES	NO
[30]	1	1	2	YES	NO
[31]	1	3	2	NO	YES
[32]	1	2	2	YES	YES
CD-DITA	1	1	2	YES	YES

2.4 Review of Grounded Inductor Simulations:-

In the network synthesis using active element to replace the actual bulky inductor there is a huge demand of grounded simulated inductor [33]. Several active elements to simulate grounded inductance such as op-amps [34], CCs [35], CCCIIs [36], CFOAs [37], DVCCIIs [38], CDTAs [39], DVCCs [40] have been reported in the vast literature and in this work a new grounded inductor has been simulated using CD-DITA.

In the table given below the comparison of various grounded inductor configurations with the proposed Grounded Inductor based on CD-DITA has been presented.

Table 2.3:- Comparison of Various Grounded Inductor configurations with the New Proposed Grounded Inductor

Ref.	No. of Active elements used	No. of resistors used	No. of capacitors used	Requirement of Matching condition	Electronic tunability availability
[41]	1	2	1	YES	NO
[36]	2	0	1	NO	NO
[37]	2	2	1	NO	NO
[38]	3	4	1	NO	NO
[39]	2	0	1	NO	YES
[40]	2	0	1	NO	YES
[42]	2	0	1	NO	YES
[43]	3	3	1	NO	NO
Proposed	1	1	1	NO	YES

2.5 Review of MM filters:

In analogue signal processing applications it may be desirable to have active filters with input currents and/or voltages and output currents and/or voltages, that is mixed-mode filters. [55] Careful inspection of the available literature shows that the mixed-mode realizations with input current and output voltage and with input voltage and output current are available but limited circuit realization is available for realizing a generalized mixed-mode active filter with input current or voltage and output current or voltage. In recent past, mixed-mode filter circuits have been extensively studied and researched in open literature with renewed interest and hence, several mixed-mode filter circuits using different current-mode active elements such as CCII[56], FDCII[57], CCCII[58], OTAs [59].However, these circuits employ too many active

and passive elements in filter realization. Besides it, few of the circuits don't offer the current tunability feature of filter characteristic parameters too. As far as the topic of this paper is concerned, the mixedmode filter circuits using single active element are of great interest, because circuits employing minimum active components are more beneficial in terms of power dissipation and manufacturing cost point of view and also satisfy the supply related specifications of portable battery operated electronic gadgets . In this work mixed-mode filter employing single CD-DITA as active element and two capacitors, two resistors has been designed and implemented using 180nm TSMC paramenters. Table2.4 for comparison of various MM filter configuration with the proposed MM filter can be given as:

Table2.4: Comparison of Various MM filter configurations with CD-DITA based Proposed MM filter

Ref.	[56]	[59]	[58]	[57]	Proposed
Active element	CCII	OTA	CCCII	FDCII	CD-DITA
No. of Active elements used	6	5	2	1	1
Passive elements	10	2	2	5	4
Electronic tenability	NO	YES	YES	NO	YES
Supply(V)	± 2.5	± 1.65	± 2.5	± 12.5	$\pm .9$
Pole Frequency (ω_n)	$.5MHz$	$1MHz$	$638.5KHz$	$3.789MHz$	$6.97MHz$
Universality of filter	YES	YES	NO	NO	NO

Chapter 3

Realization of CD-DITA

3.1 Introduction:

Current-differencing differential-input transconductance amplifier i.e. CD-DITA is one of the CM ABBs used for designing and implementing analogue circuits. In addition to the traditionally used op-amps, CD-DITA block not only supports VM but also supports CM and also the multi-mode or mixed mode operation. CD-DITA is growing as a flexible, versatile and universal ABB for analogue signal processing applications. Its profitable features and its usefulness have been renowned from [10] on active elements. The ideal and non-ideal analysis of CD-DITA can be summarized as following:-

3.1.1. Ideal CD-DITA:

CD-DITA block is a new active block, having six terminals with electronic control. The circuit symbol of CD-DITA and the behavioral model of CD-DITA [10] are presented in the Fig. 3.1(a) and (b), respectively. CD-DITA has two current input terminals and they are having low-impedance and ideally zero current input terminals i.e. p and n, and the remaining four terminals are high-impedance terminals. Out of these four terminals, two terminals are intermediate terminals that are specifically known as the current output terminal z and the input voltage terminal v and then the remaining two terminals are current output terminals i.e. $x+$ and $x-$.

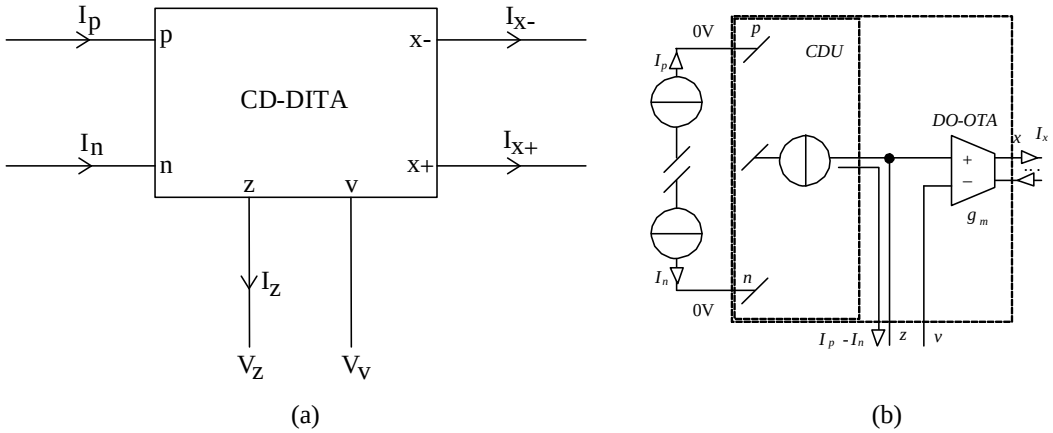


Fig. 3.1 CD-DITA (a) Schematic symbol and (b) Behavioral model[10]

The CD-DITA behavioral model includes two stages, which are basically controlled sources and these two stages are differential current-controlled current-source i.e. DCCCS with current gain unity, and differential voltage controlled current source i.e. DVCCS i.e. OTA with the transconductance gain. The input stage of CD-DITA can be realized by using a differential in-put single- out-put current differencing unit i.e. CDU , CDU basically produces the difference of the in-put currents I_p and I_n that are intended to further flow through the output terminal i.e. z terminal. There will be an appropriate voltage drop produced at the z terminal by the differential current i.e. I_z and the voltage drop that is produced will be according to any external load impedance is connected at the z terminal.

The output stage of the CDDITA block has been implemented by using a differential input and dual output OTA i.e. DO-OTA. The z output terminal of the CD-DITA block has also been internally connected to the non-inverting input terminal of the DO-OTA section. The terminal v has been brought out as the voltage input terminal of the CD-DITA block that is connected to the inverting input terminal of the DO-OTA section. The voltage difference at the input terminals of the DO-OTA section i.e. between the z and v terminals of the DO-OTA has been transformed though the DO-OTA's gain i.e. transconductance gain g_m into the output currents i.e. I_{x+} and I_{x-} intended to flow through the current output terminals of the CD-DITA block i.e. $x+$ and $x-$ terminals. These output currents flow are intended to flow in the opposite directions but these currents I_{x+} and I_{x-} will be equal in magnitude. The gain of DO-OTA can be electronically controlled using the bias currents. The relationship between the inputs and the outputs terminals of the CD-DITA block can be shown by using the following terminal equations:

$$V_p = V_n = 0 \tag{3.1}$$

$$I_v = 0 \tag{3.2}$$

$$I_z = I_p - I_n \tag{3.3}$$

$$I_{x+} = g_m\left(V_z - V_v\right) \tag{3.4}$$

$$I_{x-} = -g_m\left(V_z - V_v\right) \tag{3.5}$$

Therefore, Equation matrix of CD-DITA block has been given as

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_x \\ I_v \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & \pm g_m & 0 & \mp g_m \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_z \\ V_x \\ V_v \end{bmatrix} \tag{3.6}$$

3.1.2 Non ideal CD-DITA:-

In this section, the non-ideal CD-DITA block has been explained briefly. As presented in the Fig. 3.2 , non-ideal equivalent schematic symbol of the CD-DITA has been observed to be very similar to the CDTA block , except than the addition of the error in the transconductance transfer β_v which is due to the terminal v that has been always kept grounded in the case of CDTA block but in CD-DITA block it has been brought as the external extra voltage input terminal . The errors from the z and the v terminals are defined by the following equations:-

$$\beta_z = 1-\varepsilon_z ; \beta_v = 1-\varepsilon_v \text{ and } |\varepsilon_z| << 1; |\varepsilon_v| << 1 \tag{3.7}$$

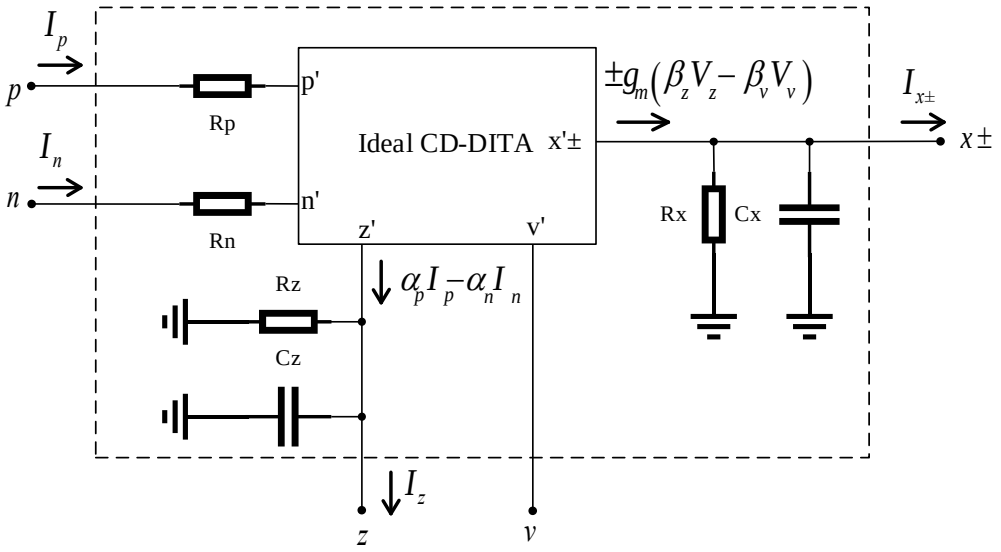


Fig. 3.2 Non ideal CD-DITA

Where ε_z is transconductance tracking error from the terminal z to the terminal $x\pm$

And ε_v is transconductance tracking error from the terminal v to the terminal $x\pm$

In the non-ideal case, the terminal equations of the CD-DITA are slightly modified and given as follows:-

$$V_p = 0 \tag{3.8}$$

$$V_n = 0 \tag{3.9}$$

$$I_z = \alpha_p I_p - \alpha_n I_n \tag{3.10}$$

$$I_{x+} = +g_m\left(\beta_z V_z - \beta_v V_v\right) \tag{3.11}$$

$$I_{x-} = -g_m\left(\beta_z V_z - \beta_v V_v\right) \tag{3.12}$$

Therefore, the Non-ideal CD-DITA block in the absence of various parasitics is presented by the following equations matrix:-

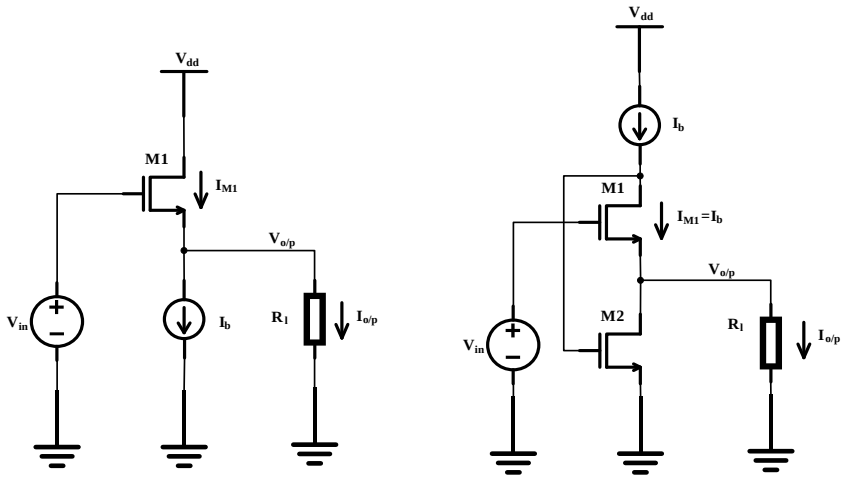
$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_x \\ I_v \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \alpha_p & -\alpha_n & 0 & 0 & 0 \\ 0 & 0 & \pm\beta_z g_m & 0 & \mp\beta_v g_m \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_z \\ V_x \\ V_v \end{bmatrix} \tag{3.13}$$

3.2 Realization of Flipped Voltage Follower(FVF) based CDDITA:-

3.2.1 Flipped voltage follower:-

In Fig. 3.3(a), a simple MOS based Common drain (CD) amplifier is shown; CD amplifier is commonly used circuit in most of the ASP applications due to the voltage buffering operation of this amplifier.

If we consider that the body effect of transistor M_1 is ignored, then with this assumption it has been observed that the output voltage signal of the CD amplifier circuit follows the input voltage signal with a dc level shift of V_{GS} of transistor M_1



(a) (b)

Fig. 3.3(a) CD amplifier or Source Follower, (b) Flipped Voltage Follower (FVF)

Thus the relation between the i/p and o/p voltages signals can be expressed as the following equation:-

$$V_{out} = V_{in} - V_{GS} \tag{3.14}$$

The DC analysis of the circuit in figure (a) shows some major drawbacks that are:

- The sinking capability of this circuit to load is large i.e. source follower can sink large amount of current to the load, but biasing current i.e. I_b is limiting the sourcing capability from output node.
- One more drawback of CD amplifier is the dependence of its o/p current I_{out} on the current through the transistor M_1 i.e. I_{M1}, such that if we vary transistor current then there is corresponding variation in its V_{GS} and, thus the voltage gain also changes resulting variable voltage gain i.e. not constant.
- Due to the DC shift, voltage gain of this circuit is also less than unity.
- If the loads are capacitive then also similar type of limitations exists in the circuit but at relatively higher frequencies.

The o/p impedance of source follower circuit is given as:

$$r_{out} = \frac{1}{g_m} \tag{3.15}$$

Where g_m is the transconductance of M_1. The typical value of r_{out} ranges from $1k\Omega$ to $5k\Omega$

In Fig. 3.4(b), the circuit shown is a negative-shunt-feedback amplifier which also acts as the source follower. Here in this circuit the usage of transistor M_1 is to buffer signals from i/p to o/p. This circuit offers some major advantages over the conventional source follower circuit and these are as follows:

- Here in this circuit, current through transistor M_1 i.e. I_{M1} is always constant with the help of bias current I_b, thus making I_{M1} independent of any variations in the o/p current I_{out}.
- Hence I_{M1} is always constant, thus V_{GS} of M_1 also remains constant.
- In this circuit the variations in output current i.e. I_{out} have been absorbed by the transistor M_1 which is nothing but a current sensing transistor. Thus as a result, the variations in the output voltage remains low even at the higher frequencies.
- This circuit provides the output node with very small value of the output impedance because of the M_2 transistor.
- FVF can source large amount of currents due to its low output impedance [44]

M_2 transistor provides the shunt feedback to the circuit. The bias current source I_b is connected to the drain terminal of transistor M_1 instead of the source terminal, due to which this particular circuit has been named as the flipped voltage follower i.e. (FVF).

The o/p impedance of Flip Voltage follower circuit is given as:-

$$r_{out} = \frac{1}{g_{m1} g_{m2} r_{o1}} \tag{3.16}$$

Where r_{o1} is the output resistance of transistor M_1 and g_{m1}, g_{m2} are transconductance of transistors M_1 and M_2 respectively. The typical value of r_{out} ranges from 10Ω to 100Ω.

3.2.2 Current Mirror based on FVF:

Considering FVF circuit, the output node of FVF follower circuit can be used as the current input node because at the output node of this circuit very low value of the impedance is shown

as is required in the current mirror. Therefore, this modified FVF, called as a current sensing cell, also named as FVF current sensor i.e. (FVFCS). In Fig. 3.5.One such circuit is shown:-

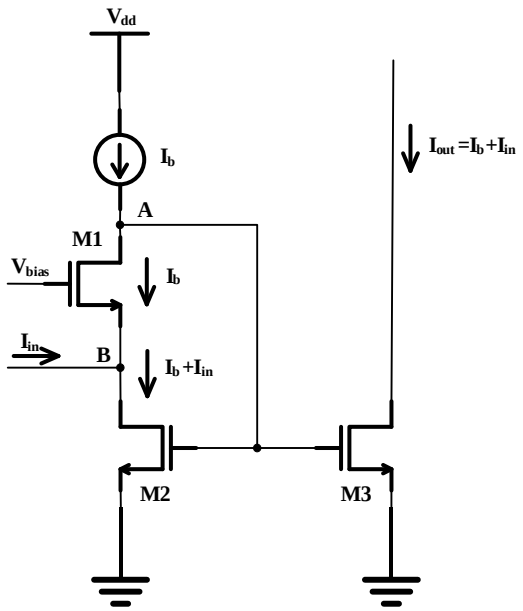


Fig. 3.4 Current Mirror based on FVF

In the above circuit, node B acts as i/p current sensing node because it's having low impedance and the negative shunt feedback is provided by transistor M_2. The variations in the input current signal at the node B will be transformed to the corresponding voltage variations at the node A. Transistor M_3 is used to form a current mirror i.e. M_3 produces the copy of the i/p current signal utilizing the variations at the node A. The i/p and the output current signals are related through the following expression:

$$I_{out} = I_{in} + I_b \tag{3.17}$$

The bias current I_b in the above expression can be easily eliminated by employing the current mirroring techniques.

The voltage levels required at the node A to keep both the transistors i.e. M_2 and M_3 are just V_{DSsat}, that is smaller than the voltage levels required for the traditional low-voltage current mirrors.

The impedance of this mirror at the input node A is very low i.e. ranging from 10Ω to 100Ω and the minimum level of voltage supply required at the node A is expressed as the following:-

$$V_{dd(\min)} = 2V_{DSsat} - V_t . \tag{3.18}$$

Thus FVF based current mirror has very low power supply requirements.

3.2.3 Current differencing unit:-

CDU can be realized using FVFCS [45] as shown in figure 3.5. In this CDU transistors from M_1-M_3 and M_4-M_6 are forming two consecutive FVF based current-mirrors and also transistor pairs M_7 and M_8 are used to realize the simple current-mirror. To bias the both FVF based current mirrors same bias current i.e. I_{b1} is used, due to which the currents through M_1 and M_6 transistors will be equal to the biasing current i.e. I_{b1}.

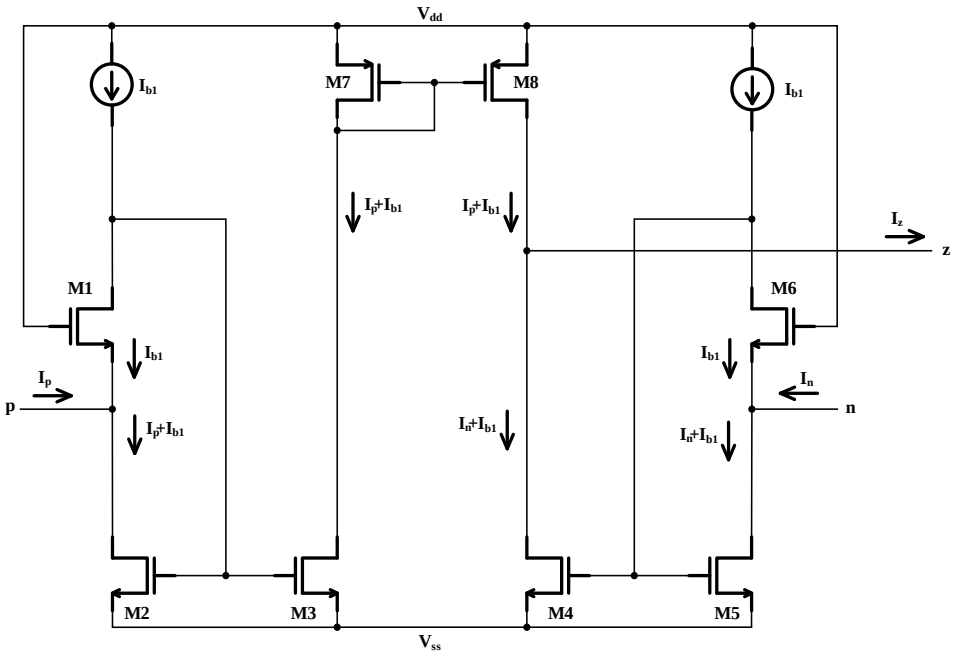


Fig. 3.5 CDU based on FVF

The input currents i.e. I_p and I_n have been applied at the current input terminals i.e. p and n of the CDU respectively. Thus the resulting currents flowing through the transistors M_2 and M_5 can be expressed by the following expressions:-

$$I_{M2} = I_p + I_{b1} \tag{3.19}$$

$$I_{M5} = I_n + I_{b1} \tag{3.20}$$

The currents flowing through the transistors M_2 and M_5 will be exactly mirrored into the transistors M_3 and M_4 because of the current mirror respectively. The current flowing through the transistor M_3 will be further mirrored into the transistor M_8 due to the usage of a simple current mirroring circuit. Thus, the resulting currents flowing through the transistors M_8 and M_4 can be expressed as the following expressions:-

$$I_{M8} = I_p + I_{b1} \tag{3.21}$$

$$I_{M4} = I_n + I_{b1} \tag{3.22}$$

In CDU unit, the z terminal has been considered as the current output and the difference of the currents flowing through the transistors M_8 and M_4 will be either sourced by the z terminal or sunk by the z terminal and hence this expressions of current flowing through the z terminal can be expressed as following:-

$$I_z = I_p - I_n \tag{3.23}$$

From the above expression it becomes clear that the current differencing operation has been realized by the z terminal of CDU unit. In CD-DITA, if some external impedance is connected at the z terminal of CDU, then the corresponding current though the z terminal i.e. I_z will be converted into the corresponding voltage drop V_z at the z terminal. The z terminal acts as one of the voltage input nodes for DO-OTA and hence the voltage drop i.e. at the z terminal i.e. V_z can be used as one of the inputs of the DO-OTA section of the CD-DITA.

3.2.4 Dual output OTA (DO-OTA):-

As presented in the Figure. 3.6, the DO-OTA section of the CD-DITA block has been realized by using a differential pair amplifier formed using a transistor pair consisting transistors M_9 and M_{10}. Transistors M_9 and M_{10} have been biased using the biasing current i.e. I_{b2} and for the purpose of obtaining the dual output current i.e. $I_x \pm$, few simple current mirror circuits based on the NMOS and PMOS have been used.

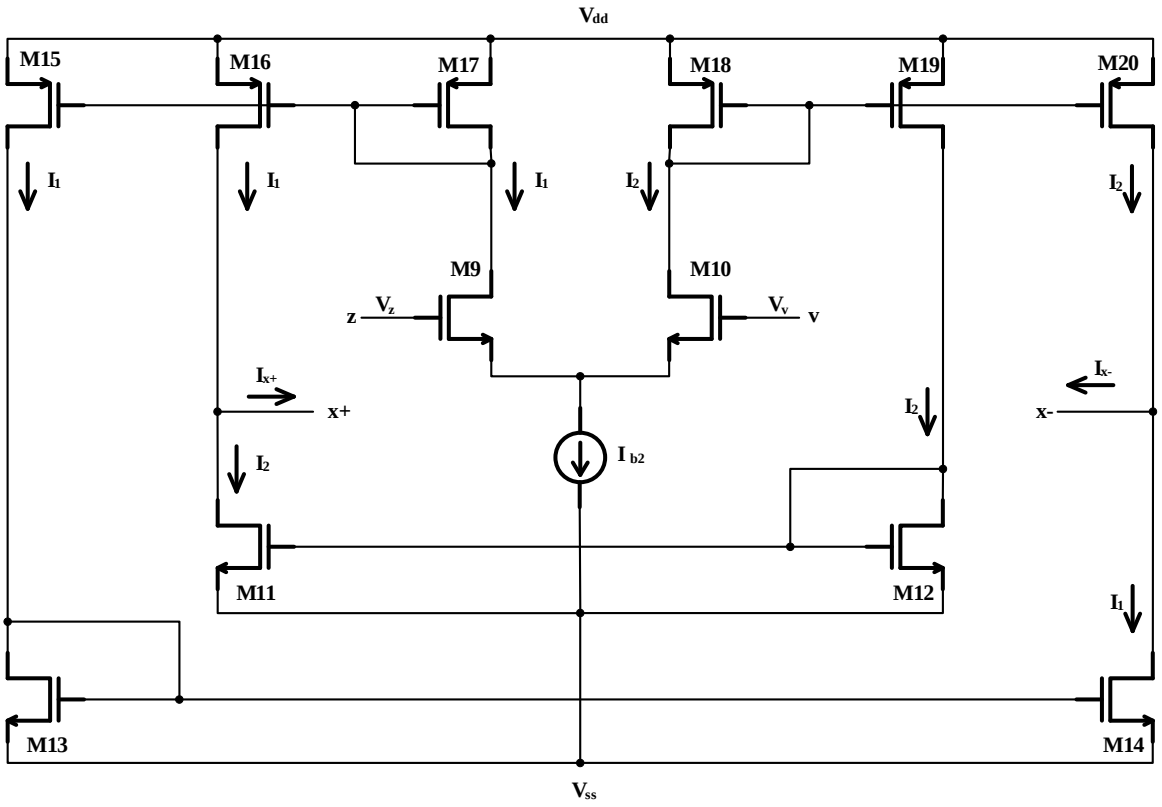


Fig. 3.6 DO-OTA [46]

The input voltage signals i.e. V_z and V_v have been applied at input voltage terminals i.e. the z terminal and the v terminal respectively. The input voltages at these input terminals i.e. at z terminal and v terminal will produce the corresponding currents i.e. I_1 and I_2 flowing through the transistor M_9 and the transistor M_{10} respectively. Here when the current I_1 i.e. flowing through the transistor M_9 has been mirrored using the transistor pair M_{16} and M_{17} and also when the current I_2 i.e. flowing through the transistor M_{10} has been mirrored using the transistor pairs i.e. M_{11}, M_{12}, M_{18} and M_{19}. Thus by mirroring the currents I_1 and I_2 according to the above configurations, then output of the DO-OTA achieved at an output terminal $x+$ will be a positive difference of the currents I_1 and I_2 .Thus the current flowing through the $x+$ terminal of the DO-OTA can be expressed as following:-

$$I_{x+} = I_1 - I_2 \tag{3.23}$$

Here when the current I_1 i.e. flowing through the transistor M_9 has been mirrored using the transistor pairs M_{13}, M_{14}, M_{15} and M_{17} ,and also when the current I_2 i.e. flowing through the

transistor M_{10} has been mirrored using the transistor pairs i.e. M_{18} and M_{20} Thus by mirroring the currents I_1 and I_2 according to the above configurations , then the output of the DO-OTA achieved at an output terminal $x-$ will be a negative difference of the currents I_1 and I_2. Thus the current flowing through the $x+$ terminal of the DO-OTA can be expressed as following:-

$$I_{x-} = -(I_1 - I_2) \tag{3.24}$$

Thus when the differential input voltage i.e. $(V_z - V_v)$ has been applied at the input of the DO-OTA then the dual output current signals i.e. $I_x \pm$ can be achieved. The expressions for the output currents of the DO-OTA section can be given as the following:-

$$I_{x\pm} = \pm(I_1 - I_2) = \pm g_m(V_z - V_v) \tag{3.25}$$

Where g_m is the transconductance gain of the DO-OTA section and this transconductance gain of the DO-OTA can be controlled by the biasing current i.e. I_{b2} . The transconductance gain of the DO-OTA i.e. g_m can be given as the following expression:-

$$g_m = \sqrt{I_{b2}\left[\mu_n C_{ox}\left(\frac{W}{L}\right)\right]_{M_9, M_{10}}} \tag{3.26}$$

Where the parameters $\frac{W}{L}, \mu_n$ and C_{ox} are of the differential pair transistors i.e. of the transistors M_9 or M_{10}. And g_m i.e. the transconductance gain of the DO-OTA can be varied by varying the bias current I_{b2}.

To realize the CD-DITA block, DO-OTA section has been clubbed with the CDU section and in the CD-DITA block the one of the voltage input terminal i.e. *z* terminal of DO-OTA section has been driven by the current output terminal i.e. *z* terminal of CDU section and the second input voltage terminals i.e. *v* terminal of the DO-OTA section is connected to some external input voltage signal. Depending upon the application requirement the connections to this *v* terminal of the DO-OTA can be made.

The complete schematic diagram of the CD-DITA block based on the FVF is presented in the Fig. 3.7:-

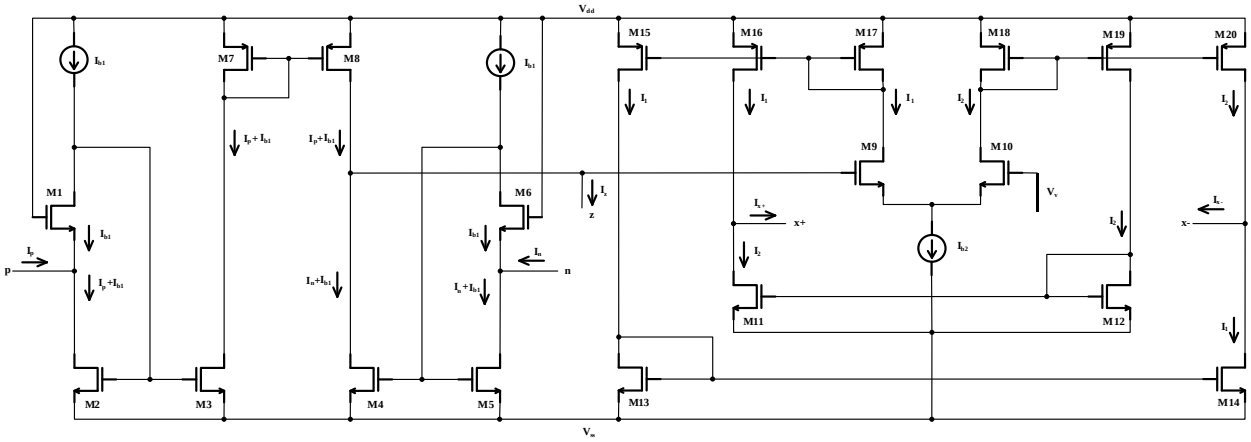


Fig. 3.7 CD-DITA based on FVF

In the above figure 3.7CD-DITA based on FVF consists of the CDU section followed by the DO-OTA section. And the aspect ratios of the transistors used to implement the realization of the CD-DITA block has been listed in the table 3.1 given below:-

Table 3.1 Aspect ratios of the transistors for CD-DITA based on FVF :

Transistors	**W in** (μm)	**L in** (μm)
$M_1 - M_8$	24	1
M_9, M_{10}	8	1
$M_{11} - M_{14}$	5	1
$M_{15} - M_{20}$	8	1

3.3 Characterization of CD-DITA:-

The CMOS implementation of the CD-DITA block based on FVF has been presented in the Fig 3.7. The CMOS implementation of the CD-DITA block has been simulated using the PSPICE simulations and also using the 0.25um technology mode i.e. 0.25um process parameter. And the power supply rails that are used are $\pm 1.2V$. This CD-DITA block characterization for both the large signal behavior i.e. the DC response of the CD-DITA block and for the small signal

behavior i.e. the Frequency response the CD-DITA block is given in the coming sections of this work:

3.3.1 DC characteristics or Large signal analysis:-

3.3.1.1 DC characteristics of CDU Section:-

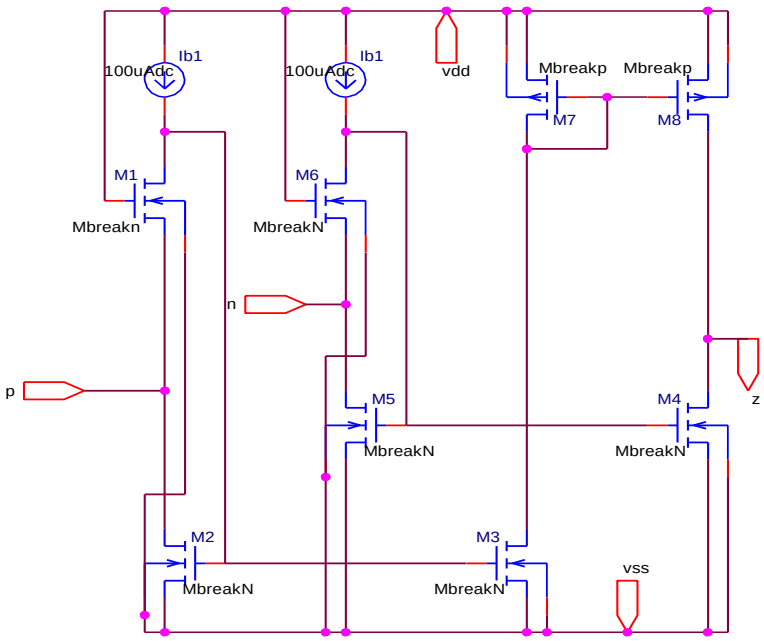


Fig. 3.8 PSPICE schematic diagram of the CDU

The PSPICE schematic diagram of the CDU Section of the CD-DITA block has been presented in the Fig. 3.8. the current that is used to bias the CDU section i.e. I_{b1} has been chosen as $100\mu A$. To verify the linear range of the ouput current when input currents are varied i.e. the dynamic range of the input currents at the current input terminal p and also along with the verification of the current tracking from p terminal to the z terminal.

The DC analysis of the output current of the CDU vs. one of the input current signal provided the other input signal is zero i.e. I_z vs. I_p with the condition of $I_n = 0$ has been plotted and To obtain this plot the current at p terminal i.e. I_p been varied from $-150\mu A$ to $150\mu A$ and presented in the Fig. 3.9

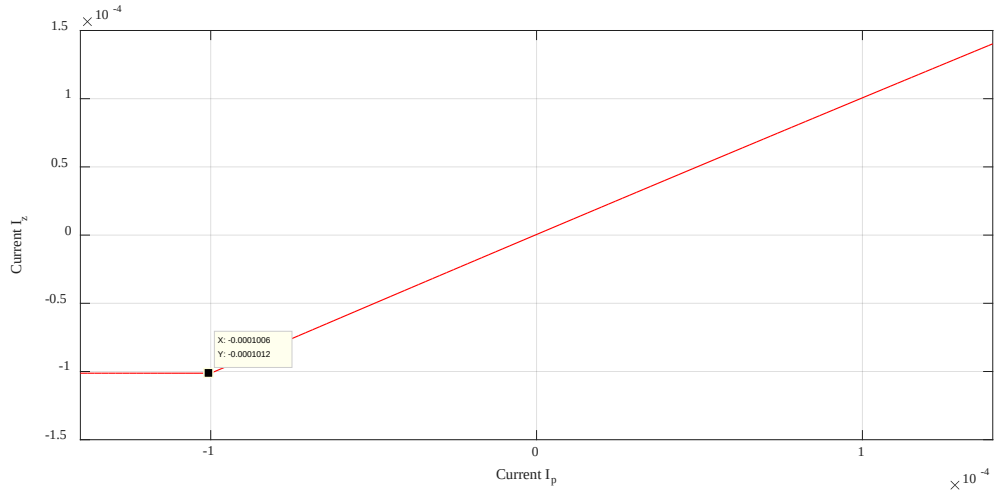


Fig. 3.9 . Current transfer from the p-terminal to the z-terminal (I_z vs. I_p) with the condition

$$I_n = 0$$

The DC analysis curves that are presented in the Fig. 3.10 show the effect of the variation of the current at the n terminal current i.e. I_n on the plot of I_z vs. I_p. To obtain this plot the current at p terminal i.e. I_p been varied from $-150\mu A$ to $150\mu A$ along with the parametric sweep of I_n that is ranging from the value of $-60\mu A$ to $60\mu A$ using interval value of $30\mu A$.

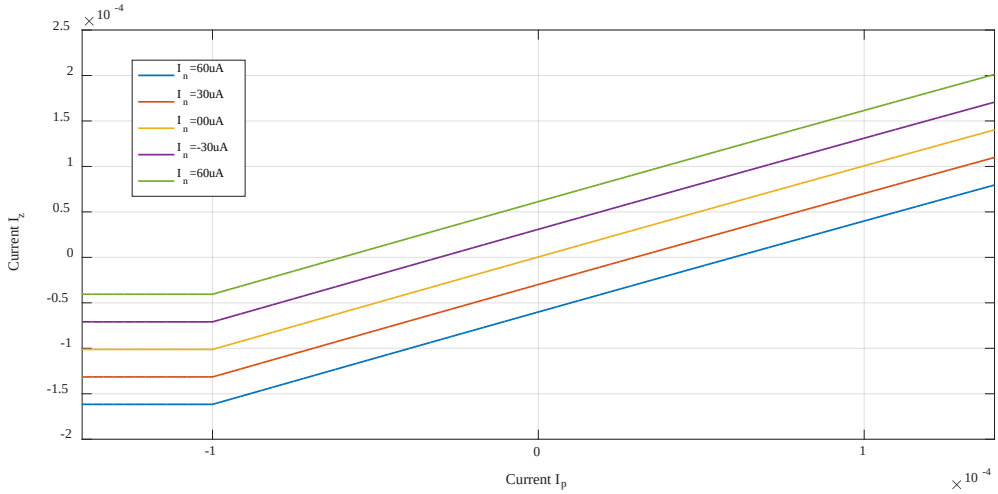


Fig. 3.10 Current transfer from the p-terminal to the z-terminal (I_z vs. I_p) with parametric sweep on I_n

To verify the linear range of the ouput current when input currents are varied i.e. the dynamic range of the input currents at the current input terminal n and also along with the verification of the current tracking from n terminal to the z terminal.

The DC analysis of the output current of the CDU vs one of the input current signal provided the other input signal is zero i.e. I_z vs I_n with the condition of $I_p = 0$ has been plotted and To obtain this plot the current at n terminal i.e. I_n been varied from $-150\mu A$ to $150\mu A$ and presented in the Fig. 3.11.

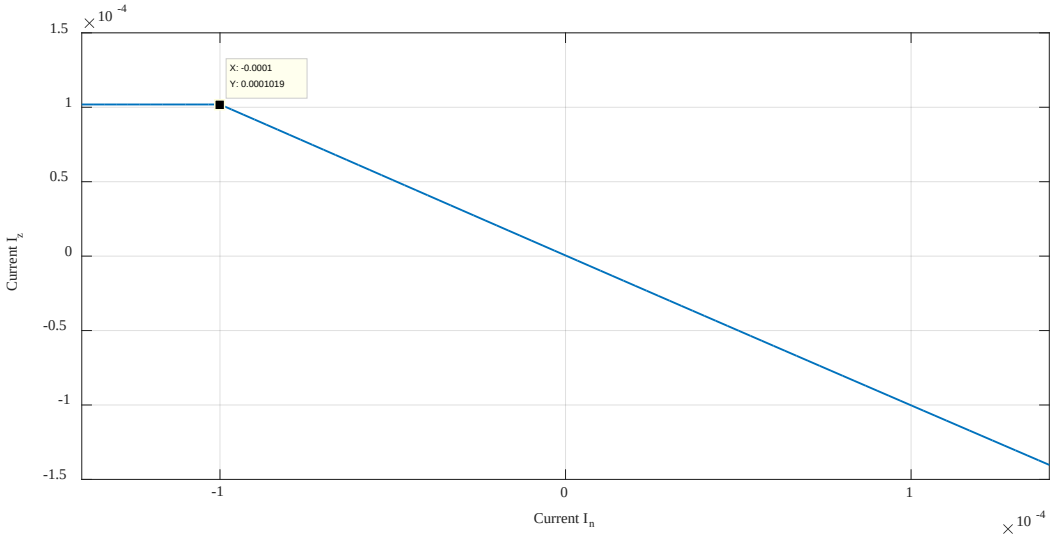


Fig. 3.11. Current transfer from the n-terminal to the z-terminal (I_z vs I_n) with the condition $I_p = 0$.

The DC analysis curves that are presented in the Fig. 3.12, show the effect of the variation of the current at the p terminal current i.e. I_p on the plot of I_z vs I_n To obtain this plot the current at n terminal i.e. I_n been varied from $-150\mu A$ to $150\mu A$ along with the parametric sweep of I_p that is ranging from the value of $-60\mu A$ to $60\mu A$ using interval value of $30\mu A$.

From the DC analysis of the of CDU conducted using the PSPICE simulations, it has been concluded that the input vs output characteristics of the CDU section will remain in linear range for the input dynamic range of $-100\mu A$ to $100\mu A$ this can also be theoretically verified by the bias current I_{b1} that tends to limit the dynamic range of CDU section.

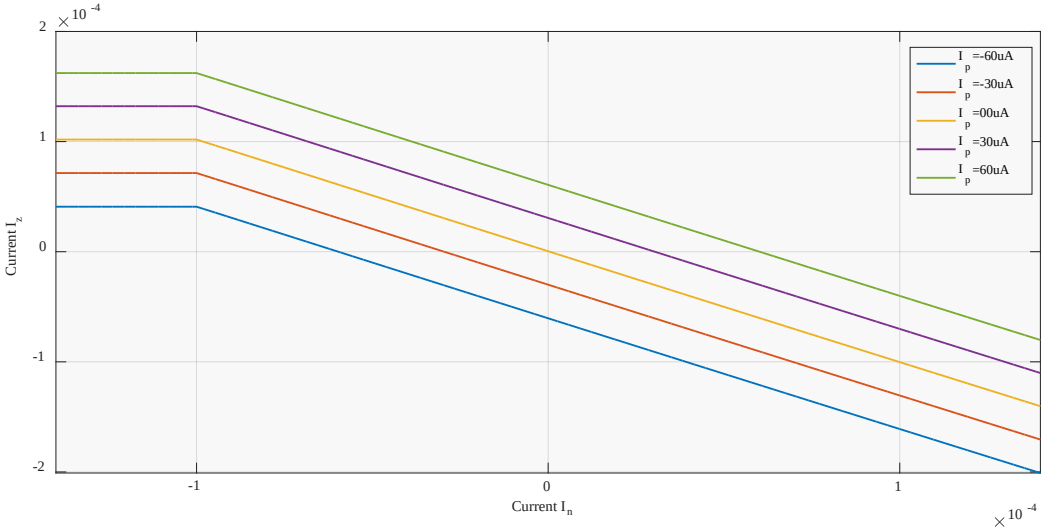


Fig. 3.12 Current transfer from the n-terminal to the z-terminal (I_z vs I_n)with parametric sweep on I_p

3.3.1.2 DC characteristics of DO-OTA Section:-

The PSPICE schematic diagram of the DO-OTA Section of the CD-DITA block has been presented in the Fig. 3.13.

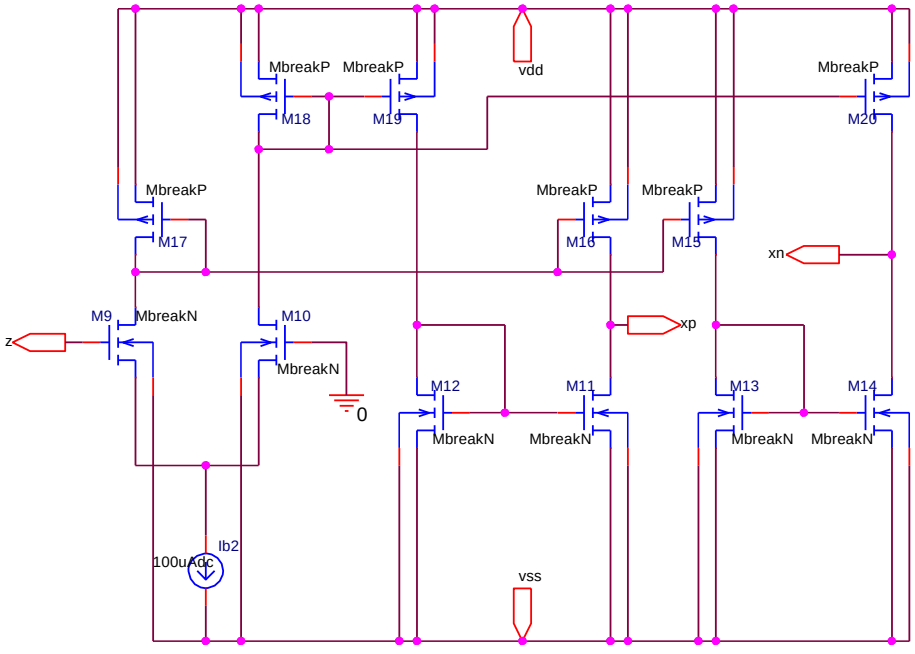


Fig. 3.13 PSPICE schematic diagram of the DO-OTA

The current that has been used to bias the DO-OTA section i.e. I_{b2} has been chosen as $100\mu A$ To verify the linear range of the output current when input voltages are varied i.e. the voltage dynamic range of the input voltage at the voltage input terminal z and also along with the verification of the of transconductance transfer from the input terminal i.e. the z terminal to the output current terminals i.e. the $x\pm$ terminals , DC analysis is achieved by varying the input voltage at the input z terminal i.e. V_z from $-1.2V$ to $1.2V$ and the resulting plot i.e. of output current vs. input voltage by keeping the other voltage terminal grounded i.e. $I_{x\pm}$ vs. V_z with the condition of $V_v = 0V$ has been presented in the Fig. 3.14.

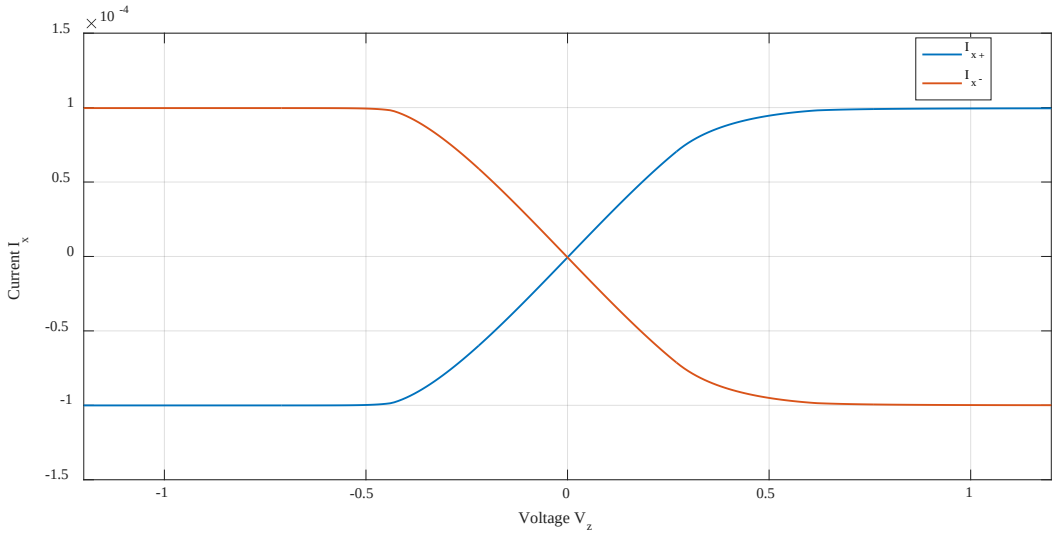


Fig. 3.14 Transconductance transfer from the z -terminal to the $x\pm$ terminal ($I_{x\pm}$ vs V_z) with $I_{b2} = 100\mu A$

The effect of the variation of the bias current I_{b2} on the output current vs input voltage curves i.e. $I_{x\pm}$ vs V_z plot has been presented in Fig. 3.15. To achieve these DC curves, the input voltage of the DO-OTA section i.e. V_z has been varied from the $-1.2V$ to $1.2V$ along with the parametric sweep applied on biasing current i.e. on I_{b2} with the values $25\mu A$, $50\mu A$, $75\mu A$ and $100\mu A$.

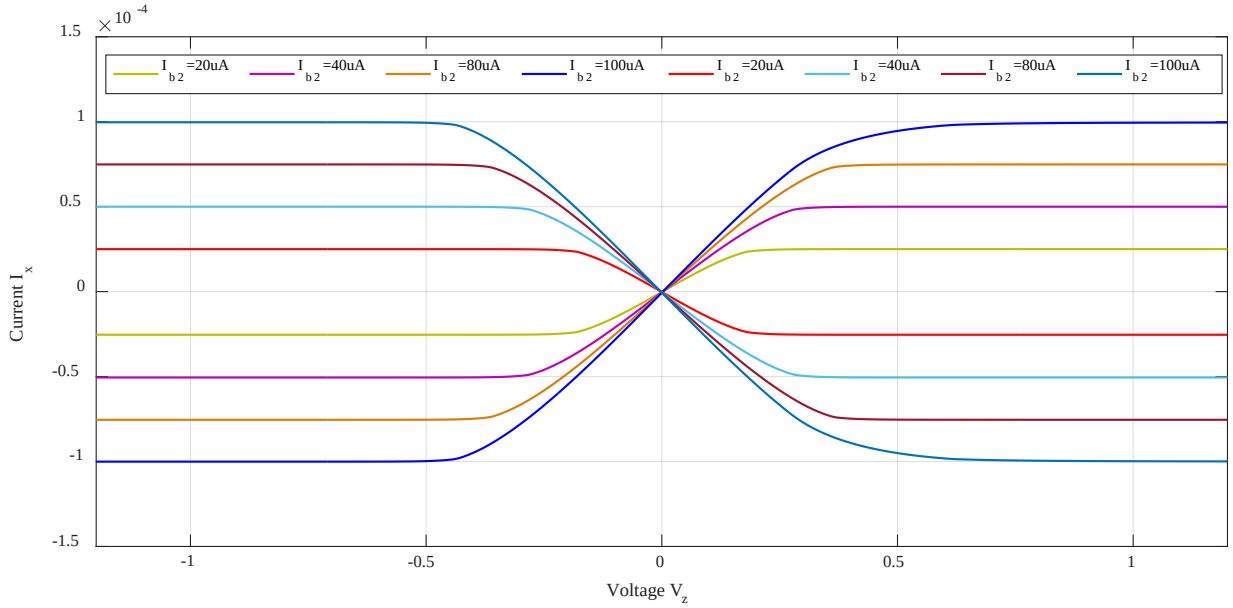


Fig. 3.15.Transconductance transfer from the z -terminal to the $x\pm$ terminals ($I_{x\pm}$ vs V_z) with I_{b2} as parametric sweep

From the DC analysis of the of DO-OTA conducted using the PSPICE simulations, it has been concluded that the input vs output characteristics of the DO-OTA section will remain in linear range for the input dynamic range of $-300mV$ to $300mV$. This input dynamic range of the DO-OTA section has been further limited by the bias current i.e. I_{b2} .

3.3.1.3 DC characteristics of CD-DITA Block:-

To form the CD-DITA block both the CDU section and the DO-OTA section has been cascaded. The PSPICE schematic of CD-DITA has been presented in the Fig. 3.16 and the Bias current used to bias the both the CDU section and the DO-OTA section i.e. I_{b1} and I_{b2} has been chosen as $100\mu A$.

For verifying unity current gain i.e. $A_I = 1$ while transferring input current from the input current terminal i.e. p terminal to the output current terminal i.e. $x\pm$ terminal, DC analysis curves between the output current and the input current i.e. I_{x+} vs I_p has been performed by varying the externally connected resistance R_z at the z -terminal has been plotted.

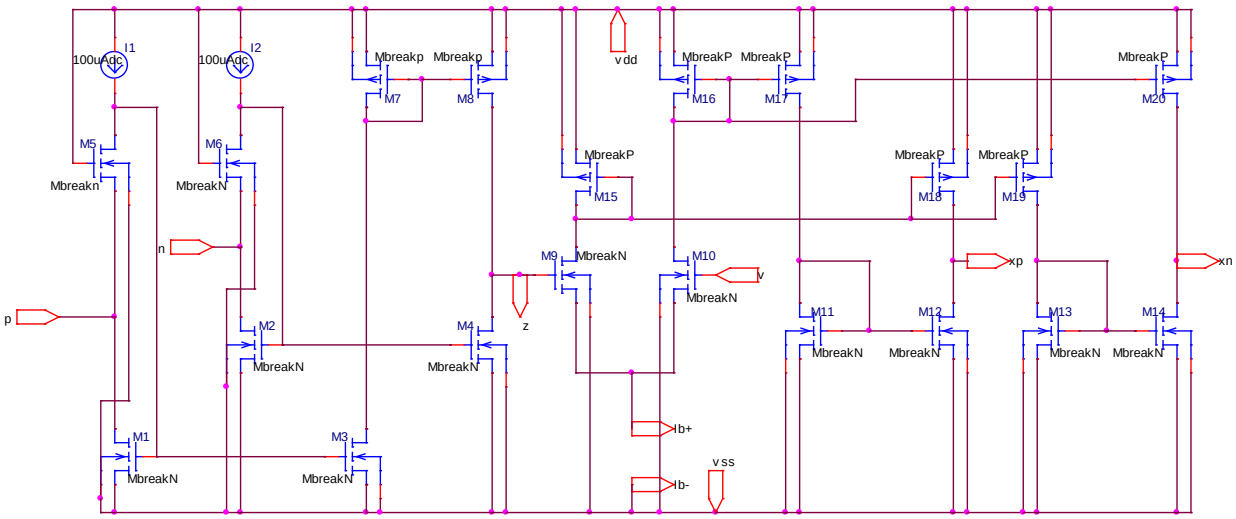


Fig. 3.16 PSPICE schematic of CD-DITA block

The DC analysis curves presented in the Fig. 3.17 shows the variation of externally connected resistance R_z at the z terminal on the output vs input i.e. I_{x+} vs I_p graph. The conditions that are used to achieve these plotted results are first the current at the input p terminal i.e. I_p has been varied from the $-60\mu A$ to $60\mu A$ along with applying the parametric sweep on R_z keeping the values of R_z as $1k\Omega, 3k\Omega, 5k\Omega \& 7k\Omega$ secondly the current at the input n terminal i.e. I_n has been kept zero i.e. $I_n = 0uA$.

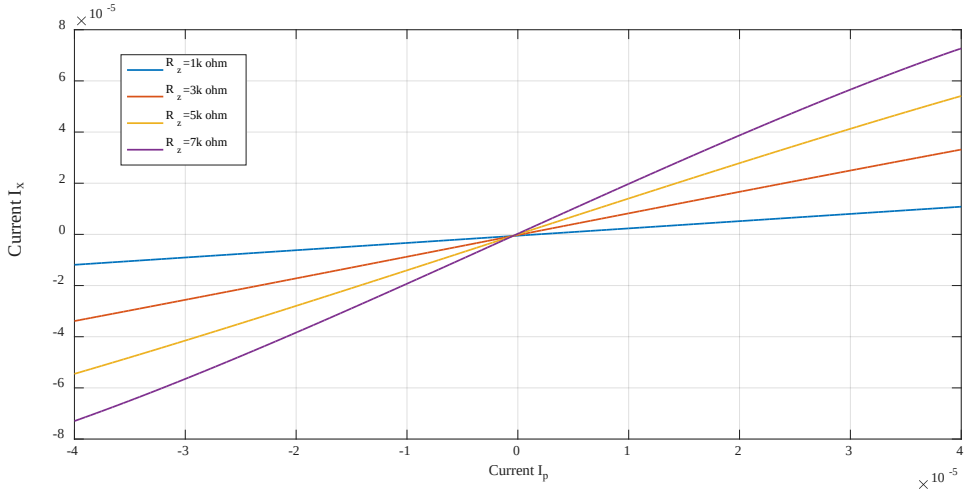


Fig. 3.17 Current transfer from the p terminal to the $x+$ terminal (I_{x+} vs I_p) with parametric sweep on $R_z \& I_n = 0$

From these DC plotted results, the value of the external resistance connected at the z-terminal i.e. R_z for achieving unity current gain i.e. $A_I = 1$ of the CD-DITA block, has come out to be the value of $3.55k\Omega$ that has been conformed from the I_{x+} vs I_p curve.

DC plotted results the value of the external resistance connected at the z-terminal i.e. R_z for achieveing unity current gain i.e. $A_I = 1$ of the CD-DITA block, has come out to be the value of $3.55k\Omega$ these has been conformed from the I_{x+} vs I_p curve that has been plotted by using the value of $R_z = 3.55k\Omega$ and has been presented in the Fig. 3.18.

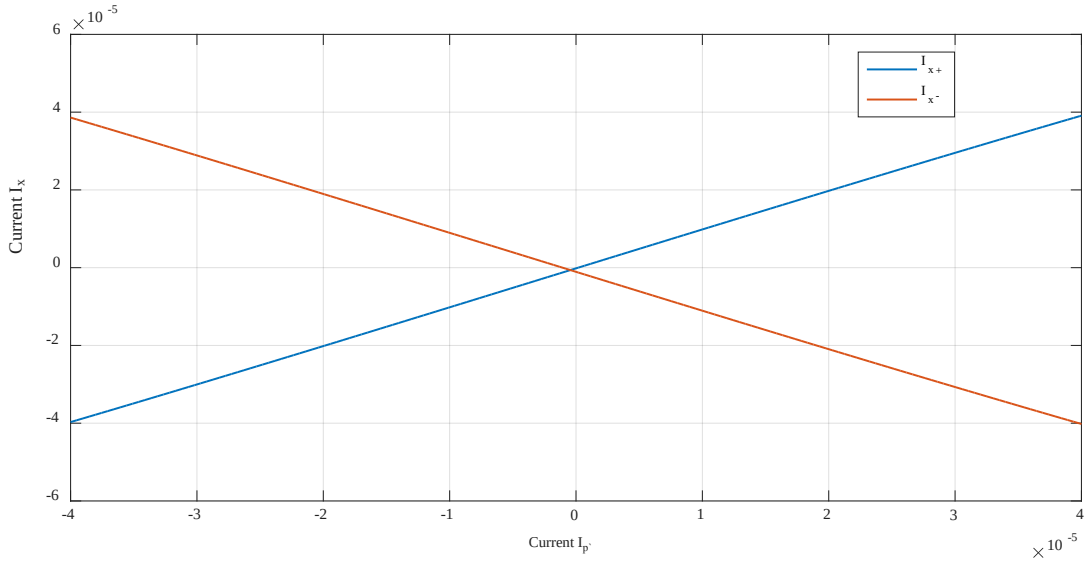


Fig. 3.18 Current transfers from p terminal to $x\pm$ terminal ($I_{x\pm}$ vs I_p) with $I_n = 0$ and $R_z = 3.55k\Omega$

DC analysis curves between the output current and the input current i.e. I_{x+} vs I_p has been performed by varying the bias current I_{b2} as been plotted. The DC analysis curves presented in the Fig. 3.19 presents the effect of the variation of the bias current I_{b2} on the output current vs the input current graphs i.e. I_{x+} vs I_p graph with the condition of keeping $I_n = 0$ and the externally connected resistance at the z-terminal i.e. $R_z = 3.55k\Omega$.

To achieve these graphs, I_p has been varied from $-60\mu A$ to $60\mu A$ with a parametric sweep of the biasing current i.e. of I_{b2} with the values of $40\mu A, 80\mu A, 120\mu A$, $160\mu A$ and $200\mu A$.

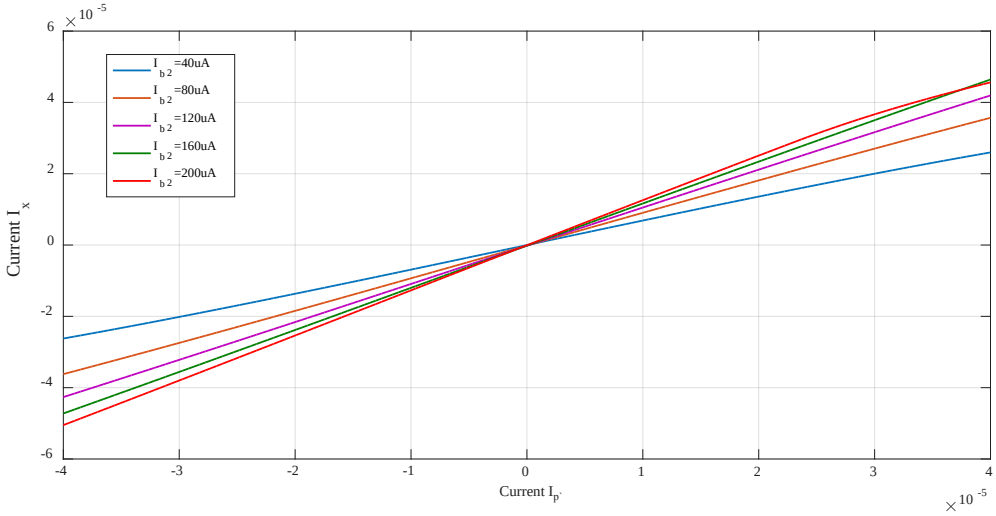


Fig. 3.19Current transfer from the p terminal to the $x+$ terminal ($I_{x\pm}$ vs I_p) keeping $I_n = 0$, $R_z = 3.55k\Omega$ and parametric sweep on I_{b2}

3.3.2 Small signal analysis (AC characteristics):-

For doing small signal analysis or for achieving AC characterization of any active block, the inputs that have to be applied should be AC signals and that must be simulated by plotting the frequency responses of the outputs of these active blocks. The Bias current I_{b1} and I_{b2} that are used to bias the CDU section and the DO-OTA section respectively; both are chosen as the value of $100\mu A$. The achieved frequency response plot of I_z/I_p has been presented in the Fig. 3.20

From the Fig. 3.20 frequency response plot of I_z/I_p the parasitic gain i.e. α_p and the current tracking error i.e. ε_p from the input terminal p to the output terminal z can be measured and along with these the bandwidth of the block CD-DITA can be measured. The practically values of these parameters as α_p , ε_p , and the bandwidth achieved from the frequency response plot of I_z/I_p has been given as following :-

$$\alpha_p = \frac{I_z}{I_p} = 110.638mdB = 1.021 \tag{3.27}$$

$$\therefore \varepsilon_p = 1 - \alpha_p = -0.021 \tag{3.28}$$

$$B.W = 202..445MHz \tag{3.29}$$

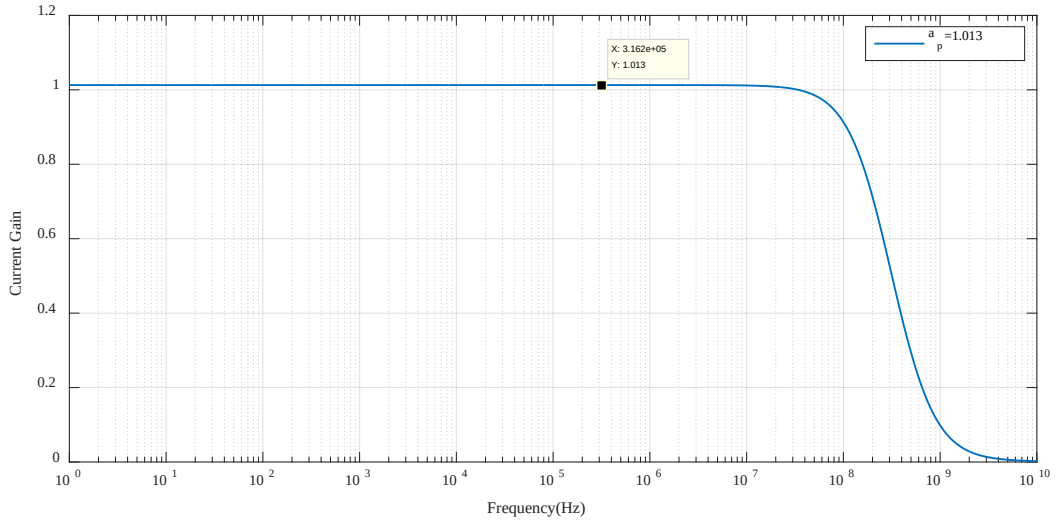


Fig. 3.20 Parasitic Current gain from the terminal p to the terminal z (I_z/I_p vs frequency) with condition $I_n = 0$

Similarly the achieved frequency response plot of I_z/I_n has been presented in the Fig. 3.21

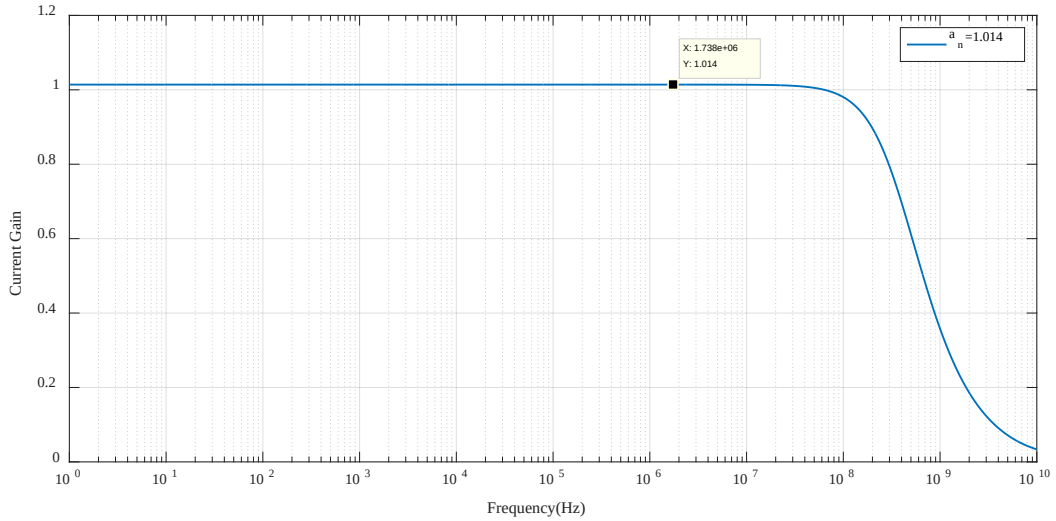


Fig 3.21. Parasitic Current gain from terminal n to terminal z (I_z/I_n vs frequency) with condition $I_n = 0$

From the Fig. 3.21 frequency response plot of I_z/I_n the parasitic gain i.e. α_n and the current tracking error i.e. ε_n from the input terminal n to the output terminal z can be measured and along with these the bandwidth of the block CD-DITA can be measured. The practical values of these parameters as α_n , ε_n , and the bandwidth achieved from the frequency response plot of I_z/I_n has been given as following :-

$$\alpha_n = \frac{I_z}{I_n} = 120.722mdB = 1.023 \tag{3.30}$$

$$\therefore \varepsilon_n = 1 - \alpha_n = -0.023 \tag{3.31}$$

$$\text{B.W.} = 372.759MHz \tag{3.32}$$

The frequency response of the transconductance gain i.e. g_m of the CD-DITA block from terminal z to the output terminals $x\pm$ has been presented in the Fig3.22. The transconductance gain i.e. g_m and the bandwidth for this has been measured by keeping $I_{b2} = 100\mu A$

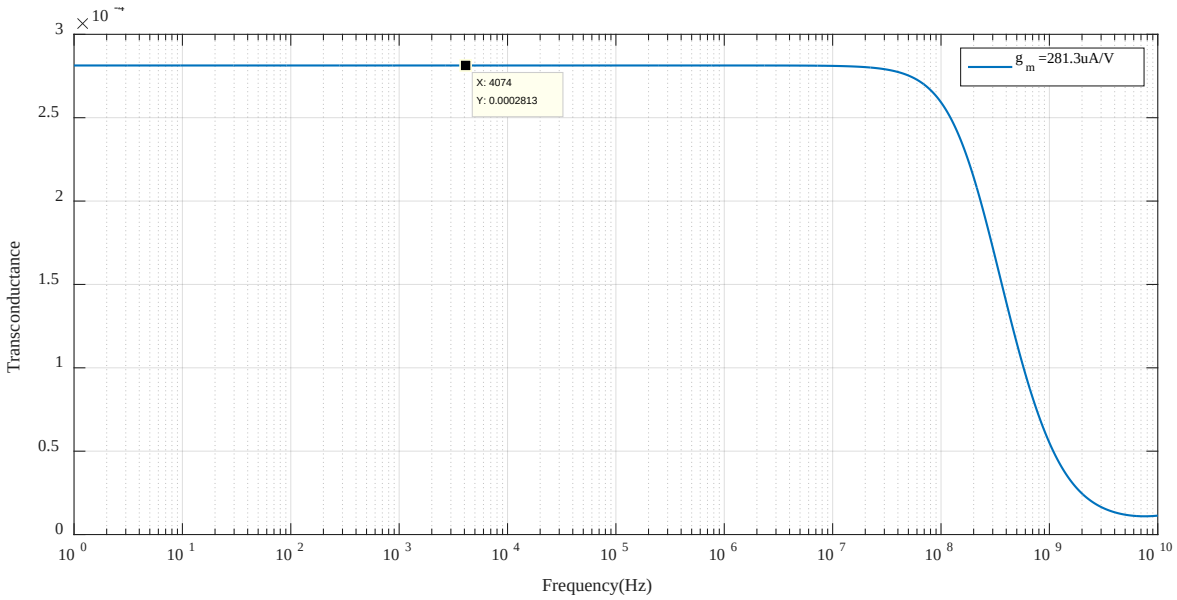


Fig. 3.22 Transconductance g_m (I_{x+}/V_z vs frequency) with the condition $I_{b2} = 100\mu A$

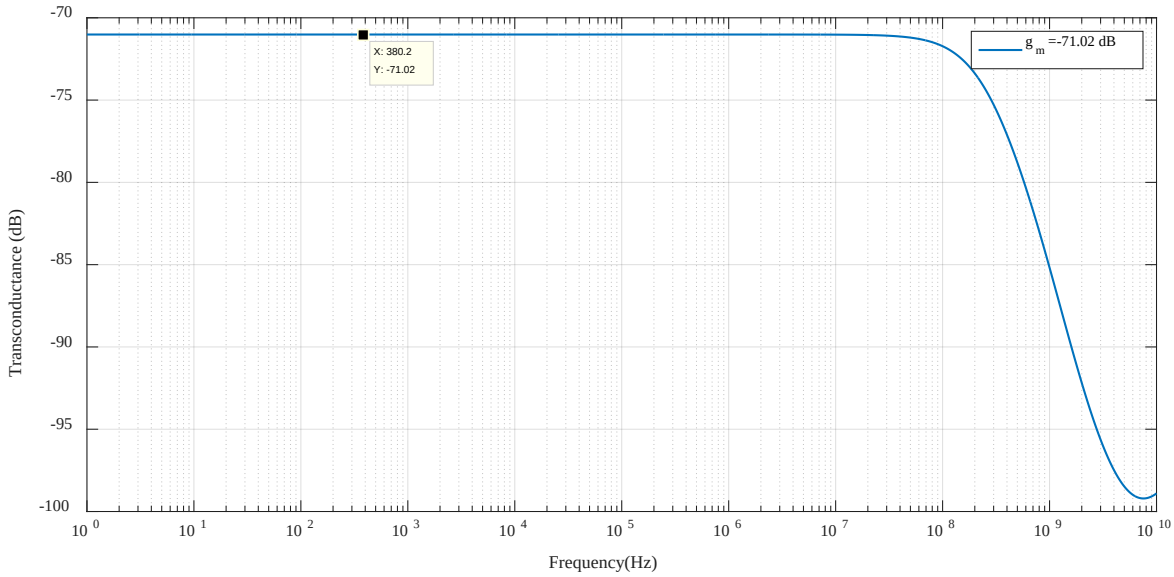


Fig. 3.23 Transconductance gain g_m in dB (I_{x+}/V_z vs frequency) with the condition

$$I_{b2} = 100\mu A$$

Practically the measured values of g_m and the bandwidth from the Fig. 3.22 and the Fig. 3.23 can be given as:-

$$g_m = -71.02dB = 281.3\,\mu A/V \quad (3.33)$$

$$\text{B.W.} = 244.585MHz \quad (3.34)$$

The simulated frequency response of the transconductance gain i.e. g_m of the CD-DITA block for various values of the biasing current i.e I_{b2} has been presented in the Fig. 3.25. I_{b2} has been varied with the values $50\mu A$, $100\mu A$, $150\mu A$ and $200\mu A$, and g_m graphs so obtained have been shown in the Fig 3.24.

From the Fig 3.25 various values of the transconductance gain i.e. g_m of the CD-DITA block has been measured for different values of the biasing current i.e. I_{b2}. The measured values of the transconductance gain i.e. g_m for the value of I_{b2} $50\mu A$, $100\mu A$, $150\mu A$ and $200\mu A$ are $213.190\,\mu A/V$, $281.752\,\mu A/V$, $325.993\,\mu A/V$ and $356.307\,\mu A/V$ respectively.

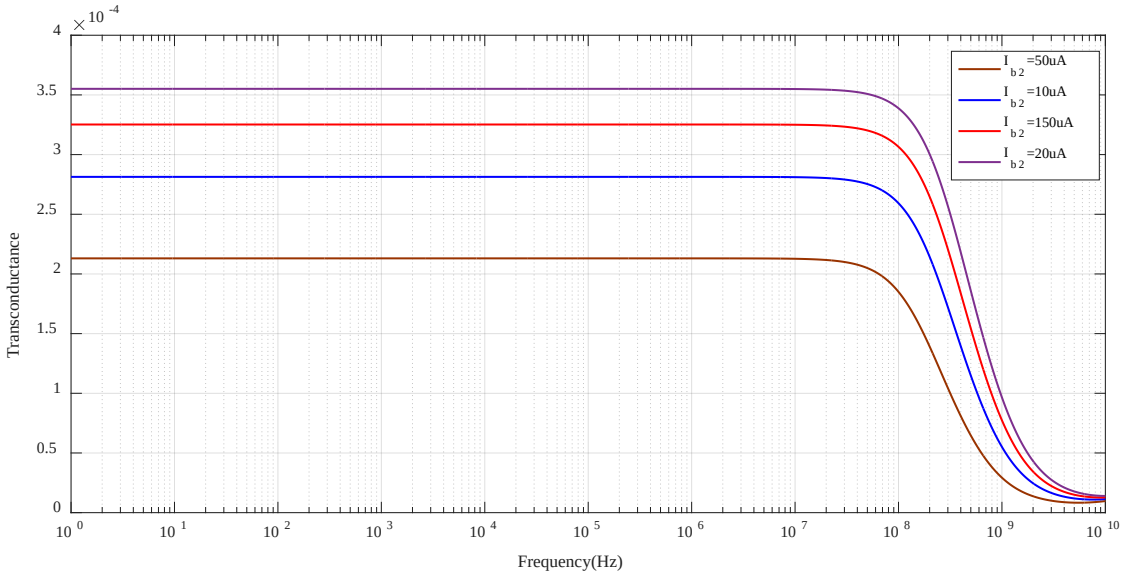


Fig. 3.24.Transconductance gain g_m (I_{x+} / V_z vs frequency) keeping I_{b2} as parametric sweep

The simulated frequency response of the overall gain of the CD-DITA block from the terminal p to the current output terminal $x+$ shown in Fig. 3.25 and the conditions for achieving the overall gain of the CD-DITA block i.e. $g_m R_z$ of 5 or $14dB$ are $I_{b2} = 100\mu A$, $g_m = 281.3\,\mu A/V$ and $R_z = 17.74k\Omega$ by:

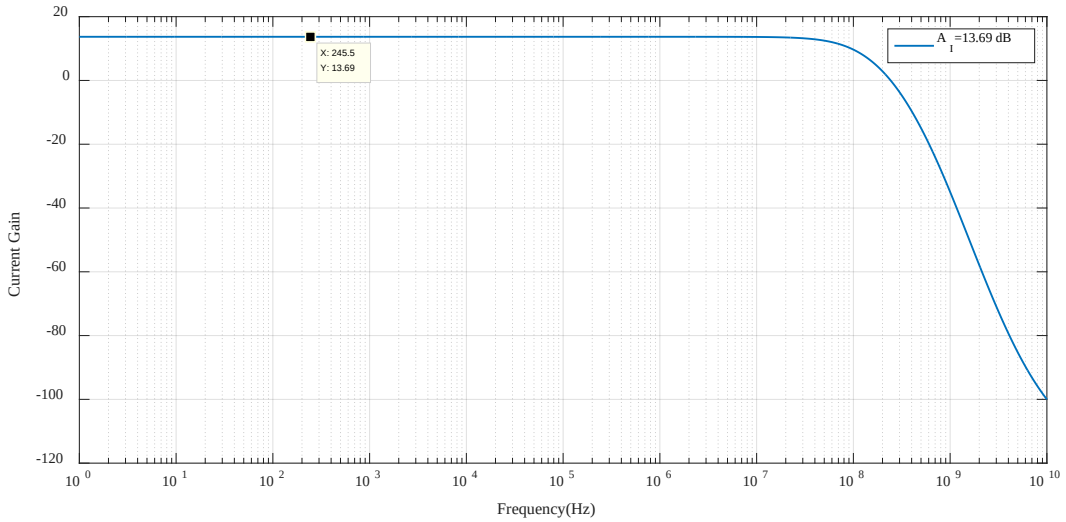


Fig. 3.25. Overall Gain of CD-DITA (I_{x+}/I_p vs frequency) with $I_n = 0$, $I_{b2} = 100\mu A$ and $R_z = 17.74k\Omega$

Thus, from Fig. 3.26 CD-DITA's measured gain and bandwidth can be given as:

$$\text{Gain} = 13.702dB \quad (3.35)$$

$$\text{B.W.} = 83.108MHz \quad (3.36)$$

Similarly The simulated frequency response of the overall gain of the CD-DITA block from the terminal n to the current output terminal $x+$ has been plotted by using the same above mentioned conditions, has been presented in the Fig. 3.26 as:-

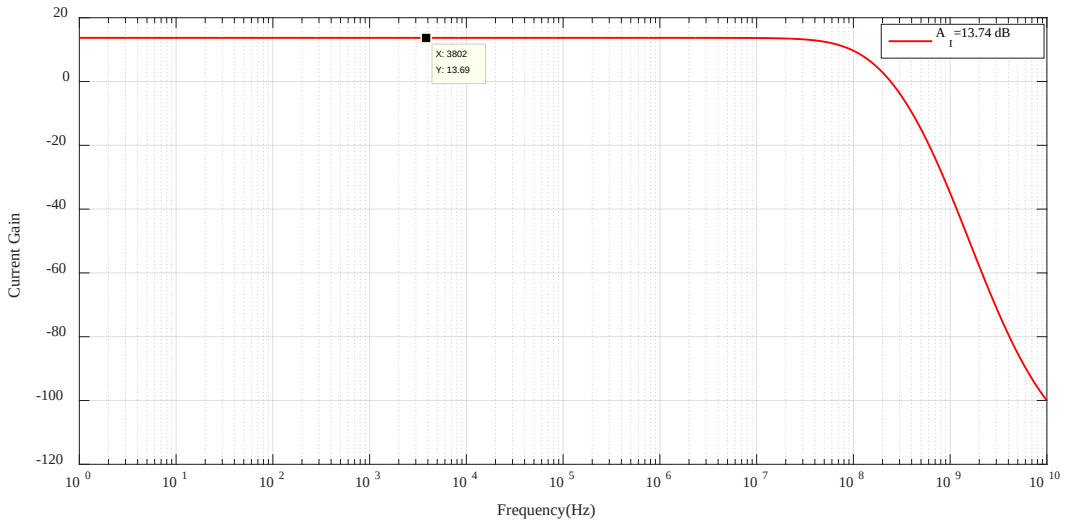


Fig. 3.26 Overall Gain of CD-DITA (I_{x+}/I_n vs frequency) with $I_p = 0$, $I_{b2} = 100\mu A$ and $R_z = 17.74k\Omega$

Thus, from Fig. 3.26 CD-DITA's measured gain and bandwidth can be given as:-

$$\text{Gain} = 13.714dB \quad (3.37)$$

$$\text{B.W.} = 92.842MHz \quad (3.38)$$

Conditions required for measuring the impedances seen through the input and the output terminals of the CD-DITA block are to apply a AC test signal to the terminal at which the impedance has to be measured and open circuit the other current terminals and short circuit other voltage terminals.

The ration of the corresponding voltage and the current at that terminal should be plotted w.r.t. to the frequency and resultant plot will give the impedance seen thorough that terminal.

Theoretically, the impedances seen through the input current terminals i.e. p and n should be low and equal. The input impedances have been presented in the Fig. 3.27 and Fig. 3.28 and the plots verify the theoretical observations.

The values of these impedances measured from their corresponding frequency responses have been written as follows:-

$$Z_p = Z_n = 437.24\Omega \tag{3.39}$$

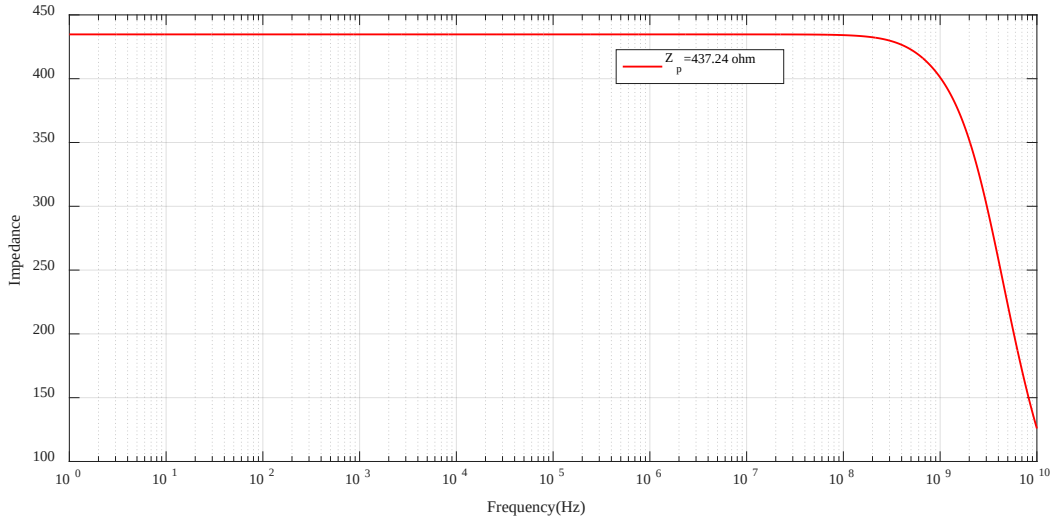


Fig. 3.27 Impedance seen through the p-terminal (Z_p vs frequency)

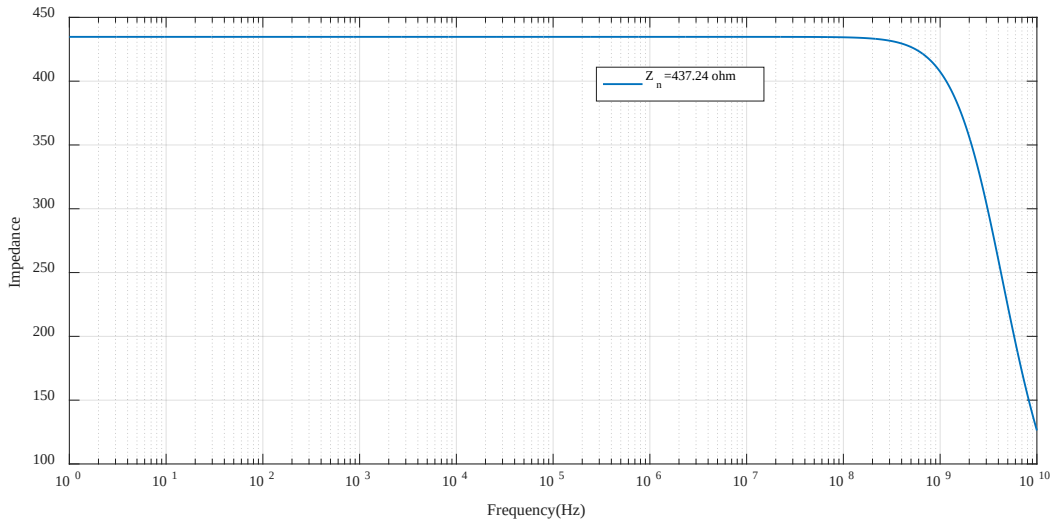


Fig. 3.28 Impedance seen through n-terminal(Z_n vs frequency)

Theoretically, impedances seen through the current output terminals i.e. z and $x\pm$ should be very high and the impedances z and $x\pm$ has been presented in the Fig. 3. 29 and Fig. 3.30 and impedance have been measured out to be of very high value which verifies the theoretical observations. And the measured values of these impedances from their corresponding frequency responses have been given as:-

$$Z_z = 391.979k\Omega \quad (3.38)$$

$$Z_{x\pm} = 1.485M\Omega \quad (3.39)$$

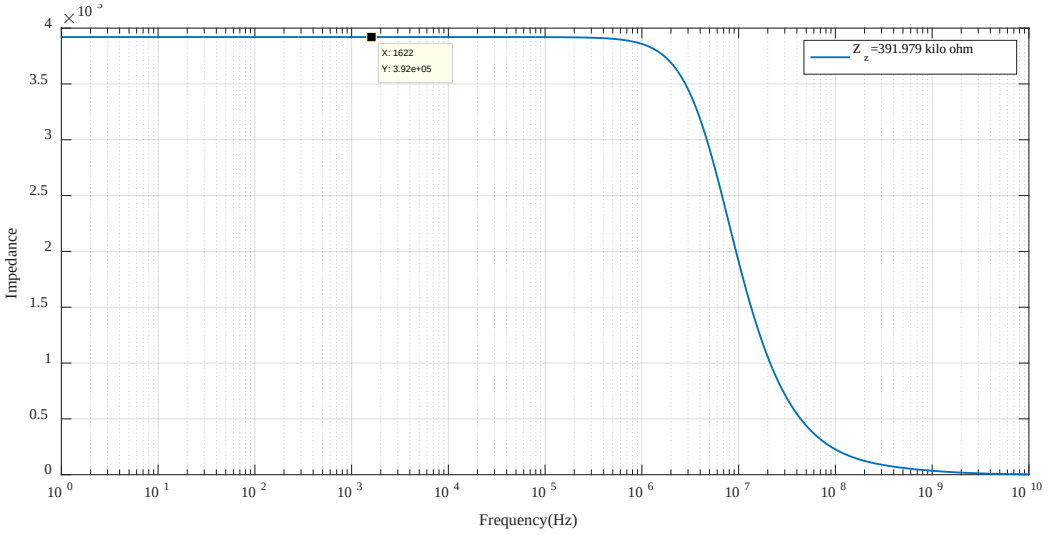


Fig. 3.29 Impedance seen through z -terminal(Z_z vs frequency)

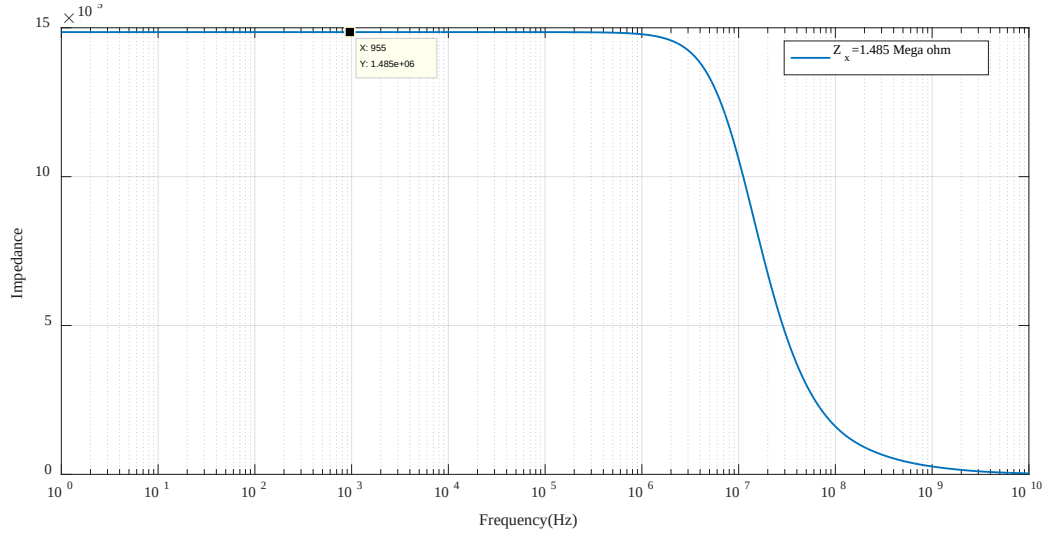


Fig. 3.30 Impedance seen through $x\pm$ terminal($Z_{x\pm}$ vs frequency)

The overall simulated power dissipation of the CD-DITA block based on FVF has been come out as 1.59 milli watts and summary of overall AC and DC performance parameters of the CD-DITA have been listed in Table 3.2.

Table 3.2 Performance parameters of CD-DITA

Parameter	**Value**	**Condition**
Power supplies	$\pm 1.2V$	-
Process parameters	TSMC $0.25\mu m$	-
Dynamic range of the Input currents I_p and I_n	$-100\mu A$ to $100\mu A$	$I_{b1} = I_{b2} = 100\mu A$
Dynamic range of the Input Voltage V_z	$-300mV$ to $300mV$	-
Parasitic gains α_p, α_n	1.021,1.023	Ground the z terminal
Bandwidth for I_z/I_p	$202.445MHz$	Ground the z terminal
Bandwidth for I_z/I_n	$372.759MHz$	Ground the z terminal
Transconductance gain g_m	$281.752\ \mu A/V$	Ground the $x\pm$ terminals and $I_{b2} = 100\mu A$
Bandwidth for I_{x+}/V_z	$244.585MHz$	Ground the $x\pm$ terminals
Overall Gain $g_m R_z$ from p	$13.702dB$	$R_z = 17.74k\Omega$ for gain of $14dB$
Overall Gain $g_m R_z$ from n	$13.714dB$	$R_z = 17.74k\Omega$ for gain of $14dB$
Bandwidth for I_{x+}/I_p	$83.108MHz$	$R_z = 17.74k\Omega$ for gain of $14dB$
Bandwidth for I_{x+}/I_n	$92.842MHz$	$R_z = 17.74k\Omega$ for gain of $14dB$
Input impedances at the input terminals p and n terminals (Z_p, Z_n)	437.24Ω	open circuit z and $x\pm$ terminals

Output impedances at the z Terminal i.e. Z_z	$391.979k\Omega$	open circuit n , p and $x\pm$ terminals
Output impedances at $x\pm$ Terminals i.e. $Z_{x\pm}$	$1.485M\Omega$	open circuit p , n and z terminals
Static Power dissipation	$1.59mW$	$I_p = I_n = 0A$ And open circuit the z and the $x\pm$ terminals

3.4 Realization of CD-DITA based on translinear loop:

In this work, 2nd circuit for CMOS implementation of the CD-DITA [47]block has been used for simulating its filter applications and is presented in Fig. 3.31, where the CDU section is formed by transistors M1-M12 and the DO-OTA section is realized by the transistors M13-M16. This circuit has been simulated using PSPICE with 180nm TSMC parameters. Supply rails used are $\pm 0.9V$.

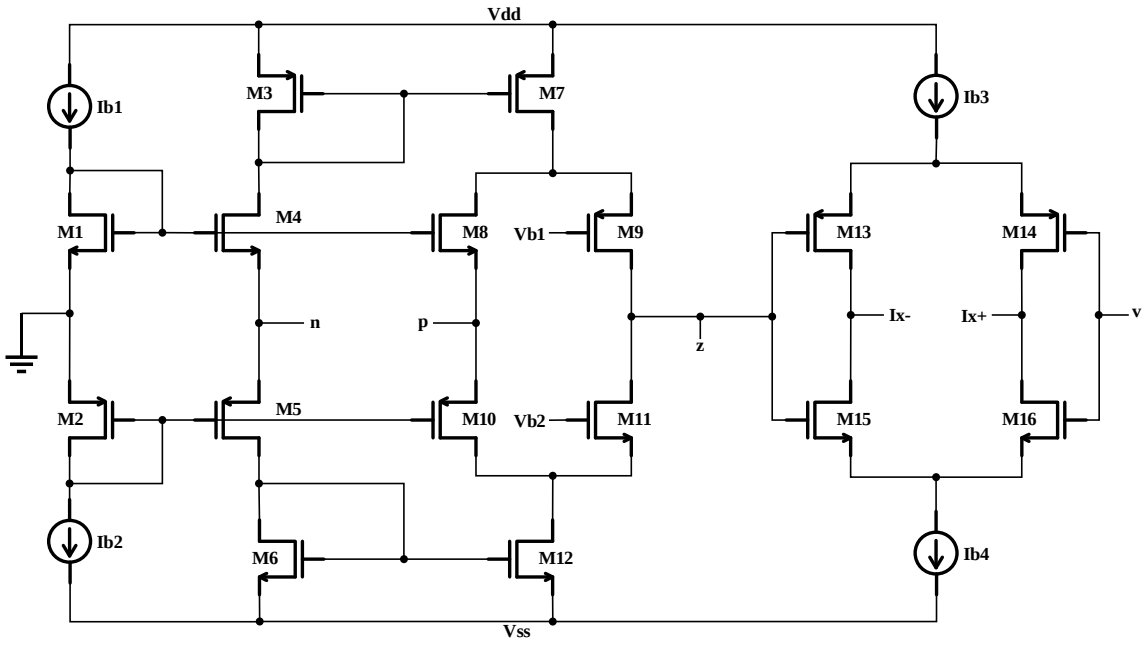


Fig. 3.31 CMOS implementation of CD-DITA[48]

This circuit, used for implementing CD-DITA, is modification of the CDTA circuit that was first presented in [47].M2, M5 and M6 transistors of CDU section are realizing floating current source [47]and transistors M3 and M4 are providing positive feedback which in turn reduces the resistance of input current terminal p. For reducing resistance of input current terminal n, transistors M4 and M6 have been used in CDU section. The DO-OTA section used was first presented in [48].

The aspect ratios of the transistors used to implement the CD-DITA block have been given in table3.3:

Table 3.3Aspect ratios of MOS transistors used in CD-DITA implementation

Transistors	**W** (μm)	**L** (μm)
$M_1 - M_3$	18	0.18
M_4, M_5	36	0.18
$M_6 - M_{12}$	18	0.18
$M_{13} - M_{16}$	6	0.18

The overall transconductance (g_m) of DO-OTA stage of the CD-DITA block can be obtained from the transconductance of the transistors (M13-M16) forming output stage. Approximated value of overall transconductance (g_m) gain can be calculated as:

$$g_m = \frac{(g_{m13} + g_{m15})}{2} \text{ Or } g_m = \frac{(g_{m14} + g_{m16})}{2} \tag{3.40}$$

Where g_{mi} is the transconductance of the ith transistor, defined by:

$$g_{mi} = \sqrt{I_{bi}\mu_{n/p}C_{ox}\left[\frac{W}{L}\right]_i} \tag{3.41}$$

Where

$\mu_{n/p}$ -the carrier mobility for NMOS and PMOS transistors respectively,

C_{ox} - Silicon oxide capacitance per unit area,

$[W/L]_i$ -W/L ratio of i[th] transistor

I_{bi} -bias currents of i[t] transistor.

Both the CDTA and CD-DITA block can be characterized by similar AC & DC characteristics. Here AC behavior of CD-DITA block will be discussed because AC analysis provides the parameters that are related to the non-idealities-of the CD-DITA block which will be useful verifying filter characteristics for non-ideal CD-DITA.

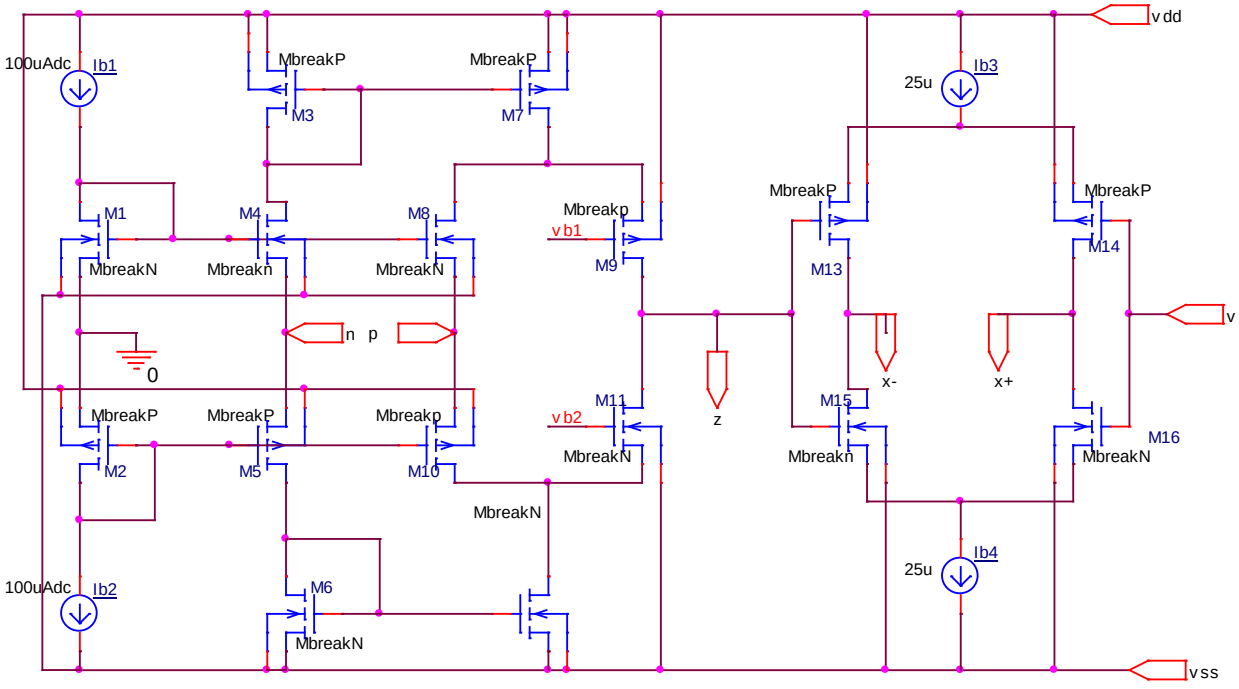


Fig. 3.32 PSPICE schematic of CD-DITA block

PSPICE schematic of CD-DITA block is presented in Fig. 3.32. Bias currents (I_{b1}, I_{b2}, I_{b3}, I_{b4} have been chosen as $100\mu A, 100\mu A$, $25\mu A, 25\mu A$ respectively and bias voltages V_{b1}, V_{b2}, have been chosen as $-400mV$ and $300mV$ respectively.

Frequency response of current transfer ratio p terminal to z terminal i.e. I_z/I_p has been shown in the Fig. 5.5and from this graph the parasitic gain α_p is measured to be as:

$$\alpha_p = \frac{I_z}{I_p} = -173.806mdB \approx 0.9802 \qquad (3.42)$$

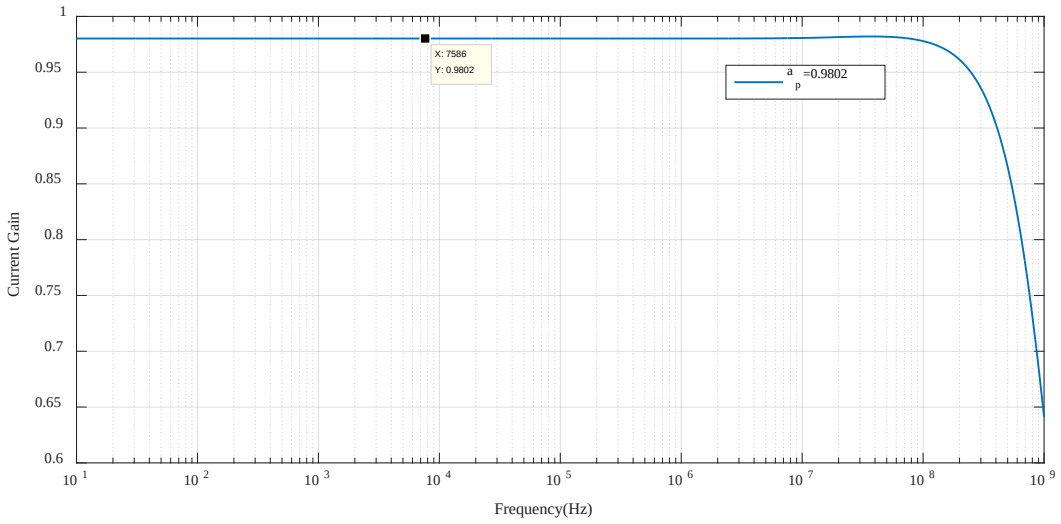


Fig. 3.33 Parasitic Current gain from p terminal to z terminal with $I_n = 0$ (I_z/I_p vs. frequency)

Frequency response of current transfer ratio from n terminal to z terminal i.e. I_z/I_n has been shown in the Fig. 3.34and from this graph the parasitic gain α_n is measured to be as:

$$\alpha_n = \frac{I_z}{I_n} = -388.787mdB \approx 0.9562 \qquad (3.43)$$

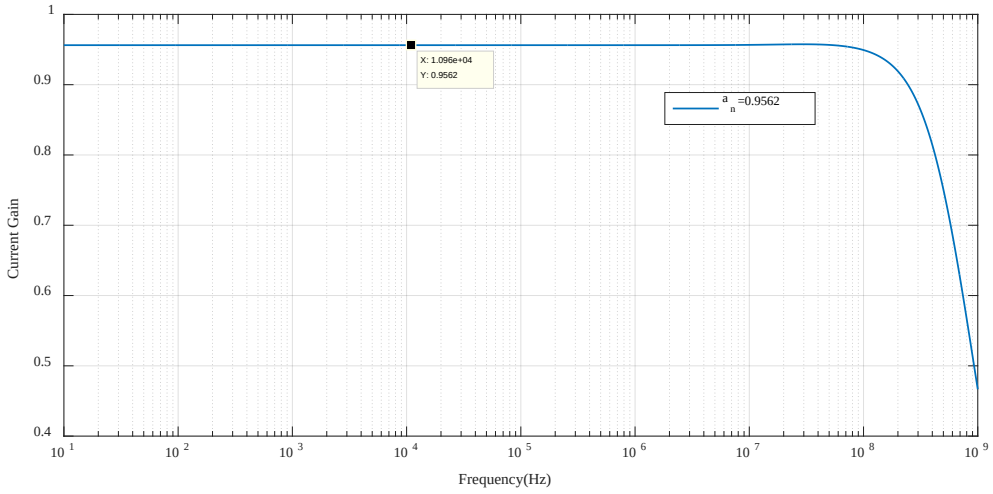


Fig 3.34 Parasitic Current gain from n terminal to z terminal with $I_p = 0$ (I_z/I_n vs frequency)

Fig. 3.35gives frequency response of g_m for fixed I_{b3} and I_{b4} and Fig. 3.36 gives frequency response of g_m by varying bias current I_{b3} and I_{b4} with values $15\mu A$, $20\mu A$ $25\mu A$ and $30\mu A$ and the respective g_m obtained are $155.612\,\mu A/V$, $198.114\,\mu A/V$, $236.659\,uA/V$ and $273.822\,\mu A/V$.

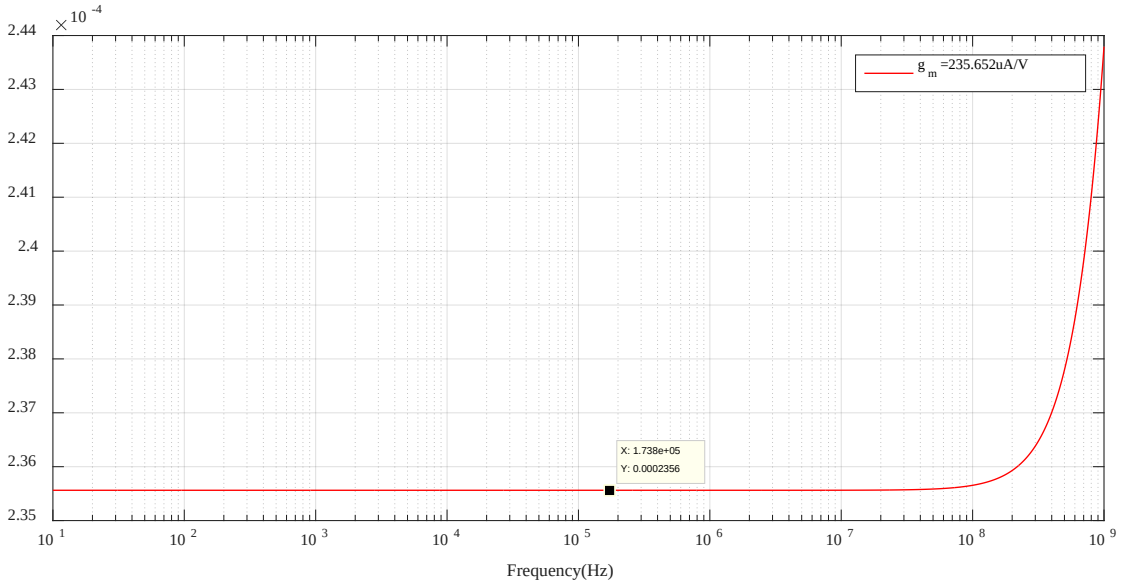


Fig3.35 Transconductance gain g_m from z -terminal to $x+$ terminals

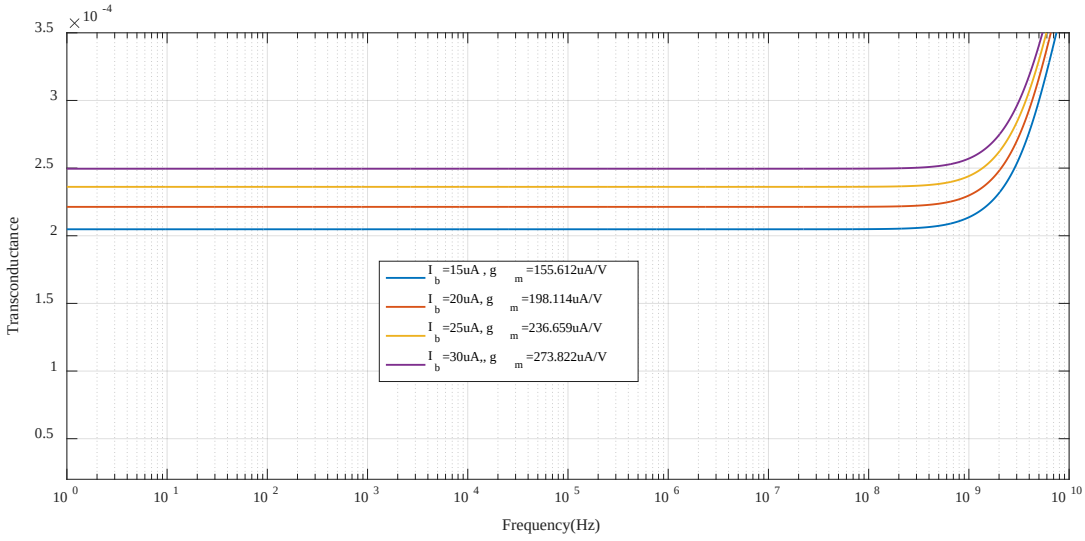


Fig. 3.36Transconductance gain g_m from z -terminal to $x+$ terminals with I_{b3} and I_{b4} as parametric sweep (I_{x+}/V_z vs frequency)

The impedances seen through the input terminals p and n have been found out to be very low and have been presented in Fig. 3.36and Fig. 3.37 respectively .Values of the parasitic

impedances at the input terminals R_p and R_n have been measured from their respective frequency response curves and the parasitic capacitances at these terminals provide negligible effect.

$$R_p \approx 492\Omega \tag{3.44}$$

$$R_n \approx 156.8\Omega \tag{3.45}$$

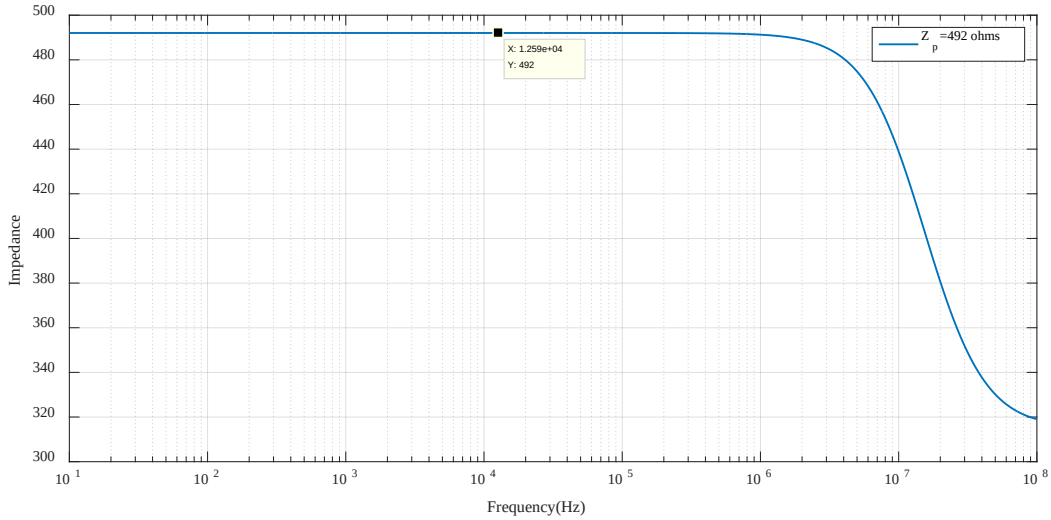


Fig 3.37Impedance seen through p -terminal (Z_p vs frequency)

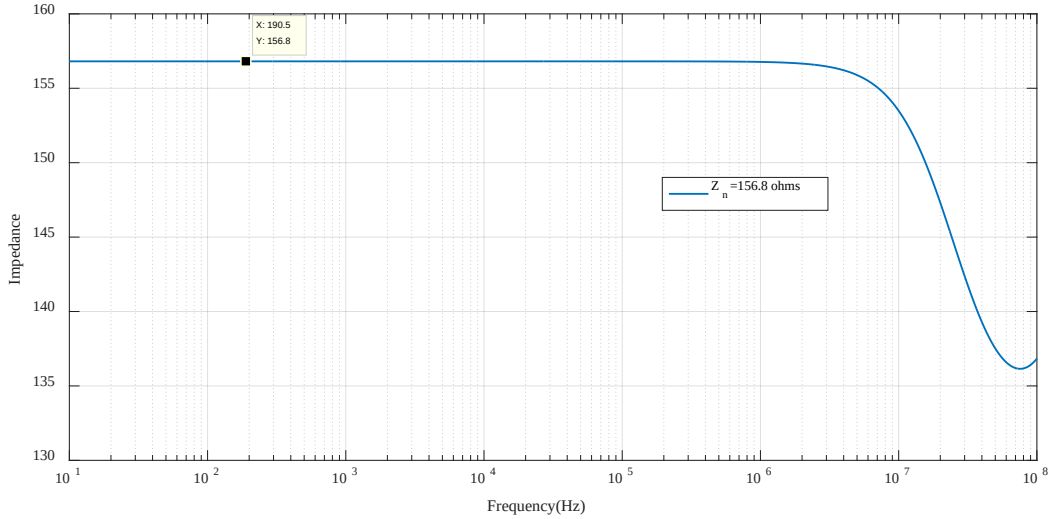


Fig. 3.38 Impedance seen through n -terminal (Z_n vs frequency)

The parasitic resistances R_z and R_x seen through the output terminals z and x have been presented in Fig. 3.37andFig. 3.38and can be measured from the irrespective frequency responses and using values of these parasitic resistances at high frequencies, the parasitic capacitances C_z and C_x can be measured because at high frequencies the effect of parasitic capacitances is predominant.

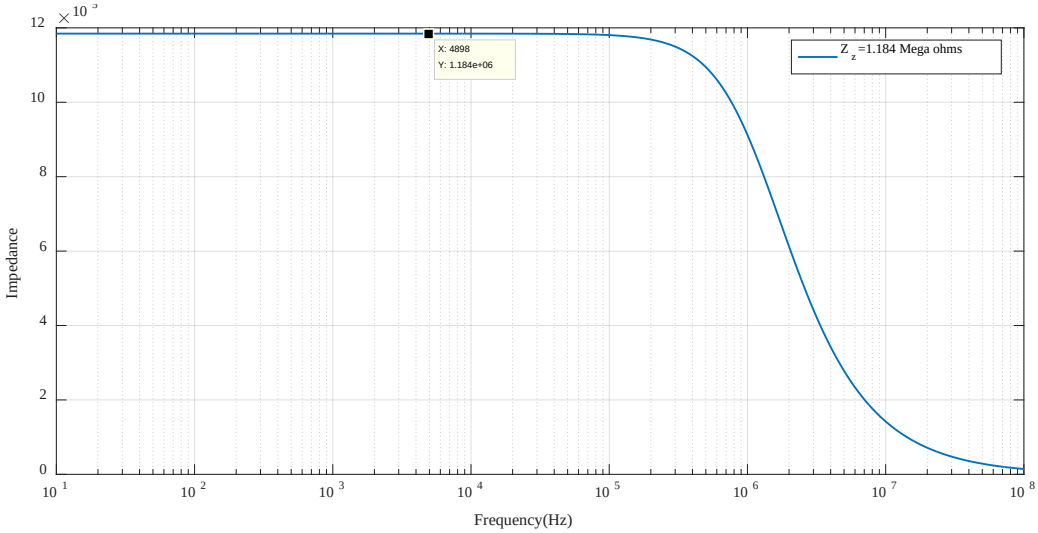


Fig. 3.39Impedance seen through z -terminal (Z_z vs frequency)

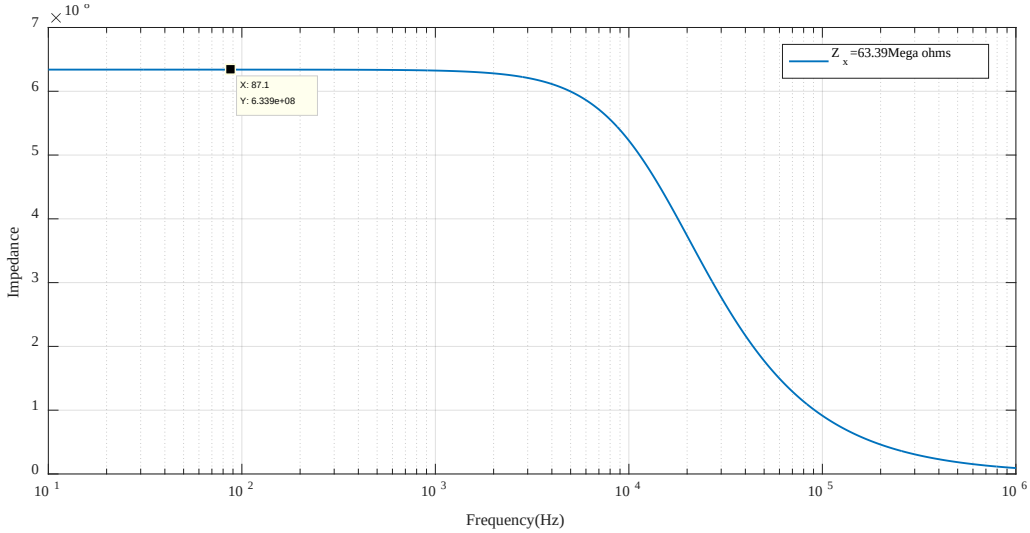


Fig. 3.40Impedance seen through $x \pm$ terminal ($Z_{x\pm}$ vs frequency)

$$\therefore R_z = 1.187 M\Omega \tag{3.46}$$

$$Z_z = \frac{R_z}{1 + sC_zR_z} \therefore |Z_z| = \frac{R_z}{\sqrt{1 + \omega^2 C_z^2 R_z^2}} \quad (3.47)$$

Referring the graph in Fig 3.37 at $f = 2MHz$, $|Z_z| = 1.187M\Omega$

$$\therefore C_z = 88.6\,fF \quad (5.21)$$

Similarly,

$$R_x = 63.39M\Omega \quad (5.22)$$

$$Z_x = \frac{R_x}{1 + sC_xR_x} \therefore |Z_x| = \frac{R_x}{\sqrt{1 + \omega^2 C_x^2 R_x^2}} \quad (5.23)$$

From the graph, at $f = 100MHz$, $|Z_x| = 53.955M\Omega$

$$\therefore C_x = 17.23\,fF \quad (5.24)$$

Thus, the impedances seen through the terminals z and $x\pm$ have been found to be very high theoretically and practically as well.

Chapter 4

CD-DITA based applications

4.1 Basic building blocks:-

Basic applications of CD-DITA like as a simple current amplifier, subtractor, adder, lossless integrator have been implemented using single CD-DITA block and some passive components. The working of these circuit applications have been validated using FVF based CD-DITA using PSPICE simulation. The theoretical results and the practical results are approximately matching hence as a result of this verifying the functionality of CD-DITA based applications.

4.1.1 Simple current amplifier:-

CD-DITA can function as a Current Mirror amplifier as in Fig. 4.1.In this CM, the i/p signal is applied at the p terminal and o/p is obtained either from $x+$ terminal or $x-$ terminal, it totally depends on the requirement of the o/p i.e. inverting or non-inverting. The gain i.e. obtained from the total gain of CD-DITA $(g_m R_z)$

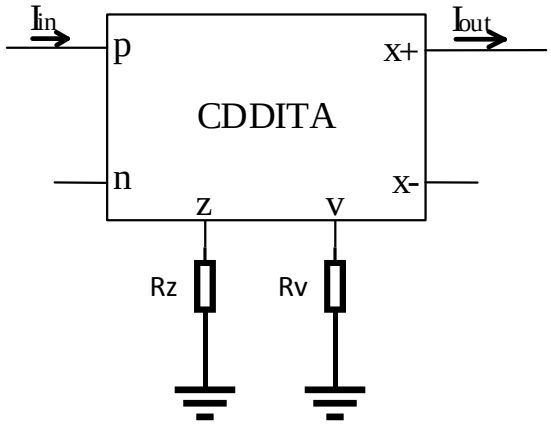


Fig. 4.1 Circuit Schematic of current amplifier based on CD-DITA.

The o/p current of CD-DITA is expressed as following

$$I_{out} = \pm g_m I_{in} R_z \qquad (4.1)$$

Using P-SPICE simulations, I_b i.e. the bias current of the DO-OTA of CDDITA is set to $100\mu A$, which controls the g_m i.e. transconductance of the OTA, and $100\mu A$ value of the base

current leads to the $g_m = 280.329\,\mu A/V$. Hence to obtain an overall CDDITA gain of 6.0023dB or 2 R_z has to be set to the value of $7.3k\Omega$.

And To obtain the transient response, sinusoidal current signal having the range from $-30\mu A$ to $+30\mu A$ have been applied at input and the frequency of the input signal is fixed to $10kHz$.

As in Fig. 4.2, the transient analysis reveals that gain of the output and Fig. 4.3reveals its 3dB bandwidth values obtained as:-

$$Gain = 5.978dB \text{ and } Bandwidth \approx 75.869MHz \qquad (4.2)$$

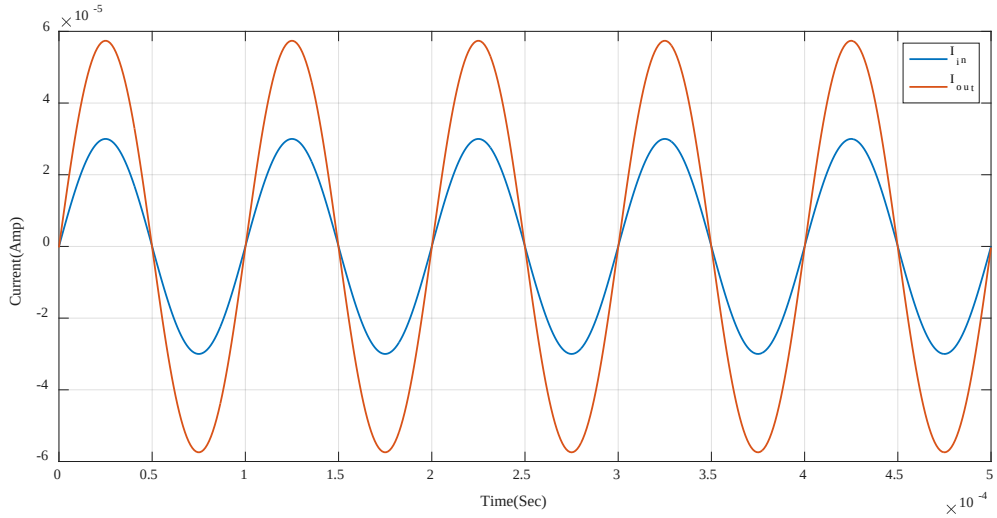


Fig. 4.2 o/p waveform of the simple current mirror amplifier matching to the sinusoidal i/p waveform

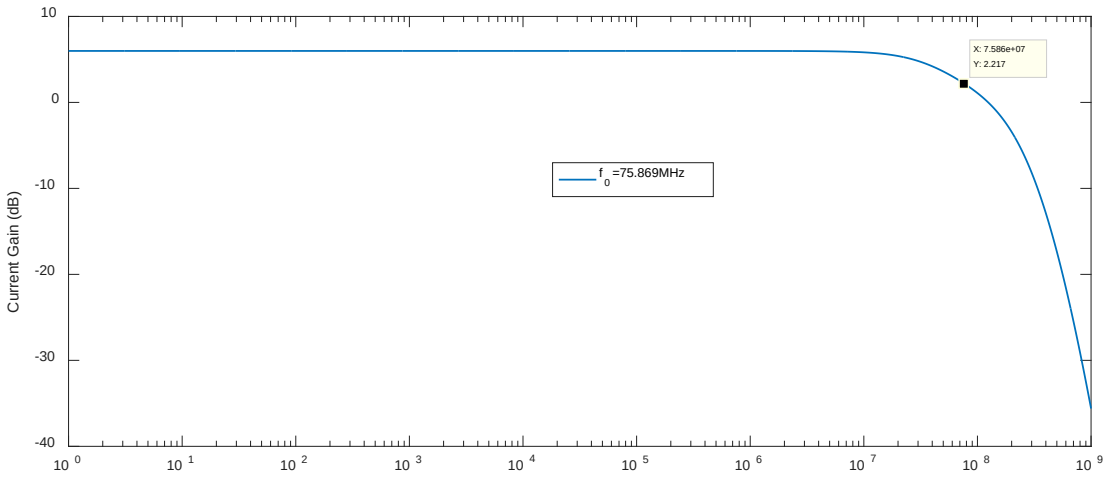


Fig. 4.3 frequency response of simple current mirror amplifier

4.1.2 Adder or Summer amplifier:-

Summing amplifiers are basically the mixers and are the most useful components in the vast analog domain applications. These summing circuits are useful in both the AC and DC, current or voltage analogue signals processing applications. These summer circuits mostly provide an o/p current or voltage i.e. equal to or proportional to the sum of multiple applied i/p's at one of the input terminals. The outputs of these summing amplifiers have been amplified by the constant gain of the active block along with summation of the i/p signals. These summer circuits have been implemented by using at least one active block. Op-Amp circuits have been always the first choice of designers for the basic designing of the summing voltage signals. The current counterpart of these summing amplifiers can be implemented by using any CM-ABB . Here for designing the summing amplifier CD-DITA has been used and the two input signals are applied at the positive terminal of CD-DITA as presented in the Fig. 4.4. The gain of this adder has been obtained by the gain of CD-DITA which is $(g_m.R_z)$

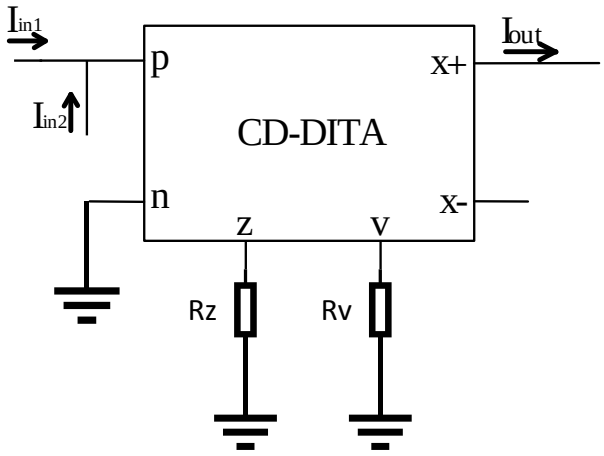


Fig. 4.4 Schematic of the summing amplifier based on CD-DITA.

The o/p current signal of the adder is expressed as

$$I_{out} = I_x = g_m(I_{in1} + I_{in2})R_z \qquad (4.3)$$

Using P-SPICE, the setup of the circuit is same as in current amplifier apart from the value of the R_z . To obtain a gain of 0dB or 1, R_z value has set to be $3.75k\Omega$. For the transient analysis of the circuit, two sinusoidal input signals i.e. current inputs have been applied. One of the input current signals is having the range of $\pm 30\mu A$ and other is having the range of $\pm 20\mu A$. As

presented in the Fig. 4.5, the transient analysis result of the output is shown which is the addition of the two i/p signals. The gain of the summing amplifier can be controlled using g_m or R_z which form basically the proportionality factor i.e. amplification along with addition of the inputs at the o/p. The 3dB bandwidth and gain are obtained from points A and B in frequency response as shown in Fig. 4.6. Therefore,

$$Gain \approx 0dB \text{ and } Bandwidth \approx 65.497MHz \qquad (4.4)$$

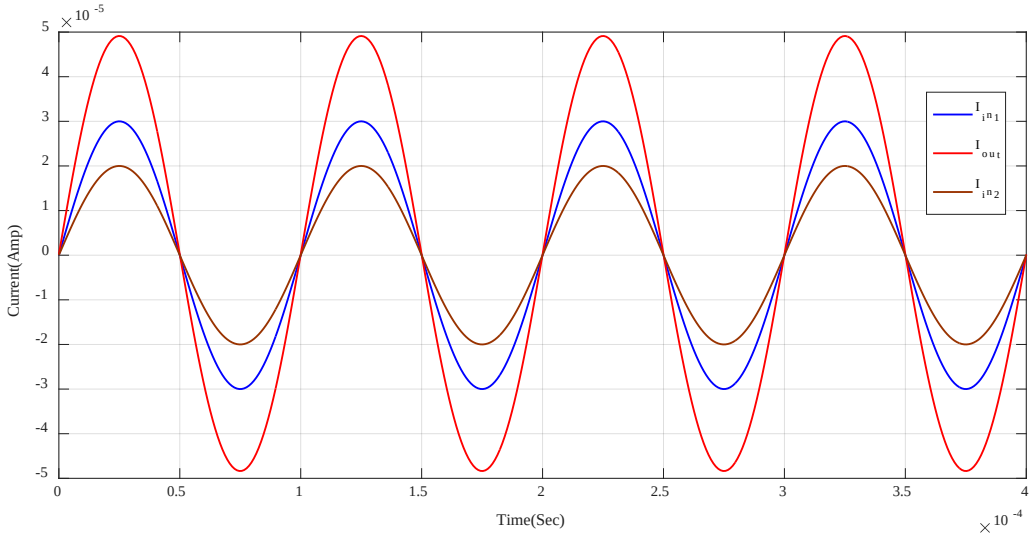


Fig. 4.5 waveforms of the output and two sinusoidal inputs of the summing amplifier

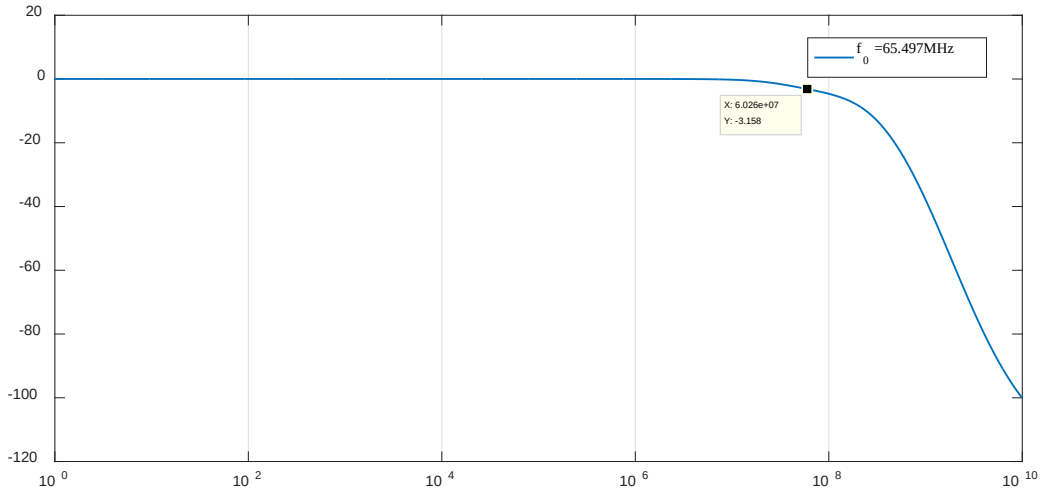


Fig. 4.6 the frequency response of the summing amplifier

4.1.3 Subtractor or The differential amplifier:

Subtractor or the differential amplifier provides an o/p current or voltage that is equal to or proportional to the difference of the multiple inputs applied at the input terminals of the CD-DITA. The Voltage Mode subtractors or the differential amplifiers have been mostly designed and implemented using op-amps because these are voltage mode active blocks. the Current Mode counterpart of these differential amplifiers o subtractors can be implemented by using CD-DITA, in this configuration one of the current i/p's is applied at negative terminal of CD-DITA and another current i/p is applied at the positive terminal as presented in the Fig. 4.7.

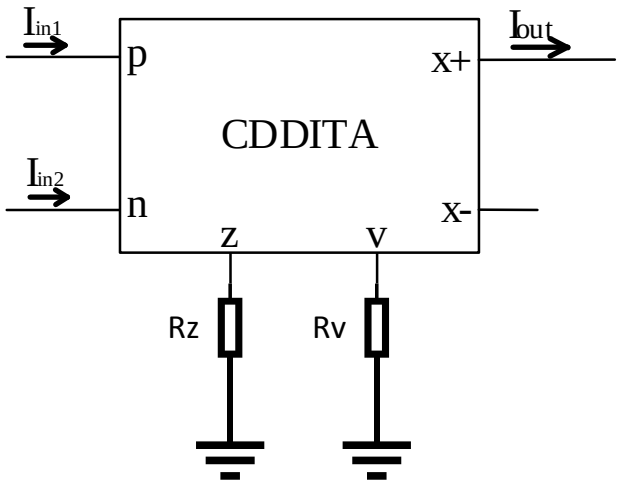


Fig. 4.7 Schematic of the current differential amplifier based on CDDITA.

The current output of CDDITA based subtractor or differential amplifier has been expressed as following:

$$I_{out} = I_x = g_m\left(I_{in1} - I_{in2}\right)R_z \qquad (4.5)$$

Using P-SPICE simulations, there the value of R_z has been set to $27k\Omega$ to get the gain of 16.9dB or 7. As presented in the Fig. 4.8, the transient analysis of the o/p that is the subtraction of the two i/p signals is shown in the below figure. An amplification of factor 7 is obtained in the output signal. The 3dB bandwidth and gain has been obtained from the points A and B in the frequency response presented in the Fig. 4.9. Thus,

$$Gain \approx 16.464dB \text{ and } Bandwidth \approx 63.697\text{MHz} \qquad (4.6)$$

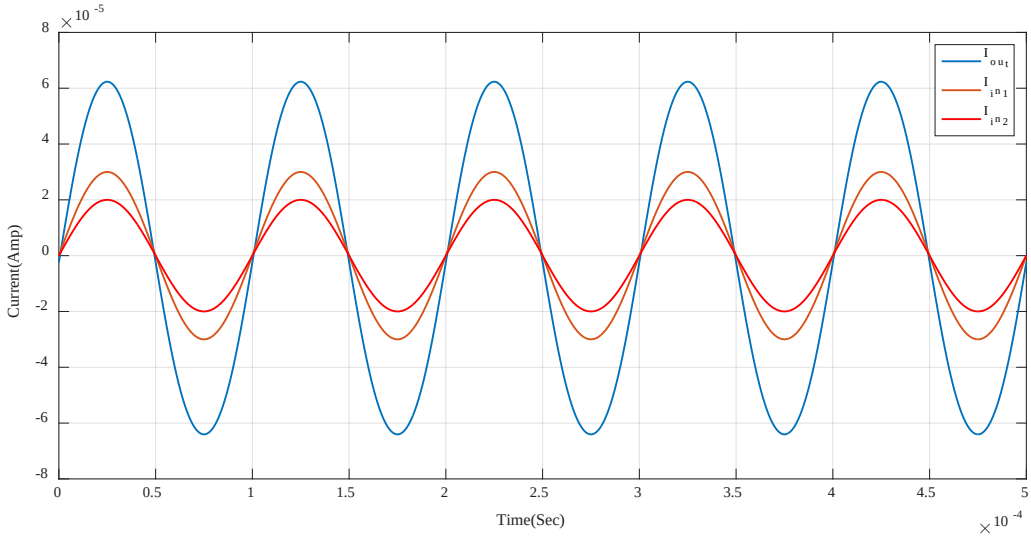


Fig. 4.8 Simulated waveforms of outputs to two sinusoidal i/p's of current differential amplifier based on CDDITA

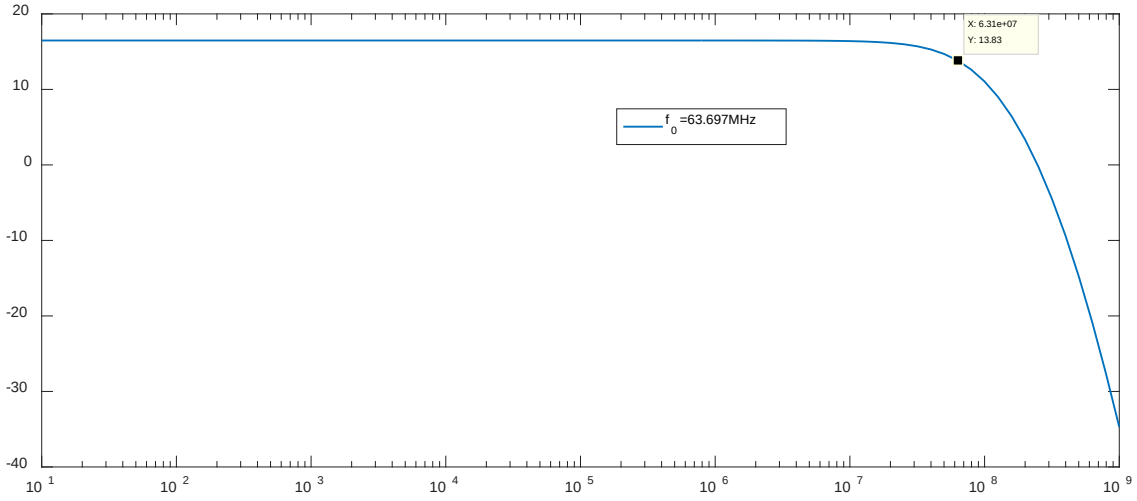


Fig. 4.9 the frequency response of the current differential amplifier based on CDDITA

4.1.4 Lossless integrator:

A simple Current Mode $g_m.C$ lossless integrator has been designed using single CDDITA. The lossless integrator circuit has been implemented using the same and has been shown in the

Fig. 4.10 and the integrating action at the output is obtained by employing a grounded capacitor as load at the terminal z of the CD-DITA.

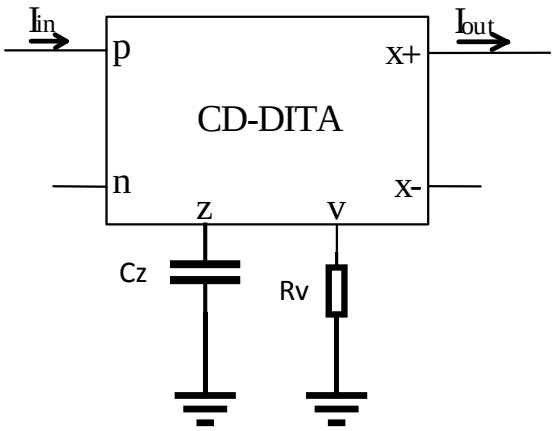


Fig. 4.10. Schematic of lossless integrator based on CD-DITA.

The o/p current of this integrator circuit has been expressed as the following equation:-

$$I_{out} = I_x = \frac{g_m}{sC_z}(I_{in}) \qquad (4.7)$$

Using the P-SPICE simulations, the value of C_z has been set to $0.5nF$ .For the transient analysis, one sinusoidal current input signal has been applied at the input terminal of the CD-DITA and this input current signal is applied with range of $\pm 30\mu A$. As presented in the Fig. 4.11, the transient analysis shows that the output signal has phase difference of 90^0 w.r.t. the corresponding input signal.

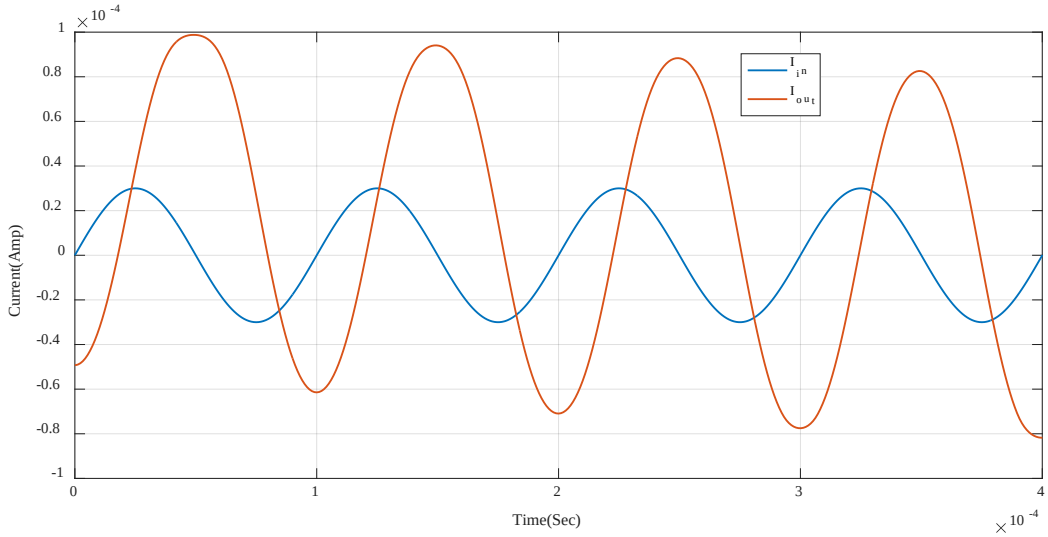


Fig. 4.11 Simulated o/p waveform of lossless integrator corresponding to sinusoidal i/p's

4.2 First Order All Pass Filter Using CD-DITA:

A first order APF is treated as among the most important active building blocks for many analogue signal processing applications. First Order APF has been widely used for the phase shifting applications along with maintaining the constant gain over the desired frequency range so that the amplitude of the output signal can be maintained constant as well.

First order APF finds applications in various domains such as quadrature oscillators and delay equalizers [49] ,and also in realizing active bandpass filters with the high selectivity. A large literature can be obtained on first order filters that have been realized using various active blocks such as OTAs[50] , DVCC [51], OTRAs[53]. All these configurations suffered from the drawbacks of excessive use of active building blocks and also excessive use of the resistors and capacitors or use of floating capactive elements and along with the non availability of the electronic control of various circuit parameters

First order APF using CD-DITA overcomes all the drawbacks by providing electronically tunability of the circuit parameters and employing single CD-DITA along with one capacitor and resistor for implementation. The APF using CD-DITA block has been shown in the below figure Fig:4.12

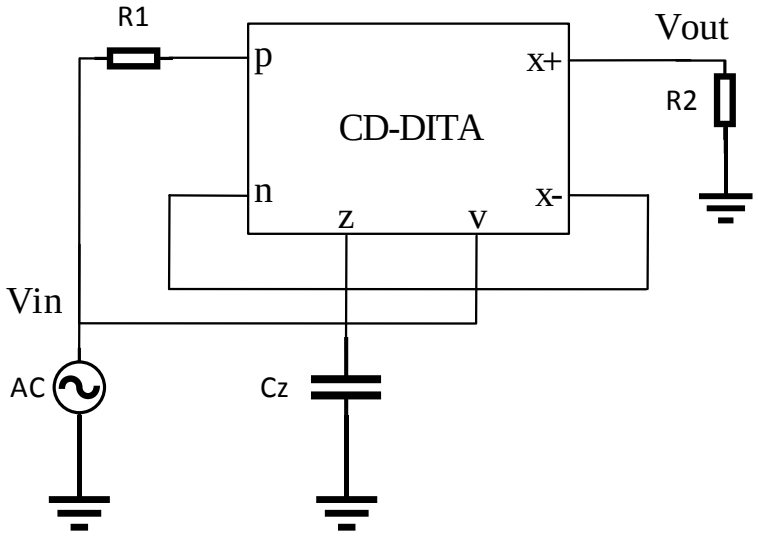


Fig: 4.12Schematic of first order APF based on CD-DITA

AC voltage input signal has been applied at v terminal and at p terminal through resistor R_1.

From the circuit analysis of the Voltage Mode-APF presented in the Fig. 5.1, the following transfer function can be obtained:-

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{sC_z - g_m}{sC_z + g_m} \tag{4.8}$$

Where

$$R_1 = R_2 = \frac{1}{g_m} \tag{4.9}$$

Equation 4.8 suggests that voltage gain A_v obtained in the transfer function is unity and the pole frequency ω_0 calculated from the Equation 5.1 can be given as:-

$$\omega_0 = \frac{g_m}{C_z} \tag{4.10}$$

And the phase response i.e. obtained from Equation 4.8 can be given as

$$\angle \frac{V_{out}(s)}{V_{in}(s)} = \phi(\omega_p) = \pi - 2\tan^{-1}\left(\frac{\omega_p C_z g_m}{g_m}\right) \tag{4.11}.$$

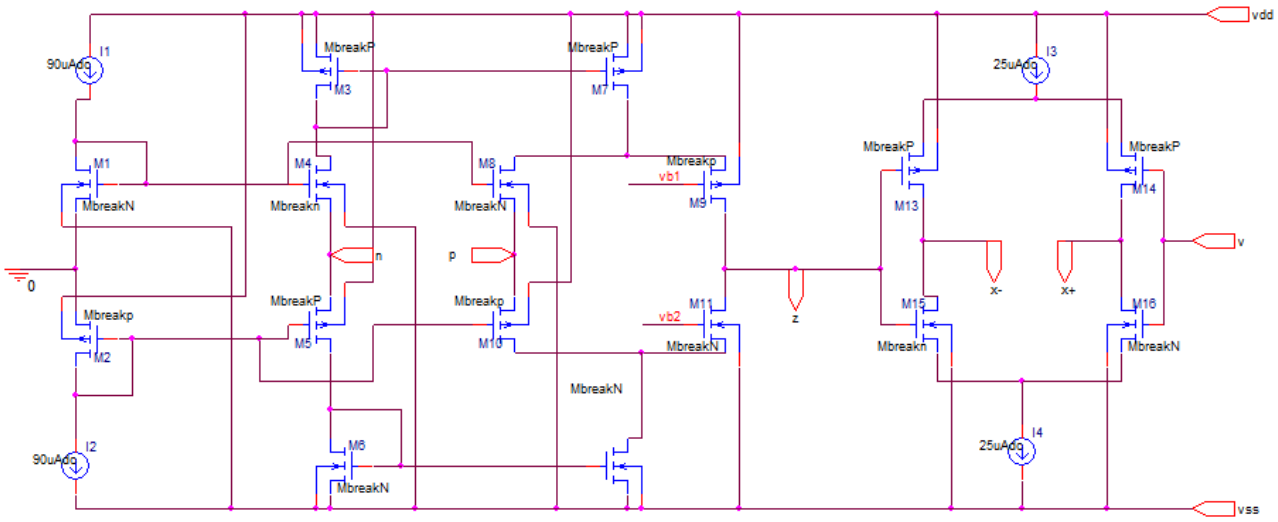


Fig. 4.13 PSPICE schematic of CD-DITA

The circuit behavior has been verified using the P-SPICE and the simulation results have been obtained by employing Translinear Loop based CDDITA as shown in the Fig. 4.13. and supply

used is $\pm 0.9V$ DC and biasing currents taken as $I_{b_1} = 90uA$ and $I_{b_2} = 25uA$. And the CD-DITA circuit has been implemented using $180nm$ technology parameters.

The frequency response analysis of the first order APF has been performed using PSPICE and its magnitude response has been presented in this Fig. 4.14 which suggests gain is $0.443dB$ and phase response has been presented in the Fig. 4.15.

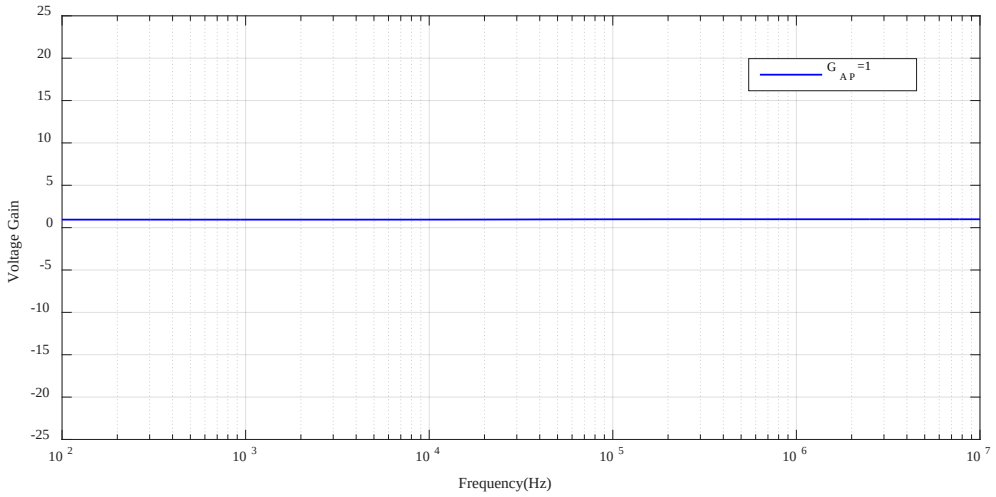


Fig. 4.14 Magnitude response of the first order APF

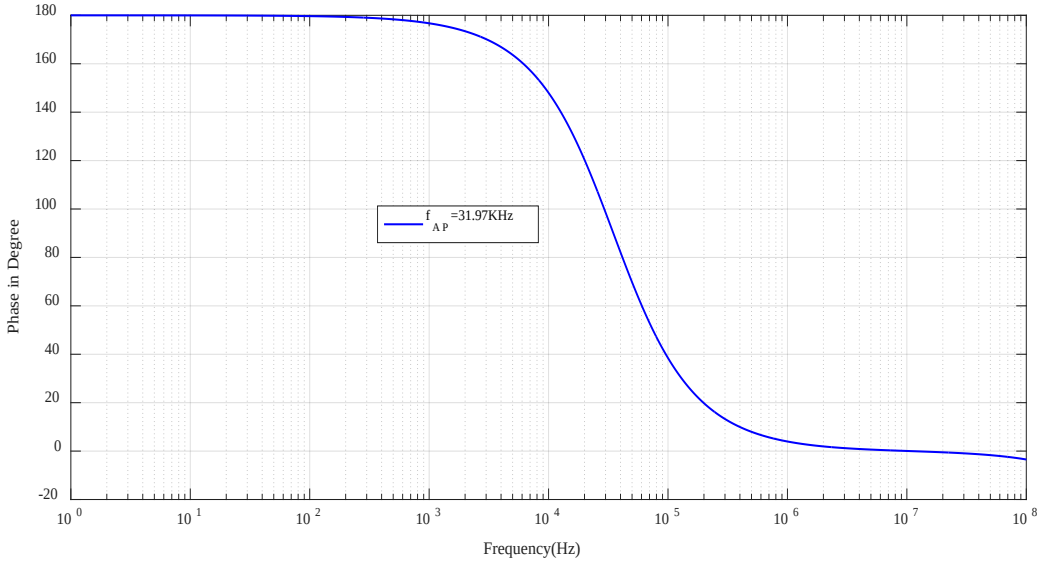


Fig. 4.15 Phase response of the First Order APF

4.3 CD-DITA based CM-SIMO type universal filter:-

4.3.1 Basic Introduction:-

Active filters have been always one of the most important and frequently used basic building blocks. Active filters are mostly used in many electrical and electronics engineering applications. There are various approaches to design any active filters but mostly the CM approach for designing the active filters is becoming popular now a days due to the advantageous features CM approach offers over other approaches for example such as dynamic range for CM filters is large and also wide bandwidth when CM Counterparts are compared to VM counterparts if we particularly talk about the higher frequency operations, low power consumption and also simple filtering configurations.

Among the filter topologies the widely used topology is SIMO type CM filters. The SIMO based circuit is also capable of implementing the three basic filter functions i.e. LP, BP and HP whereas the remaining two output responses i.e. notch and AP can be obtained by summing the right output currents that too without changing the components and also topology of the circuit. One such CM filter using on single CD-DITA is given in this work.

4.3.2 CM Filter based on single CD-DITA:-

SIMO type CM universal biquad filter using single CD-DITA has been shown in Fig. 4.16. This CM biquad circuit consists of one floating resistor and two grounded capacitors along with one active element i.e. CDDITA.

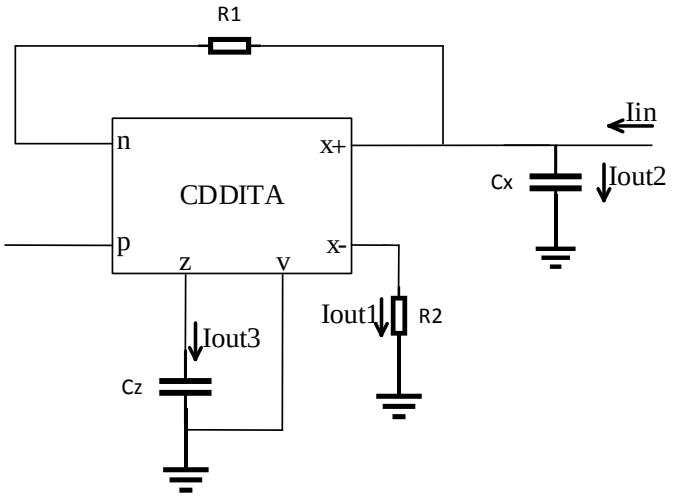


Fig. 4.16 CD-DITA based SIMO-type CM Universal filter circuit.

Considering the ideal analysis of the CD-DITA block, the basic circuit analysis of the new filter shown in the figure4.16 gives the relation between the output currents and input current and as given in the following equations:-

1. If I_{out} is taken across I_{x-} i.e. $I_{out} = I_{x-}$ and input I_{in} is applied at the $x+$ terminal of CD-DITA then low pass filter(LPF) will be realized as shown in the equation:-

$$\frac{I_{LP}}{I_{in}} = \frac{I_{x-}}{I_{in}} = \frac{g_m}{s^2 C_1 C_2 R_1 + sC_2 + g_m} \tag{4.12}$$

2. If I_{out} is taken across C_x i.e. I_{C_1} i.e. $I_{out} = I_{C_1}$, then high pass filter (HPF) can be realized as shown in the equation:-

$$\frac{I_{HP}}{I_{in}} = \frac{I_{C_1}}{I_{in}} = \frac{s^2 C_1 C_2 R_1}{s^2 C_1 C_2 R_1 + sC_2 + g_m} \tag{4.13}$$

3. If I_{out} is taken across C_z i.e. I_{C_2} i.e. $I_{out} = I_{C_2}$, then inverting Band Pass Filter(BPF) can be realized as shown in the equation:-

$$\frac{I_{BP}}{I_{in}} = \frac{I_{C_2}}{I_{in}} = \frac{-sC_2}{s^2 C_1 C_2 R_1 + sC_2 + g_m} \tag{4.14}$$

4. If I_{out} is taken as the summation of the output currents I_{x-} and I_{C_1} i.e $I_{out} = I_{x-} + I_{C_1}$, then the resulting filter that can be implemented will be Band Reject Filter (BRF) or notch filter, the implementation of notch filter can be shown through the equation below:-

$$\frac{I_{BR}}{I_{in}} = \frac{I_{LP} + I_{HP}}{I_{in}} = \frac{I_{x-} + I_{C_1}}{I_{in}} = \frac{s^2 C_1 C_2 R_1 + g_m}{s^2 C_1 C_2 R_1 + sC_2 + g_m} \tag{4.15}$$

5. If I_{out} is taken as the summation of the output currents I_{x-}, I_{C_1} and I_{C_2} i.e. $I_{out} = I_{x-} + I_{C_1} + I_{C_2}$, then the resulting filter that can be implemented will be All Pass Filter (APF), the implementation of All Pass Filter can be shown through the equation below:-

$$\frac{I_{AP}}{I_{in}} = \frac{I_{LP} + I_{HP} + I_{BP}}{I_{in}} = \frac{I_{x-} + I_{C_1} + I_{C_2}}{I_{in}} = \frac{s^2 C_1 C_2 R_1 - sC_2 + g_m}{s^2 C_1 C_2 R_1 + sC_2 + g_m} \quad (4.16)$$

From Equation 4.12 to Equation4.16, the denominator of all the equations is same and that is:-

$$D(s) = s^2 C_1 C_2 R_1 + sC_2 + g_m \quad (4.17)$$

And denominator of the filter transfer functions i.e. $D(s)$ gives the theoretical value of the natural frequency (ω_n) also called as the pole frequency of the filter and $D(s)$ also gives the theoretical value of the quality factor (Q_0) of the filter.

The natural frequency can be expressed by the following equation i.e. derived from the $D(s)$ the denominator:-

$$\omega_n = \sqrt{\frac{g_m}{R_1} \cdot \frac{1}{C_1 C_2}} \quad (4.18)$$

Quality factor can be expressed by the following equation i.e. derived from the $D(s)$ the denominator:-

$$Q_0 = \sqrt{g_m R_1 \cdot \frac{C_2}{C_1}} \quad (4.19)$$

If the value of resistor R_1 is set to be as

$$R_1 = \frac{1}{g_m} \quad (4.20)$$

Then the resulting value of the quality factor will be independent of any variation of the transconductance gain and also the variation in the resistor R_1 and the value of the natural frequency becomes:-

$$\omega_n = g_m \sqrt{\frac{1}{C_1 C_2}} \qquad (4.21)$$

And the value of the quality factor becomes:-

$$Q_0 = \sqrt{\frac{C_2}{C_1}} \qquad (4.22)$$

From the above equation 5.25 and equation 5.26, it can be settled that once the value of the quality factor i.e. Q_0 of the filter is adjust to some value by using the capacitors C_1 and C_2 then, ω_n of the filter can be tuned electronically and also independently of Q_0 by just varying the DO-OTA's g_m which means the transconductance gain of the DO-OTA

The Current gains of all the filters are unity and can be expressed as following equations:-

$$G_{LP} = G_{BP} = G_{HP} = G_{BR} = G_{AP} = 1 \qquad (4.23)$$

4.3.3 **Sensitivity Analysis**:-

Sensitivity Analysis is a technique that is used to determine how the independent variable values will effect the particular dependent parameter values under a specific set of assumptions. The sensitivity analysis, of natural frequency (ω_n) i.e. referring equation 4.21and of quality factor (Q_0) i.e. referring equation 4.22, due to the variations of all the passive and the active elements can be given by the following equations:

$$S_{g_m}^{\omega_n} = \frac{1}{2} \text{ and } S_{R_1}^{\omega_n} = S_{C_1}^{\omega_n} = S_{C_2}^{\omega_n} = -\frac{1}{2} \qquad (4.24)$$

$$S_{g_m}^{Q_0} = S_{R_1}^{Q_0} = S_{C_2}^{Q_0} = \frac{1}{2} \text{ and } S_{C_1}^{Q_0} = -\frac{1}{2} \qquad (4.25)$$

By observing the equations 4.24 and 4.25 the conclusion that can be made is that all the active and the passive of sensitivities of this circuit are half i.e. less than unity.

4.3.4 Effect of non-idealities of the CD-DITA on filter performance:

Due to the various non-idealities present in the CD-DITA block, the performance of the CD-DITA based Current Mode New filter may slightly deflect or vary from its ideal behavior. The equivalent circuit of the CD-DITA block in the presence of various nonidealities at input and intermediate terminals has been already discussed in one of the previous sections of this work. The non-ideal model of the CD-DITA block can be shown as:-

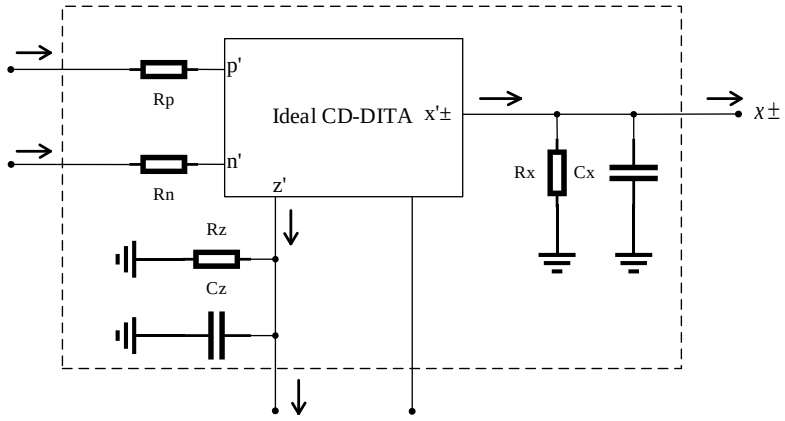


Fig. 4.17 CD-DITA circuit model with non-idealities

The various errors present such as the transfer error in the transconductance of the DO-OTA and the tracking errors present in CDU, and also the parasitics present at the input, output and intermediate terminals of the CD-DITA block will all affect the filter performance especially when used in CM.

The probability of affecting the filter performance due to the parasitics present at the z terminal and at the $x\pm$ terminal of the CD-DITA depends upon how these parasitics will appear with the externally connected passive filter elements. These parasitics are either absorbed by the externally connected grounded impedances only when these parasitics will appear in shunt or in parallel with the grounded impedances or these parasitics will add extra terms in the transfer functions which shows that these can not only affect the center frequency of the filter and quality factor of the filter, but also these parasitics can add parasitic zeros to some of the filter responses. In this new filter circuit using CD-DITA, parasitic capacitances C_z and C_x , i.e. present at z and x terminals, will appear in shunt or in parallel with the externally connected capacitance C_2 and C_1, respectively. The externally connected resistance R_1 between the n terminal and the x terminal of the CD-DITA block will be increased by the parasitic resistance present at the n terminal i.e. R_n, and hence in the similar way the parasitic present at the p terminal of the CD-DITA is R_p .Thus , the overall parasitic resistance present at the x terminal of the CD-DITA block will be equal to the parasitic resistance present at the x terminal i.e. R_x in parallel with $R_1 + R_n$. The Parasitic resistance R_z i.e. present at the z terminal of CD-DITA

neither appears in parallel nor in series with any of the externally connected impedances and hence it will cause the considerable variations in the filter responses

Considering the non-idealities of CD-DITA into account the relationship between the output currents and input currents can be modified as:

1. If I_{out} is taken across I_x i.e. $I_{out} = I_x$ and input I_{in} is applied at the $x+$ terminal of CDDITA then low pass filter(LPF) will be modified to a new transfer function as shown in the equation:-

$$\frac{I_{LP}}{I_{in}} = \frac{I_{x-}}{I_{in}} = \frac{g_m \beta_z \alpha_n G_1^*}{s^2 C_1^* C_2^* + s\left(C_1^* G_z + C_2^* G_1^* + C_2^* G_x\right) + \left(\beta_z g_m \alpha_n G_1^* + G_x G_z + G_1^* G_z\right)} \quad (4.26)$$

2. If I_{out} is taken across I_{C_1} i.e. $I_{out} = I_{C_1}$, then high pass filter (HPF) will be modified to a new transfer function as shown in the equation:-

$$\frac{I_{HP}}{I_{in}} = \frac{I_{C_1}}{I_{in}} = \frac{s^2 C_1^* C_2^* + s G_z C_1^* + s G_x C_2^* + G_z G_x}{s^2 C_1^* C_2^* + s\left(C_1^* G_z + C_2^* G_1^* + C_2^* G_x\right) + \left(\beta_z g_m \alpha_n G_1^* + G_x G_z + G_1^* G_z\right)} \quad (4.27)$$

3. If I_{out} is taken across I_{C_2} i.e. $I_{out} = I_{C_2}$, then inverting Band Pass Filter (BPF) will be modified to a new transfer function as shown in the equation:-

$$\frac{I_{BP}}{I_{in}} = \frac{I_{C_2}}{I_{in}} = \frac{-(s\alpha_n G_1^* C_2^* + \alpha_n G_z G_1^*)}{s^2 C_1^* C_2^* + s\left(C_1^* G_z + C_2^* G_1^* + C_2^* G_x\right) + \left(\beta_z g_m \alpha_n G_1^* + G_x G_z + G_1^* G_z\right)} \quad (4.28)$$

Where

$$C_1^* = C_1 + C_x \text{ and } C_2^* = C_2 + C_z \quad (4.29)$$

$$G_z = \frac{1}{R_z} \text{ and } G_x = \frac{1}{R_x} \quad (4.30)$$

$$G_1^* = \frac{1}{R_1 + R_n} \text{ and } G_2^* = \frac{1}{R_2 + R_p} \quad (4.31)$$

For simplicity the filter responses, we can ignore the parasitic resistance present at the x terminal i.e. R_x because R_x is a very large value parasitic resistance i.e. typically its value is in mega ohms and also R_x appears in shunt or in parallel with $R_1 + R_n$ which has low value in comparison with R_x i.e. the typical value of $R_1 + R_n$ is in kilo ohms. Thus, the modified expression for I_{out} for all the expressions can be given as

1. If I_{out} is taken across I_x i.e. $I_{out} = I_x$ and input I_{in} is applied at the $x+$ terminal of CDDITA then low pass filter (LPF) will be modified to a new transfer function as shown in the equation:-

$$\frac{I_{LP}}{I_{in}} = \frac{I_{x-}}{I_{in}} = \frac{g_m \beta_z \alpha_n G_1^*}{s^2 C_1^* C_2^* + s\left(C_1^* G_z + C_2^* G_1^*\right) + \left(\beta_z g_m \alpha_n G_1^* + G_1^* G_z\right)} \tag{4.32}$$

2. If I_{out} is taken across I_{C_1} i.e. $I_{out} = I_{C_1}$, then high pass filter (HPF) will be modified to a new transfer function as shown in the equation:-

$$\frac{I_{HP}}{I_{in}} = \frac{I_{C_1}}{I_{in}} = \frac{s^2 C_1^* C_2^* + s G_z C_1^*}{s^2 C_1^* C_2^* + s\left(C_1^* G_z + C_2^* G_1^*\right) + \left(\beta_z g_m \alpha_n G_1^* + G_1^* G_z\right)} \tag{4.33}$$

3. If I_{out} is taken across I_{C_2} i.e. $I_{out} = I_{C_2}$, then inverting Band Pass Filter (BPF) will be modified to a new transfer function as shown in the equation:-

$$\frac{I_{BP}}{I_{in}} = \frac{I_{C_2}}{I_{in}} = \frac{-(s\alpha_n G_1^* C_2^* + \alpha_n G_z G_1^*)}{s^2 C_1^* C_2^* + s\left(C_1^* G_z + C_2^* G_1^*\right) + \left(\beta_z g_m \alpha_n G_1^* + G_1^* G_z\right)} \tag{4.34}$$

From the equation (4.34), it can be seen that the parasitic resistance R_z present at the z terminal adds a zero in the BPF transfer function which, in turn, gives the finite low-frequency attenuation in the BPF frequency response. This low-frequency attenuation can be increased if we keep $R_z \rangle\rangle R_1 + R_n$. This condition can be achieved by simply designing the CDU section of

the CD-DITA block for high output resistance. The natural frequency ω_n and the quality factor Q_0 have been also affected by the parasitic resistance R_z present at the z terminal and can be expressed as the following equations:

$$\omega_n = \sqrt{\frac{\beta_z g_m \alpha_n G_1^* + G_1^* G_z}{C_1^* C_2^*}} \tag{4.35}$$

$$\therefore \omega_n = \sqrt{\frac{\beta_z g_m \alpha_n R_z + 1}{(C_1 + C_x)(C_2 + C_z) R_z (R_1 + R_n)}} \tag{4.36}$$

$$Q_0 = \sqrt{\frac{C_1^* C_2^* (\beta_z g_m \alpha_n G_1^* + G_1^* G_z)}{C_1^* G_z + C_2^* G_1^*}} \tag{4.37}$$

$$\therefore Q_0 = \sqrt{\frac{(C_1 + C_x)(C_2 + C_z)(\beta_z g_m \alpha_n R_z + 1)}{(C_1 + C_x)(R_1 + R_n) + R_z (C_2 + C_z)}} \tag{4.38}$$

From the above equations, it can be concluded that if the parasitic resistances R_p and R_n values are much lower than the R_1 and R_2 then it can be seen that these parasitic resistances put negligibly small effect on ω_n and Q_0 and also the effect of the parasitic capacitances C_z and C_x is absorbed by C_2 and C_1 because parasitic capacitances C_z and C_x appear in shunt with externally connected grounded capacitances i.e. C_2 and C_1 therefore, parasitic capacitances C_z and C_x can also be neglected.

4.3.5 **Sensitivity analysis including Non-Idealities:**

There non-ideal sensitivities with respect to active and passive elements are found as:-

$$S_{\beta_v}^{\omega_n} = S_{R_p}^{\omega_n} = S_{\alpha_p}^{\omega_n} = S_{R_2}^{\omega_n} = S_{\beta_v}^{Q_0} = S_{R_p}^{Q_0} = S_{\alpha_p}^{Q_0} = S_{R_2}^{Q_0} = 0 \tag{4.39}$$

$$S_{C_1}^{\omega_n} = -\frac{1}{2}\frac{C_1}{C_1 + C_x}; S_{C_2}^{\omega_n} = -\frac{1}{2}\frac{C_2}{C_2 + C_z} \tag{4.40}$$

$$S_{Cz}^{\omega_n} = -\frac{1}{2}\frac{C_z}{C_2 + C_z}; S_{C_x}^{\omega_n} = -\frac{1}{2}\frac{C_x}{C_1 + C_x} \tag{4.41}$$

$$S_{R_1}^{\omega_n} = -\frac{1}{2}\frac{R_1}{R_1+R_n}\,;\, S_{R_n}^{\omega_n} = -\frac{1}{2}\frac{R_n}{R_1+R_n} \tag{4.42}$$

$$S_{R_z}^{\omega_n} = -\frac{1}{2}\frac{R_z}{(\beta_z g_m \alpha_n R_z + 1)} \tag{4.43}$$

$$S_{\beta_z}^{\omega_n} = S_{g_m}^{\omega_n} = S_{\alpha_n}^{\omega_n} = S_{\beta_z}^{Q_0} = S_{g_m}^{Q_0} = S_{\alpha_n}^{Q_0} = \frac{1}{2}\frac{\beta_z g_m \alpha_n}{(\beta_z g_m \alpha_n R_z + 1)} \tag{4.44}$$

$$S_{C_1}^{Q_0} = \frac{1}{2}\frac{C_1}{C_1+C_x}\frac{(R_1+R_n)(C_2+C_x)}{[(C_1+C_x)(R_1+R_n)+R_z(C_2+C_z)]} \tag{4.45}$$

$$S_{C_2}^{Q_0} = \frac{1}{2}\frac{C_2}{C_2+C_z}\frac{(R_1+R_n)(C_2+C_x)}{[(C_1+C_x)(R_1+R_n)+R_z(C_2+C_z)]} \tag{4.46}$$

$$S_{Cz}^{Q_0} = \frac{1}{2}\frac{C_z}{C_2+C_z}\frac{(R_1+R_n)(C_2+C_x)}{[(C_1+C_x)(R_1+R_n)+R_z(C_2+C_z)]} \tag{4.47}$$

$$S_{C_x}^{Q_0} = \frac{1}{2}\frac{C_x}{C_1+C_x}\frac{(R_1+R_n)(C_2+C_x)}{[(C_1+C_x)(R_1+R_n)+R_z(C_2+C_z)]} \tag{4.48}$$

$$S_{R_z}^{Q_0} = \frac{1}{2}\frac{R_z}{(\beta_z g_m \alpha_n R_z + 1)}\frac{\beta_z g_m \alpha_n (C_1+C_x)(R_1+R_n)-(C_2+C_z)}{[(C_1+C_x)(R_1+R_n)+R_z(C_2+C_z)]} \tag{4.48}$$

$$S_{R_1}^{Q_0} = -\frac{1}{2}\frac{R_1(C_1+C_x)}{[(C_1+C_x)(R_1+R_n)+R_z(C_2+C_z)]} \tag{4.49}$$

$$S_{R_n}^{Q_0} = -\frac{1}{2}\frac{R_n(C_1+C_x)}{[(C_1+C_x)(R_1+R_n)+R_z(C_2+C_z)]} \tag{4.50}$$

As observed from the above equations, the conclusion obtained is that all the active and the passive sensitivities are less than $1/2$ in magnitude for the new CD-DITA based CM-SIMO universal filter.

4.3.6 Simulation results of CD-DITA based CM-SIMO universal filter:-

To verify the working of the CD-DITA based biquad filter referring 4.13. The simulation is done using PSPICE software with 180nm process technology. The filter is designed for $f_0 = 7Mhz$ with $Q_0 = 1$ and for this C_1 and C_2 have been chosen as $5\,pF$. For $f_0 = 7Mhz$ using $C_1 = C_2 = 5\,pF$ the calculated value of $g_m = 221.236\,\mu A/V$ and R_1 and R_2 have been set to $1/g_m$

equals to $4.52k\Omega$. Theoretically the value of g_m is related to MOS process parameters and bias current by the relation given by equations 4.51and 4.52.

$$g_m = \frac{(g_{m13} + g_{m15})}{2} \text{ Or } g_m = \frac{(g_{m14} + g_{m16})}{2} \qquad (4.51)$$

Where g_{mi} is the transconductance of i[th] transistor which is defined by

$$g_{mi} = \sqrt{I_{bi}\mu_{n/p}C_{ox}\left[\frac{W}{L}\right]_i} \qquad (4.52)$$

If the values of parameters $\left(\frac{W}{L}\right)_n = \left(\frac{W}{L}\right)_p = 12$, $\mu_p = 112.51 cm^2/V\sec$, $\mu_n = 296.84 cm^2/V\sec$, $t_{ox} = 4.1\times10^{-9} m$ and $\varepsilon_{ox} = 3.9\varepsilon_0$ are put into equation 4.52, along with the required value of $g_m = 221.236\mu A/V$, then the bias currents required to design this filter turn out to be $I_{b3} = I_{b4} \approx 25\mu A$

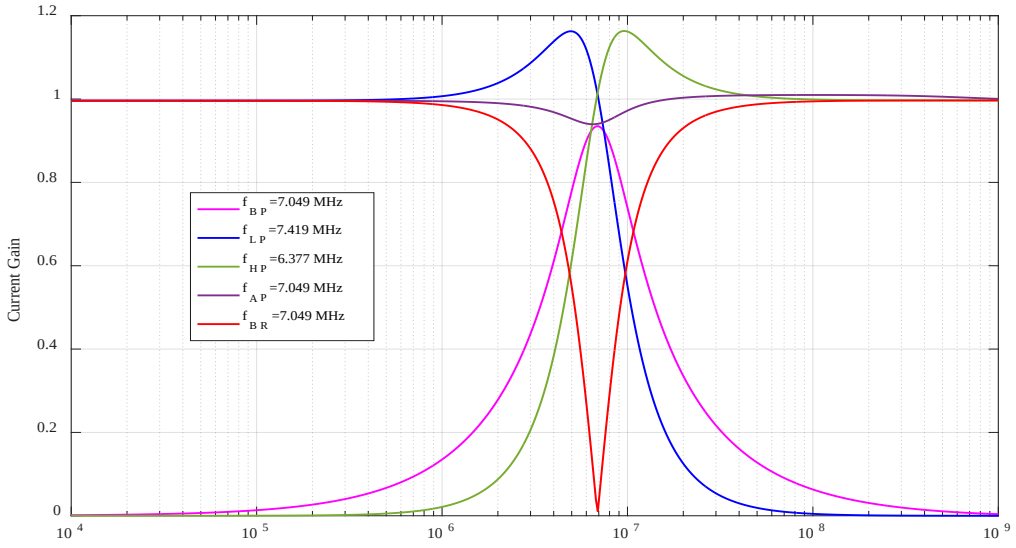
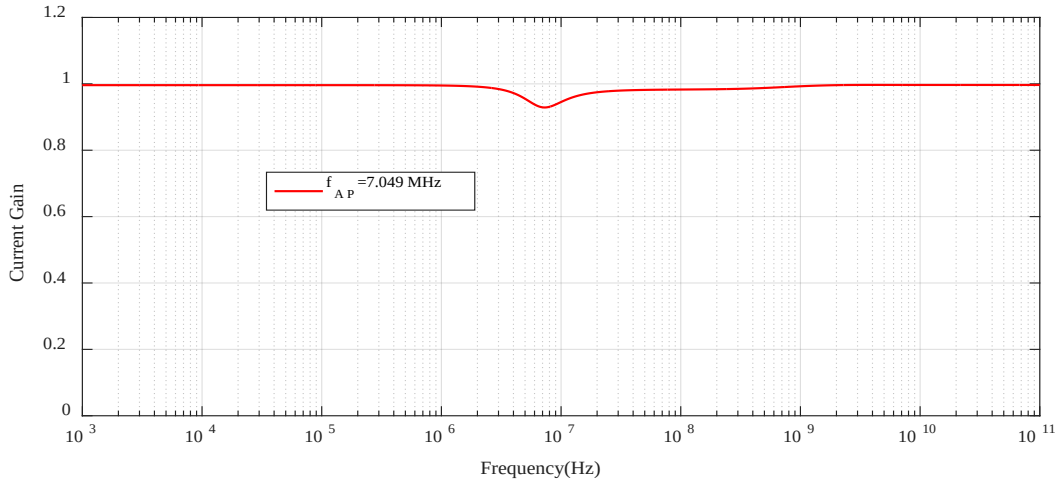
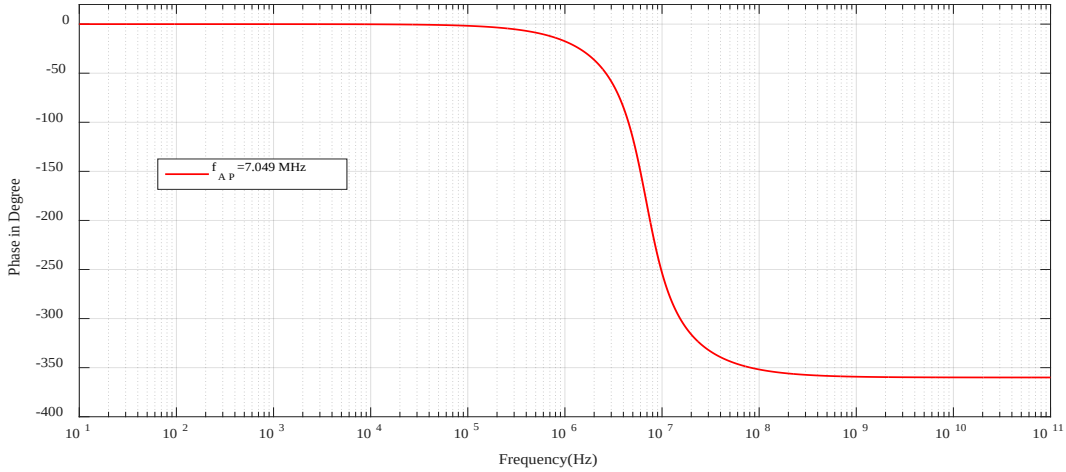


Fig. 4.18 Simulated filter responses of CD-DITA based CM-universal filter

Fig. 4.18 shows the responses of proposed filter: LPF, HPF, BPF, Notch and APF and Fig. 4.19 shows the APF magnitude and phase responses of proposed filter



(a)



(b)

Fig. 4.19 Simulated APF: (a) magnitude and (b) phase response CM Biquad filter

Simulated center frequency can be measured using phase response of APF by measuring frequency at phase $= -180^0$. The measured center frequency in phase response of APF is $f_0 = 7.049MHz$ which is close to theoretical frequency.

Chapter 5

Proposed Applications of CD-DITA

5.1 Proposed Grounded Inductor and its BPF implementation:

The importance of grounded and floating simulated inductors in the context of active network synthesis is well known [33]. The purpose of this work is to introduce new CD-DITA based lossless grounded inductor using single CD-DITA along with one resistor and one grounded capacitor and that too without requiring any matching condition.

5.1.1 The Proposed Configuration of Grounded Inductor:

The schematic symbol of the grounded inductor based on CD-DITA is shown in the below Fig.5.1. This model of CD-DITA based grounded inductor employs one grounded capacitor and one resistor along with single CD-DITA block. The input signal is applied at the p terminal.

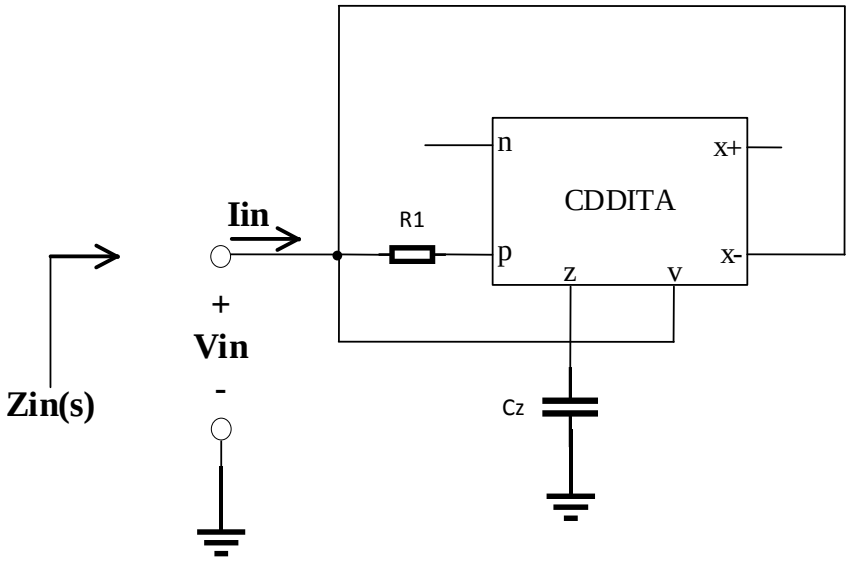


Fig. 5.1. Proposed Grounded Inductor Based on CD-DITA

Assuming ideal CD-DITA i.e. characterized by the following terminal equations:-

$$V_p = V_n = 0 \qquad (5.1)$$

$$I_v = 0 \tag{5.2}$$

$$I_z = I_p - I_n \tag{5.3}$$

$$I_{x+} = g_m\left(V_z - V_v\right) \tag{5.4}$$

$$I_{x-} = -g_m\left(V_z - V_v\right) \tag{5.5}$$

And hence the Equation matrix for Ideal CD-DITA can be given as following:-

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_x \\ I_v \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & \pm g_m & 0 & \mp g_m \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_z \\ V_x \\ V_v \end{bmatrix} \tag{5.6}$$

By solving the equations for the schematic symbol shown in Fig.5.1, the resulting equations verifying the grounded inductor simulation using CD-DITA can be given as:-

$$Zin(s) = \frac{Vin(s)}{Iin(s)} \tag{5.7}$$

$$Zin(s) = s\left(\frac{C_z R_1}{g_m}\right) \tag{5.8}$$

Thus, the simulated equivalent value of the grounded inductor from the above equation is given by:-

$$L_{eq} = \left(\frac{C_z R_1}{g_m}\right) \tag{5.9}$$

The performance of this proposed newly simulated grounded inductor has been evaluated by using PSPICE (version 9.1) simulations. A new FVF based CMOS implementation of the CD-DITA block shown in Fig. 5.2 that has been used to implement this grounded inductor and also has been used to find out the frequency response of the simulated grounded inductor.

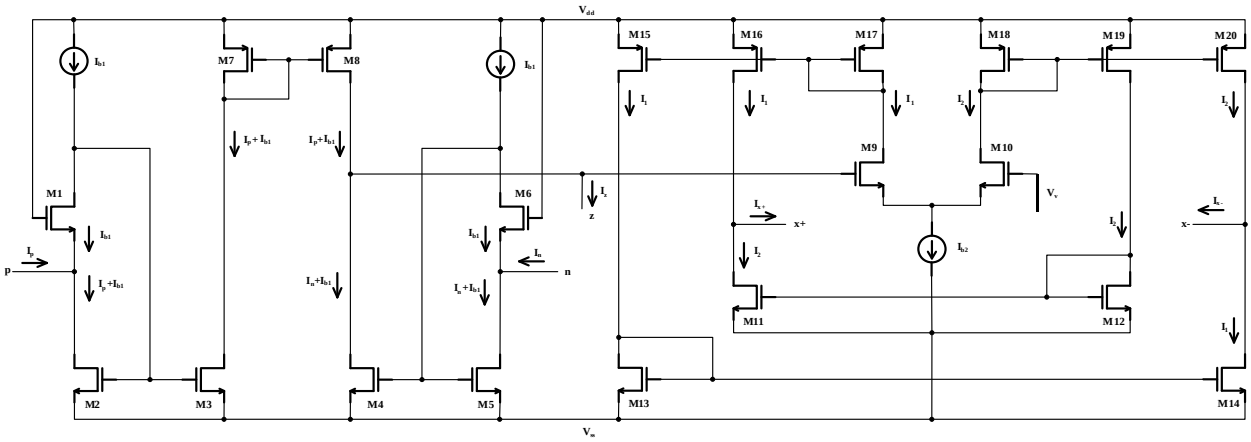


Fig. 5.2 CD-DITA based on FVF

The circuit in Fig. 5.1has been designed for inductance ofvalue $L = 10uH$. The calculated values of capacitor and resistor for simulating grounded inductor are $C_z = 0.793pF$, $R_1 = 3.55k\Omega$. The bias current $I_{b2} = 100uA$ and the corresponding value of $g_m = 281.791uA/V$ and the r supply. used is $\pm 1.2V$. As in Fig. 5.3., practical value of the grounded inductor $L_{eq} = 9.58uH$. It has been also observed that this simulated value of inductance remains constant upto $30.316MHz$.

The frequency response of the simulated grounded inductance can be presented in the Fig. 5.3.

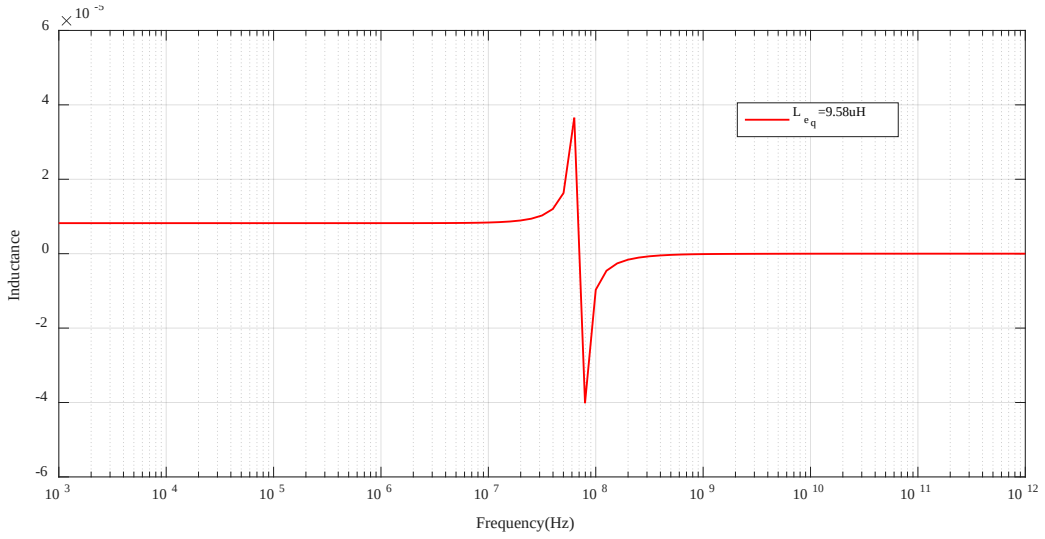


Fig. 5.3Frequency response of the Grounded Inductor Based on CD-DITA

5.1.2 Implementaion of BPF using grounded Inductor:

In Fig.5.4, presented simple R, L, C combination to represent a second order BPF

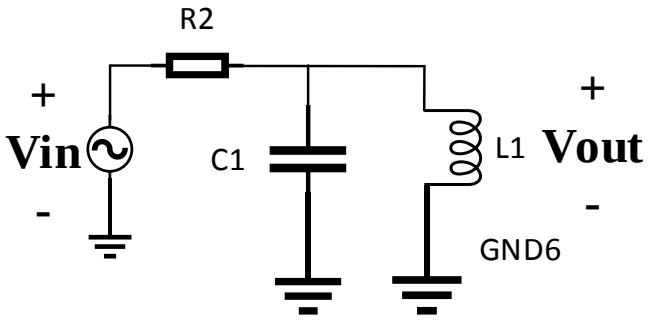


Fig. 5.4 BPF using Simple R, L, C

And the schematic symbol for implementing BPF based on proposed grounded inductor employing CD-DITA block has been in presented Fig. 5.5.

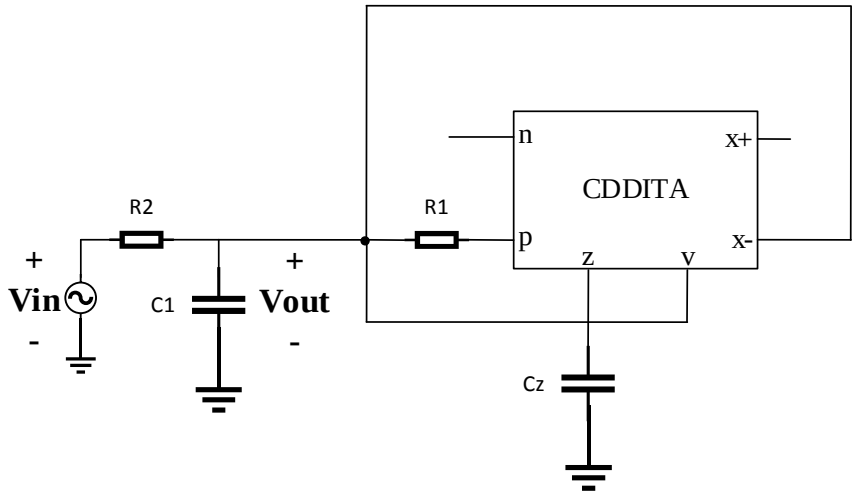


Fig. 5.5:- Schematic Symbol for Second Order BPF Using Proposed Grounded Inductor

And the equation that verify the functioning of the Fig.5.9 as a BPF can be given as:-

$$\frac{V_{out}}{V_{in}} = \frac{sC_1}{s^2 C_1 L_{eq} R_2 + sL_{eq} + R_2} \tag{5.10}$$

Where L_{eq} can be given as:-

$$L_{eq} = \left(\frac{C_z R_1}{g_m} \right) \tag{5.11}$$

The filter response of the second order BPF filter configuration for the grounded inductor has been simulated using PSPICE and the technology node that is used is 180nm. Fig.5.10 illustrates the practical result of the frequency response. The centre frequency of the presented BPF practically is $6.974MHz$. Thus, the BPF application response of the proposed new grounded inductance circuit based on the CD-DITA is given as :-

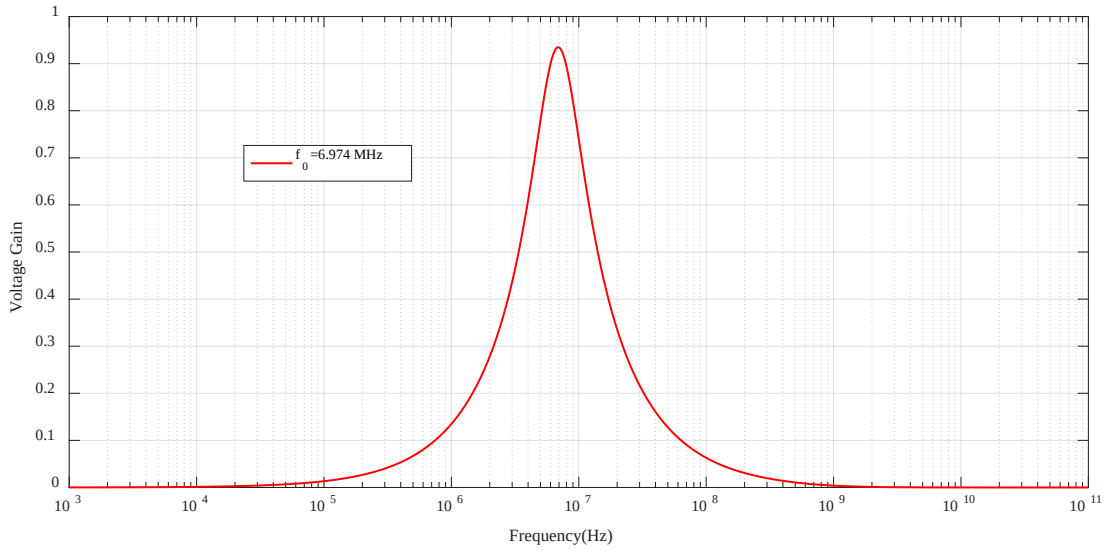


Fig.5.6Frequency Response of BPF using Grounded Inductor

5.2 Proposed MM filter using CD-DITA:

In this work, a new mixed-mode biquad filter topology with electronicaltunability has been introduced which employs single CD-DITA as ABB along with two capacitors and one resistor. This filter topology can realize LPF, BPF, HPF, BRF and APF responses in four possible modes namely CM, VM trans-impedance-mode (TIM) and trans-admittance-mode (TAM), by selecting appropriate combinations of inputs and condtions[55].

While implementing this filter topology with CD-DITA, the circuit do'nt require any inverted current or voltage input for realizing any filter response. This circuit also encourages the feature of electronic tunability of both the quality factor and natural frequency independently. This proposed filter topology has been simulated using PSPICE software and 180nm TSMC CMOS parameters.

5.2.1 PROPOSED MM FILTER CIRCUIT:-

The proposed MM filter topology employing single CD-DITA alond with two capacitors and one resistor has been shown in Fig 3. In the Fig presented the inputs applied and the outputs corresponding to those inputs have been realized using PSPICE.

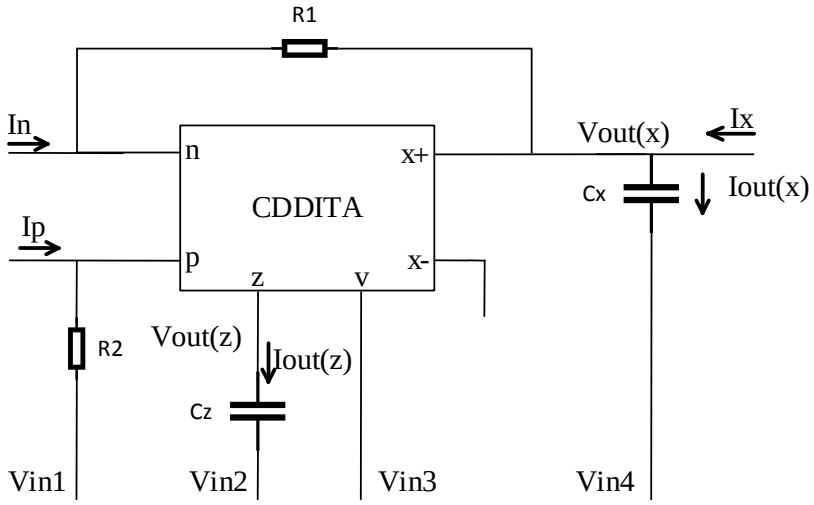


Fig. 5.6 Schematic Symbol for Proposed MM filter

Considering the ideal CD-DITA, the circuit analysis of the proposed filter will provide the following relations between outputs and inputs:-

(A) V_{out} taken as the voltage across capacitor i.e. $V_{C_2,out}$ and in that case the relation between the output voltage and various inputs can be stated as:-

$$V_{C_2,out} = \frac{K_1}{D} I_p + \frac{K_2}{D} I_n + \frac{K_3}{D} I_x + \frac{K_4}{D} V_{in1} + \frac{K_5}{D} V_{in2} + \frac{K_6}{D} V_{in3} + \frac{K_7}{D} V_{in4} \quad (5.12)$$

Where

$$D = s^2 C_1 C_2 + s G_1 C_1 + g_m G_2 \quad (5.11)$$

And the filter constants can be given as:-

$$K_1 = g_m(LPF)\ K_2 = -g_m(LPF)\ K_3 = sC_1(BPF) \qquad K_4 = g_m G_2(LPF) \qquad K_5 = g_m(LPF)$$

$$K_6 = -sC_1(BPF)\ \ K_7 = s^2 C_1 C_2(HPF) \quad (5.12)$$

(B) V_{out} taken as the voltage across Z terminal of CDDITA and in that case the relation between the output voltage and various inputs can be stated as:-

$$V_{Z,out} = \frac{K_1}{D} I_p + \frac{K_2}{D} I_n + \frac{K_3}{D} I_x + \frac{K_4}{D} V_{in1} + \frac{K_5}{D} V_{in2} + \frac{K_6}{D} V_{in3} + \frac{K_7}{D} V_{in4} \quad (5.13)$$

Where

$$K_1 = G_1 + sC_2 \;\; K_2 = -G_1 + sC_2 \;\; K_3 = -G_1(LPF) \;\; K_4 = G_1(G_1 + sC_2)$$

$$K_5 = sC_1(G_1 + sC_2) \qquad K_6 = -g_m G_1 \qquad K_7 = -sG_1C_2 \quad (5.14)$$

(C) I_{out} taken as the current across X terminal of CD-DITA and in that case the relation between the output current and various inputs can be stated as:-

$$I_{X,out} = \frac{K_1}{D} I_p + \frac{K_2}{D} I_n + \frac{K_3}{D} I_x + \frac{K_4}{D} V_{in1} + \frac{K_5}{D} V_{in2} + \frac{K_6}{D} V_{in3} + \frac{K_7}{D} V_{in4} \quad (5.15)$$

Where

$$K_1 = g_m(G_1 + sC_2) \;\; K_2 = -g_m(G_1 + sC_2) \;\; K_3 = -g_m G_1(LPF) \qquad K_4 = g_m G_2(G_1 + sC_2)$$

$$K_5 = sC_1 g_m(G_1 + sC_2) \qquad K_6 = -sC_1 g_m(G_1 + sC_2) \qquad K_7 = sG_1C_2(BPF) \quad (5.16)$$

(D) I_{out} taken as the current across Z terminal of CD-DITA and in that case the relation between the output current and various inputs can be stated as:-

$$I_{Z,out} = \frac{K_1}{D} I_p + \frac{K_2}{D} I_n + \frac{K_3}{D} I_x + \frac{K_4}{D} V_{in1} + \frac{K_5}{D} V_{in2} + \frac{K_6}{D} V_{in3} + \frac{K_7}{D} V_{in4} \quad (5.17)$$

Where

$$K_1 = sC_1(G_1 + sC_2) \;\; K_2 = -sC_1(G_1 + sC_2) \;\; K_3 = -sC_1G_1(BPF) \qquad K_4 = sG_1C_1(G_1 + sC_2)$$

$$K_5 = -sC_1 g_m G_1 \qquad K_6 = -sC_1 g_m G_1 \qquad K_7 = s^2 C_1C_2G_1(HPF) \quad (5.18)$$

(E) I_{out} taken as the current across C_2 of CD-DITA and in that case the relation between the output current and various inputs can be stated as:-

$$I_{C_2,out} = \frac{K_1}{D} I_p + \frac{K_2}{D} I_n + \frac{K_3}{D} I_x + \frac{K_4}{D} V_{in1} + \frac{K_5}{D} V_{in2} + \frac{K_6}{D} V_{in3} + \frac{K_7}{D} V_{in4} \qquad (5.19)$$

Where:-

$$K_1 = sg_m C_2(BPF) \quad K_2 = -sg_m C_2(BPF) \quad K_3 = s^2 C_1 C_2(HPF) \quad K_4 = sg_m C_2 G_2(BPF)$$

$$K_5 = s^2 C_1 C_2 g_m G_2(HPF) \quad K_6 = -s^2 C_1 C_2 g_m(HPF) \quad K_7 = s^2 C_1 C_2 + sC_2 g_m \qquad (5.20)$$

pole frequency or natural frequency(ω_0)of the filter and quality factor (Q_0) can be expressed as:-

$$\omega_0 = \sqrt{\frac{g_m}{R_1} \cdot \frac{1}{C_1 C_2}} \qquad (5.21)$$

$$Q_0 = \sqrt{g_m R_1 \cdot \frac{C_2}{C_1}} \qquad (5.22)$$

If $R_1 = R_2 = \frac{1}{g_m}$ then,

$$\omega_0 = g_m \sqrt{\frac{1}{C_1 C_2}} \qquad (5.23)$$

$$Q_0 = \sqrt{\frac{C_2}{C_1}} \qquad (5.24)$$

From the above equations, it can be concluded that ω_0 and Q_0 can be tuned independently.

5.2.2 **Sensitivity Analysis**:-

The sensitivity analysis, of natural frequency (ω_n) i.e. referringequation 5.23and of quality factor (Q_0) i.e. referring equation 5.24, due to the variations of all the passive and the active elements can be given by the following equations:

$$S_{g_m}^{\omega_n} = \frac{1}{2} \text{ and } S_{R_1}^{\omega_n} = S_{C_1}^{\omega_n} = S_{C_2}^{\omega_n} = -\frac{1}{2} \quad (5.25)$$

$$S_{g_m}^{Q_0} = S_{R_1}^{Q_0} = S_{C_2}^{Q_0} = \frac{1}{2} \text{ and } S_{C_1}^{Q_0} = -\frac{1}{2} \quad (5.26)$$

By observing the equations 5.25 and 5.26 the conclusion that can be made is that all the active and the passive of sensitivities of this circuit are half i.e. less than unity.

5.2.3 Effect of non-idealities of the CD-DITA on filter performance:

Referring to Fig. 4.17, Considering the non-idealities of CD-DITA into account the relationship between the output currents and input currents can be modified and For simplicity the filter responses , we can ignore the parasitic resistance present at the x terminal i.e. R_x because R_x is a very large value parasitic resistance i.e. typically its value is in mega ohms and also R_x appears in shunt or in parallel with $R_1 + R_n$ which has low value in comparison with R_x i.e. the typical value of $R_1 + R_n$ is in kilo ohms. Thus , the modified expression for all the responses can be given as:

(A) V_{out} taken as the voltage across capacitor i.e. $V_{C_2,out}$ and in that case the relation between the output voltage and various inputs can be stated as:-

$$V_{C_2,out} = \frac{K_1}{D} I_p + \frac{K_2}{D} I_n + \frac{K_3}{D} I_x + \frac{K_4}{D} V_{in1} + \frac{K_5}{D} V_{in2} + \frac{K_6}{D} V_{in3} + \frac{K_7}{D} V_{in4} \quad (5.27)$$

Where

$$D = s^2 C_1^* C_2^* + s\left(C_1^* G_z + C_2^* G_1^*\right) + \left(\beta_z g_m \alpha_n G_1^* + G_1^* G_z\right) \quad (5.28)$$

$$C_1^* = C_1 + C_x \text{ and } C_2^* = C_2 + C_z \qquad G_z = \frac{1}{R_z} \qquad G_x = \frac{1}{R_x} \qquad G_1^* = \frac{1}{R_1 + R_n} \; G_2^* = \frac{1}{R_2 + R_p}$$

And the filter constants can be given as:-

$$K_1 = g_m \beta_z \alpha_n G_1^* \; K_2 = -g_m \beta_z \alpha_n G_1^* \; K_3 = -(s\alpha_n G_1^* C_2^* + \alpha_n G_z G_1^*) \qquad K_4 = g_m \beta_z \alpha_n G_1^* G_2^*$$

$$K_5 = g_m \beta_z \alpha_n G_1^* \; K_6 = -(s\alpha_n G_1^* C_1^* + \alpha_n G_z G_1^*) \qquad K_7 = s^2 C_1^* C_2^* + s G_z C_1^* \quad (5.29)$$

(B) V_{out} taken as the voltage across Z terminal of CD-DITA and in that case the relation between the output voltage and various inputs can be stated as:-

$$V_{Z,out} = \frac{K_1}{D} I_p + \frac{K_2}{D} I_n + \frac{K_3}{D} I_x + \frac{K_4}{D} V_{in1} + \frac{K_5}{D} V_{in2} + \frac{K_6}{D} V_{in3} + \frac{K_7}{D} V_{in4} \quad (5.30)$$

Where

$$K_1 = G_1^* + s\alpha_n G_1^* C_2^* + \alpha_n G_z G_1^* \quad K_2 = -(G_1^* + s\alpha_n G_1^* C_2^* + \alpha_n G_z G_1^*) \quad K_3 = -G_1^*$$
$$K_4 = G_1^*(G_1^* + s\alpha_n G_1^* C_2^* + \alpha_n G_z G_1^*) \qquad K_5 = (s\alpha_n G_1^* C_2^* + \alpha_n G_z G_1^*)$$
$$K_6 = -g_m \beta_z \alpha_n G_1^* \qquad K_7 = -(s\alpha_n G_1^* C_2^* + \alpha_n G_z G_1^*) \quad (5.31)$$

(C) I_{out} taken as the current across X terminal of CD-DITA and in that case the relation between the output current and various inputs can be stated as:-

$$I_{X,out} = \frac{K_1}{D} I_p + \frac{K_2}{D} I_n + \frac{K_3}{D} I_x + \frac{K_4}{D} V_{in1} + \frac{K_5}{D} V_{in2} + \frac{K_6}{D} V_{in3} + \frac{K_7}{D} V_{in4} \quad (5.32)$$

Where

$$K_1 = g_m \beta_z \alpha_n (G_1^* + s\alpha_n G_1^* C_2^* + \alpha_n G_z G_1^*) \quad K_2 = -g_m \beta_z \alpha_n (G_1^* + s\alpha_n G_1^* C_2^* + \alpha_n G_z G_1^*)$$
$$K_3 = -g_m \beta_z \alpha_n G_1^* \quad K_4 = g_m \beta_z \alpha_n G_2^* (G_1^* + s\alpha_n G_1^* C_2^* + \alpha_n G_z G_1^*) \quad K_5 = sC_1 g_m \beta_z \alpha_n (G_1 + sC_2)$$
$$K_6 = -sC_1 g_m \beta_z \alpha_n (G_1^* + s\alpha_n G_1^* C_2^* + \alpha_n G_z G_1^*) \qquad K_7 = s\alpha_n G_1^* C_2^* + \alpha_n G_z G_1^* \quad (5.33)$$

(D) I_{out} taken as the current across Z terminal of CD-DITA and in that case the relation between the output current and various inputs can be stated as:-

$$I_{Z,out} = \frac{K_1}{D} I_p + \frac{K_2}{D} I_n + \frac{K_3}{D} I_x + \frac{K_4}{D} V_{in1} + \frac{K_5}{D} V_{in2} + \frac{K_6}{D} V_{in3} + \frac{K_7}{D} V_{in4} \quad (5.34)$$

Where

$$K_1 = sC_1(G_1^* + s\alpha_n G_1^* C_2^* + \alpha_n G_z G_1^*)\ K_2 = -(s\alpha_n G_1^* C_1^* + \alpha_n G_z G_1^*)(G_1^* + s\alpha_n G_1^* C_2^* + \alpha_n G_z G_1^*)$$
$$K_3 = -(s\alpha_n G_1^* C_2^* + \alpha_n G_z G_1^*)\ \ K_4 = (s\alpha_n G_1^* C_1^* + \alpha_n G_z G_1^*)(G_1^* + s\alpha_n G_1^* C_2^* + \alpha_n G_z G_1^*)$$
$$K_5 = -sC_1 g_m \beta_z \alpha_n G_1^* G_1\ K_6 = -sC_1 g_m \beta_z \alpha_n G_1^* G_1\ K_7 = (s^2 C_1^* C_2^* + sG_z C_1^*)G_1^* \quad (5.35)$$

(E) I_{out} taken as the current acrossC_2 of CD-DITA and in that case the relation between the output current and various inputs can be stated as:-

$$I_{C_2,out} = \frac{K_1}{D} I_p + \frac{K_2}{D} I_n + \frac{K_3}{D} I_x + \frac{K_4}{D} V_{in1} + \frac{K_5}{D} V_{in2} + \frac{K_6}{D} V_{in3} + \frac{K_7}{D} V_{in4} \quad (5.36)$$

Where:-

$$K_1 = sg_m \beta_z \alpha_n G_1^* C_2\ K_2 = -sg_m \beta_z \alpha_n G_1^* C_2 (BPF) \qquad K_3 = s^2 C_1^* C_2^* + sG_z C_1^*$$
$$K_4 = sg_m \beta_z \alpha_n G_1^* C_2^* G_2^* \qquad K_5 = (s^2 C_1^* C_2^* + sG_z C_1^*) g_m \beta_z \alpha_n G_1^* G_2 (HPF)$$
$$K_6 = -(s^2 C_1^* C_2^* + sG_z C_1^*) g_m \beta_z \alpha_n G_1^*\ \ K_7 = s^2 C_1^* C_2^* + sG_z C_1^* + sC_2 g_m \beta_z \alpha_n G_1^* \quad (5.37)$$

The natural frequency ω_n and the quality factor Q_0 can be expressed as the following equations:

$$\omega_n = \sqrt{\frac{\beta_z g_m \alpha_n G_1^* + G_1^* G_z}{C_1^* C_2^*}} \quad (5.38)$$

$$\therefore \omega_n = \sqrt{\frac{\beta_z g_m \alpha_n R_z + 1}{(C_1 + C_x)(C_2 + C_z) R_z (R_1 + R_n)}} \quad (5.39)$$

$$Q_0 = \sqrt{\frac{C_1^* C_2^* (\beta_z g_m \alpha_n G_1^* + G_1^* G_z)}{C_1^* G_z + C_2^* G_1^*}} \quad (5.40)$$

$$\therefore Q_0 = \sqrt{\frac{(C_1 + C_x)(C_2 + C_z)(\beta_z g_m \alpha_n R_z + 1)}{(C_1 + C_x)(R_1 + R_n) + R_z (C_2 + C_z)}} \quad (5.41)$$

From the above equations, it can be concluded that if the parasitic resistances R_p and R_n values are much lower than the R_1 and R_2 then it can be seen that these parasitic resistances put negligibly small effect on ω_n and Q_0 and also the effect of the parasitic capacitances C_z and C_x is

absorbed by C_2 and C_1 because parasitic capacitances C_z and C_x appear in shunt with externally connected grounded capacitances i.e. C_2 and C_1 therefore, parasitic capacitances C_z and C_x can also be neglected.

5.2.4 **Sensitivity analysis including Non-Idealities:**

There non-ideal sensitivities with respect to active and passive elements are found as:-

$$S_{\beta_v}^{\omega_n} = S_{R_p}^{\omega_n} = S_{\alpha_p}^{\omega_n} = S_{R_2}^{\omega_n} = S_{\beta_v}^{Q_0} = S_{R_p}^{Q_0} = S_{\alpha_p}^{Q_0} = S_{R_2}^{Q_0} = 0 \tag{5.42}$$

$$S_{C_1}^{\omega_n} = -\frac{1}{2}\frac{C_1}{C_1 + C_x}; S_{C_2}^{\omega_n} = -\frac{1}{2}\frac{C_2}{C_2 + C_z} \tag{5.43}$$

$$S_{Cz}^{\omega_n} = -\frac{1}{2}\frac{C_z}{C_2 + C_z}; S_{C_x}^{\omega_n} = -\frac{1}{2}\frac{C_x}{C_1 + C_x} \tag{5.44}$$

$$S_{R_1}^{\omega_n} = -\frac{1}{2}\frac{R_1}{R_1 + R_n}; S_{R_n}^{\omega_n} = -\frac{1}{2}\frac{R_n}{R_1 + R_n} \tag{5.45}$$

$$S_{R_z}^{\omega_n} = -\frac{1}{2}\frac{R_z}{\left(\beta_z g_m \alpha_n R_z + 1\right)} \tag{5.46}$$

$$S_{\beta_z}^{\omega_n} = S_{g_m}^{\omega_n} = S_{\alpha_n}^{\omega_n} = S_{\beta_z}^{Q_0} = S_{g_m}^{Q_0} = S_{\alpha_n}^{Q_0} = \frac{1}{2}\frac{\beta_z g_m \alpha_n}{\left(\beta_z g_m \alpha_n R_z + 1\right)} \tag{5.47}$$

$$S_{C_1}^{Q_0} = \frac{1}{2}\frac{C_1}{C_1 + C_x}\frac{\left(R_1 + R_n\right)\left(C_2 + C_x\right)}{\left[\left(C_1 + C_x\right)\left(R_1 + R_n\right) + R_z\left(C_2 + C_z\right)\right]} \tag{5.48}$$

$$S_{C_2}^{Q_0} = \frac{1}{2}\frac{C_2}{C_2 + C_z}\frac{\left(R_1 + R_n\right)\left(C_2 + C_x\right)}{\left[\left(C_1 + C_x\right)\left(R_1 + R_n\right) + R_z\left(C_2 + C_z\right)\right]} \tag{5.49}$$

$$S_{Cz}^{Q_0} = \frac{1}{2}\frac{C_z}{C_2 + C_z}\frac{\left(R_1 + R_n\right)\left(C_2 + C_x\right)}{\left[\left(C_1 + C_x\right)\left(R_1 + R_n\right) + R_z\left(C_2 + C_z\right)\right]} \tag{5.50}$$

$$S_{C_x}^{Q_0} = \frac{1}{2}\frac{C_x}{C_1 + C_x}\frac{\left(R_1 + R_n\right)\left(C_2 + C_x\right)}{\left[\left(C_1 + C_x\right)\left(R_1 + R_n\right) + R_z\left(C_2 + C_z\right)\right]} \tag{5.51}$$

$$S_{R_z}^{Q_0} = \frac{1}{2}\frac{R_z}{\left(\beta_z g_m \alpha_n R_z + 1\right)}\frac{\beta_z g_m \alpha_n \left(C_1 + C_x\right)\left(R_1 + R_n\right) - \left(C_2 + C_z\right)}{\left[\left(C_1 + C_x\right)\left(R_1 + R_n\right) + R_z\left(C_2 + C_z\right)\right]} \tag{5.52}$$

$$S_{R_1}^{Q_0} = -\frac{1}{2}\frac{R_1\left(C_1 + C_x\right)}{\left[\left(C_1 + C_x\right)\left(R_1 + R_n\right) + R_z\left(C_2 + C_z\right)\right]} \tag{5.53}$$

$$S_{R_n}^{Q_0} = -\frac{1}{2}\frac{R_n\left(C_1 + C_x\right)}{\left[\left(C_1 + C_x\right)\left(R_1 + R_n\right) + R_z\left(C_2 + C_z\right)\right]} \tag{5.54}$$

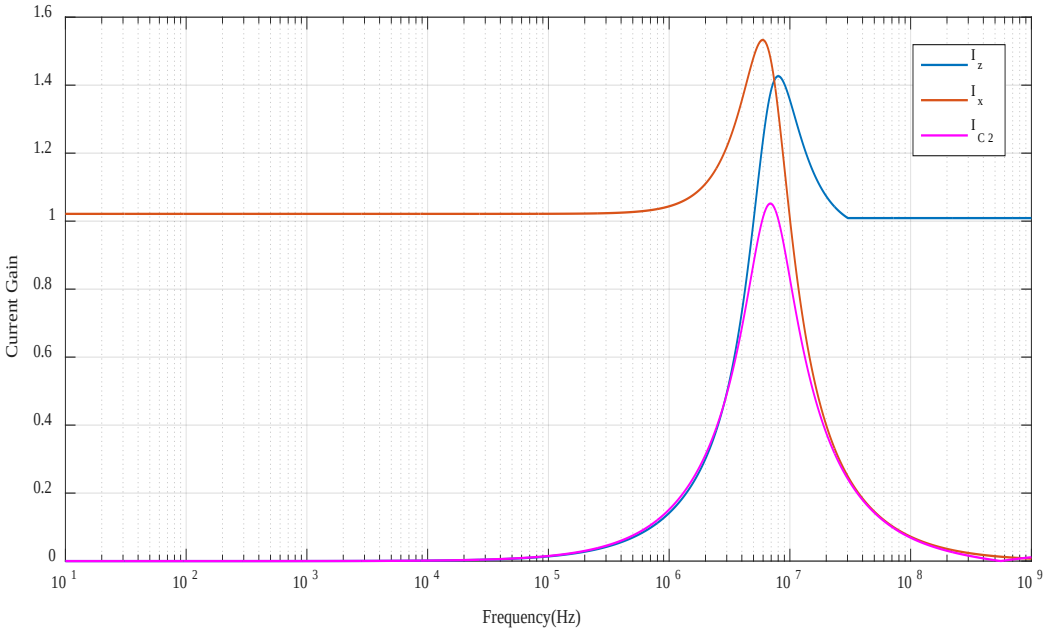
As observed from the above equations, the conclusion obtained is that all the active and the passive sensitivities are less than $1/2$ in magnitude for the new CD-DITA based CM-SIMO universal filter.

5.2.5 **Simulation results:**

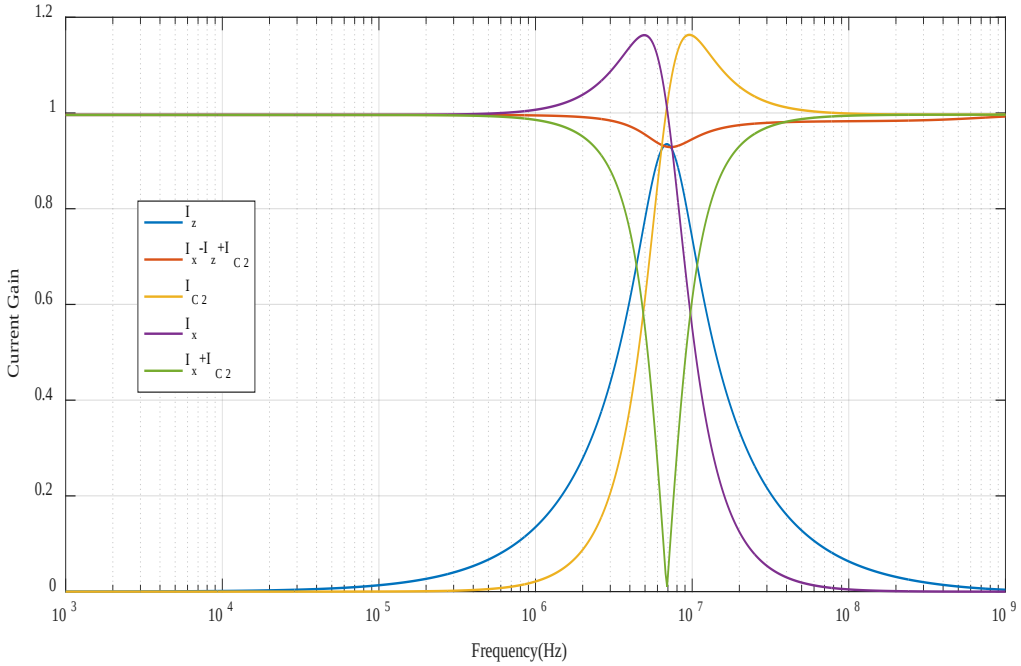
The circuit has been designed to achieve the frequency of $f_0 = \frac{\omega_0}{2\pi} = 7MHz$ and $Q_0 = 1$ and to achieve this frequency the components values selected are $R_1 = R_2 = 4.52k\Omega$ and $C_1 = C_2 = 5pF$, the biasing current used to bias the DO-OTA section of the CD-DITA section are selected as $I_{b1} = I_{b2} = 25uA$, and supply rails are $V_{DD} = \pm .9V$.

The linear responses of various filter response for different inputs have been shown as

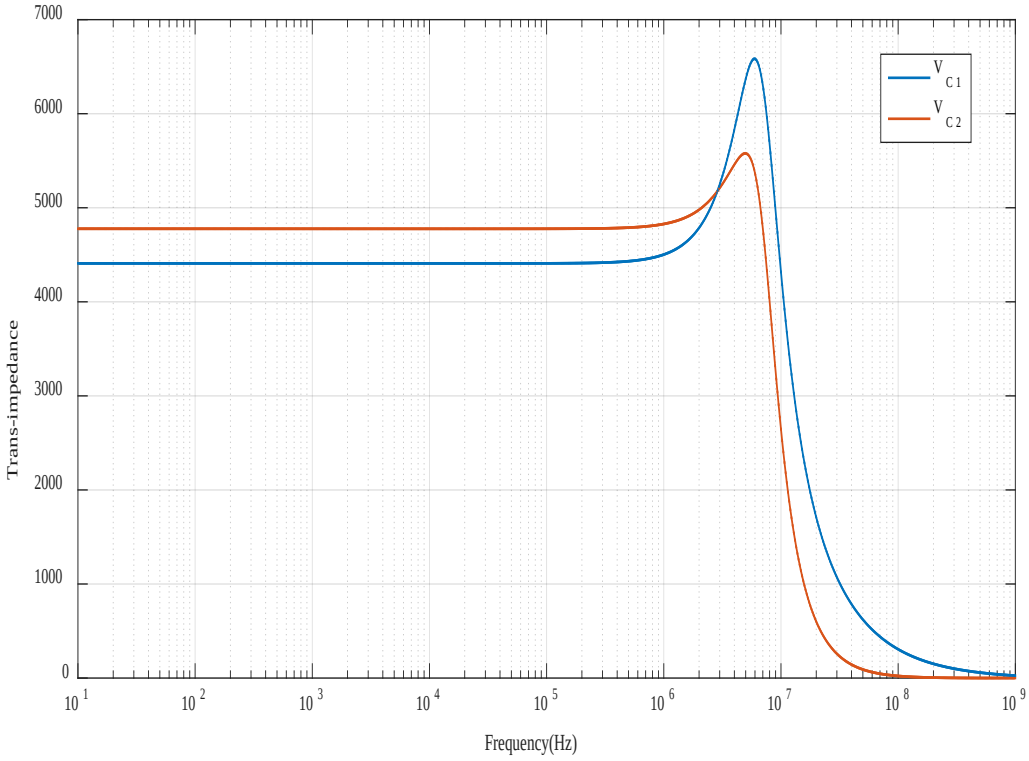
1. When current input is applied at the p terminal i.e. I_p then the output responses are presented in Fig:5.8



(A)



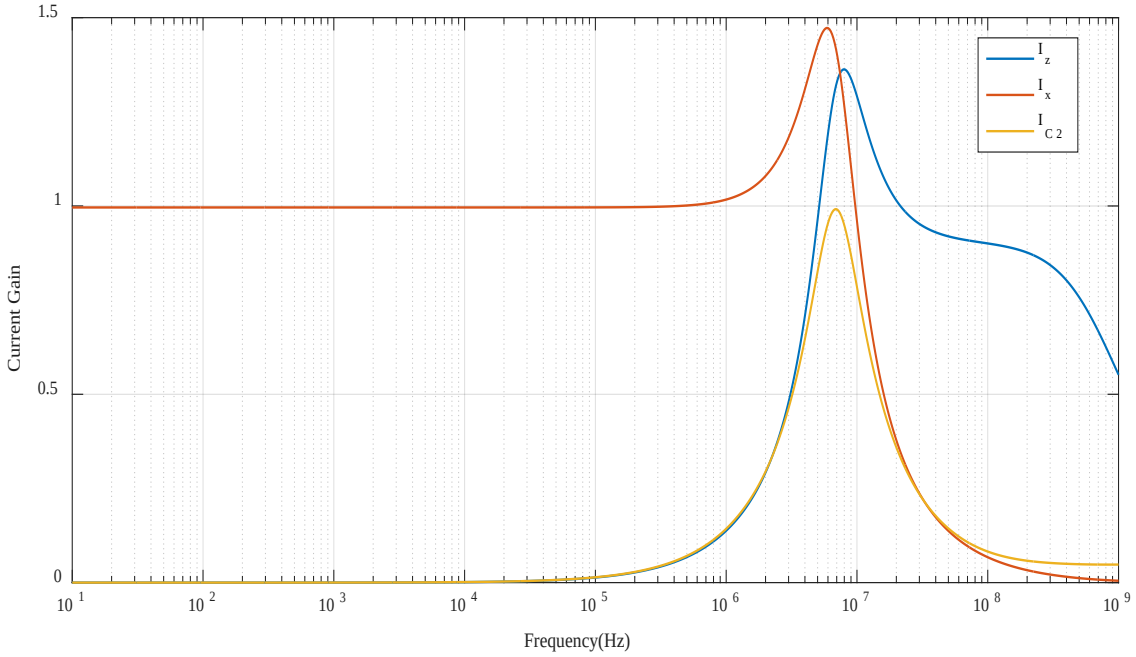
(B)



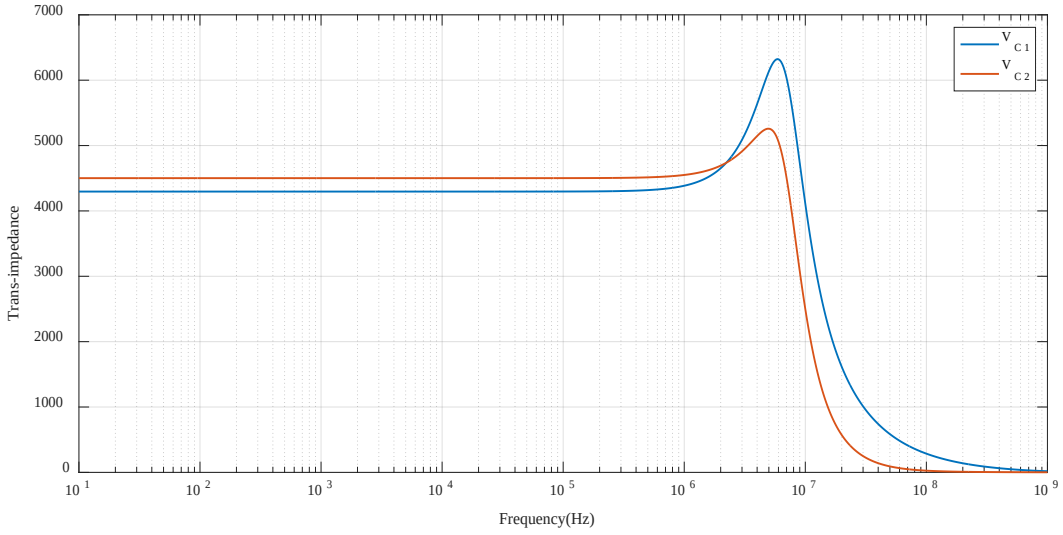
(C)

Fig:5.8 Responses for current input at p terminal

2. When current input is applied at the n terminal i.e. I_n then the output responses arepresented in Fig:5.9



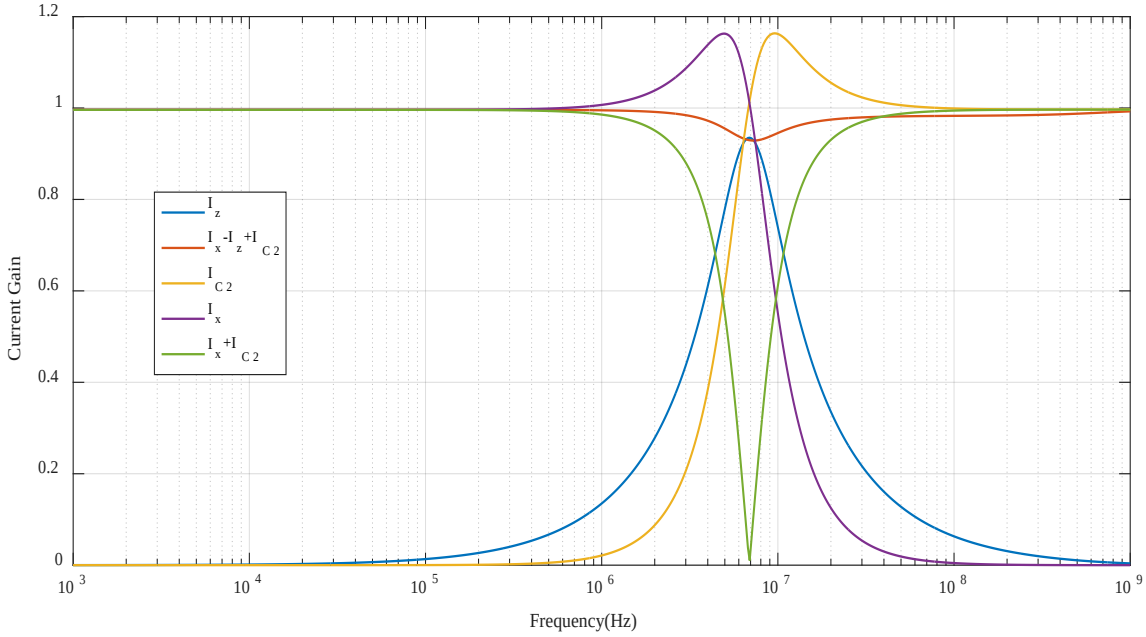
(A)



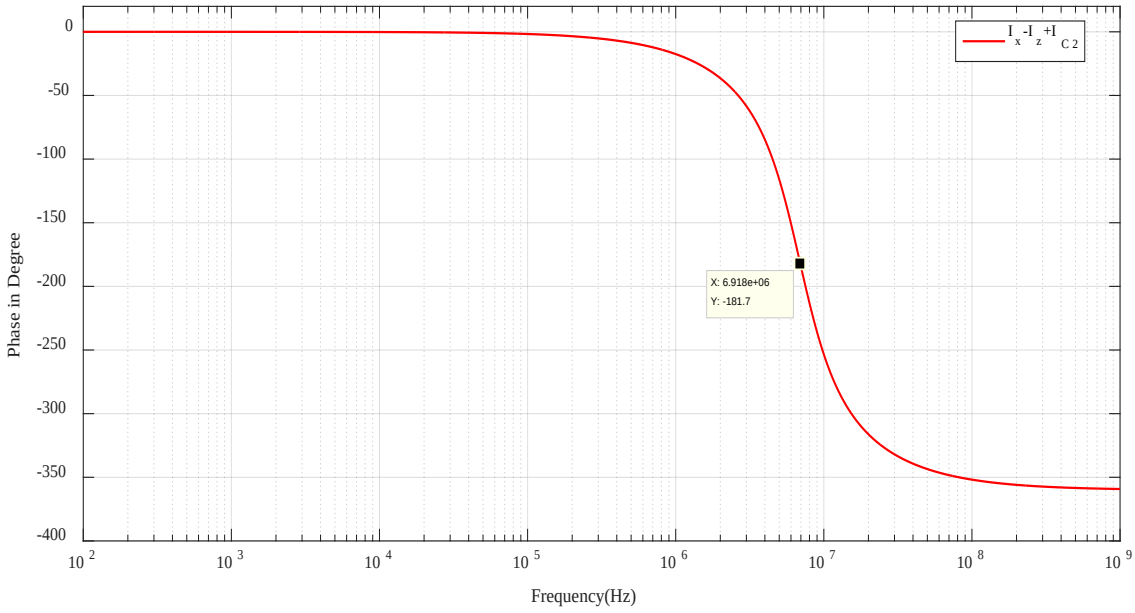
(B)

Fig:5.9 Responses for current input at n terminal

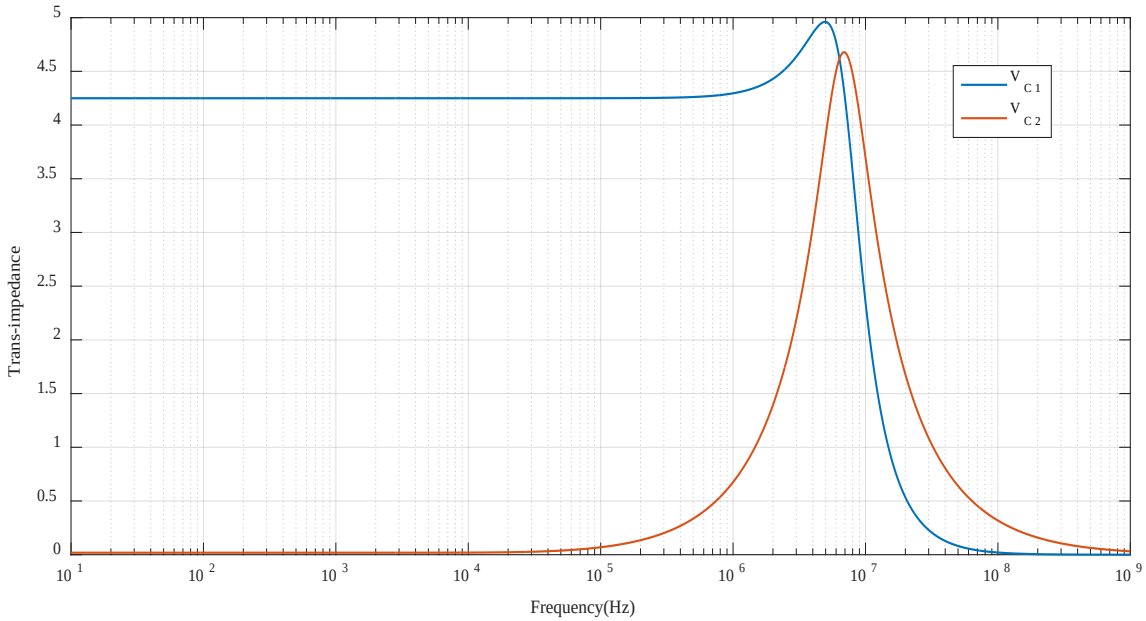
3. When current input is applied at the X terminal i.e. I_X then the output responses are presented in Fig: 5.10



(A)



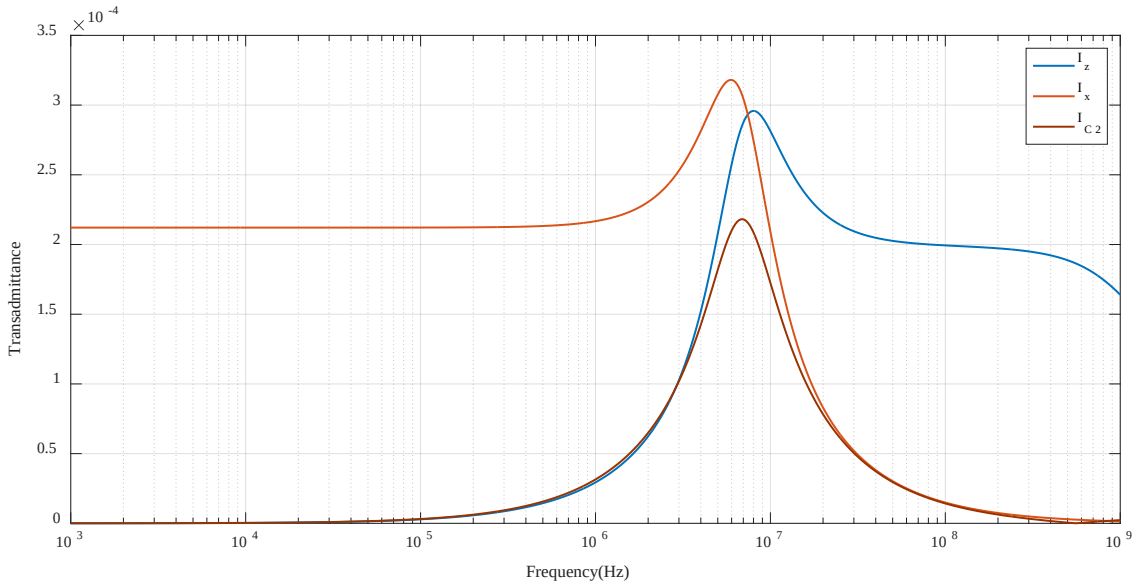
(B)



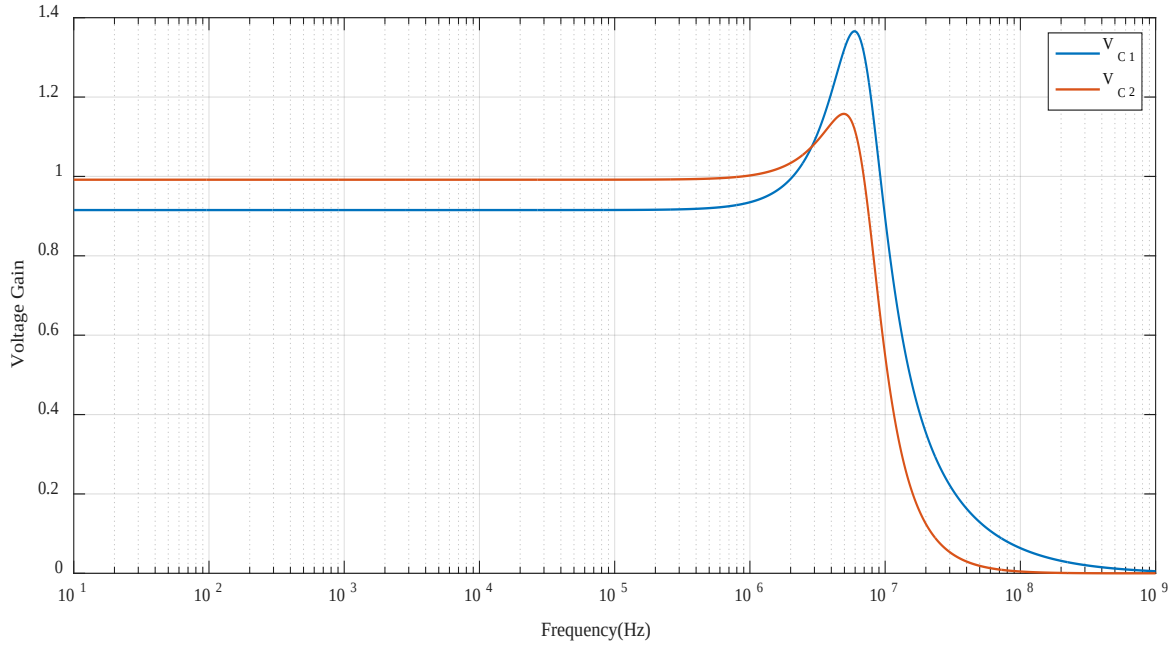
(C)

Fig: 5.10 Responses for current input at X terminal

4. When voltage input is applied at the p terminal through resistor R_1 i.e. $V_p = V_{in1}$ then the output responses are presented in Fig: 5.11



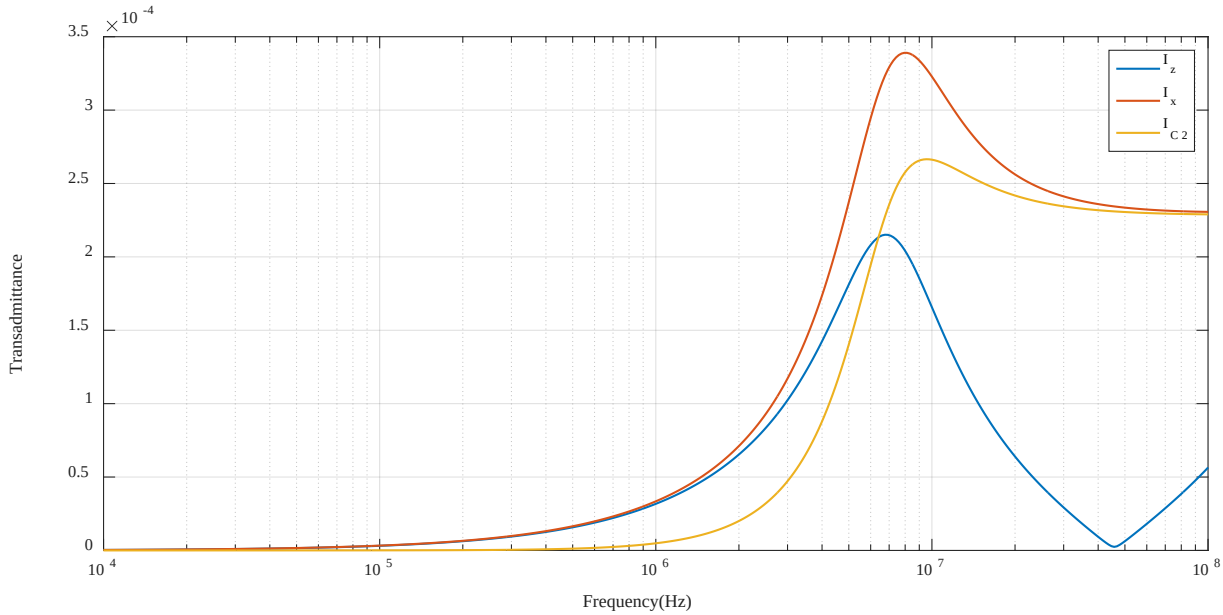
(A)



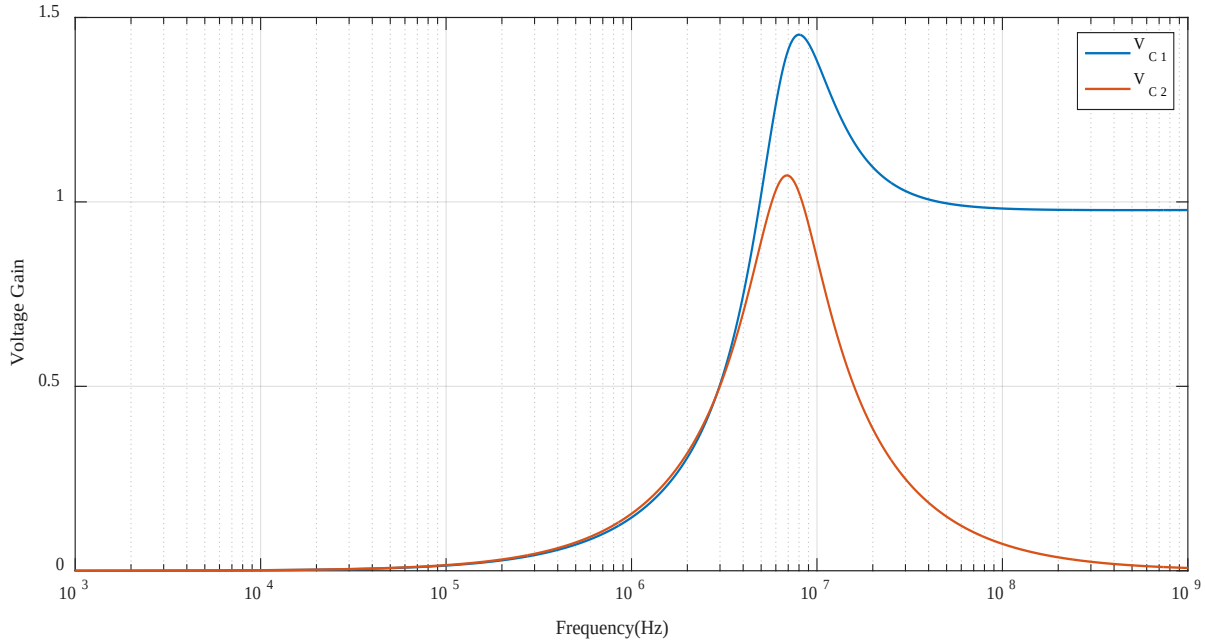
(B)

Fig: 5.11 Responses for voltage input $V_p = V_{in1}$

5. When voltage input is applied at the C_1 connected at Z terminal i.e. V_{in2} then the output responses are presented in Fig: 5.12



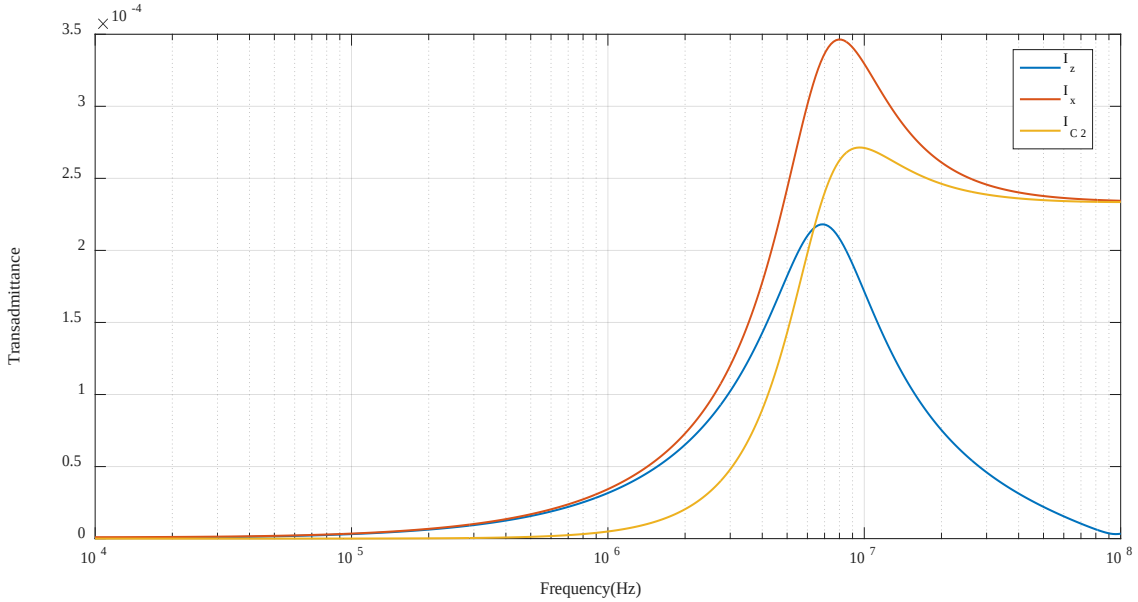
(A)



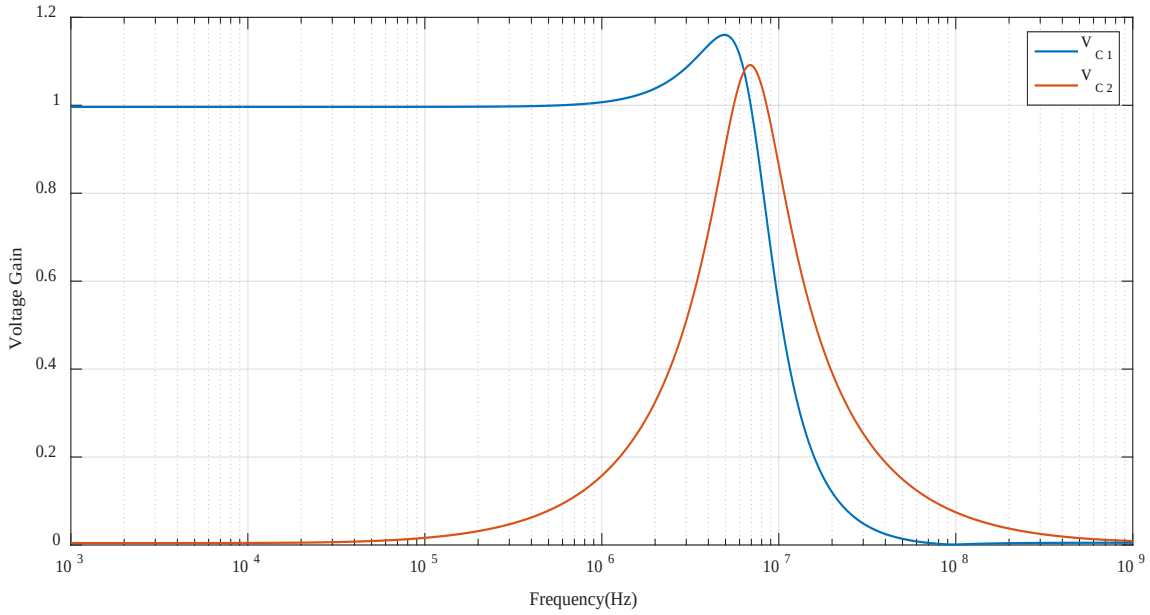
(B)

Fig: 5.12 Responses for voltage input V_{in2}

6. When voltage input is applied at the V terminal i.e. $V_V = V_{in3}$ then the output responses are presented in Fig: 5.13



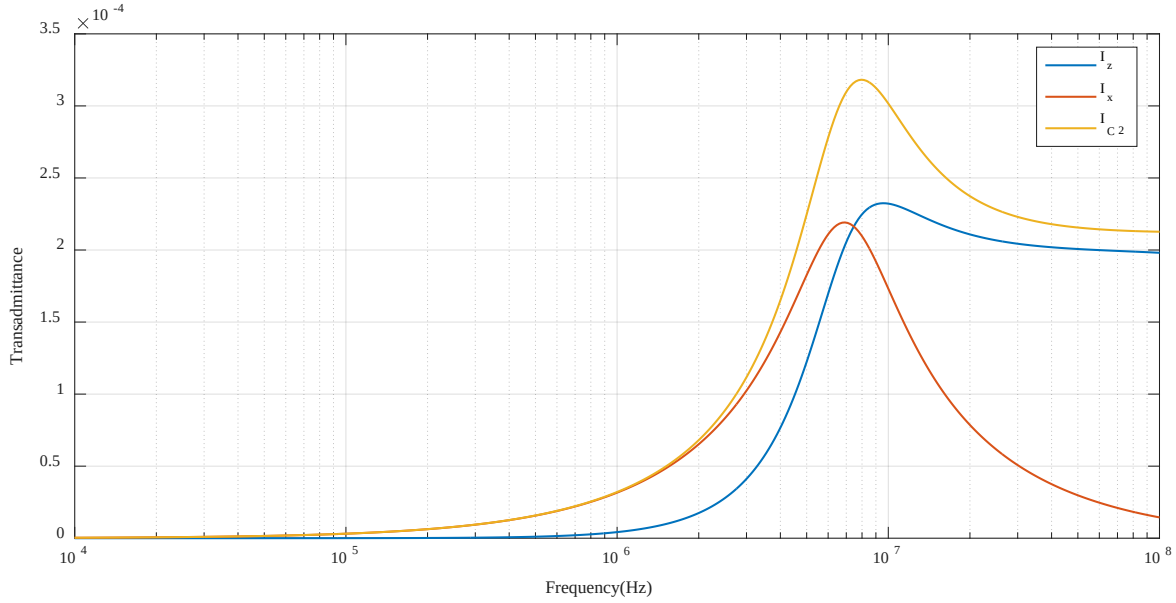
(A)



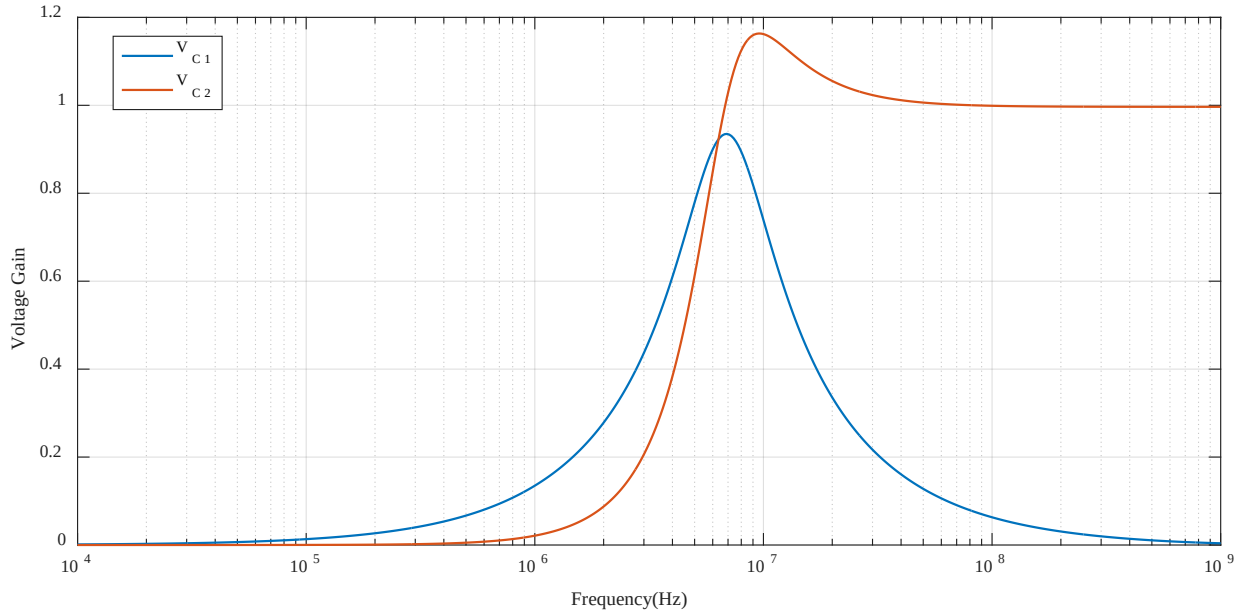
(B)

Fig: 5.13 Responses for voltage input $V_V = V_{in3}$

7. When voltage input is applied at the C_2 externally connected at X terminal i.e. V_{in4} then the output responses are presented in Fig: 5.14



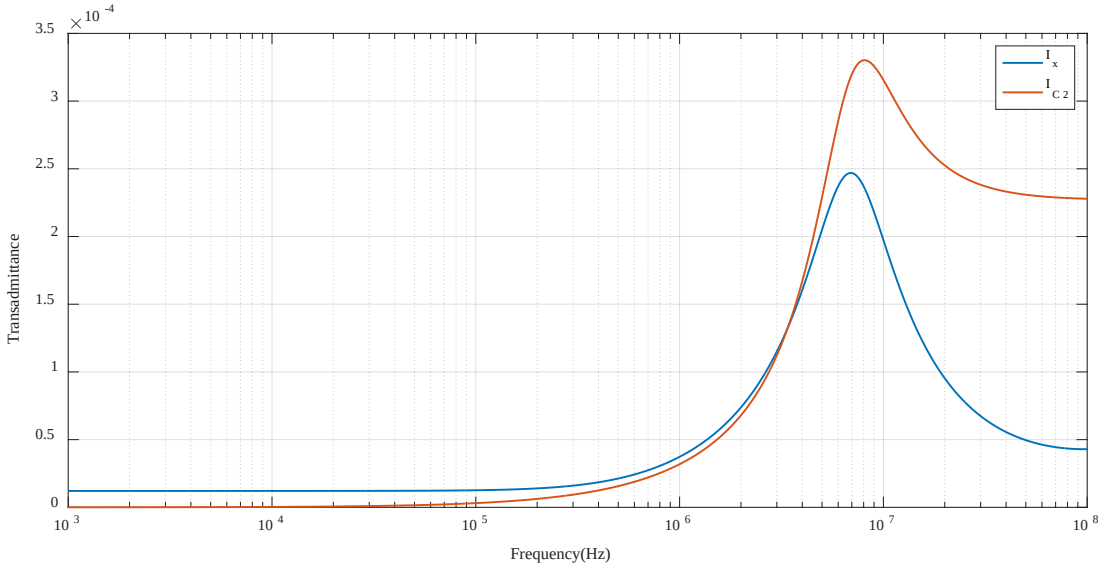
(A)



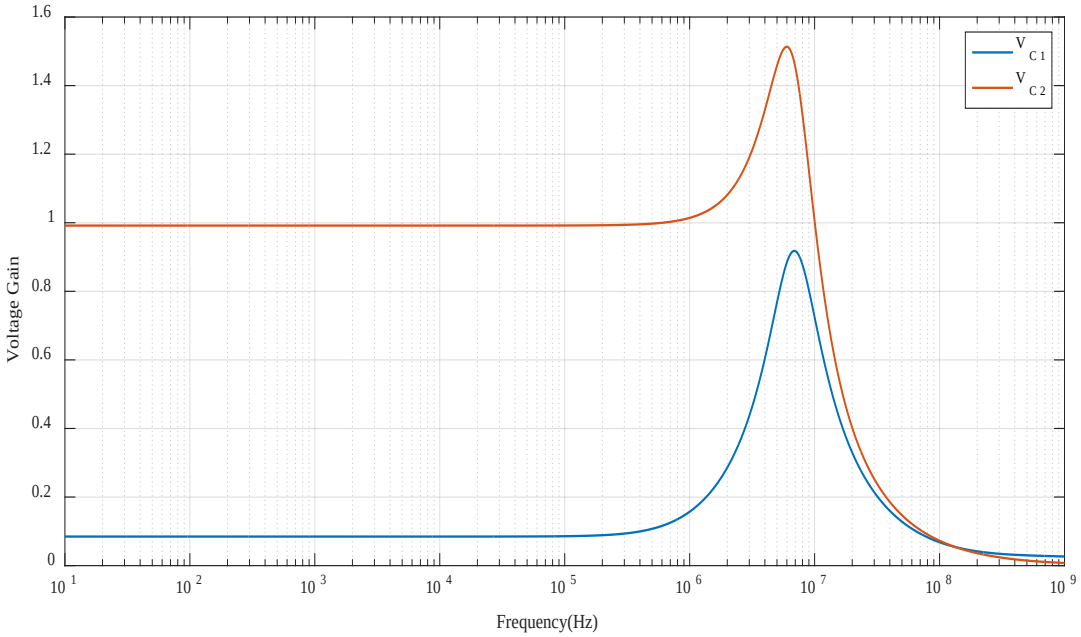
(B)

Fig: 5.14 Responses for voltage input V_{in4}

8. Combination of voltage input signals have been applied i.e. $V_{in1} + V_{in2}$ then the output responses are presented in Fig: 5.15



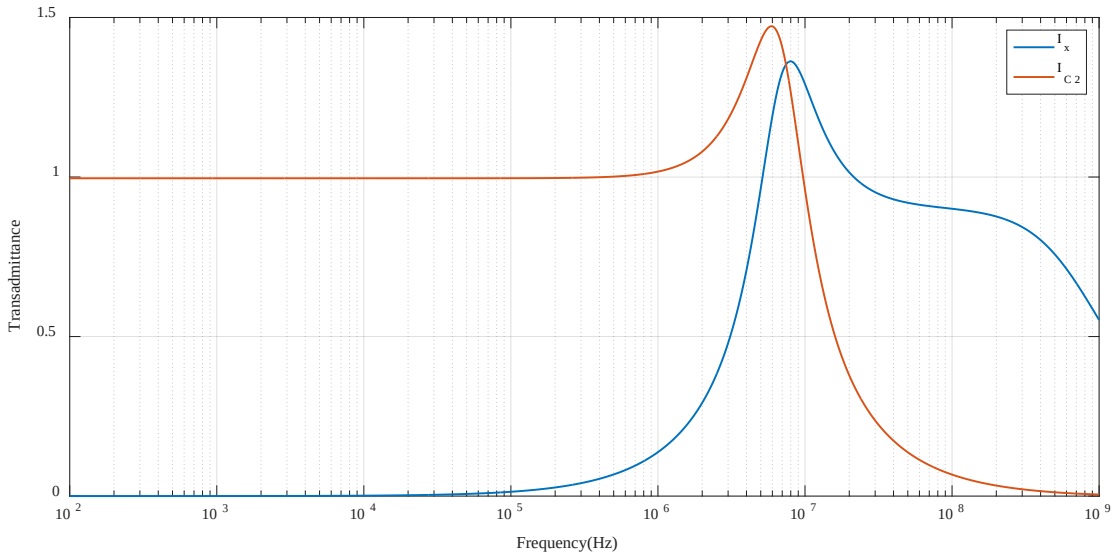
(A)



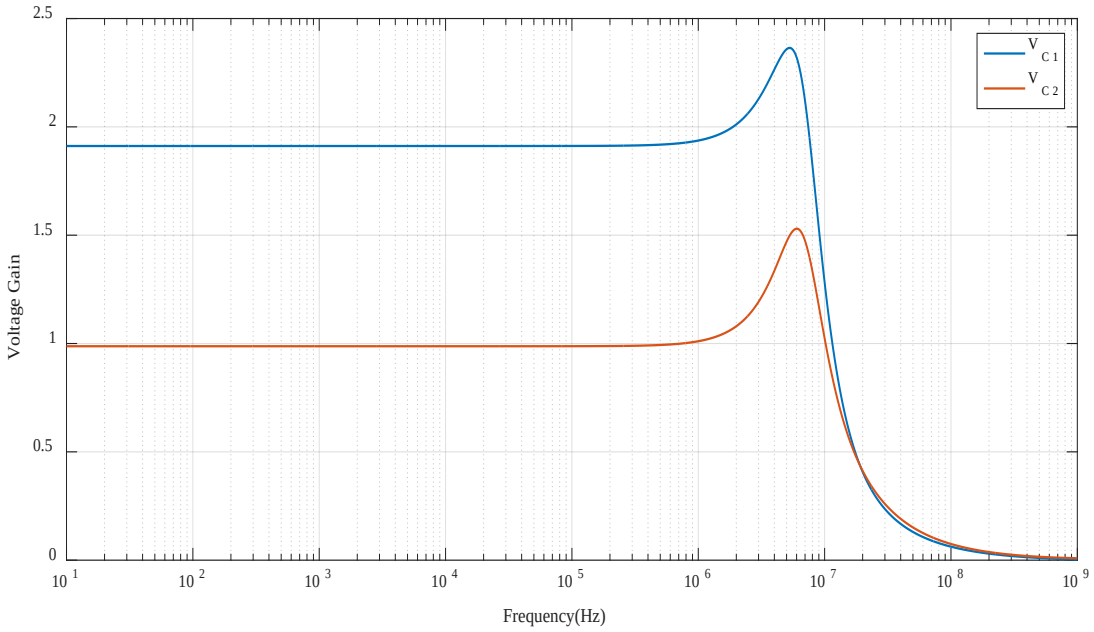
(B)

Fig: 5.15 Responses for voltage input $V_{in1}+V_{in2}$

9. Combination of voltage input signals have been applied i.e. $V_{in1}+V_{in3}$ then the output responses are presented in Fig: 5.16



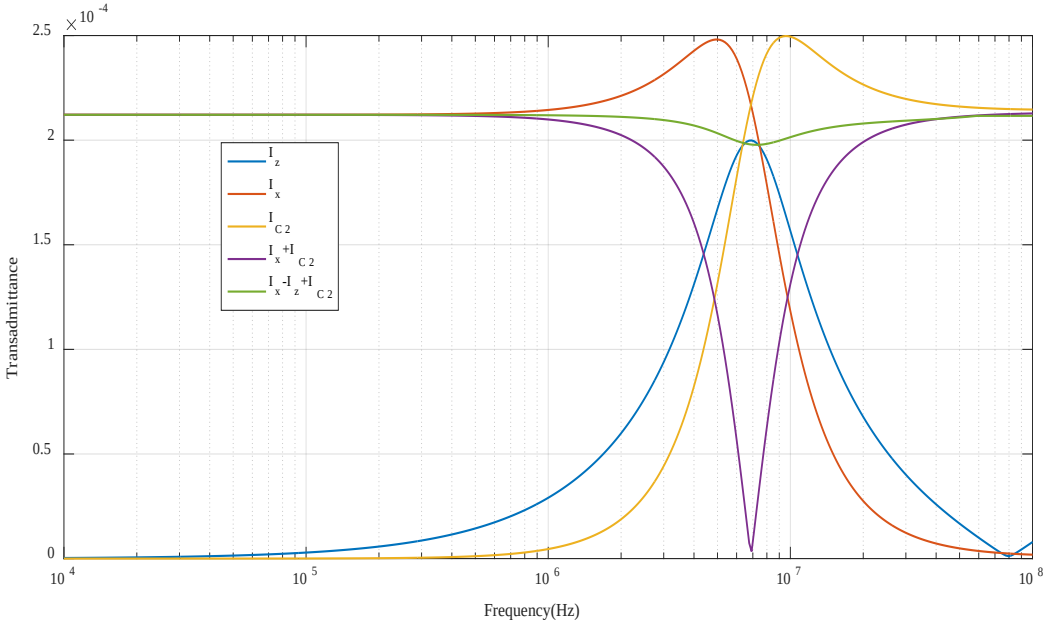
(A)



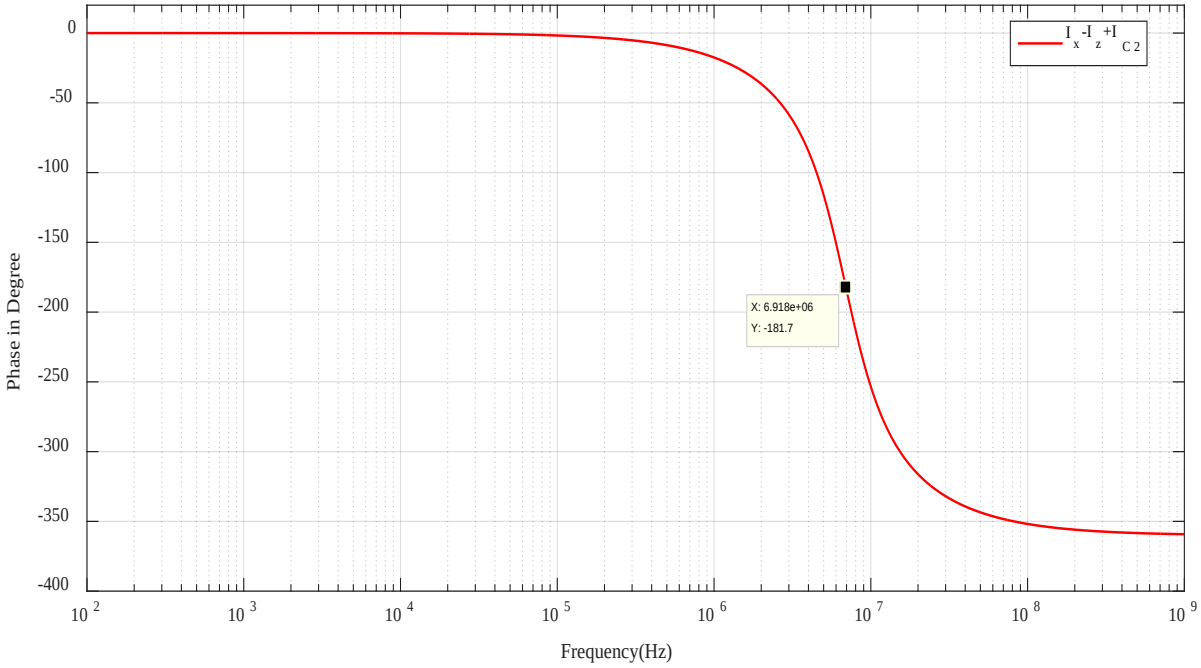
(B)

Fig: 5.16 Responses for voltage input $V_{in1}+V_{in3}$

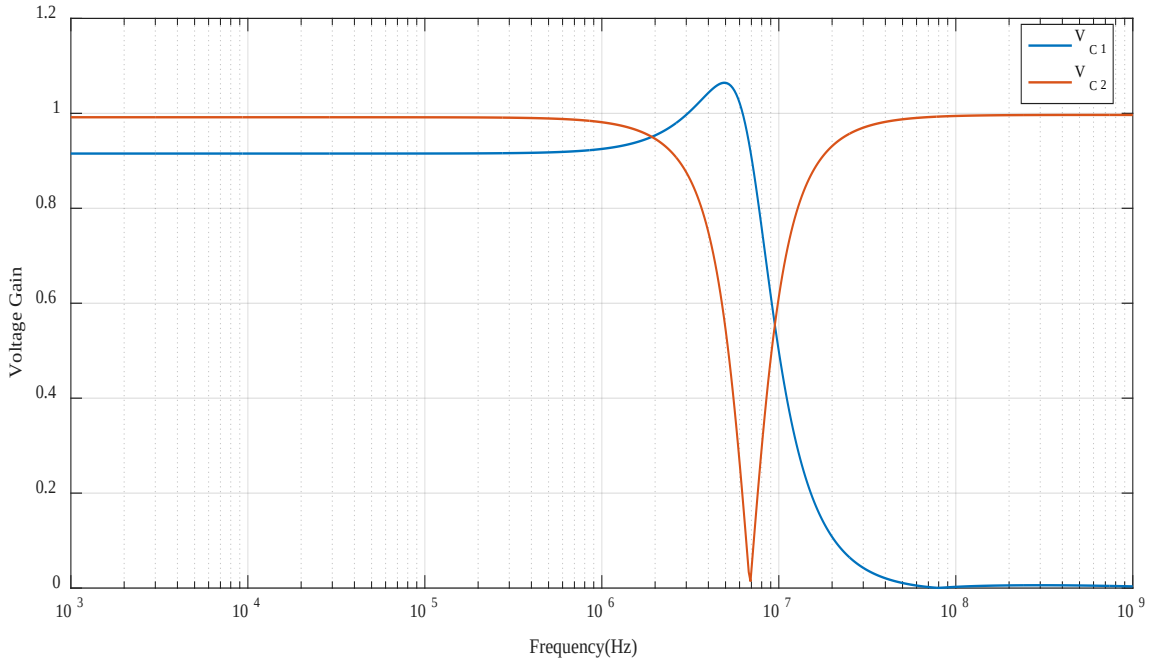
10. Combination of voltage input signals have been applied i.e. $V_{in1}+V_{in4}$ then the output responses are presented in Fig: 5.17



(A)



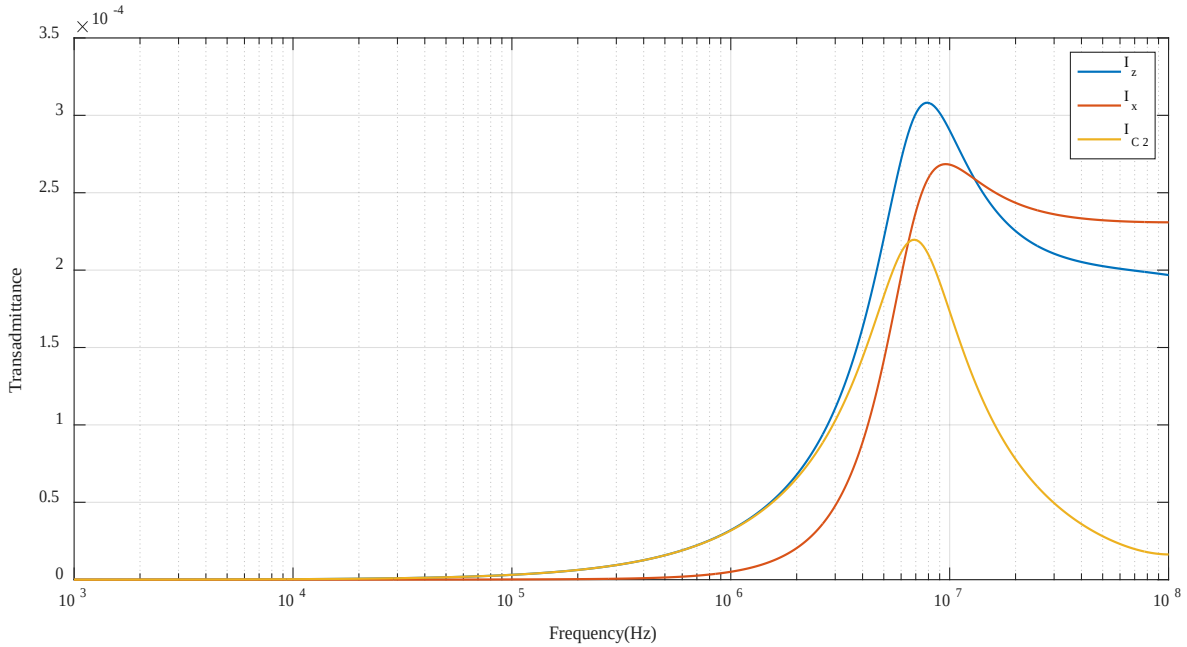
(B)



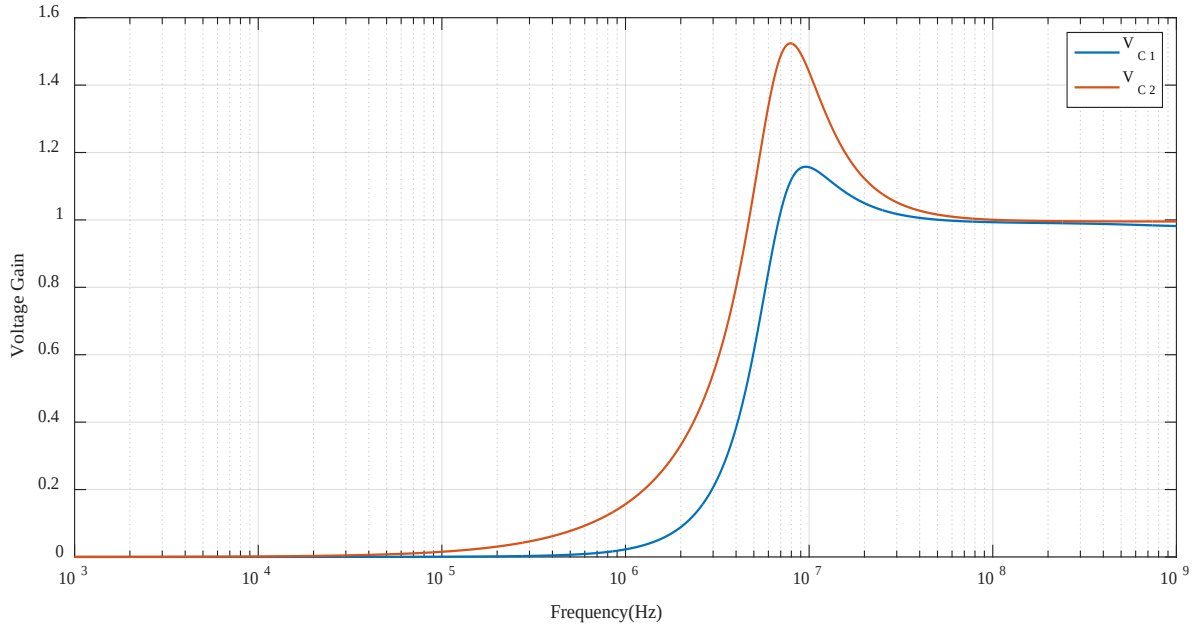
(C)

Fig: 5.17 Responses for voltage input $V_{in1}+V_{in4}$

11. Combination of voltage input signals have been applied i.e. $V_{in2} + V_{in4}$ then the output responses are presented in Fig: 5.18



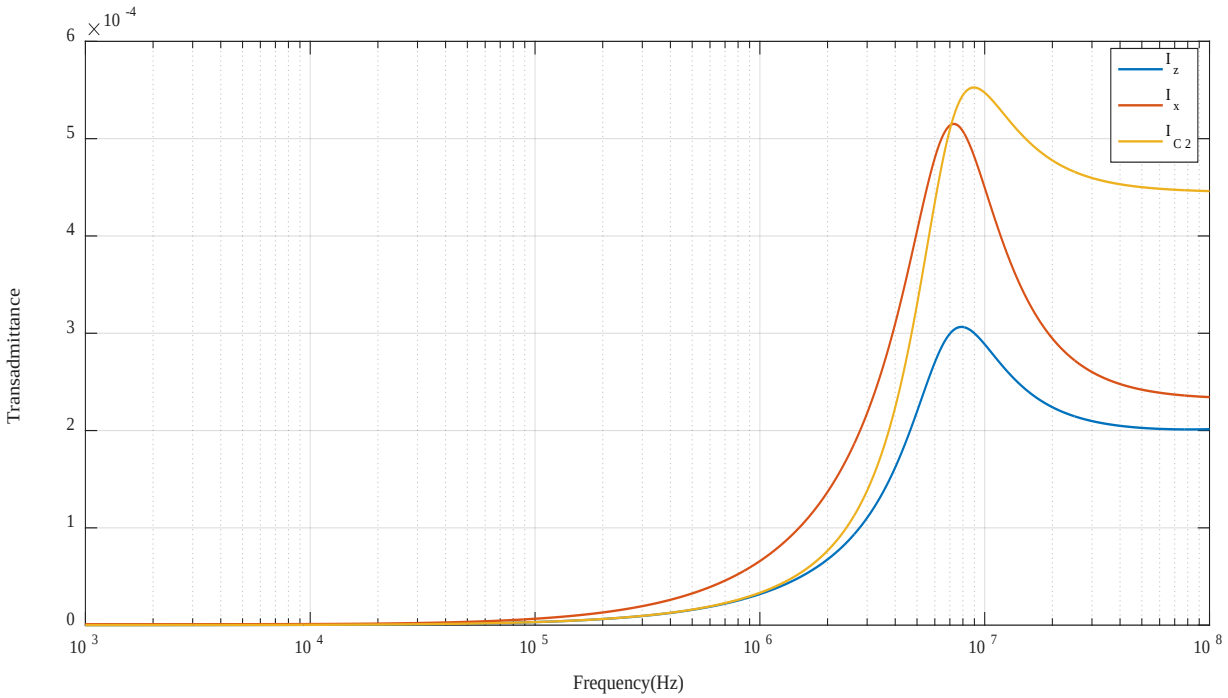
(A)



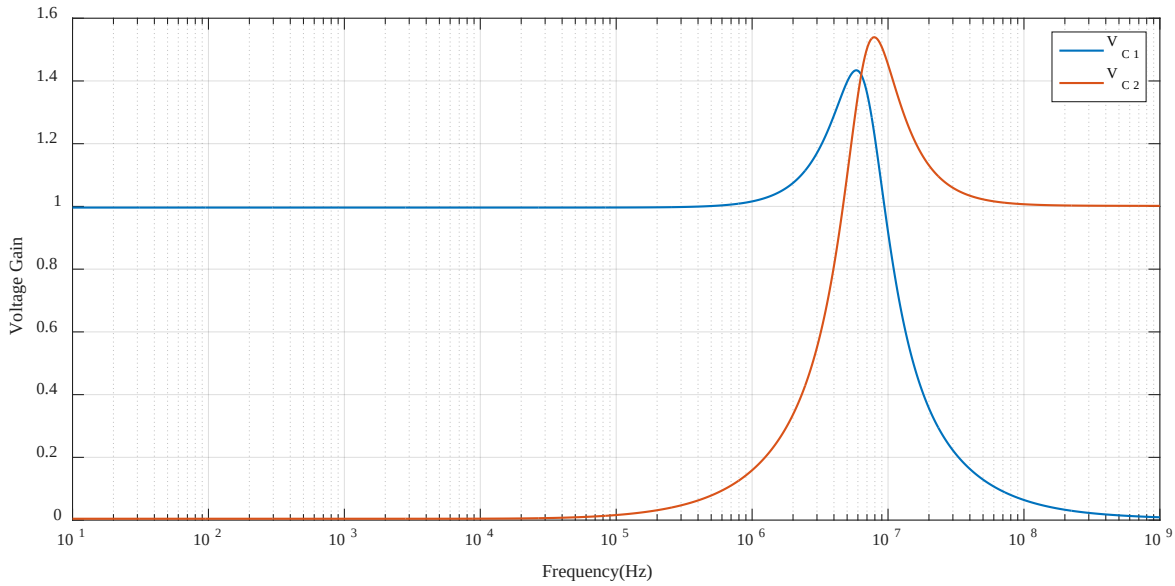
(B)

Fig: 5.18 Responses for voltage input $V_{in2} + V_{in4}$

12. Combination of voltage input signals have been applied i.e. $V_{in3}+V_{in4}$ then the output responses are presented in Fig: 5.19



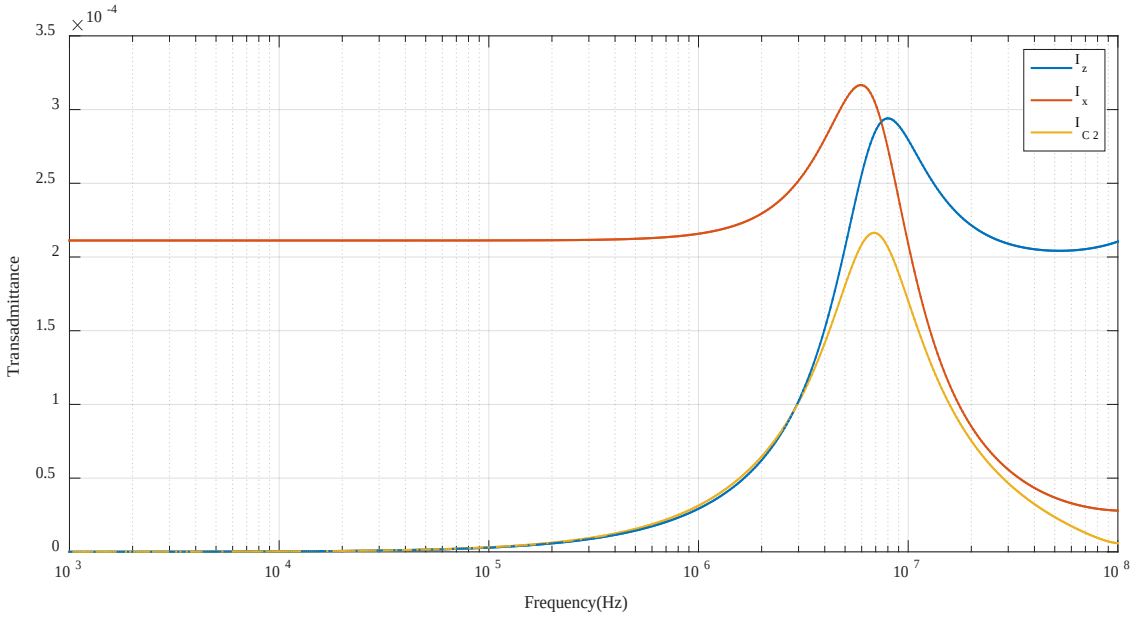
(A)



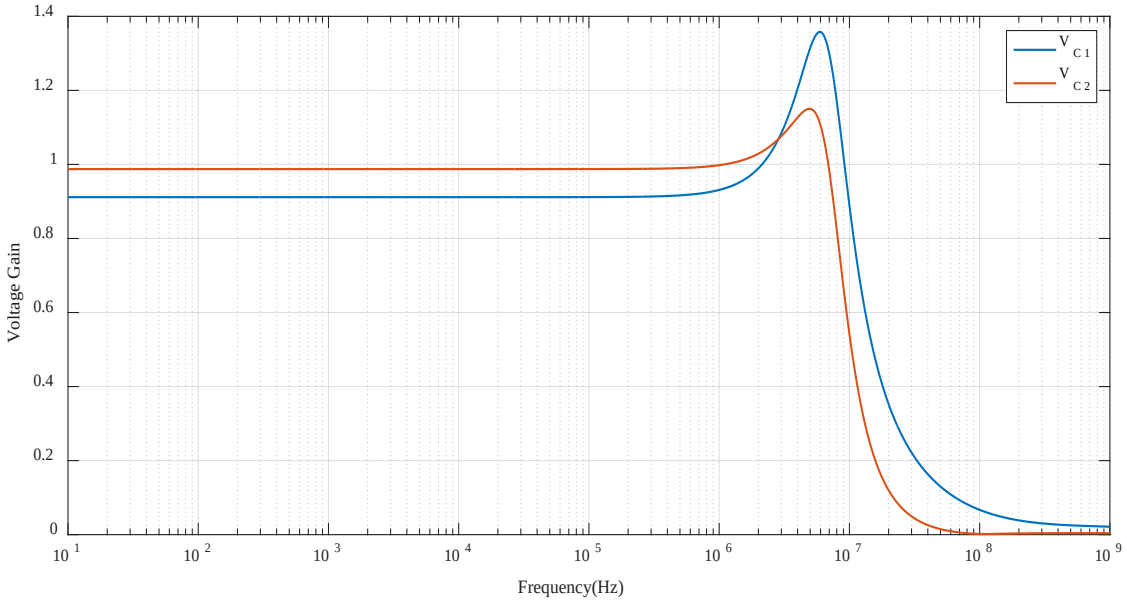
(B)

Fig: 5.19 Responses for voltage input $V_{in3}+V_{in4}$

13. Combination of voltage input signals have been applied i.e. $V_{in1}+V_{in2}+V_{in3}$ then the output responses are presented in Fig: 5.20



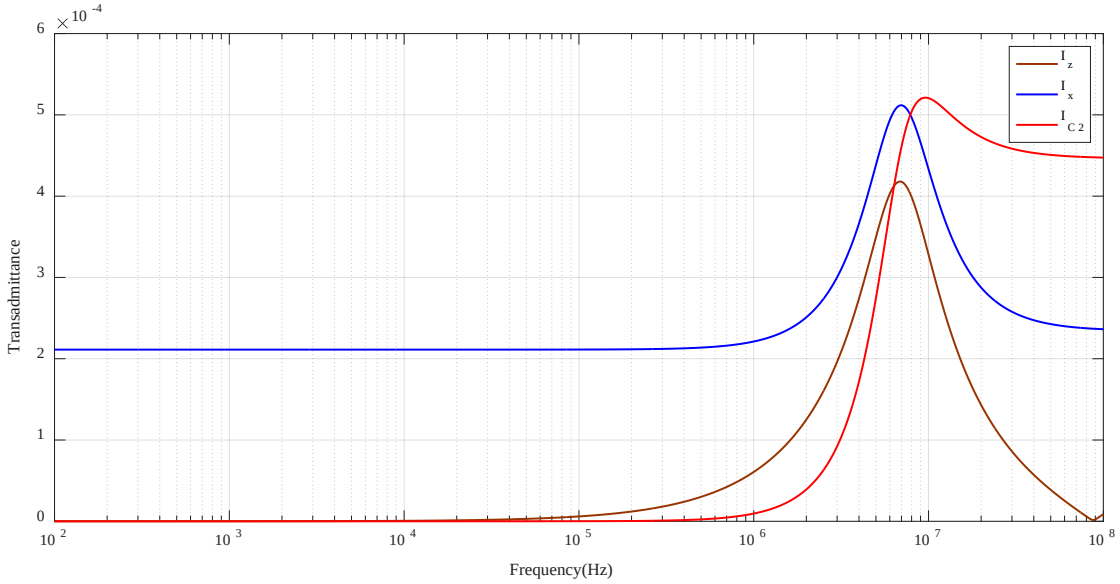
(A)



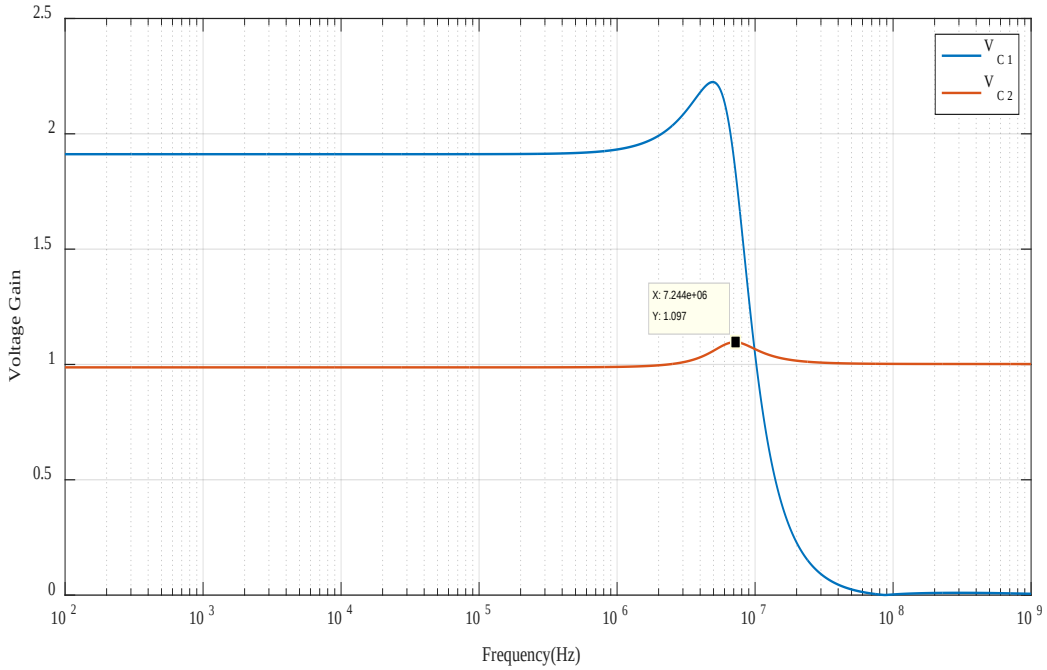
(B)

Fig: 5.20 Responses for voltage input $V_{in1}+V_{in2}+V_{in3}$

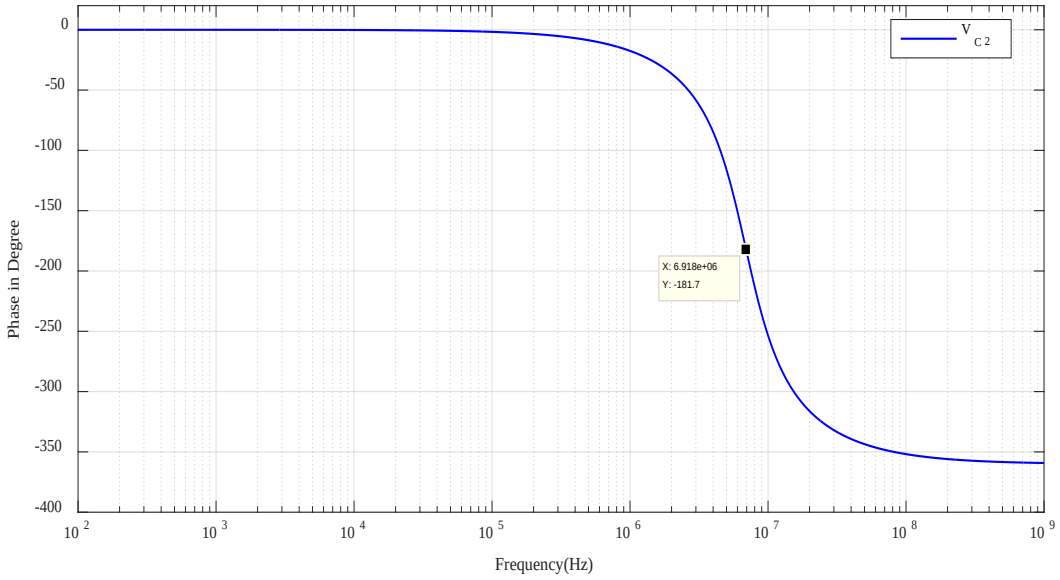
14. Combination of voltage input signals have been applied i.e. $V_{in1}+V_{in2}+V_{in4}$ then the output responses are presented in Fig: 5.21



(A)



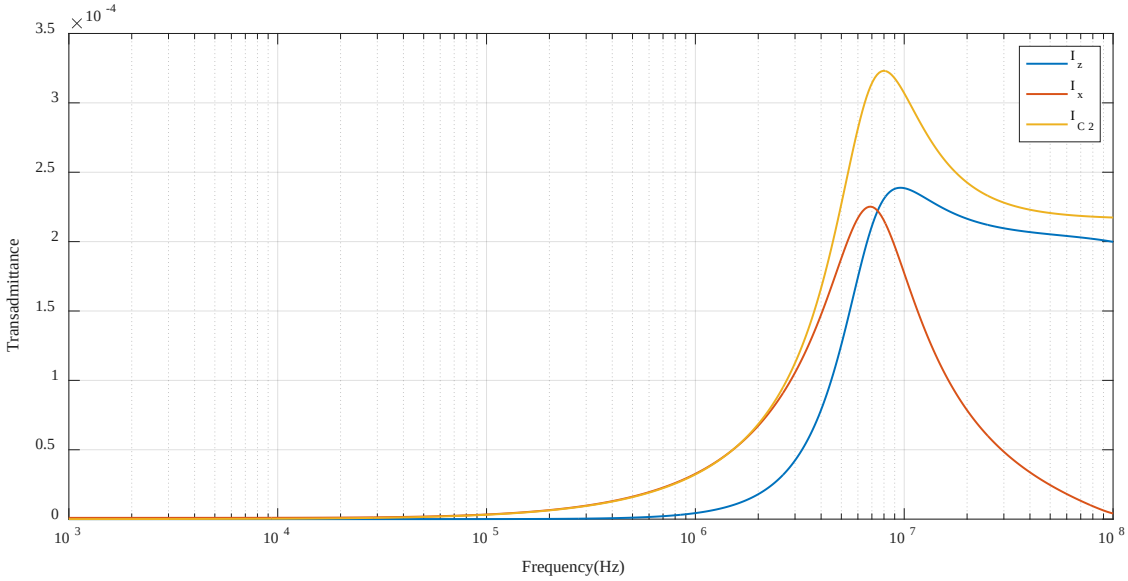
(B)



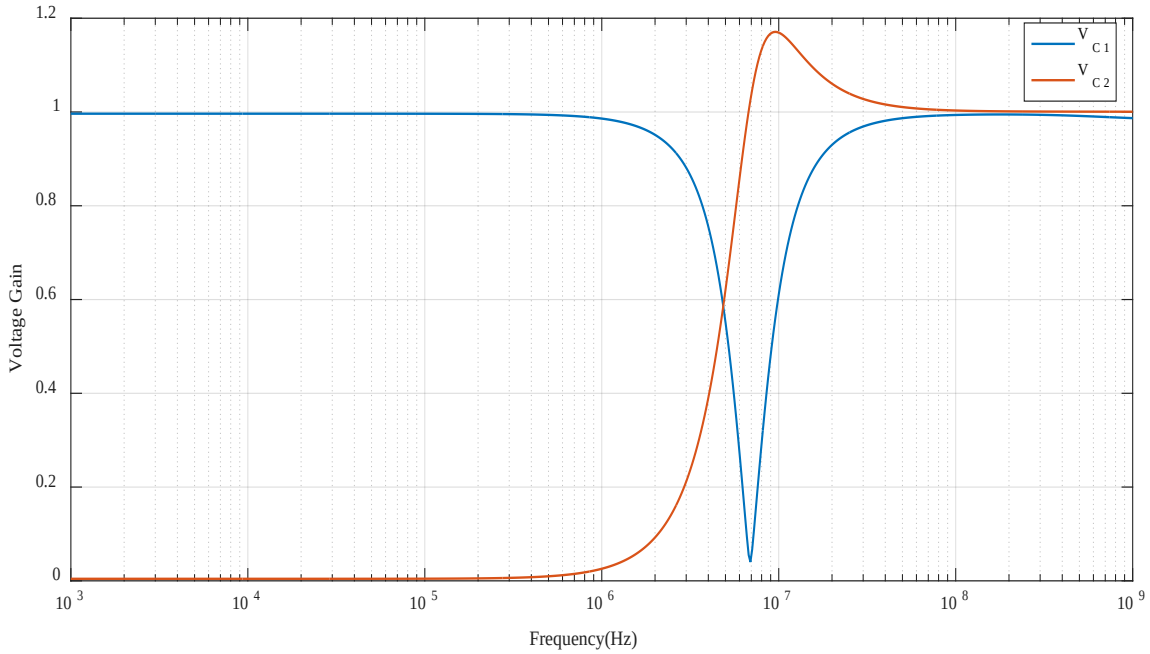
(C)

Fig: 5.21 Responses for voltage input $V_{in1}+V_{in2}+V_{in4}$

15. Combination of voltage input signals have been applied i.e. $V_{in2}+V_{in3}+V_{in4}$ then the output responses are presented in Fig: 5.22



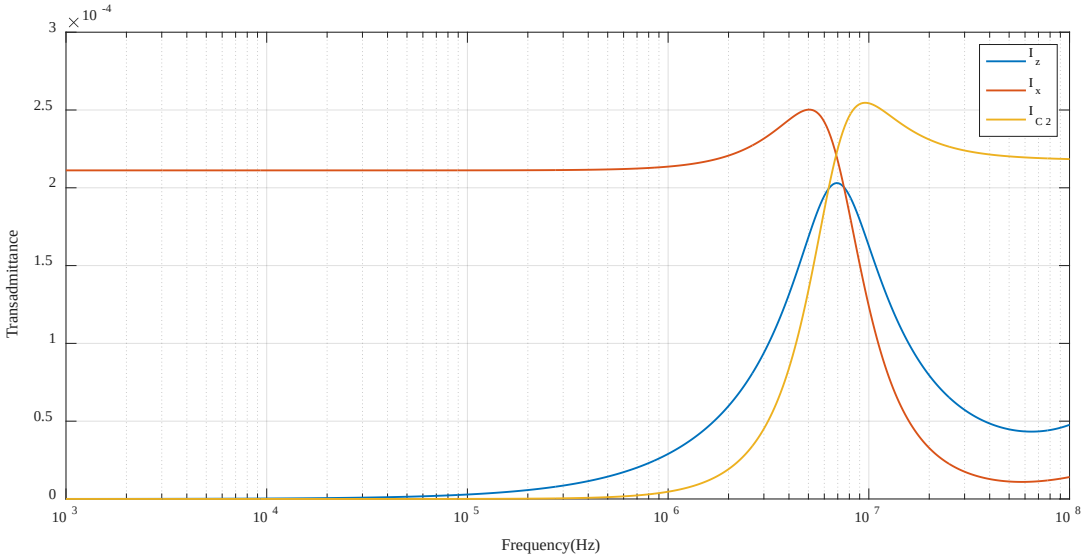
(A)



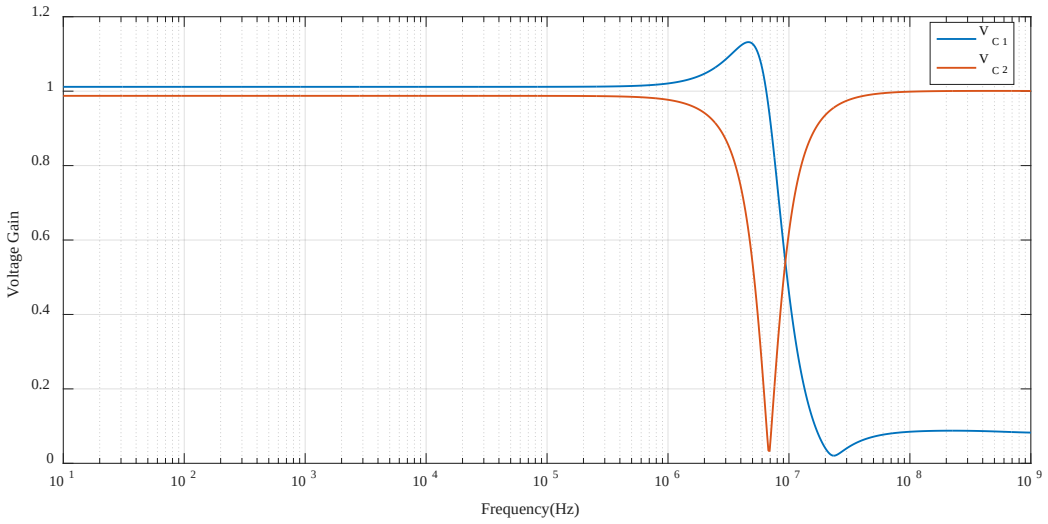
(B)

Fig: 5.22 Responses for voltage input $V_{in2}+V_{in3}+V_{in4}$

16. Combination of voltage input signals have been applied i.e. $V_{in1}+V_{in2}+V_{in3}+V_{in4}$ then the output responses are presented in Fig: 5.23



(A)



(B)

Fig: 5.23 Responses for voltage input $V_{in1}+V_{in2}+V_{in3}+V_{in4}$

Table for all the filter response:-

Table5.1Filter responses for MM biquad filter

Input Combinations	$I_{Z,out}$	$I_{X,out}$	$I_{C_2,out}$	$V_{Z,out}$	$V_{C_2,out}$
I_p	HPF	LPF	BPF	LPF	LPF
I_n	HPF	LPF	BPF	LPF	LPF
I_X	HPF	LPF	BPF	LPF	BPF
V_{in1}	HPF	LPF	BPF	LPF	LPF
V_{in2}	BPF	HPF	HPF	LPF	BPF
V_{in3}	HPF	HPF	HPF	HPF	BPF
V_{in4}	HPF	BPF	HPF	BPF	HPF
$V_{in1}+V_{in2}$	-------	BPF	HPF	BPF	LPF
$V_{in1}+V_{in3}$	-------	-------	LPF	LPF	LPF
$V_{in1}+V_{in4}$	BPF	LPF	HPF	LPF	BRF
$V_{in2}+V_{in4}$	HPF	HPF	BPF	HPF	HPF

$V_{in3}+V_{in4}$	HPF	BPF	HPF	LPF	HPF
$V_{in1}+V_{in2}+V_{in3}$	HPF	LPF	BPF	LPF	LPF
$V_{in1}+V_{in2}+V_{in4}$	BPF	------	HPF	LPF	APF
$V_{in2}+V_{in3}+V_{in4}$	HPF	BPF	HPF	BRF	HPF
$V_{in1}+V_{in2}+V_{in3}+V_{in4}$	HPF	LPF	BPF	LPF	BPF

Chapter 6

Conclusion and future work

In this thesis, analogue circuit applications based on CMOS based CD-DITA have been presented. In the introduction a brief on current mode signal processing has been presented which has lead to the motivation for work presented in this thesis. FVF based CD-DITA block has been realized and characterized in the chapter 3 using PSPICE simulations and CD-DITA based basic applications have been presented in 4thChapter . In 5th chapter modified MM filter based on CD-DITA has been proposed and grounded inductor nusing CD-DITA has been implemented. It has been simulated using CD-DITA block and 180nm technology parameters.

The future work will include the implementation of CD-DITA block as oscillators and other analog signal processing circuits.

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