GRID/OFF-GRID MULTILEVEL SPLIT VOLTAGE CONVERTER FOR PHOTOVOLTAIC SYSTEM FEEDING VARIETY OF LOADS

DISSERTATION

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
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OF

DOCTOR OF PHILOSOPHY

Submitted by:

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DECLARATION

I, AMRITESH KUMAR (2K11/PhD/EE/13) hereby declare that the work, which is being presented in the project report entitled, **"GRID/OFFGRID MULTILEVEL SPLIT VOLTAGE CONVERTER FOR PHOTOVOLTAIC SYSTEM FEEDING VARIETY OF LOADS"** submitted for partial fulfilment of the requirements for the award of the degree of Doctor of Philosophy is an authentic record of my own work carried out under the able guidance of Dr. VISHAL VERMA, Professor, EED, DTU. The matter embodied in the dissertation work has not been plagiarized from anywhere and the same has not been submitted for the award of any other degree or diploma in full or in part.

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CERTIFICATE

This is to certify that the thesis entitled, "**GRID/OFF-GRID MULTILEVEL SPLIT VOLTAGE CONVERTER FOR PHOTOVOLTAIC SYSTEM FEEDING VARIETY OF LOADS**", submitted by Mr. **AMRITESH KUMAR**, Roll No. 2K11/PhD/EE/13, student of Doctor of Philosophy in Electrical Engineering Department at Delhi Technological University (Formerly Delhi College of Engineering), is a dissertation work carried out by him under my guidance during session 2011-2017 towards the partial fulfillment of the requirements for the award of degree of Doctor of Philosophy.

The uniqueness of the thesis pertains to grid/off-grid multilevel split voltage converter for photovoltaic system feeding variety of loads, which has not been reported elsewhere.

I wish him all the best in his endeavors.

(Dr. VISHAL VERMA)
Professor, EED, DTU
SUPERVISOR

ACKNOWLEDGMENT

One looks back with appreciation to the brilliant teachers, but with gratitude to those who touched our human feelings. The curriculum is so much necessary raw material, but warmth is the vital element for the growing plant and for the soul of the child.

— Carl Jung

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GRID/OFF-GRID MULTILEVEL SPLIT VOLTAGE CONVERTER FOR PHOTOVOLTAIC SYSTEM FEEDING VARIETY OF LOADS

ABSTRACT

With growing pressure on depleting fossil fuels reserves, the focus has been shifted for harnessing more and more energy from renewable sources for sustainable growth. Photovoltaic system has emerged as a most appropriate solution due to proximity to the load centers and more or less predictable nature of intermittency. Conventional centralized photovoltaic (PV) grid tie inverters suffer from the problem of lower efficiency, high filter size, and limited depth of operation for remaining in connection with the grid, particularly under lower insolation/partial shading condition. The effect is reported to be more pronounced for single stage inverters integrating with weak distribution systems.

Further with the advancement of technology the residential loads have witnessed a paradigm shift from linear loads to nonlinear, dynamic and constant power loads which are customizable and configurable to cater specific application. To avoid multiplicity of AC – DC through DC-DC or DC-AC conversions, the concept of DC nanogrids have also evolved to cater the need of a variety of such loads.

Investigation of a multirole bidirectional cascaded multilevel converter (CMC) configuration in which a single phase supply is split into 3 different DC links enabling staggered PV connections and possibility of feeding variety of loads have been carried out. The considered configuration is also utilized to feed isolated single phase loads in an off-grid mode using appropriate modulation technique. Considered loads include dynamic, constant power and passive loads in addition to open-end winding induction motor drive (OEIM), battery charging/discharging etc. The connectivity of the load is considered on DC buses while in off-grid/grid connected mode and on AC side too while in off-grid modes. The proposed system configuration and the considered control algorithm suits to the majority of the residential loads while enabling it to act smartly for stabilizing the grid in case of the need. Further investigation on algorithm involved the DC bus balancing embedded in the control to ensure balanced voltage operation or operation at different voltages dictated by individual MPPT controller

across the DC links. The control scheme is further explored for bidirectional power transfer with smartly charging/discharging control of the split battery stacks at customized rates depending on the SoC's of battery stacks and on feeder loading conditions, without disturbing the DC bus voltages. The exploration has been extended for operation during under-voltage grid condition where the customization in proposed algorithm enables the rotating charge control algorithm which helps the grid to stabilize its voltage in conjunction with maintaining life cycle of the battery.

The proposed configuration and control enjoys the advantage of 3 separate DC buses having both voltage and power level 1/3rd of the total DC voltage and power, which enables the reduction in the voltage rating of capacitor; making system more modular and compact and deriving power from AC is with reduced voltage THD and providing immunity against unbalanced DC link voltages across the H-bridges.

The complete model of the CMC with a variety of loads and their embedded control is analytically derived and simulated in MATLAB Simulink environment before testing on hardware prototype for its validation. A detailed stability analysis is also presented in the d-q frame for the control design to access the feasibility of operation with a variety of loads. The effectiveness of the control algorithm under low grid frequency and dip in voltage conditions are clearly demonstrated through results. The results clearly show derived current from the grid at unity power factor ensuring improved power quality operation. Further, keeping the entire voltages on the DC buses constant or at voltage dictated by MPPT controller ensures immunity against disturbance both from AC or DC side. A comparative analysis is also done for the operation of PV under partial shading condition for a conventional 2 –level PV inverter vis-à-vis proposed CMC-based approach. Further PV-CMC system for enhanced performance under voltage sag is studied to demonstrate the LVRT capability. The d-q based control provides efficient independent and smartly control with active/reactive or both power support depending on the voltage sag and PV panel power condition. The thesis also proposes control techniques for off-grid mode, which will match the utilization and storage of power provided by the PV panels of the same capacity and same size of the battery connected at each level. The control method utilizes rotation policy for the operation of each bridge at each level in three

fundamental cycles, to enhance both the lifetime of the battery, the operation of H-bridges and PV panels used.

Same scale hardware prototype using open end induction motor, passive loads and battery loads (charging/discharging) on different DC links is developed and experimentally validated using requisite hardware and DSP controllers (dSPACE 1104 and dspic33FJ16GS502). The development of hardware including fabrication of various control cards, interface card, voltage and current measurement cards etc. have been indigenously done. Both simulation and experimental results are presented which always show good agreement with theoretical analysis.

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LIST OF ABBREVIATIONS

Abbreviations	Full-Form
PV	Photovoltaic
AC	Alternating Current
DC	Direct Current
P&O	Perturb And Observe
InC	Incremental Conductance
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
VSI	Voltage Source Inverter
MIC	Module Integrated Converter
THD	Total Harmonic Distortion
SHE	Selective Harmonic Elimination
LED	Light Emitting Diode
BLDC	Brushless DC Motor
TV	Television
CMC	Current Mode Control
EMI	Electromagnetic Interference
STATCOM	Static Compensator
PWM	Pulse Width Modulation
d-q	Direct-Quadrature
VVVF	Variable voltage variable frequency
CCAR	Cascaded Converter Active Rectifier
OEIM	Open end winding induction motor
G2V	Grid to Vehicle
V2G	Vehicle to Grid
SoC	State of Charge
SPS	Smart Parking System
EVs	Electric Vehicles
LVRT	Low Voltage Ride Through
BOS	Balance Of System
PSO	Particle Swarm Optimization
HF	High Frequency

VSC	Voltage Source Converter
LSPWM	Level-Shifted Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modulation
IPD	In-phase disposition
APOD	Alternative Phase Opposition Disposition
POD	Phase Opposition Disposition
PS-PWM	Phase shifted pulse width modulation
LMS	Least Mean Square
ADALINE	Adaptive Linear Element
CMV	Common Mode Voltage
BESS	Battery Energy Storage System
CMAR	Cascaded Multilevel Active Rectifier
SRF	Synchronous Reference Frame
PLL	Phase Locked Loop
PCC	Point Of Common Coupling
LPF	Low Pass Filter
PI	Proportional Integral
UPF	Unity Power Factor
PQ	Power Quality
HEV	Hybrid Electric Vehicle
PHEV	Plug-In Hybrid Electric Vehicle
LI-ION	Lithium Ion
CHBMLI	Cascaded Half Bridge Multilevel Inverter
THD	Total Harmonic Distortion
V/F	Voltage/Frequency
DSO	Digital Storage Oscilloscope
SPL	Smart Pump Load
VIL	Variable Illumination Load
ADC	Analog to Digital Converter
LV	Low Voltage
CMCS	Cascaded H-bridge Multilevel Converter System
NO / NC	Normally Open / Normally Close
SSSVC	Solid State Split Voltage Converter
CMIPV	Cascaded Multilevel Inverter Photovoltaic

Chapter I

INTRODUCTION

1.1. General

In the era of rapid industrialization and modernization has created a spurt in energy demand which cannot be avoided. With the limitations imposed by environmental concerns and depleting fuel reserves the generation from conventional sources, has been slowly migrating towards renewable energy sources for sustainable growth. In contrast to centralized generation system, the distributed generation system includes many generating and storage units, facilitating energy efficiency due to consumption at load centers, reduction in the pollution due to the use of renewable sources and good power quality due to quick response and more reliability [1]. Further energy efficient devices, circuit configurations and components are encouraged for use, to harvest the maximum available power from the sources and thereby reducing the burden on the power system. Particularly the power electronics came as a great booster for the efficient power conversion system using renewable sources based generation. Specifically, PV technology has advanced and gets developed at a much faster rate than the efforts made on the development of grid code for effectively and efficiently managing the high penetration of distributed PV systems within the existing distribution system [2].

Technological growth has envisaged various conventional and contemporary types of loads like non-linear, dynamic and constant power. Particularly residential places have witnessed varied types of loads like led lighting, consumer electronics, pump loads, battery loads and electric vehicle loads as shown in Fig. 1.1. All these loads demand multiple units of inverter and converter to feed power for a particular application. To ease the multiple conversion and losses, the concept of DC nanogrid has evolved for residential loads. Further to make these DC nanogrids more reliable, efficient and configurable, there is a need to explore efficient control schemes and converter configurations to zero down on multi-role converter systems which are capable of

integrating the renewable energy sources and storage sources with the grid, besides supplying to the load. Such converter/inverter systems further need to be smart enough to enable bidirectional power transaction with the grid as per need and condition prevailing on the grid.

The multilevel configurations, therefore, become the center of interest for the investigation to suit the multirole operation. With an intention to maximize the utilization of PV power, the widespread and staggered PV configuration are advocated utilizing cascaded multilevel converter/inverter configuration which is shown suitable for grid coupled applications. In this thesis, the single phase cascaded multilevel configuration is investigated in both grid/off-grid mode for its suitability and applicability to the variety of varying residential loads. The structure and its control under the varied condition of the grid are also probed using both level shifted and phase shifted modulation techniques

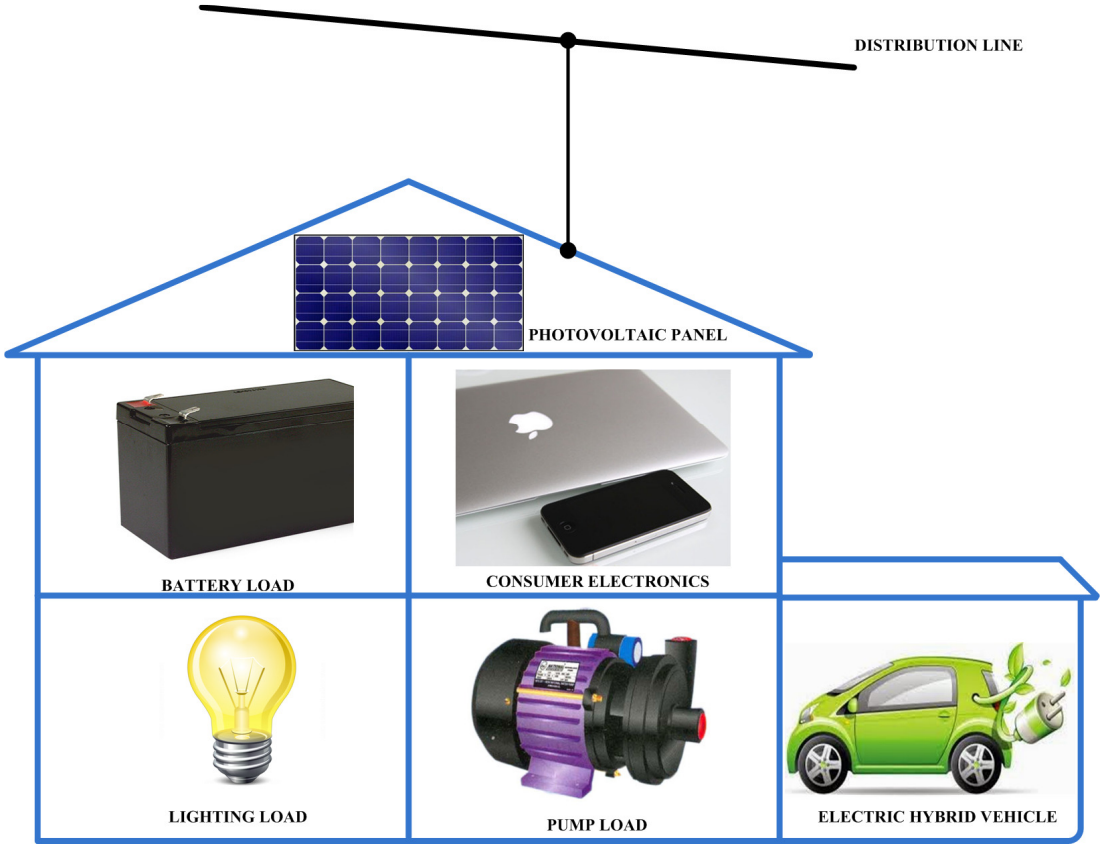


Fig.1.1: Simplified representation of residential loads having roof top PV Panels.

to get the desired good quality stepped output voltage waveform with minimal or no filter applications in consonance with IEEE 519 standard.

The following sections and subsections give an insight of the state of the art photovoltaic (PV) and multilevel converter/inverter topologies. In addition, the issues of grid connected and off-grid PV systems are also presented. Further to this selection of the cascaded multilevel converter for its suitability to feed residential load is presented and the later put a brief outline of the scope of the work and organization of the thesis is given.

1.2. Solar Photovoltaic System: Issues and Opportunities

For effective utilization of power generated through PV panels the harvesting of full energy, becomes mandatory. If it is left unharnessed, it may further deteriorate the efficiency due to heating of PV panels and to a great extent may eat away the productive life of PV cells. Various control algorithm like Perturb and observe (P&O), Incremental Conductance (INC) etc. are in practice for keeping the energy production near maximum power point (MPP) through the use of power electronics converter.

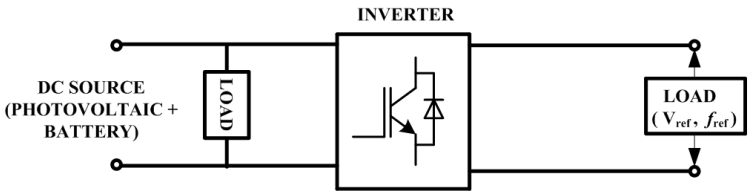


Fig. 1.2: Single phase off-grid PV system.

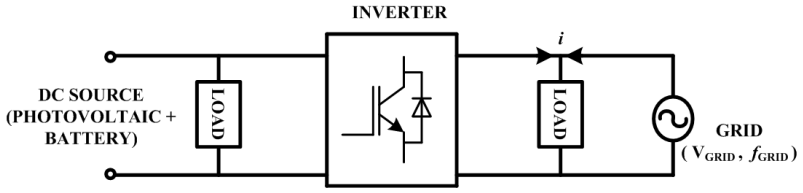


Fig. 1.3: Single phase grid connected PV system.

A large number of topologies of DC-DC converter both isolated and non-isolated have emerged with a core focus on the cost-effectiveness, efficiency and reliability of the operation. Isolated converter offers better safety, as it prevents the flow of leakage current due to the creation of common mode path, but at an increased cost. For effective use, the developed power is further inverted (DC – AC) to feed power to the AC load or to the distribution network fed through the national grid or operating in off-grid configurations as shown in Fig. 1.2 and Fig. 1.3. However, to cater such loads at the standardized voltage levels often string/array of PV panel are used to power the dc bus of the inverter with/without (single stage) DC-DC converters with higher efficiencies. In single stage application, the inverter needs to perform the dual duty i.e. MPP tracking (MPPT) and bidirectional Power transfer. Though single stage configuration eliminates the need for an extra DC-DC converter, during voltage sag the instantaneous increase in PV system output current results into momentarily decreases in DC link voltage dragging the operating point towards I_{SC} on the I-V characteristics of PV panel and thus system gets auto protected.

The country like India where solar insulation is quite steady and evenly distributed the single stage configuration with a large number of PV panels on the DC link can be a cost effective scheme. Conventional voltage source converter (VSC) with 2 level output suffers when the large PV string undergoes partial shading condition due to bypassing of few panels in the string, making it difficult to make up the DC bus, in turn failing to deliver power to the grid. Such low power transaction with low output current drives the voltage across many panels towards the open circuit voltage (V_{oc}) away from MPP voltage, leading to the loss of PV power generation. Such situations will unnecessary burden the grid, even when PV generation is otherwise available. German grid code for LV grid dictates that PV system should remain connected with the grid to the extent possible, supporting the grid and to derive the accelerated payback on hardware installation even under partial shading conditions upto the limits of the power generation.

1.3. PV String and Array: Challenges

PV panels exhibit a typical non-linear I-V and P-V characteristics. This varies with varying irradiance and temperature conditions as shown in Fig. 1.4 and Fig. 1.5. The PV panel is comprised of many single solar cell units connected in series and in parallel. To offer power at a requisite voltage and current levels PV arrays are made by connecting many such panels in series and parallel. If the number of panels are increased in series it leads to increase in open circuit voltage and when paralleled it increases the short circuit current of the PV arrays. Various MPPT algorithm such as perturb and observe (P & O),

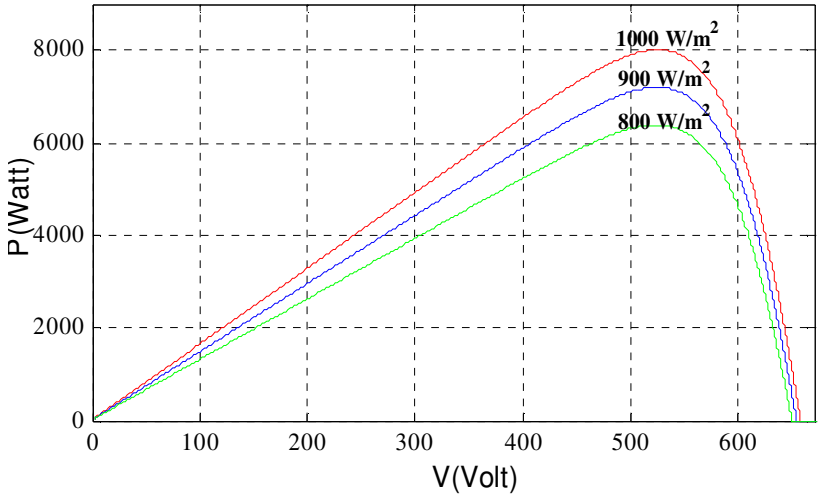


Fig. 1.4: P-V characteristic of PV array.

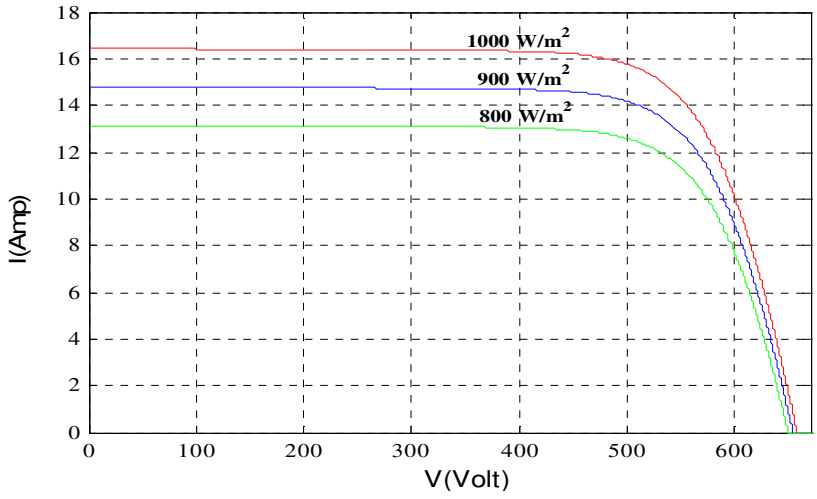


Fig. 1.5: I-V characteristic of PV array.

Incremental conductance (INC) etc. are advocated in literature for operation at MPPT during unshaded conditions of panels, which is uncommon for rooftop PV system prevalent for urban areas. Under partial shading condition due to bypassing of few panels in the string, such algorithms fail to track the global maximum power point (MPP) operation as explained in Fig. 1.6 and Fig. 1.7.

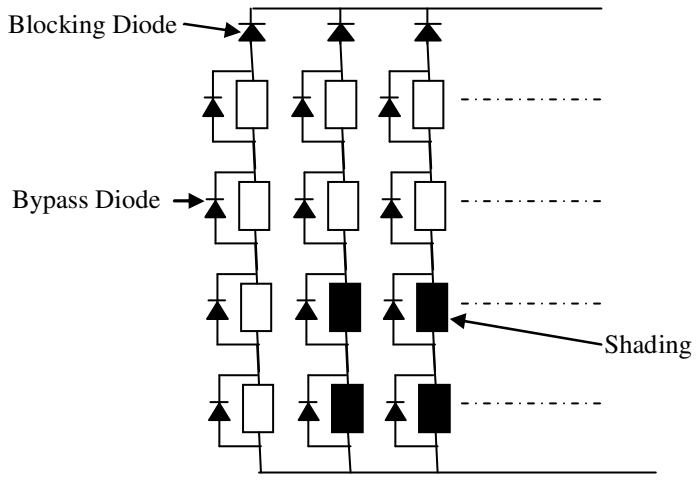


Fig. 1.6: Panel configuration showing partial shading.

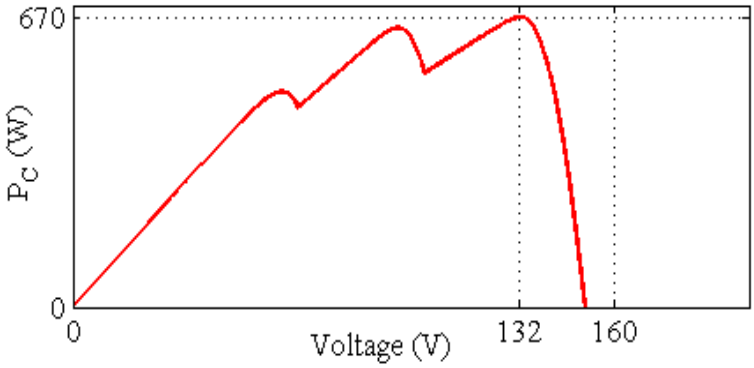


Fig. 1.7: P-V curve showing partial shading condition.

1.4. Converter/Inverter for PV System

Converter/Inverters are the enablers for transacting PV power into the grid. The conventional grid integration is based on centralized inverters that interface a large

number of PV modules placed in an array to a common dc link. These PV modules are coupled to the grid either in single stage or two stage configuration as shown in Fig. 1.8 and Fig. 1.9 [3]. Many parallel strings of PV panels are connected to generate sufficiently high voltage and power to avoid amplification by converters in single stage configuration. But the main problems associated with these centralized single stage inverters lies with high-voltage dc cables between the PV modules and the inverter, power losses due to a centralized MPPT, mismatch losses between the PV modules and losses in the string diodes.

Sometimes in the absence of sufficient number of panels to build up the requisite voltage, DC-DC converters are used in between the string of PV panels and the inverter making it a two stage configuration as shown in Fig. 1.9. In double stage mainly isolated or non-

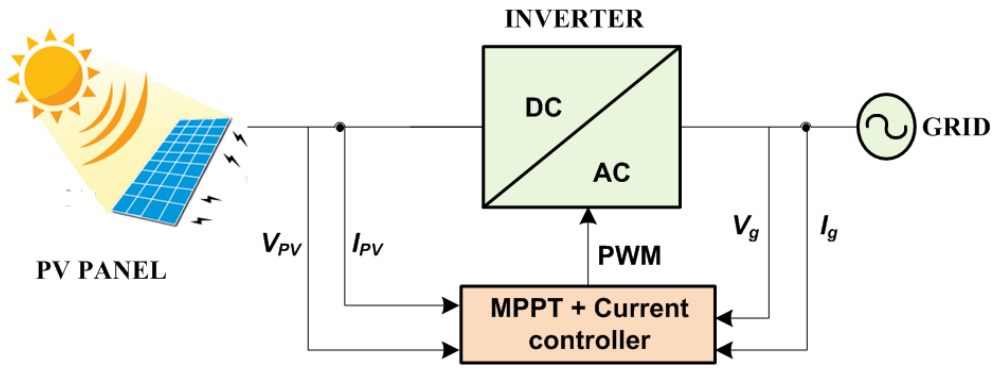


Fig. 1.8: Single stage topology where the dc–ac inverter is responsible for the MPPT and the grid current control.

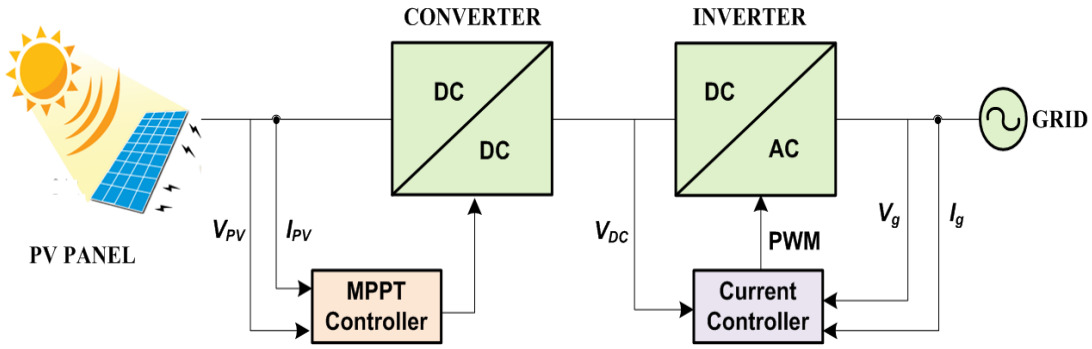


Fig. 1.9: Double stage topology where the dc–dc converter is responsible for the MPPT and the dc–ac inverter controls the grid current.

isolated DC-DC converters are used in conjunction with voltage source inverter (VSI). Isolated topology though enhances the overall cost of the system, but provides an additional advantage in terms of isolation, which avoids leakage current, preventing the occurrence of hazardous situations. For the low wattage PV system, low cost non-isolated converters are preferred.

Recently module integrated converters (MIC) have gained popularity, wherein the generated power is transformed to grid quality, which is capable of avoiding the mismatch losses between PV modules since there is only one PV module and it also facilitates the individual MPPT. But since, single PV module is being used; it requires high amplification to match the grid voltage making it a costly proposition.

2- Level multi-string/string inverter is popularly deployed in the field. The topology consists of several PV strings, each connected with separate dc-dc converters to a common dc–ac converter [4] [5]. This topology features several advantages such as the independent tracking of the MPP of each string and the possibility to scale the system by plugging more strings to the existing plant. But the power output suffers a lot from partial shading condition. Further, the losses and stresses on switches are quite high due to the high voltage condition prevailing on single DC link capacitor. Due to the heavy power transaction across the common capacitor, its capacitance is kept to be very high which further deteriorate the life of the PV system.

The classical two-level VSIs is mainly limited to low or medium power applications due to the power-semiconductor voltage limits. With the inclusion of few components, like diodes or capacitors, a new set of inverter/converter topology popularly known as multilevel-VSI technology is came into use. Multilevel inverter/converter topologies produce high-quality AC voltage waveforms even with power semiconductor switches operating at a lower frequency as compared to 2-level inverter [6].

1.5. Multilevel Topologies for PV System

Voltage source based multilevel topologies may be divided among classical or traditional topologies and modern hybrid topologies as shown in Fig. 1.10. Classical topologies like neutral-point clamped (NPC), a flying capacitor (FC), and the cascaded H-bridge (CHB)as shown in Fig. 1.11 are the most studied and commercialized [7] [8]. Though the NPC and FC may be utilized for PV system with good quality output voltage waveform, due to the availability of common DC link the PV panels could not be distributed to avail relief during partial shading conditions. Further, the requirement of high DC tank capacitor and losses due to panel mismatch are also not circumvented.

Among the available multilevel converter topologies, the cascaded H-bridge multilevel converter/inverter forms a promising alternative as it provides the benefit of integrating each PV panel through separate DC link, and utilizing low voltage rating of the capacitor

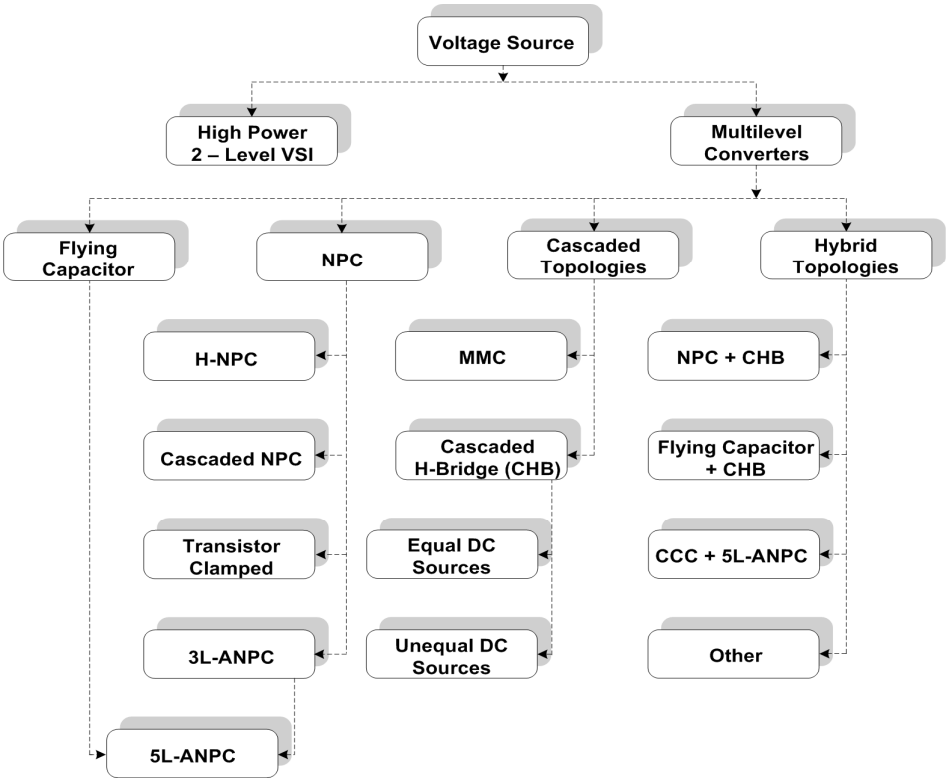


Fig. 1.10: Voltage source based multilevel converter classification.

for cost offsetting and lifetime improvement.

1.6. Cascaded Multilevel topology for PV System

Cascaded multilevel converter (CMC) is having multiple dc links which facilitate for housing multiple PV panels and enable independent voltage control and the tracking of the MPP in each string. It increases the efficiency of the PV system in case of mismatch in the strings, due to unequal solar radiation, aging of the PV panels etc. [9]. The structure allows a transformerless connection to the grid as individual H-bridge voltage gets cascaded to build the terminal voltage which is a match with grid PCC voltage. Further, the multilevel topology features several degrees of freedom that make possible the continuous operation even in case of a fault. It is, therefore, the system been enjoyed higher reliability. Further, multiple DC links facilitate theintegration of multiple residential loads in conjunction with PV panels.

1.6.1. Basic Configuration And Operation

Fig. 1.11 (c) shows the single phase leg of CHB structure having 2 units of H-bridge cells connected in series. Each cell produces namely three states + V_{dc}, 0, - V_{dc} through

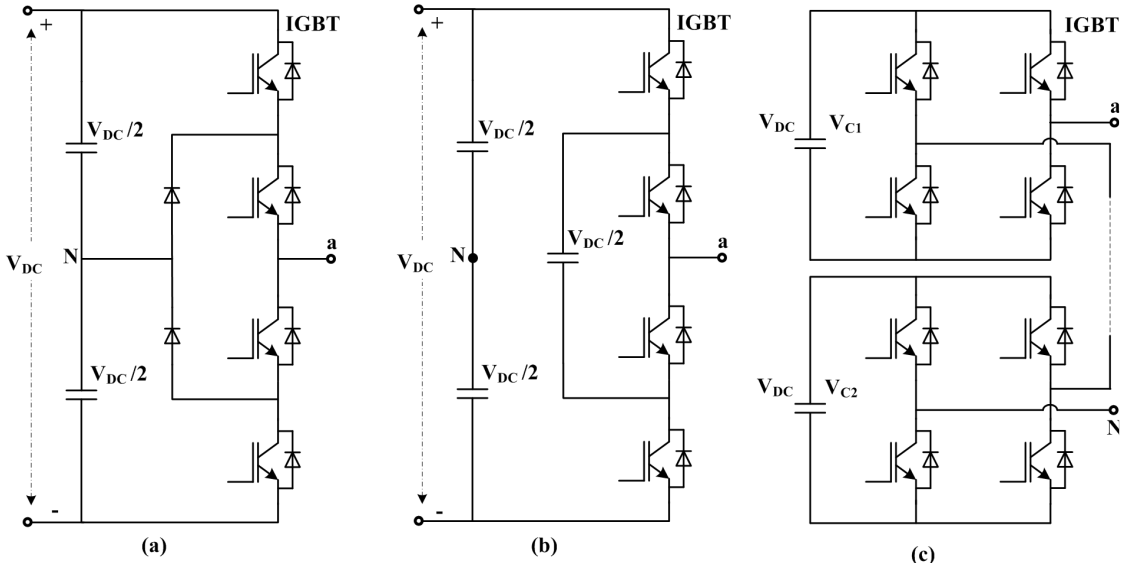


Fig. 1.11: Classic multilevel converter topologies (a) 3L-NPC (b) Three-level FC (c) Five-level CHB

independent sources namely battery, PV etc. The resulting phase voltage is obtained by addition of individual cell voltage. In the present case output ac voltage waveform swings from - $2V_{dc}$ to + $2V_{dc}$ with 5 levels making output to closely following sinusoidal waveform without a filter as shown in Fig. 1.12. With the increase in levels, the waveform gets more and more closure to the sinusoidal waveform and thereby bringing a reduction in voltage THD drastically.

For multilevel converter in inverter mode (DC-AC) the DC link may either to be fed from the battery or for PV system output. On the other hand in absence of PV during the night or at low insolation level, the converter may operate in rectifier mode (AC-DC) to fulfill the power need of load connected to the DC links. Multilevel converter voltage is controlled through different modulation schemes. Mainly sine-triangle modulation and space vector modulation scheme for switching sequence generation for H-bridge cells are practiced. Selective harmonic elimination (SHE) methods also are reportedly used for cell control. Under sine-triangle modulation, mainly level shifted and phase shifted techniques are used for pulse generation [10]. Fig. 1.13 (a) and (b) shows the basic

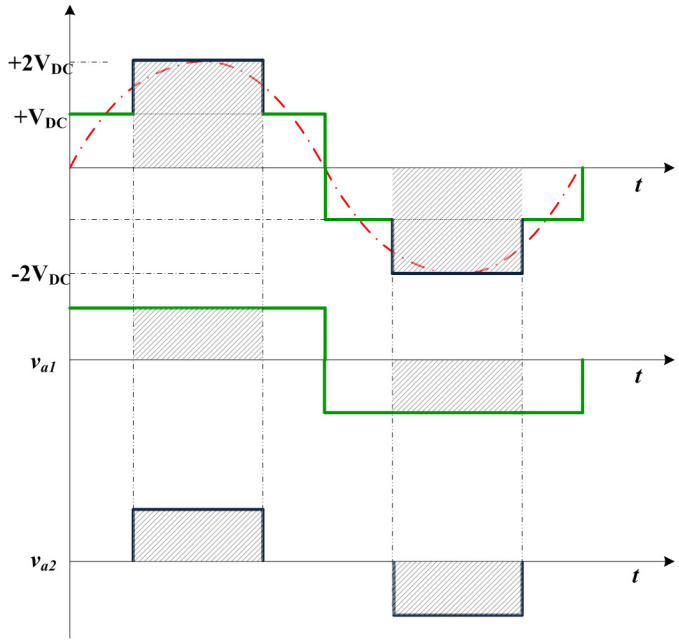


Fig. 1.12: Five-level CHB associated voltage waveforms.

switching sequence generation using both PWM methods for individual H-bridge cell by comparing the modulating signal with the carrier signal.

1.6.2. Issues of Multilevel Converter

The CHB converter is typically designed for equal power sharing across individual H-bridge cell. But due to non-uniform insolation, partial shading condition or particular H-bridge cell degradation the generated or available power at each DC link might not be equal. Further, in rectifier mode, the loading at individual DC link might be different.

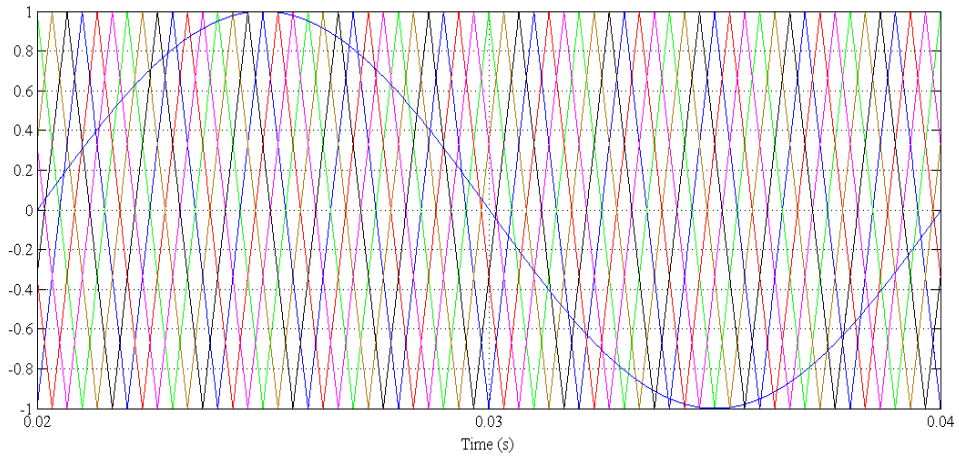


Fig. 1.13 (a): Waveforms of phase shifted carrier signals and modulating signal.

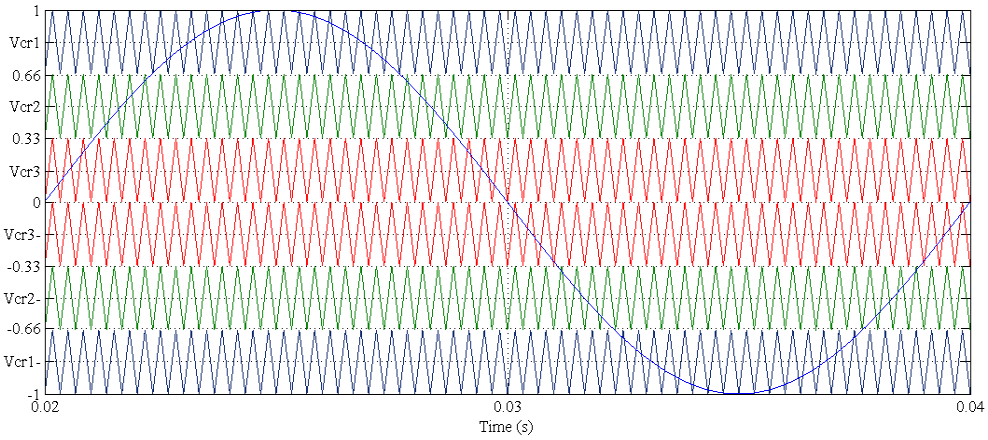


Fig. 1.13 (b): Waveforms of level shifted carrier signals and modulating signal.

This uneven power distribution across the H-bridges if left unattended may cause the uneven voltage across the DC links. And, this uneven DC voltage condition gets reflected into 3 phase current, causing unbalance currents. So as to maintain the power quality of

voltage and current waveform, it is necessary to incorporate voltage/power balance control. The power imbalance problem may be classified as [11]:

(a) Inter-phase (clustered) power imbalance, which occurs when each phase generates a varying amount of power.

(b) Inter-bridge (individual) power imbalance, which happens when each H-bridge cell in the same phase leg generates a varying amount of power.

1.6.3. Large PV Farms Connected to 3 Phase System

Three legs of similar configurations as shown in Fig. 1.11 (c) for a single leg, when connected in star or delta connection, makes a 3 phase structure. The modular structure of CMC allows easy extension of H-bridge cell to reach high voltage and power, thus making it feasible the integration of with large PV system to the 3 phase medium voltage network. The CMC configuration is mostly discussed and been commercialized for 3 phase system as it may handle high voltage and power with single converter unit. However, the exploration of the usefulness of the CMC structure is due for the investigation to residential applications to practice the concept of distributed consumption and distributed generation.

1.6.4. Small PV–Grid System for Residential PV

The residential single phase grid connected 7 level PV system shown in Fig. 1.14, clearly depicts each individual DC link may house separate PV panels. Majority residential loads are turning to low voltage DC loads, may it be LED lighting, BLDC fan or pump loads, TV, mobile chargers, battery chargers etc. Such load may conveniently connect to the DC links of such multilevel converters making a more reliable and efficient PV-grid hybrid power source working incoherence. Since the structure is connected in single stage mode, therefore the task of MPPT and bidirectional power transfer is fully managed by the CMC. In grid connected mode, the DC link voltage maintenance is done by CMC, which

is derived from the MPPT controller of individual PV panel/small string connected to each DC link, enabling maximum power harvesting for all times, even during partial shading conditions. The MPP for an individual panel or small string causes PV panels to remain in operation to contribute towards a wider range of power transfer. When the PV power generation is more than demanded power on the DC link, the excess power is transferred to the grid by CMC, under inverter mode of operation. On the other hand, when demanded load power is more than that of PV generation, the deficit power is drawn from the grid source to cater the demand, curbing intermittency full and final. Cascaded structure enjoys the advantage of operation with the low switching frequencies of the H-bridges, thereby improving the efficiency of the system in conjunction with low EMI to produce higher voltage quality at the terminals avoiding the requirement of the filter. Moreover due to low PV voltage at individual DC links, the ratings of switching devices, capacitors will be of lower value, thereby offsetting the cost of a multiplicity of converters.

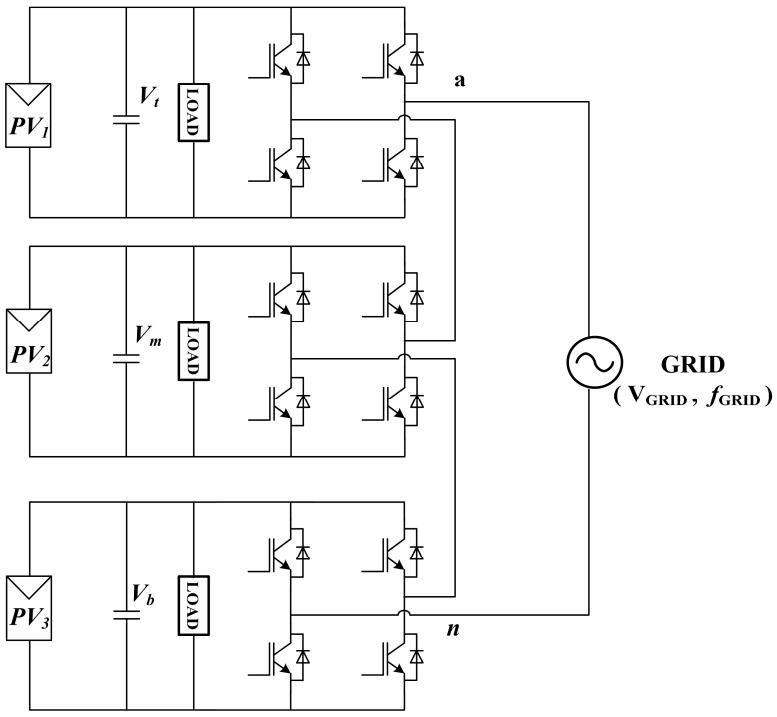


Fig. 1.14: Seven-level PV-CMC system housing various loads on the DC link.

1.7. Controlling of Cascaded Multilevel Topology for PV System

Various control techniques for operation of CMC for different application such as STATCOM, PWM rectification etc. are reported. The issue as raised in sec 1.6.2 has been discussed in many kinds of literature and various control methodologies are proposed for voltage/power balance of individual H-bridge cell. Mainly passivity based control, selective harmonic elimination based control is used for DC bus balancing control.

The reported cascaded PV system utilizes static reference frame based control, using proportional controllers. But such control does not guarantee the error reducing to zero [11]. On the other hand, a controller based on the instantaneous power theory does not guarantee stable operation for the whole range of irradiance levels. So there is need to develop a fast d-q frame based control algorithm for single stage CMC based grid connected system for wide range/depth of operation, particularly for partial shading condition.

1.8. Variety of DC Loads in Residential Power System

With socio and economic pressure focus of society has been shifted towards renewable sources and the use of energy efficient power electronic based equipment. In the present scenario, it is quite visible that a residential load consists of many electronic gadgets and devices but each using its independent rectifier/inverter circuit. This causes unnecessary conversion losses. Mostly device use rectifier as an integral part of their circuit. Since almost all the device needs DC source for their operation a concept of DC nanogrid has evolved. According to this concept, instead of AC distribution network, there should be a network of DC distribution network for residential units to avoid the losses.

A major part of the total energy being utilized in the residential building includes the conventional single phase induction motor for water pumping application due to the availability of single phase supply is the distribution network, knowingly that, such

motors are highly inefficient as compared to 3 phase induction motors. To avert such situation, the single phase AC-DC-3 phase AC conversion has been advocated for motor-pump control using variable voltage variable frequency (VVVF) based drives which maintain a steady excitation of the machine indifferent to the frequency changes in the grid [12]. The major issues with VVVF drive lie with the requirement of high value capacitor on the DC link. Such electrolytic capacitors are very sensitive to heat, and its lifetime reduces to half on every 10° rise in temperature at higher voltages [13]. This thesis work presents a CMC based rectifier (CCAR) unit for splitting single phase to 3 phase to cater open end winding induction motor (OEIM) based pump drive.

Now a day's another type of heavy load is looming around us is that of electric vehicle load. The majority of the reported centralized charging converters works on single full battery stack, which upon aging and repeated charge/discharge cycle may lead to dissimilar characteristics of individual battery units causing imbalance voltage across the units [14]. The probe on the utilization of CMC based integrated Grid to vehicle (G2V), Vehicle to Grid (V2G) and traction converter may be utilized for smartly charging / discharging the split battery stacks with customized rates depending on the SoC's of battery stacks and on feeder loading conditions.

Further, the investigation as done for envisaging the DC links of CMC to act as nanogrids to cater the demand of a variety of composite loads as aforesaid by a single converter/inverter system fed from both PV system and the grid.

1.9. Scope of the work

Looking into the prima facie needs a focused study on the cascaded multilevel based converter/inverter system in off-grid and grid connected configuration with PV and storage system at DC bus for residential applications catering both AC grid side loads and loads connected to different DC links of the multilevel converter is due for investigation. The study also needs to incorporate for exploring various techniques for phase splitting to demonstrate how a single converter/inverter unit may cater to multiphase AC load, DC loads and is utilized for multiple residential purposes. Further suitability for creating

multiple DC nanogrids is also a need to be probed avoiding high step up / step down converter configurations.

Further, the investigation is also due for solutions which minimize the dependency on the grid for feeding various types of the residential loads avoiding the use of multiple numbers of converters. The prime focus should center around the design of the single phase cascaded multilevel configuration and its control algorithm for feasibility with both grid and off-grid mode. Further, the performance needs to be evaluated for utilization with the integration of PV and Battery storage. To enable the fruitful study the system as a whole needs to modeled and simulated to finalize the algorithm for control and management of storage systems with dynamics of loads and sources. And, further prototyping of the same be done to ensure its feasibility, suitability for real life situations. Based on the need of the aforesaid research the attempt has been made in the thesis to develop end to end solution with the systematic approach. The following subsection deals with details of investigations.

1.9.1. Development of 1φ to 3 Φ Voltage Splitter via CMC for Feeding Power to Three Phase OEIM Drive Load

Though single phase supply is investigated in literature for obtaining 3 phases using single common DC link, the CMC configuration may also be probed as voltage splitter to get three DC links for energizing the independent windings of OEIM as a 3 phase.

1.9.2. Development of Appropriate Simulink Model for the Realization of Single Phase CMC for Feeding Variety of Loads

As discussed in the last section, the CMC may be utilized to feed various types of load such as constant power, passive loads, and active loads. For the realization of any control, it is necessary that simulation model is developed before going for hardware implementation.

1.9.3. Derivation of Smart Power Control of CMC Unit for OEIM Pump Drive

Residential pumping system which marks a sizeable load on the grid is generally blind on assessment of peak demand time, while in operation. Such operation if smartly controlled may avoid unnecessary shedding of some connected loads to match power demand. The need of the hour is to work on smart control for CMC to enhance the grid support by flexibly controlling power on the DC links.

1.9.4. Development of Split Battery Charging/Discharging Topology using 1φ CMC Unit for Bidirectional Power Flow

The multiple converter/inverter units with complex control algorithms and space constraint are some of the impediments for modern Plug-in Hybrid Electric Vehicle having multiple numbers of battery units. The CMC based converter is due for deep investigation which is capable of charging/discharging the split battery stacks, as per condition prevailing on the grid.

1.9.5. Derivation of Control Logic for Customized Charging/Discharging of CMC for Life Cycle Improvement of Battery Units

The improved control scheme and closely knitting control algorithm is the necessity for smartly charging/discharging the split battery stacks with customized rates depending on the SoC's of battery stacks and on feeder loading conditions. This not only helps in better resource utilization but further helps in optimum charging/discharging of battery stacks. In addition, some dedicated control needs to be investigated to prevent gasification and other battery related issues.

1.9.6. Derivation of Fast and Decoupled Control Logic for Integration of Separate PV Units on Individual DC links of CMC

The work needs to investigate a staggered PV connection through separate DC links of the cascaded multilevel converter (CMC) for PV-grid tie application utilizing independent MPPT controller.

1.9.7. Development of PV-CMC Control Logic for Ride Through Capability under Dip in Grid Voltage

As per the recent grid code, a thorough investigation is due for PV-CMC configuration and its energy injection control under dip in grid voltage. The decoupled control need to be developed for formulating appropriate ratio of active and reactive power depending upon the voltage sag conditions.

1.10. Organization of Thesis

Following this introductory chapter, the work in this thesis is organized as follows:

Chapter-II: In this chapter, a brief literature review of state of the art PV-CMC technology is presented for residential loads. Further, it also includes the review of various control techniques used for CMC system including voltage balance control. The review of various grid connected PV topologies is also surveyed.

Chapter-III: In this chapter the mathematical modeling of PV cell, array and string are carried out with a set of the equation to approximately match the actual PV panels. Further,an set of analysis for CMC control is derived in the d-q frame to access the feasibility of control algorithm and design the same through a detailed stability analysis. Further to test the bidirectional a capability of the said configuration Li-Ion battery is modeled mathematically to act as load/source. Moreover, through phasor representation, the limit of the DC voltage control is presented to a draw a critical limit of the

unbalanced condition without losing the stability of the system. The OEIM model is also derived in the chapter for implementation of various drive control.

***Chapter-IV*:** In this chapter, CMC structure is being analyzed for its application to feed isolated loads. The topology provides transformerless operation where separate DC links of each bridge are fed from individual PV units. PV units are integrated with incremental conductance (IC) based MPPT charge controllers to extract maximum power at all time of operation. Further on each DC link batteries are also being integrated via a dc-dc converter to compensate for any loss of Power due to low insolation to feed the load constantly.

Chapter-V: In this chapter, the operation and control of 1φ CMC unit feeding OEIMare presented. The CMC structure is controlled to obtain 3 separate DC links, to excite the 3 phase pump load through three single phase bridge H-bridge inverters, one for each winding. The proposed configuration is shown with the merit of having both voltage and power level 1/3rd of the total DC voltage and power, enabling the reduction in the voltage rating of capacitors and voltage stresses. Further, the voltage balance control algorithm is shown to provide immunity against unbalanced DC link voltages across the H-bridges caused due to disturbance from either source and load side, ensuring smooth drive operation. The performance of the system is analyzed through MATLAB simulation and experimental results. The performance demonstrates the effectiveness of proposed control and stability of configuration.

***Chapter-VI*:** In this chapter, CMC structure is analyzed for smart pumping load (SPL) represented for autonomous variable speed pumping system with single phase grid connectivity. The variable speed pumping system is facilitated by 7 level cascaded multilevel active rectifier feeding three DC links working as one end of the back to back connected H-bridges, in turn forming three phase connection to operate the pump as vector controlled OEIM drive. Such variable speed smart pump loads are shown operating as per variation in grid frequency by controlling the power drawn from the AC mains by controlling the speed to control the throughput of the machine. The lab prototype of the proposed SPL unit is developed and integrated with sensors, interfacing circuits, driver etc. for real time implementation. The performance of the system is

analyzed through simulation and experimental results, which demonstrate the effectiveness of proposed control.

***Chapter-VII*:** In this chapter CMC unit feeding open end winding induction motor (OEIM) pump load with Adaline based control is presented to address the challenges and problems under the aegis of the weak grid. Adaline utilizing LMS algorithm extracts the weights of current corresponding to real power and reactive power from source current by fast minimizing the error with respect to a reference generated by unit vectors. The analysis of the proposed configuration and the implemented control is detailed along with the simulated results which are shown in consonance with the experimental results on the developed prototype.

***Chapter-VIII*:** In this chapter, single phase split voltage bidirectional converter is analyzed for both charging (also called Grid to Vehicle (G2V)) and discharging (also called as Vehicle to Grid (V2G)) applications. The proposed converter topology employ CMC with boost converter and use modified droop control scheme by closely knitting control algorithm enabling the system capable of smartly charging (G2V) / discharging (V2G) the split battery stacks with customized rates depending on the SoC's of battery stacks and on feeder loading conditions. Different modes of operation and dynamic response of the proposed control are demonstrated through simulation and hardware results for G2V/V2G to/from the stacks of the batteries clustered in the group of four batteries in each stack.

***Chapter-IX*:** In this chapter reliable, efficient and stable operation of the distribution grid is envisaged using information communication technology appropriately controlling smart parking stations (SPS) for peak saving, valley filling and dynamically customized charging rates for multiple EVs. The proposed SPS caters to solid state split voltage converter units to enable bidirectional power flow control to/from EVs. These units enable G2V / V2G of multiple vehicles based on the SOC's of the batteries and, other characteristics of individual vehicle battery stack and grid condition through supervisory control. Further, these units facilitate customized and cyclic charging of the battery stacks of multiple EVs, averting the problem of blindfolded power exchange form grid. The

cyclic battery stack charging provides stability to the grid and extends the life cycle of the battery.

***Chapter-X*:** This chapter analyzes the CMC structure for the integration of renewable energy. A d-q based control algorithm for single stage grid connected PV system using Cascaded multilevel inverter is presented. Through proper analysis and control, the extent or range for unperturbed grid connectivity upon reduction in reference MPP voltage due to partial shading is also presented in the paper. Under non-uniform insolation on the PV panels, or provide shading conditions, individual DC links even though having voltages different voltage the power at MPP is shown extracted from the set of 4 panels on each link. The proposed controller is also shown capable of taking care of the regulation of individual DC link voltages according to voltage dictated by MPP algorithm. The effectiveness of proposed algorithm and operation is validated through MATLAB simulation and experimental result.

***Chapter-XI*:** In this chapter, the PV-cascaded multilevel inverter system is analyzed under low voltage or voltage sag condition through LVRT capability. The d-q based control is shown to provide efficient independent individual H-bridge control for smartly controlling the active/reactive or both power to support the low voltage or voltage sag and PV panel power condition.

***Chapter-XII*:** In this chapter a brief conclusion of all the chapters are presented. Moreover the chapter also includes the the suggestions for future work.

Chapter IX

SMART PARKING FOR PHEV/EV USING SOLID STATE SPLIT VOLTAGE BIDIRECTIONAL CONVERTER AT UPF WITH V2G CAPABILITY

9.1. General

With established control for EV/PHEV application, control is further tested for bigger horizon i.e. for smart parking application. In this chapter, a smart parking station housing split voltage bidirectional converter for both vehicle battery charging and discharging (for V2G) application with a control scheme for seamless grid integration for Plug-in Hybrid Electric Vehicle (PHEV) is presented. The converter topology is capable of charging/discharging the vehicle batteries with customized rates depending upon each individual vehicles battery stacks condition and grid health condition. Further, during under voltage grid condition the proposed rotating charge control algorithm helps the grid to stabilize its voltage in conjunction with maintaining life cycle of the battery. The scheme is effectively tested both through experimentation on the developed hardware prototype. The prototype is controlled with dSpace-1104 real time controller.

9.2. Features of OEIM Pump Drive using Single Phase Cascaded Multilevel Converter

In this chapter for the efficient, reliable and stable operation of the distribution grid using ICT and smart parking stations (SPS) for peak shaving, valley filling and dynamically customized charging rates for multiple EVs is advocated. The proposed SPS caters to CMC based solid state split voltage converter (SSSVC) units to enable bidirectional power flow control to/from EVs. This SSSVC unit enables charging/discharging or G2V/V2G of multiple vehicles at a time based on the SOC's, other characteristics of

individual vehicle battery stack and grid condition through supervisory control. Further, these SSSVC facilitate customized and cyclic charging of the battery stacks of multiple

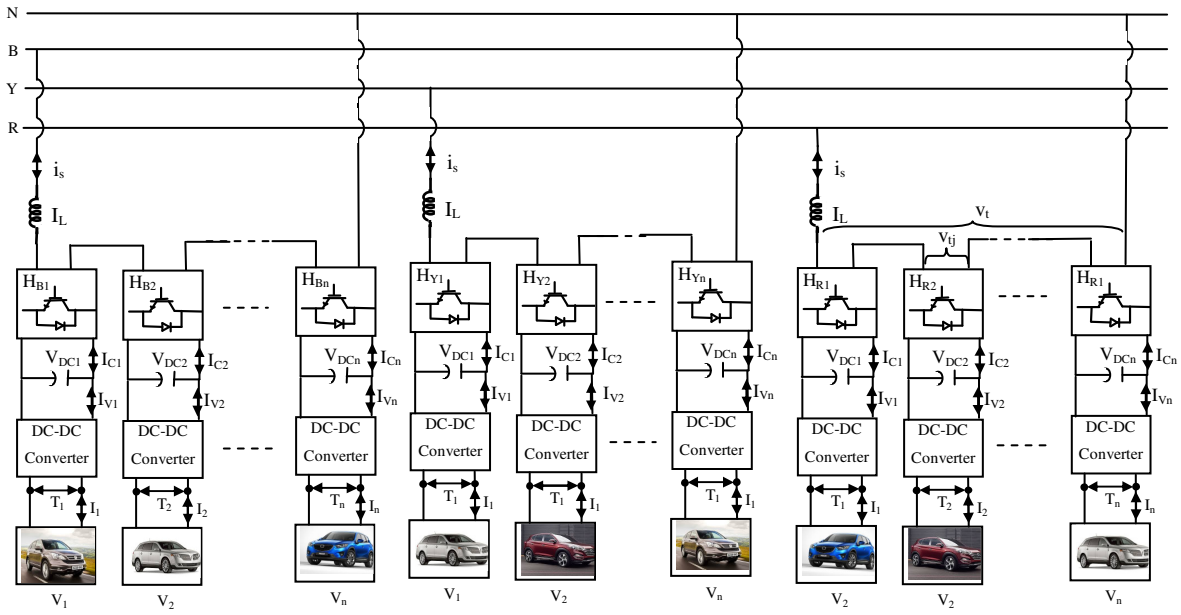


Fig. 9.1: Block diagram representation of SSSVC.

EVs, averting the problem of the blindfolded power exchange form grid. The cyclic battery stack charging provides stability to the grid and extends the life cycle of the battery. The SSSVC units under normal charging/discharging operation transact current at unity power factor. Further SPS becomes very compact due to the absence of a filter, This saves a lot of money as it is not using transformers i.e. bulky and costly and can cater very fast and quick support in case of any contingencies on the grid.

9.3. System Configuration of Single Phase Cascaded Multilevel Converter

Fig. 9.1. shows the schematic of the proposed CMC based 3 phase SPS system housing SSSVC units connected to 415 V, 50 Hz, three phase AC input. Each phase consists of n (HR1, HR1,.. HRn) number H-bridges connected in cascade providing n Independent DC links (VDC1, VDC2…….VDCn). Each independent DC link facilitates customized charging /discharging of individual vehicle battery stacks independently via a DC-DC converter. Each individual vehicle battery stack may consist of similar or dissimilar

SoCs, no. of battery units, AH capacity etc. But each vehicle should have the provision for providing its detailed characteristics of battery stack to facilitate the supervisory control. The overall power that needs to be transacted through SSSVC units for charge/discharge of battery stacks is facilitated through interface inductor of 6 mH connected between 415 V AC supply and SSSVC unit. The DC link capacitance (C) value is decided based on the allowable voltage ripple and power exchange via independent DC link.

9.4. Flowchart for Smartly Charging/Discharging Operation

The detailed flowchart for the decision of charging/discharging of vehicles is represented as in Fig. 9.2 to facilitate proper exchange of power. First, the grid voltage condition is sensed (V_S (K)). Then complete information like DoD, SoC for each of the 3 vehicles (one vehicle connected to each DC link) is collected. Based on the information for each vehicle, cumulative charging/discharging power is calculated. If sensed grid voltage is more than nominal rated grid voltage, then charging for each vehicle has to be done as per the need of the vehicle else rotation based charging control algorithm is initiated to reduce the burden on the grid. It also helps in charging of vehicle without compromising with the life cycle of the battery through reduction of the charging rate.

9.5. Control Logic for SSSVC Operation

The proposed control makes feasible for smart charging/discharging operation of SSSVC without adding any extra hardware. The basiccontrol algorithm for charging and discharging remains same as in last chapter (Fig. 8.5 and Fig. 8.6) of the vehicle through SSSVC unit. The control also embeds DC bus balancing algorithm so that proper power quality is also maintained at a terminal voltage (v_t). The synchronous reference frame (SRF) theory, which is widely advocated for three phase system is altered to suit for single phase system. The source current is assumed to be i_α and it is passed through an orthogonal signal generator to obtain i_β. The unit vectors ($\cos\theta$, $\sin\theta$) are obtained by passing the sensed PCC (point of common coupling) voltage through a fast acting PLL.

By utilizing the unit vectors AC quantities are transformed to DC in SRF using park

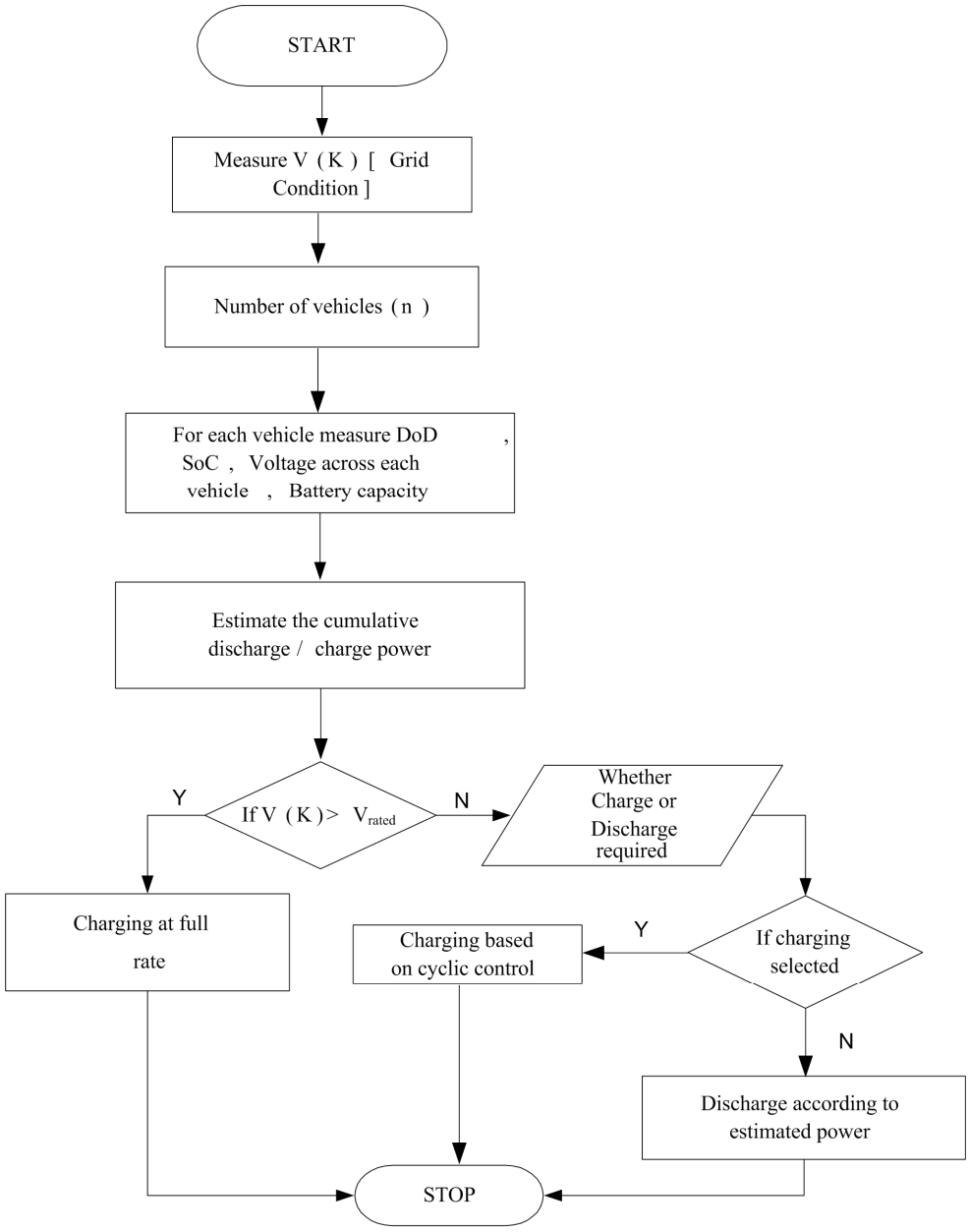


Fig. 9.2: Flowchart for vehicle charging/discharging control of SSSVC unit.

transformation. Assuming source current as

$$i_s = i_{\alpha s} = A.\sin \omega t \qquad (9.1)$$

And assumed imaginary component of source current as:

$$i_{\beta s} = A.\sin(\omega t - \frac{\pi}{2}) \quad (9.2)$$

For vehicle charging reference real component current (I_{ds*}) will have positive magnitude with the assumed direction of vehicle current and its value depends on the combined vehicle charging power demanded by individual battery stacks and for discharging, the reference current becomes negative. In case of charging of vehicle the referenced terminal voltage (V_{t*}) of SSSVC should be less than grid voltage (V_S) to facilitate the charging of a battery of the vehicle (G2V) and vice versa to enable discharging of vehicle batteries for theV2G application.

9.6. MATLAB Based Simulation of PHEV/EV using Solid State Split Voltage Bidirectional Converter

The single phase AC power source, interface inductor, SSSVC and independent battery stacks operated via buck-boost converter are modeled in MATLAB Simulink/Power system block set. To illustrate the multi-mode capability of the presented system, the proper control logic is developed for discharging/charging operation of the small battery stack in conjunction with the cyclic charging of stacks under abnormal grid condition. On each DC link 12 V, 17 AH battery is cascaded to form 48 V battery stack. The SSSVC control logic is verified under varying/uniform battery charging condition, V2G application and for cyclic charging during a dip in grid voltage.

9.6.1. Performance Evaluation of Bidirectional Cascaded Multilevel Converter under Cyclic Control

Fig. 9.3 (a)-(g) shows the waveform of PCC voltage (V_{PCC}), source current (i_s), terminal voltage (V_t), DC link voltages for 3 independent H-bridges (V_{DC}) and battery currents (I_{BT}, I_{BM}, I_{BB}). Neglecting initial transient condition, the analysis is carried out from t=1.5s onwards for SSSVC operation. Hence as aninitial condition, the SSSVC is drawing 7.07A from source (grid) for battery charging as depicted in Fig. 9.3 (b) at

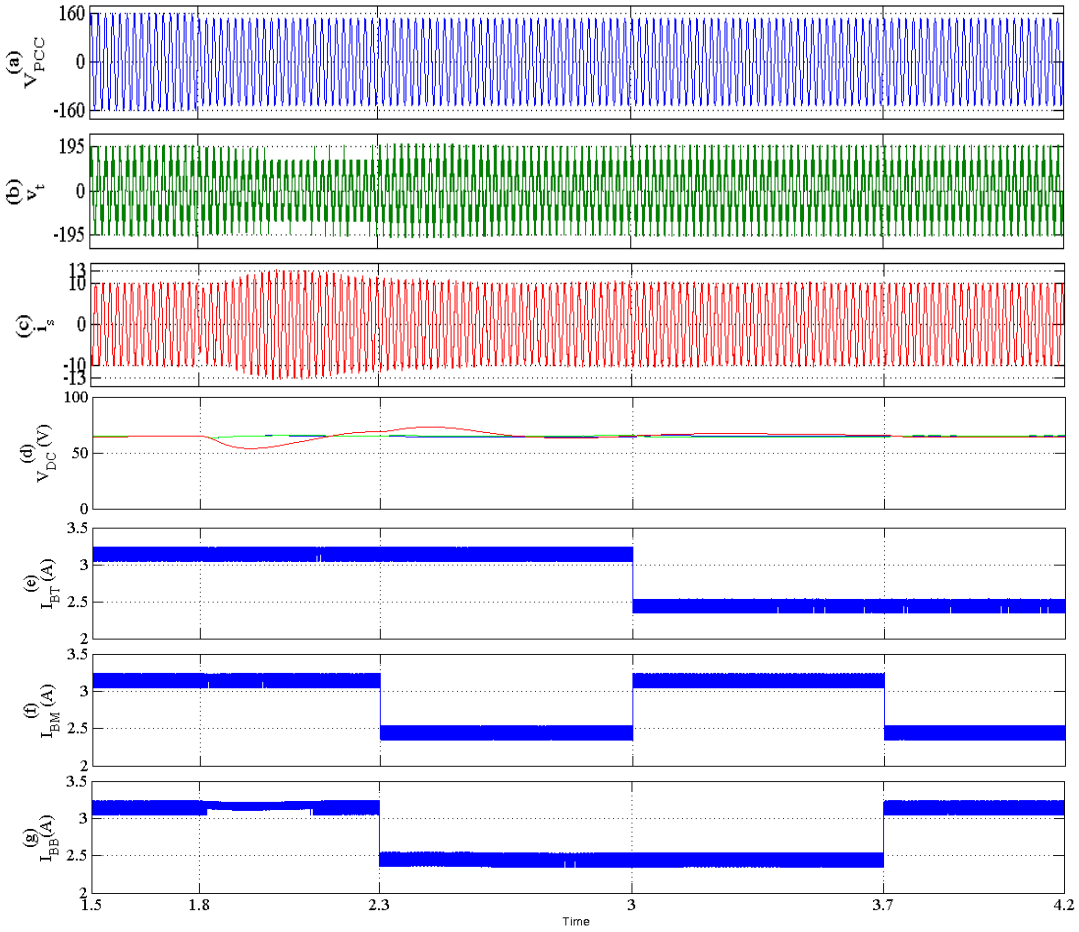


Fig. 9.3: Simulation waveforms of SSSVC unit depicting PCC voltage in volt (V_{PCC}), source current in Amp, terminal voltage in Volt (V_t), battery voltage in Volt (V_{BB}), DC link voltages in volt (V_T), battery charging current in Amp (I_{BT}) under cyclic control.

constant PCC voltage of 110 V. Further, from Fig. 9.3 (d) it is clear that DC link voltages are approximately equal and close to set the value of 65 V. These DC links are further interface with buck/boost converter for charging of batteries stacks at 3.2 A as shown in Fig. 9.3 (e)- (g). Fig. 9.3 (b) shows the 7 level terminal voltage having RMS value being decided as per modulation index and depending on the power required from source for charging of battery stacks. At t=1.8s, a command for a dip in the magnitude of PCC voltage from 110 V to 100 V is initiated as already shown in Fig. 9.3 (a). This causes an increase in demanded source current from 7.07 A to 9.02 A for maintaining same charging current of 3.2 A at reduced PCC voltage as shown in Fig. 9.3 (c). The transition

further causes some displacement of DC link voltage from steady state value of 65 V as in Fig. 9.3 (d). This further aggravates the loading of the grid.

To relieve the grid from such undue stress a cyclic control is initiated at t=2.3s, where each battery is being charged at a full rate during a fixed interval of time and rest other time charging is maintained at reduced current value as shown in Fig. 9.3 (e)-(g). As soon as at t=2.3s the cyclic control starts the source current decreases from 9.1 A to 7.07 A relieving the grid from undue loading condition as shown in Fig. 9.3 (c). Further, it is evident from Fig. 9.3 (d) that DC link voltages remain maintained at 65 V with a slight deviation at t=2.3s.

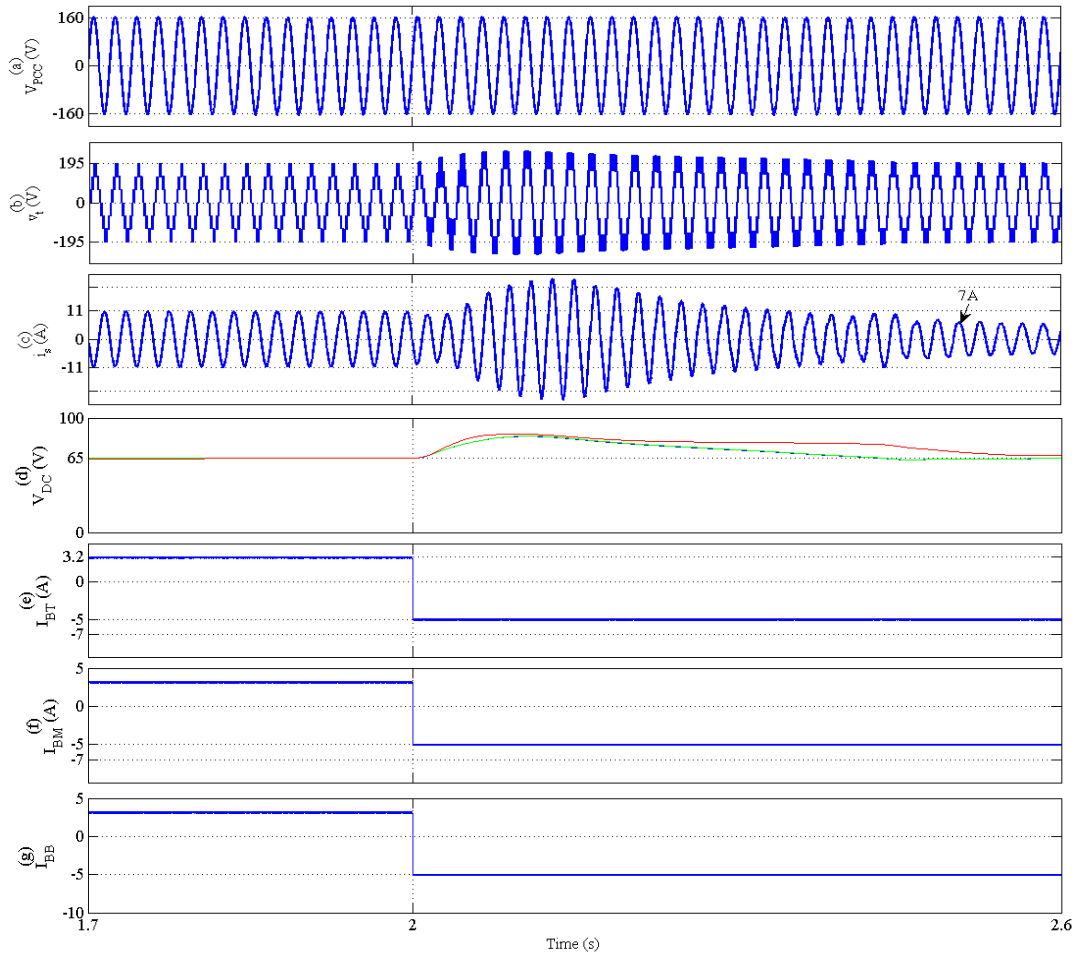


Fig. 9.4: Simulation waveforms of SSSVC unit depicting PCC voltage in volt (V_{PCC}), source current, terminal voltage in Volt (V_t), battery voltage in Volt (V_{BB}), DC link voltages in volt (V_T), battery charging current in Amp (I_{BT}) for transition from charging to discharging mode.

At t=3s, with cyclic control, the middle batteries stack starts charging at full rate at a current of 3.2 A and rest battery stacks at a reduced value of 2.5 A as shown in Fig. 9.3 (e) - (g).Similarly, another rotation in charging happens at t=3.7s.

9.6.2. Performance Evaluation of Bidirectional Cascaded Multilevel Converter with Transition from Charging to Discharging Mode

To evaluate the effectiveness of control algorithm for the transition from charging to charging and vice-versa a further Matlab simulation is done whereat t=2s a transition command is initiated as shown in Fig. 9.4 (a) – (g). Neglecting initial transient condition from t=1.7s to t=2s for are quisite charging current of 3.2 An SSSVC is drawing a current of 7.8 A as shown in Fig. 9.4 (c) with constant 110 V AC supply. At t=2s a command for discharging is initiated at a current of 5 A as shown in Fig. 9.4 (e) – (g). The SSSVC quickly respond to the command and it resulted in swelling of DC buses above 65 V before settling to steady state value gradually as shown in Fig. 9.4 (d). From Fig. 9.4 (c) it is clear that before t=2s, the source current (i_s) is in phase with PCC voltage, but from t=2s onwards under steady state PCC voltage is out of phase with respect to source current (i_s) maintaining UPF operation.

9.7. Hardware implementation of PHEV/EV using Solid State Split Voltage Bidirectional Converter

The same scale/rated hardware prototype of Solid State Split Voltage Bidirectional Converter is developed for evaluation of the control algorithms for meeting the outlined objectives of the present work. The development of hardware prototype includes fabrication of power circuits, a target board hosting DSPIC33FGS502 microcontroller, driver circuits, sensor interfaces and other cards meant for synchronized switching of the power switches. The phase shifted PWM of 2 kHz is generated through three compare units of PWM timers of the DSPIC33FGS502 microcontroller to accurately shifting the carrier by 60° with a requisite hardware interface.

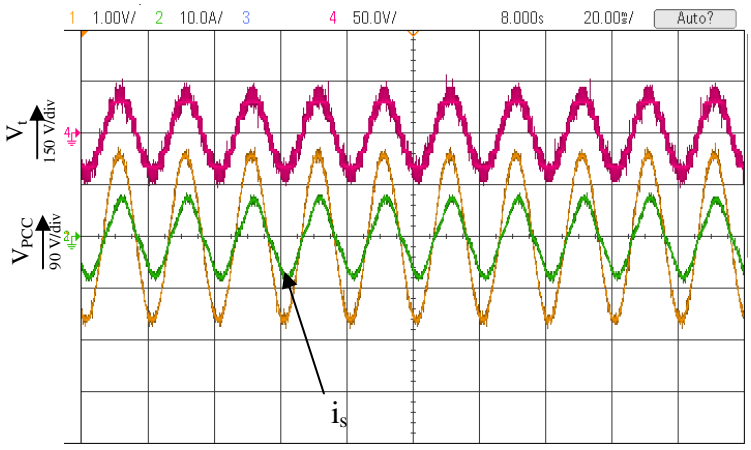


Fig. 9.5: Measured source voltage ($V_{pcc,}$), terminal voltage (V_t) and source current (i_s: 10A/div).

9.8. Result and discussion

The performance of smart parking station (SPS) housing SSSVC is experimentally validated by developing 1 kW lab prototype and tested using 110 V AC with 3 H-bridges in cascade. The SSSVC unit housing SPS station with inbuilt smart discharging/charging control is experimentally validated and various waveforms are recorded using Agilent scopes.

9.8.1. Performance Evaluation of Bidirectional Cascaded Multilevel Converter under Balanced DC link Voltage Condition and Study Dynamic Response with Transition from Charging (G2V) to Discharging (V2G)

Fig. 9.5. shows the source current (i_s) in phase with PCC voltage confirming to the UPF operation. In the same figure, terminal voltage is also shown with stepped seven level voltage waveform. To study the dynamics response of the proposed system, initially the vehicles batteries are being charged at the uniform rate of 1.5 A each as shown in Fig. 9.6. At t=7s, the command for discharging is executed, it results in small rise in DC link voltage, before settling to steady state value of 65 V. Soon the current (battery) reveres to

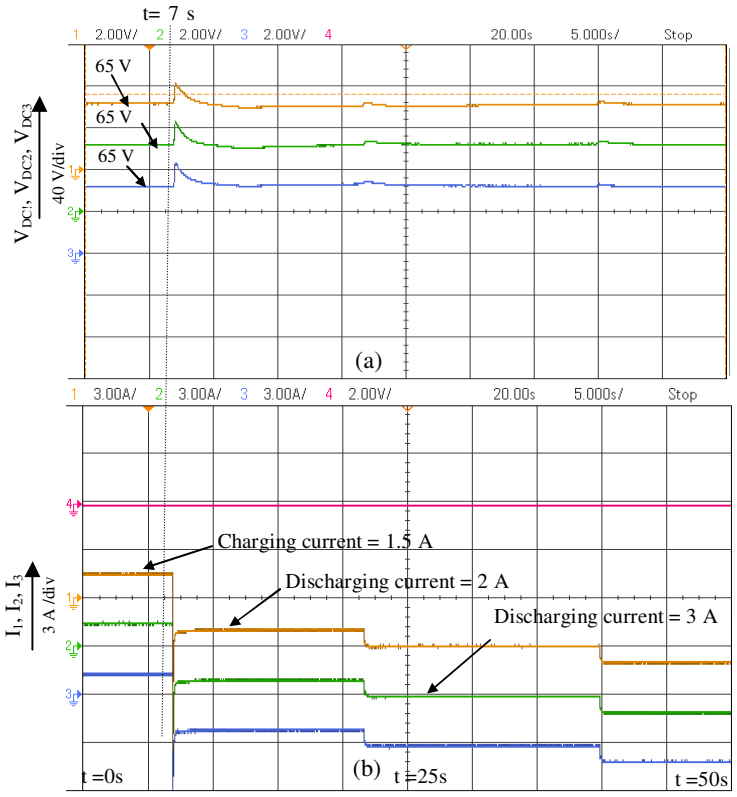


Fig. 9.6: Experimental result showing waveforms for step transition from charging to discharging mode (a) DC link voltages (V_{DC1},V_{DC2},V_{DC3}) (b) Battery currents (I_1, I_2, I_3).

-2A in a very short time which actually acts as a portable source for maintaining grid health condition as shown in Fig. 9.6 (b).

9.8.2. Performance Evaluation of Bidirectional Cascaded Multilevel Converter with Cyclic Control under Voltage Droop

To study the dynamics under droop in grid voltage (V_{PCC}), intentionally the voltage at grid is dropped by 15 V at t=3s as in Fig. 9.7 (a). Accordingly, it may be observed that there is an instant rise in source current (i_s) to cater the same charging current demand (1.5 A). It resulted into disturbances in the DC link voltage also. At t=6.9s, the rotating charging control algorithm is executed and it may see that only i_1 is maintained at 1.5 A after t=6.9s, the rest i_2 and i_3 comes to 1 A. It helps the grid voltage to recover its health condition. If there might be several such SPS then definitely the control algorithm helps in appreciable recovery of the grid voltage. After 1 cycle i_1 and i_3 is reduced but i_2 is

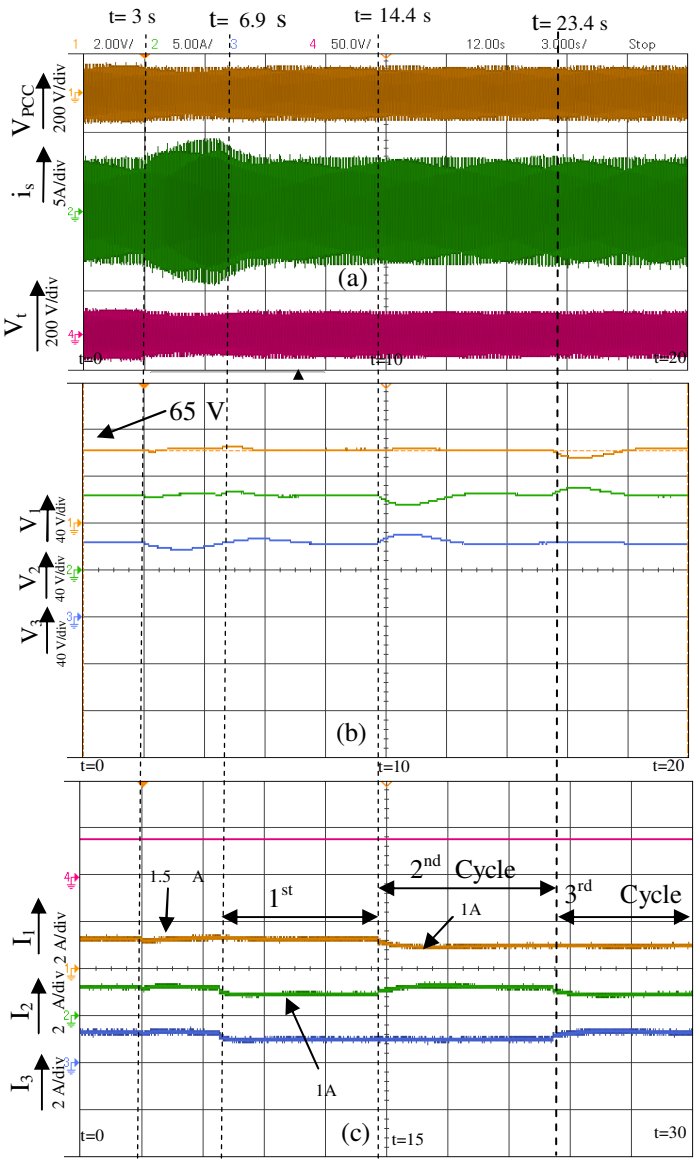
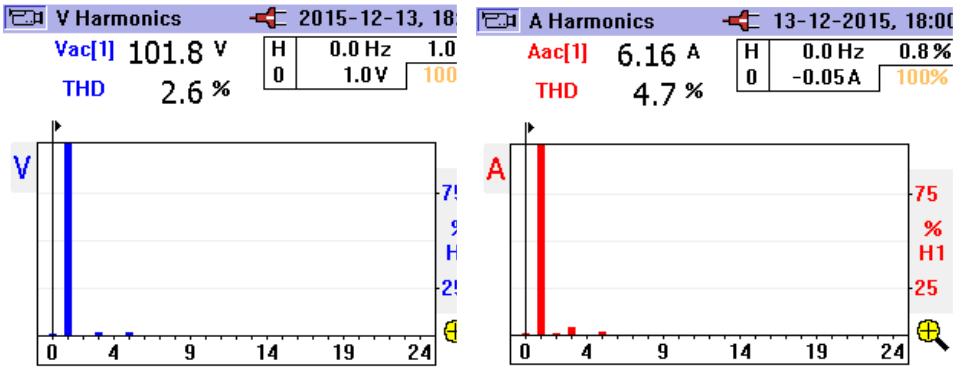


Fig. 9.7: Experimental results showing (a) source voltage (V_{pcc}), source current (i_s) and terminal voltage (V_t) (b) DC link voltages (V_{DC1}, V_{DC2}, V_{DC3}) (c) Vehicle battery currents (I_1, I_2, I_3) for cyclic control of SSSVC.

being charged at full rate. Similarly in the 3rdcycle, i_3 is being charged at full rate and rest at 1 A.

Fig. 9.8 (a) and Fig. 9.8 (b) shows the THD of source current and terminal voltage which is well within limits (4.8 % and 3.2 % respectively) conforming to the IEEE 519 standards.



(a) (b)

Fig. 9.8: (a) Waveform for THD of source voltage (b) THD of source current harmonics for SSSVC.

9.9. Conclusion

The proposed SPS housing CMC based bidirectional unit operation for EV/PHEV is successfully demonstrated through experimental results. The results clearly demonstrate the capabilities of the controller for providing balanced/unbalanced customized charging/discharging rate to battery stacks of the individual vehicle depending on SoC's and grid health condition. The results clearly demonstrate the cyclic battery stack control algorithm to relieve the grid under high demand. The control makes the feasible fast transition from G2V to V2G with a nominal overshoot in DC link voltage without compromising the THD of terminal voltage.

Chapter X

PERFORMANCE ENHANCEMENT OF SINGLE PHASE GRID CONNECTED PV SYSTEM UNDER PARTIAL SHADING USING CASCADED MULTILEVEL CONVERTER

10.1. General

With established Cascaded Multilevel Converter (CMC) based grid connectivity, the PV integration at individual DC link is due for investigation. In this chapter proposes a staggered PV connection through the cascaded multilevel converter (CMC) for PV-grid tie application utilizing independent MPPT controller providing the larger depth of operation under partial shading condition, with smaller filter size and EMI. The proposed topology and its d-q frame control are investigated for performance evaluation of the proposed system. A comparative analysis is also done for the operation of PV under partial shading condition for a conventional PV inverter, two stage string inverter vis-à-vis proposed CMC-based approaches. The performance analysis is demonstrated both through simulation and experimentation.

10.2. Features of Single Phase Grid Connected PV System using Cascaded Multilevel Converter

In this work, a d-q based control algorithm for single stage grid connected PV system using CMC is proposed. Through proper analysis and control, the extent or range for unperturbed grid connectivity upon reduction in reference MPP voltage due to partial shading is also presented in the paper. Under non-uniform insolation on the PV panels, or under shading conditions, individual DC links voltages would be different for extraction of power at MPP from the set of 4 panels on each link. The proposed controller is also capable of taking care of the regulation of individual DC link voltages according to voltage dictated by MPP algorithm. The controller enjoys maximum utilization of PV-

CMC unit for real power transaction of maximum available power, by maintaining grid

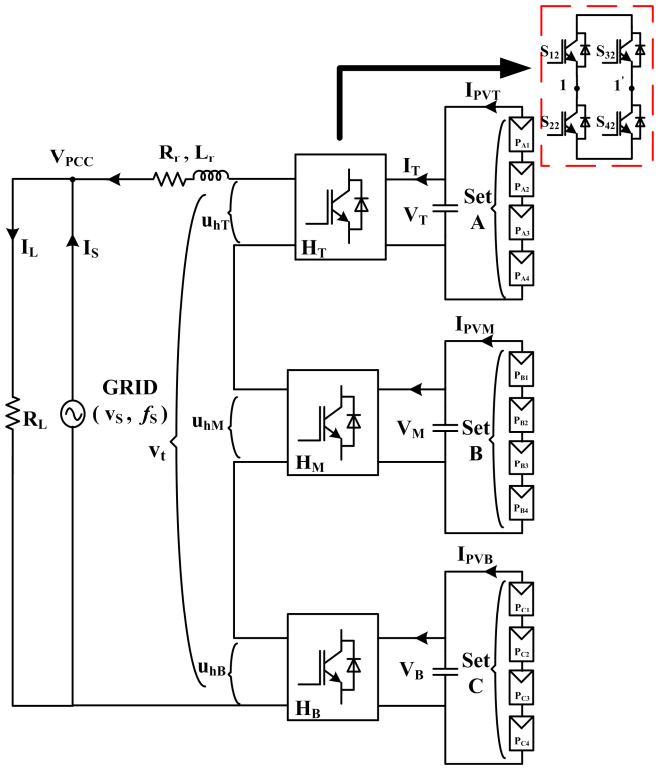


Fig. 10.1: Single Phase single stage PV Cascaded Multilevel converter.

current at UPF with an enhanced range of operation under insolation change and partial shading conditions.

10.3. System Configuration of Single Phase Grid Connected PV System using Cascaded Multilevel Converter

Fig. 10.1 shows the schematic of single phase grid connected CMC unit housing a set 4 PV panels on each DC links namely set A, B and C. Having the advantage of modularity 'n' number of H-bridges may be connected in cascade for having individual MPPT control for PV panel string on individual DC links shows the scalability of the proposed

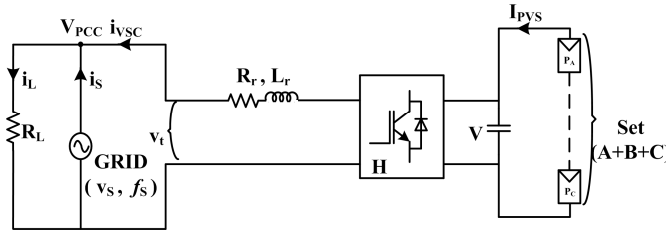


Fig. 10.2: Conventional 2 level single stage single phase VSC-PV system.

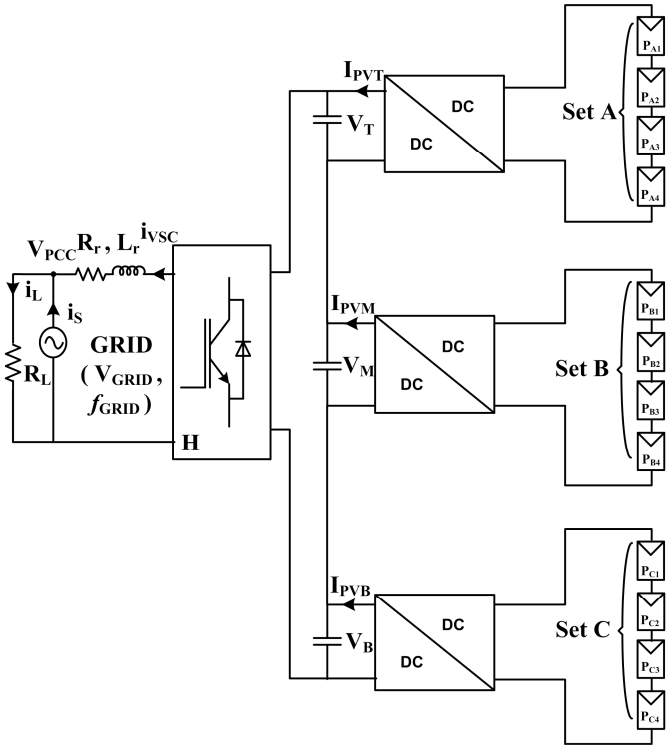


Fig. 10.3: Conventional 2 level double stage single phase VSC-PV system.

system. With the 'n' number of bridges, the output voltage of converter will be of 2n+1 level thus further reducing the voltage THD. In the present work, 3 H-bridges are cascaded to form output of 7 levels. The CMC unit is connected to PCC point via interface inductor (L_r). Resistive load is considered connected at PCC to consume the locally produced power from PV panels. Each DC link capacitor is designed at appropriate value considering the ripple voltage and power transaction across it. DC link is maintained at MPP voltage by the grid, references of which are derived from MPPT controllers at individual DC links. For comparative analysis a conventional 2 level single and double stage VSC based PV system with equivalent number of panels connected as string on DC link is shown in Fig. 10.2 and Fig.10.3.

10.4. PV Panel Sizing

For the present work characteristics of Neosol make TSE 250 PV panel is used for modeling for simulation in MATLAB. The detail for modeling of PV panel is shown in

TABLE 10.1
Parameters of the NEOSOL PV panel (TSE 250) at nominal operating conditions

Number of series connected cell (N_s)	60
Open circuit voltage of module (V_{OC})	38.22 V
Short Circuit Current (I_{sc})	8.70 A
Maximum Power (P_{max})	250 W
Maximum Power Voltage (V_{mpp})	30.46 V
Maximum Power Current (I_{mpp})	8.21 A
Temperature Coefficient of V_{oc}	-0.35 V/K
Temperature Coefficient of I_{sc}	0.05 A/K
Rp	415.405 Ω
Rs	0.221 Ω

Table 10.1. To make it feasible for PV generated power to be transacted to the LV grid (230 V_{rms}), the summation of DC link voltage must be sufficiently greater than peak value 325 V. Further to provide sufficient margin during transients, the modulation index is kept at 0.9. Accordingly, the sum of DC link voltages is kept at 360 V, which is selected by choosing an adequate number of PV panels in a string. For a V_{MPP} voltage of 30.46 V, each DC link shall carry 4 panels to accommodate a voltage of around 120 V,

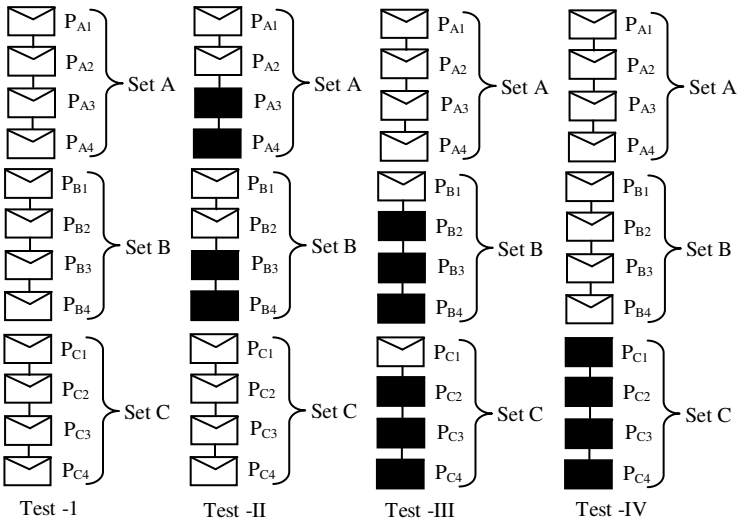


Fig. 10.4: PV panel arrangement for different shading condition.

thus aggregating to 360 V for 3 DC links provided by proposed PV-CMC. PV-VSC system shall accordingly cascade 12 panels in series keeping power at par with PV-CMC.

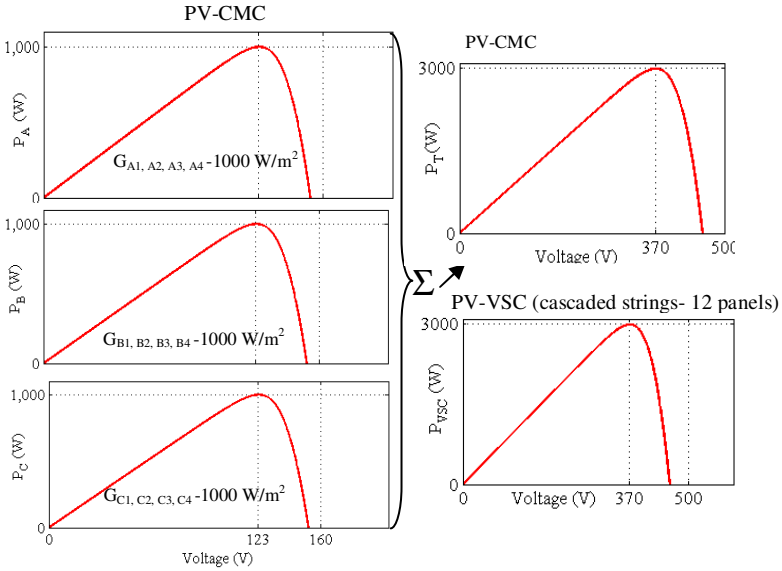


Fig. 10.5: P-V curves for PV-CMC (Individual and combined) and PV-VSC.

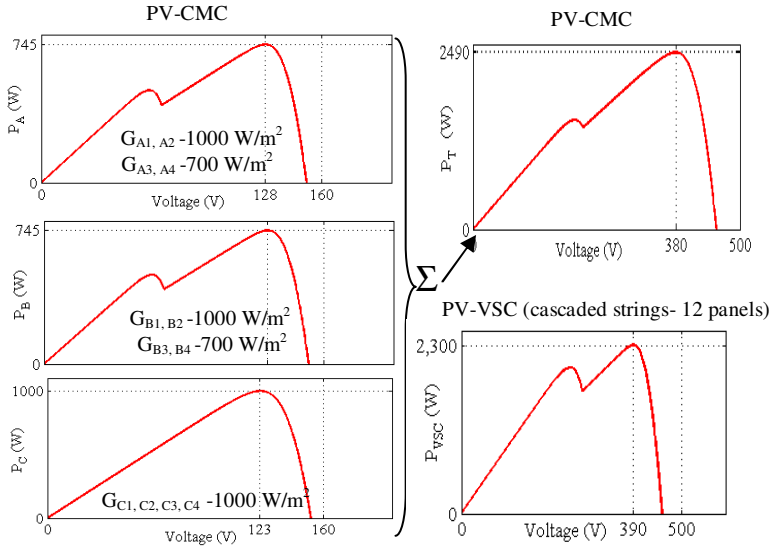


Fig. 10.6: P-V curves for PV-CMC (Individual and combined) and PV-VSC under shading.

10.5. Partial Shading Condition/Non-Uniform Insolation

Particularly in urban areas non-uniform insolation and partial shading condition are very frequent phenomena. To reduce the power loss under such condition, the panels use inbuilt bypass diode. The situation becomes more detrimental and lossy with the use of conventional 2 level VSC connecting a big string of PV panels at DC bus to arrive at a higher voltage for single stage grid connected operation, due to steep fall in voltage at global MPP. For studying the effect partial shading condition on performance of PV-VSC

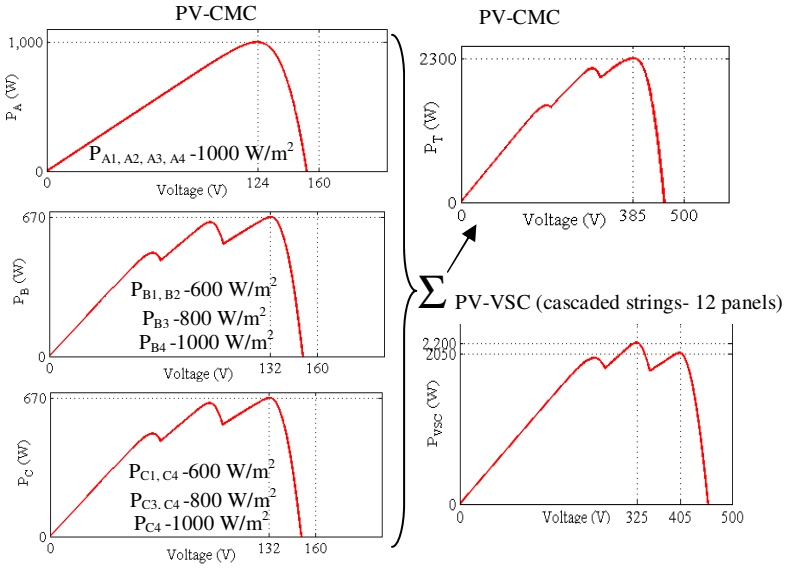


Fig. 10.7: P-V curves for PV-CMC (Individual and combined) and PV-VSC under shading.

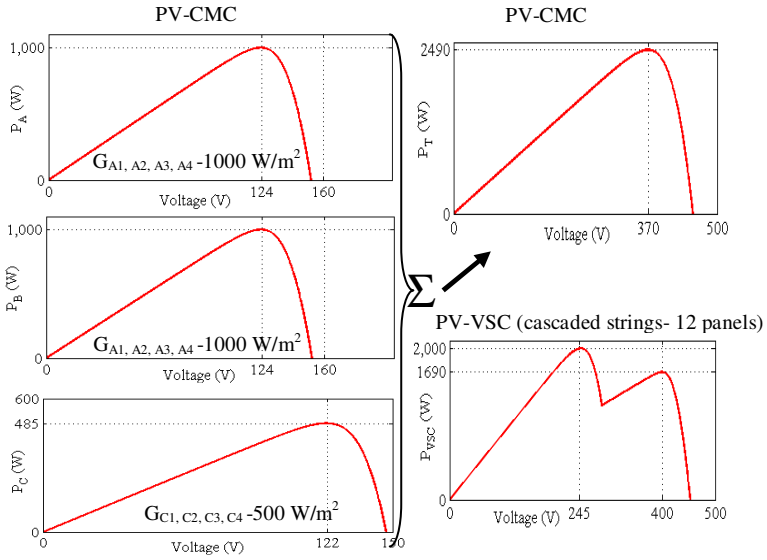


Fig. 10.8: P-V curves for PV-CMC (Individual and combined) and PV-VSC under shading.

and PV-CMC system, a set of four test conditions marked by string Set A, Set B, and Set C is investigated, as shown in Fig. 10.4. For a clear-cut understanding of their performance, P-V curves for PV-CMC system and PV-VSC system under different aforementioned test condition are presented. For lucid depiction, the net output of PV curves for PV-CMC and PV-VSC configuration are reported.

Under test –I condition (shown in Fig. 10.4), all set of PV panels are kept at uniform insolation of 1000 W/m^2 depicted in Fig. 10.5. At individual DC links, a separate MPPT controller is employed for each set of 4 panel string (set A,B,C), accordingly, P-V curves for the individual set is drawn for PV-CMC configuration and added to arrive at the total P-V curve (P_T –V). Under similar insolation levels for set A, B, C in series cascade connection of strings P-V curves are drawn for PV-VSC configuration. From P-V curve under test 1 condition, it may be observed that under uniform insolation, of strings in each set A, B, C the performance of PV-VSC and PV-CMC are at par with each other.

Similarly, test –II condition is shown in Fig. 10.4, for partial shading of two panels, shaded each in set A and set B, reveals two peaks due to two different insolation levels. In Fig. 10.6. the output response of P-V constructed for PV-CMC and PV-VSC reveals that under test 2 condition, the performance of PV-CMC is better than PV-VSC both in terms of the maximum power of 2490 W at 380 V for PV-CMC as compared to 2300 W at 390 V, where both the configuration are capable of remaining connected to the grid.

Under test –III condition as per Fig. 10.4 another set of partial shading condition is applied. The P-V curves of set B and set C show three peaks showing 3 panels partially shaded in each set. The aggregated P-V results clearly show that PV-CMC exhibit far better performance than PV-VSC system. It happens as the maximum power of 2200 W occur at very low voltage of 325 V for PV-VSC at which grid connection/power transfer to the grid cannot be ascertained, as the modulation index would reach to critical value in overmodulation range as shown in Fig.10.7. Whereas, PV-CMC is shown capable of output 2300 W at 385 V as against PV-VSC, which can output 2055 W at 405 V to remain connected to the grid for power transfer, thereby lowering power transfer capability.

With critical test –IV condition, all the panels in a string of set C are partially shaded. The PV-CMC system could only be continue to be operative under such condition outputting at 2490 W at 370 V whereas, PV-VSC can only continue to operate with 1690 W despite having a maximum power of 2000 W occurring at 245 V as shown in Fig. 10.8.

The claim is therefore justified for overall performance of PV-CMC with higher throughput as compared to PV-VSC particularly under partial shading condition. It will offset the marginal escalation of cost due to an increased component in light of accelerated payback. The control algorithm for operation of CMC with MPPT operation is discussed in subsequent chapters.

10.6. Control Theory for PV-CMC Operation

To facilitate proper transfer of generated power, a d-q based control strategy is incorporated into single phase PV-VSC and PV -CMC VSC. Unlike the centralized MPPT controller in two level PV-VSC system, the individual MPPT controller of each set of 4 panels provides separate MPP reference voltage as shown in Fig. 10.9. These reference voltages of the individual set of PV panels are added and compared with actual DC link voltages of individual H- bridges and the error are processed through PI controller to arrive at reference d-component i_{CMC}^{*}. The reference value has to be supplied through CMC for maintaining referenced DC link voltage. Further referenced current component is compared with actual PV-CMC output current and processed properly to get d-component of terminal voltage after adding the feedforward component as shown in Fig. 10.9. Similarly, for UPF operation, the q component of the referenced current is set to 0, to arrive at the requisite voltage for appropriate transfer of power.

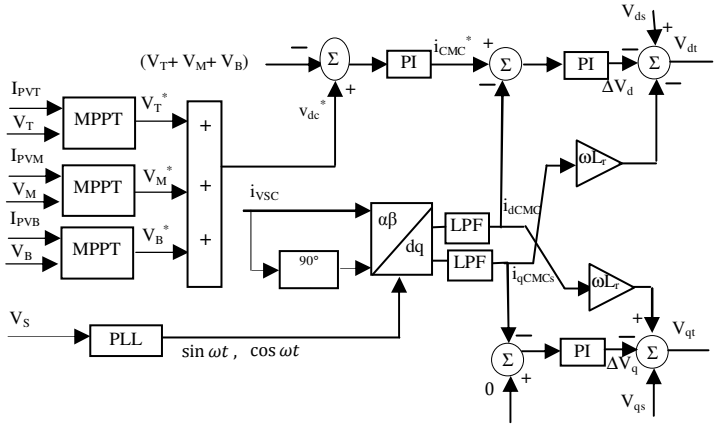


Fig. 10.9: Control blocks of proposed PV-CMC Configuration.

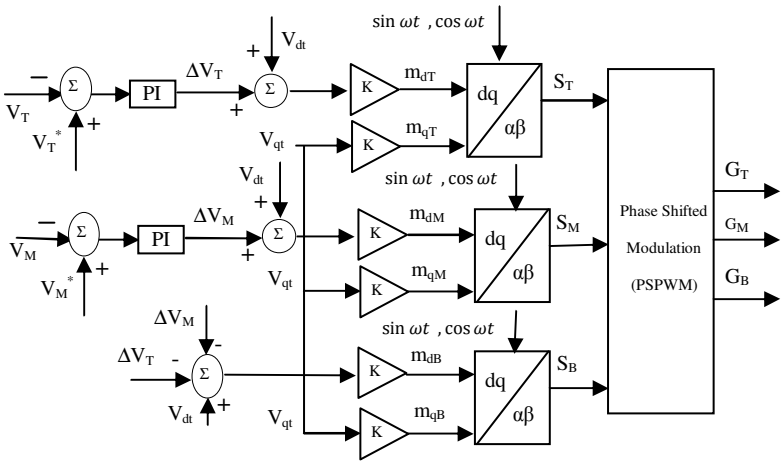


Fig. 10.10: Control blocks for individual MPPT control of the proposed PV-CMC Configuration.

Since only single phase source is available, the CMC current (i_{CMC}) is considered as i_α component and orthogonal components is obtained by delaying the $i_{VSC}$by 90° contributing to i_β component as a virtual component for park transformation as shown in Fig.10.9.

Due to multiple DC links in PV-CMC configuration, each having a set of PV panels under varying/different insolation, the referenced DC link voltage may be different for each level. If this situation is not properly compensated for different MPP voltage at individual DC links, the individual set of 4 panels at each DC links will no longer be in a position to generate the power corresponding to MPP point. To avoid such condition, the inner voltage control loop is being embedded which sets the individual DC link voltage commanded by MPPT controller. Fig. 10.9. shows the control logic for remediation to

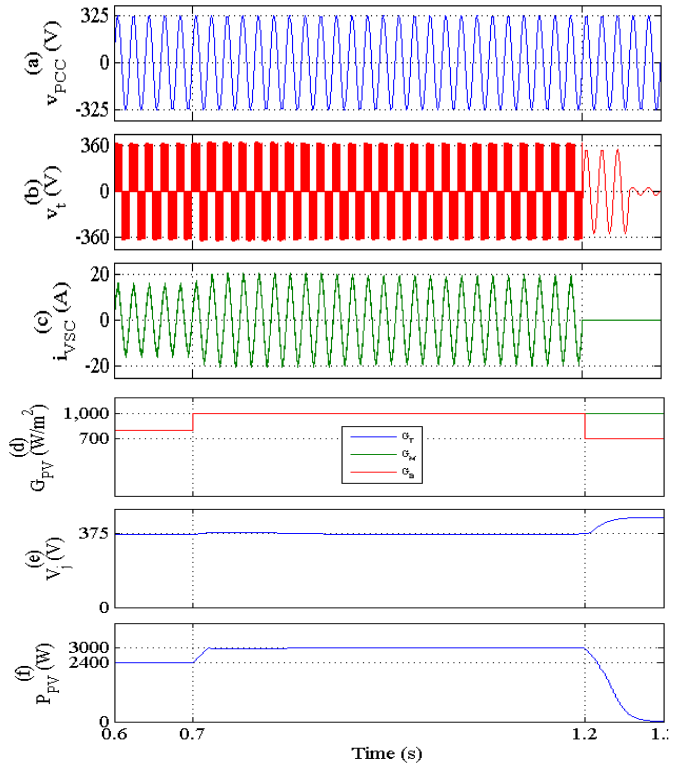


Fig. 10.11: Simulation results of single stage 2 level VSC showing (a) source voltage (V_{pcc}) (b) VSC terminal voltage (V_t), (c) source current (i_{VSC}), d) Insolation (G_j) (e) DC link voltages (V_{DC}) (f) PV power (W).

enable desired control. After proper compensation as per insolation conditions, the reference modulation switching function (S_T, S_M, S_B) is used for PSPWM as in Fig.10.10.

10.7. MATLAB Based Simulation of Single Phase Grid Connected PV Multilevel System

The 2 level single stage and double stage VSC topology and the proposed PV-CMC unit are simulated under MATLAB Simulink environment and later results are compared.

10.7.1. Performance Evaluation of 2 Level Single Stage PV-VSC

The various results and waveforms for PV-VSC unit neglecting the initial transient condition are shown in Fig. 10.11. From t=0.6s onwards till t=0.7s uniform irradiance of 800 W/m^{2}is maintained on each 3 sets (set A, set B, set C) having 4 PV panels in each as in Fig. 10.11 (d). At 800 W/m^2 insolation level, the MPP extracted power is 2400 W at DC link voltage of 370 V as clear from Fig. 10.11 (e)-(f) confirming to P-V characteristics at 800 W/m^2. It is seen that current (i_{VSC}) is in phase with PCC voltage maintain UPF operation and delivers power to the grid with 9.2 A of output VSC current as in Fig. 10.11 (a)-(c). At t=0.7s irradiance level is changed uniformly for all 3 sets to 1000 W/m^2 as clear from Fig. 10.11 (d). With the change in insolation, the MPP extracted power to reach to new MPP point of 3000 W as shown in Fig. 10.11 (f). This further leads to change in output VSC current 9.2 A from 13.2 A as in Fig. 10.11 (c). The insolation also results in displacement of DC link voltage from steady state value and finally reaches to new steady state value dictated by MPP controller. At t= 1.2s, a situation for partial shading condition is created as discussed earlier in modeling section. With two set remains at 1000 W/m^2 and other at 700 W/m^2 leads to new MPP point as

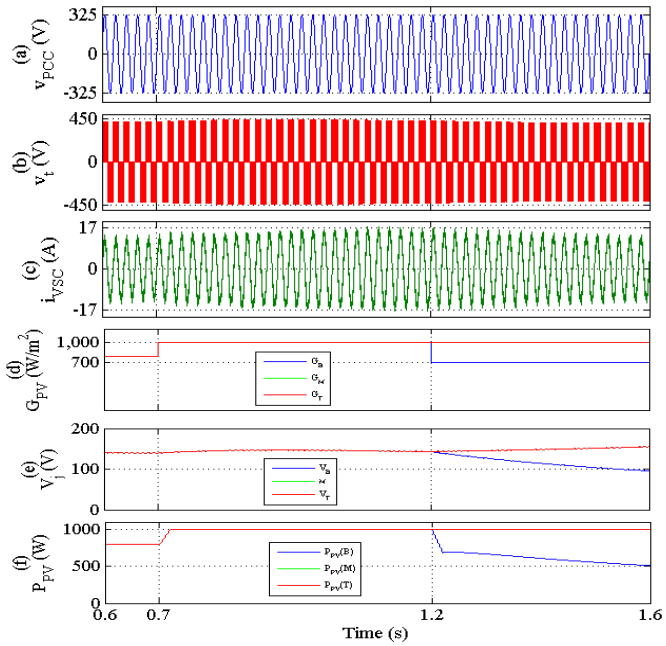


Fig. 10.12: Simulation results of double stage 2 level VSC showing (a) source voltage (V_{pcc}) (b) VSC terminal voltage (V_t), (c) source current (i_{VSC}), d) Insolation (G_j) (e) DC link voltages (V_{DC}) (f) PV power (W).

dictated by the controller. The new MPP point has reference DC link voltage of around 245 V, i.e. well below the 325 V. The reduction in MPP voltage leads to complete shutdown of the VSC unit even though there is the availability of sufficient power at an individual set of PV panels as in Fig. 10.11 (b)-(f). The shutting down of VSC, the panel voltage starts moving towards open circuit voltage (V_{OC}).

10.7.2. Performance Evaluation of 2 Level Double Stage String PV-VSC

Similarly, PV-VSC for 2 stage string topology is simulated in MATLAB Simulink environment and the results are shown in Fig. 10.12. Operation consideration remains same till t=1.2s as discussed for single stage topology. At t=1.2s, the same level of partial shading condition is applied by changing the insolation at one set of PV panels. In spite of shading on one panel set, the other 2 sets of panels contribute towards the generation of power to the grid even with stiff DC bus voltage as shown in Fig. 10.12 (d) – (f) as compared to single stage topology where the system gets shut down completely.

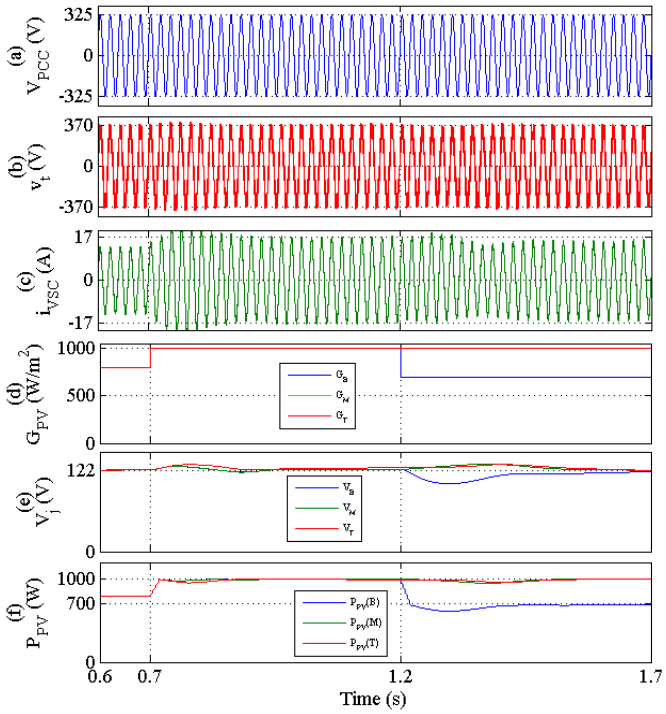


Fig. 10.13: Simulation results of single stage CMC showing (a) source voltage (V_{pcc}) (b) VSC terminal voltage (V_t), (c) source current (i_{VSC}), d) Insolation (G_j) (e) DC link voltages (V_{DC}) (f) PV power (W).

But since each independent string are connected in series at DC link, there will be a common DC current, providing flexibility in DC bus voltage is available, the unshaded panel may be displaced from MPP point to accommodate inception of the shaded panel. Such complex and tedious control are difficult to implement and it also decimates the efficiency of VSC. Even though with loss of power generation from one string, other two strings are transferring the generated power to the grid by appropriately boosting the voltage to reach the level of the reference DC link voltage (assumed sum of individual DC voltage of each DC-DC converter, $V_T + V_M + V_B$). From Fig. 10.12 (e), it is clear that as the power and voltage contribution from shaded string decays steadily whereas the individual output voltage of DC-DC converters (unshaded string) rise together to reach the reference voltage. Though stresses on switches of DC-DC converter get increased in this topology, there will be more power transfer as compared to centralized single stage topology.

10.7.3. Performance Evaluation of Proposed Single Stage PV-CMC

Similarly, the PV-CMC unit is simulated under MATLAB Simulink environment and results and waveforms are shown in Fig. 10.13. Between t=0.5s to 0.7s, insolation is maintained at 800 W/m^2 as in Fig. 10.13 (d). Fig. 10.13 (e)-(f) shows, the individual DC link voltage, and MPP extracted power via each H-bridge. DC link voltages are at some voltage as dictated by individual MPP controller. To transfer the overall PV power to the grid, the terminal voltage (v_t) is maintained at a higher voltage with 7 level stepped waveform as in Fig. 10.13 (b). At t=0.7s, insolation changes which further increase in output of CMC current from 9.2 A to 13.2 A. At 1.2 s under partial shading condition, with one set of PV panel at 700 W/m^2cause a dip in DC link voltage of bottom H-bridge (V_B) as in Fig. 10.13 (e). But slowly DC link recovers at t=1.4s to the reference MPP voltage as dictated by the controller. With lower insolation, the PV extracted power also gets affected and is reduced to 475 W as shown in Fig. 10.13 (f). So even though with partial shading condition, the PV-CMC is capable of sending power to grid against 2 level VSC where PV power generation gets halted under such odd situation, unless the DC link voltage is made flexible.

So under partial shading condition, the PV-CMC outshines the single and double stage topology for enhanced power transaction to the grid. The capability of maneuvering the voltage phasor, and thereby controlling the real and reactive power gives PV – CMC a clear edge over its competitors particularly under partial shading condition as already discussed with reference in Fig. 10.13. Moreover, THD at terminal voltage is also low compared to conventional two level VSC, enhancing the power quality.

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10.8. Hardware Implementation of Single Phase Grid Connected PV Multilevel System

The same scale/rated hardware prototype of single phasegrid connected PV multilevel system is developed for evaluation of the control algorithms for meeting the outlined objectives of the present work. Each DC link is connected to 2 PV panels. The prototype is tested with a source voltage of 80 V. dSPACE 1104 real time controller and DSPIC33FJ16G502 microcontroller are used for implementing the control of PV-CMC. The LEM LV25P and ABB EL 25 P1, hall effect voltage and current sensors are employed for sensing the voltage at PCC, individual DC links of CCAR and source side current of CCAR respectively. The sampling frequency of simultaneous sampled ADC channels is kept at 10 kHz, which also corresponds to real time compilation loop of dSPACE 1004 real time controller. The phase shifted PWM of 2 kHz is generated through three compare units of PWM timers of the DSPIC33FGS502 microcontroller to accurately shifting the carrier by 60° with a requisite hardware interface.

10.9. Result and Discussion

The developed hardware prototype is tested for both steady state and transient conditions. For evaluating transient performance under partial shading condition a portion of the PV panel is shaded and the other transient is studied for perturbation of loads at DC links. Experimental waveforms are recorded using Agilent DSO 2014A and fluke 345 power quality analyzer for evaluation of the performance of the proposed PV-CMC unit.

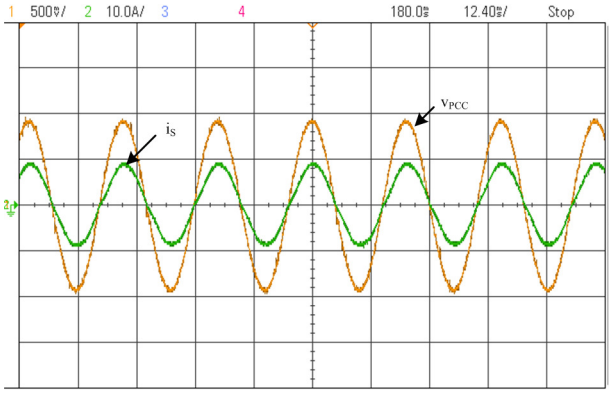


Fig. 10.14: Experimental results showing CMC output current (i_s- 10 A/div) in phase with PCC voltage (V_{PCC} – 135 V/div).

10.9.1. Performance Evaluation Single Phase Grid Connected PV Multilevel System for UPF Operation

For maximizing the real power transfer to the grid the CMC output is maintained in phase with the PCC voltage as shown in the trace of the DSO in Fig. 10.14. Further to judge the quality of the terminal voltage, a stepped 7 level output terminal voltage is shown together with PCC voltage and current to access the performance of the CMC system as in Fig. 10.15.

10.9.2. Performance Evaluation of Single Phase Grid Connected PV Multilevel System When One set of Panels is Under Partial Shading Condition

Simultaneously triggered three DSO's are used to record the dynamics of the AC source side parameters, DC link voltages and PV currents (as dictated by MPPT controller) as shown in Fig. 10.16 (a), Fig. 10.16 (b), and Fig. 10.16 (c) respectively. To analyze the transient performance of PV-CMC unit initially the system is started with uniform insolation level as shown in Fig. 10.16. But due to non-uniformity in the performance of the PV panels and non-uniform dust deposition, individual DC links receives 5.1 A, 3.8 A and 4.1 A, are the same as shown in Fig. 10.16 (c). Due to this, dissimilar outputs are depicted as varied MPP voltage i.e. 52 V, 54 V and 53V respectively on individual three

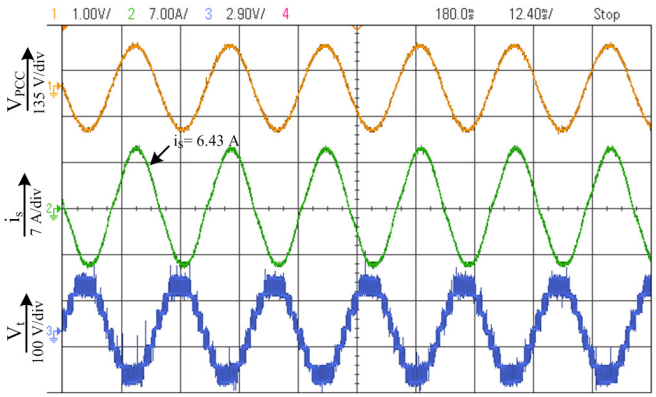


Fig. 10.15: Experimental set up of PV- CMC PCC voltage, output current (i_s- 10 A/div), terminal voltage (V_{PCC} – 100 V/div).

DC links. From Fig. 10.16 (c) it is also clear, that PV power harvested at the top DC link is around 220 W, and the total generated PV power is around 600 W which is utilized to feed some passive loads connected to the DC links and remaining for transfer to the grid.

At t=0.36s, the transient is created by shading some portion of one panel connected to the DC link of the top bridge. As soon as the portion is shaded, there is a sudden dip in top DC link voltage i.e. from 52 V to 35 V due to bypassing of some the cells, as shown in Fig. 10.16. This has resulted into a dip in PV current too i.e. from 5.1 A to 3.8 A and power generated from PV panels from 220 W to 180 W. From experimental results it is also clear that with a disturbance at one PV units, it actually displaces other DC links from MPP point as H-bridges are connected in series. From Fig. 10.16 (b) it may be observed that DC link voltage of middle H-bridge has increased from 54 V to 58 V and lower DC link from 53 V – 57 V before settling to MPP voltages. The experimental results show the similar trend as shown by the simulation results, validating the performance comparison established through the simulation.

10.9.3. Performance Evaluation of Single Phase Grid Connected PV Multilevel System with Load Perturbation on DC links

Further to test the dynamic performance of the PV-CMC system another set of experimentation is performed, where the transient condition is created by switching off the loads connected the DC links as in Fig. 10.17. Till t=0.47s the conditions on the panel remains the same as mentioned for before the partial shading was done. Equal loading of

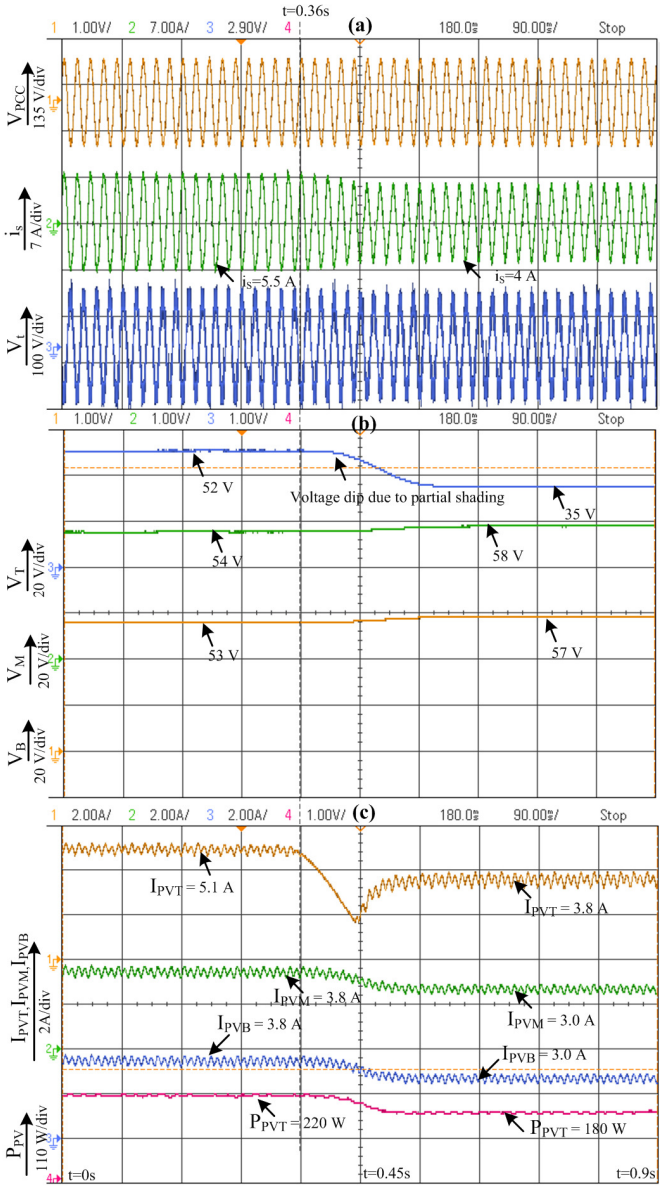


Fig. 10.16: Experimental results showing partial shading scenario (a) PCC voltage, VSC current, terminal voltage (b) DC link voltages of CMC unit dictated by MPPT controller of PV system (c) PV MPP dictated currents, MPP referenced PV power of single PV set connected at the top DC link.

40 Ω is connected to each DC link. At t=0.47s, the connected loads on each DC link are disconnected. This resulted into dislodging of the reference voltage from MPP point causing a decrease in PV power and generated current at each DC links as shown in Fig. 10.17 (c). The switching of the loads also causes an increase in currents fed to the grid from initial 4.5 A to 5.5 A. In order to depict clearly the transients the interval of observations are kept upto t=0.9 s in Fig. 10.17 (b). However, steady state of generation

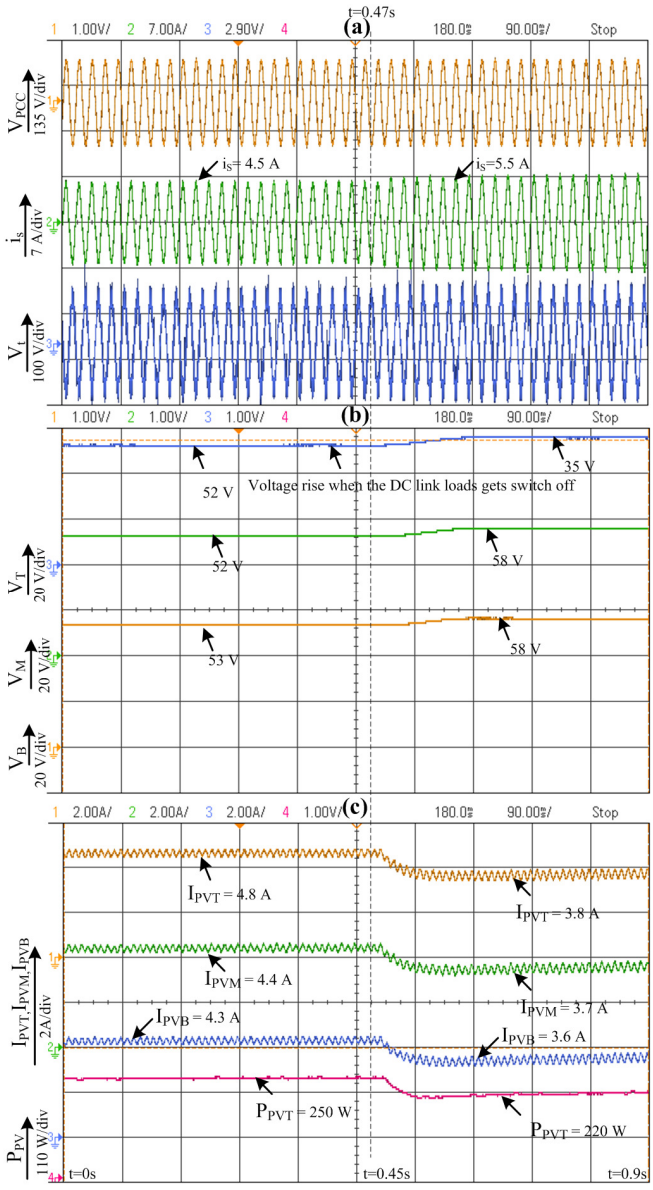


Fig. 10.17: Experimental results showing transients under DC link Load perturbation (a) PCC voltage, VSC current, terminal voltage (b) DC link voltages of CMC unit dictated by MPPT controller of PV system (c) PV MPP dictated currents, MPP referenced PV power of single PV set.

is returned in 1.8s. The steady state the DC link voltage again settles to MPP dictated reference point. Fig. 10.18 which depicts the individual PV currents guided through MPPT. Fig.10.19 shows the PV panels having partial shading condition.

Fig. 10.20 shows the THD of output grid current and terminal voltage which is well within limits (3.9 % and 2.0 % respectively) conforming to the IEEE 519 standards. Waveform of Fluke 345 power analyzer is also shown in Fig. 10.21 depicting power

supplied by CMC prototype unit. From waveforms, it is further clearly illustrated that source current is maintained at UPF.

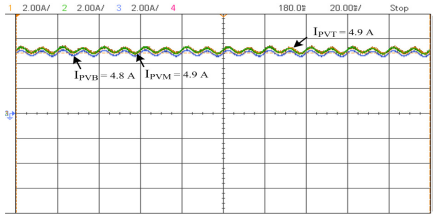
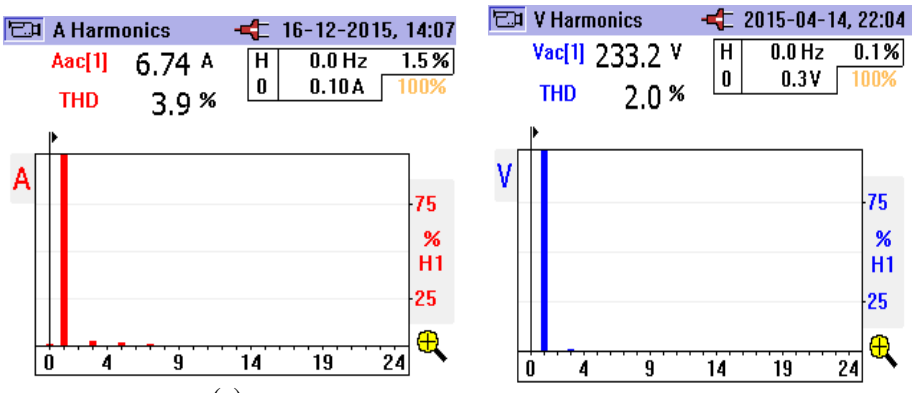


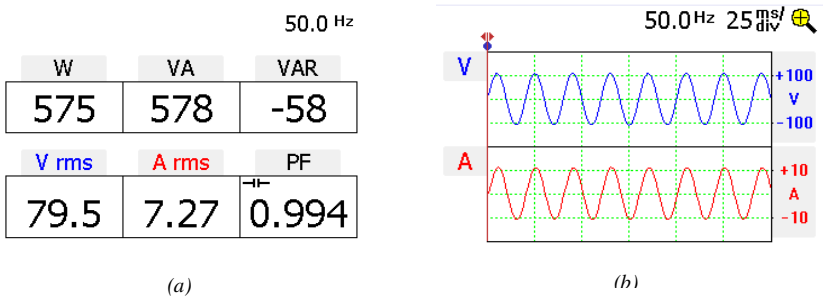
Fig. 10.18: Experimental results showing MPP dictated PV currents.

Fig. 10.19: Rooftop PV panels showing partial shading condition.



(a) (b)

Fig. 10.20: (a) Waveform for THD of source current harmonics, (b) THD of CMC terminal voltage $v_{t.}$.



(a) *(b)*

Fig. 10.21: Fluke 345 waveform showing (a) Power transaction through grid, (b) Grid voltage and current.

10.10. Conclusion

The enhanced performance of PV-CMC over single and double stage PV-VSC system during partial shading condition is established both by simulation and experimentation results. The effectiveness of the control algorithm under influences of dynamic and uneven insolation across the bridges is clearly demonstrated through results. The comparative performance presented clearly shows the advantages of using proposed topology over conventional one. Despite varying insolation condition, the DC link voltage of individual H-bridge is maintained at voltage dictated by MPP and current transacted through CMC is maintained at UPF ensuring improved power quality operation. The proposed structure and algorithm have the advantage of modularity, greater depth of operation so as to provide better grid connectivity and meets the requirement of partial shading condition/varying insolation.

Chapter XI

LOW VOLTAGE RIDE THROUGH CAPABILITY OF PV-GRID CONNECTED CASCADED MULTILEVEL INVERTER THROUGH MULTIMODE OPERATION

11.1. General

In this chapter an investigation into the enhanced operation of cascaded multilevel inverter based PV (CMIPV) system in compliance with grid code under perturbed voltage condition at PCC, viz, voltage sag by robust control demonstrating low voltage ride through (LVRT) capability is presented. The decoupled methodology provides an efficient and independent control of individual H-bridges for active/reactive power or both to support the grid depending on the voltage sag and / or the availability of power output from the PV panels. Moreover, an algorithm for operation of CMIPV capacity limited control under voltage sag condition is discussed in detail. The performance of the proposed configuration and control is investigated both through MATLAB simulation and experimentation. For performance evaluation, intentionally the experiment work has been done on actual PV panels, so as to study its exact behavior in practical scenario.

11.2. Features of Low Voltage Ride Through Capability of PV-Grid Connected Cascaded Multilevel Inverter through Multimode Operation

German grid code for PV system has been adopted as the guiding principle for dealing with a disturbance on the distribution network. The applicability of the same is proposed for single stage CMIPV system. Through proper analysis and control, a different mode of operation of CMIPV under constant current, constant active power, and constant apparent power load is investigated with reference to state of the art grid code. The control logic is developed devising the displacement of an operating point from MPP point under

perturbed voltage levels at PCC is also probed. The proposed controller is also investigated for demonstrating the capabilities of taking care the regulation of individual DC link voltages according to the voltage dictated by MPP algorithm and or guided by grid codes respecting the capacity of the inverter system. The controller ensures the maximum utilization of CMIPV unit for real power transaction out of maximum available power, by maintaining grid current at appropriate power factor with an enhanced range of operation under insolation changes and partial shading conditions. The effectiveness of proposed algorithm and operation is validated through MATLAB simulation and experimental results.

11.3. System Configuration of PV-Grid Connected Cascaded Multilevel Inverter for LVRT Capability through Multimode Operation

Fig. 11.1 shows the schematic of single phase cascaded multilevel inverter based PV (CMIPV) unit housing a set of 4 PV panels on each DC links namely set A, B, C. Having the advantage of modularity 'n' number of H-bridges may be connected in cascade for

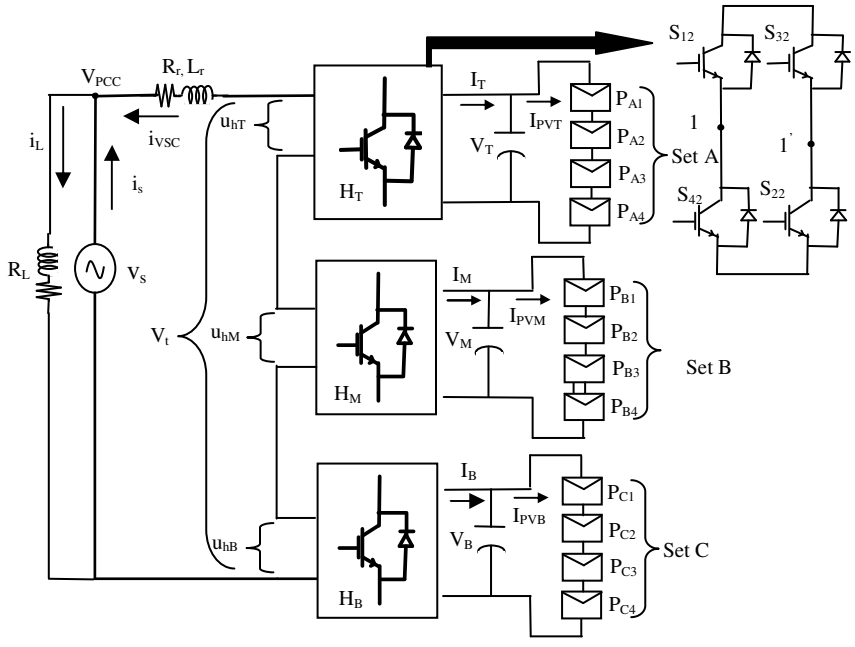


Fig. 11.1: Single Phase cascaded multilevel inverter based PV (CMIPV) system under LVRT.

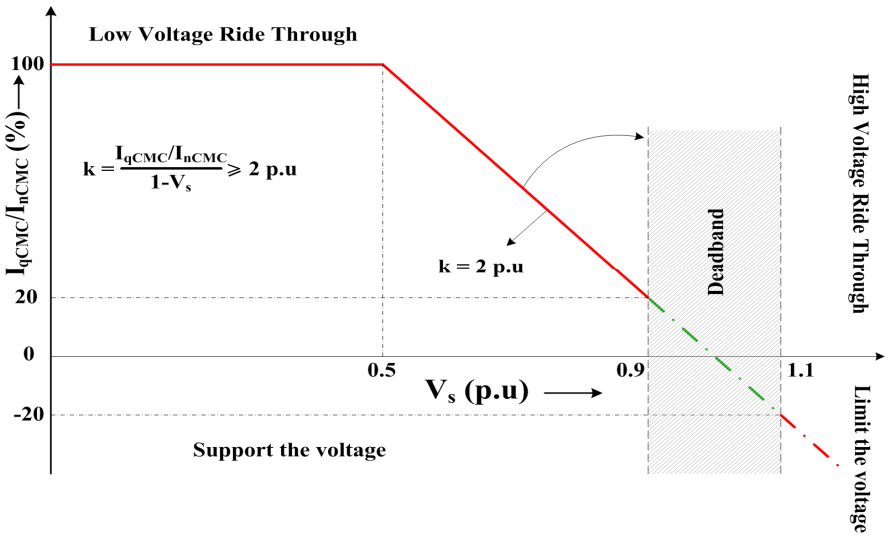


Fig. 11.2: Reactive current injection requirement as per E.ON grid code.

having individual MPPT control under normal condition and other reference guided by grid codes under perturbed voltage conditions for small string of PV panels on individual DC links shows the scalability of the proposed system. The CMIPV unit is connected to PCC point via interface inductor (L_r). At the PCC point local resistive loads are also considered connected to consume the locally produced power from PV panels in majority. Each DC link capacitor is designed for appropriate value considering the ripple voltage and power transaction across it. DC link voltage is maintained at an appropriate value by the grid, whose reference value is derived either from MPPT technique or more than that of MPP value as decided by LVRT controller depending on a dip in grid voltage. For the present study, the characteristic of Neosol TSE 250 make PV panel is used for both simulation in MATLAB and experimentation.

11.4. Control Theory for Working Operation of PV-Grid Connected Cascaded Multilevel Inverter

Increasing penetration of PV technology in existing grid has led to the imposition of stricter grid code. It is utmost important to comply with the applicable grid codes for

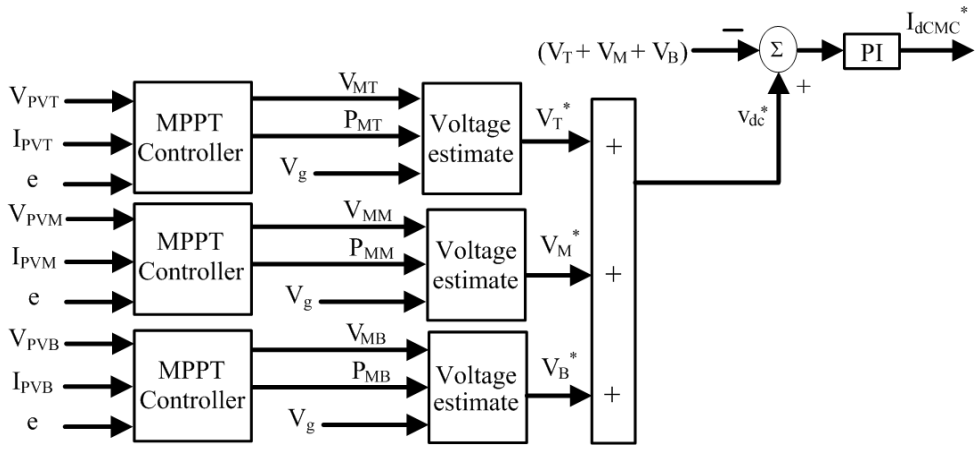


Fig. 11.3: Control blocks of proposed CMIPV for voltage loop.

maintaining the reliability of the system. As per the E.ON grid code, for the PCC voltage between 0.9 V_s to 1.1 V_s, which is considered as healthy grid condition, the CMIPV has to supply the generated power available from PV panels, the said region is shown in shaded portion in Fig. 11.2. From 0.9 V_s to 0.5 V_s the CMIPV is expected to reduce the power extraction from the PV panel by shifting the reference voltage towards V_{oc} for the same scale of insolation so as to accommodate the provision of requisite reactive power support to the grid. Further region left of 0.5 V_s calls for zero generation i.e. bringing the CMIPV to V_{oc}, thereby zeroing the generation support and using the available capacity only for reactive power support. The control for CMIPV operates to handle both the task of MPPT and for power transfer to enable multimode operations. To facilitate both the operations simultaneously the controller is designed with outer voltage control loop and inner current loop with feed forward stabilization. Further the voltage control employ regulation control of individual DC links due to varying PV power generation requirements at the individual DC links.

11.4.1. Voltage Control Loop

For requisite generation of power, the individual DC link voltage is regulated either at MPP voltage or at desired voltage estimated for implementing the LVRT capabilities. The control loop is shown in Fig. 11.3. The error between dc link voltage and the average individual referenced voltage is processed through a PI controller to deduce the estimate

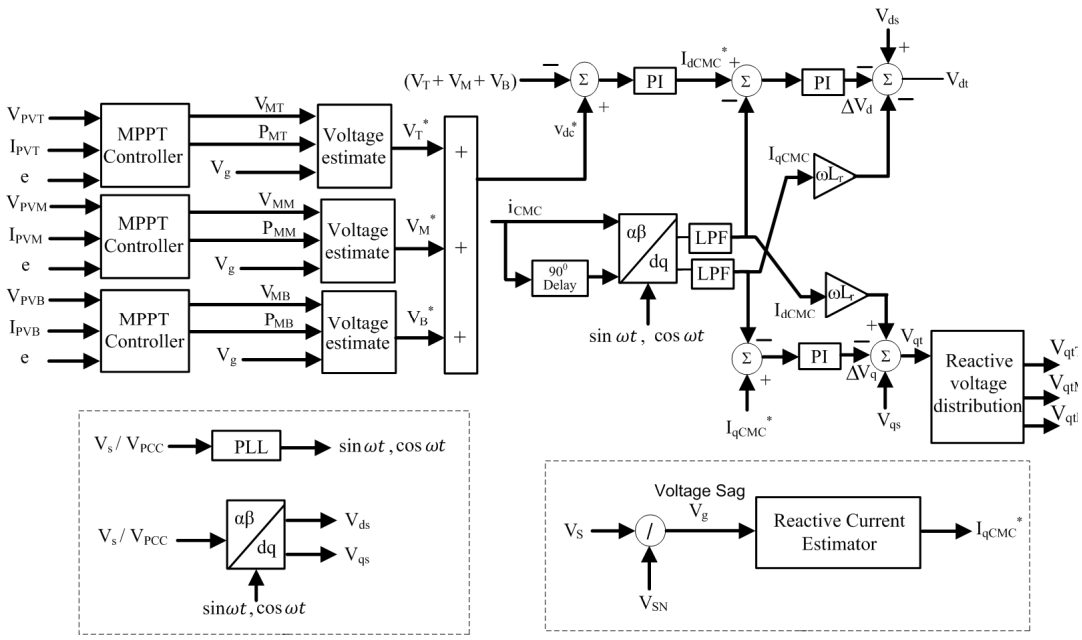


Fig. 11.4: Control blocks of proposed CMIPV with individual MPPT controller and reference reactive current generation.

of the real component of source current (I_{dCMC}^{*}) required for dispatching the requisite generated power. The obtained reference current I_{dCMC}^{*} is compared with actual d-axis component of the source current (I_{dCMC}) obtained from the output side of CMIPV by segregating through Clarke/Parke transformation referred for single phase system discussed in earlier section.

11.4.2. Current Control Loop

The error between referenced d- component of current and actual d-axis component of source current is processed through PI controller to arrive at ΔV_d which need to be added with feed-forwarded source voltage (V_{ds}) and the decoupling d-axis component to compute the terminal voltage (V_{dt}). Similarly the q-axis component of the current (I_{qCMC}^{*}), responsible for reactive power transaction, is first estimated, and then is forced to zero, for UPF operation under normal/healthy condition. It is maintained at the estimated value to enable LVRT capability. The current loop block diagram is shown in Fig. 11.4. The error between referenced q-axis component and actual q-axis component is processed through PI controller to arrive at ΔV_q which is further added with V_{qs} along with decoupling component to arrive at q-axis component of terminal voltage (V_{qt}).

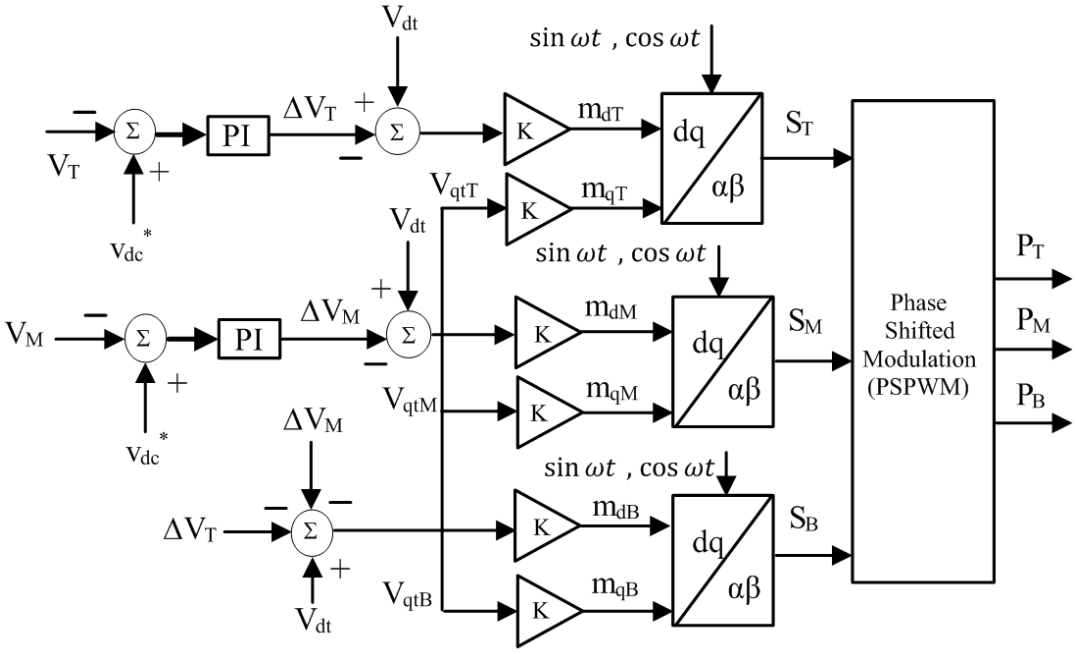


Fig. 11.5: Control blocks of proposed CMIPV for individual DC link control based on reference generated through LVRT.

11.4.3. Voltage Regulation Control of individual DC links

Since the individual PV panel(s) interfaced at each DC link might not be operating at uniform insolation, if left uncontrolled, might cause displacement of some panels from their MPP point due to increase or decrease of MPP voltage from the average reference voltage. To force the individual DC links to MPP point, the MPP reference voltage is compared with the actual voltage and the error is processed though PI controller and the output is added to V_{dt} to arrive at modulating signal of individual H-bridge cell as shown in Fig. 11.5.

It is clear from Fig. 11.2 that in the event of voltage sag the CMIPV has to swiftly move away from MPP point marked by the control as per the droop rate prescribed by the grid side to provide reduced real power to enable support of requisite reactive power to the grid with limited power quality. If the voltage at PCC droops below 0.5 of nominal grid voltage (V_s), the CMIPV has to only supply reactive power sacrificing real power extraction for grid stability.

The ratio of active and reactive power has to be decided as per condition prevailing on the grid as discussed in next section.

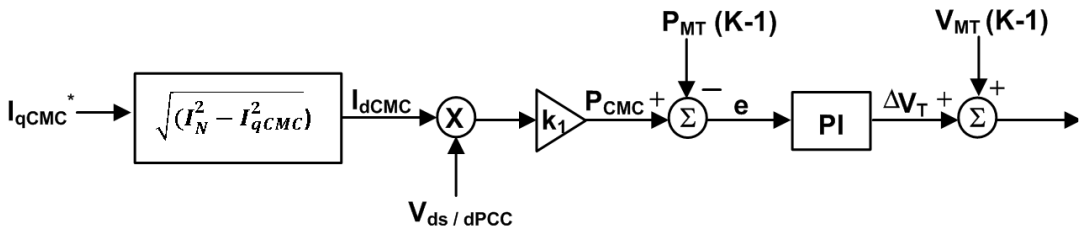


Fig. 11.6: Control blocks for MPPT displaced DC link voltage reference estimator under mode b operation (for displaced MPP operation).

11.5. Capacity Limited Power Control of CMIPV under LVRT

The control devised for LVRT support during low voltage of the grid, between 0.9 V_s – 0.5 V_s the power is transacted by the CMIPV based on the capacity of the inverter to cater the requirements mandated by the grid codes. These modes of operation can be broadly constrained for two situations:

(a) Mode a: When generated power is less than allocated capacity left after catering the mandated requirement of reactive support as per grid codes.

(b) Mode b: When the generation is above the allocated slot left after the mandate requirement of reactive support as per grid code.

11.5.1. Mode 'a': When Generation is Less than the Allocated Capacity Left after Catering the Mandated Requirement

Under this control mode, first the requisite reactive power support is decided as per grid mandate based on the dip in grid voltage and curve for LVRT condition. Thereafter, as per the rating of the CMIPV, the capacity left for utilization determines the extraction of active power from the PV panels. As PV power generation is lesser than that capacity left after requisite reactive power support, the PV harvesting remains at MPP (i.e. active power transfer to the grid is maintained at MPP). For CMIPV to act as per grid code, fast detection of grid voltage and phase becomes paramount. For the current study a fast acting PLL based on EPLL is used. As per the detected magnitude of grid voltage, the sag percentage is calculated, which is further decided based on the reference reactive current (I_{qCMC}^{*}) component as per the following equation [74]:

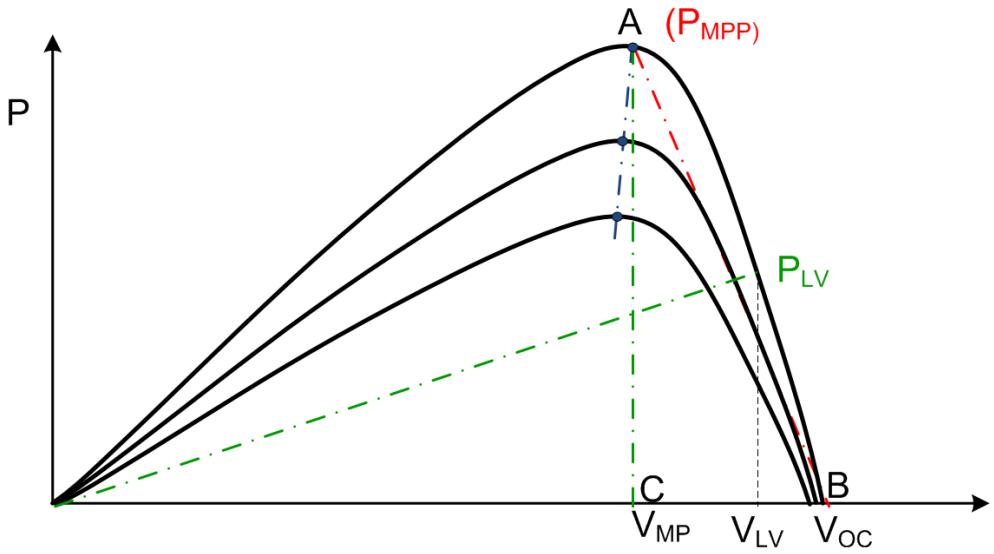


Fig. 11.7: P-V curve drawing for estimation of reference voltage in case of mode 'b' control.

$$I^{*}_{qCMC} \geq K\left(1 - {}^{V_s}/_{V_{sn}}\right) * I_{nCMC} \qquad (11.2)$$

Where V_{sn} is the nominal grid voltage, I_{nCMC} is the rated current of CMIPV. Further, the obtained reactive current component as per eq. (11.2) is divided equally amongst 3 H-bridges for uniform distribution of reactive power. Meanwhile, since generation remains at MPPT the active power fed by the CMIPV is maintained as per the MPP point.

11.5.2. Mode 'b': When Generation is more than the Allocated Slot Left after the Mandate Requirement of Reactive Power Support

Under this control mode, involving the determination of I_{qCMC}^{*} as discussed in the last section, capacity left for active power support is determined in accordance with grid code. With PV generation more than that of available capacity, to fit into the rating of CMIPV, the extraction of power from PV harvesting need to be reduced by shifting the generation point from MPP towards V_{oc}. The active component of grid current is calculated as per the block diagram given in Fig. 11.6 and to obtain I_{dCMC} is used to estimate active power for each individual H-bridge. The referenced active power is

compared with last sampled MPP power out of PV panels connected on particular H-bridge and the error is processed through PI controller to arrive at voltage displacement (ΔV_{j} , where j is T, M, B) that has to be added to last sampled MPP voltage to arrive at new reference voltage (V_T^*), as shown in Fig. 11.6. Similar process is repeated for other bridges also. The new displaced reference point i.e. movements towards V_{oc} lower the output power which cumulatively decreases the current component for active power from CMIPV for maintaining constant current as per the ratings of CMIPV. The Fig. 11.7 through P-V curve and Fig. 11.8 through I-V shows the new displaced reference operating point having lower power, current harvested from PV as compared to MPP power (P_{MPP}).

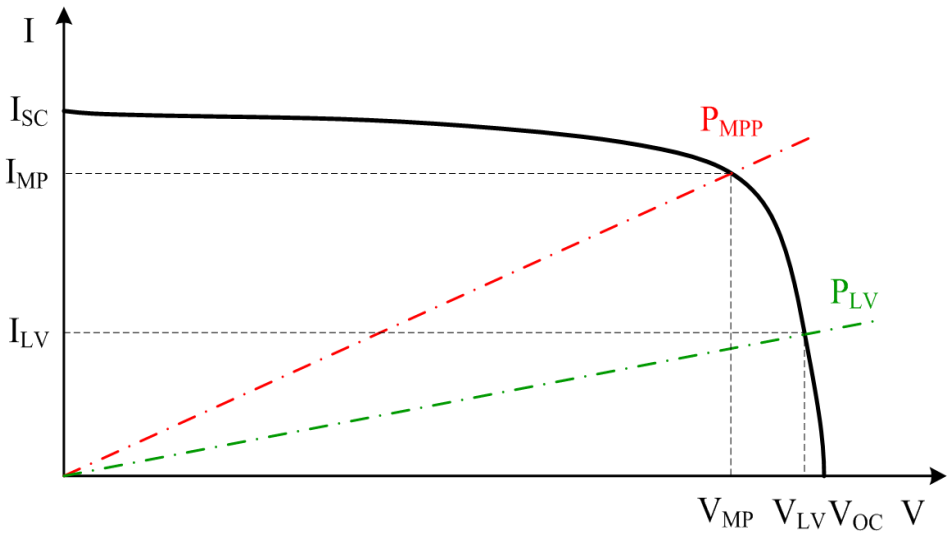


Fig. 11.8: I-V curve representing MPP displaced operating point under constant control mode during LVRT.

11.6. MATLAB Based Simulation of PV-Grid Connected Cascaded Multilevel Inverter Through Multimode Operation

The presented CMIPV unit is simulated under MATLAB Simulink environment using Simpower system. The grid voltage is perturbed through programmed voltage source in MATLAB for the realization of LVRT condition. The various results and waveforms for CMIPV unit neglecting the initial transient condition are shown in Fig. 11.9- Fig. 11.11.

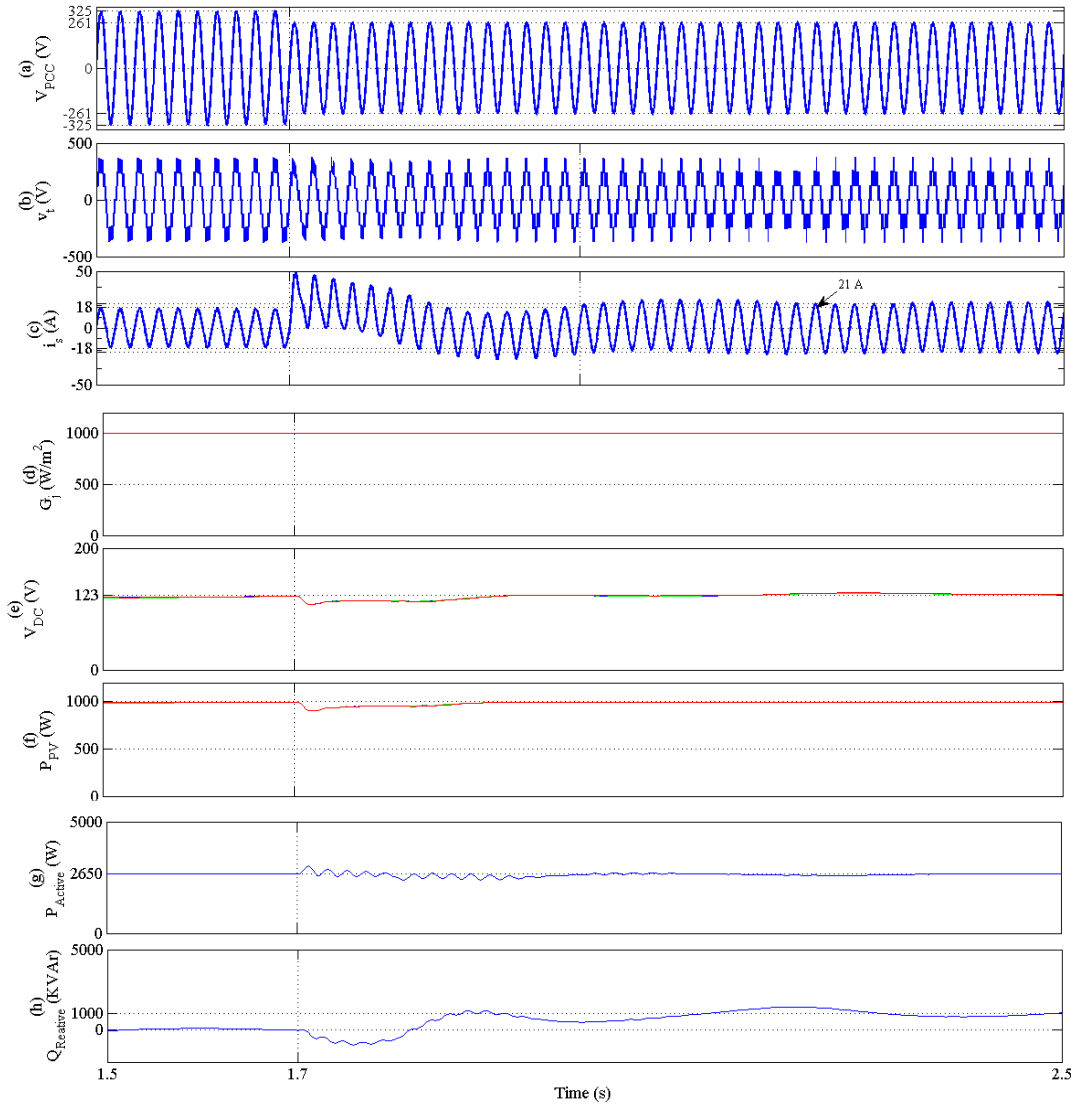


Fig. 11.9: Simulation waveforms of CMIPV under mode 'a' control having constant active power support depicting PCC voltage (v_{PCC}), terminal voltage (v_t), source current (i_s), PV insolation (G_j), DC link voltages (V_T, V_M, V_B), PV power (P_{PV}), active or real power transaction to grid (P_{Active}), reactive power supported to the grid ($Q_{Reactive}$).

11.6.1. Performance Evaluation of PV-Grid Connected Cascaded Multilevel Inverter Through Multimode Operation under Mode 'a' Control

The proposed CMIPV unit is simulated under MATLAB Simulink environment using Simpower system. The various results and waveforms for CMIPV unit neglecting the initial transient condition are shown in Fig. 11.9. Hence from t=1.5s onwards with

uniform insolation of 1000 W/m^2, 1000 W PV generation connected on each 3 individual DC link is shown in Fig 11.9 (d) - (f). The PV is generating its optimum power through CMIPV converter whose DC link voltage reference is around 123 V, which is guided by individual MPPT controller as shown in Fig 11.9 (e).The DC link voltage referenced at MPP voltage in single stage mode ensures optimum power extraction and feed power to the grid at 12.7 A from t=1.5s to t=1.7s as shown in Fig 11.9 (c) at UPF. Meanwhile, the PCC voltage is maintained at 230 V and terminal voltage just sufficient to transfer the requisite generated power as shown in Fig 11.9. (a) – (d). From Fig 11.9 (g) – (h) it is clear that total active power being fed to the grid is around 2650 W and reactive power is 0, conforming to the UPF operation. Apart from feeding the grid, PV is also feeding asmall amount of passive loads connected to the DC links.

At t=1.7s, through programmed source PCC voltage is dipped from 230 V to 185 V which is around 20% dip from the nominal voltage. In mode 'a' control with a dip in voltage, the control should also provide reactive power support depending on prevailing grid code and the percentage dip in voltage. Since in this control active power transfer needs to be constant as the PV panel remains at MPP point at particular insolation level as shown in Fig 11.9 (d) – (g). From Fig 11.9 (f), it may be observed that PV generation remains at 1000 W with small perturbation at t=1.7s, with DC link maintained at MPP of 123 V. Since active power support remains same, it results into increase in source current from 12.7 A to 14.8 A as shown in Fig 11.9 (c). Moreover, as per the mathematical analysis discussed in control section for mode 'a' control a support of 1 KVAr is provided as shown in Fig 11.9 (h). This results in displacement of the source current from UPF.

11.6.2. Performance Evaluation of PV-Grid Connected Cascaded Multilevel Inverter Through Multimode Operation under Mode 'b' Control

To evaluate the effectiveness of control algorithm, for mode 'b' with a generation more than left capacity after reactive power support, the CMIPV is modeled in MATLAB Simulink environment under low voltage grid condition. The initial condition from t

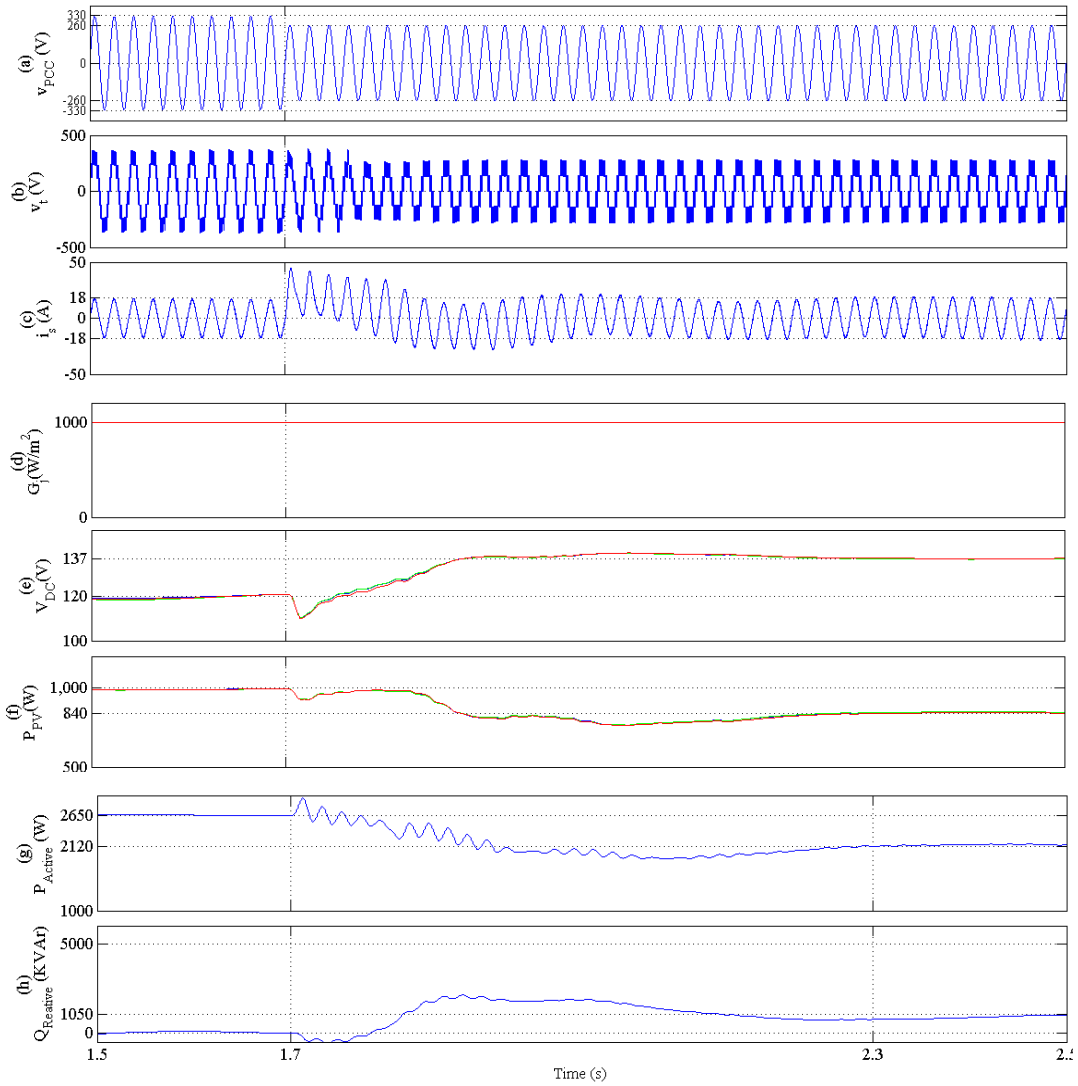


Fig. 11.10: Simulation waveforms of CMIPV under mode 'a' control having displace MPP operation depicting PCC voltage (v_{PCC}), terminal voltage (v_t), source current (i_s), PV insolation (G_j), DC link voltages (V_T, V_M, V_B), PV power (P_{PV}), active or real power transaction to grid (P_{Active}), reactive power supported to the grid ($Q_{Reactive}$).

=1.5s to t=1.7s remains same with uniform insolation of 1000 W/m^2 and MPP power at 1000 W as discussed in the last section.

At t=1.7s a 20 % dip in voltage command is observed, initiating mode ‘b control. As per the grid code, the control has to provide a requisite reactive power support according to percentage dip in grid voltage. Accordingly, the active power support as per the limited available capacity left is compared with last sampled MPP power to displace the reference voltage from MPP point through voltage estimate block set shown in Fig. 11.3. Accordingly at t=1.7s, it is clear from Fig 11.10 (e) that with same insolation DC links voltage changes from 123 V to 137 V. This causes dislodging of PV output power from MPP point towards the V_{oc} causes decreasing in PV power harvesting from 1000 W to 840 W as shown in Fig 11.10 (f). At the same instance, total active power support decreases from 2650 W to 2120 W as shown in Fig 11.10 (g). Further, as per grid code, a reactive support of 1 KVAr is provided as shown in Fig 11.10 (h). For all these intervals of operation, grid current remains constant at 12.7 A with small perturbation at t=1.7s as shown in Fig 11.10 (e).

Fig 11.11 shows the voltage and current waveform of CMIPV together to investigate the

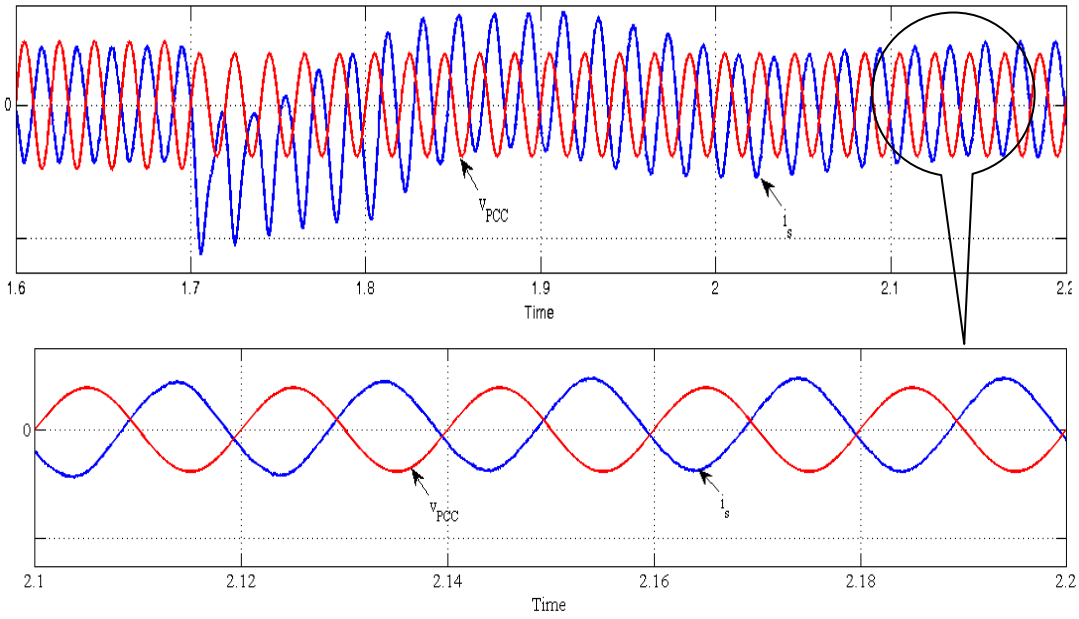


Fig. 11.11: Zoomed Simulation waveforms of CMIPV showing grid current w.r.t PCC voltage at different power factor.

operating power factor (Pf) of CMIPV to transfer the power to the grid. Under normal

grid condition source current is shown 180^0 out of phase with respect to PCC voltage conforming to VSC supplying power to the grid at UPF. At t=1.7s, with a dip in grid voltage, reactive power support needs to be provided as per grid code so the current will no longer remain at UPF and there will be some phase displacement between source current and PCC voltage as shown in Fig 11.11. This zoomed figure conform to the both the active and reactive power support to the grid after t=1.7s.

11.7. Hardware Implementation of PV-Grid Connected Cascaded Multilevel Inverter Through Multimode Operation

The control scheme and hardware prototype is tested on a scaled down voltage for low voltage ride through capability in compliance with grid codes. Each DC link is connected to two series connected PV panels as a string. The prototype is tested keeping a source voltage at 80 V. Both dSPACE 1104 real time controller and DSPIC33FJ16G502 microcontroller are used for knitting the control of CMIPV. The sampling frequency of simultaneous sampled ADC channels is kept at 8.5 kHz, which also corresponds to real time compilation loop of dSPACE 1004 real time controller. The phase shifted PWM of 2 kHz is generated through three compare units of PWM timers of the DSPIC33FGS502 microcontroller to accurately shift the carrier by 60° with a requisite hardware interface.

11.8. Result and Discussion

The simulated performance of CMIPV is experimentally validated on the developed 1.5 KW (6 panels, each 250 W) prototype The CMIPV unit with the multimode operation is experimentally validated and various waveforms are recorded using Agilent DSO's.

The hardware prototype for CMIPV unit is tested both for steady state and transient conditions under different modes of operation. For evaluation of multimode operation, the control algorithm is altered as per the identified modes and the various waveforms are recorded using DSO to depict the dynamics in the measured parameters both on the AC and DC sides.

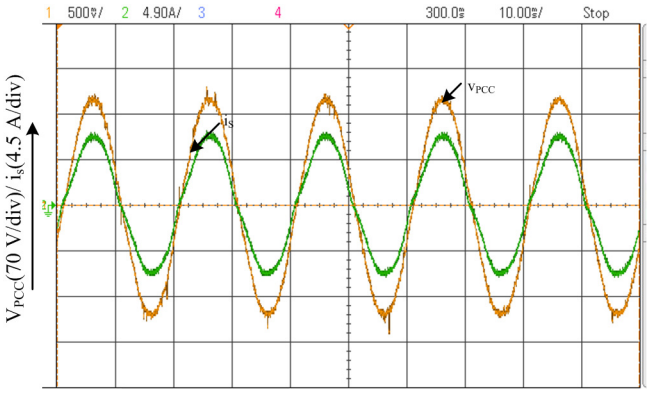


Fig. 11.12: Experimental results showing MPP dictated PV currents and voltage (PCC).

11.8.1. Performance Evaluation Single Phase PV-Grid Connected Cascaded Multilevel Inverter for UPF Operation

Fig. 11.12 shows the grid side output current of CMIPV with PCC voltage. It is clear from Fig.11.12 that CMIPV output current is in phase with respect to PCC voltage i.e. conforming UPF operation. Further, steady state response of output current, inverted terminal voltage of CMIPV is depicted with respect to grid voltage (PCC) in Fig. 11.13. Terminal voltage waveform clearly shows the 7-level operation of CMIPV system.

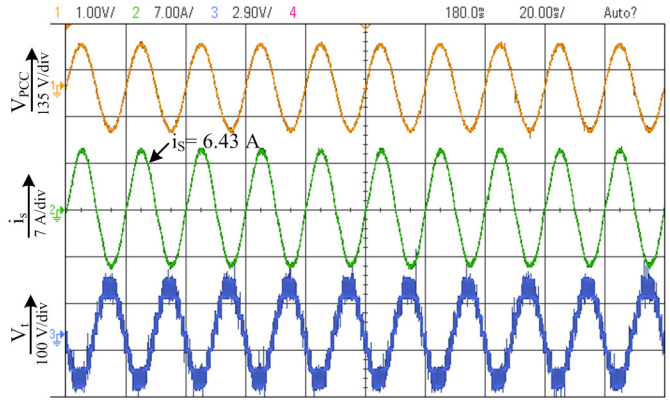


Fig.11.13: Experimental results showing MPP dictated CMIPV output currents, voltage, and terminal voltage.

11.8.2. Performance Evaluation of PV-Grid Connected Cascaded Multilevel Inverter Through Mode 'a' Control

For the demonstration of control in mode 'a' (having PV generation lesser than capacity of inverter left the requisite reactive power support) of CMIPV under LVRT condition, an intentional droop in grid voltage is created. Using three simultaneously triggered

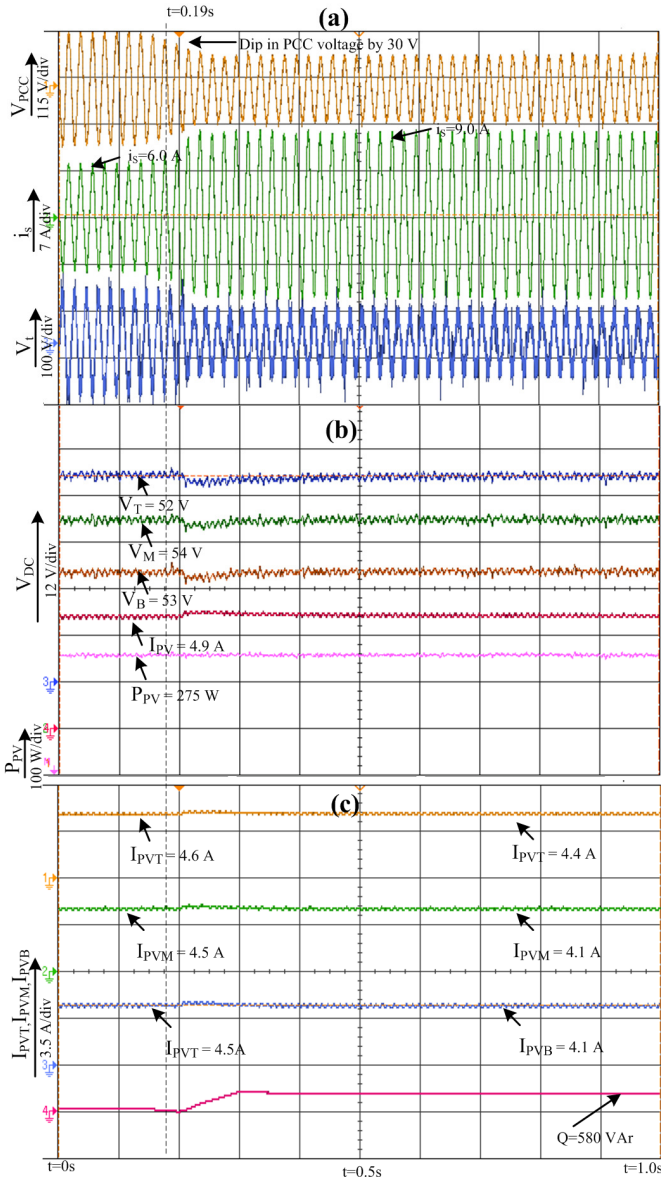


Fig. 11.14: Experimental results showing dynamic response under mode 'a' control depicting (a) PCC voltage, VSC current, terminal voltage (b) CMIPV output real and reactive power, one DC link voltages as dictated by MPPT controller of PV system (c) PV MPP dictated currents, MPP referenced PV power of single PV set connected at the top DC link.

DSO's waveforms are recorded for AC side dynamics, DC link voltage with real, reactive power of CMIPV and PV output currents respectively as shown in Fig. 11.14.

To analyze the dynamics and response of the proposed control algorithm initially the system is started with healthy grid condition having PCC voltage is kept at 80 V and CMIPV outputs a current at 6 A on AC side as shown in Fig. 11.14 (a). Initial PV power support of around 276 W from PV panels and no reactive power supply is provided with DC link voltages maintained at 52V, 54V and 53V respectively for top, middle and lower DC links as shown in Fig. 11.14 (b). The dictated MPPT PV currents of 4.6 A, 4.5 A, 4.5 A respectively are maintained at individual DC links as shown in Fig. 11.14 (c).

At t=0.25 s, an intentional voltage dip is created on the grid side voltage to an extent of

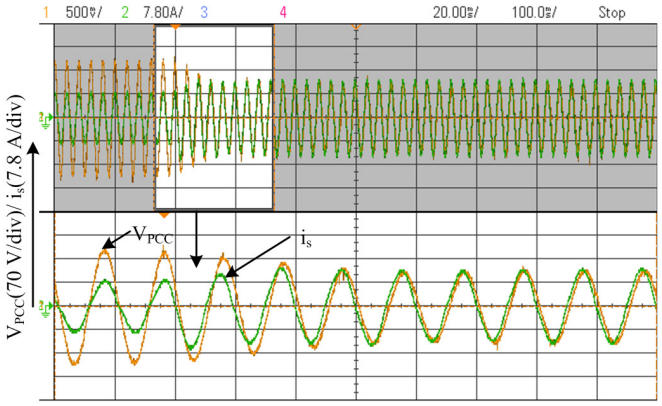


Fig. 11.15: Experimental results showing transient response with dip in PCC voltage and its zoomed waveform for clarity of reactive power support.

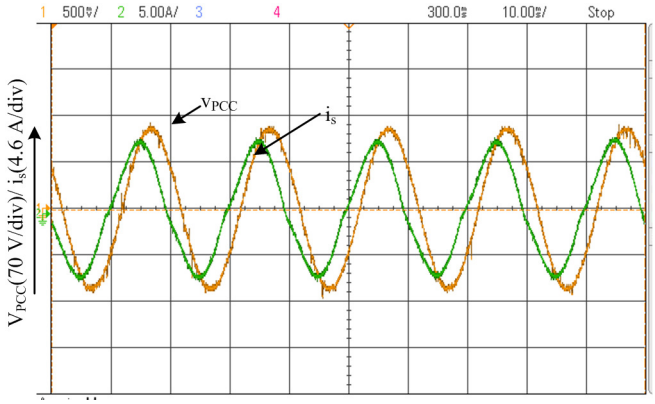


Fig. 11.16: Experimental result showing steady state PCC voltage and CMIPV output current with reactive power support.

30% as shown in Fig. 11.14 (a). With this dip in voltage as per EON grid code a control for appropriate reactive power supply is given, which is reflected as resulting as rise in reactive power support at t = 0.19 s as a shown in Fig 11.14 (c). A simultaneous small perturbation on DC link voltage may also be observed in Fig. 11.14 (b) before it settles again to MPP reference voltage. Due to these perturbations on the DC link, PV current is also disturbed from MPP reference point causing a small decrease in real power support, but slowly it retains back to the MPP value while the insolation level is not disturbed.

From Fig. 11.14 (a) it can also be observed that with a dip in voltage, an increase in CMIPV output current from 6A to 9.0A follows on the AC side due to decrease in modulation index below 0.68 causing terminal voltage operation from 7 levels to 5 levels. The increased current pertains to the reactive power of 580 VAr as shown in Fig. 11.14 (c), which forces the CMIPV output current to exhibit lagging characteristics.

Fig. 11.15 shows zoomed view of the dynamic response of PCC voltage and CMIPV output current at the time of the occurrence of the dip in PCC voltage. It can be observed that the CMIPV output current slowly starts to lag with respect to the PCC voltage before reaching to the steady state conditions as shown in Fig. 11.16.

11.8.3. Performance Evaluation of PV-Grid Connected Cascaded Multilevel Inverter Through Mode 'b' Control

For the demonstration of control mode 'b' control, where PV generation is more than the available capacity left after requisite reactive power support an intentional droop is created. Accordingly, the results are recorded which are shown in Fig. 11.17 and in Fig.11.18. Initial conditions are kept as healthy grid conditions, and at t=0.2s a dip in PCC voltage is created as shown in Fig. 11.17 (a). As per droop percentage, reactive support is provided and the same is depicted in Fig. 11.17 (c). Since in this mode, the remaining capacity of CMIPV is lesser than that of PV generation, it becomes necessary to displace the individual DC link from MPP point towards V_{OC} to match the power with the remaining capacity of PV generation. Accordingly, individual DC links are commanded to change the reference value which came out to be 59V. The displaced DC

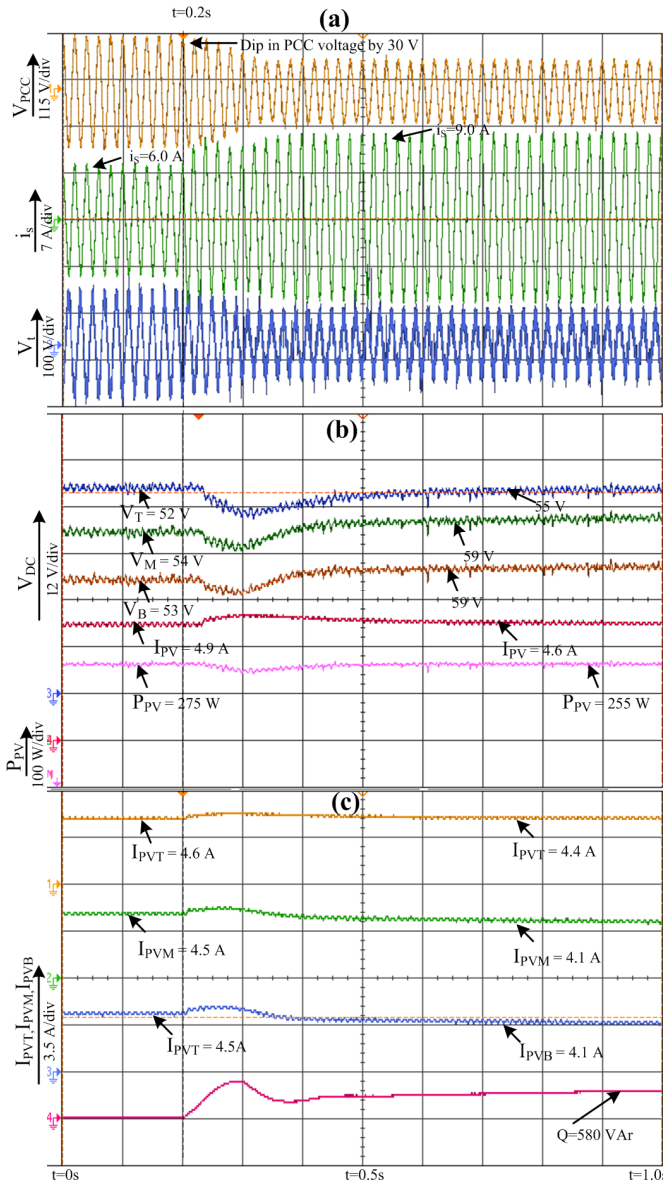


Fig. 11.17: Experimental results showing dynamic response under mode 'b' control with MPP operation depicting (a) PCC voltage, VSC current, terminal voltage (b) DC link voltages of CMIPV and output reactive power ($Q_{reactive}$) (c) PV output currents.

links are shown in Fig. 11.17 (b) where DC link slowly rises to new reference voltage points after initial small voltage dip because of large instantaneous reactive power support. It may be observed in Fig. 11.18 (b) which shows response for larger duration, and voltage on individual DC links reaching out voltages towards V_{oc} to decrease the PV generation.

This decreased power output may be observed from Fig. 11.17 (b). The individual PV output current decreases from 4.6A to 4.4A for top DC link and others to 4.1 A as in Fig. 11.17 (c) Similar things follow for other DC links also.

Fig. 11.18 shows the waveforms observed for large duration to assess the response of

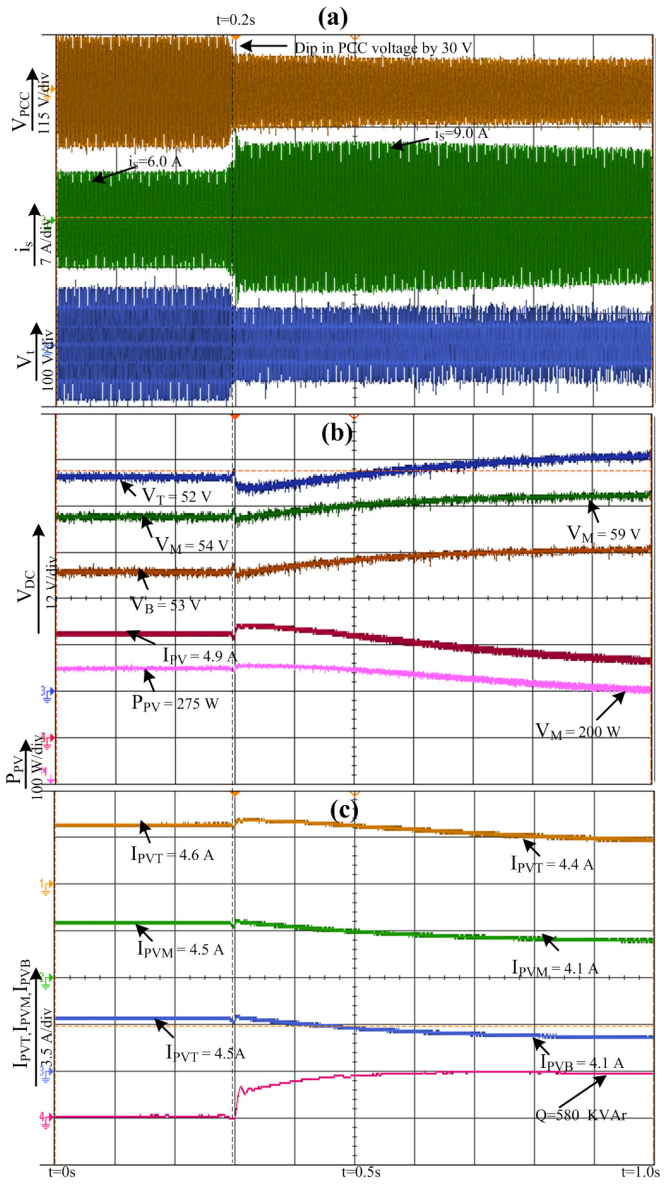


Fig. 11.18: Experimental results showing dynamic response under mode 'b' in large time scale control with MPP operation depicting (a) PCC voltage, VSC current, terminal voltage (b) DC link voltages of CMIPV and output reactive power ($Q_{reactive}$) (c) PV output currents.

control to achieve the steady state values. From Fig. 11.18 (b), it is clearly observed that DC link voltage settles down to 59V, and PV output current decreases to 4.4A, 4.1A and

4.1A respectively, bringing down the active power support to 200 W, as shown in Fig. 11.18 (b).

11.9. Conclusion

The performance of CMIPV system is extensively investigated for LVRT capability through various simulation and experimental results. Particularly the control based on mode ‘a’ where PV generation is assumed to be lesser than the remaining capacity left after reactive power support, and with mode ‘b’, where PV generation is more than the remaining capacity left after proper reactive support as per mandated grid code is successfully demonstrated for grid tied CMIPV system. Further, as per grid code for reduction in the PV generation, the MPP displaced operating point is accurately tracked and the same has been demonstrated through various simulation and experimental results. The depicted results also clearly show the fast dynamics under transient conditions.

Chapter II

LITERATURE SURVEY

2.1. General

The increasing power demand has posed a huge burden on the existing distribution grid infrastructure. The residential loads have become a major consumer of the available power. To meet the growing energy demand local photovoltaic generation and consumption are encouraged by using power electronics interface for adequate control. The PV and balance of the system required for efficient power extraction in grid/off-grid mode, various topologies of the voltage converter, issues of PV system have been envisioned as the scope of the work. In this chapter, a brief on the advancement of PV technology, an insight view of state of the art technologies for various converters suitable for PV system is presented to pinpoint the objectives of the research.

2.2. Literature Survey

The literature review for PV system and its balance of system for application to different loads are discussed and through an extensive survey of literature, the research objectives are drawn.

2.2.1. Solar PV System

Solar photovoltaic (PV) power is one of the most widely used green and clean renewable sources for generation of electric power to fulfill the ever increasing demand of the utility [15]. A major challenge for harnessing the energy rests with generation cost/wattage, availability, reliability when compared to with other power sources based on fossil fuels. With the exponential growth in semiconductor technology cost of PV module and its balance of the system (BOS) have gone down steeply, and the trend is continuing, hence it makes PV based generation, a prospective future power generating system [16].

PV cell follows non-linear I-V and P-V characteristics which vary with insolation and temperature change. The characteristics get more complicated if the entire array does not receive uniform insolation, as in partially cloudy (shaded) conditions, resulting in multiple peaks [17]. The experimental validation of the effect of shading is shown through I-V and P-V characteristics. The numerical algorithm to study the effect of mismatch of varying insolation on individual PV panel cells is also reported in the literature [19]. Few authors have investigated the effect of shading on the grid and concluded that it may have a financial implication and may also lead to instability of the utility [20] [21]. The Estimation of the power output at various conditions of insolation and temperature is not feasible with practical PV panels due to unavailability of various environmental situations at all the time. To cope up with such problem, many researchers have proposed a mathematical modeling of the PV panels in MATLAB to closely approximate with the actual PV panel characteristics [22].

2.2.2. MPPT Techniques for PV System

With the rise in temperature, the conversion efficiency of PV modules goes down drastically; whereas generated power changes with a change in insolation. The generated power if not utilized but freewheeled through the PV module would unnecessary heat the panel and adversely affects its generation efficiency [23]. Moreover, the cost of PV modules are quite high so there is a need for maximum power point tracking (MPPT) and the complete evacuation from PV modules for maximizing the system efficiency is a necessity. Various MPPT techniques are reported in literature wherein, perturb and observe (P&O) method is most widely used due to the simplicity of algorithm and its fast implementation [24] [25]. Though the MPPT technique based on the P&O algorithm is widely used, its performance is reduced the following problems: (i) its dependence on the step size, such that a small step size represents a slow dynamic, while a long step size represents low efficiency; (ii) oscillations around the MPP in both transient and steady-state operations; (iii) local minima tracking (LMT); and others [26]. Amidst varying insolation conditions the Incremental conductance (IC) method is reported to effectively tracking the MPP [27] [28]. The INC MPPT algorithm usually has a fixed iteration step

size determined by the requirements of the accuracy at steady state and the quickness of the response of the MPPT. For fast tracking and efficient control fuzzy logic based MPPT controller is also reported [29]. In [30], neural network algorithm is utilized for MPPT in which through proper training of data, optimal MPP is reached.

Due to the availability of multiple local and global peaks, the conventional algorithm fails to track MPP under partial shading condition [31]. In [32] algorithm for partial shading works well with multicell high voltage application but fails to extract power from individual cells, and the tracking speed is not fast. Others have also proposed a tracking algorithm based on Power estimation for both under the grid and off-grid modes [33]. Some of the reported algorithms employ metaheuristic optimization methods such as particle swarm optimization (PSO) [34]. But most of the algorithm is quite complicated and needs multiple iterations along with scanning.

2.2.3. Converter/Inverter Topologies for Grid/Off-Grid PV System

Single stage and double stage circuit configuration are reported in the literature for grid connected PV system [35]. Grid-connected PV systems usually employ two stages: The first stage is a dc-dc boost converter for boosting the PV voltage and achieving MPPT, and the second stage is a dc-ac inverter for conditioning the output power and synchronizing it with the grid. However, such systems have drawbacks on the count of the higher part count, lower efficiency, lower reliability, higher cost, and larger size [36]. In double stage topology, isolated or non-isolated dc-dc converters are used in conjunction with voltage source converter (VSC) [37]. For the low wattage, low cost PV system non-isolated converters are preferred. To further reduce the operation cost the single stage grid connected PV systems are advocated [38]. Different single-stage topologies have been proposed, and a comparison of the available interface units is presented in [39]. However, the voltage buck properties of the VSI increase the necessity of using a bulky power frequency transformer on the grid side or higher dc voltage at the DC link. Moreover, inverter control is also complicated because the control objectives,

such as MPP tracking (MPPT), power factor correction, and harmonic reduction, are simultaneously considered [40].

Several PV inverters configuration has been presented in the literature to harvest the energy efficiently and cost effectively [41]. The technology based on centralized inverters that interfaced a large number of PV modules to the grid is very old and is discovered for lower efficiency and limited duty periods [42]. The technology involving multiple string inverters is more popular nowadays, where multiple strings of PV modules are connected in parallel instead of an array [43]. The multi-string inverter is the further development of the string inverter, where several strings are interfaced with their own dc-dc converter to a common dc–ac inverter [44]. The ac module or module integrated inverter is the combination of one PV module with a grid-connected inverter connected in a dual-stage mode with an embedded HF transformer. Reviews of ac module inverters are given in [45]. In literature voltage source converter (VSC) based PV grid coupling is also considered with limited power conditioning to utilize the capacity of VSC at maximum to solve Grid power quality issues like unbalance current, harmonics [46].

The conventional VSC with 2 level output suffers during partial shading condition due to bypassing of few panels in the string, making it difficult to make up the DC bus, leading to total loss of PV power generation, which unnecessarily burden the grid, even if PV generation is otherwise available. This necessitates further deep investigation for different configuration for PV system. Further literature have addressed multilevel converter technology and stressed the growing importance of multilevel converters for high-power applications and improving the power quality of voltage waveform [47]. Traditional and well-established multilevel converter topologies, such as the neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitor (FC) are discussed most [48] [49]. Among all practical multilevel topologies, the Cascaded H Bridge (CHB) multilevel converter is considered as one of the most promising alternative for large-scale photovoltaic (PV) power plants [50] [51].

2.2.4. Cascaded Multilevel Converter/Inverter Suitability for PV System

The availability of the separate DC link for independent connection of PV panels makes this topology more interesting, where the multiple dc links can be readily connected to separate PV strings and independent MPPT may be feasible [52] [53]. Further, the modular design can be extended to allow a transformerless connection to the grid [54]. The main reasons for the choice of this topology are reported in literature, which are mainly [55]:

(i) multiple DC links allows separation of the PV arrays so that multiple MPPT algorithms can optimize the extraction of power;

(ii) various control algorithms exist which control the balancing of capacitor voltages for high level numbers; and

(iii) the level number can be increased to allow direct connection of the converter to medium voltages which avoids the losses and expensive interface transformer.

The cascaded multilevel converter (CMC) may be operated in a single stage or double stage mode in grid connected PV system. In [56] isolated dc-dc converter is proposed for achieving high DC link voltage even with smaller PV units, to help in avoiding leakage current. Most of the available literature focuses more on big PV plants using the CMC structure. Very less attention is been given for low power PV application with CMC unit for residential places, where the topology might be quite helpful in solving many problems.

For multilevel converter the major challenge lies in voltage balancing, arising due to the difference in loading on the DC links, varying PV power output and losses across each H-bridge of 3 phases or single phase CMC unit [57]. In general interphase and inter bridge control for voltage balancing is studied in the literature [58] [59].

Various proposed control methods of balancing the voltage may be grouped into two major categories. The first method utilizes modified modulation techniques for voltage balance [60]. In [61], a space vector modulation technique for dc capacitor voltage balancing through redundant vectors is proposed. Few literature deals with the selective harmonic elimination (SHE) modulation were used to balance the dc capacitor voltage by

swapping the pulse signals [62]. These modified modulation scheme reported for 5-7 level CMC cannot be applied or will be very complicated with an increase in the number of H-bridges for voltage balancing. So, researchers are more inclined to use feedback closed loop regulation for DC link voltage balancing. In [63] a small-signal-based voltage-balancing control has been proposed for STATCOM application. Further, a d-q based voltage and power balance control for single phase rectifier based on solid state transformer are also presented in the literature [64]. Few literature is also reported for the proportional integral (PI)-based control methods for a multilevel active rectifier [65].

2.2.5. Modulation Methods for Cascaded Multilevel Converter/Inverter System

Various modulation techniques for CMC have been developed to satisfy the following need:

(a) to generate a stepped switched waveform to best approximate the sinusoidal signal;
(b) to generate voltage and current waveform of high quality and low THD; and
(c) to have a minimum switching frequency of operation.

The mainly level shifted PWM (LS-PWM) and phase shifted PWM modulation methods are discussed in the literature [66] [67]. These modulation schemes have simply modified the form of Sine PWM scheme (SPWM). Since in multilevel control, numbers of H-bridges are more so for their switching, multiple numbers of carrier signals are used. For LS-PWM number of carrier required is 2n+1, where n is the number of H-bridges [68]. Three schemes for the level-shifted multicarrier modulation are: (a) in-phase disposition (IPD), where all carriers are in phase; (b) alternative phase opposite disposition (APOD), where all carriers are alternatively in opposite disposition; and (c) phase opposite disposition (POD), where all carriers above the zero reference are in phase but in opposition with those below the zero reference. Similarly, for PS-PWM, the number of carrier signals remains same, as it associates a pair of carriers to each cell of the CMC

and a phase shift is provided by the carriers of the different cells introduces asynchronism, which generates the stepped waveform.

LS-PWM scheme gives inherent power imbalance at each H-bridge, so needs extra balancing circuitry and control. Since in PS-PWM the power is evenly distributed across the H-bridge, it gives correct operation of the multilevel rectifier. That is why; it is most preferred modulation scheme.

Selective harmonic elimination (SHE) is also commercially available modulation method for multilevel [69] [70]. In this modulation, the switching angles are computed offline and are designed in such a way that arbitrary harmonics (usually of lower order) are eliminated. This method has the advantage of having very few commutations per cycle and is, therefore, achieves better efficiency. The computation intensive SHE algorithm computes angles using Fourier series and the assumption of steady-state sinusoidal voltages; hence, for variable-speed operation, these angles will not fully eliminate the harmonics. Recently, real-time (online) SHE methods have been proposed based on the total THD minimization rather than individual harmonic analysis [71]. Other advanced modulation methods have the potential to be more effective than space vector modulation (SVM) [72] [73].

2.2.6. Low Voltage Ride Through (LVRT) Capability of PV Converter System

As the capacities of the PV system growing norms, the grid codes have emerged from different countries to dictate various ancillary services apart from active power support to the grid by PV-VSC system for reliability, power system stability and maintaining the quality of power to the grid [74]. The initial grid codes for PV system mainly focused on frequency and voltage stability besides embedding anti-islanding protection scheme in the controller. Such controller under low voltage/voltage sag, the PV systems are reported to be disconnected from the main network to avoid reverse power flow and to meet the existing protection issues [75]. But with increasing penetration of PV system particularly in single phase LV grid, and the disconnection and reconnection may create a very

unstable power system, the new German grid code for LV/MV grid connected PV system mandates the low voltage ride through capability (LVRT) capability a compulsory element of the PV system [76].

In [77] adaptive DC link interleaved boost converter based PV system is advocated for tackling LVRT issues. With adaptive DC link under LVRT, the VSI definitely requires an optimized modulation index to increase the efficiency of the system. A similar topology through normal boost converter is also reported for combating the voltage sag condition [78]. But the system suffers from the problem of overvoltage during light load condition, and the extra cost of DC-DC converter besides lower efficiency. In [79] voltage is shifted to V_{OC} to decrease the PV power to provide room for reactive support. In literature for multi mode operation of PV system for supporting LVRT capability with constant current mode, constant active component mode and constant power mode are reported [80]. The cascaded multilevel inverter (CMI) structure shows a promising future for transfer of PV power to the grid. But topology so far has not been explored for its LVRT capability.

Keeping in view of the future functionalities of the PV-CMC system, the control must be ready for accurate reference signal generation for LVRT. For that, synchronization techniques are also very important. In [81] various PLL methods are advocated for correct estimation of synchronizing signals. For controlling single-phase inverters, an orthogonal signal generation (OSG) block is required to be provided for computation of the orthogonal components of the grid current/voltage in a α-β frame [82]. Conventionally, OSG is implemented using phase shifting methods such as Hilbert transform [83], time delay [84], and second-order generalized integrator (SOGI) [85].

2.2.7. Control Aspects of PV-CMC System

Various control technique for VSC based converter/inverter is reported in literature classified broadly as conventional and intelligent techniques [86]. SRF based control is widely advocated for control, but it requires a fast acting PLL for which control is quite complicated and since the power distribution system is highly non-linear, any change in

any parameter of the distribution system may result in malfunction of PLL, resulting in chaos in the overall control [87]. Moreover, the synchronization with PLL provides slow dynamics and transient response. The other control algorithm based on Instantaneous power theory (IRPT) for converter offer very simple and PLL less implementation, but is seriously affected by noisy environment in the vicinity of switching of power converters on the feeder line [88].

Further intelligent control is advocated in literature, where self tuned PI controller with fuzzy logic is proposed [89]. But due to practical implementation problem of rule based fuzzy logic control, the control based on Adaptive Linear Element (Adaline) utilizing least mean square (LMS) based self tuning controller are aggressively advocated [90]. Adaline based control provides least computation time and is very easy to implement. Few literatures are also reported for Adaline based control of active power filters, hybrid filters and STATCOM application [91].

2.2.8. PV-CMC System Feeding Variety of Loads (Static Load, Dynamic Load and Constant Power Load)

A number of literatures are available for 3 phase cascaded multilevel converter/inverter for a specific application. A major part of the literature discusses big PV farms. Very few have dug deep into the research for single phase distribution network using PV generation.

A major part of the total energy being utilized in residential areas includes the conventional single phase induction motor for water pumping as a dynamic load due to the availability of single phase supply in far flung areas. Such motors are highly inefficient as compared to 3 phase induction motors [92]. The 3 phase induction motor pumps fed from single phase using passive elements are reported, but such configuration often leads to improper phase displacement due to shorter life of capacitor, which adversely affects the motoring operation [93] [94].

To avert such situation, the single phase AC-DC-3 phase AC conversion has been advocated which maintain a steady excitation of the machine indifferent to the frequency changes in the grid. Converter- Inverter variable voltage variable frequency (VVVF) based drives have been recently advocated with enhanced efficiency and better throughput and accordingly 3 phase induction motor drive fed from single phase power supply have been reported in the literature [95] [96]. The major issues with VVVF drive lie with the requirement of high value capacitor on the DC link. Such electrolytic capacitors are very sensitive to heat, and its lifetime reduces to half on every 10° rise in temperature at higher voltages [97]. Further, the conventional drive operation with common single high DC bus suffers from a problem of high dv/dt stress, common mode voltage (CMV) and leakage current. To reduce some of the said problems, OEIM drive using single common DC source with space vector modulation technique is reported [98]. Others have also proposed OEIM drive with separate DC source using dual bridge configuration to avoid the problem CMV and zero sequence current [99]. The dynamics and transient response of the drive (inverter- motor pump system) depend on the techniques used for the drive control. Recently in literature v/f controlled OEIM for photovoltaic pumping application using DSAZE algorithm is reported [100]. Often such pump loads act blindly and operate without any active interaction with the grid, which, in a case is participated for demand side management with the grid, can reasonably avert the peaking of demand [101]. Direct load control (DLC) has been advocated in literature for smartly controlling the loads in commercial/office buildings in urban areas thereby helping the utility to offset the financial burden and passively providing support to the grid stability [102].

With growing environmental concerns, the more electric eco-friendly automobile industry is expected to grow and it is going to be one of the major loads on residential places [103] [104]. Major impediments to the growth of HEV/PHEV hovers around the size, weight and efficiency of the charging/discharging system besides the performance of batteries [105] [106]. The majority of the reported centralized charging converters works on single full battery stack, which upon aging and repeated charge/discharge cycle may lead to dissimilar characteristics of individual battery units causing imbalance

voltage across the units [107]. The problem becomes graver when the higher dissimilar number of batteries is included in the stacks, and discharge/charge capability of the battery stack is decided on the weakest SoC of battery stack, prompting the use of charge equalization circuits [108]. This in turn appreciably decreases the power transaction and eludes the asset utilization [109] [110].

To avoid the multiplicity of converter units and saving the space for EV's the use of integrated converters are advocated [111] [112]. In [113] split phase induction motor (IM) windings based integrated converters for traction drive and charging from 3 phase outlet is advocated, which requires extra windings for providing isolation. Other reported papers have also advocated the use of modular multilevel converters as an integrated converter for EV, but experimental validation of concept remained to be probed [114].

2.3. Research Gap

Following research gaps are identified based on the literature survey. Based on these the objectives of the thesis are identified as:

- The scope of CMC to act as a residential or community DC nanogrid.
- The possibility of utilizing single phase CMC as 3 phase voltage splitter for residential drive application.
- To develop a smart control for CMC, being utilized for residential drive application keeping in view the grid health condition.
- The CMC configuration for bidirectional power handling capability for battery charging/discharging application.
- To make PV system more reliable and efficient, with the CMC configuration.
- To develop improved and noise immune controller for PV-CMC system.
- The suitability of PV-CMC as per the new grid code under LVRT situation.
- To utilize PV-CMC configuration in islanded or off-grid mode for feeding loads.

2.4. Conclusion

This chapter has meticulously figured out various challenges with PV system and identified suitable converter/inverter topologies best fitted for residential application. Particularly the CMC based configuration is in-depth investigated for the possibility of utilizing it as DC nanogrid. Apart from the investigation on PV and the CMC structure and its control, a detailed study is presented for various residential applications like pump drive, battery charging/discharging etc. Further various appropriate switching and control techniques for CMC are identified with details for application suited for CMC. Finally, challenging issues and research gaps are exclusively identified.

Chapter III

MODELING AND CONTROL OF PV INTERFACED CMC FOR APPLICATION WITH GRID / OFF-GRID SYSTEM AND SUBSYSTEMS

3.1. General

The prerequisite to design and implementation of any technology is its mathematical modeling. The mathematical model of system enables simulation for the analysis of its behavior prior to its development and to design the controller, its tuning parameters and near actual transient behavior or response of the system under perturbing condition of the source, load, and parametric variation.

In this chapter, the reported work is mainly confined to the development of various mathematical models of PV system, multilevel converter, BESS system, and OEIM drive for their use in the investigation as per the laid out objectives. To access the feasibility of control design a detailed stability analysis is also presented in the d-q frame. Moreover, a brief design and operation of the control of the multilevel system are also presented through phasor analysis for the bidirectional operation of the system.

3.2. Modeling of PV System

PV panels are composed of many single solar cell units connected in series and parallel and similarly, panels are integrated in series and parallel to form arrays. Increase in the number of panels in series leads to increase in open circuit voltage and similarly when increasing number of units in parallel; it improves the short circuit current capacity. To understand the modeling of the string or the PV array the model of the single cell needs to study and therefore need to be developed in MATLAB.

3.2.1 Modeling of PV Cell

The PV array can be understood by modeling of a single cell, which may be extended to simulate the PV array. Fig. 3.1 represents an idealistic model of a PV cell. The basic equations that govern I-V characteristic of the ideal photovoltaic cell are reported in literature [115]:

$$I = I_{pv,cell} - \underbrace{I_{o,cell}\left[\exp\left(\frac{qV}{akT}\right) - 1\right]}_{I_d} \quad (3.1)$$

where $I_{pv,\ cell}$ is the current generated by the incident light (changing with varying isolation), I_d depicted as part of (3.1), represents current in the Shockley diode, $I_{o,cell}$ is the reverse saturation current of the diode, *k* is the Boltzmann constant, T is the temperature of the p-n junction in Kelvin and *a* is the ideality factor of the diode.

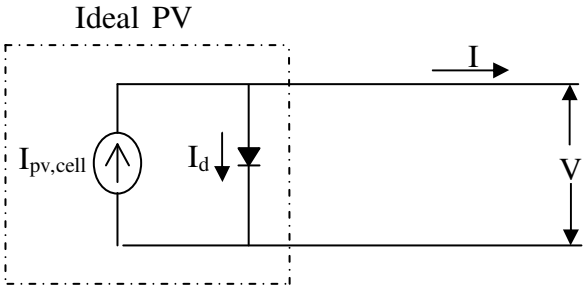


Fig. 3.1: Ideal PV cell model.

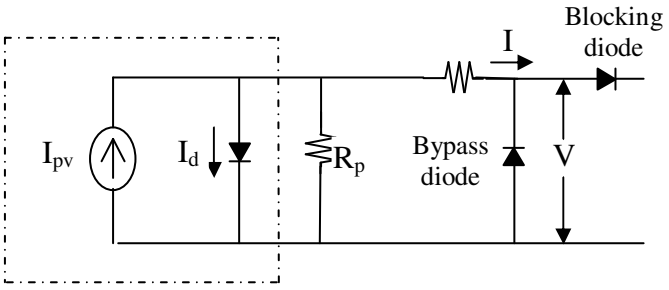


Fig. 3.2: PV Panel model.

3.2.2 Modeling of PV Panel

Actual PV panel is comprised of the series and parallel connected PV cells which incorporates contact resistance R_s and leakage current in the circuit represented by shunt resistance R_p. In light of these (3.1) may be rewritten as:

$$I = I_{pv} - I_O \left[\exp\left(\frac{V+R_S I}{V_t a}\right) - 1\right] - \frac{V+R_S I}{R_P} \qquad (3.2)$$

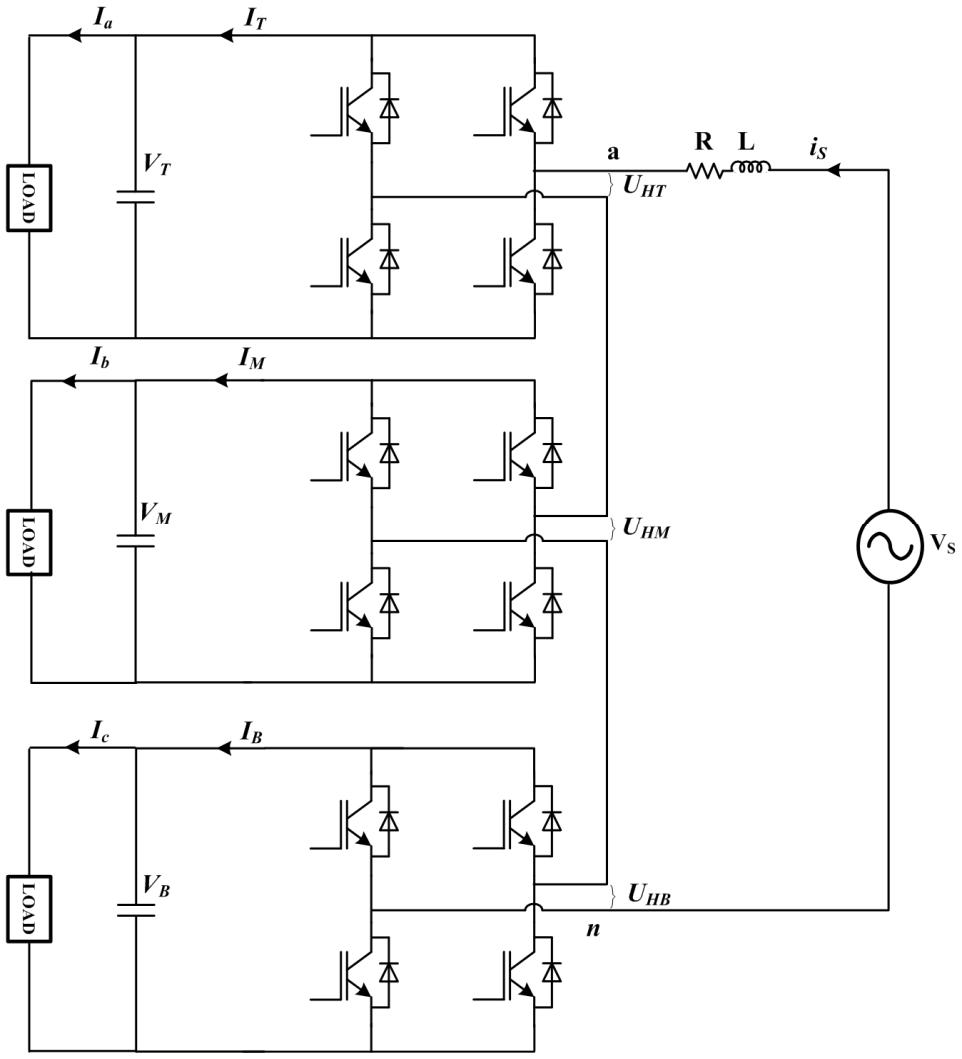


Fig. 3.3: System configuration of grid connected multilevel system.

Where $V_t=\frac{N_S kT}{q}$, N_s-Number of cells connected in series; R_p=Equivalent parallel

Resistance; R_s= Equivalent contact series Resistance. Fig. 3.2 shows the model of a PV panel which incorporates losses due to leakage current and the voltage drop across contact resistance. Bypass diodes are connected across the panel to give safety to the panel against shadow on the panel and failure of PV cell (s). Additionally, a blocking diode is also connected to the terminal to avoid reverse current towards PV panel.

3.3. Modeling and Control of Cascaded Multilevel Converter

This section deals with all the mathematical modeling of the cascaded multilevel converter system identified for present study and designing its controller through analysis of control loop and its verification through simulation in MATLAB environment.

3.3.1. Basic Mathematical Modeling of Cascaded Multilevel Converter

The schematic of the Cascaded multilevel system as shown in Fig. 3.3 is expressed in terms of set differential equations as follows:

$$\frac{di_s}{dt} = \frac{1}{L}(v_s - i_s R - m_T V_T - m_M V_M - m_B V_B - 3R_{switch} i_s) \quad (3.3)$$

$$\frac{dV_T}{dt} = \frac{1}{C}\left(\frac{i_s m_T}{\sqrt{2}} - \frac{V_T}{R_a}\right) \quad (3.4)$$

$$\frac{dV_M}{dt} = \frac{1}{C}\left(\frac{i_s m_M}{\sqrt{2}} - \frac{V_M}{R_b}\right) \quad (3.5)$$

$$\frac{dV_B}{dt} = \frac{1}{C}\left(\frac{i_s m_B}{\sqrt{2}} - \frac{V_B}{R_c}\right) \quad (3.6)$$

Where i_s is source current, L is interface inductor and resistance, R is interfaced inductor resistance, m_i(where i is *T, M* and *B*) represents modulation index of corresponding bridge; R_j (where j is *a, back*) is equivalent load in each phase), R_{switch} represents the losses in each bridge V_i (i is T, M, B) is the DC link capacitor voltage, v_s is the source voltage.

$$\frac{d}{dt}\begin{bmatrix} i_s \\ v_T \\ v_M \\ v_B \end{bmatrix} = \begin{bmatrix} \frac{-(R+3R_{switch})}{L} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_s \\ v_T \\ v_M \\ v_B \end{bmatrix} + \begin{bmatrix} \frac{-v_T}{L} & \frac{-v_M}{L} & \frac{-v_B}{L} & 0 \\ \frac{i_s}{\sqrt{2}C} & 0 & 0 & 0 \\ 0 & \frac{i_s}{\sqrt{2}C} & 0 & 0 \\ 0 & 0 & \frac{i_s}{\sqrt{2}C} & 0 \end{bmatrix} \begin{bmatrix} m_T \\ m_M \\ m_B \\ 0 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 & 0 & 0 \\ 0 & \frac{-1}{C} & 0 & 0 \\ 0 & 0 & \frac{-1}{C} & 0 \\ 0 & 0 & 0 & \frac{-1}{C} \end{bmatrix} \begin{bmatrix} v_s \\ I_a \\ I_b \\ I_c \end{bmatrix} \quad (3.7)$$

Using (3.3) - (3.6) the average model of CMAR can be modeled in the matrix form as in (3.7)

The developed averaged model represented through (3.7) clearly depicts that source current (i_s), DC link voltages can be controlled by modulation indices, m_T, m_M, m_B.

3.3.2. D-Q Based Modeling of Cascaded Multilevel Converter

The conventional 3 phase SRF based theory is modified to suit for single phase system. The heart of the control scheme lays with a correct estimation of the synchronizing signals in phase with phase voltage though phase locked loop (PLL), which is used for generation of unit template vectors. The output '$\sin \omega t$' of the PLL will be in phase with single phase voltage at PCC. For applying modified SRF theory to single phase system, phase voltage or current is assumed as alpha (α) component in α-β frame (stationary frame of reference), and β the component is obtained by introducing phase delay of 90° to alpha components. Using modified SRF theory, the parameters are transformed into d-q components and passed through a low pass filter (LPF) to obtain only averaged or DC components which corresponds to the measured parameters at fundamental frequency.

For, $$x_s = x_{\alpha s} = A.\sin \omega t \quad (3.8)$$

Where x represents i, v and A is amplitude.

The virtual quadrature component in stationary frame is represented as:

$$x_{\beta s} = A.\sin(\omega t - \frac{\pi}{2}) \tag{3.9}$$

Using park transformation the x_{ds} and x_{qs} components are expressed as:

$$\begin{pmatrix} x_{ds} \\ x_{qs} \end{pmatrix} = \begin{bmatrix} \sin\omega t & -\cos\omega t \\ \cos\omega t & \sin\omega t \end{bmatrix} . \begin{pmatrix} x_{\alpha s} \\ x_{\beta s} \end{pmatrix} \tag{3.10}$$

Where ω is the grid frequency and $\sin\omega t$ is the in phase component of the PCC voltage obtained through PLL. Using above transformations the (3.3)-(3.6) may be transferred to the d-q frame to get the decoupled component as:

$$\frac{di_{ds}}{dt} = \frac{1}{L}(V_{ds} + \omega L i_{qs} - i_{ds}(R + 3R_{switch}) - (m_{dT}V_T + m_{dM}V_M + m_{dB}V_B) \tag{3.11}$$

$$\frac{di_{qs}}{dt} = \frac{1}{L}(V_{qs} - \omega L i_{ds} - i_{qs}(R + 3R_{switch}) - (m_{qT}V_T + m_{qM}V_M + m_{qB}V_B) \tag{3.12}$$

$$\frac{dV_T}{dt} = \frac{1}{C}\left(\frac{i_{ds}m_{dT}}{\sqrt{2}} - \frac{V_T}{R_a}\right) \tag{3.13}$$

$$\frac{dV_M}{dt} = \frac{1}{C}\left(\frac{i_{ds}m_{dM}}{\sqrt{2}} - \frac{V_M}{R_b}\right) \tag{3.14}$$

$$\frac{dV_B}{dt} = \frac{1}{C}\left(\frac{i_{ds}m_{dB}}{\sqrt{2}} - \frac{V_B}{R_c}\right) \tag{3.15}$$

Where, m_{dj} (j is T, M, B) is the modulation index along the d-axis. With the help of above transformation decoupled real and reactive power component of source currents are obtained. Active power component is represented as i_{ds}, by assuming V_d as constant (d-component of PCC voltage).

3.3.3. Plant Model Design of Cascaded Multilevel Converter

Transformed parameters in the d-q frame are further used to draw a plant model. Through a plant model a transfer function is deduced, which is helpful in finding out the stability of the system for the tuned parameters of the proposed PI controller. The stability of the system is gauged through the bode plot drawn on the basis of the obtained transfer function.

From the plant model as shown in Fig. 3.4, reference component of source current (I_{ds}^*) is

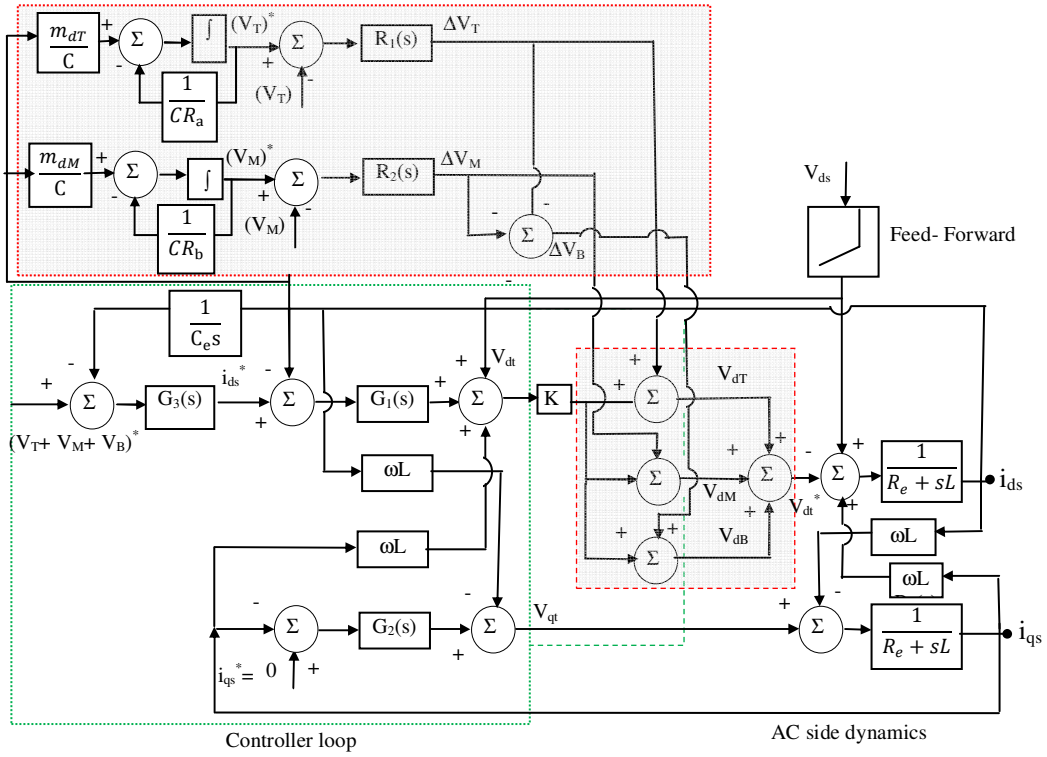


Fig. 3.4: Plant model of the cascaded multilevel system.

estimated through PI controller by passing error between the DC link voltage reference value (sum of the reference DC links) and mean sensed sum of the DC link voltages. The error between the actual source current with respect to the reference value is also processed through PI controller ($G_1(s)$) to output the deficit voltage from PCC voltage. It is further added to filtered d-component of the source voltage, which in-turn is fed forward to estimate the d-component of terminal voltage (V_{dt}) after adding a decoupled component and the same is may be expressed as:

$$V_{dt} = [I_{ds}^*(s) - I_{ds}(s)]\, G_1(s) + V_{ds}(s) + I_{qs}(s)\omega L \qquad (3.16)$$

Under uneven losses across the bridges, the individual bridge might draw unequal power from the mains due same source current flowing in each, leading to different voltages at the DC links. Inclusion of losses in the individual H-bridges is made through control and the same is depicted by shaded portion as shown in Fig. 3.4.

To remediate the unbalance in voltages due to losses, the individual DC link voltages are compared with reference DC link voltage and pass through PI controller ($R_1(s)$, $R_2(s)$) to obtain ΔV_j, where j- T, M, B and the same is added to the 1/3 (for uniform distribution of voltage component) of the d-axis terminal voltage (V_{dt}) to obtain modulating signal for individual H-bridges, which may be mathematically expressed as:

$$V_{dT} = (KV_{dt} + \Delta V_T) \tag{3.17}$$

$$V_{dM} = (KV_{dt} + \Delta V_M) \tag{3.18}$$

To maintain the overall system balance, the reference modulating signal of the bottom bridge may be obtained as:

$$V_{dB} = (KV_{dt} + (-\Delta V_T - \Delta V_M) \tag{3.19}$$

The obtained individual H-bridges reference voltages are summed up as to yield the reference V_{dt}^* voltage.

$$V_{dt}^* = V_{dT} + V_{dM} + V_{dB} = 3KV_{dt} \tag{3.20}$$

For K =1/3 the obtained reference terminal voltage is same obtained earlier through controller loop (unshaded portion) depicted in Fig. 3.4. Hence, the main control loop (Controller) will work independently of balancing control algorithm (shaded portion). The inner control is basically being used to distribute the power among the H-bridges taking into account the losses in the individual H-bridges. This model of the inner current loop is developed from the actual source current (i_{ds}) and the same is represented as:

$$i_{ds} = [-V_{dt} + V_{ds} + i_{qs}(s)\ \omega L] \frac{1}{R_e + sL} \tag{3.21}$$

Where $R_e = R+3R_{switch}$

Substituting the V_{dt} form (3.16) in (3.21) the simplified model of the current loop is shown in Fig. 3.5 (a) and its transfer function may be expressed as:

$$T_1(s) = \frac{i_{ds}(s)}{i_{ds}^*(s)} = \frac{G_1(s)}{R_e + sL + G_1(s)} \tag{3.22}$$

Where, $G_1(s) = K_{p1} + \frac{K_{i1}}{s}$

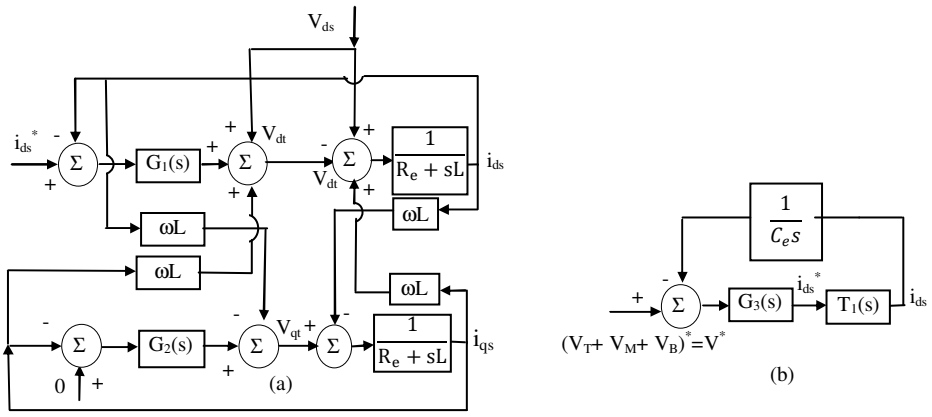


Fig. 3.5: (a) Simplified model for current loop (b) Simplified model for voltage loop.

The overall model incorporating the inner loop and outer loop for the system may thus be as shown in terms of $G_3(s)$ and $T_1(s)$ as shown in Fig. 3.5 (b). The overall transfer function may now be expressed as:

$$T(s) = \frac{i_{ds}(s)}{v^*(s)} = \frac{G_3(s)*T_1(s)}{1+G_3(s)T_1(s)\frac{1}{C_e s}} \tag{3.23}$$

Where, $G_3(s) = K_{P3} + \frac{K_{i3}}{s}$, C_e is the equivalent averaged capacitor value seen from the source side.

Substituting the values of $G_1(s)$, $G_3(s)$ and $T_1(s)$ in the overall transfer function;

the system transfer function may then be expressed as:

$$T(s) = \frac{s^3\left(C_e L K_{P1}^2 K_{P3}\right)+s^2 C_e L K_{P1} A+s\,(C_e L K_{P1} K_{i1} K_{i3})}{s^4\left(C_e L^2 K_{P1}\right)+s^3(C_e L R_e K_{P1})+s^2(C_e L K_{P1} B)+s\,(L K_{i1} A)+L K_{i1}^2 K_{i3}} \tag{3.24}$$

Where, $A = K_{i1} K_{P3} + K_{P1} K_{i3}$, $B = K_{i1} K_{P1} + \frac{K_{i1} K_{P3}}{C_e}$

3.3.4. Switching Technique for Cascaded Multilevel Converter

For 7 level operation of the cascaded multilevel converter, generally, phase shifted modulation technique is used in grid connected mode. To form the 7 level terminal voltage through the multilevel six carrier signals displaced by 60° each is compared with reference modulating sine wave signal to provide the PWM signals for three H-bridge.

An example to such, considering balanced loading condition, is shown in Fig. 3.7. Utilizing the switching signals so generated and output of each H-bridge so obtained (shown in Fig 3.8), the cascaded connection yields 7 level terminal voltages as shown in Fig. 3.8. Decreasing the modulation index (m_j) in turn increases the power intake from

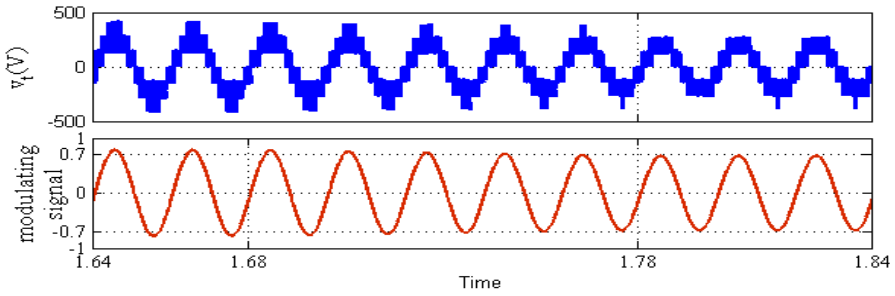


Fig. 3.6: Waveform for multilevel terminal voltage under varying modulation index.

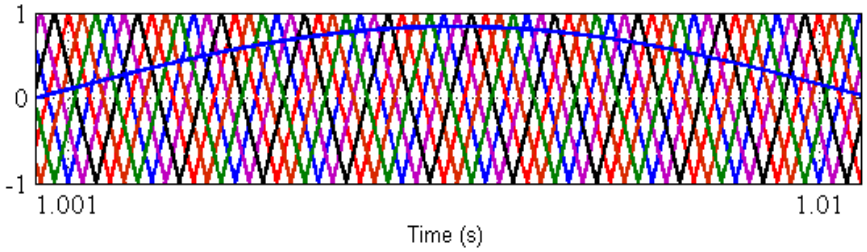


Fig. 3.7: Multilevel system control operation with phase shifted modulation technique.

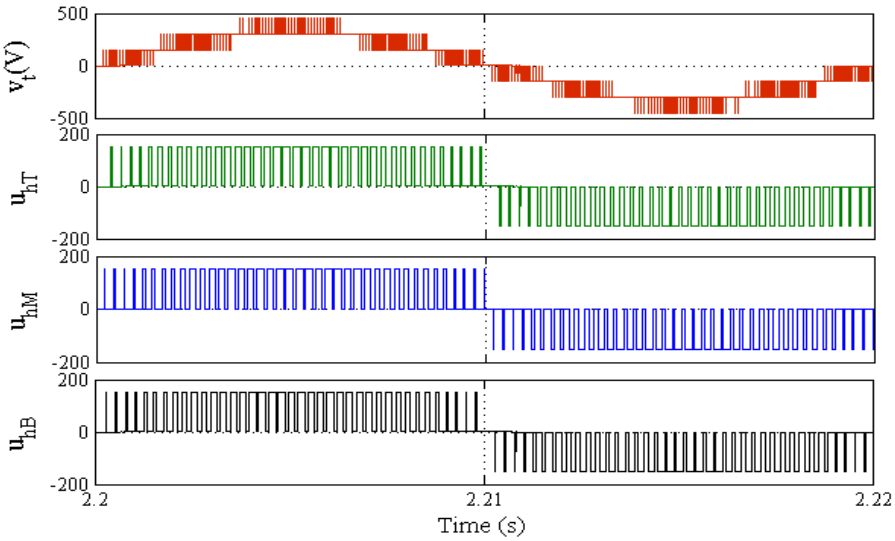


Fig. 3.8: Multilevel system instantaneous terminal voltage of each H-bridge contributing towards formation of 7 level multilevel converter.

AC to 3 different DC links on which appropriate loads are being connected. Decreasing modulation index has got some critical limit beyond that there is a reduction in the levels of terminal voltage from 7 to 5, as also depicted from 1.78 s onwards in Fig. 3.6.

3.3.5. Phasor Representation for Multilevel System Operation

For individual H-bridges (H_T, H_M, H_B) shown in Fig. 3.3, the power is drawn by each H-bridge is given by

$$P_j = u_{hj}. i_s \tag{3.25}$$

Where, u_{hj} (j is T, M, B) is the terminal voltage of individual H-bridges and i_s is the source current common to all H-bridge.

Further, the component of real power drawn by individual bridges is given as:

$$P_{j,\,real} = U_{hj}\, I_s \cos(\theta_j) \tag{3.26}$$

U_{hj} is the rms value of individual bridge, I_s is the rms value of current common to all the H-bridges and θ_j (θ_j equal to φ under balanced loading on each DC link) is the power factor angle between the fundamental frequency source current (i_s) and the terminal voltage (u_{hj}) of each bridge respectively. This will also be the power angle (φ) for UPF operation of multilevel under uniform balanced loading. For unity power factor operation the reflected ac voltage component from each H-bridge across separate DC links adds in phase to realize the net terminal voltage. The phasor diagram of the multilevel system can be represented as shown in Fig. 3.9.

Moreover, for the balanced loading condition on DC links, θ_j will be same for all the 3

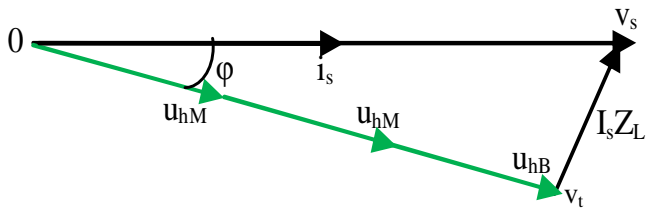


Fig. 3.9: Phasor representation for unity power factor operation under balanced loading.

bridges. Hence, For balanced loading conditions alteration in power is equally shared by each bridge by changing both individual bridge terminal voltage with equal power factor angle θ_j (angle will get altered with load changes) through a change in modulation index for UPF operation.

To make the illustration more lucid a phasor diagram for UPF operation under balanced loading conditions having equal DC link voltage and same θ_j (equal to φ) for each bridge is shown in Fig. 3.10. The terminal voltage phasor (v_t) in Fig 3.10 is divided into two parts of magnitude $(m_T + m_M)V_{dc}$ and $m_B V_{dc}$ and the point of operation (p) of cumulative two bridges with respect to the third bridge is shown identifiable through the corresponding arcs. The arcs corresponding to $2V_{dc}$ and V_{dc} intent to explain an overlapping area which encloses this point conforming to the feasibility of operation. Any mismatch in loading during transient operation will dislodge the point 'p'. If this displacement is within the overlapping area, it can be reinstated by appropriately controlling the modulation indexes of the bridges for UPF operation with balanced loading conditions for rectifier application. Accordingly, the section pz:pw will be

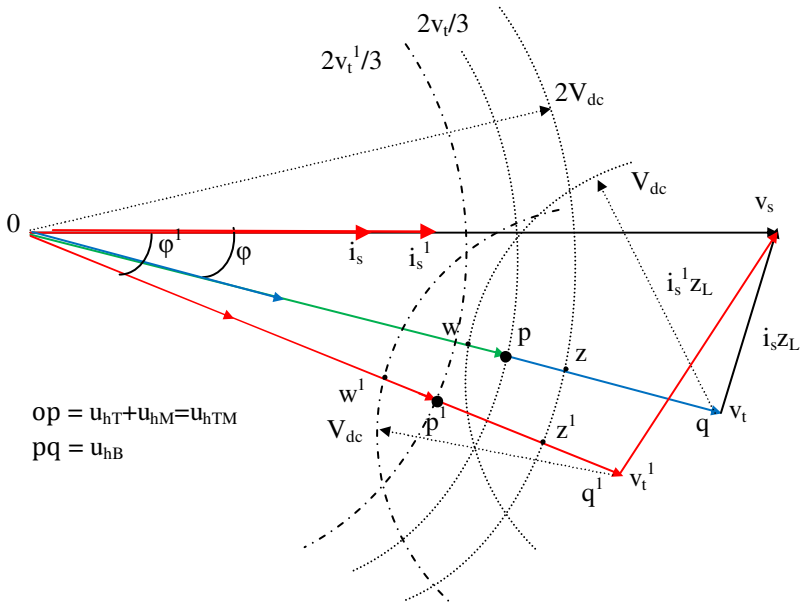


Fig. 3.10: Phasor diagram representing UPF and operating region with changing loading condition.

reinstated to 2:1 ratio.

Even with changed balanced loading condition under UPF operation, the ratio of 2:1 has to be always maintained. To make a lucid presentation of phasor and its range of operation under rectifier mode variation in modulation index and power angle is made. Modulation index is decreased which results decrease in v_t and increase in power angle represented as oq^1 (v_t^1) and φ^1 respectively is evident from Fig.3.10, which clearly shows increased balanced loading condition on individual H-bridges. This resulted into changed operating points (p^1) bounded by arcs $2V_{dc}$, $2m_j^1V_{dc}$ and $m_j^1V_{dc}$, where m_j^1 is the new modulation index of individual H-bridges (j is T, M, B). As evident from phasor diagram, the increased loading resulted into the wider scope of handling unbalance on individual H-bridge. The details of the same will be discussed in next section. Further decrease in modulation index, beyond the critical value may cause a change in the levels of terminal voltage from 7 to 5, as, beyond the critical limit, the modulation indices are not sufficient enough to enable simultaneous utilization of three individual H-bridges as evident from Fig. 3.6. This may lead to deterioration in the power quality (PQ) at the PCC. So to have improved PQ operation, the region of control for the modulation index is made between $0.7<m_j<1$. The operation of CMC with PV, however, may continues to work with requisite voltage levels directed by the MPPT conditions.

3.4. Modeling of Battery Energy System Emulating near Constant Power Load (CPL)

For more realistic and accurate response of Li-Ion battery, Randle's equivalent circuit is used for mathematical modeling and simulation as shown in Fig. 3.11 [116]. The mathematical model represented as:

$$V_{BB} = E_{BB} - IR_0 - V_1 \tag{3.27}$$

Where V_{BB} is the terminal voltage, V_1 is the voltage across the parallel network (R_1, C_1)

Dynamic voltage (V_1) across the RC parallel network may be represented as:

$$\frac{dV_1}{dt} = \frac{V_1}{R_1 C_1} + \frac{I}{C_1} \tag{3.28}$$

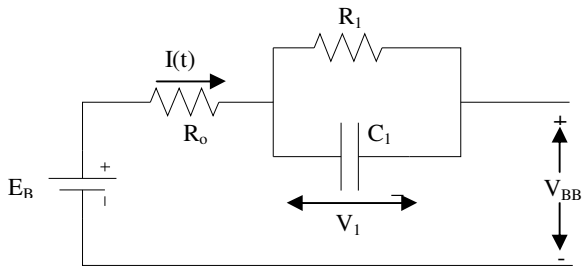


Fig 3.11: Randle's Li-Ion equivalent battery model application.

$$\frac{dV_1}{dt} = \alpha V_1 + \alpha\beta I \tag{3.29}$$

Where $\alpha = 1/(R_1C_1)$ is the inverse time constant and $\beta = R_1$ is the input coefficient and E_{BB} is open circuit voltage which is a function of SOC and temperature. The other parameters R_0, R_1, C_1 are a function of SOC, temperature, and direction of the current.

3.5. Modeling of Open End Winding Induction Motor (OEIM) Pump Drive

Every induction motor comes with 6 terminals which may be connected in star or delta by proper connections. Fig. 3.12 (a) shows the 3 phase 6 terminals induction motor feeding a pump load. Here the terminals a_2, b_2, c_2 are shorted together to get the neutral

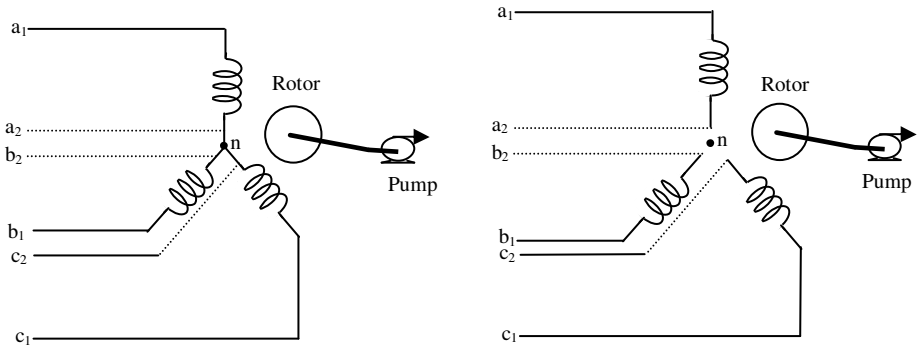


Fig. 3.12: 3φ (a) star winding induction motor (b) open end winding induction motor (OEIM).

point of a star connection. To get the open end winding induction motor, the end point of each phase (a_2, b_2, c_2) is kept open as in Fig. 3.12 (b) so that individual phase can be fed

through separate H-bridges. For modeling of the open winding induction motor, synchronously rotating reference frame is used. Since the rotor bars are short-circuited the induced voltage in the rotor becomes zero as in (3.32) and (3.33).

The dynamic model of the induction motor is depicted in (3.30) – (3.33) [29].

$$V_{qs} = R_s i_{qs} + \omega_s(L_s i_{ds} + L_m i_{dr}) + p(L_s i_{qs} + L_m i_{qr}) \quad (3.30)$$

$$V_{ds} = R_s i_{ds} + \omega_s(-L_s i_{qs} - L_m i_{qr}) + p(L_s i_{ds} + L_m i_{dr}) \quad (3.31)$$

$$0 = R_r i_{qr} + (\omega_s - \omega_r)(L_m i_{ds} + L_r i_{dr}) + p(L_m i_{qs} + L_r i_{qr}) \quad (3.32)$$

$$0 = R_r i_{dr} + (\omega_s - \omega_r)(-L_m i_{qs} - L_r i_{qr}) + p(L_m i_{ds} + L_r i_{dr}) \quad (3.33)$$

Where, L_m = magnetizing inductance of the stator, L_s = Self inductance of the stator, L_r = Self inductance of the rotor referred to stator side, R_s is stator resistance, d/dt is represented as p, i_{ds} and i_{qs} represents the stator d axis and q-axis current; i_{dr} and i_{qr} represents the rotor d-axis and q-axis currents referred to stator, ω_s is the synchronous speed, ω_r represents the rotor speed.

3.6. Conclusion

PV- Multilevel system, modeling, control aspects and its applications has been discussed in this chapter. Through proper mathematical modeling of PV panel, its behavior is approximately matched with actual PV panel. Further, a plant model of the multilevel system is deduced to arrive at controllable parameters of it in terms of modulation index. Multilevel system involves a multiple numbers of PI controllers. The challenging task of tuning their parameters is eased by derivation of the transfer function in this chapter. Mathematical models of OEIM drive and battery loads has also been developed for MATLAB Simulation. A detailed phasor analysis of CMC system for determining the limits of the control operation under balanced loading condition at DC links and control of the modulation index has also been explained.

Chapter IV

SINGLE PHASE OFF-GRID PHOTOVOLTAIC SOURCED CASCADED MULTILEVEL INVERTER FOR POWER BALANCED OPERATION

4.1. General

Having discussed the modeling and a brief generalized control for CMC, PV with varied residential loads, investigation is due for establishing the suitability of the CMC for off-grid application. In this chapter a cascaded H-bridge multilevel inverters (CHBMLI) based rooftop photovoltaic (PV) inverters feeding isolated loads for the off-grid application is presented. The traditional control techniques using battery supported PV panels using level shifted technique lead to the non uniform operation and utilization of each H-bridge, where some bridges are under high stress as compared to others. Proposed controller levels the utilization of storage and power generated by PV panels at each level having same capacity PV panels and battery. The control method utilizes rotation policy for the operation of each bridge at each level in three fundamental cycles, to enhance both the lifetime of the battery, H-bridges and PV panels used.

4.2. Features of Single Phase Off-Grid PV System using Cascaded Multilevel Inverter

In this work, a control strategy is proposed which levels the utilization of the all the H-bridges in three fundamental frequency cycles. The proposed method is based on the rotation of PWM based gating pulses for each bridge in a cycle, each being generated through level shifted multicarrier SPWM for each PV and battery unit connected to DC link at each H-bridge.

4.3. System Configuration of Single Phase Grid Connected PV System using Cascaded Multilevel Inverter

Fig. 4.1 shows the block diagram of proposed seven level CHBMLI configurations comprising of 3 units each of PV arrays, MPPT charge controller, battery storage system, CHBMLI gating pulse controller and capacitor connected to form DC bus of each H-bridges which in turn is connected in cascade to feed the R-L load. Power capacity of PV

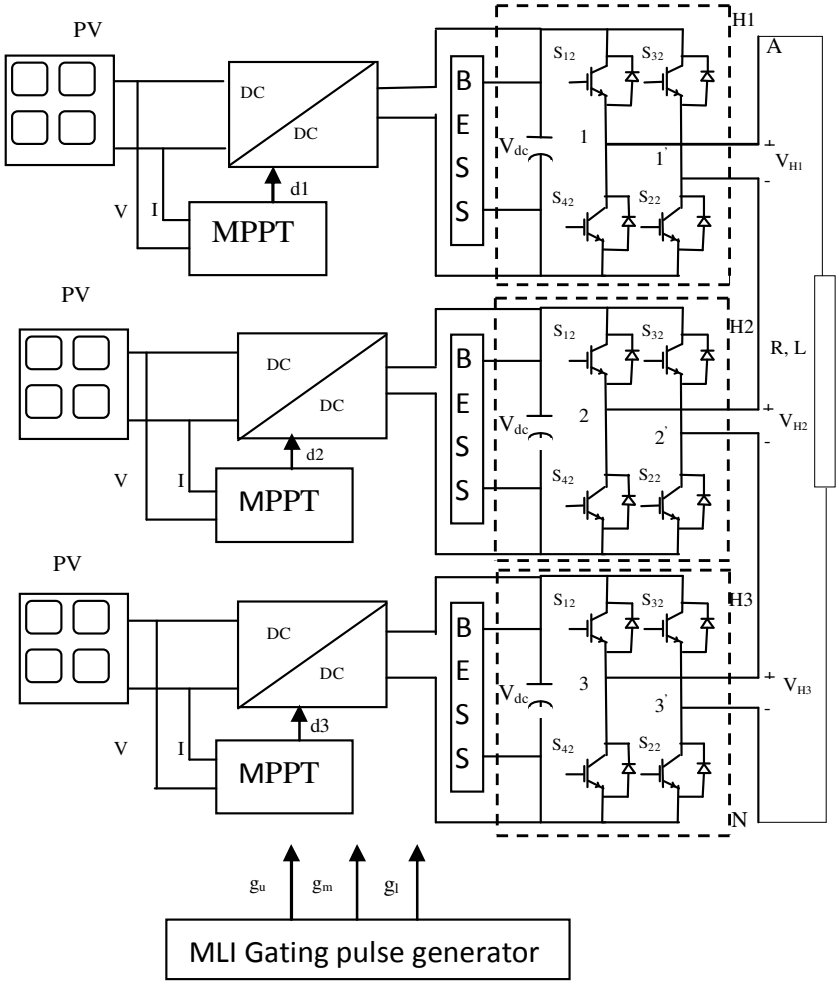


Fig. 4.1: Block diagram for the proposed CHBMLI configuration for feeding off-grid loads.

unit of each H-bridge is kept at the same power level of 800 watts. It is depicted in Fig. 4.1 that PV arrays connected to each bridge consist of panels (2X2 array configurations). The dc-dcboost converter is connected in between the H-bridge and PV array. MPPT

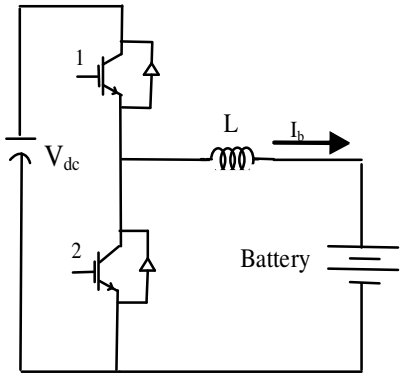


Fig. 4.2: Schematic of battery connection.

controller generates the gating pulse by sensing the voltage and current at PV array output terminal. The power flow control is obtained by keeping the DC bus voltage constant and keeps the equilibrium of energy supplied, stored/released and consumed in the load. Each battery unit houses independent buck-boost converter interfaced to the battery for proper charging and discharging.

4.4. Control Theory for PV Fed Cascaded Multilevel Inverter

Gating signals for the seven level CHBMLIare generated by making amendments in reported in-phase disposition (IPD) level-shifted multicarrier modulation technique. Gating signals for each H-bridge are generated by comparing themodulating signal with thecorresponding carrier wave. Gating pulses to each of the H-bridge are applied on rotation basis cyclically so that power handled by each H-bridge is equal in three fundamental cycles (shown in table 4.1). From the table it may be clear that in first cycle g_u, g_m, g_l pulses are applied respectively to H1, H2, H3, where g_u is the gating pulse for least time interval, $g_l$is the gating pulse for maximum time and g_m is the time interval between g_u and g_l. In the second fundamental cycle g_l, g_u, g_m pulses are applied

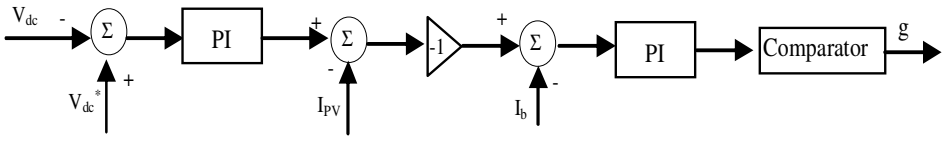


Fig. 4.3: Control logic for battery operation.

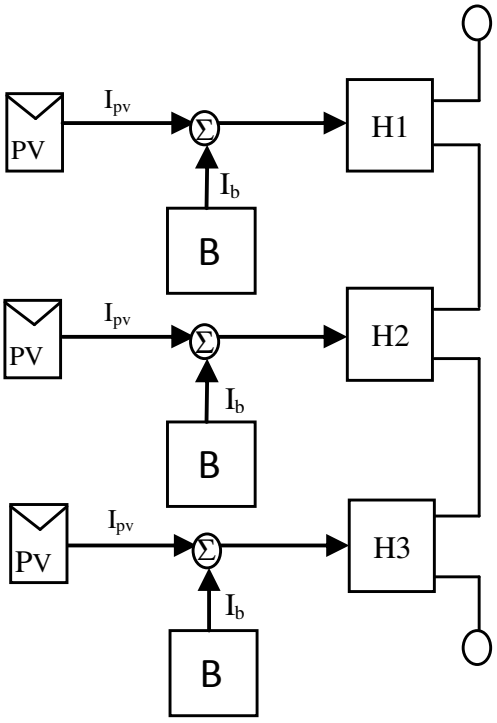


Fig. 4.4: Single line diagram for 7 levels CHBMLI.

respectively to H1, H2, H3 and so on. Gating sequence for the bridges gets repeated after three fundamental sequences. A more explicit representation of gating sequence and its rotation policy is given in Fig. 4.5.

In the standalone mode storage element is always needed so that deficit/excess power could be provided, stored to meet current demand. Since PV panels are operating at MPPT, extracted power is divided into two components; one feeding the load demand and the remaining excess/deficit power can be utilized /derived for/by charging/discharging the battery. Power flow through battery system is controlled by abuck and boost converter as shown in Fig. 4.2, whose gating pulses are controlled by processing the error separately between voltages across each DC link capacitor and reference dc bus voltage by a PI controller. PI controller estimates the current reference for supplying to the load by each H Bridge from the hybrid of PV panel and the battery source. Battery reference current is estimated by subtracting PV current from the total reference current. When the difference is processed by a PI controller, it provides reference voltage modulating thesignal for the PWM control of CHBMLI. The battery

may operate in either in charging or discharging mode depending on the load demand, PV generation and gating pulses applied to bridges. Single line diagram for the current distribution at each bridge is shown in Fig. 4.4. When gating pulse applied to a bridge is g_u then it will lead to thecharging of thebattery for a larger interval of time as compared to thecondition when gating pulses are g_l.Using rotational gate sequence gating pulses repeats after 3 fundamental cycles leading to uniform utilization of battery at each level. From, Fig. 4.5 it may be more explicitly clear that gate control (g_{H1}, g_{H2}, g_{H3}) pulses for each bridge during three fundamental cycle levels the power transfer across the H-bridge at each level.

Table 4.1
Switching sequence for CHBMLI gating

Fundamental cycle	H1	H2	H3
I cycle	g_u	g_m	g_l
↓			
II cycle	g_l	g_u	g_m
↓			
III cycle	g_m	g_l	g_u

4.5. MATLAB Based Simulation of Single Phase PV Off-Grid Cascaded Multilevel Inverter System

The CHBMLI with rotating gating sequence control for power balance operation of each battery supported PV panel at each level on DC bus of CHBMLI is simulated under MATLAB Simulink environment as shown in Fig. 4.6, with RL load (R=25 Ω, L=35 H) having 0.9 pf. The output voltage at the AC side is maintained at 230V by proper selection of modulation index. DC link voltage at each bridge is maintained at 120 V with the proper switching of each H bridge and controlling the current of battery units. Maximum power from the PV array is tracked through IC based MPPT controller whose algorithm is written in embedded MATLAB function in Simulink. PV arrays are configured to deliver maximum power of 800 Watts ateach bridge with 1000 W/m^2

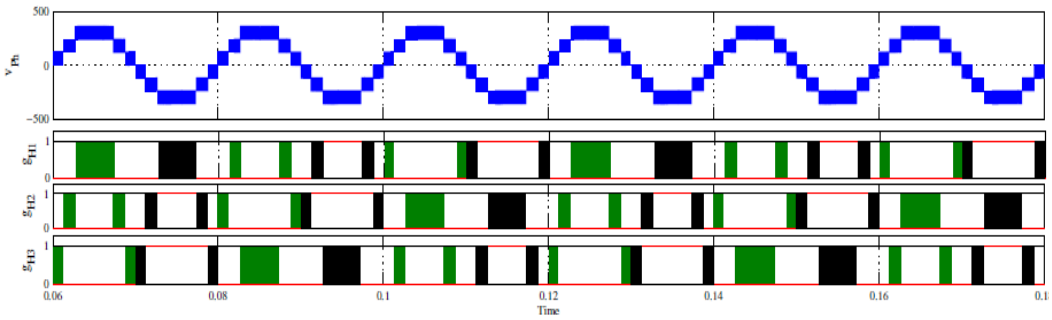


Fig. 4.5: Rotating gating pulse signal sequence for each H-bridge.

insolation level. Gating pulse sequence is being rotated for bridges using the multiport switch in Simulink after 0.02s. 7-level CHBMLI is configured in MATLAB by cascaded stacking of H-Bridge one over the other.

4.5.1. Performance Evaluation of Single Phase PV Fed Multilevel System under Varying Insolation Condition

The control scheme for CHBMLI with hybrid PV and battery source for an R-L is simulated under MATLAB Simulink environment. The effectivenessof the proposed scheme has been verified by changing the insolation conditions simultaneously at each level uniformly. As shown in Fig. 4.6 (a-g) CHBMLI operation is kept with uniform insolation of 1000 W/m^2 from t=0.0s till 0.25s. At the start of operation, thebattery is assumed to be fully charged. With the start of operation at t=0s PV power starts increasing to reach its MPP through duty cycle based IC controller (shown in Fig. 4.7 (d)). MPPT controller maintained the PV power at a constant value of 800 watt for 1000 w/m^2 till 0.25s by proper duty cycle control. As shown in Fig. 4.6 (c) DC link voltage reaches the steady state value of 120 V and is maintained throughout in operation. The voltage at the output terminal of CHBMLI marks 7 levels in the voltage waveform is at the fundamental frequency and very close to sin wave with the peak of 360 V and RMS voltage of 230 V with THD of 0.58 % (Refer Fig. 4.6 (a)). The load current as shown in Fig.4.6 (b) is almost sinusoidal and at the fundamental frequency with THD of 0.43 %, with a peak current of 12.8 A and RMS current of 9.017 A.

4.5.2. Performance Evaluation of CHBMLI for Power Balance Operation using Battery Supported PV Systems

The crux of the control scheme for power balance of battery supported PV systems of each level of CHBMLI is presented in Fig. 4.6 (e-g). For a proper understanding of power equalization instantaneous battery current, average battery current, the current supplied by PV panels and net current offered by battery supported PV panel is presented for

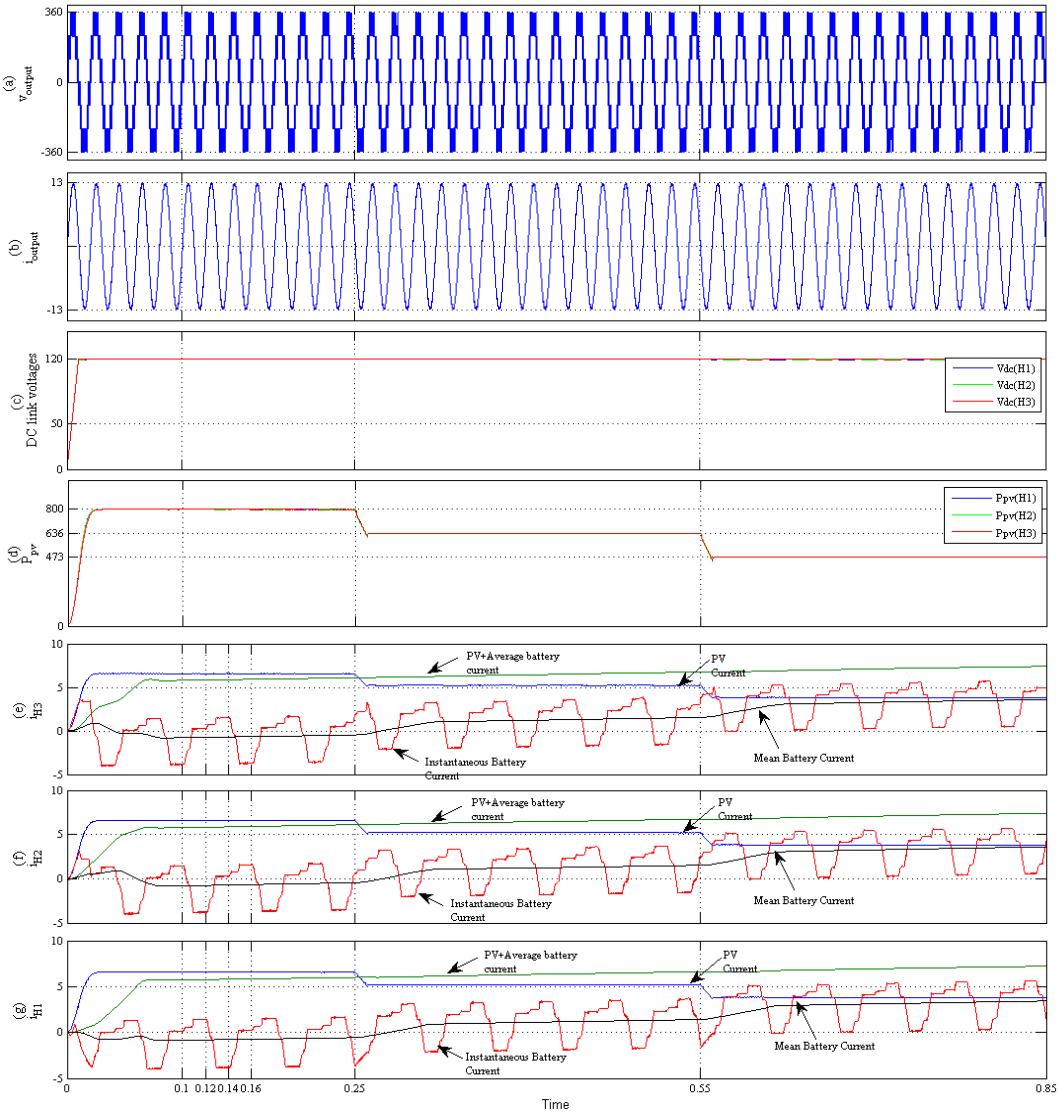


Fig. 4.6: Simulation waveforms for output terminal voltage and current, DC link voltages of each bridge, MPPT tracked power, PV and battery currents at each bridge.

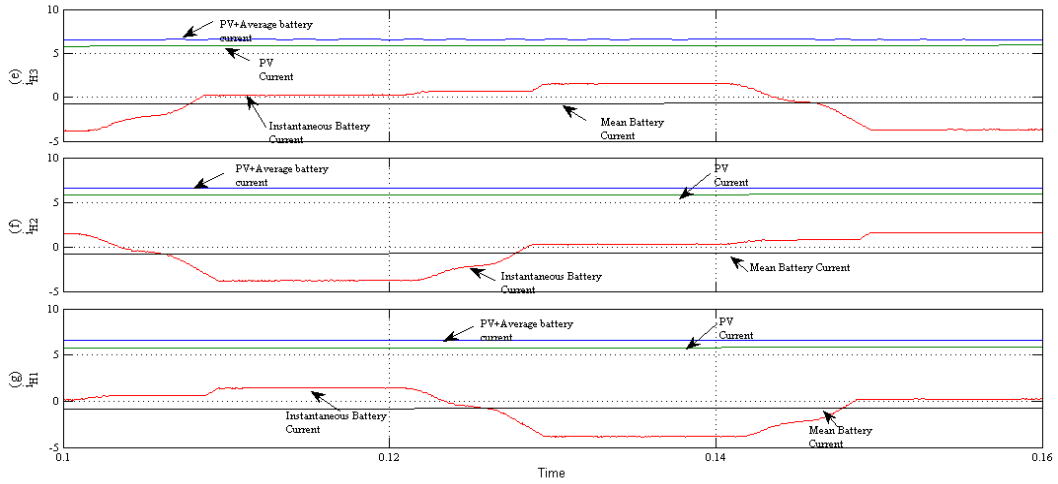


Fig. 4.7: Simulation waveforms for zoomed conditions of PV and battery currents.

entire space of operation of the system with varying insolation levels. The average battery current is computed by averaging instantaneous battery over three cycles corresponding to fundamental frequency. It may be observed from each Fig. 4.6 (e-g) corresponding to H1, H2 and H3 bridges that averaged power is balanced in all three bridges and achieved the steady state within three fundamental cycles. The averaged battery current at 1000 W/m^2, 800 W/m^2, 600 W/m^2 is -0.71 A, 1.21 A and 3.35 A respectively. Further, it may be observed that battery supported PV CHBMLI operation resulted in a sum of the averaged currents in battery and PV panel for each aforesaid insolation levels. Typically currents from PV panel and battery presented as couplets are respectively 6.58 A, -0.71 A; 5.11 A, 1.01 A; 3.01 A, 3.2 A; and of the hybrid battery supported PV panels are 5.87 A, 6.12A and 6.21 A which matches closely. To better understand the balancing of power in H1, H2 and H3 more closely, a section of the result is zoomed for exactly three cycles starting from t=0.1s to t=0.16s and the same is presented in Fig. 4.7. The direction of currents from battery and PV panels is as per depiction in Fig. 4.4. The beginning of the cycle from t=0.1s is marked by PWM Pulse set gl for H1, gu for H2 and gm for H3. The same may be verified from Fig. 4.5.

At t=0.1s as shown in Fig. 4.7 instantaneous battery current starts increasing from –3.84 A to 0.25 A to deliver the deficient load current not being supplied by PV unit as gating pulse g_m (explained in control section) is applied to H3 bridge till 0.12s (fundamental cycle). Between the same time intervals H2 is being applied with g_u, which represents

conduction for least interval of time resulting into a drop in battery current from 1.52 A to -3.84 A for charging of the battery to maintain the power balance as shown in Fig. 4.7. For the same time, interval gating pulse applied to H1 is g_l requiring maximum battery support as the bridge is in conduction for a maximum time interval in conjunction with PV unit to supply the load leading to increase in current from 0.25 A to steady state value of 1.52 A as shown in Fig. 4.7. Between t=0.12s to t=0.14s g_u, g_m and g_l gating pulses are applied respectively to H1, H2 and H3 bridges and explanation go same as discussed above for other cycles also.

4.6. Hardware Implementation of Single Phase PV off-Grid Cascaded Multilevel Inverter System

The hardware prototype of single phase off-grid PV multilevel system is developed for evaluation of the control algorithms for meeting the outlined objectives of the present work. Each DC link is connected to 2 PV panels via a DC-DC converter. dSPACE 1104 real time controller is used for generating the appropriate pulses. The LEM LV25P and

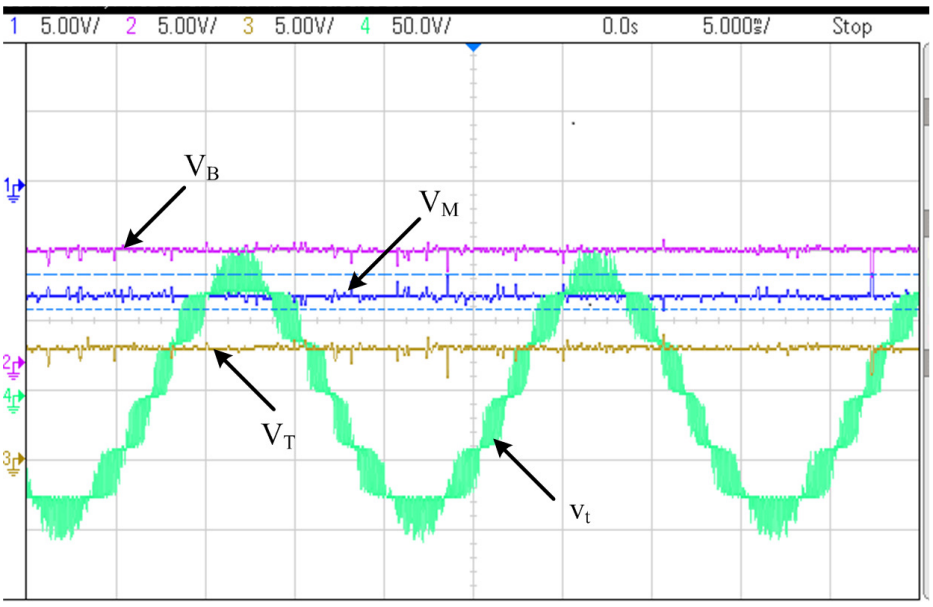


Fig. 4.8: Experimental results showing waveforms for DC link voltages (V_T, V_M, V_B), terminal voltage (v_t).

ABB EL 25 P1, Hall Effect voltage and current sensors are employed for sensing the terminal voltage, individual DC links and load side current of CHBMLI. In addition to PV, batteries are also connected to DC links via buck-boost converter whose control is given through PWM channel of dSPACE 1104.

4.7. Result and Discussion

The simulated performance of PV- CHBMLI is experimentally validated on the developed 1.5 KW (6 panels, each 250 W). The CHBMLI unit with inbuilt MPPT controller is experimentally validated and various waveforms are recorded using Agilent scopes.

4.7.1. Performance Evaluation of Off-Grid PV Fed Single Phase Cascaded Multilevel Inverter for UPF Operation

To investigate the control algorithm experimentally and to examine the system feasibility, various waveforms are recorded using Agilent scope as shown in Fig. 4.8 to Fig. 4.11. Fig. 4.8 shows the terminal voltage of CHBMLI together with 3 dc links voltages whose

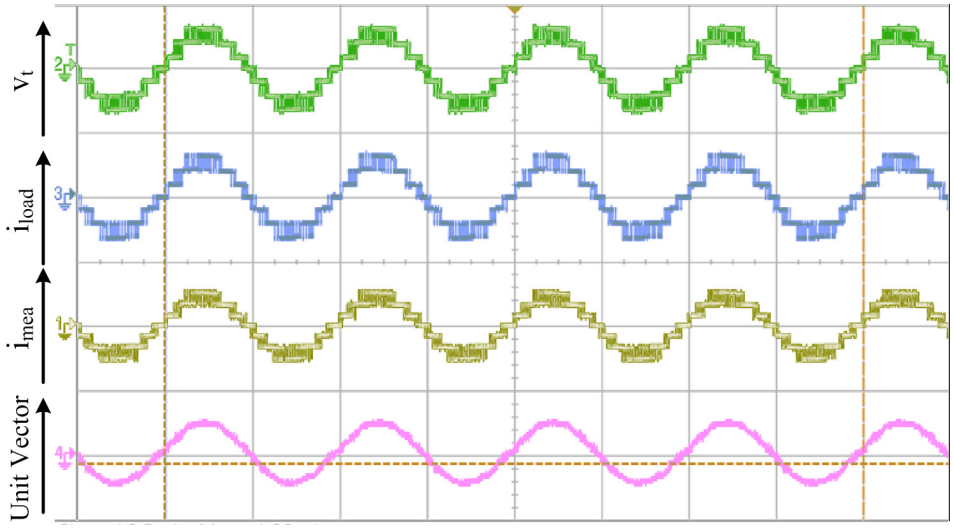


Fig. 4.9: Simulation waveforms for zoomed conditions of PV and battery currents.

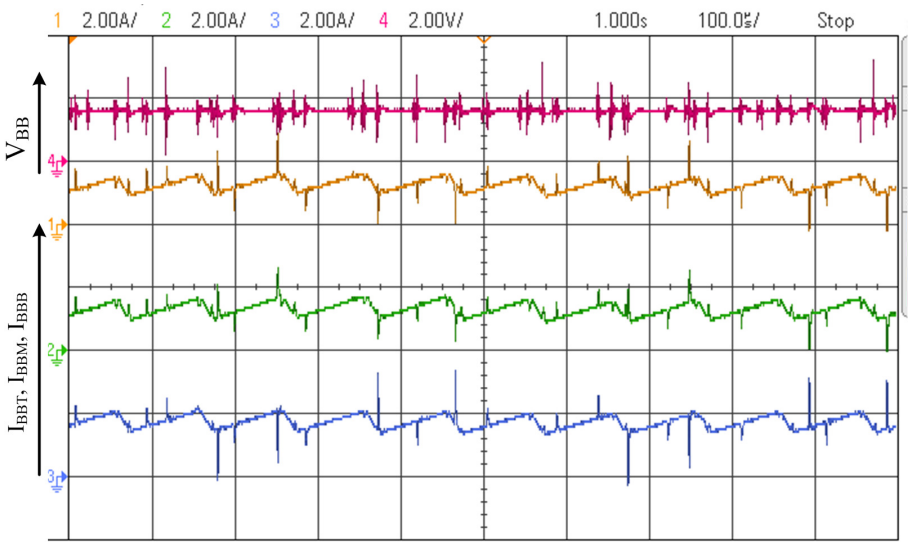


Fig. 4.10: Experimental result showing waveforms for Battery currents (I_{BBT}, I_{BBM}, I_{BBB}), Battery voltage (V_{BB}).

value is maintained at 65 V through battery storage connected via a dc-dc converter. The results clearly show equal dc link voltages across the capacitors irrespective of the irradiance level. Further the results show the 7 level terminal voltage of CHBMLI system. Fig. 4.9 shows the waveform for terminal voltage, inverter output current and unit vectors derived from the terminal voltage. From the figure, it is clear that current feed to a resistive load is in-phase with respect to terminal voltage.

4.7.2. Performance Evaluation of off-Grid PV Fed Multilevel System with Power Transaction through Battery

Under low insolation level, to feed power constantly to a load there is a need to maintain constant terminal voltage. To maintain constant terminal voltage, the battery comes in operation. Battery discharges to compensate the power due to low insolation level. Fig. 4.10 shows the battery being operating in discharging mode. Since the battery is connected to the DC links via a buck-boost converter, the zoomed battery current waveforms show instantaneous current rising and falling and repeating at switching frequency of 10 kHz. The battery voltage of 48 V is also shown in Fig. 4.10. Fig. 4.11 shows the PV output current connected at individual DC links, of particular insolation.

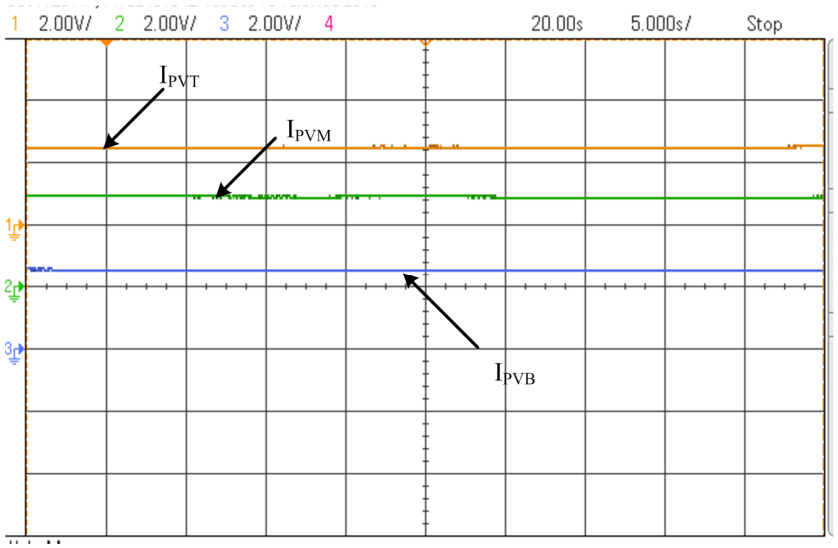


Fig. 4.11: Experimental result showing waveforms for PV currents (I_{PVT}, I_{PVM}, I_{PVB}).

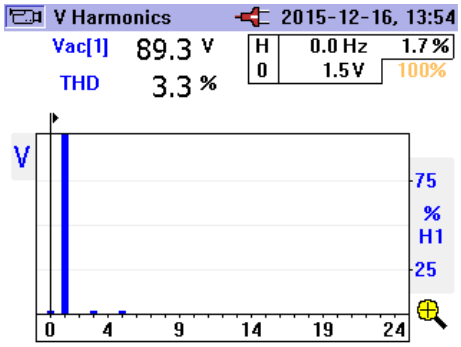


Fig. 4.12: Waveform showing THD of terminal voltage harmonics.

Fig. 4.12 shows the THD of terminal voltage which is well within limits (4.8 %) conforming to the IEEE 519 standards.

4.8. Conclusion

A control scheme for maximum power point tracked power balancing of a battery supported PV panels for each H bridge of 7 level multilevel inverter has been successfully demonstrated through simulation and experimental results. The power balancing at each dc bus of H-bridge is successfully achieved in three fundamental frequency cycles. It has also been demonstrated through results that power balancing at each level of CHBMLI yields better utilization of the capacity thus increase the lifetime

and reduce the requirement of the high capacity battery thus provides cost effective solution. CHBMLI configuration offer opportunity to have lower DC bus voltage, thus lowers the boost ofvoltage required and multilevel output reduces THD, stress on switches, switching losses and also it requires low capacity filters. The scheme operates effectively at varying insolation levels and is fast, simple and easily implementable. The scope of integrating more number of levels of MLI is inherently embedded in the scheme, which in turn would level the power more effectively with an increase in the levels.

Chapter V

CONTROL AND IMPLEMENTATION OF OEIM PUMP DRIVE USING CASCADED MULTILEVEL CONVERTER

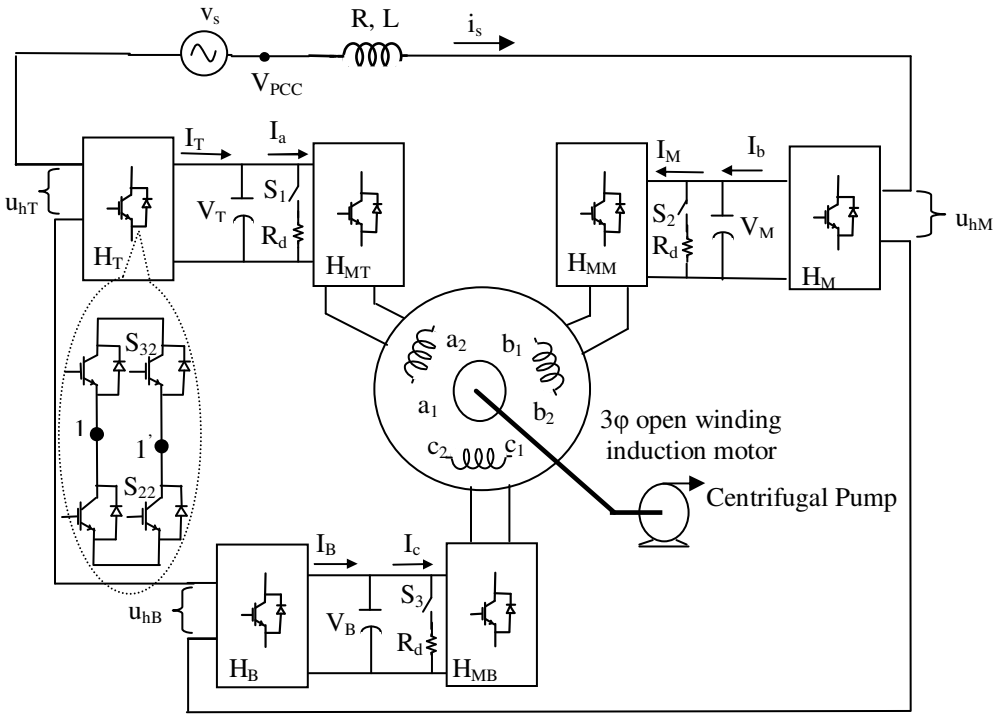
5.1. Introduction

Having already established the control logic for off-grid application, the investigation is due for CMC structure suitability for grid-tie application feeding variety of loads. In this chapter a major agricultural/residential application of CMC unit for water pumping is presented through OEIM drive. The main emphasis has been laid out on the splitting single phase supply into 3 phases via 3 independent DC links with the help of phase shifted control technique discussed in chapter 3. The effectiveness of control is probed against the possibilities of unbalance voltage and uneven power drawn from the individual DC links. The embedded control forces the system to exhibit balanced drive operation amidst uneven losses across the H-bridges and /or unbalanced motor loading effect during transients or intermittent operation. The effectiveness of proposed control algorithm is validated both through simulation and experimentation on the developed same scale hardware prototype.

5.2. Features of OEIM Pump Drive using Single Phase Cascaded Multilevel Converter

The present configuration utilizes the advantage of both cascaded H-bridges structure and open end winding 3 phase induction motor drive for pumping using single phase AC supply. In the presented system cascaded converter active rectifier (CCAR) is controlled to obtain 3 separate DC links. On each DC link separate H- bridge inverter is placed and controlled to excite individual windings of open end induction motor. The proposed configuration and control enjoys many advantages, which offsets the cost of additional

hardware: The configuration offers the advantage of 3 separate DC links each having 1/3rd of the total DC voltage and power rating, which enables the reduction in the voltage rating of capacitor thus increasing the life cycle of the drive on account of the reduced voltage stresses; System becomes more modular and compact; The drive can offer low voltage ride through capability as any disturbance on AC side will be distributed equally on the three DC links resulting in only 1/3rd instantaneous dip in the voltage with respect to the reduction in voltage at motor terminals when fed from 3 phase inverter with common DC link; The power is drawn from AC is with reduced voltage THD and avoids bulky filter requirement; Immunity against unbalanced DC link voltages across the H-bridges caused due to disturbance from either the source and / or the load side, which is incorporated in the control algorithm ensuring smooth drive operation using simple V/f



v_t (terminal voltage)= $u_{hT} + u_{hM} + u_{hB}$

v_s – Source Voltage
i_s - Source Current
H_j- H-bridges at front end
H_{Mj}- H-bridges as motor drive
T- Top, M- Middle, B-Bottom

Fig. 5.1: System configuration of CCAR feeding OEIM Pump loads.

control.

5.3. System Configuration of Single Phase Cascaded Multilevel Converter

Fig. 5.1 shows the schematic of seven level CCAR converting 240 V, 50 Hz AC to DC with 3 different DC link feeding varying motor pump load (3φ, 1 hp, 200 V). Seven level CCAR is made by connecting 3 H-bridges (H_T, H_M, H_B) consisting of 2 modules of IGBT in each bridge in series as shown in Fig. 5.1. An interface inductor is connected in series with CCAR on AC side to enable requisite power drawn from grid. The control of the front end is made in such a way that near unity power factor is maintained at PCC for such drawing of power. The DC link capacitor of CCAR is selected on the basis of allowable change in DC link voltage and power exchange through each link. The individual winding of OEIM is connected at each DC link via H-bridges (H_{MT}, H_{MM}, H_{MB}). For protection point of view the load controller is also connected at each DC link so that, overvoltage if arising due to switching off the motor pump load can be easily avoided. The reference for load controller (kept at 180V) is made above the reference DC link voltage (kept at 160 V) so that unwanted switching of load controller can be averted.

5.4. Control Approach for Single phase Cascaded Multilevel Converter

Based on control system design, Fig. 5.2 and Fig. 5.3 shows the complete control logic

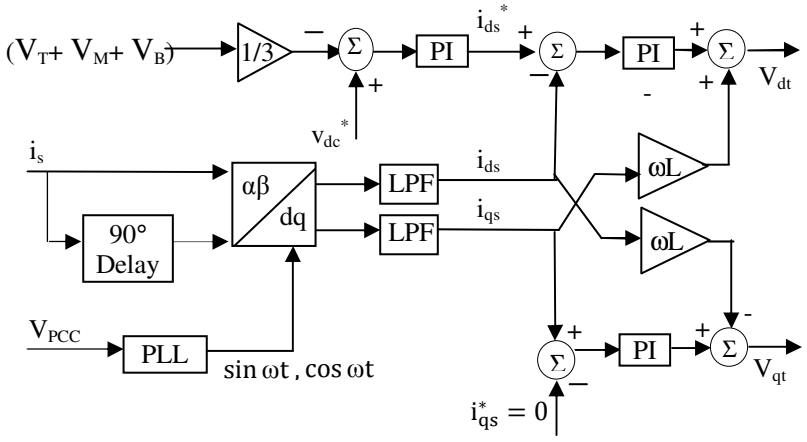


Fig. 5.2: Control blocks of proposed CCAR Configuration.

for arriving at switching function of individual H-bridges for feeding pump load. Moreover the single phase source has to also cater varying losses across individual H-bridges and unbalanced power demanded by the pump load. For catering such varying power through individual H-bridges by keeping DC link voltage constant for the same source current would require varying modulation index for each bridge. The individual

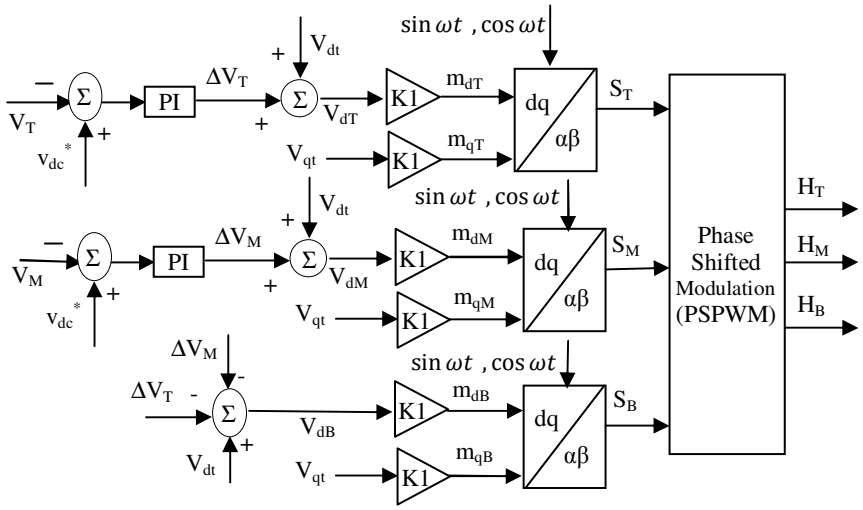


Fig. 5.3: Control blocks of proposed CCAR configuration for handling uneven losses across the H-bridges.

modulation index of each H-bridge is obtained by passing the error between the reference DC link voltage and the sensed DC link voltage through PI controller to add ΔV_j to V_{dt} as shown in Fig. 5.3. ΔV_j represents the compensated voltage added to the d-component of the terminal voltage for uneven losses. Only two PI controllers are required to formulate the control for balancing the DC link voltage since third may be derived from the two PI's controller output keeping overall change in voltage as zero (ΔV_B=- (ΔV_T+ΔV_M) as shown in control Fig. 5.3.

The scaled value as per modulation index for each H-bridge along d –axis and q-axis is reverse park transformed and α component is retained (called continuous switching (S_j). These switching functions are further compared with phase shifted carrier waveform to arrive at individual switching command H-bridges. For each individual H-bridge the reference switching function is controlled separately depending on the losses, resulting into varied magnitude and phases of the switching functions.

5.5. Feasibility Analysis of the Designed Controller using Bode Plot for Cascaded Multilevel Converter

The transfer function given as per (3.24) given in chapter III is used to draw bode plot for studying the dynamic model for stability and control design having multiple PI's. Using the values given in Table (5.1) for the PI's controllers, the bode plot is drawn as in Fig. 5.4. From the gain and phase plot with respect to frequency, it is clear that phase margin of the system is around 112°, i.e. high enough to accommodate any transient and disturbance. This justifies the higher stability of the system particularly suitable for the drive operation. From the plot it is also clear that near operating frequency i.e 2 kHz, gain decreases linearly and phase angle is stable and constant.

5.6. Control Approach for V/F Control of Open End Winding Induction Motor

Every induction motor comes with 6 terminals connections which may be connected in star or delta by proper connections. To get the open end winding induction motor, the end point of each phase is left open so that individual phase can be fed through separate H-bridges.

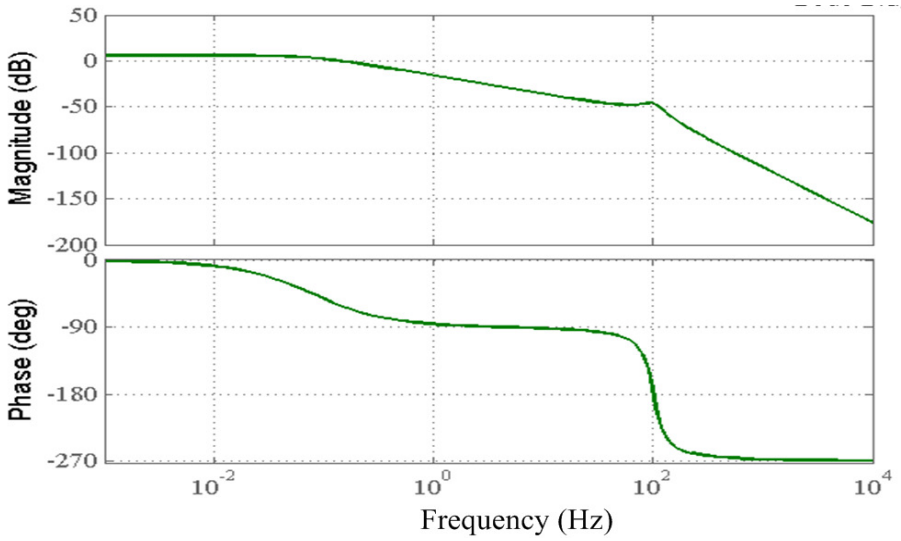


Fig. 5.4: Stability analysis of controller using Bode plot.

Electromagnetic Torque is expressed as (discussed in section 3.5):

$$T_e = \frac{3P}{4} L_m (i_{qs}i_{dr} - i_{ds}i_{qr}) \quad (5.1)$$

Where, P is number of poles. For pump load the load torque is expressed as (neglecting viscous friction):

$$T_L = K\omega_m^2 \quad (5.2)$$

Therefore power is directly proportional to cube root of speed as:

$$P_L = K_m\omega_m^3, \text{ where } K_m \text{ is torque constant} \quad (5.3)$$

$$P_a = (1\text{-}s)\, P_L \quad (5.4)$$

Where P_a is air gap power, ω_m is the pump speed, s is the slip. Neglecting the losses across the stator, the air gap power is equivalent to the electrical input power fed via H-bridges controlled using v/f. Further neglecting the losses across the bridges this is being fed by single phase AC source as:

$$I_{ds}\,[m_{dT} + m_{dM} + m_{dB} - j(m_{qT} + m_{qM} + m_{qB})]V_{dc} = (1\text{-}s)K_m\omega_m^3 \quad (5.5)$$

Further $\omega_m = (1\text{-}s)\,\omega_{ms}$, where ω_{ms} is the synchronous speed. Replacing ω_m with ω_{ms}, the equation may be further written as:

$$[m_{dT} + m_{dM} + m_{dB} - j(m_{qT} + m_{qM} + m_{qB})]I_{ds} = (1\text{-}s)^4K_m/V_{dc} = K_{mt}(1\text{-}s)^4\omega_{ms}^3 \quad (5.6)$$

where $K_{mt} = K_m/V_{dc}$.

From (5.6) it is clear that the change in reference speed command will result into both change in slip (s) and ω_{ms}.

$K_m = 0.000222$ is considered corresponding to rated condition of the motor (Using (5.3) at 746 W and 149.7 rad/s). Each phase of the open end induction motor is fed from

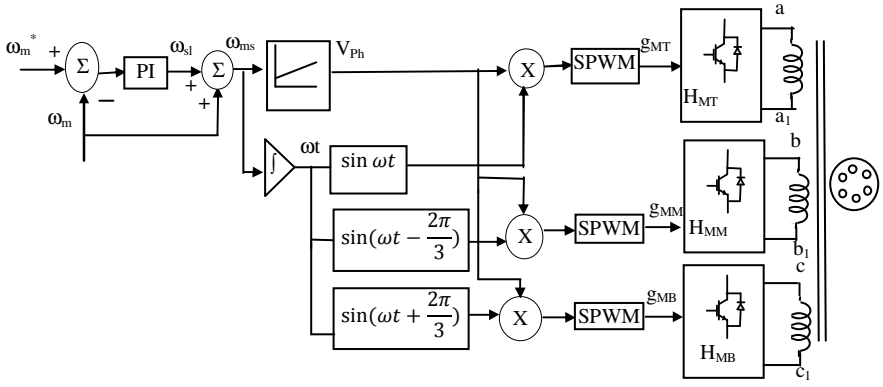


Fig. 5.5: Control blocks of V/f control of OEIM drive.

separate H-bridges, which are controlled through 3 phase SPWM scheme modulated for reference signals obtained from the V/F controller as shown in Fig. 5.5. With splitting of voltage using proposed structure and further using V/F control on split H-bridge inverter reduces dv/dt problem. Moreover due to absence of path for 3rd harmonic component leakage current reduces.

5.7. MATLAB Based Simulation of Single Phase Cascaded Multilevel Interfaced 3 Phase Pump Drive

The single phase AC power source, interface inductor, CCAR, hybrid loads representing power converter for LED lighting and pump load with open end induction motor drive is modeled in MATLAB simulink/Power system block set. To check the applicability of the proposed algorithm first the load of 65 ohm is connected across each DC link of H-bridges accumulating to overall power of 1170 Watt. After a gap of few seconds, a step increase in load is applied by connecting 80 ohm of load across one of the DC bus intentionally creating unbalanced loading to gauge the effectiveness of the algorithm for balancing of DC buses of the H-bridges. The algorithm for balancing the dc buses is kept slow paced in order to avert any oscillations, an incorporating large value of capacitors (2200 μF) to support the dc bus meant for availability of clean dc voltage for connected loads. However selection of such a large value capacitor poses a power quality issues on

TABLE 5.1

Parameters of Cascaded Converter and OEIM

Main supply voltage 1φ, Line Frequency	240V, 50 Hz
DC link voltages	160V
DC link Capacitance (C)	470 μF
Interface Inductor (L), Resistance (R)	6 mH, 0.4 ohm
Motor Rated Voltage , Frequency, Power	3 phase , 200V , 50 Hz, 1 Hp
Motor Rated Speed	1428 RPM
Rotor Resistance (R_r), Stator Resistance (R_s)	2.26 Ω, 2.7 Ω
Motor Mutual Inductance (L_m)	138.4 mH
PI_1	K_{P1}=5; K_{i1}=30
PI_3	K_{P3}=0.1; K_{i3}=5

the grid side. The effectiveness of control algorithm is validated even in this extreme condition by making THD of current less than 5 % at unity power factor meeting IEEE 519 standard. The effectiveness of the control algorithm has also been tested by connecting active load (open winding 3 phase induction motor pump load) via back to back H-bridge controlled using scalar techniques. The detail of the parameters of the open winding induction motor and multilevel active rectifier is shown in Table 5.1.

5.8. Hardware Implementation of Single Phase Cascaded Multilevel Interfaced 3 Phase Pump Drive

The same scale/rated hardware prototype of cascaded active multilevel rectifier is developed for evaluation of the control algorithms for meeting the outlined objectives of the present work. The development of hardware prototype includes fabrication of power circuits, a target board hosting DSPIC33FGS502 microcontroller, driver circuits, sensor interfaces and other cards meant for synchronized switching of the power switches as shown in Fig. 5.6. An in house PCB design is done to make these hardware electronics

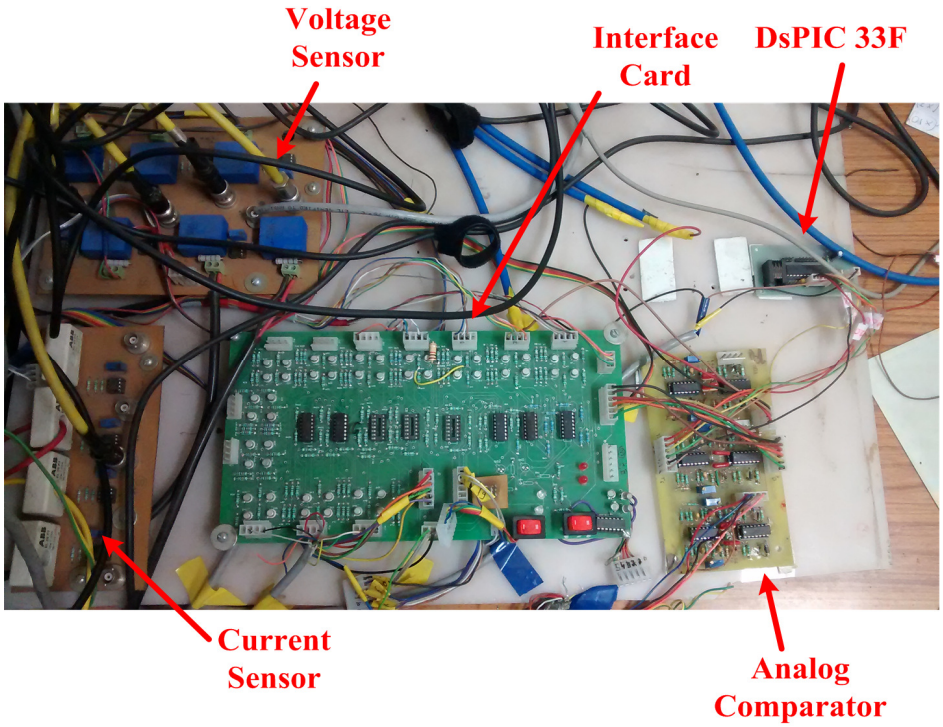


Fig. 5.6: PCB's of interfacing, DsPIC33f and control cards.

cards compact and easy to handle with requisite protection scheme. The H-bridge utilized to construct CCAR use 2 IGBT modules of one leg (SKM50GB063D) each and 3 such units are connected in cascade to form 7 level of multilevel active rectifier. Each DC bus of the H-bridge is supported by 450 V, 2200 μF capacitor for providing ripple free DC to the connected loads. Each module of IGBT is driven through Skyper pro 32 driver as shown in Fig. 5.7. Hitachi made 200 V, 1 HP motor is used with segregated neutral point to enable its connection with separate set of H-bridge inverters fed from three individual DC buses evolved through CCAR connected to single phase distribution grid as shown in Fig. 5.8. The speed of the motor is estimated through hollow shaft incremental encoder mounted on the motor shaft. dSPACE 1104 real time controller and DSPIC33FJ16G502 microcontroller are used for knitting the control of CCAR and the scalar controlled induction motor drive. The LEM LV25P and ABB EL 25 P1, hall effect voltage and current sensors are employed for sensing the voltage at PCC, individual DC links of CCAR and source side current of CCAR respectively. The sampling frequency of simultaneous sampled ADC channels is kept at 10 kHz, which is also corresponds to real time compilation loop of dSPACE 1004 real time controller as shown in Fig. 5.9. The phase shifted PWM of 2 kHz is generated through three compare units of PWM timers of the DSPIC33FGS502 microcontroller to accurately shifting the carrier by 60° with requisite hardware interface.

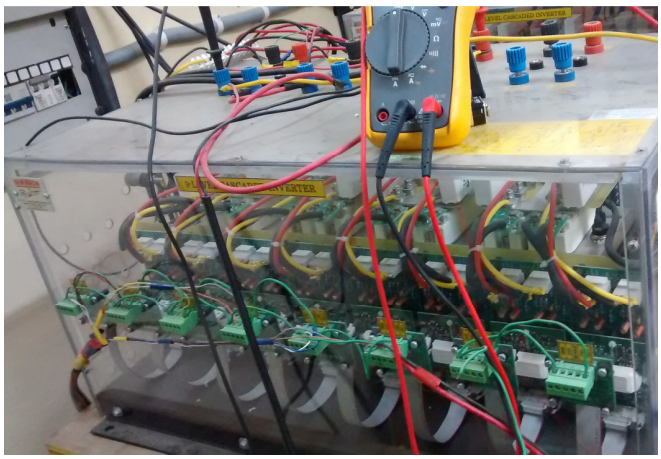


Fig. 5.7: Experimental hardware unit of cascaded multilevel converter/inverter.

Fig. 5.8: Open end winding induction motor with digital encoder and fan load.

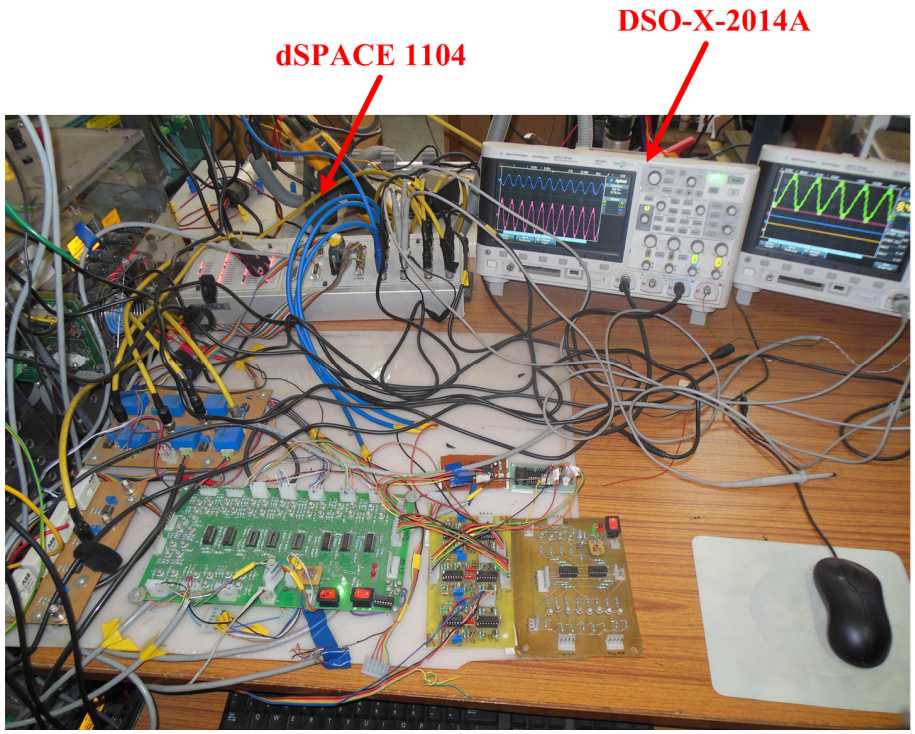


Fig. 5.9: Experimental setup of multilevel system showing dSPACE and DSO's.

5.9. Result and Discussion

The performance of the proposed configuration meant for feeding three phase dynamic load together with static load is evaluated both through simulation under MATLAB/ simulink and experimented on developed same scale prototype of CCAR. The effectiveness of the control algorithm to balance the DC bus is demonstrated through perturbed static and dynamic loading so as to consume different power at different DC buses of the CCAR. The demonstrated simulation and experimental research show close

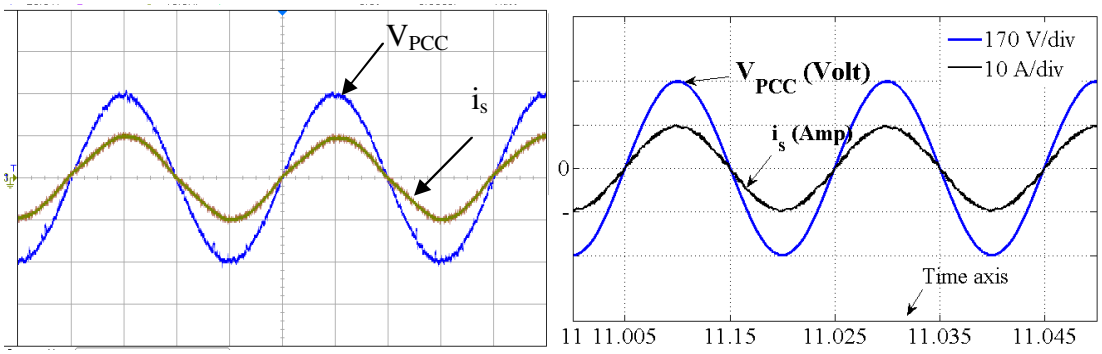


Fig. 5.10: (a) Experimental result showing source voltage (170 V/div), and source current (10 A/div) (b) Simulated source voltage, and source current.

matching to validate the proposed concept of single phase CCAR feeding three phase motor pump load, even under unbalanced power drawl at different CCAR DC buses. To show the accurate dynamics on AC and DC sides simultaneously triggered oscilloscopes are used.

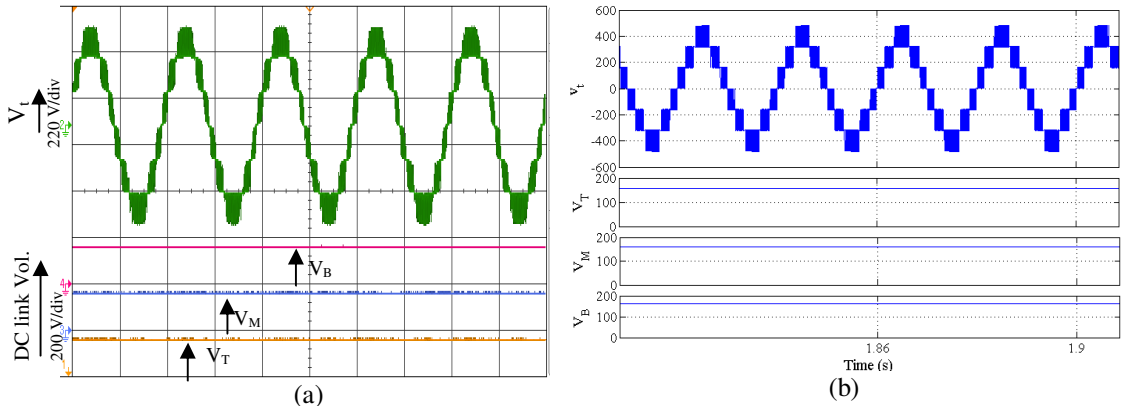
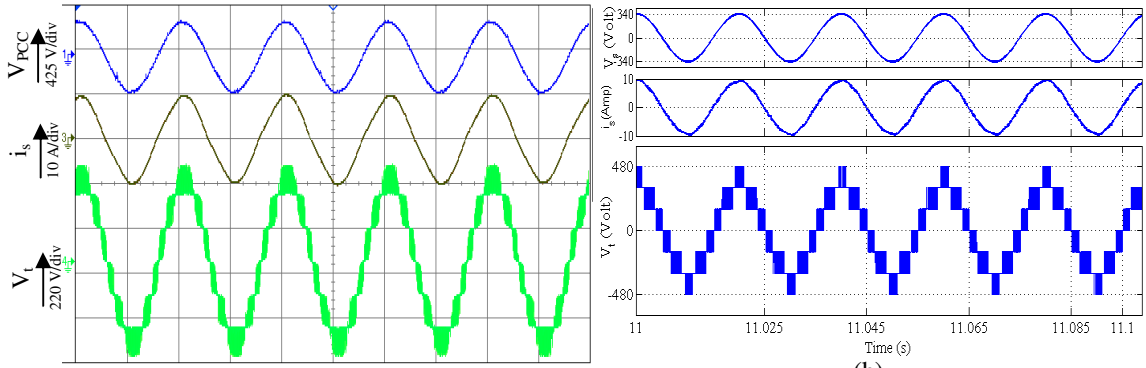


Fig. 5.11: (a) Experimental results showing terminal voltage V_t and DC link voltages V_T, V_M , V_B, Time- 10 ms/div (b) Simulated results showing terminal voltage Vt and DC link voltages V_T, V_M , V_B.

5.9.1. Performance Evaluation of Single Phase Cascaded Multilevel Converter for Balanced DC Links and UPF Operation

For full discourse of experimental and simulation studies source current is maintained at unity power factor as depicted in experimental and simulation results as shown in Fig. 5.10 (a) and Fig. 5.10 (b) respectively. The system is started firstly with balanced loading conditions and steady state experimental and simulated results are shown respectively in Fig. 5.11 (a), Fig. 5.11 (b) and in Fig. 5.12 (a), Fig. 5.12 (b). It is clearly evident from the voltages depicted in Fig. 5.11 that all three DC links are balanced and maintained at 160 V. In the same result of oscilloscope the terminal voltage is maintaining seven levels, where each level is of same magnitude, which also corroborate the existence of balanced DC buses. The simulation results show very close matching of experiment results though depicted in different scales. To further establish the effectiveness of the proposed control for UPF operation of converter the voltage at point of common coupling (V_{pcc}), source current (i_s) and terminal voltage (V_t) are shown in Fig. 5.12 (a), where it may be observed that the source current is in phase with V_{pcc}, and terminal voltage of CCAR maintains 7 levels. The simulation results depicted in Fig. 5.12 (b) duly appropriately cropped show very close matching with experimental results.



(a) (b)

Fig. 5.12: (a) Measured zoomed source voltage (V_{pcc}), source current (i_s) and CCAR input voltage (V_t), and time (10 ms/div) (b) Simulated zoomed source voltage (V_{pcc}), source current (i_s) and CCAR input voltage (V_t).

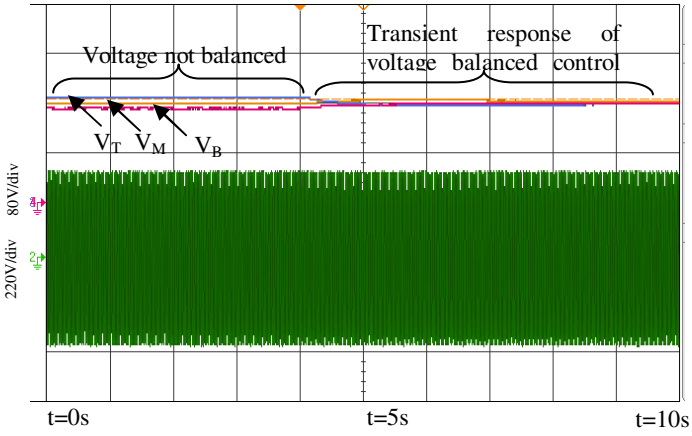


Fig. 5.13: Experimental results of DC link voltages (V_T, V_M, V_B) and terminal voltage (V_t) showing balanced control scheme.

To demonstrate the effectiveness of proposed control algorithm in case of unbalanced

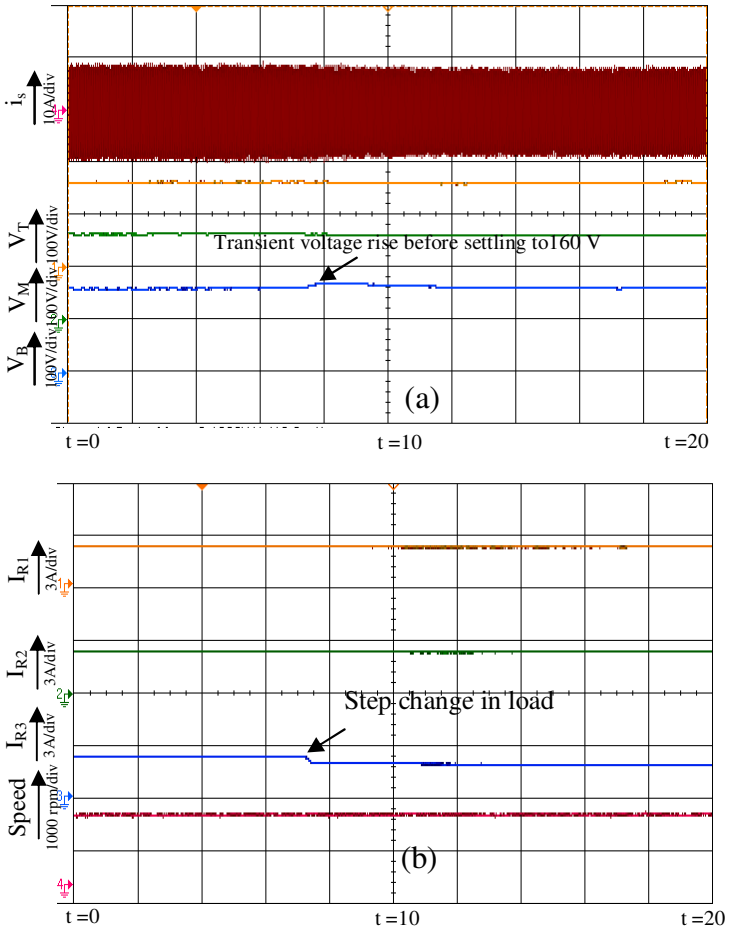


Fig. 5.14: Experimental result showing waveforms for (a) Source current (i_s), DC link voltages (V_T, V_M, V_B) (b) LED's load currents (I_{R1}, I_{R2}, I_{R3}) and Motor speed (in rpm).

loading on the DC bus, intentional unbalancing is created by decreasing the load on DC bus of the bottom bridge by 75 watt resulting instantly in unbalanced dc link voltages, as shown in Fig. 5.13. At t=4s, voltage balancing control algorithm is executed and results into balance DC link voltages across H-bridges by altering the switching function (S_T, S_M, S_B) with effect from at t= 7s onwards.

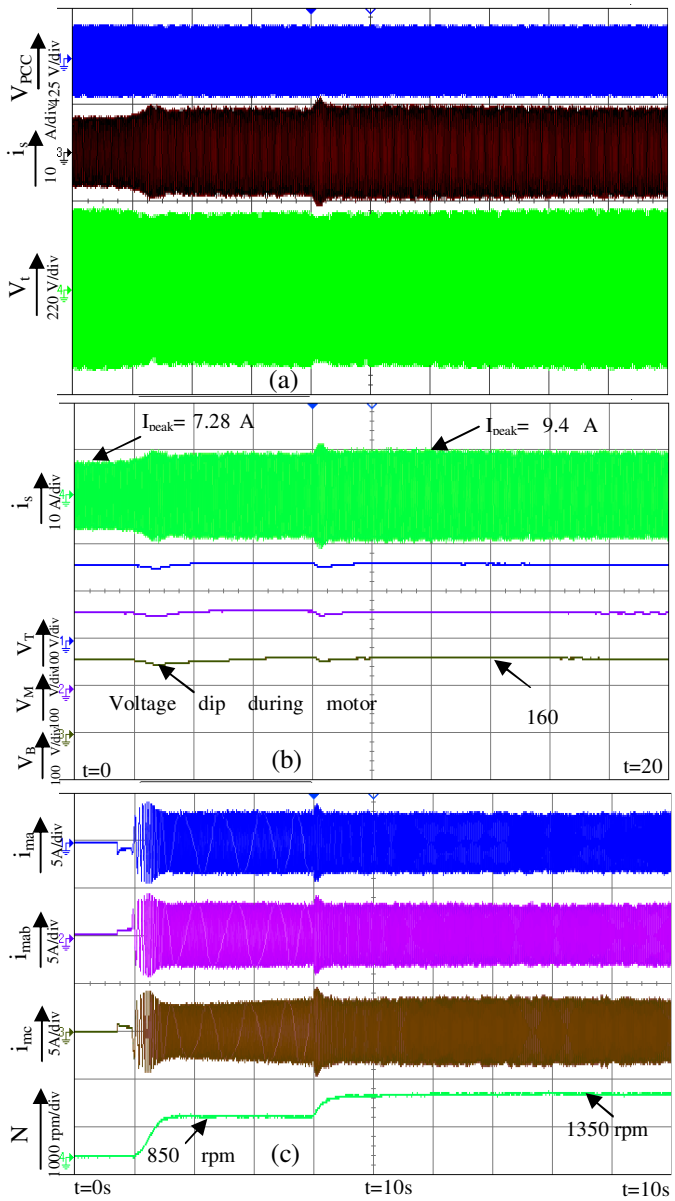


Fig. 5.15: Experimental results showing (a) source voltage (V_{pcc}), source current (i_s) and CCAR input voltage (V_t) (b) source current (i_s) and DC link voltages (V_T, V_M, V_B) (c) motor currents (i_a, i_b, i_c), motor speed (rpm) under change in motor pump load with change in speed.

5.9.2. Performance Evaluation of Single Phase Cascaded Multilevel Drive System Under Perturbing Pump Load Using V/F Control

Further to study the dynamics of the CCAR in the presence of perturbing unbalanced loading the experiment is performed afresh to validate the proposed algorithm. As shown in Fig. 5.14 (a)-(b) with step decrease in load at around t =7.6s, current decreases from 2.46 A to 2 A at one of the dc link where, there is small rise in the corresponding dc link voltage (V_B), before the algorithm damps the rise and balances the DC bus by taking out the power from the corresponding DC bus making all the voltage returning to 160 V quickly resulting in decrease in source current Fig. 5.14 (a).

Further the testing of algorithm is explored for connectivity to dynamics load which drastically affect the loading at DC bus. To validate the proposed algorithm for single phase of CCAR with motor pump load on its three DC buses through scalar controlled 3 phase inverter experimental results are shown in Fig. 5.15. To study the dynamics and evaluate the performance with dynamic load, initially a balanced fixed connected load of 1170 watt is considered on all the three DC links together. The source voltage and current waveforms are shown during t= 0 to t= 2s (with respect to origin) in Fig. 5.15. (a). It is clearly seen in Fig. 5.15 (b) that source current (i_s) is around 5.05 A for balanced dc link voltage of 160 V on each DC link. At t=2s in Fig. 5.15 (b), when motor pump load drive is started with constant v/f control and the speed reference is ramped up to 850 rpm, resulting in increase in motor phase currents with frequency gradually increasing from low value to rated value. It may be observed that within 0.75s the starting transient of the motor diminishes and it settles down to reference value of 850 rpm without any overshoot in accordance with properly tuned speed controller. As soon motor picks up speed at t=2s the demanded power of 105 watt is instantly met by the tank capacitors on the three dc links resulting into small dip in the dc link voltages, which recovers fast due to the support of voltage balancing control algorithm, leaving footprint of peaking in source current (i_s) as shown in Fig. 5.15 (a). The terminal voltage also experiences a dip and the same is observed in Fig. 5.15 (a).

Further to evaluate the dynamic response of the CCAR a step change in speed commanded at t= 8s, from 850 rpm to 1350 rpm as shown in Fig. 5.15 (c). Tracking the given reference command as shown in Fig. 5.15 (c) motor accelerated to 1350 rpm in

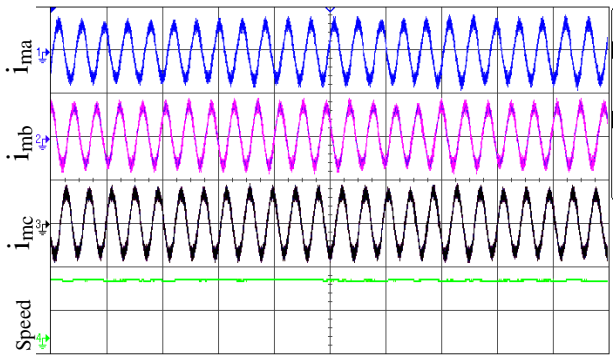
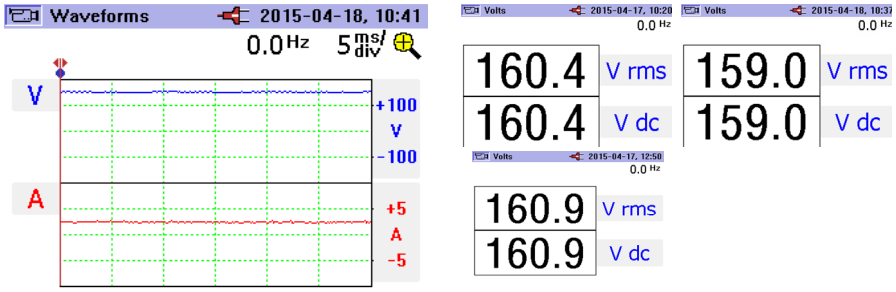


Fig. 5.16: Experimental results showing zoomed motor current i_{ma} (5A/div), i_{mb} (5A/div) , i_{mc} (5A/div) and speed (1000 rpm/div).

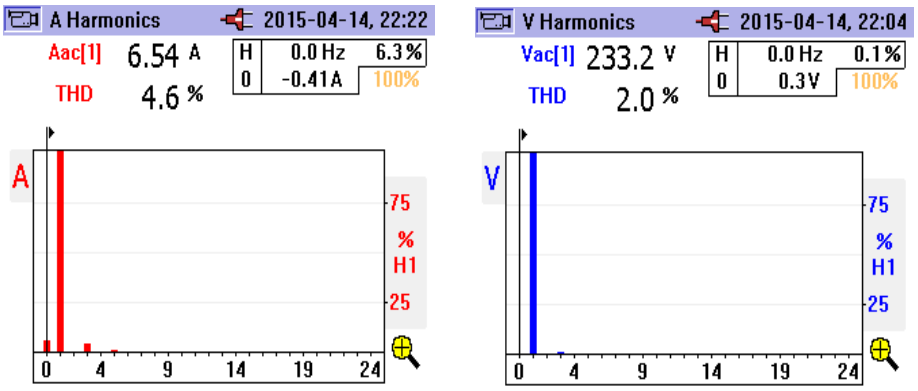
roughly 0.6s without any overshoot. It may be further observed in Fig. 5.15 (c) that the increased speed command further increases the torque demand resulting into increased



(a) (b)

Fig. 5.17: (a) Waveform showing one DC link voltage V_M and passive load current I_{R2} (b) DC link voltages V_T,V_M,V_B using Fluke 345.

overall active power demand of the motor from 105 watt to 375 watt in addition to constant load of 1170 watt. Such transient causes a small dip in dc link voltage at t= 8s as evident in Fig.5.15 (b), which is quickly recovers within 1 sec. The steady state response showing the balanced current as shown in Fig. 5.16. To assess the power quality and the DC link voltages, and load currents across one H-bridge during balanced condition is recorded using Fluke 345 II single phase power quality analyzer and waveform is shown in Fig. 5.17 (a). The PQ analyzer for DC link voltages is also shown in Fig. 5.17 (b).



(a) (b)

Fig. 5.18: (a) Waveform showing THD of source current harmonics current I_{R2} (b) THD of CCAR terminal voltage V_t.

Harmonics are also analyzed with the same PQ analyzer for input terminal voltage (V_t) and source current (i_s) and the same are shown in Fig. 5.18 (a) and Fig. 5.18 (b) respectively. The observed THD conforms to IEEE 519 standard, where the current THD is around 4.6 % with majority of 3rd harmonic component with a magnitude 4.35 % of fundamental and for voltage the THD is around 2.0 % with 3rd harmonic component around 1.8 % of the fundamental.

5.10. Conclusion

The proposed power electronics hardware for splitting single phase supply to 3 phase utilizing CCAR for feeding 3 phase constant v/f controlled OEIM is demonstrated through both by simulation and experimental results for satisfactory operation with improved power quality. The effectiveness of the control algorithm under influences of dynamic and uneven losses across the bridges is clearly demonstrated through results. Despite of different dynamics applied to CCAR, the source current always remains always in phase with source voltage ensuring improved PQ and keeping the entire voltages of the DC buses constant and balanced ensuring smooth operation of the pump drive immune to the disturbance from AC or DC side. With the d-q model applied to CCAR system, the control algorithm remains immune to any noise and harmonics in voltage at PCC. The proposed algorithm and structure has advantage of modularity, high

efficiency and meets the requirement of varying dynamic pump load. The structure has its advantage of small size dc capacitor, which in turn guarantees the extended life ensuring smooth operation of pump drive.

Chapter VI

SMART OEIM PUMP DRIVE AND DC LOADS USING CASCADED MULTILEVEL CONVERTER

6.1. General

With the establishment of grid connected CMC topology for voltage splitting suitability for pump drive, a smart and advanced control is due for investigation. In this chapter the CMC structure is probed for providing power through 3 different DC links. Such arrangements should facilitate reduction of the voltage rating of capacitors and enable smooth operation of vector controlled open end winding induction motor (OEIM) pump drive in addition to other DC load, such as variable illumination LED (VIL) lighting. The control employed for CMAR enhances the grid support operation by flexibly controlling the power on the DC links. The control is invoked by adjusting the speed of the pump by sensing the grid frequency using droop characteristics thereby acting as smart pump load (SPL). The effectiveness of the proposed configuration and control is investigated both through simulation and experimentation on same scale hardware prototype.

6.2. Features of OEIM Pump Drive using Single Phase Cascaded Multilevel Converter

The SPL unit for autonomous variable speed pumping system with single phase grid connectivity is presented. The variable speed pumping system is facilitated by 7 level cascaded multilevel active rectifier feeding three DC links working as one end of the back to back connected H-bridges, in turn forming three phase connection to operate the pump as vector controlled OEIM drive. With the proposed structure for SPL, the problem of the conventional and non-interactive pumping system can be easily circumvented due to the structure and its flexible control for variable pump load with reduced DC link

capacitor size. Further, due to the division of voltage along the three DC links any stress from grid side will also get distributed on the split DC links, leading to an increased lifetime of the capacitor and the drive. Such variable speed smart pump load which operates as per variation in grid frequency by controlling the power drawn from the AC mains. When the demand peaks up during a day, sensing the grid frequency, the droop characteristics dictates the power drawn through the SPL and the same is matched by an appropriate reduction in the speed of the pump load. For the proposed control applied to the SPL, the droop rate is decided based on the prevailing grid frequency and the individual capacity of the pump drive load. When the CMAR is also feeding variable illumination LED (VIL) on the DC link, the control is then altered according to the droop rate considering the net reduction in equivalent loads on DC links and the decrease/increase in speed resulting in increase/decrease in power demand from the grid to stabilize the grid frequency. In rural areas with many such proposed connected SPL, the grid will be more stabilized and load shedding would be in turn averted.

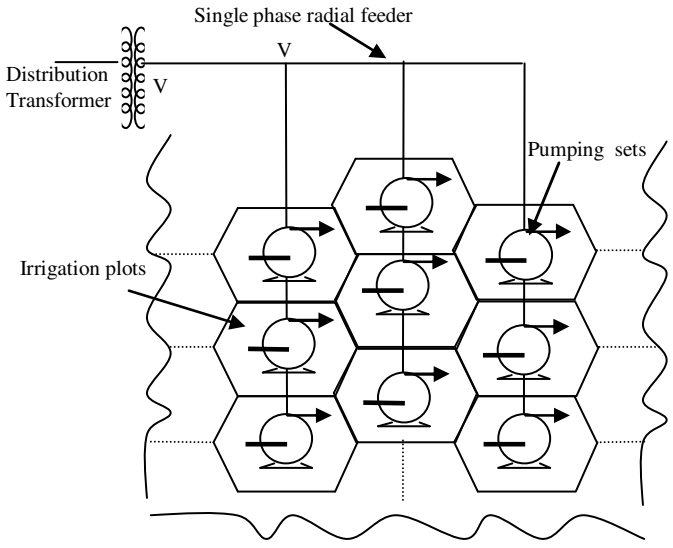


Fig. 6.1: Conventional system of pumping.

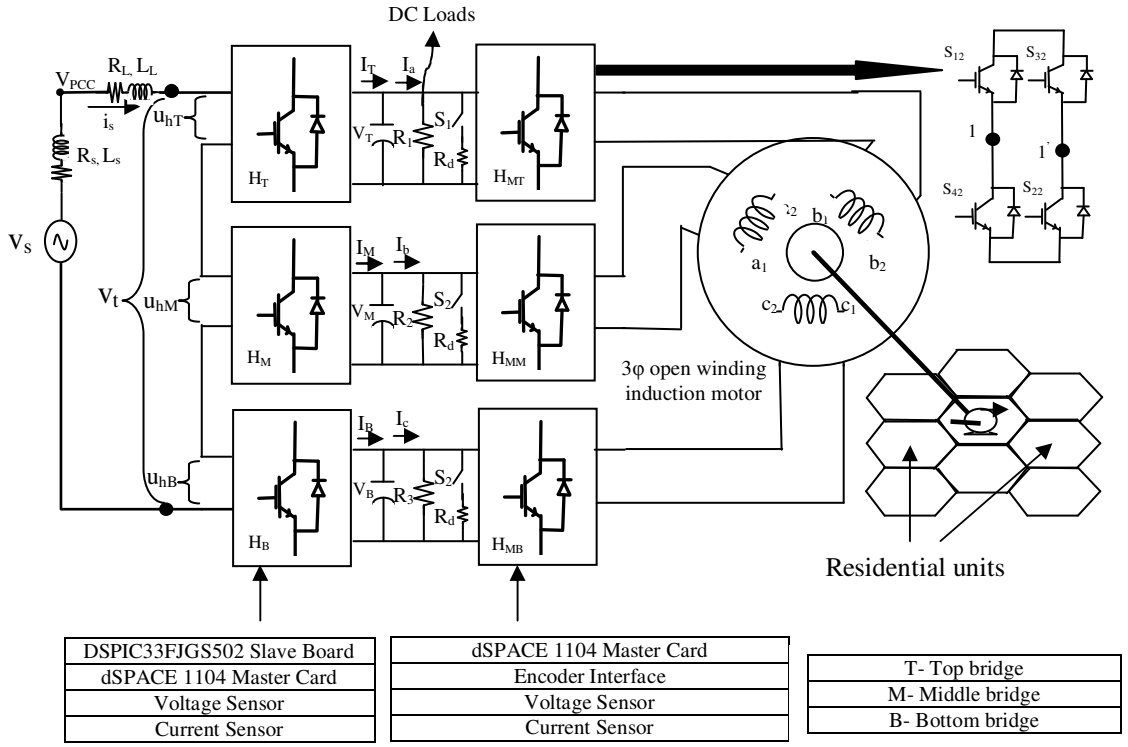


Fig. 6.2: Proposed system Configuration for SPL operation.

6.3. System Configuration of Single Phase Cascaded Multilevel Converter

Fig. 6.1 depicts a broader view of the linked problem associated with connectivity of array of pumps on residential units on a single phase distribution system. Fig. 6.2 shows the proposed SPL connected to a 240 V, 50 Hz single phase AC input. The SPL is composed of both, open end winding 3 phase variable speed induction motor pump (1 Hp, 200 V) and other VIL loads (960 W, at 150 V) connected to three separate DC links of CMAR. The SPL transacts power through active rectifier in cascaded multilevel mode creating three DC links which in turn feeds three independent H-bridges to vector control the OEIM pump load. Each of the three smaller DC links hosts a common DC link capacitor between the rectifier and inverter bridges. The SPL is interfaced with single phase grid via interface inductor which helps in controlling the power transaction from the grid. To additionally create a scope of unbalance loading, on each of the 3 separate DC links, three independent VIL loads (R_1, R_2, R_3) are connected depicted by variable duty cycle passive loads. This will test the effectiveness of the control algorithm against

any unbalance situations. Load controllers are also connected to the DC links for protection and to avert any case of transient overvoltage arising due to switching on/off of dynamic load. The three DC links so created feeds vector controlled OEIM pump drive, where individual H-bridges act as power modulators. The overall power drawn by the SPL and another VIL depends on the prevailing grid frequency conditions. The different loads attached with the DC links are smartly altered to draw adequate power from the grid dictated by grid frequency. The alteration of power drawn is ranged by the value of interface inductor (6 mH, assuming 10% ripple component in the inductor current), which is connected to 240 VAC grid and SPL [118]. The rating of the capacitor on each DC link is decided on the basis of the allowable voltage ripple and power exchange.

6.4. Smart Pump Load Management Control

The power flow from the grid is governed by power angle between the point of common coupling (V_{PCC}) and terminal voltage (V_t), which in turn is controlled by modulation index for the operation of individual bridges of CMAR. Hence, the decrease in power flow shall be marked by an increase in modulation index, directing the control for reduction in the speed of SPL. Thus, the decision of selection of modulation indices should be duly governed in respect of grid capacity (freq≥50 Hz, power surplus or freq ≤50 Hz power deficient). During power surplus condition the modulation indices get

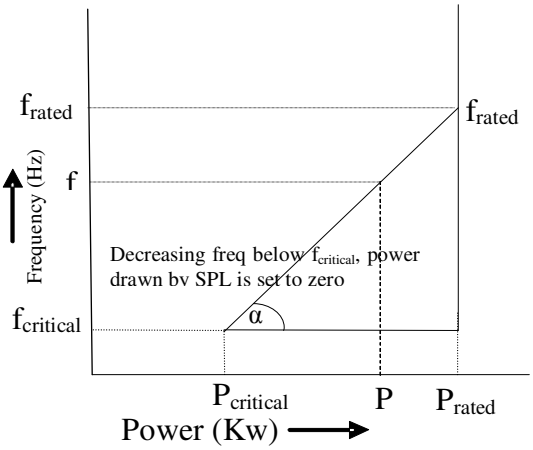


Fig. 6.3: Droop curve according to individual capacity of pump load.

decided as per predefined reference values of the speed of SPL unit. Whereas for deficient power condition SPL prompt for slower speed as commanded by the droop characteristics, directing the changes to control for alteration in the modulation indices. The cumulative autonomous efforts of multiple SPL on the rural feeder smartly reduce the power burden and contribute towards stability and frequency restoration on the grid. The droop characteristic of individual SPL is considered in conformance with an individual power capacity of the pump load. The slope for the droop rate bounded by critical limits of the frequencies can be expressed as (shown in Fig. 6.3):

$$\tan \alpha = \frac{f_{rated} - f_{critical}}{P_{rated} - P_{critical}} \quad (6.1)$$

where, f_{rated} and P_{rated} are rated frequency and rated power respectively, and $f_{critical}$ and $P_{critical}$ reflects the critical frequency of the reference grid (decided on the basis of installed capacity by the regulator) and the critical power (beyond which the SPL should be disconnected for the grid support) respectively.

Similarly, the expression for the relationship between power and frequency may be expressed as:

$$f - f_{rated} = \tan \alpha * (P - P_{rated}) \quad (6.2)$$

Substituting the value of tan α from (6.1) in (6.2), the power drawn from the grid at any frequency can thus be suitably estimated as:

$$P = P_{rated} + (f - f_{rated}) * \frac{P_{rated} - P_{critical}}{f_{rated} - f_{critical}} \quad (6.3)$$

Since the rural load approximately comprise 60-70 % pump load [119], if controlled smartly, reduce the power consumption and aid to the restoration of the grid frequency. The quantum of frequency restoration will depend on the capacity of grid and number of units of SPL connected to the grid. As per Central Electricity Regulatory Commission, India, the critical frequency ($f_{critical}$) is fixed to 49.5 Hz [120]. The power to be drawn by CMAR in consonance with (6.3) is required to be shared between VIL and SPL as:

$$P = P_{VIL} + P_{SPL} \quad (6.4)$$

For constant voltages maintained on the DC links the eq. (6.4) may be modified as:

$$P = V_{dc}^{\ 2} \sum_{j=1}^{3} \left(\frac{1}{R_j}\right) + K_m \omega_r^{\ 3} \quad (6.5)$$

Where, V_{dc} is common DC link voltage ($V_T = V_M = V_B = V_{dc}$), R_j(j=1,2,3) is the equivalent resistance (VIL) seen on individual DC links, K_m is motor constant and ω_r is motor speed. Thus from (6.5) it is clear that the power (P) estimated through the droop curve, is controlled mainly by decreasing /increasing the speed of the SPL to match the power estimated through the droop curve as in the day time (peak demand hour) when the lighting loads will be in OFF state. In the night time when the supply is surplus to feed both the VIL load and SPL, both shall operate at the fullest capacity. Only in critical cases, typically in the evening the VIL may also be altered by changing the illumination to match the power dictated by droop characteristics, while the pump is being operated at lowest critical speeds.

6.5. Control Theory of CMAR and DC Link Balancing Scheme

After making an estimate of the total power to be drawn by CMAR unit with the help of droop characteristics, the individual power to be drawn by each H- Bridge under balanced/unbalanced loading has to be directed through proper control algorithm. In the absence of incorporation of different θ_j and m_j for different H-bridges under uneven

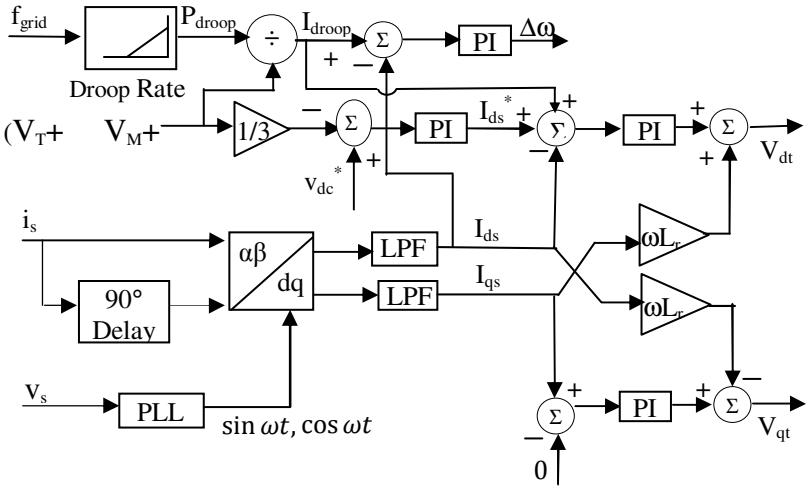


Fig. 6.4: Control blocks of proposed CMAR+SPL Configuration.

loading condition on different DC links, the H-bridges are forced to draw unequal power from the mains for the same source current. This may lead to different voltages at the different DC links. So, for balancing the DC link voltages, the modulation of individual H-bridges has to be changed to accommodate the load demand. For precise determination of θ_j and m_j components for each H-bridge, control operation based on SRF theory is developed. The control logic provides very accurate and noise free decoupled reference d-q component of terminal voltage for individual H-bridge. Fig. 6.4 and Fig. 6.5 depict the complete control logic for control of individual H-bridges with balanced/unbalanced loading on DC links. For the present control, SRF based control has been designed for referencing all the ac quantities into dc using park transformation and utilizing unit vector ($\cos\omega t$, $\sin\omega t$). The source current vector and its delayed (90°) component is used to obtain i_α and i_β represented as:

$$i_s = i_\alpha = A.\sin\omega t \tag{6.6}$$

$$i_\beta = A.\sin(\omega t - \frac{\pi}{2}) \tag{6.7}$$

Where, A is amplitude.

Further using park transformation the d-q components are computed as:

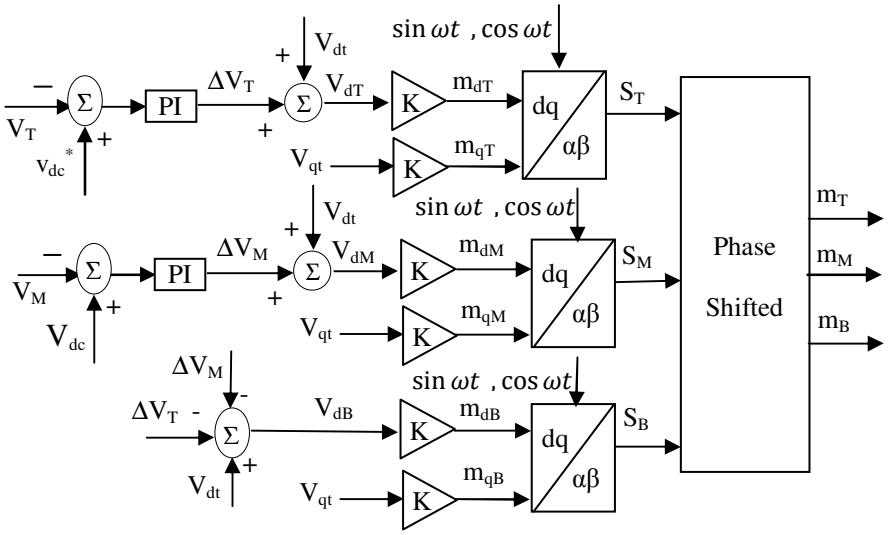


Fig. 6.5: Control blocks of proposed SPL+CMAR configuration for switching function generation for each H-bridge incorporating control block set for handling unbalanced loading.

$$\begin{pmatrix} i_{ds} \\ i_{qs} \end{pmatrix} = \begin{bmatrix} \sin\omega t & -\cos\omega t \\ \cos\omega t & \sin\omega t \end{bmatrix} . \begin{pmatrix} i_{\alpha} \\ i_{\beta} \end{pmatrix} \quad (6.8)$$

With SRF based control, the decoupled control of real and reactive power is easily implemented under the assumption of constant bus voltage at PCC. From (6.8) it is clear that i_{ds} represents the active power component and i_{qs} represents the reactive power component. From Fig. 6.4, it is clear that reference source current (i_{ds}^{*}) is derived by comparing the averaged DC link voltage of individual H-bridges with a reference voltage. But due to varying power demand by individual bridges the power demanded at each H-bridge may be expressed in d- q frame as:

$$P_j = \frac{i_{ds}}{2}(V_{dj} - jV_{qj}) \quad (6.9)$$

Where P_j (where *j* is *T, M, B*) is the power demanded and V_{dj} ,V_{qj} is the voltage in thed-q frame of the corresponding H-bridge.

So total power demanded by 3 H-bridges is expressed as:

$$P_{demanded} = P_T + P_M + P_B = \frac{i_{ds}}{2}[V_{dT} + V_{dM} + V_{dB} - j(V_{qT} + V_{qM} + V_{qB})] \quad (6.10)$$

And power supplied through the input terminal is given by

$$P_{supplied} = (V_{dt} - j\,V_{qt})\frac{i_{ds}}{2} \quad (6.11)$$

where $v_t = (V_{dt} - j\,V_{qt})$ terminal voltage as shown in Fig. 6.2.

For power balanced operation (neglecting the power losses occurring in the system) the equation may be expressed as:

$$P_{supplied} = P_{demanded} \quad (6.12)$$

$$(V_{dt} - j\,V_{qt})\frac{i_{ds}}{2} = \frac{i_{ds}}{2}[V_{dT} + V_{dM} + V_{dB} - j(V_{qT} + V_{qM} + V_{qB})] \quad (6.13)$$

Where V_{dt} and V_{qt} can be expressed as:

$$V_{dt} = V_{dT} + V_{dM} + V_{Db} \quad (6.14)$$

$$V_{qt} = V_{qT} + V_{qM} + V_{qB} \quad (6.15)$$

Moreover, terminal voltage can be expressed in terms of source voltage and drop across inductor in d-q reference frame as:

$$V_{dt} = - L_L\frac{di_{ds}}{dt} + L_L\omega i_{qs} + V_{ds} - i_{ds}\,(R_L + 3\,R_{switch}) \qquad (6.16)$$

$$V_{qt} = - L_L\frac{di_{qs}}{dt} - L_L\omega i_{ds} + V_{qs} - i_{qs}\,(R_L + 3\,R_{switch}) \qquad (6.17)$$

Neglecting the losses across the bridges and in the interface inductor ($R_L + 3\,R_{switch} = 0$); substituting $V_{qs} = 0$ (as v_s is synchronized with sin ωt obtained through PLL) and $i_{qs} = 0$ (for unity power factor) the (6.16)-(6.17) may be written as:

$$V_{dt} = - L_L\frac{di_{ds}}{dt} + V_{ds} \qquad (6.18)$$

$$V_{qt} = - L_L\omega i_{ds} \qquad (6.19)$$

Substituting value of (6.18) in (6.14) and rewriting (6.18) as:

$$L_L\frac{di_{ds}}{dt} = V_{dT} + V_{dM} + V_{dB} - V_{ds} \qquad (6.20)$$

Dividing both sides by V_{dc} to probe the relation for modulation indices (assuming $V_T = V_M = V_B = V_{dc}$) the (6.20) may be written as:

$$\frac{L_L}{V_{dc}}\frac{di_{ds}}{dt} = \frac{1}{V_{dc}}(V_{dT} + V_{dM} + V_{dB} - V_{ds}) = (m_{dT} + m_{dM} + m_{dB} - \frac{V_{ds}}{V_{dc}}) \qquad (6.21)$$

Similarly substituting (6.19) in (6.15) and dividing both sides by V_{dc}, the (6.19) may be

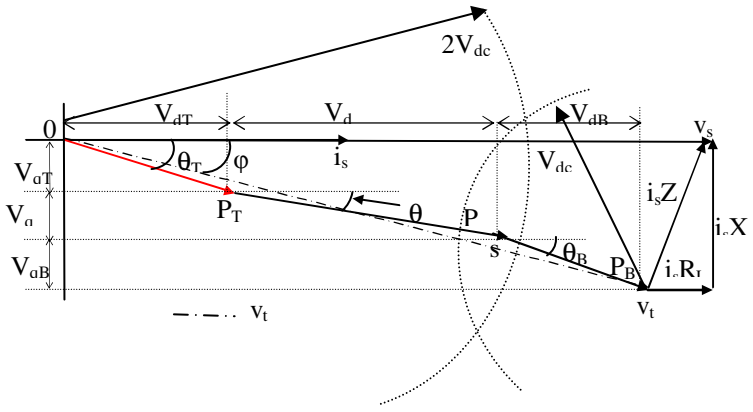


Fig. 6.6: Phasor representation of individual voltages in case of unbalanced loading.

written as:

$$\frac{\omega L_L i_{ds}}{V_{dc}} = m_{qT} + m_{qM} + m_{qB} \quad (6.22)$$

For a stable region of operation of CMAR the (6.21) and (6.22) have to be always satisfied irrespective of the loading conditions at the individual H-bridges.

For either balanced/unbalanced loading condition of individual H-bridges, the overall power drawn by CMAR is determined through magnitude and power angle (φ) of the overall terminal voltage phasor (V_t) as shown in Fig. 6.6. The distribution of terminal voltage of individual H-bridges under unbalanced loading will be distributed non – uniformly depending on power to be handled by each bridge. The distribution may only guarantee the equal DC link voltages of H-bridges with appropriate modulation index. For tackling such unbalanced situation, the individual DC link voltages are compared with the reference voltage and the error is passed through PI controller to add voltage (ΔV_j) to V_{dt} as shown in control diagram Fig. 6.5. Only two PI controllers are required to formulate the control for balancing the DC link voltage since third output may derive from the output of two PI's controllers with the overall change in voltage as zero (ΔV_B=-(ΔV_T+ΔV_M) as shown in control Fig. 6.5. As individual H-bridges are connected in series, the same current will be flowing from them. So to accommodate the unbalance power demand from each H-bridge, their terminal voltage phasor voltage (P_j- where is T, M, B) should be of varying magnitude and at different angle due to different modulation indices. So from control, it is evident that unbalance power requirement is fulfilled by changing the modulation indices m_{dj}(j –T, M, B), which leads to change in magnitude of d-axis voltage component (V_{dj}). Since the reference voltage along the q-axis is divided uniformly along the H-bridge for UPF operation, the individual H-bridge power factor angle (θ_j) depends on the magnitude of d-axis voltage component (V_{dj}) which in turn depends on loading condition i.e. higher the terminal voltage (V_{dj}) of the H-bridge will require higher modulation index leading to smaller power factor angle and, therefore, more real power will be drawn by the particular H-bridge as shown in Fig. 6.6. Such customized modulation index guarantees the operation of the H-bridges with equal DC

link voltages irrespective of the loading condition at each bridge amid load perturbation /disturbances on the grid.

Transforming these individually controlled variable ($m_{dj,}$ m_{qj}) from d-q to the α-β frame using reverse park transformation and computing individual switching function as S_j (where *j* is *T, M, B)* which is further being used as an input for phase shifted modulation (PSPWM) to generate individual H-bridge gating pulses.

6.6. Control Approach for Vector Control of Open End Winding Induction Motor

3 phase induction motor is modeled as OEIM by opening the common neutral point to get 2 terminals for each phase which eases each phase to be fed through individual H-bridges. OEIM is modeled in synchronously rotating reference frame.

Electromagnetic torque may be expressed as:

$$T_e = \frac{3P}{4} L_m (i_{mqs} i_{dr} - i_{mds} i_{mqr}) \quad (6.23)$$

where p is the number of poles

For pump load, the load torque is expressed as (neglecting viscous friction):

$$T_L = K_m \omega_r^2 + B\omega_r \quad (6.24)$$

where B is viscous friction coefficient

Neglecting viscous coefficient the load Power is expressed as cube root of speed as:

$$P_L = K_m \omega_r^3 \quad (6.25)$$

Where K_m is estimated for the rated condition of the motor which is estimates as K_m = 0.000222. Further, the load power may be expressed in terms of motor air gap power as:

$$P_a = \left(\frac{\omega_r}{\omega_r + \omega_{sl}}\right) P_L \quad (6.26)$$

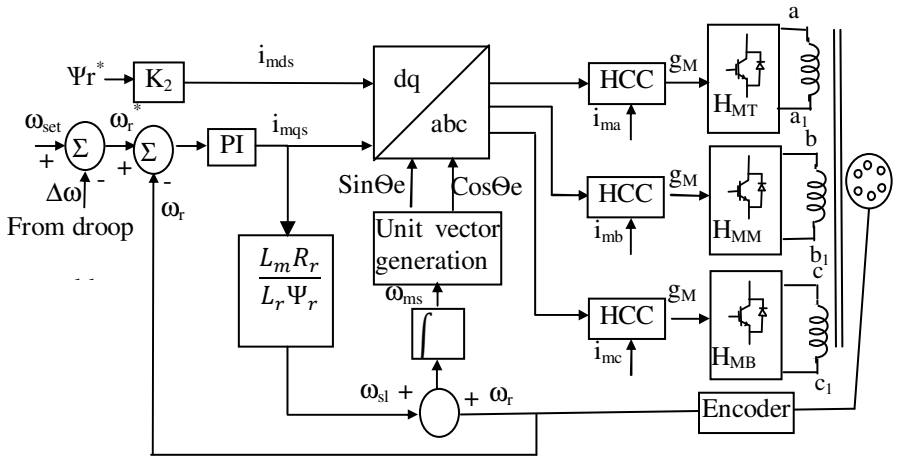


Fig. 6.7: Control blocks for Vector control of OEIM drive.

Where P_a is air gap power, ω_r is the motor speed, ω_{sl} is the slip speed. Neglecting the losses across the stator, the air gap power is equivalent to the electrical input power fed via H-bridges. Further neglecting the losses across the bridges the power fed by single phase AC source as through the CMAR is:

$$\frac{i_s}{2}(m_T + m_M + m_B)\, V_{dc} = \left(\frac{\omega_r}{\omega_r+\omega_{sl}}\right) K_m \omega_r^3 \qquad (6.27)$$

Where, i_s is source current and m_j (where j-T, M, B) is the modulation index of the individual H-bridges. The (6.27) may be further reduced as:

$$(m_T+m_M+m_B) i_s K_{mt} = (\omega_r^4) \qquad (6.28)$$

Where, $K_{mt} = \frac{V_{dc}}{2*K_m}\omega_{ms}$ and $\omega_{sl} + \omega_r$ is ω_{ms} (Synchronous frequency)

$$\sqrt[4]{(m_T + m_M + m_B) i_s K_{mt}} = \omega_r \qquad (6.29)$$

Actual motor speed as per (6.29) is governed by the reference motor speed (ω_r^*) which in turn is decided based on the set reference speed (ω_{set}) and $\Delta\omega$, the component obtained by PI controller operating on error between d –component of the source current (i_{ds}) and the reference current obtained through droop characteristics (i_{droop}) as per prevailing grid frequency as in Fig. 6.4. Thus, the reference ω_r^* is obtained by adding ω_{set} to $\Delta\omega$ to provide requisite grid support smartly to aid to the stability of the grid. With the change in reference speed command, the slip speed (ω_{sl}) is also altered, which is given as:

$$\omega_{sl}=(\frac{L_m R_r}{\Psi_r L_r})i_{mqs} \quad (6.30)$$

Where, Ψ_r is the rated flux along d-axis. Further, the synchronous speed is computed by adding the $\omega_{sl}$to ω_r to determine the power frequency of the motor, which in turn is used

TABLE 6.1
Parameters of Active Rectifier and Induction motor

Main supply voltage 1φ, Line Frequency	240V, 50 Hz
DC link voltages (V_T, V_M, V_B)	150V
DC link Capacitance	2200 μF
Interface Inductor	6mH
Passive load	966 Watt
Motor Rated Voltage , Frequency, Power	200V , 50 Hz, 1 Hp,
Motor Rated Speed	1428 RPM
Rotor Resistance (R_r), Stator Resistance (R_s)	2.26 Ω, 2.7 Ω
Motor Mutual Inductance (L_m)	138.4 mH

to determine the synchronizing component as shown in Fig. 6.7. The obtained torque and flux component (i_{mds}, i_{mqs}) are transformed through reverse park transformation using unit vectors to get the individual motor winding currents. These reference currents are compared with actual motor current and pass through hysteresis comparator to obtain switching command for the individual bridges.

Further for pump load any change in speed command would corroborate increase in load torque (due to its dependence on the square of speed and viscous friction), which eventually pushes the torque component (i_{mqs}) to reach saturation limit for fast acceleration. Such sudden acceleration tends to increase ω_{sl} which further increases the ($\omega_r + \omega_{sl} = \omega_{ms}$) synchronous speed initially, before settling it down to steady state frequency, when speed settles to steady state value.

6.7. MATLAB Based Simulation of Single Phase Cascaded Multilevel Interfaced 3 Phase Pump Drive

The SPL with passive load sharing the DC links having H-bridge cascaded multilevel active rectifier unit at the front is simulated under MATLAB Simulink environment using power system block set. To gauge the interactive action of the SPL under varying grid frequency, a programmed single phase source with programmable frequency is created. Using e-PLL, the frequency changes are accurately tracked for proper operation of SPL using SRF based control. The drive performance has been tested by changing the reference command for speed. The pump load on the drive is modeled using mathematical equations. For ripple free and noise less operation of vector control drive, intentionally a large size (2200 μF) having smaller voltage rating capacitor has been connected to the common DC links, shared by a pair of H-bridges. The SPL control is verified for working with a harsh condition imposed by the higher capacitance value of DC link capacitor which may lead to Power quality (PQ) issues in voltage and current on grid side. The detail parameters of the active rectifying unit and open end winding induction motor are shown in Table 6.1.

The operation of the proposed SPL unit is simulated in MATLAB Simulink and the results are shown in Fig. 6.8. Fig. 6.8. shows the waveforms for PCC voltage, which is shown maintained at 240 V (V_{PCC}), source current (i_s), terminal voltage (V_t), frequency (f) of the grid, DC link voltage (V_{DC}), power drawn by CMAR unit (P), motor speed (RPM) and motor phase current (i_{ma}). The waveforms depicts steady state operation between t= 1.4s to t= 1.7s, where it is clear that for constant grid frequency of 50 Hz the CMAR is delivering 1746 W (Fig. 6.8(f)) to VIL and pump load while maintaining DC link voltage of 150 V (Fig.6.8(e)). From Fig. 6.8 (g) it may be observed that motor speed remains fixed at 1428 rpm during the aforesaid time period. It may also be seen in Fig. 6.8 (b) that source current is in phase with PCC voltage conforming to UPF while maintaining a current of 7 A. At t= 1.7s when grid frequency is slowly reduced to 49.65 Hz as evident from Fig. 6.8 (d), the SPL react smartly to the drop in frequency by adequately decrease in reference motor speed in accordance with droop characteristics.

Accordingly, it may be observed from Fig. 6.8 (g), that motor speed decreases to 950 RPM, which in turn resulted into a decrease in active power demand of SPL to 1200 W as evident from both Fig. 6.8 (f). Meanwhile, a decrease in motor current from 3.5 A to 2.8 A (Fig. 6.8 (h)) and in the source current from 7 A to 4.9 A (Fig. 6.8 (b)) further confirm the SPL operation. Thus such incorporation of the proposed control, when implemented for many such SPL units together, would help in the demand side management.

6.8. Hardware Implementation of Single Phase Cascaded Multilevel Interfaced 3 Phase Pump Drive

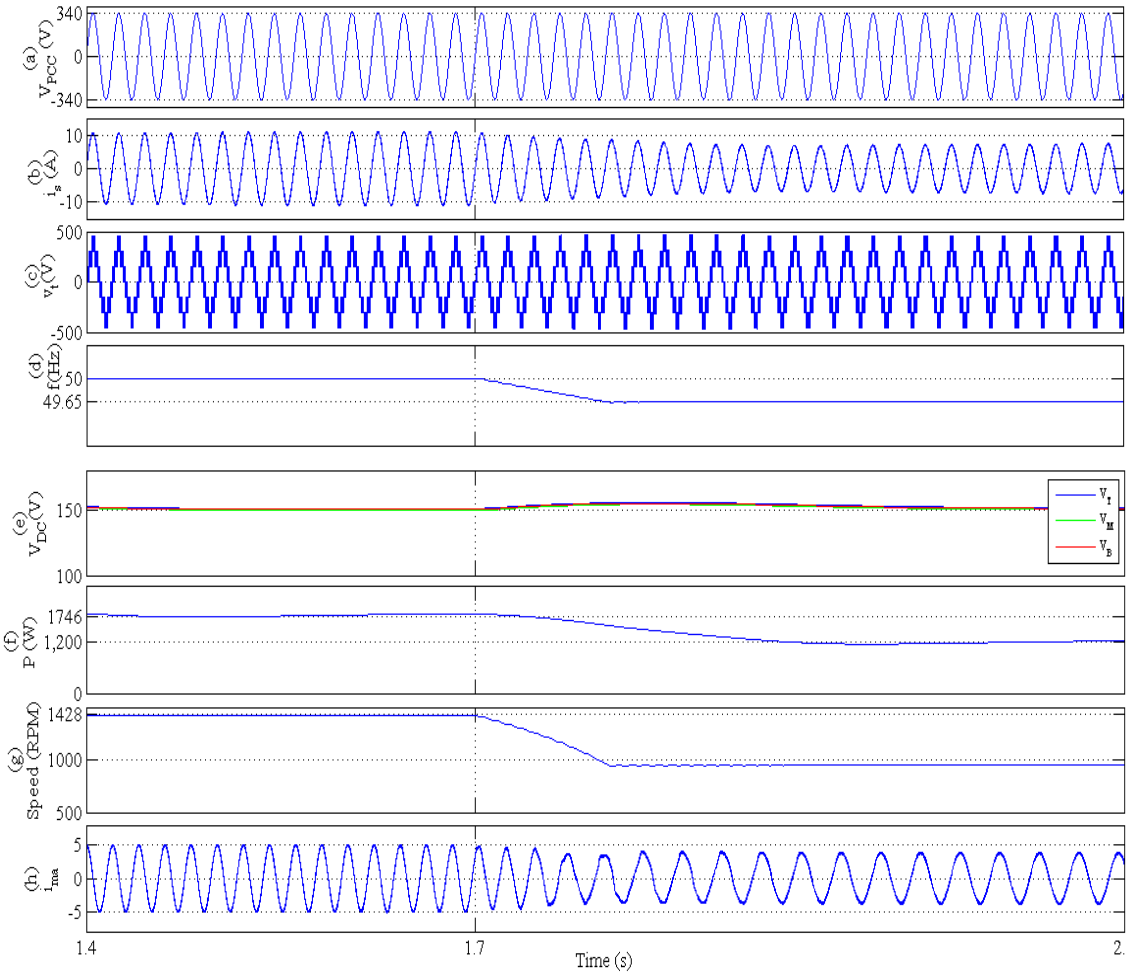


Fig. 6.8: Simulation waveforms of SPL unit depicting PCC voltage, Source current, Terminal voltage (V_t), Grid frequency (Hz), DC link voltage, Power drawn from grid by CMAR (P), motor Speed (RPM), Motor current (i_{ma}).

Same scale prototype using 1 HP OEIM in conjunction with 966 W VIL on different DC links is experimentally validated using requisite hardware and DSP controllers. The development of hardware includes fabrication of various control cards, interface card, voltage and current sensor cards etc. A 415 V LEM make LV25P and 25 A ABB make EL25P1 voltage and current sensor board respectively are designed and fabricated using PCB designer software in conjunction with the development of PCB's for microcontrollers and its interface. The Semikron make SKM50GB063D two modules are used to construct H-bridge, and connecting such three H-bridges in cascaded configuration forms 7 level of active rectifier, including 2200 μF, 250 V capacitors at each DC link of each H-bridges. The capacitor is shared by the back to back H-bridges, where one is connected with 3 phase open end winding induction motor having neutral point opened to enable each phase to be connected across each H-bridge and other forms the multilevel active rectifier unit. For the indirect vector control of OEIM, speed estimation is facilitated by connecting a hollow shaft incremental encoder mounted on the motor shaft. On the very same shaft to emulate the behavior of the pump load, a fan type of load is connected. Such complete SPL unit is controlled using dSPACE 1104 real time controller and dspic33FJ16GS502 DSP microcontroller together. The sensed parameters viz. current, voltage is feed through ADC units at a sampling frequency of 9 KHz on the dSPACE 1104 board and where the speed is sensed through the incremental encoder interface available on the dSPACE board. The vector control is incorporated through hysteresis current control, where switching pulses are given though digital I/O pins available on dSPACE board.

6.9. Result and Discussion

The same scale developed hardware prototype is tested under perturbing static (different value of R loads on each DC bus) and dynamic load (3 phase induction motor pump load) and results are recorded for different condition of both balanced and unbalanced loading condition at DC buses using Agilent DSO-X 2014A oscilloscope and Fluke 345 single

phase power analyzer for evaluation of the performance of proposed SPL. The complete experimental hardware system configuration is shown in Fig. 6.9.

6.9.1. Performance Evaluation of Single Phase Cascaded Multilevel Converter for Balanced DC Links and UPF Operation

At every perturbation and different point of operations of SPL, the current drawn (i_s) from grid always remains at unity power factor (UPF) as shown in the trace of the oscilloscope in Fig.6.10. The scaling factor for terminal voltage sensor is taken as 100:1. Moreover, for more clarity, the 7 level stepped terminal voltage (V_t) result shown in Fig. 6.11, depicts the source current (i_s) which is in phase with PCC voltage (V_{PCC}). Further to first check the effectiveness of the control algorithm for the proposed configuration enacting SPL even under unbalanced loading at DC buses, intentional unbalancing is created by connecting 60 Ω, 62 Ω, 68 Ω passive loads across each DC link, and their voltages are recorded before and commencement of balancing control algorithm and the same is shown in Fig. 6.12. It is clear from Fig. 6.12. that at t=2s, when balancing algorithm is started, each DC link voltage settles to 150 V, and accordingly, the

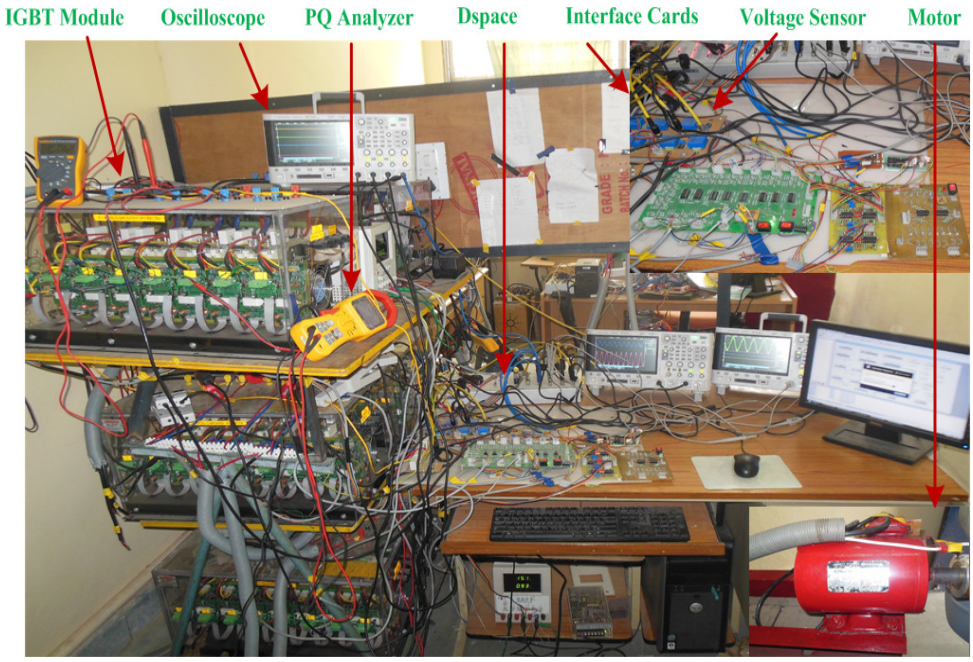


Fig. 6.9: Experimental setup of CMAR feeding SPL unit.

unbalanced static load currents get redistributed confirming to balanced voltages on DC link.

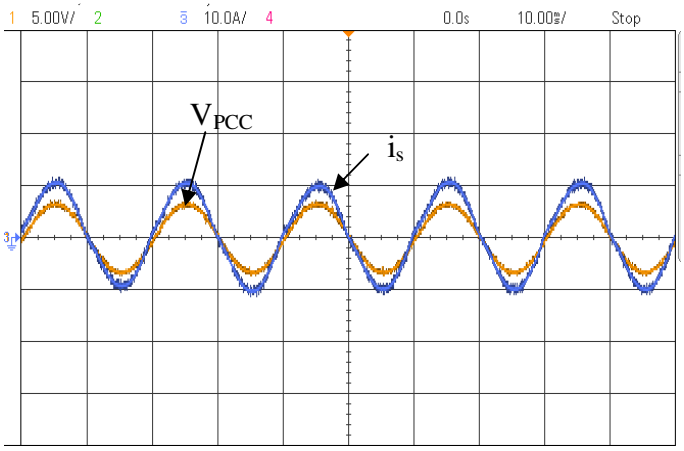


Fig. 6.10: Experimental result showing source voltage (500 V/div), and source current (10 A/div).

6.9.2. Performance Evaluation of Single Phase Cascaded Multilevel Converter under perturbing pump load using Vector Control

Simultaneously triggered three oscilloscopes are employed to record the dynamics in AC source side parameters, DC bus voltages, and the motor (Pump) current and speed output, respectively in Fig. 6.13 (a), Fig. 6.13(b) and Fig.6.13(c). To analyze the performance of SPL unit is initially started with the only static load as shown in Fig. 6.13. Till t= 0.4s, where SPL draws 4.1 A from source as shown in Fig. 6.13 (a) and the motor is not

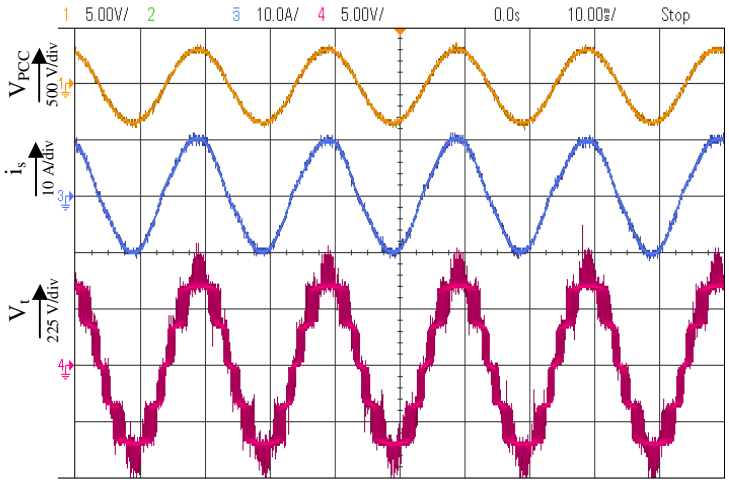


Fig. 6.11: Measured zoomed source voltage ($V_{pcc,}$), source current (i_s) and CMAR input voltage (V_t).

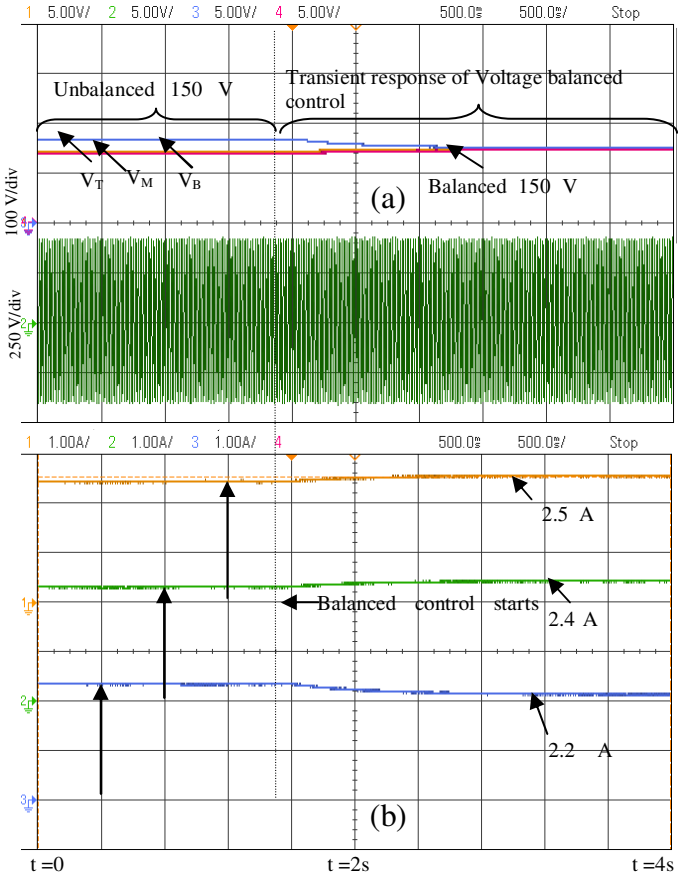


Fig. 6.12: Experimental results showing waveforms for DC link voltages, (V_T, V_M, V_B), terminal voltage and DC link load current- 1 A/div under balanced/unbalanced condition.

started as depicted in Fig. 6.13(c), where it maintains zero level till t=0.4s. When OEIM is started at t= 0.4s as shown in Fig. 6.13(c) with vector control it steadily reaches to the steady state value of 745 rpm. From Fig. 6.13(c), it is evident that motor current remains at the constant maximum allowable current limit to provide maximum acceleration till nearly t =1.5s. In the very same time duration, it may be observed from Fig.6.13(a), that source current rises from 4.1 A to 5.2 A, causing small voltage dip at DC link which recovers fast to retain back its reference voltages. A similar dip may also be seen in Fig. 6.13(a), where for short time dip is observed in the terminal voltage conform its connectivity to the weak grid. At t=4s another step change in speed is commanded and vector control swiftly changes the speed from 745 rpm to 930 rpm and the transitions are also shown in zoomed Fig. 6.14. It may be observed that frequency gets increased to a higher value as soon as speed command is stepped up a bit higher value before settling

down to the steady state frequency, once speed gets settles in conjunction with an increase in source current due to very nature of the load. The footprint of acceleration may also be observed in Fig. 6.13 (a) in source current waveforms. Since in vector control, the flux is not disturbed, but real component changes only unlike in starting case no dips in the voltage are observable. Similar dynamics have been given at t=10s.

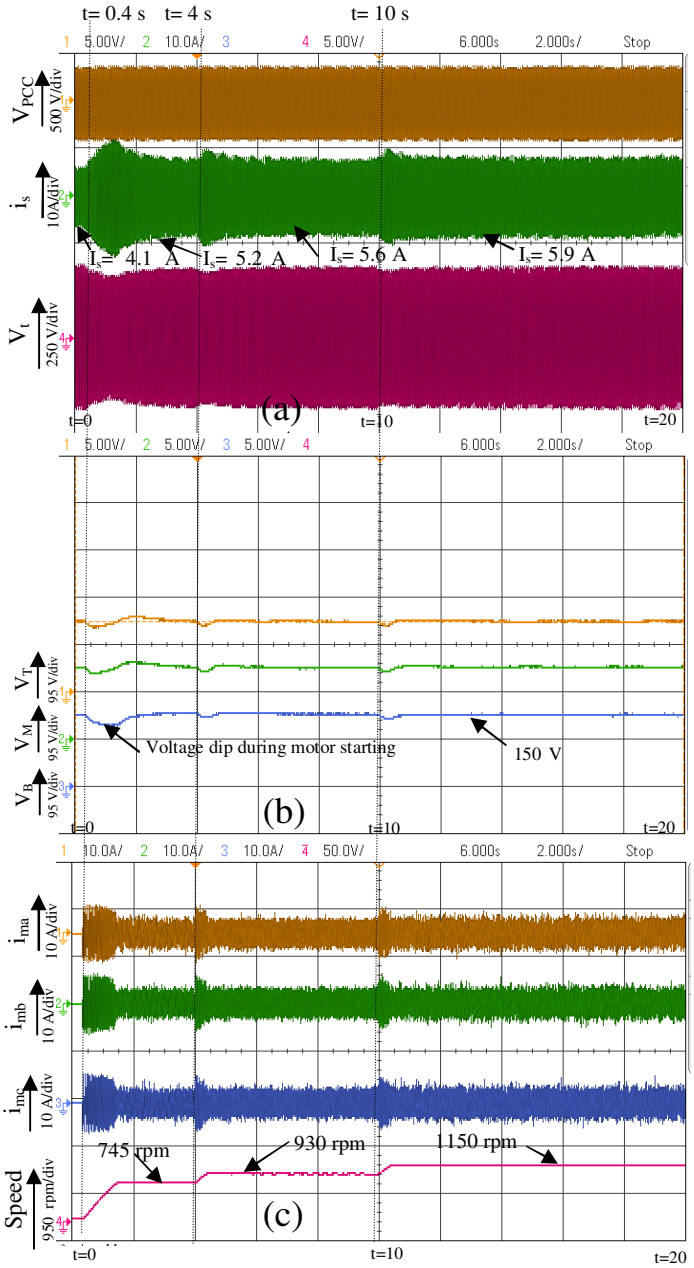


Fig. 6.13: Experimental results showing (a) source voltage (V_{pcc}), source current (i_s) and CMAR input voltage (V_t) (b) DC link voltages (V_T, V_M, V_B) (c) motor currents (i_a, i_b, i_c), motor speed.

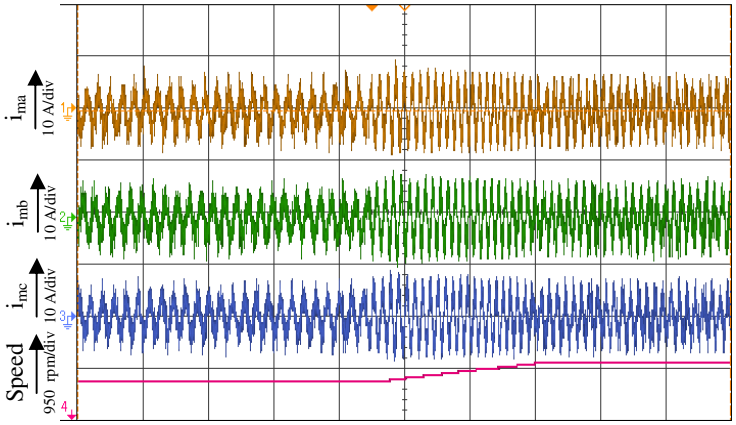


Fig. 6.14: Experimental results showing zoomed motor current i_{ma} , i_{mb} , i_{mc} and speed.

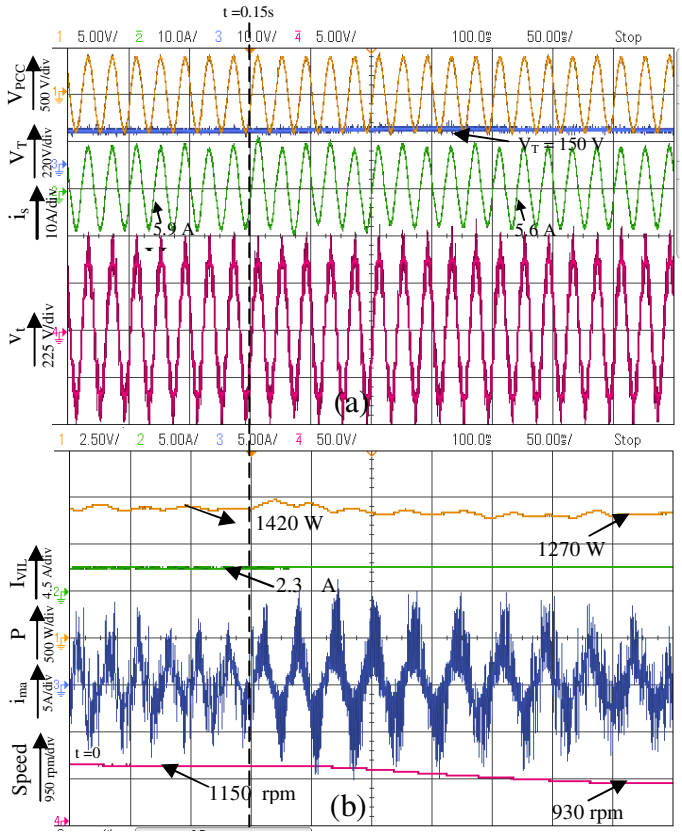


Fig. 6.15: Experimental result showing (a) source voltage (V_{pcc}), DC link voltage, source current (i_s) and CMAR terminal voltage (V_t) (b) Power drawn by CMAR (P), VIL current (I_{VIL}), motor current (i_{ma}) and speed.

6.9.3. Performance Evaluation of Single Phase Cascaded Multilevel Drive System Under Changing Grid Frequency Condition

Since the grid frequency can't be changed at the whims and fancies of the individual, to check the effectiveness of control algorithm, the initial operating grid frequency of 50 Hz, is assumed altered at t= 0.15s to 49.65 Hz by altering the P_{droop} reference in accordance with the droop characteristics. This changed P_{droop} accordingly commands the change in speed as per the designed control scheme to account for offsetting the burden. Accordingly, at t=0.15s, the controller prescribe a new reference command making the motor speed swiftly dropped to 930 rpm from 1150 rpm, in turn, reducing the frequency

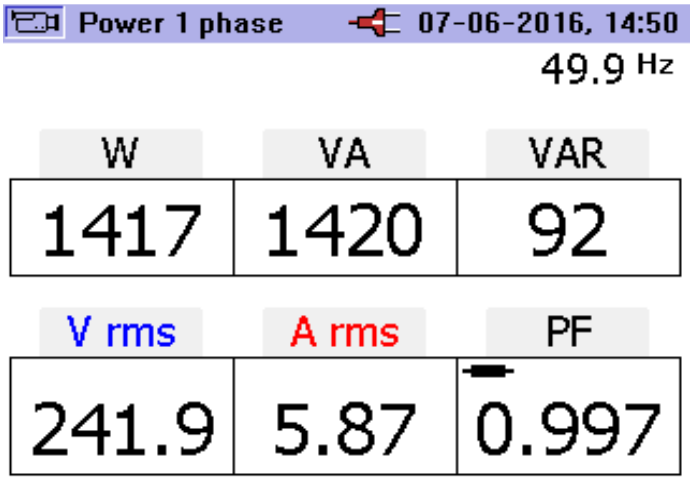
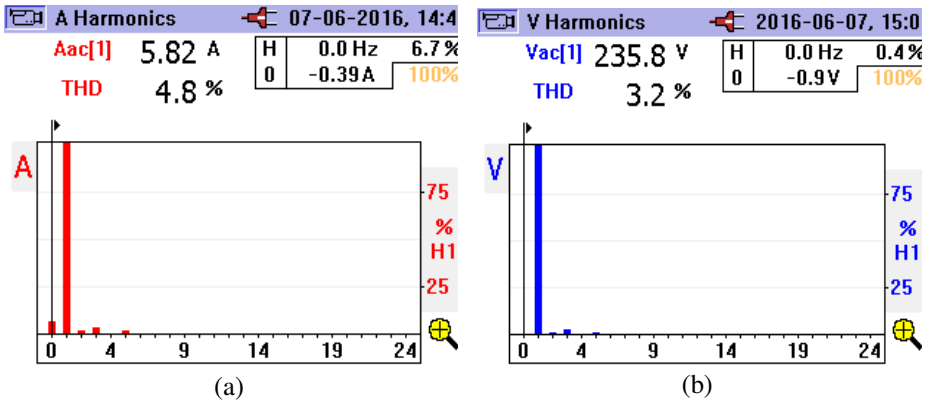


Fig. 6.16: Results of power quality analyzer using Fluke 345.



(a) (b)

Fig. 6.17: (a) Waveform for THD of source current (b) THD of CMAR terminal voltage V_t.

of the motor currents from 40 Hz to 28.8 Hz as clearly evident in the simultaneously triggered oscilloscope traces shown in Fig. 6.15(b). Such reduction in speed reflected in the reduction of the total power drawn from grid from 1420 W to 1270 W, maintaining VIL current same at 2.3 A shown in Fig. 6.15(b). Moreover, such reduction in speed resulted in a reduction of overall source current demanded by SPL unit from 5.9 A to 5.6 A (Fig 6. 15(a)). Meanwhile, the DC link voltage remains maintained at 150 V as shown in Fig. 6.15 (a). Such multiple units of SPL if used on rural distribution grid prompts to the reduction of the overall loads smartly with grid frequency and would, in turn, reduce the net demand on the grid, contributing to the stability of the grid.

Waveforms of Fluke 345 power analyzer is shown in Fig. 6.16 depicting power drawn by SPL prototype unit when the motor is running at 1240 rpm. It is further clearly illustrated that source current is maintained at UPF with current magnitude of 5.87 A. Fig. 6.17 (a) and Fig. 6.17 (b) shows the THD of source current and terminal voltage which is well within limits (4.8 % and 3.2 % respectively) conforming to the IEEE 519 standards.

6.10. Conclusion

The new concept of smart pump load using power electronics hardware for splitting single phase supply to three phase utilizing CMAR for vector control of 3 phase OEIM and other passive loads on its three different DC buses (balanced /unbalanced) is demonstrated through both by simulation and experimental results for grid interactive operation with improved power quality. The effectiveness of the droop control algorithm under low grid frequency conditions is clearly demonstrated through results by fast vector operation control operation of OEIM. CMAR always draw current from the grid at unity power factor ensuring improved power quality operation. Further, keeping the entire voltages on the DC buses constant and balanced ensures smooth operation of the smart pump drive immune to the disturbance both from AC or DC side. The control algorithm in d-q frame ensures immunity to any noise and harmonics in voltage at PCC. The proposed algorithm operates in conjunction with grid and enjoys the advantage of modularity, high efficiency for feeding smart pump loads and other passive loads

connected on DC buses. The proposed configuration has the advantage of small voltage rating capacitor, which guarantees the extended life and also provides ride through capability ensuring smooth operation of smart pump drive for cooperative operation with the grid. The smart pump load also helps in reduction of the dv/dt stress on the switches and also reduces the heat dissipation across the devices, besides strengthening the stability of the grid by providing adequate demand-side management. Such multiple units acting together smartly would strengthen the grid even under the influence of integrated low inertia sources.

Chapter VII

ADALINE CONTROLLED CASCADED MULTILEVEL RECTIFIER FEEDING 3 PHASE SUBMERSIBLE PUMP ON SINGLE PHASE RURAL FEEDER

7.1. General

Having established the strong foundation with control algorithm for CMC topology, other intelligent control algorithm is due for investigation. In this chapter CMC is probed with intelligent control for feeding pump drive system for its uninterruptable connected operation on rural grid particularly, the rural feeder suffers from under voltage condition particularly during peak hours besides other power quality issues. The contemporary 3 phase AC pump drives having AC-DC-AC conversion require proper estimation of voltage, frequency and power through fast and robust PLL. These conventional drives require heavy filter to avoid noise and harmonics to be propagated in the main line. In this chapter an Adaptive Linear Element (ADALINE) based multilevel power active rectifier control is probed for front end pump drive connected to single phase system for transient immune operation even during under voltage condition. The performance of the proposed configuration and control is investigated both through MATLAB simulation and experimentation on same scale hardware prototype.

7.2. Features of OEIM Pump Drive using Single Phase Cascaded Multilevel Converter

The ADALINE based control provides faster and transient immune operation and also do not require any filter for noise and harmonics filtration. In the proposed configuration a single phase supply is split into 3 different DC links using 7 level multilevel active rectifier (CMAR) being utilized to cater 3 phase open end induction motor drive. The configuration helps in reducing the problem of common mode voltage in conjunction

with less switching frequency operation using low value DC link capacitor size and lower rating of the devices. Since the switches/devices and the capacitor used are of smaller voltage rating the overall cost of the system will be economical and more compact. Moreover, the structure provides the bidirectional power transfer capability, thus can circumvent any swelling of DC link due to the sudden reduction of power drawn by the pump drive. The LMS based algorithm extracts the weights pertaining to the current corresponding to real and reactive power from noisy/distorted source current by minimizing the error with respect to a reference generated by unit template method.

7.3. System Configuration of Single Phase Cascaded Multilevel Converter

Fig. 7.1. shows the CMAR structure composed of 3 H-bridges connected in cascade to form 7 level active rectification unit having 3 different DC links. These DC links further may be utilized to feed open end winding induction motor (200V, 1 Hp) drive (OEIM) through a three different H-bridges across the other end of the DC links. The OEIM is controlled through indirect vector control using encoder based speed sensor and current

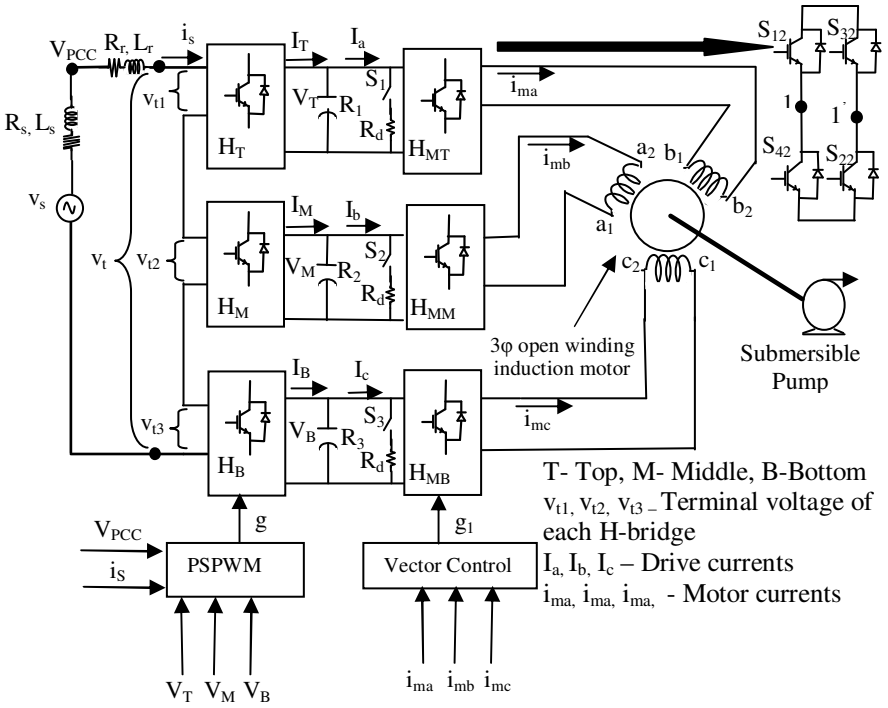


Fig. 7.1: Block diagram representation of CMAR feeding Pump drive.

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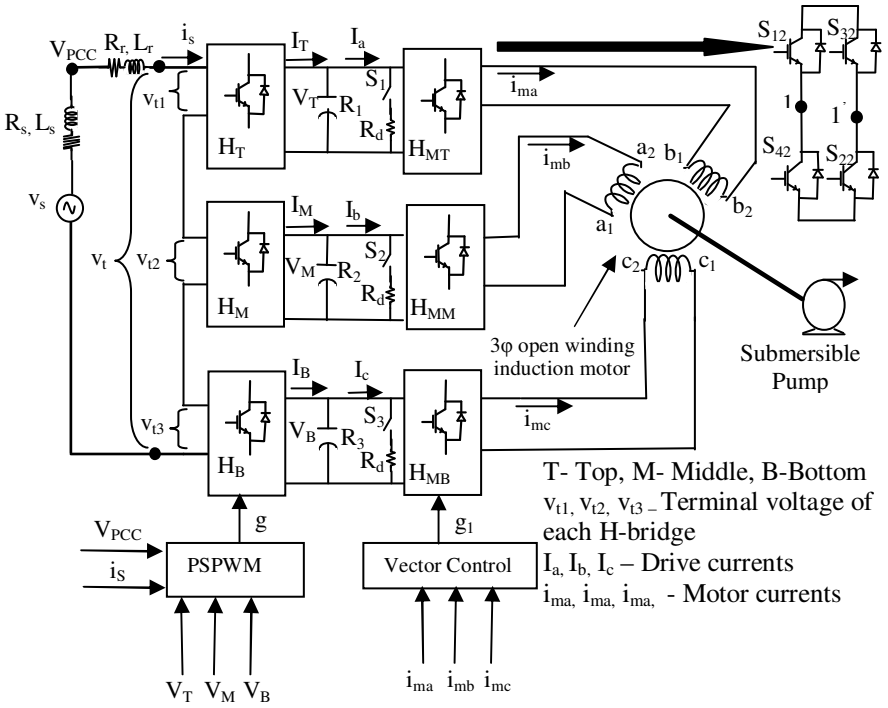


Fig. 7.1: Block diagram representation of CMAR feeding Pump drive.

sensors. For validation of results and control algorithm a weak grid represented by impedance (R_s and L_s) shown in Fig. 7.1 is considered where the PCC voltage is shown dipping. The CMAR pumping system is able to draw power from the weak grid through interface inductor. The control of the bridges is made in such a way that near unity power factor is maintained at PCC. The rectifier DC link capacitor is kept at appropriate value considering the allowable ripple voltage dynamic storage of charge, which would definitely be lower as compared to a single large capacitor. To have protection for the drive operation, a bleeder resistor is connected across individual DC links which are controlled by switches having reference value set at 180 V i.e. 1.2 times referenced DC link voltage.

7.4. Control Approach for ADALINE Controlled Single Phase Cascaded Multilevel Converter

The proposed control scheme of CMAR feeding the 3 phase OEIM is based on the accurate estimation of real and reactive components by proper decomposition of source current (i_s). The following section deals with the LMS based control scheme in detail for these components extraction. And in sub-section, based on reference current generated by LMS, the control scheme for generation of switching functions for the CMAR is taken up in detail.

7.4.1. ADALINE Based Control Scheme for Parameter Extraction

Basic logic for ADALINE is based on LMS algorithm for estimation of weights through proper training in feedback using reference unit template. For accurate estimation of weights in a signal proper reference unit is essential, since the weights depend on the phase and amplitude of the reference signal. For a single phase AC system the source voltage and current are given as:

$$v_s = V_m \sin \omega t \tag{7.1}$$

$$i_s = I_s \sin(\omega t + \varphi) \tag{7.2}$$

Further i_s may be decomposed into:

$$i_s = I_p \sin \omega t + I_q \cos \omega t \quad (7.3)$$

Where $I_P = I_s \cos \varphi$, $I_q = I_s \sin \varphi$, V_m is the amplitude of source voltage and I_s is the amplitude of source current.

Further I_P and I_q may be replaced with weight components w_p and w_q respectively and (7.3) may be written as:

$$i_s = W_p \sin \omega t + W_q \cos \omega t \quad (7.4)$$

For estimation of the unit template, the voltage at PCC is sensed. The sensed voltage signal is passed through orthogonal signal generator using Hilbert transform for estimating the amplitude of source voltage using (7.5)-(7.7)

$$v_s = v_\alpha = V_m \sin \omega t \quad (7.5)$$

$$v_\beta = V_m \sin(\omega t - 90°) \quad (7.6)$$

$$V_m = \sqrt{v_\alpha^2 + v_\beta^2} \quad (7.7)$$

Upon the division of the original and quadrature signal obtained as aforesaid by the

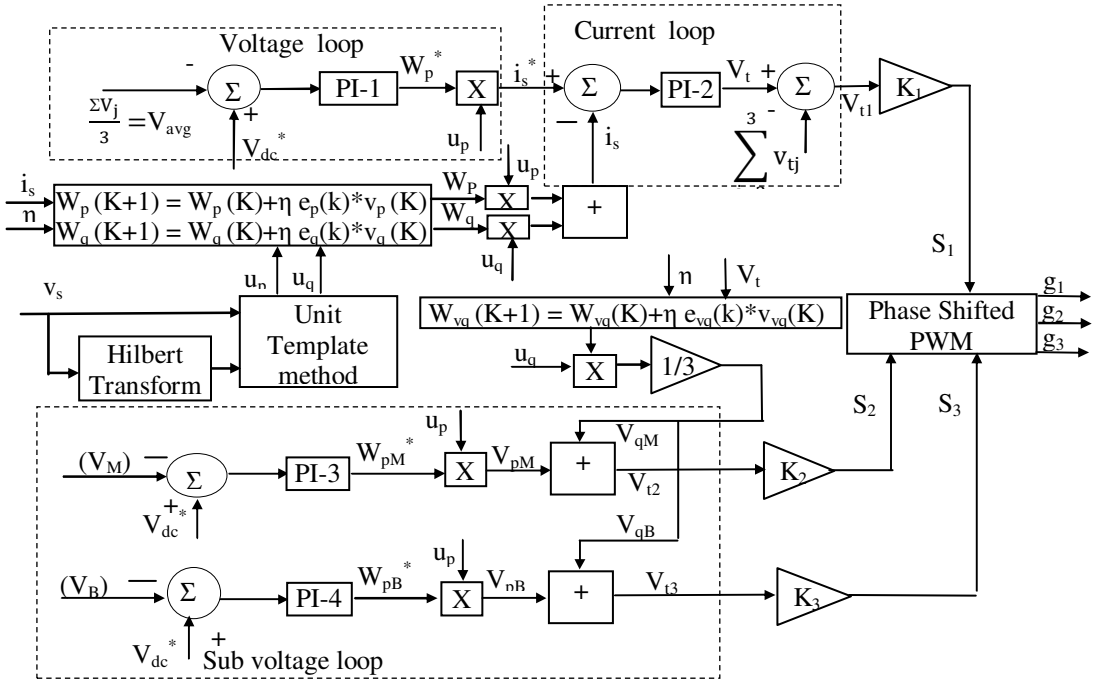


Fig. 7.2: Adaline based control scheme for CMAR.

amplitude (V_m) so obtained the unit template (having a maximum amplitude as a unit) may be obtained as represented in (7.8) below:

$$u_p = \frac{v_\alpha}{V_m}, u_q = \frac{v_\beta}{V_m} \tag{7.8}$$

Where u_p (t) and u_q(t) are respectively real and reactive unit template components. Utilizing these unit template for weight estimation it is utmost important that the referenced unit template should be perfectly sinusoidal. In case of distortion, the zero crossing of phase voltage is detected to generate a sinusoid template, synchronized with the source voltage. The signal is generated from a look-up table by adjustment of delay to track the change in phase and frequency of the mains by a digital processor. Utilizing this unit template, the filtered real and reactive components of source current may be expressed as:

$$i_p = W_p * u_p \tag{7.9}$$

$$i_q = W_q * u_q \tag{7.10}$$

where W_p and W_q are respectively the optimum weight components corresponding to real and reactive components of source current. The optimum value of weight components is obtained through LMS which processes the square of error to minimize the error between source current (i_s) and the referenced unit template as:

$$e_p(k) = i_s(k) - W_p(k) * v_p(k)\} \tag{7.11}$$

$$e_q(k) = i_s(k) - W_q(k) * v_p(k)\} \tag{7.12}$$

Based on LMS, these weights (W_p, W_q) are obtained by iteration given as:

$$W_p(K+1) = W_p(k) + \eta\, e_p(k) * v_p(K) \tag{7.13}$$

$$W_q(K+1) = W_q(k) + \eta\, e_q(k) * v_q(k) \tag{7.14}$$

Where η is the convergence factor whose value typically lie between $0.1 < \eta < 1$ and practically the value has to be decided based on compromising between how fast weights reach its stable state and the oscillations around the mean position. After offline training of the ADALINE, for the present control scheme, 0.2 is taken as convergence factor for optimum result.

7.4.2. CMAR DC Bus Voltage Control Scheme Based on ADALINE

Fig. 7.2 shows the block diagram of a comprehensive control scheme for CMAR handling OEIM load with uneven losses across the H-bridges and perturbing grid condition. The control scheme is implemented utilizing mainly three control loops, namely outer loop (Voltage loop), inner loop (Current loop) and sub voltage loop. The outer voltage loop is used to obtain the reference weight component (W_p^*) to ensure the constant DC link voltages across the H-bridges. Ensuring constant voltages across the DC links guarantees the delivery of demanded current by the OEIM pump load. W_p^* is

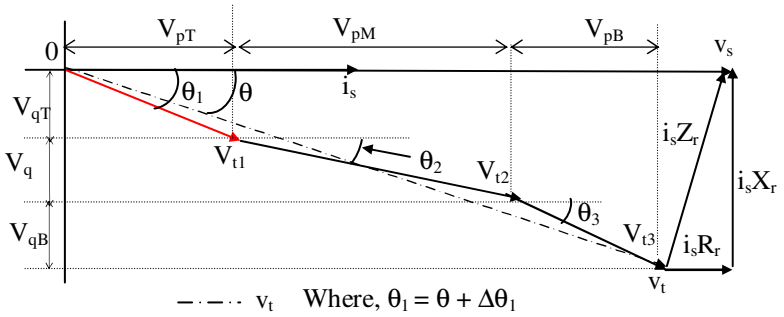


Fig. 7.3: Phasor representation of individual voltages in case of even/uneven losses.

obtained by processing the error between averaged DC link voltage (V_{avg}) and referenced voltage (V_{dc}^*) through PI controller, whose k^{th} sample may be expressed as:

$$W_p(k+1)=W_p(k)+K_{p1}\{V_{dc}(k+1)-V_{dc}(k)\}+K_{i1}V_{dc}(k) \qquad (7.15)$$

Where K_{p1} and K_{i1} are a proportional and integral constant of the PI-1 controller as shown in Fig. 7.2.

In the inner control loop, the reference source current (i_s^*) in phase with PCC voltage obtained by the outer loop is compared with actual source current (i_s) to arrive at a total terminal voltage (v_t) having both real and reactive voltage component as shown in Fig. 7.2. To distribute reactive voltage uniformly across the H-bridge to arrive at UPF operation, the terminal voltage (v_t) is passed through another ADALINE control loop having u_q and v_t as input. The obtained total reactive voltage component is multiplied by gain 1/3 to uniformly distribute the reactive voltage drop among 3 H-bridges.

7.4.3. Control Scheme for Handling Uneven Losses and Perturbing Grid Condition

The individual H-bridge losses might not be equal due to the difference in their characteristic, may lead to the uneven voltage across each DC links. So applying voltage balancing algorithm becomes utmost important for smooth balanced drive operation and also for improving the voltage THD at terminals of CMAR. For either even/uneven current demand at individual H-bridges, the overall power drawn by CMAR is determined through magnitude and power angle (φ) of the overall terminal voltage phasor (v_t) as shown in Fig. 7.3. The distribution of total terminal voltage among individual H-bridges depends on the power required to be transacted through each bridge taking into account the losses across each bridge. The appropriate terminal voltage of H-bridge may only guarantee the equal DC link voltages of H-bridges. For tackling such unbalanced situation, the individual DC link voltages are compared with the reference voltage (150 V) and the error is passed through PI-3 and PI-4 controller to arrive at W_{PM}^* and W_{PB}^* respectively. The reference weight components are multiplied by real reference template (u_p) and added with reactive voltage component to arrive at individual H-bridge terminal voltages (v_{t2},v_{t3}). A further sum of the obtained terminal voltage (v_{t2}, v_{t3}) of the middle and the top bridge is subtracted from the overall terminal voltage (v_t) to arrive at top bridge terminal voltage (v_t). These terminal voltages are passed through the gain block to arrive at switching function of individual H-bridge (S_1, S_2, S_3) as shown in Fig. 7.2.

These switching functions when applied on the phase shifted carrier, a phase shifted PWM (PS-PWM) for individual bridges are obtained to switch the power devices in each bridge.

Since the H-bridges are connected in series, the same current will be drawn by them, thus, to handle the uneven power requirement, the terminal voltage phasor of individual H-bridge voltage (v_{tj}) should be of varying magnitude. So from control, it is evident that unbalance power requirement is fulfilled by varying weight component (W_{pM}^*, W_{pM}^*) which leads to change in magnitude of terminal voltage component (v_{tj}). Since the reactive voltage reference is divided uniformly along the H-bridge for UPF operation, the

individual H-bridge power factor angle (θ_j) depends on the share of magnitude of real reference voltage component (V_{pM}, V_{pB}), which in turn depends on power need to be transacted i.e. higher the referenced real voltage of the H-bridge leads to smaller power factor angle (θ_j) and, therefore, more real power will be drawn by the particular H-bridge as shown in Fig. 7.3. Such customized terminal voltage guarantees the operation of the H-bridges with equal dc link voltages irrespective of the losses each bridge amid load perturbation /disturbances on the grid.

The individual power demanded by each bridge may be expressed by equations as:

Let

$$i_S = A.\sin \omega t \tag{7.15}$$

where, 'A' is amplitude.

$$P_{demanded}=I_S \sum_{j=1}^{3} V_{tj} \cos(\theta \pm \Delta\theta_j) \tag{7.16}$$

Where, I_s is the rms value of source current, θ is the angle between V_s and V_t in balanced state as shown in Fig. 7.3. V_{tj} (where j- 1, 2 and 3) represents the individual bridge terminal voltages.θ_j is the deviation of individual voltage phasor frombalanced state.

And the power supplied from grid is expressed as

$$P_{supplied} = I_S V_t \cos(\theta) \tag{7.17}$$

where V_t is the CMAR terminal voltage on AC side at the point just before the interface inductor.

Moreover, the terminal voltage may be expressed in terms of source voltage as

$$V_t = V_s - I_s (R_s + X_r) = V_s - I_s Z_r, \tag{7.18}$$

where Z_r is R_r+X_r

Substituting the equation (7.16) in (7.15) yields:

$$P_{supplied} = I_S V_t \cos(\theta) = I_S (V_s - I_s Z_r) \cos(\theta) \tag{7.19}$$

Since power supplied is equal to total power consumed, neglecting the losses

($P_{supplied}= P_{demanded}$), then

$$I_S(V_s - I_sZ_r)\cos(\theta) = I_S \sum_{j=1}^{3} V_{tj} \cos(\theta \pm \Delta\theta_j) \quad (7.20)$$

$$\cos(\theta \pm \Delta\theta_j) = \cos(\theta)\cos(\Delta\theta_j) \pm \sin\Delta\theta_j \sin\theta \quad (7.21)$$

Substituting equation (7.21) in (7.20) and dividing both sides by V_{dc} (where, $V_{dc} = V_T = V_M = V_B$), eq. reduced to

$$I_S(V_s - I_sZ_r) = \sum_{j=1}^{3} \frac{V_{tj}}{V_{dc}} (\cos\Delta\theta_j \pm \sin\Delta\theta_j \tan\theta) \quad (7.22)$$

Assuming $\Delta\theta_j$ is very small right hand side of eq. can be reduced to $\sum_{j=1}^{3} \frac{V_{tj}}{V_{dc}} (1 \pm \Delta\theta_j \tan\theta)$

For balanced condition$\Delta\theta_j = 0$ and the eq. (7.22) may be expressed as:

$$\frac{I_sZ_r}{V_{dc}} = \left(\frac{V_s}{V_{dc}} - \frac{1}{\sqrt{2}} \sum_{j=1}^{3} m_{tj}\right) \quad (7.23)$$

Where m_{tj} is the individual H-bridge modulation index and the eq. (7.23) need to always satisfy irrespective of the individual H-bridge modulation indices.

7.4.4. Working of Controller under Transient Condition

A step change in speed command, load change or dip/rise in PCC voltage give rise to transients operation and the same is illustrated in Fig. 7.4 (I) - (VI) through phasor. The gradual phasor movement explains the dynamic response of the CMAR system during transient operations. Fig. 7.4 (I) represents the phasor representation under steady state operation with balanced loading condition. Whenever the load demand increases on account of starting of the motor or change in speed command, a spurt in power is necessitated, which in turn draw from DC bus causing momentarily, reduction in both the DC link and the terminal voltage for the same modulation index. The sudden drawing of load current further displaces current phasor from UPF as depicted in Fig. 7.4 (II). And the current phasor continues to move further in lagging as depicted in Fig. 7.4 (III). This leads to drawing of reactive VAR before current phasor starts recovering to new steady state values in two stages as depicted in phasor in Fig. 7.4 (IV) and Fig. 7.4 (V). Another transient may be observed when there is a decrease in speed command resulting into

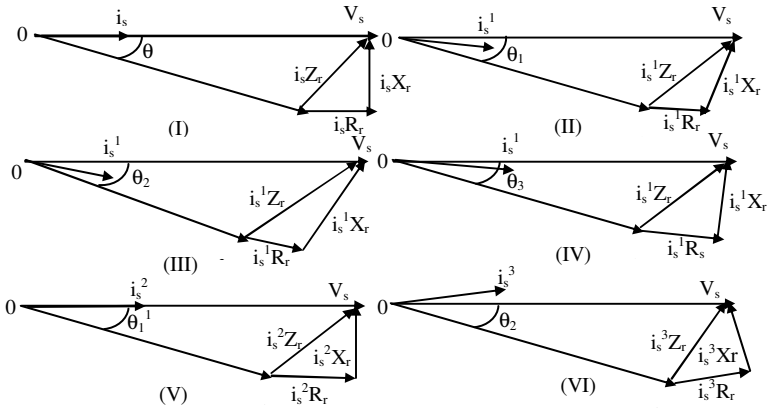


Fig. 7.4: Phasor representation during transient operation.

TABLE 7.1

Hardware and Simulation components of CMAR

Main supply voltage 1φ, Frequency	240V, 50 Hz
DC link voltages	150V
IGBT module	SKM50GB063D
IGBT driver	Skyper Pro 32
DC link Capacitance	2200 µF, 415 V
Controller	dSPACE1104, dsPIC33fJ16GS502
Voltage sensor	LV25P (0-415 V)
Current sensor	EL25P (0-25 A)
Current Probe	Agilent 1146A
Oscilloscope	Agilent DSOX 2014 A
Single Phase Power analyzer	Fluke 345
Multimeter	Fluke 115
Interface Inductor	6 mH
Passive load	960 Watt
Motor Rated Voltage, Frequency, Power	200V, 50 Hz, 1 Hp,
Motor Rated Speed	1428 RPM
Rotor Resistance (R_r), Stator Resistance (R_s)	2.26 Ω, 2.7 Ω
Motor Mutual Inductance (L_m)	138.4 mH
Incremental Encoder	ABZ Encoder

momentarily swelling of the DC bus and with same modulation index terminal voltage

phasor increase resulting into current phasor displacement from UPF towards leading side as shown in Fig. 7.4 (VI). Further, these transients also die out and new steady state reach in small time.

7.5. MATLAB Based Simulation of Single Phase Cascaded Multilevel Interfaced 3 Phase Pump Drive

The proposed CMAR model is simulated in MATLAB using Imposer system blockset with a connection to 3 phase OEIM (active load). The weak source is programmed in such a way that, a drop in voltage at some instant by a margin of 20 V, depicts a weak rural feeder. The PCC voltage is sensed and the unit template is computed for estimation

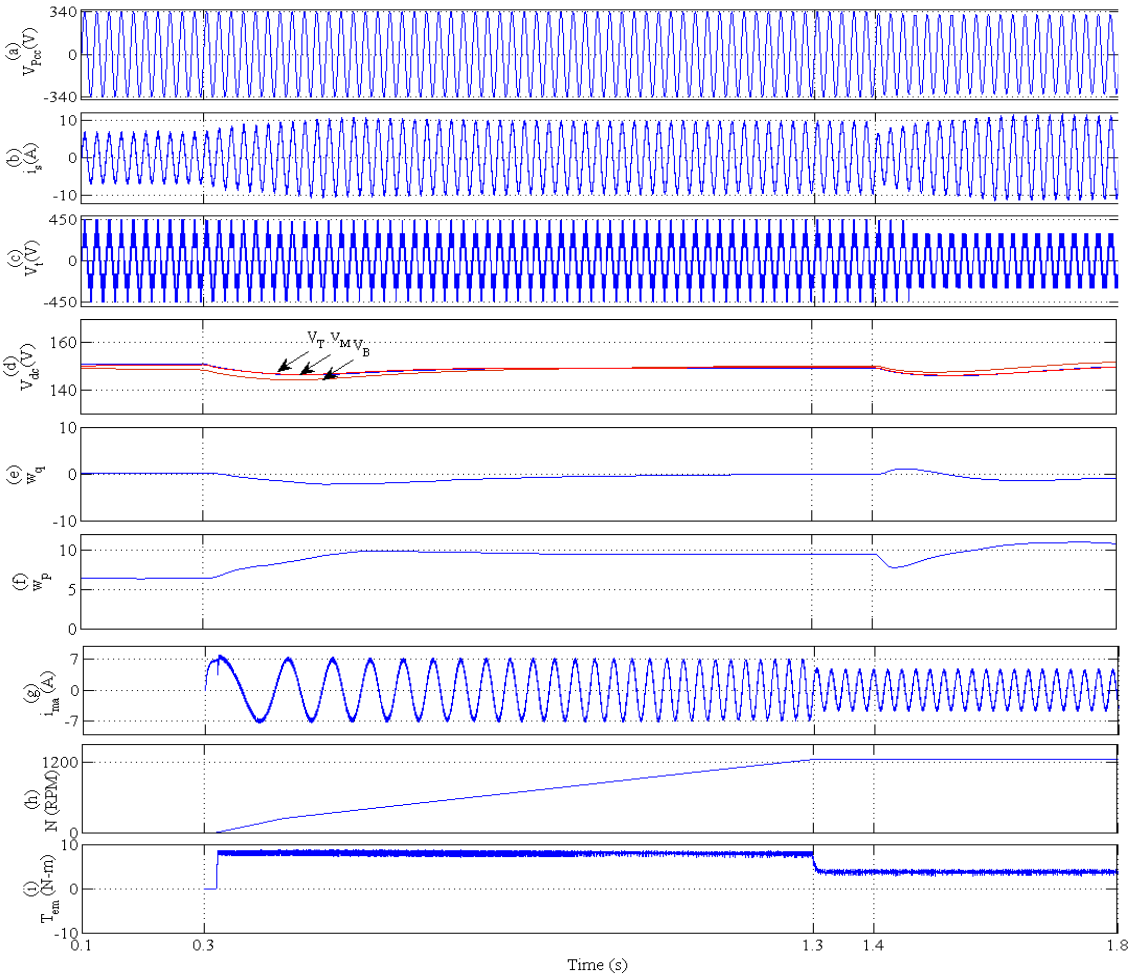


Fig. 7.5: Simulation waveforms of CMAR unit depicting PCC voltage (V_{PCC}), source current, terminal voltage (V_t), DC link voltages, weight components (W_p, W_q), speed (rpm), Motor current (i_{ma}), Electromagnetic torque (T_{em}).

of weights corresponding to real and reactive source current component. The detail parameters of CMAR with OEIM and other passive load are shown in Table 7.1.

The simulation results and various waveforms of the CMAR system from t=0.1s onwards neglecting initial transient condition are shown in Fig. 7.5. From Fig. 7.5(a) it is clear that the PCC voltage is maintained at 240 V till t=1.4s. Initially, till t=0.3s, the system is working under constant resistive bleeder loads with a resistance of 60 Ω at each DC link, a source current (i_s) of 4.2 A is demanded which is shown in Fig. 7.5(b). During the same time, 7 level terminal voltages is also shown in Fig. 7.5(c). Meanwhile, it is clear from Fig. 7.5(d) that dc link voltages are maintained at 150 V, with real and reactive current weight components at value 5.9 and 0 respectively as depicted in Fig.7.5(e)-(f). Zero weight for reactive components of current conforms to the unity power factor operation of the system. At t=0.3s, when the OEIM is started, it may be observed in Fig. 7.5 (g)-(i) that a small dip in DC link voltages occurs which is reflected, and the same in Fig. 6.5(d), recovers in presence of fast and adequate control for maintenance of DC link voltage. At the same time, it is evident from Fig. 7.5(e) that W_q also displaces from UPF as accelerating motor demand heavy current momentarily being supplied through DC links leading to dip in terminal voltage also for same modulation index. Soon the recovery starts in two stages; the current phasor also starts moving back towards UPF as explained before in control operation during transients as in Fig.7.5 (e). With OEIM starting under the vector control the frequency of motor current (i_{ma}) smoothly increases from low value to a steady state value of 1240 rpm as commanded by the reference speed the same may be viewed in Fig. 7.5(h). Further, the OEIM operation in addition to the earlier connected passive loads also resulted into increase in source current from 4.2 A to 5.8 A, for the same PCC voltage as shown Fig. 7.5 (b).

Continuing with same loading condition on DC links at t=1.4s a voltage droop on PCC voltage is created with a sudden decrease in voltage magnitude of 20 V, and the same is shown in Fig. 7.5 (a). With the droop in voltage at PCC, in order to cater the same amount of power demanded by OEIM at each DC link the modulation index of each H-bridge of CMAR is reduced by the control to draw more current from the source which steadily increases to 6.5 A in order to maintain the power balanced operation and the

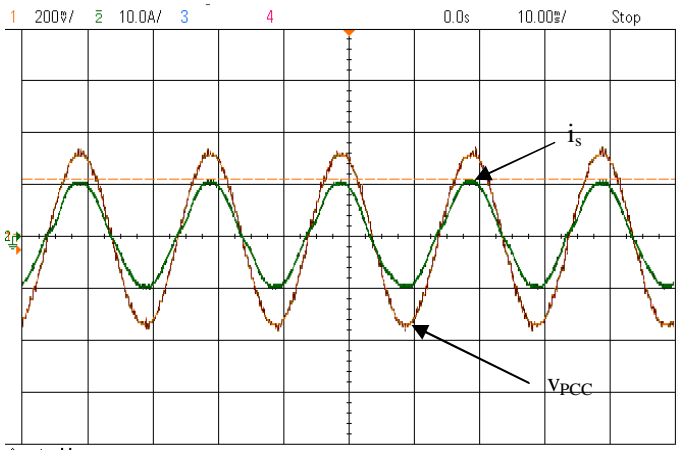


Fig. 7.6: Experimental result showing source voltage (200 V/div), and source current (10 A/div).

same may be observed in Fig. 7.5(b). The reduced modulation index also resulted into 5 level terminal voltage due to the reduction below critical value may be verified as in Fig. 7.5(c). The transient effect of droop in PCC voltage is also visible in weights computed by the algorithm for real component (W_p) and the reactive (W_q) weight components of the source current as shown in Fig. 7.5 (d)-(e). With small deviation from UPF operation controller again forces the W_q towards zero value, which is depicted in Fig. 7.5(e). Moreover, DC link voltages and motoring operation remain unaffected with such dip in PCC voltage due to fast dynamics of the proposed control.

7.6. Hardware Implementation of ADALINE Controlled Single Phase Cascaded Multilevel Interfaced Pump Load For 3 Phase Drive

The simulated control strategy for proposed CMAR using LMS is experimentally validated through the development of same scale prototype feeding a 1 Hp OEIM in addition to aggregate 960 watt static load distributed on three DC links of the proposed structure. The following table depicts the components and equipment utilized for the development of prototype and recording of the experimental results:

Apart from the components listed in Table 7.1 various interface PCB's cards and other sensors interfaces are also developed for realizing the control algorithm. The dSpace1104 controller facilitates various sensing function i.e. voltage and current through ADC interface and speed is sensed through incremental encoder interface, which in control

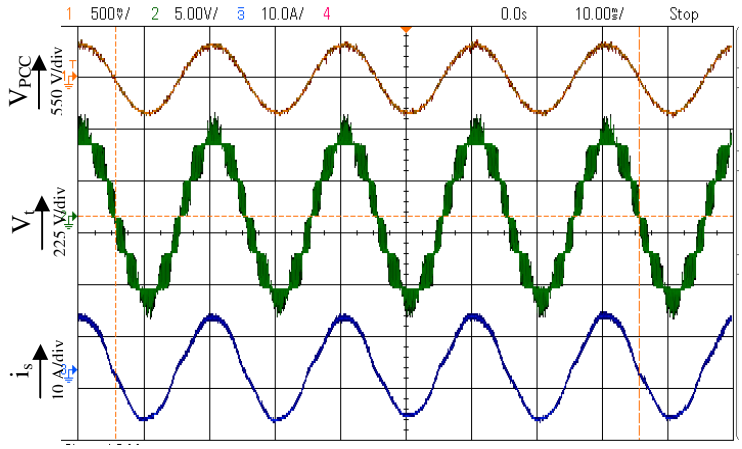


Fig. 7.7: Measured source voltage ($V_{pcc,}$), CMAR input voltage (V_t) and source current (i_s).

loop have a sampling frequency of 10 kHz. The H-bridge feeding the OEIM are controlled using hysteresis current control, by taking pulse output through Digital I/O port of dSpace 1104.

7.7. Result and Discussion

The simulation results and control algorithm are validated through various experimental results on the developed same scale prototype of the proposed CMAR feeding OEIM. The Table I depict the components and equipment utilized for the development of prototype and recording of the experimental results. The hardware prototype is tested for perturbing active (OEIM) loads in conjunction with a dip in the PCC voltage which is

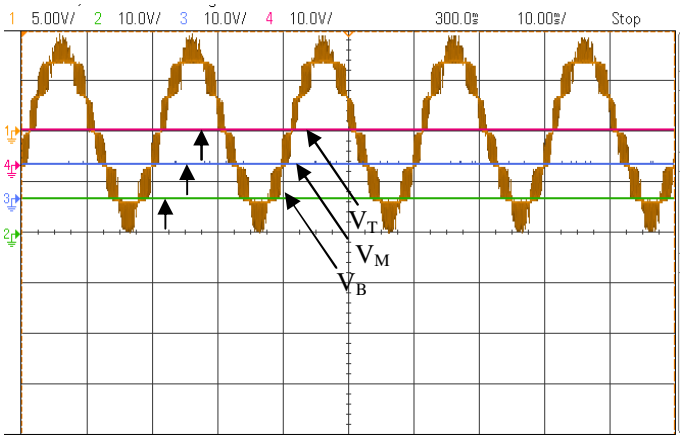


Fig. 7.8: Experimental results showing waveforms for DC link voltages, (V_T, V_M, V_B), terminal voltage.

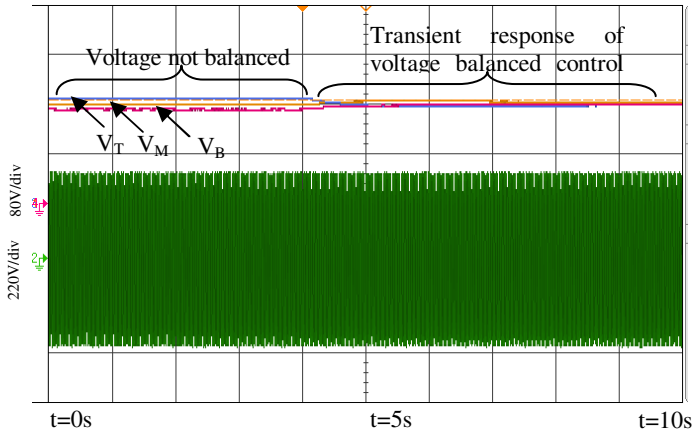


Fig. 7.9: Experimental result of DC link voltages DC link voltages (V_T, V_M, V_B) and terminal voltage (V_t) showing balanced control scheme.

common on the weak grid to demonstrate the robustness of the algorithm.

7.7.1. Performance Evaluation of Single Phase Cascaded Multilevel Converter for Balanced DC Links and UPF Operation

For all operating conditions of CMAR, the current is required to be maintained at unity power factor (UPF) as evident from oscilloscope trace shown in Fig. 7.6. Under steady state condition, the 7 level terminal voltage is also shown in Fig. 7.7 with respect to PCC voltage. Fig. 7.8 shows the DC link voltages of each H-bridge with respect to the terminal voltage of CMAR where each level of terminal voltage may be seen equal conforming to the maintenance of equal voltage at different DC links, also referenced through arrows. To validate the control algorithm in case of uneven losses across individual bridges, an intentionally unbalanced condition is created by connecting 65 Ω, 57 Ω, and 60 Ω respectively on individual H-bridges. Fig. 7.9. Show the oscilloscope traces conforming to the effectiveness of the control algorithm for balancing the voltages on the DC links before and after the invoking of balancing control algorithm with respect to 7 level terminal voltage.

7.7.2. Performance Evaluation of Single Phase Cascaded Multilevel Converter under perturbing pump load using Vector Control

To gauge the effectiveness of control under perturbing active load, the CMAR is started first with only passive loads on each DC link at t= 0s demanding an aggregate power of 960 watt by drawing 4.2 A from single phase mains, while DC link voltages are maintained at 150 V. The steady state operation is depicted in Fig. 7.10(a) and Fig. 7.10(b). The weights (W_p ,W_q) corresponding to the active and reactive power demand raised by the pump load as shown in Fig. 7.10(a) to give greater insight of the control algorithm. The sudden dip in voltages at DC links due to step change in load (Starting of OEIM drive) is seen as reduction in terminal voltage which in turn displaces the operation from UPF and CMAR starts to draw reactive power from the mains. It may be seen that the voltage recovery directed by the proposed control algorithm reacts exactly

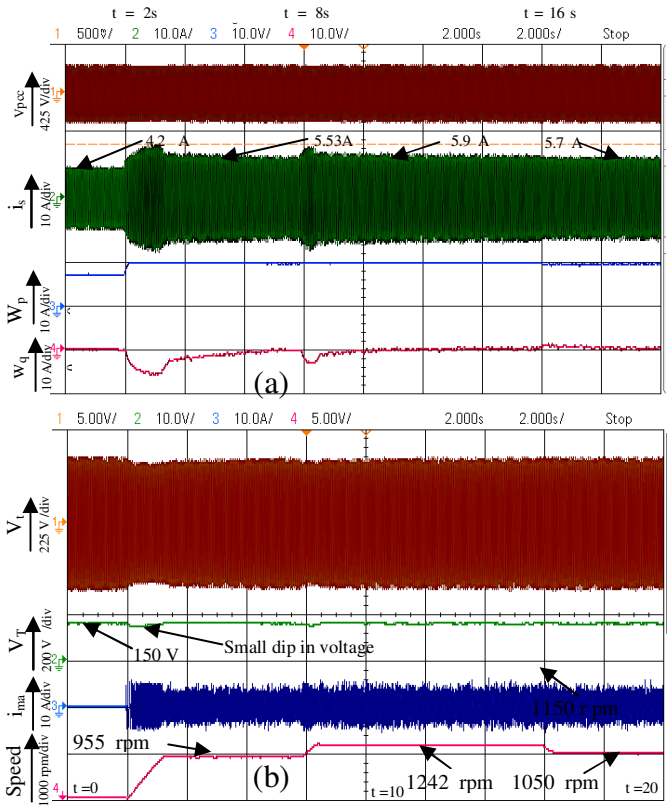


Fig. 7.10: (a) Experimental result showing waveforms of PCC voltage (V_{PCC}) source current (i_s), Weights corresponding to real and reactive component (W_{ds}, W_{qs}) (b) Terminal voltage (V_t), One dc link voltage (V_T), motor current (i_{ma}), Motor speed (rpm).

the simulation way as dealt in the previous section. At t=2s, when the command for vector controlled OEIM drive operation is given with referenced speed at 955 rpm, very soon the speed is reached to referenced value without any overshoot as shown in Fig. 7.10(b). At the same time, it may be evident from Wq in Fig. 7.10(a) that the acceleration

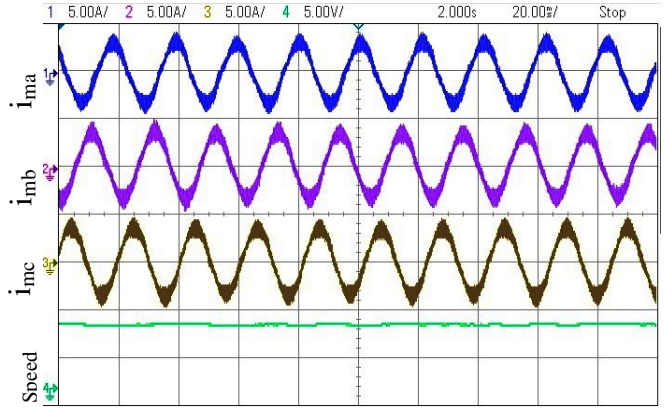


Fig. 7.11: Experimental results showing zoomed motor current i_{ma}, i_{mb}, i_{mc} and speed (1000 rpm/div).

of motor has displaced the operation from UPF and it is forced to draw reactive power from the main, in turn causing a drop in terminal voltage (shown in Fig. 7.10(b). The two stage recovery is carried out by first displacing the source current phasor back to near UPF condition sharply and then slowly and thus altering the power flow angle to suit new steady state conditions, with voltage at DC link restored back to 150 V. The controlled algorithm eventually forces W_q to 0 tracing UPF operation as evident from Fig. 7.10(a). The increase W_p is also evident from the increase in source current to 5.53 A for meeting increased loading conditions after a small transient operation to maintain the same dc link voltages.

At t=8s another perturbation is done by changing the referenced speed command from 955 rpm to 1242 rpm as shown in Fig. 7.10(b). The changed speed also resulted into increase in power demand that further resulted into increase in source current from 5.53 A to 5.9 A, and the same is shown in Fig.7.10 (a). During the same time period W_q is displaced from 0, and after small time recovers back to zero. To further probe the robustness of scheme another perturbation is given at t=16s by changing speed reference from 1242 rpm to 1050 rpm. A similar set of various waveforms are analyzed and it may be observed that W_q in Fig. 7.10(a) hence makes a transition to a higher from zero

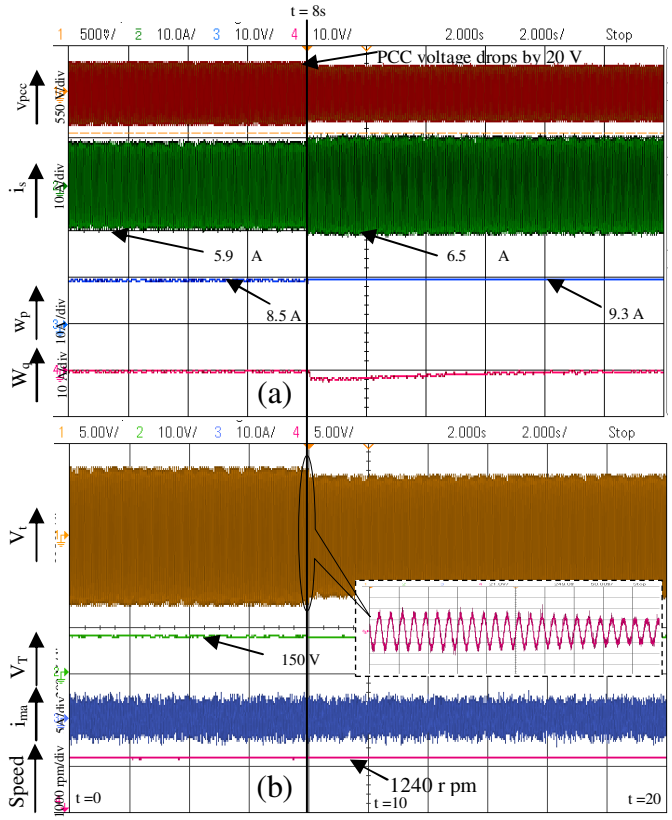
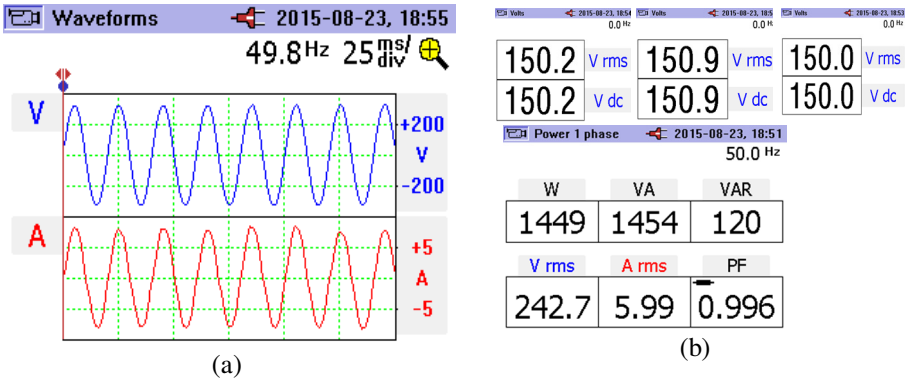


Fig. 7.12: Experimental result showing waveforms of PCC voltage (V_{PCC}) source current (i_s), Weights corresponding to real and reactive component (W_{ds}, W_{qs}), Terminal voltage (V_t), One dc link voltage (V_T), motor current (i_{ma}), Motor speed (rpm).

depicting excess power, thus displacing the current towards leading condition for matching the real power and slow settling the reactive power through alteration of modulation index to force it back to steady state condition. To show the speed transition with respect to motor current and frequency a zoomed waveform is shown in Fig. 7.11.

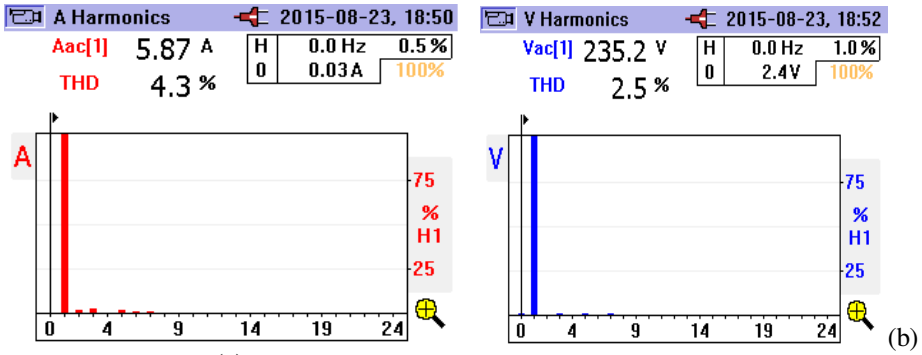
7.7.3. Performance Evaluation of Single Phase Cascaded Multilevel Drive System Under Changing Grid Voltage

To probe the effectiveness of the control algorithm in case of voltage changes on PCC prevalent at weak grids, PCC voltage is intentionally dropped by 20 V at t=8s to depict the under voltage and the same is shown in Fig. 7.12(a)-(b). Before the droop in PCC voltage is created, the CMAR is shown operating with both active and passive load running in steady state. From Fig. 7.12(a) it is evident that drop in voltage at PCC has



(a) (b)

Fig. 7.13: (a) Waveform showing source voltage and source current (b) Waveform showing DC link voltages and power demanded.



(a) (b)

Fig. 7.14: (a) Waveform for THD of source current (b) Waveform for THD of CMAR terminal voltage V_t.

resulted into increase in source current i.e. from 5.9 A to 6.5 A, to cater the same capacity loads at reduced PCC voltage. It is pertinent to observe that W_p which marks the increase of current pertaining to real power is slightly increased, whereas W_q is displaced from zero to accommodate such increase of current pertaining to real power, thus causing drawing reactive power the mains, which ultimately recovers back to UPF operation. The control works efficiently as it is clearly evident from DC link voltage, which is maintained at 150 V and also ascertaining the motoring operation remaining immune to PCC disturbance as shown in Fig. 7.12 (b). Further to provide room for more current at constant DC link voltages, the terminal voltage gets reduced to 5 level voltage waveform as shown in Fig. 7.12 (b).

Fig. 7.13 (a) shows the waveform of fluke 345 power analyzer showing voltage and current in phase, confirming to UPF operation. Fig. 7.13 (b) shows the Fluke 345 waveform for balanced DC link voltages and power demanded at 1240 rpm of motor

speed. Fig. 7.14 (a) and Fig. 7.14 (b) shows the THD of source current and terminal voltage i.e. 4.3 % and 2.5 % respectively confirming to IEEE 519 standard.

7.8. Conclusion

The proposed ADALINE based control of 7 level cascaded H-bridge rectifiers used for splitting a phase into three phase to feed OEIM pump drive on the rural feeder is demonstrated through both by simulation and experimental results. The effectiveness of the transient immune control algorithm under low voltage condition on the rural grid for the uninterruptable operation of vector controlled OEIM drawing source current always at unity power factor is clearly demonstrated. CMAR always maintains the DC bus voltages constant and balanced ensuring smooth operation of the pump drive immune to any disturbance both on AC side on the grid or split DC side. The PLL less operation of control provides faster dynamics and less computation time. The proposed system provides the advantage of smaller size dc capacitor, ensuring the extended life, helps in reduction of the dv/dt stress on the switches, reduces the heat dissipation across the devices. Using such units of CMAR on the rural grid would facilitate the uninterruptible operation of the pump drive.

Chapter VIII

SINGLE PHASE ON-BOARD SMART SPLIT VOLTAGE MULTI-MODE INTEGRATED BIDIRECTIONAL CONVERTER FOR EV/PHEV

8.1. General

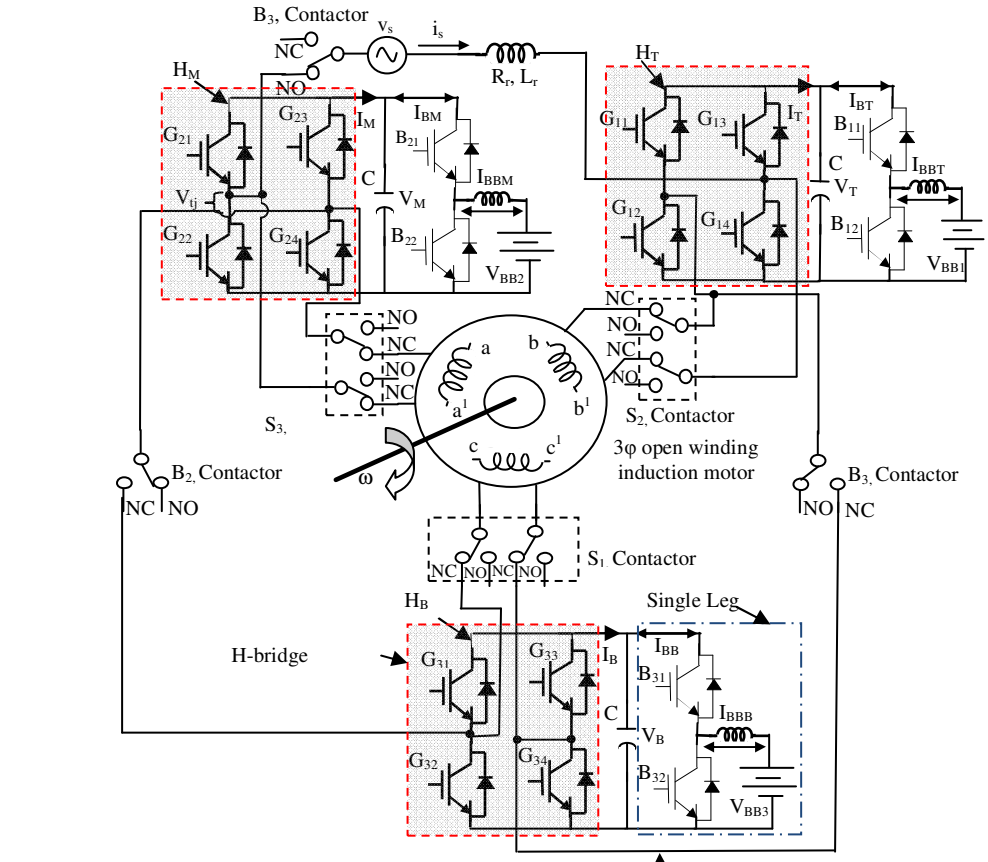
Having established control topology of CMC for grid tie application, the PV-CMC is tested is further need to be investigated for constant power application for In this chapter a single phase active multi-mode bidirectional grid interactive Cascaded H-bridge Multilevel Converter System (CMCS) and control algorithm for EV/PHEV with smart charging (Grid to Vehicle also called G2V) / Discharging (Vehicle to Grid also known asV2G) is presented. The battery stack may be utilized for drive operation using three phaseopen end winding induction motor (OEIM). The proposed converter topology using modified droop control scheme and closely knitting control algorithm is capable of smartly charging (G2V) / discharging (V2G) the split battery stacks with customized rates depending on the SoC's of battery stacks and on feeder loading conditions at the time when there is no drive operation. The multimode operation of the proposed scheme is effectively tested both through simulation and experimentation on the developed hardware prototype.

8.2. Features of Battery Charging/Discharging Topology Using Bidirectional Single Phase Cascaded Multilevel Converter

The bidirectional capability of the CMCS with an active voltage balancing at the DC buses for customized charging/discharging of the battery, smart grid-interactive V2G operation, G2V and integrated drive operation with the same structure provides uniqueness to the proposed configuration and control. During the G2V/V2G operation

amplitude of the current flowing to/from batteries is decided smartly by monitoring the grid voltage condition relieving the LV feeder from undue stresses. The control also dictates the operation with balanced DC bus voltages even under varying rates of the charging of the batteries. For drive mode, the proposed CMCS is configured via contactor to excite the 3 phase open end winding of induction motor load through each individual H-bridge for each winding controlled via field oriented indirect vector control.

The modularity of its structure offers multiple DC links to enable efficient charging of smaller battery units in the stacks, which also facilitates the reduction in the dv/dt transition for enhancing the life of the batteries, besides reduction in voltage rating of DC



I_{BX}- Equivalent battery current at DC links, where X is T, M, B
T- Top bridge, M- Middle bridge, B- Bottom bridge
I_X – DC link currents
i_s- Source current, V_s- Source voltage
V_{ij} – terminal voltage of individual bridge, j-1,2,3.
S_i– Normally closed (NC) during motoring operation.
B_i – Normally open (NO) during normal G2V/V2G.
where i is 1, 2, 3

Fig. 8.1: Block diagram representation for Multi mode operation using CMCS.

bus capacitors, and offer low THD confirming to IEEE 519 and reduced EMI due to lower switching frequency operation on AC side. Additionally, the facility of the splitting of battery stack provided by the structure circumvents the necessity of charge equalizing circuit for enhancing the efficiency, which otherwise would decrease tremendously. A comparison has also been drawn to illustrate this effect in the absence of costly and complex charge equalizing circuit additionally required otherwise. Since the switches/devices and the capacitor used are of smaller rating the overall cost of the proposed seven level CMCS offers economical and more compact integrated converter solution for PHEV/EV.

8.3. System Configuration of Bidirectional Single Phase Cascaded Multilevel Converter

Fig. 8.1 shows the schematic of the proposed CMCS connected to 110 V, 50 Hz, single phase AC input. The system consists of 3 H-bridges (H_T, H_M, H_B) either connected in series as cascade connection or works independently to feed drive operation actuated through proper contactors. Each 3 H-bridges provides 3 Independent DC links (V_T, V_M, V_B). The multi-mode operation is facilitated through contactors (B_i, S_i) as shown in Fig. 8.1. In normal vehicular drive mode, B_i remains at NO position and S_i remains at NC position as shown in Fig. 8.1. Multiple DC links facilitate charging/discharging of battery stacks independently via a buck-boost converter. The battery stack (BB_j where j is 1, 2, 3) on each DC link consists of a series connection of 4 units of 12 V, 17 Ah Li-ion batteries, and each DC link is maintained at 65 V for G2V/V2G operation. For traction drive mode the individual DC link voltage is maintained at 150 V through boost converter operation on the connected battery stack. The power transaction through CMCS for G2V/V2G operation is facilitated through interface inductor connected to 110 V AC at the point of common coupling (PCC). The plugging in of vehicle actuates NO contacts to restrict the operation for only G2V/V2G by simultaneously opening the NC contacts which otherwise would make the connection for traction drive operation invoking the multimode operation. The DC link capacitance (C) value is decided based on the

allowable voltage ripple and power exchange via independent DC link. The independent DC links provide different multiple charging/discharging stacks which leads to better asset utilization.

8.4. Concept of Charging/Discharging of Battery in a String with Dissimilar SOC's

In absence of charge equalizing circuitry the discharge and charge limit of the battery units will be governed by the weakest battery unit in the stack i.e. the one with lesser SoC in case of discharging (V2G) and highest SoC in case of charging (G2V) to avoid deep discharge or overcharging of the battery unit in the stack.

To understand this concept 3 stacks of battery each having 4 battery units are considered. Test- a and Test-b prescribed in Fig. 8.2(a) for discharge mode particularly during V2G and for G2V mode of operation respectively.

Under Test–a condition one battery unit (encircled in Fig. 8.2(a)) of the lower stack

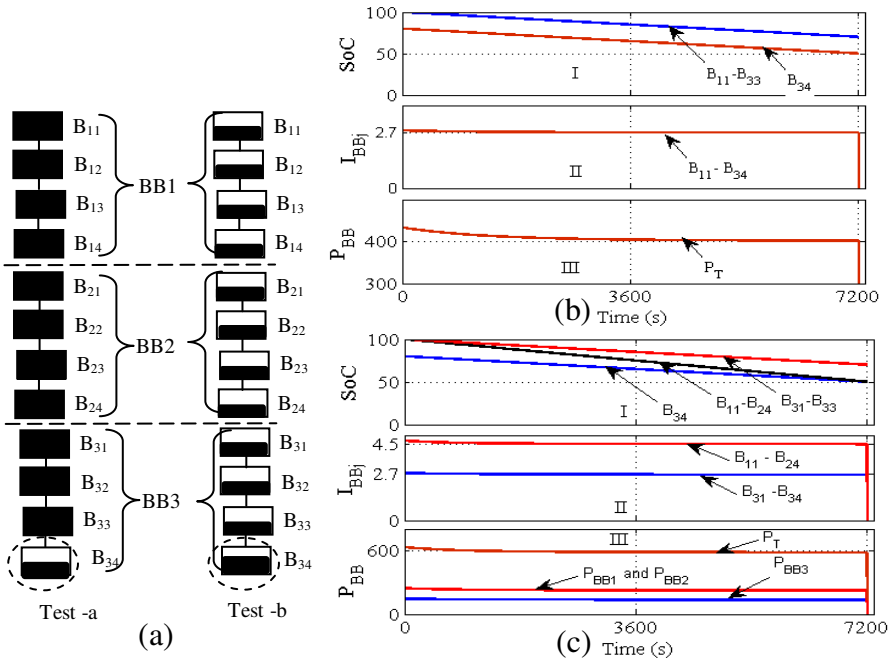


Fig. 8.2: (a) Battery stacks for G2V/V2G (b) Test -a centralized control for V2G and (c) Test –a CMCS based split control for V2G.

(BB3) having lower SoC (80 %) and rests others having 100 % SoC. With centralized converter having all the 3 stacks in series has to keep discharging rate as per the battery unit having lowest SoC, else, it may lead to the deep discharge of the battery in BB3. Fig. 8.2(b) and Fig. 8.2(c) shows the comparative performance for discharging mode under centralized and split control of battery stacks respectively. In Fig. 8.2(b) and Fig. 8.2(c) 50 % is taken as thecritical limit for discharge (during V2G) and G2V, beyond that battery support is turned off to avoid deep discharge of the battery in the stack. In a centralized control operating on 12 units of batteries connected in cascade, set the current limit at 2.7 A due to lower SoC of one battery (80%) restricting to output to 2 hours for a set of the load as shown in Fig. 8.2(b)-II, at a power 400 W (P_{BB}). The remaining eleven batteries (B_{11} –B_{33}) are underutilized.

If the same battery stack is divided into 3 parts (BBj – j is 1, 2, 3) for split voltage configuration, 2 stacks having uniform SoC's (BB1 and BB2) discharged at full rate of 4.5 A while the lower stack (BB3) discharges at 2.7 A due to lower SoC of one battery unit in BB3 stack as shown in Fig. 8.2(c) –II. This results into power discharge capacity of 2 stacks (BB1 and BB2) each around 232 W and for lower stack around 130 W amounting to maximum total power (P_T) is around 600 W as shown in Fig. 8.2(c)-IV, depicts better asset utilization.

Similarly under Test –b for G2V control where the bottom battery unit, as encircled for SoC assumed at 70 % and others having SoC at critical limit of 50 %, the result could be slower charging of stacks with centralized control as compare to split voltage configuration where the stacks may be charged at customized rates as per the need leading to fast charging of battery units.

From the above discussion, it may conclude that without charge balance circuitry, the performance of split voltage control providesbetter-enhanced power transaction capability as compared to centralized one by circumventing extra circuit and complex control.

8.5. Phasor Analysis for Unity Power Factor (UPF) Operation of CMCS for Charging/Discharging

The charging/discharging to/from the split stack is made though H-bridges connected to single phase AC distribution grid to realize plug-in charging and V2G interface. The power drawn /supplied by each of the cascaded multilevel H-bridges (H_T, H_M, H_B) are given by

$$P_j = V_{tj}.\, I_s \tag{8.1}$$

The power exchanged by individual bridges is comprised of both real and reactive power. The real power exchanged is expressed as:

$$P_{j,real} = V_{tj}\, I_s \cos(\varphi) = \frac{1}{\sqrt{2}} (m_i V_i) I_s \cos(\varphi) \tag{8.2}$$

where j is 1, 2, 3 and i is T, M, B as shown in Fig. 8.1. V_{tj} is the RMS value of individual bridge, I_s is the rms value individual H-bridge current and φ is the phase angle between fundamental frequency source current (i_s) and terminal voltage (V_{tj}). For charging φ remains acute angle, but to discharge battery φ becomes obtuse angle as shown in phasor Fig. 8.3 (a) and Fig. 8.3 (b). For cascaded H-bridges connection same source current (I_s) will flow in all the 3 H-bridges of CMCS. The angle between V_{tj} and I_s will automatically arrive at a fixed value through proper control and the same is maintained constant for all 3 bridges under balanced charging/discharging condition as shown in Fig. 8.3. From (8.2) it is clear the for a fixed value of φ, power transacted through each bridge ($P_{j,real}$) may be controlled through individual H-bridge by an alternation in modulation indices (m_i).

8.6. Control Theory for Multimode Operation

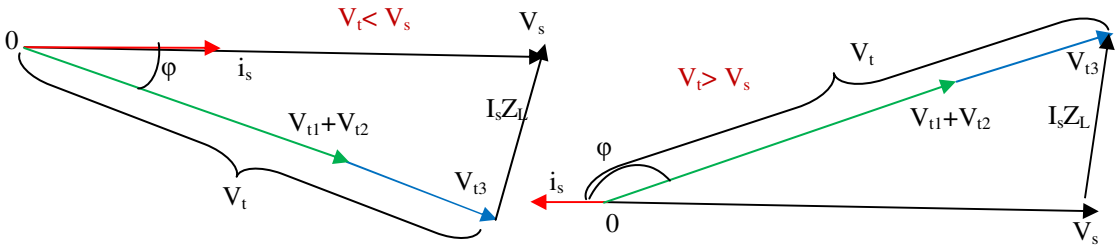


Fig. 8.3: (a) Phasor diagram for charging operation maintaining UPF (b) Phasor diagram for discharging operation maintaining UPF.

The proposed control algorithm paves the way for multi-mode operation of CMCS with the same hardware. Fig. 8.4. shows control blocks for charging and discharging of CMCS system. For battery charging/discharging the reference real component current (i_{ds}^*) either have positive/negative magnitude and its value depends on the overall charging/discharging power demanded by individual battery stacks. The individual battery stack reference current is derived based on droop concept.

8.6.1. Droop Concept for Smart Power Flow Control

Low voltage (LV) grid presents a resistive nature, thus holds R/X ratio greater than 7, prompting higher grid voltage drop with increased power flow in the line, paving the way for P/V control droop for LV grid, which can be expressed as.

$$V_s = V_{s,nom} - K_i\,(P_{BBJ} - P_{BBJ,nom}) \tag{8.3}$$

V_s is the grid voltage, $V_{s,nom}$ is the rated PCC grid voltage, P_{BBJ} is the overall power drawn at any time, $P_{BBJ,nom}$ is the rated allowable power which may be transacted through CMCS system, K_i is the droop constant

In the steady state, assuming PCC voltage as constant, the power exchanged through grid may be written as :

$$V_s = V_{s,nom} - K_i\,V_s\,(I_s - I_{s,nom}) \tag{8.4}$$

Where I_s is RMS value of source current and $I_{s,nom}$ is the rated RMS current allowable to

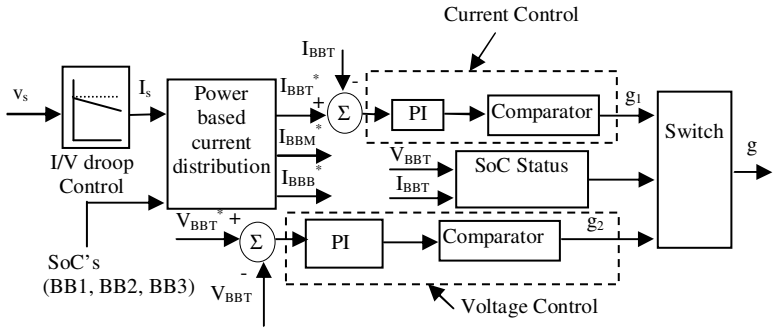


Fig. 8.4: Control blocks for I/V droop control for battery charging/discharging operation in CC and CV mode.

be drawn.

The obtained I_s value as per (8.4) is further distributed through power distribution block for getting reference currents for charging/discharging via a buck-boost converter for individual battery stack according to SoC's of individual battery stack as shown in Fig. 8.4 . As per the allocated share of the individual battery stack, the buck-boost converter is controlled for the transaction of power in current controlled mode or voltage control mode depending on the SoC's of battery stacks. When the battery Soc's reaches 90 % of full charge, the switch control changes the operation from current control mode voltage control mode. Fig. 8.4 shows the gating pulse control for a buck-boost converter for BB3 battery stack.

8.6.2. Control Analysis for Even/Uneven Charge/Discharge of Battery Stack

Conventional Synchronous Reference Frame (SRF) theory, applicable to three phase system for decoupled control, is modified for single phase application for the present system. The source current vector is assumed as i_α and it is delayed by 90° using Hilbert transform to obtain i_β. The unit vectors (cos ωt, sin ωt) are obtained by passing the sensed PCC (point of common coupling) voltage through a fast acting PLL. By utilizing the unit vectors, AC quantities are transformed to DC in SRF using Park transformation.

For
$$x_s = x_{\alpha s} = A \sin \omega t \tag{8.5}$$

Where, x represents i, v and A is amplitude. The virtual quadrature component in stationary frame is represented as:

$$x_{\beta s} = A \sin\left(\omega t - \frac{\pi}{2}\right) \tag{8.6}$$

Using Park transformation the x_{ds} and x_{qs} components are expressed as:

$$\begin{pmatrix} x_{ds} \\ x_{qs} \end{pmatrix} = \begin{pmatrix} \sin \omega t & -\cos \omega t \\ \cos \omega t & \sin \omega t \end{pmatrix} . \begin{pmatrix} x_{\alpha s} \\ x_{\beta s} \end{pmatrix} \tag{8.7}$$

Whereω is the Grid frequency and$\sin \omega t$ is the in phase component of PCC voltage obtained though PLL as shown in Fig. 8.5.

Dynamics of the system depends on the involved active and passive components in a configuration. To arrive at dynamic behavior of the CMCS a set differential equation in d-q frames is being derived for charging condition of battery i.e CMCS takes power from grid to facilitate the battery charging using Fig. 8.1.

$$\frac{di_{ds}}{dt}=\frac{1}{L_r}(V_{ds}+\omega L_r i_{qs}-i_{ds}(R_e)-(m_{dT}V_T+m_{dM}V_M+m_{dB}V_B)) \quad (8.7)$$

$$\frac{di_{qs}}{dt}=\frac{1}{L_r}(V_{qs}-\omega L_r i_{ds}-i_{qs}(R_e)-(m_{qT}V_T+m_{qM}V_M+m_{qB}V_B)) \quad (8.8)$$

Where, i_{ds} and i_{qs} are the d-q component of source current (i_s).

Applying KCL across the node connecting DC link capacitor, the eq. is as follows:

$$\frac{dV_T}{dt}=\frac{1}{C}\left(\frac{i_{ds}m_{dT}}{\sqrt{2}}-I_{BT}\right) \quad (8.9)$$

$$\frac{dV_M}{dt}=\frac{1}{C}\left(\frac{i_{ds}m_{dM}}{\sqrt{2}}-I_{BM}\right) \quad (8.10)$$

$$\frac{dV_B}{dt}=\frac{1}{C}\left(\frac{i_{ds}m_{dB}}{\sqrt{2}}-I_{BB}\right) \quad (8.11)$$

Where, i_s is source current, V_s is the PCC voltage, L_r is line inductance, R_r+3R_{switch} represented as R_e , R_{switch} represents the losses across each H-bridge, R_r is line resistance , I_{Bj} (where j is T,M,B) is battery current at individual DC link, V_i (i is T, M, B) is the DC link capacitor voltage, m_{dj} (j is T,M,B) is the modulation along the d-axis, m_{qj} (j is T, M, B) is the modulation along the q-axis. With the help of above transformation decoupled real and reactive power component of source current are obtained. i_{ds} component of the source current depicts the active power requirement of the load for V_{ds} being constant (d-component of PCC voltage). Reference component of source (i_{ds}^*) is estimated through PI controller by passing error of reference total DC link voltage and actual total DC link voltage as shown in Fig. 8.5. The error in reference source current (i_{ds}^*) with respect to actual value when processed through PI controller to output the deficit/excess voltage under PCC voltage,which when is feed forward estimates the d-component of the voltage which in turn added with decoupled component control yields terminal voltage (V_{dt}) as in Fig. 8.5.

Power demanded/supplied by individual H-bridges is expressed in d- q frame as:

$$S_j = \frac{i_{ds}}{2}(V_{dj} - jV_{qj}) \quad (7.12)$$

Where S_j (where j is T, M, B) is the power demanded/supplied and $V_{tj} = V_{dj} - V_{qj}$ is the terminal voltage in d-q frame of the corresponding individual H-bridge.

So total power demanded/supplied by 3 H-bridges is expressed as:

$$S_{demanded/supplied} = S_T+S_M+S_B = \frac{i_{ds}}{2}[V_{dT}+V_{dM}+V_{dB} - j(V_{qT}+V_{qM}+V_{qB})] \quad (8.13)$$

and power supplied/demanded through the input terminal is given by

$$S_{supplied/demanded} = (V_{dt} - j\,V_{qt})\,\frac{i_{ds}}{2} \quad (8.14)$$

where $V_t = (V_{dt} - j\,V_{qt})$ terminal voltage as shown in Fig. 8.1.

For power balanced operation the (8.13) and (8.14) should be equal and may be expressed as:

$$S_{supplied/demanded} = S_{demaded/supplied} \quad (8.15)$$

$$(V_{dt}-jV_{qt})\,\frac{i_{ds}}{2}=\frac{i_{ds}}{2}\,[V_{dT}+V_{dM}+V_{dB}- j(V_{qT}+V_{qM}+V_{qB})] \quad (8.16)$$

Where V_{td} and V_{tq} can be expressed as:

$$V_{dt} = V_{dT} + V_{dM} + V_{dB} \quad (8.17)$$

$$V_{qt} = V_{qT} + V_{qM} + V_{qB} \quad (8.18)$$

Moreover, terminal voltage can be expressed in generalized terms of source voltage and drop across inductor in d-q reference frame neglecting resistance drop as:

$$V_{dt}=L_r\frac{di_{ds}}{dt}- L_r\omega i_{qs} +V_{ds} \quad (8.19)$$

$$V_{qt} = L_r\frac{di_{qs}}{dt}+ L_r\omega i_{ds} \quad (8.20)$$

For unity power factor operation $i_{qs} = 0$, so above equations can be written as:

$$V_{dt} = L_r\frac{di_{ds}}{dt}+V_{ds} \quad (8.21)$$

$$V_{qt} = L_r\omega i_{ds} \quad (8.22)$$

Substituting value of (8.21) in (8.17), and rewriting (8.21) as:

$$L_r \frac{di_{ds}}{dt} = V_{dT} + V_{dM} + V_{dB} - V_{ds} \qquad (8.23)$$

Dividing both sides by V_{dc} (assuming $V_{dc} = V_T = V_M = V_B$ under steady state), the eq. (8.23) may be written as:

$$\frac{L_r}{V_{dc}} \frac{di_{ds}}{dt} = \frac{1}{V_{dc}}(V_{dT} + V_{dM} + V_{dB} - V_{ds}) = (m_{dT} + m_{dM} + m_{dB} - \frac{V_{ds}}{V_{dc}}) \qquad (8.24)$$

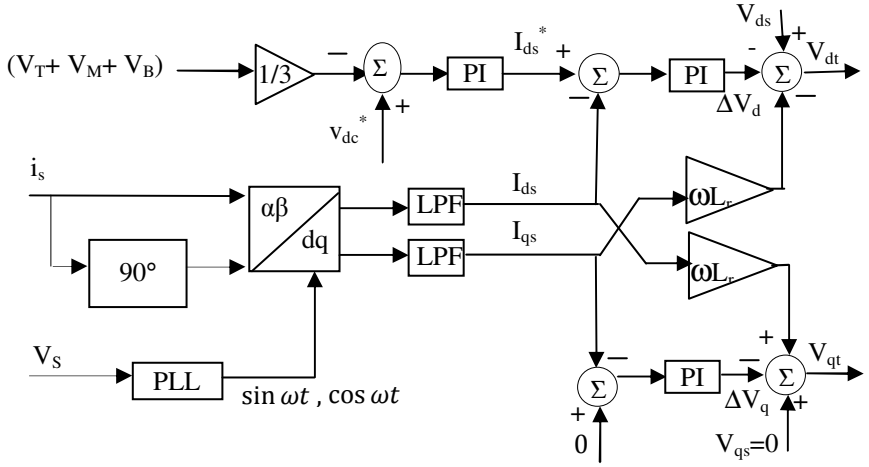


Fig. 8.5: Control blocks of proposed CMCS Configuration.

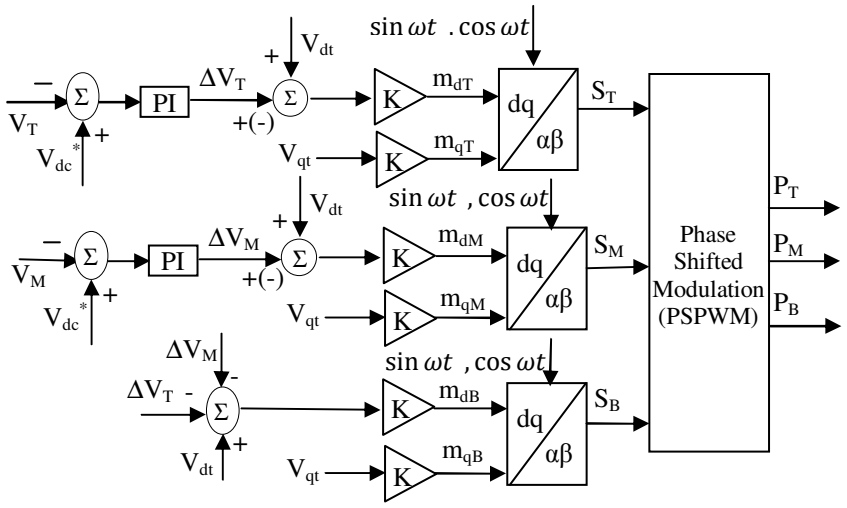


Fig.8.6: Control blocks of proposed CMCS configuration for even /uneven charging/discharging.

Similarly (8.18) can be rewritten by substituting (8.22) in (8.18) and dividing both sides by V_{dc}, the (8.18) may be expressed as:

$$\frac{\omega L_r i_{ds}}{V_{dc}} = m_{qT} + m_{qM} + m_{qB} \qquad (8.25)$$

For stable operation of CMCS, the (8.20) and (8.25), which gives relation among individual H-bridge modulation index have to be always satisfied irrespective of the charging/discharging conditions at the individual H-bridges.

Non-uniform SoC's of different stacks of batteries connected at each level represents the uneven impedance across each DC link. Despite varying impedance across each DC links, if the equal current has to be transacted though buck –boost converter, it may lead to the unequal voltage across DC link of individual H-bridges. So applying voltage balancing algorithm becomes utmost important for smooth charging/discharging of the battery without getting affected by varying rate of charging and SoC of battery stacks on the particular DC link. For DC link voltage balancing individual DC link voltages are compared with reference voltage and the error which might be positive or negative depending whether reference voltage is at positive (+) terminal of summer block or at negative (-) is processed through PI controller to arrive at ΔV_j (where j-T, M, B). Further the obtained voltage (ΔV_j) is added from V_{dt} to arrive at reference d-component of terminal voltage as shown in Fig. 8.6. The reference voltage is at positive terminal (+) in case of G2V and negative (-) in case of V2G to enable proper power transfer. Only two PI controllers are required to formulate the control for balancing the DC link voltage since third may be derived from two PI's controller output with overall change in voltage as zero (ΔV_B=- (ΔV_T+ΔV_M) as shown in control Fig. 8.6.

For either even/uneven current demand at individual H-bridges, the overall power drawn

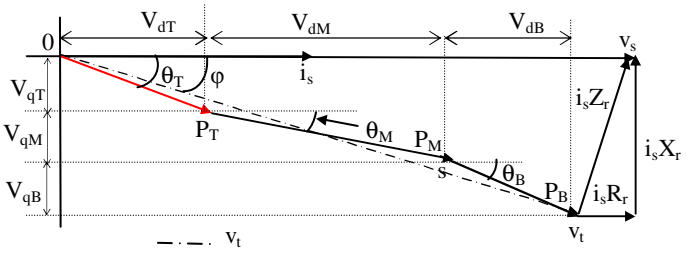


Fig. 8.7: Phasor representation of individual voltages in case of unbalanced loading.

by CMCS is determined through magnitude and power angle (φ) of the overall terminal voltage phasor (V_t) as shown in Fig. 8.7. The distribution of terminal voltage of individual H-bridges under uneven loading will be distributed non –uniformly depending on power to be handled by each bridge. The distribution may only guarantee the equal

DC link voltages of H-bridges with appropriate modulation index. For tackling such unbalanced situation, the individual DC link voltages are compared with the reference voltage and the error is passed through PI controller to add voltage (ΔV_j) to V_{dt} as shown in control diagram Fig. 8.6. Since the H-bridges are connected in series, the same current will be drawn by them, thus, to accommodate the unbalance power requirement, the terminal voltage phasor of individual H-bridge (P_j- where is T, M, B) should be of varying magnitude due to different modulation indexes of individual H-bridges. Such modification forces the alignment of individual ac side voltage phasor (P_j- where j is T, M, B) to be oriented at a different angle as shown in Fig. 8.7. Transforming these individual controlled variable ($m_{dj,}$ m_{qj}) from d-q to α-β frame using reverse park transformation and computing individual switching function as S_j (where j is T, M, B) which is further being used as a input for phase shift modulation (PSPWM) to generate individual H-bridge gating pulses for CMCS.

8.7. MATLAB Based Simulation of Bidirectional Single Phase Cascaded Multilevel Converter

The proposed control for CMCS is simulated under MATLAB simulink environment using Simpower system blockset. To illustrate the multi mode capability of system, the proper control logic is developed for discharging/charging operation of the small battery stack. On each DC link 12 V, 17 AH battery is cascaded to form 48 V battery stack. The CMCS control logic is verified under varying/uniform battery charging condition and V2G application.

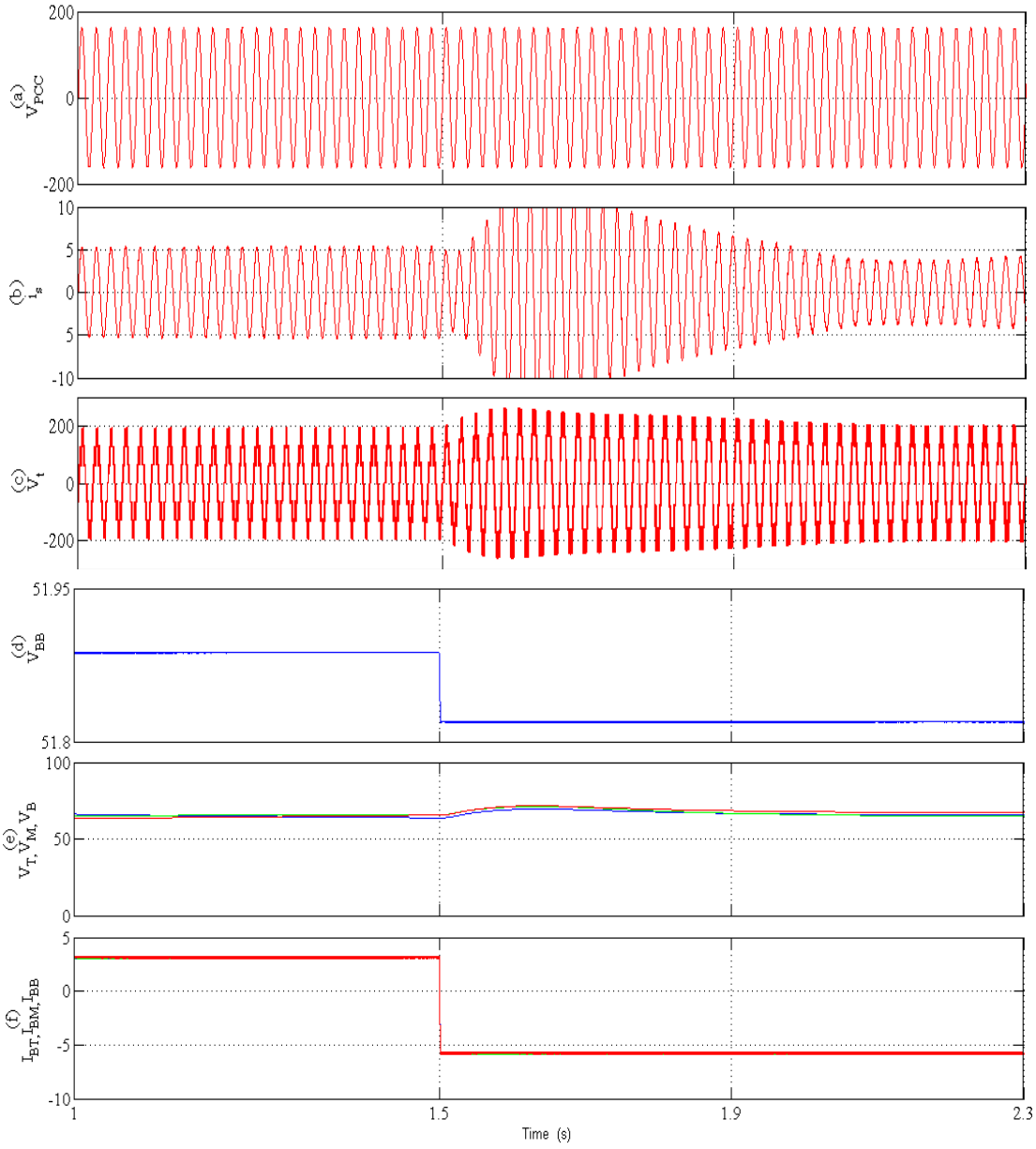


Fig. 8.8: Simulation waveforms of CMCS unit depicting (a) PCC voltage in volt (V_{PCC}) (b) Source current in Amp, (c) Terminal voltage in Volt (V_t) (d) Battery voltage in Volt (V_{BB}) (e) DC link voltages in volt (V_T) (f) Battery charging current in Amp (I_{BT}).

Fig. 8.8. (a)-(f) shows the waveform of PCC voltage (V_{PCC}), source current (i_s), terminal voltage (V_t), battery voltage (V_{BB}), DC link voltages (V_T, V_M, V_B) and battery currents (I_{BT}, I_{BM}, I_{BB}). Neglecting initial transient condition analysis is carried out from t=1s onwards for CMCS operation. Hence as initial condition the CMCS is drawing 3.5 A from source for battery charging as depicted in Fig. 8.8 (b) at constant PCC voltage of

TABLE 8.1
Hardware Components of CMCS

Main supply voltage 1φ, Line Frequency	110V, 50 Hz
DC link voltages	65V
IGBT module	SKM50GB063D
IGBT driver	Skyper Pro 32
DC link Capacitance	2200 μF, 415 V
Controller	Dspace 1104, DSPIC33fJ16GS502
Voltage sensor	LV25P (0-415 V)
Current sensor	EL25P (0-25 A)
Current Probe	Agilent make
Oscilloscope	Agilent DSOX 2014 A
Single Phase Power analyzer	Fluke 345
Multimeter	Fluke mkae
Interface Inductor	6 mH
Motor Mutual Inductance (L_m)	138.4 mH
Battery Rating	17 AH, 12 V, VRLA

110 V. The seven level terminal voltage of the CMCS is shown of slightly reduced value due to charging operation from the utility grid as shown in Fig. 8.8 (c). Meanwhile, from Fig. 8.8 (e) it is clear that DC link voltages are approximately equal and close to set the value of 65 V, while batteries are charged through individual DC links via buck/boost converter. The batteries are shown getting charged at a constant current of 3 A maintained via buck/boost converter as shown in Fig. 8.8 (f). At t=1.5s, on a step transition from charging to discharging modes, a command of 5.2 A is initiated as depicted in Fig. 8.8 (f). In response to such command source current and terminal voltage make a transition to 10 A peak and 230 V peak respectively before settling to the prescribed referenced condition as shown in Fig. 8.8 (b)-(c). From Fig. 8.8 (a)- (b) it may be noted that that steady state source current slowly became out of phase with respect to voltage at PCC confirming the UPF operation in V2G mode. The terminal voltage transient gets settle down to steady state value in a short time of 0.4s as shown in Fig. 8.8

(c). The small rise in DC link voltages across the H-bridges also settles down to steady state value of 65 V in a short span, confirming the robustness and fastness of control.

8.8. Hardware implementation of Bidirectional Single Phase Cascaded Multilevel Converter

The simulated performance of CMCS is experimentally validated on the developed 1.5 KW prototype for multimode operation requisite in PHEV/EV application. The details of hardware components inverters, drivers, sensors, capacitors, inductors and other equipment used for gauging the performance is presented in Table 8.1. Apart from the components mentioned in the Table-8.1 various PCB's cards for different interfaces and

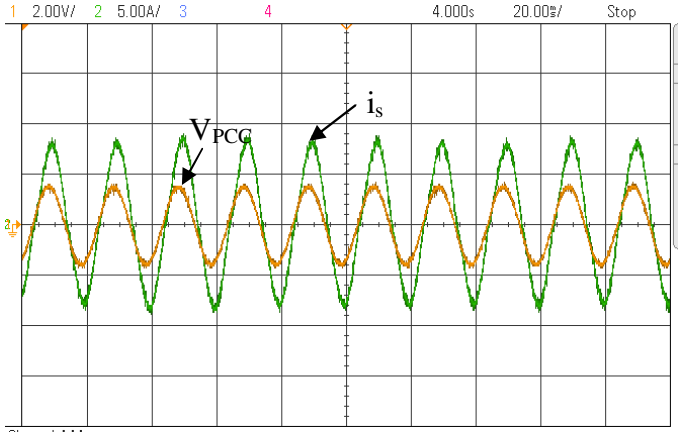


Fig. 8.9: Experimental result showing source voltage (200 V/div), and source current (4 A/div).

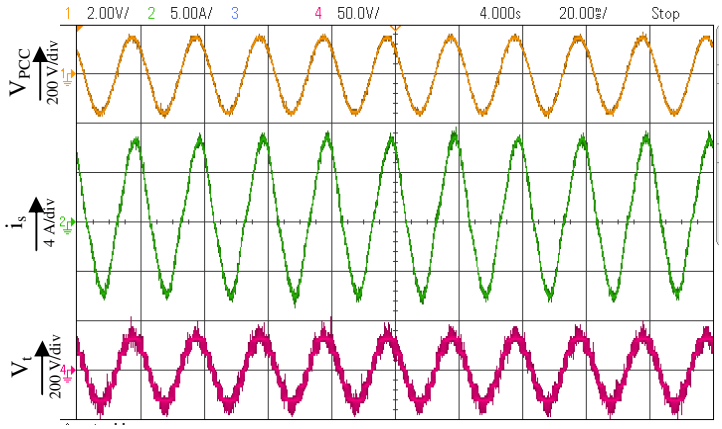


Fig. 8.10: Measured zoomed source voltage ($V_{pcc,}$), source current (i_s) and CMAR input voltage (V_t).

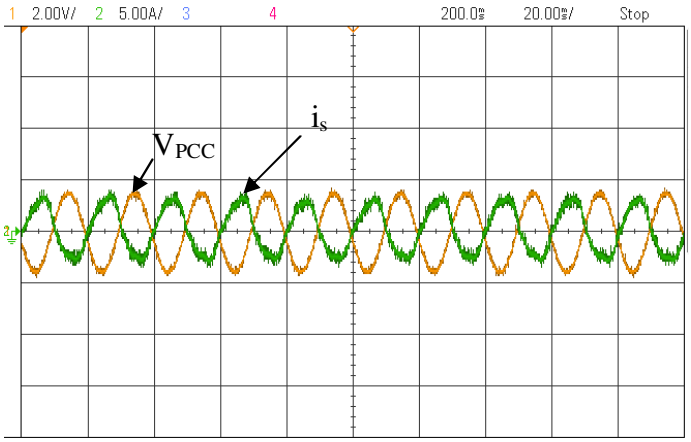


Fig. 8.11: Experimental result showing source voltage (200 V/div), and source current (4 A/div) during discharging for V2G support.

target boards of microcontroller are also developed to realize the system for conducting the experiment. The dSpace 1104 controller facilitate sensing of currents and voltage at different places via on board ADC channels at a sampling frequency of 10 KHz. The multilevel system is operating at 2 KHz. The buck-boost converter controlled for setting the battery charging/discharging rate using slave processor in dSpace 1104 for PWM

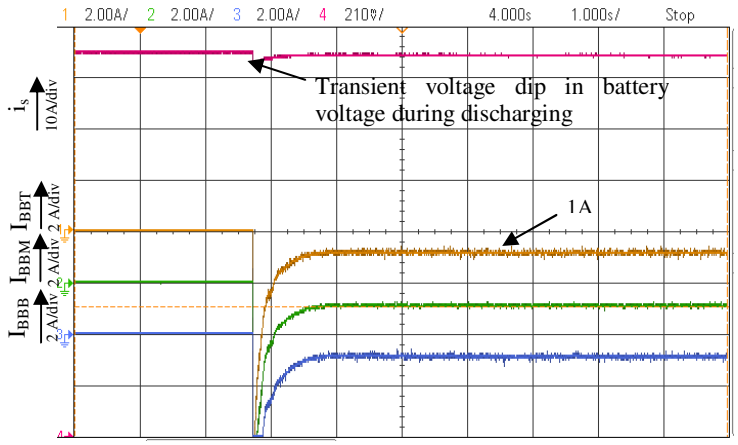


Fig. 8.12: Experimental result showing waveforms for change in battery voltage during discharging mode depicting - Battery currents (I_{BBT}, I_{BBM}, I_{BBB}), Battery voltage (V_{BB}).

generation at 10 KHz.

8.9. Result and Discussion

V2G supportive on-board multi mode CMCS is tested experimentally with the developed prototype in line with simulation. To investigate the control algorithm experimentally and

to examine the system feasibility, various waveforms are recorded using Agilent digital storage oscilloscope (DSO) and Fluke 345 single phase power analyzer.

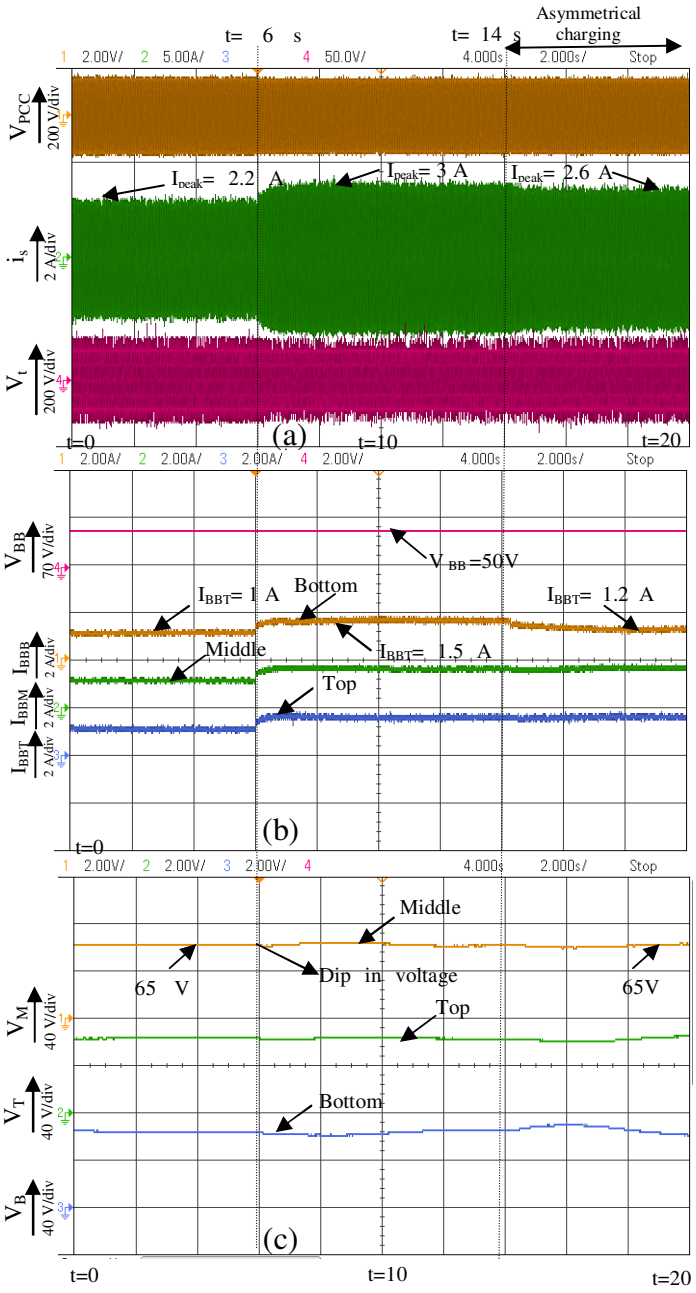


Fig. 8.13: Experimental results showing charging mode of operation (a) source voltage (V_{pcc}), source current (i_s) and CMCS input voltage (V_t) (b) Battery currents (I_{BBT}, I_{BBM}, I_{BBB}), (c) DC link voltages (V_T, V_M, V_B).

8.9.1. Performance Evaluation of Single Phase Cascaded Multilevel Converter for Balanced DC links and UPF Operation

The experimental results shown in Fig. 8.9 conforms to the UPF operation of CMCS where it is clearly shown that source current is in phase with the voltage at PCC. In Fig. 8.10 the voltage at PCC and current drawn by CMCS are shown with respect terminal voltage of CMCS showing 7 distinct levels in voltage waveforms. Similarly, during V2G support, the supplied source current through battery discharging is shown in anti phase with voltage at PCC conforming UPF operation, the same is shown in Fig. 8.11. With a start command as shown in Fig. 8.12. For V2G support, a small dip of 2 V is observed in terminals due to drawl of excessive transient currents requisite establishing the DC link voltage. After the expiry of transient the current settles down at 1 A level indicating approach of steady state condition in one tenth of seconds.

8.9.2. Performance Evaluation of Single Phase Cascaded Multilevel Converter under Same/Different Battery Charging Currents and Study its Dynamics Response

To study the dynamics and response of CMCS under same/different battery charging currents another set of experimentation is performed and results are recorded by triggering three DSO's simultaneously as shown in Fig. 8.13 (a)-(c). Initially with set reference charging current of 1A for individual stack as shown in Fig. 8.13 (b), the drawl from the source (i_s) is 1.5 A as shown in Fig. 8.13 (a). Meanwhile DC link voltage across the H-bridges is maintained constant at 65 V as shown in Fig. 8.13 (c). At t=6s, a step change in reference current command for symmetric battery charging is applied and within 0.1s the charging currents in each battery stack is reach to its referenced value. Accordingly the makes a transition source current from 1.5 A to 2.1 A as shown in Fig. 8.13 (a). However, a small dip in DC link voltages are observed, which recovers quickly with increase in source current, to bring back DC link voltage to 65 V on each DC link as shown in Fig. 8.13 (c). At t=14s, a command for dissimilar charging current is given,

where for the stack on top DC link is commanded to 1.2 A while others are kept as same to determine robustness of CMCS under dissimilar charging conditions. It may be observed in Fig. 8.13 (b) that currents quickly follow the command and settles to

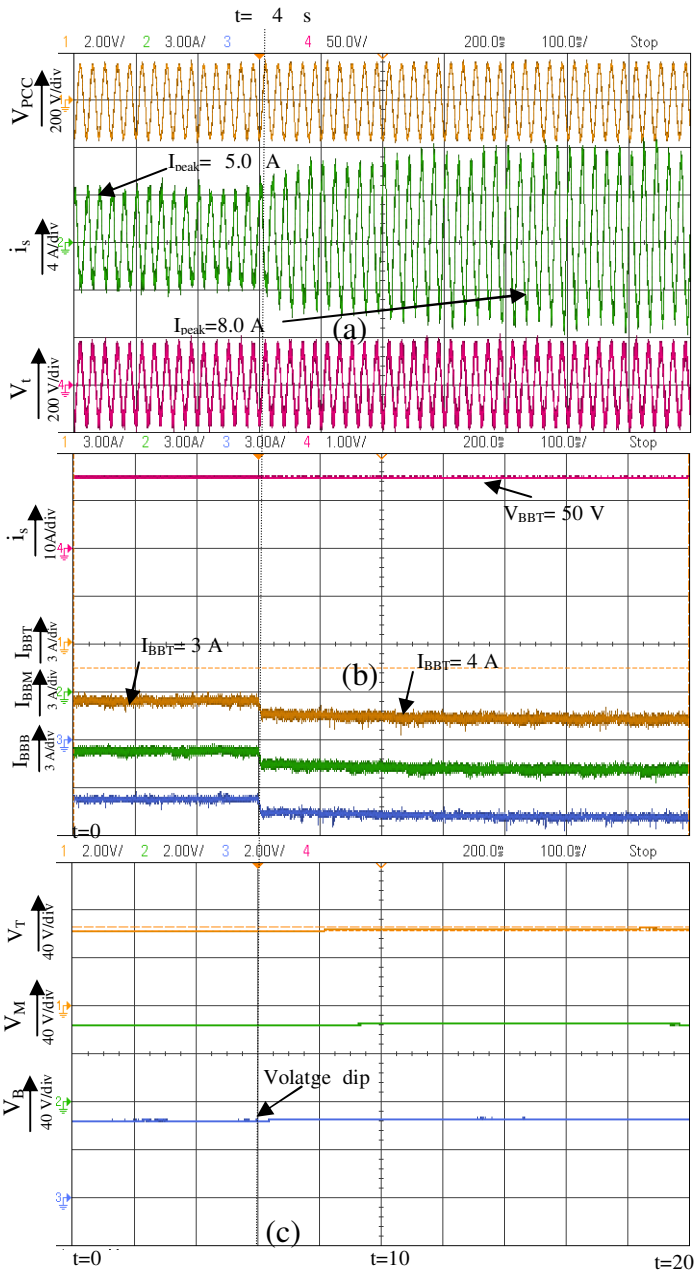


Fig. 8.14: Experimental results showing discharging mode of operation(V2G) support (a) source voltage (V_{pcc}), source current (i_s) and CMCS input voltage (V_t) (b) Battery currents (I_{BBT}, I_{BBM}, I_{BBB}), (c) DC link voltages (V_T, V_M, V_B).

referenced value quickly. Further it may be seen that the drawl of currents from the single

phase utility line drops to 1.8 A. However, due to such asymmetry in current, the DC link

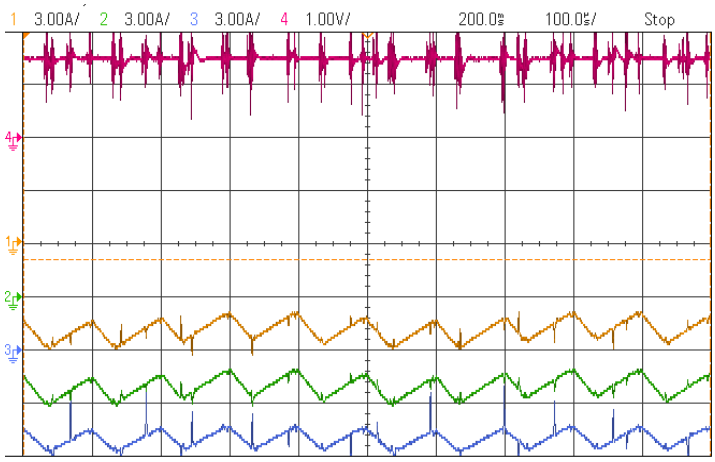


Fig. 8.15: Experimental result showing zoomed waveforms for battery currents (I_{BBT}, I_{BBM}, I_{BBB}) Battery voltage (V_{BB}) during discharging.

voltage of bottom bridge, where current is reduced to 1.2 A show the rise in voltage, which under influence of control return the DC link voltage back to 65 V within 4s.

8.9.3. Performance Evaluation of Single Phase Cascaded Multilevel Converter for V2G support and its transition from G2V to V2G

To establish the performance of proposed solution for V2G support, the set of DSO are used to record similar transients and waveforms in discharging mode as shown in Fig. 8.14 (a)-(c). With a reference command of symmetrical discharge of 3.2 A from individual stack of battery, the source current is steadily maintained at becomes 3.6 A, but in anti-phase with respect to source voltage conforming V2G application as shown in Fig. 8.14 (a). It may be observed that DC link voltage remain balanced at 65 V on each DC link. At t=4s when discharging current command is raised to 4 A, the discharge current instantly follows the suit, as shown in Fig. 8.14 (b), which in turn increases the source current from 3.6 A to 5.6 A. To access the minute details of the happening a zoomed batteries current waveforms are captured and shown in Fig. 8.15, which also shows the battery terminal voltage of the bottom bridge. It may be observed the switches in buck-boost converter are switched at 10 KHz and with a small ripple of 0.5 A the battery currents also follow the same with small ripple in current.

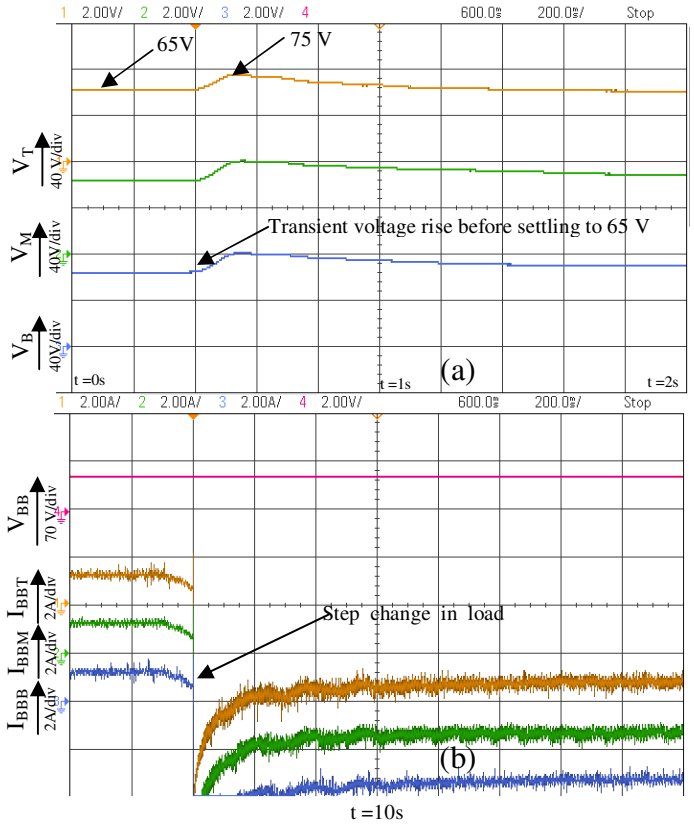
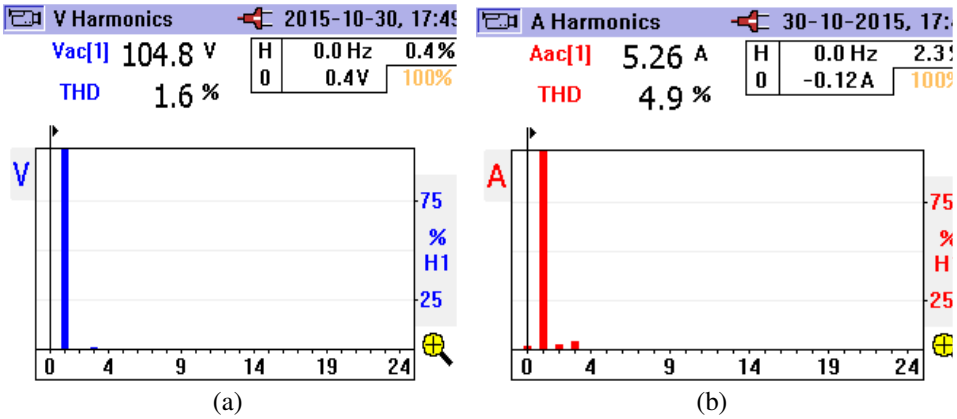


Fig. 8.16: Experimental results showing step transition from charging to discharging mode (a) DC link voltages (V_T,V_M,V_B) (b) Battery currents (I_{BBT}, I_{BBM}, I_{BBB}), Battery voltage (V_{BB}).

To establish the performance of the proposed system for fast current reversal an experiment is conducted, where step transition (charging to discharge) command for battery is applied at t=0.4s as shown in Fig. 8.16 (a) -(b). It may be observed that battery current instantaneously jumps from +1.5 A through each split battery stack to -3.75 A, as



(a) (b)

Fig. 8.17: (a) Waveform for THD of source voltage harmonics showing 3rd harmonic around 1.2% of fundamental (b) THD of source current harmonics showing 3rd harmonic around 4.4% of fundamental.

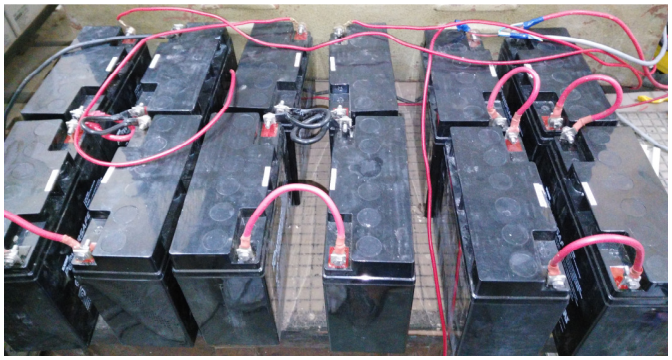


Fig. 8.18: Battery stacks used for experimental setup in CMCS.

shown in Fig. 8.16 (b). Accordingly there occurs a small rise of 15 V on each DC link before settling back to reference value of 65 V in 0.6s. The transient last only for 0.18s. Fig. 8.17 (a) and Fig. 8.17 (b) shows the THD of terminal voltage and source current which is well within limits (1.8 % and 4.9 % respectively) conforming to the IEEE 519 standards. The experimental hardware containing battery units are shown in Fig. 8.18.

8.10. Conclusion

The proposed single phase on-board smart split voltage multi-mode integrated bidirectional converter for EV/PHEV is successfully demonstrated through developed hardware prototype through experimental results. The experimental results clearly demonstrate the capabilities of the controller for providing balanced/unbalanced charging/discharging rate to battery stacks depending upon the SoC's of the stack. The results clearly demonstrate the control algorithm is capable of making the fast transition from G2V to V2G with a nominal overshoot in DC link voltage without compromising the THD of terminal voltage and currents. The result also shows vector control traction drive operation using OEIM having independent windings energized via separate H-bridges. The control algorithm in SRF frame ensures immunity to any noise and harmonics in voltage at PCC. The proposed CMCS system enjoys the advantage of modularity, requirement of small size DC link capacitor which guarantees the extended life for ensuring smooth charging/discharging operation.

GRID/OFF-GRID MULTILEVEL SPLIT VOLTAGE CONVERTER FOR PHOTOVOLTAIC SYSTEM FEEDING VARIETY OF LOADS

DISSERTATION

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE AWARD OF THE DEGREE
OF

DOCTOR OF PHILOSOPHY

Submitted by:

Amritesh Kumar

(Roll no. 2K11/PhD/EE/13)

Under the supervision of

Prof. Vishal Verma

DEPARTMENT OF ELECTRICAL ENGINEERING
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2017

DECLARATION

I, AMRITESH KUMAR (2K11/PhD/EE/13) hereby declare that the work, which is being presented in the project report entitled, **"GRID/OFFGRID MULTILEVEL SPLIT VOLTAGE CONVERTER FOR PHOTOVOLTAIC SYSTEM FEEDING VARIETY OF LOADS"** submitted for partial fulfilment of the requirements for the award of the degree of Doctor of Philosophy is an authentic record of my own work carried out under the able guidance of Dr. VISHAL VERMA, Professor, EED, DTU. The matter embodied in the dissertation work has not been plagiarized from anywhere and the same has not been submitted for the award of any other degree or diploma in full or in part.

Submitted by:-

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CERTIFICATE

This is to certify that the thesis entitled, "**GRID/OFF-GRID MULTILEVEL SPLIT VOLTAGE CONVERTER FOR PHOTOVOLTAIC SYSTEM FEEDING VARIETY OF LOADS**", submitted by Mr. **AMRITESH KUMAR**, Roll No. 2K11/PhD/EE/13, student of Doctor of Philosophy in Electrical Engineering Department at Delhi Technological University (Formerly Delhi College of Engineering), is a dissertation work carried out by him under my guidance during session 2011-2017 towards the partial fulfillment of the requirements for the award of degree of Doctor of Philosophy.

The uniqueness of the thesis pertains to grid/off-grid multilevel split voltage converter for photovoltaic system feeding variety of loads, which has not been reported elsewhere.

I wish him all the best in his endeavors.

(Dr. VISHAL VERMA)
Professor, EED, DTU
SUPERVISOR

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One looks back with appreciation to the brilliant teachers, but with gratitude to those who touched our human feelings. The curriculum is so much necessary raw material, but warmth is the vital element for the growing plant and for the soul of the child.

— Carl Jung

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Mr. Amritesh Kumar
Delhi Technological University
New Delhi

GRID/OFF-GRID MULTILEVEL SPLIT VOLTAGE CONVERTER FOR PHOTOVOLTAIC SYSTEM FEEDING VARIETY OF LOADS

ABSTRACT

With growing pressure on depleting fossil fuels reserves, the focus has been shifted for harnessing more and more energy from renewable sources for sustainable growth. Photovoltaic system has emerged as a most appropriate solution due to proximity to the load centers and more or less predictable nature of intermittency. Conventional centralized photovoltaic (PV) grid tie inverters suffer from the problem of lower efficiency, high filter size, and limited depth of operation for remaining in connection with the grid, particularly under lower insolation/partial shading condition. The effect is reported to be more pronounced for single stage inverters integrating with weak distribution systems.

Further with the advancement of technology the residential loads have witnessed a paradigm shift from linear loads to nonlinear, dynamic and constant power loads which are customizable and configurable to cater specific application. To avoid multiplicity of AC – DC through DC-DC or DC-AC conversions, the concept of DC nanogrids have also evolved to cater the need of a variety of such loads.

Investigation of a multirole bidirectional cascaded multilevel converter (CMC) configuration in which a single phase supply is split into 3 different DC links enabling staggered PV connections and possibility of feeding variety of loads have been carried out. The considered configuration is also utilized to feed isolated single phase loads in an off-grid mode using appropriate modulation technique. Considered loads include dynamic, constant power and passive loads in addition to open-end winding induction motor drive (OEIM), battery charging/discharging etc. The connectivity of the load is considered on DC buses while in off-grid/grid connected mode and on AC side too while in off-grid modes. The proposed system configuration and the considered control algorithm suits to the majority of the residential loads while enabling it to act smartly for stabilizing the grid in case of the need. Further investigation on algorithm involved the DC bus balancing embedded in the control to ensure balanced voltage operation or operation at different voltages dictated by individual MPPT controller

across the DC links. The control scheme is further explored for bidirectional power transfer with smartly charging/discharging control of the split battery stacks at customized rates depending on the SoC's of battery stacks and on feeder loading conditions, without disturbing the DC bus voltages. The exploration has been extended for operation during under-voltage grid condition where the customization in proposed algorithm enables the rotating charge control algorithm which helps the grid to stabilize its voltage in conjunction with maintaining life cycle of the battery.

The proposed configuration and control enjoys the advantage of 3 separate DC buses having both voltage and power level 1/3rd of the total DC voltage and power, which enables the reduction in the voltage rating of capacitor; making system more modular and compact and deriving power from AC is with reduced voltage THD and providing immunity against unbalanced DC link voltages across the H-bridges.

The complete model of the CMC with a variety of loads and their embedded control is analytically derived and simulated in MATLAB Simulink environment before testing on hardware prototype for its validation. A detailed stability analysis is also presented in the d-q frame for the control design to access the feasibility of operation with a variety of loads. The effectiveness of the control algorithm under low grid frequency and dip in voltage conditions are clearly demonstrated through results. The results clearly show derived current from the grid at unity power factor ensuring improved power quality operation. Further, keeping the entire voltages on the DC buses constant or at voltage dictated by MPPT controller ensures immunity against disturbance both from AC or DC side. A comparative analysis is also done for the operation of PV under partial shading condition for a conventional 2 –level PV inverter vis-à-vis proposed CMC-based approach. Further PV-CMC system for enhanced performance under voltage sag is studied to demonstrate the LVRT capability. The d-q based control provides efficient independent and smartly control with active/reactive or both power support depending on the voltage sag and PV panel power condition. The thesis also proposes control techniques for off-grid mode, which will match the utilization and storage of power provided by the PV panels of the same capacity and same size of the battery connected at each level. The control method utilizes rotation policy for the operation of each bridge at each level in three

fundamental cycles, to enhance both the lifetime of the battery, the operation of H-bridges and PV panels used.

Same scale hardware prototype using open end induction motor, passive loads and battery loads (charging/discharging) on different DC links is developed and experimentally validated using requisite hardware and DSP controllers (dSPACE 1104 and dspic33FJ16GS502). The development of hardware including fabrication of various control cards, interface card, voltage and current measurement cards etc. have been indigenously done. Both simulation and experimental results are presented which always show good agreement with theoretical analysis.

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LIST OF ABBREVIATIONS

Abbreviations	Full-Form
PV	Photovoltaic
AC	Alternating Current
DC	Direct Current
P&O	Perturb And Observe
InC	Incremental Conductance
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
VSI	Voltage Source Inverter
MIC	Module Integrated Converter
THD	Total Harmonic Distortion
SHE	Selective Harmonic Elimination
LED	Light Emitting Diode
BLDC	Brushless DC Motor
TV	Television
CMC	Current Mode Control
EMI	Electromagnetic Interference
STATCOM	Static Compensator
PWM	Pulse Width Modulation
d-q	Direct-Quadrature
VVVF	Variable voltage variable frequency
CCAR	Cascaded Converter Active Rectifier
OEIM	Open end winding induction motor
G2V	Grid to Vehicle
V2G	Vehicle to Grid
SoC	State of Charge
SPS	Smart Parking System
EVs	Electric Vehicles
LVRT	Low Voltage Ride Through
BOS	Balance Of System
PSO	Particle Swarm Optimization
HF	High Frequency

VSC	Voltage Source Converter
LSPWM	Level-Shifted Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modulation
IPD	In-phase disposition
APOD	Alternative Phase Opposition Disposition
POD	Phase Opposition Disposition
PS-PWM	Phase shifted pulse width modulation
LMS	Least Mean Square
ADALINE	Adaptive Linear Element
CMV	Common Mode Voltage
BESS	Battery Energy Storage System
CMAR	Cascaded Multilevel Active Rectifier
SRF	Synchronous Reference Frame
PLL	Phase Locked Loop
PCC	Point Of Common Coupling
LPF	Low Pass Filter
PI	Proportional Integral
UPF	Unity Power Factor
PQ	Power Quality
HEV	Hybrid Electric Vehicle
PHEV	Plug-In Hybrid Electric Vehicle
LI-ION	Lithium Ion
CHBMLI	Cascaded Half Bridge Multilevel Inverter
THD	Total Harmonic Distortion
V/F	Voltage/Frequency
DSO	Digital Storage Oscilloscope
SPL	Smart Pump Load
VIL	Variable Illumination Load
ADC	Analog to Digital Converter
LV	Low Voltage
CMCS	Cascaded H-bridge Multilevel Converter System
NO / NC	Normally Open / Normally Close
SSSVC	Solid State Split Voltage Converter
CMIPV	Cascaded Multilevel Inverter Photovoltaic

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5. V. Verma, D. Bhardwaj and A. Kumar, "Power equalized hybrid control of PV fed induction motor pump," 2012 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Bengaluru, 2012, pp. 1-5.

6. V. Verma and A. Kumar, "Single phase cascaded multilevel photovoltaic sources for power balanced operation," 2012 IEEE 5th India International Conference on Power Electronics (IICPE), Delhi, 2012, pp. 1-6.

7. V. Verma and A. Kumar, "Power balanced cascaded multilevel inverter fed scalar controlled induction motor pump sourced from photovoltaic source," 2012 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Bengaluru, 2012, pp. 1-6.

BIODATA

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PROFESSIONAL EXPERIENCE

- Dec 7, 2012- Till date**: Assistant Professor**, Department of Electrical Engineering, Delhi Technological University, Delhi.

EDUCATIONAL QUALIFICATION

➢ **Doctor of Philosophy in Electrical** (Solar Power fed Pump in both grid and islanded mode using H-bridge Multilevel Inverter) (Pursuing)

Delhi Technological University (DTU), Delhi, Completed course work with CGPA 8.5.

➢ **Master of Engineering** in Electrical with specialization in power electronics and drives (2009-2011)

Birla institute of Technology and science, Pilani (**BITS PILANI**), Rajasthan with CGPA 9.27.

➢ **Bachelor of Technology in Electrical and Electronics Engg (2005-2009)**

SASTRA University, India, Graduated with CGPA of 8.44.

➢ **All India Senior School Certificate Examination, (2001-2003)**

Delhi Public School, Central Board of Secondary Education, (C.B.S.E.), Passed with 73%.

➢ **All India Secondary School Examination (2000-2001)**

May Flower School, Central Board of Secondary Education, (C.B.S.E.), Passed with 85%.

Subjects Taught/Laboratory Handled/Developed

- Taking **M.Tech (Part Time) Classes for Power Electronics System (PES)** for DMRC.
- Taking **M.Tech (Full Time) Classes for Renewable Energy System (RES).**
- Power Electronics and Drives , Power Electronics (**B. Tech**)
- Power Electronics Lab, Basic Electrical Engineering Lab
- DSP based Electromechanical System Lab development at DTU (in progress)

- Setting up Photovoltaic Lab and Energy Storage Lab at DTU (in progress)

SHORT TERM / GIAN COURSES

1. One week GIAN course on "Photovoltaic array to utility interface power converter" held in Aug 22-27, 2016 at Department of Electrical Engineering, Delhi Technological University, Delhi.
2. One week GIAN course on "Photovoltaic array to utility interface power converter" held in Aug 22-27, 2016 at Department of Electrical Engineering, Delhi Technological University, Delhi.
3. Two day NaMPET_II sponsored national workshop on Power Electronics held in Nov 6-7, 2015 at Department of Electrical Engineering, Delhi Technological University, Delhi.
4. One week TEQIP-11 sponsored Short Term Training Programme on "Nature Inspired Algorithm & their Application" held in July 13-17, 2015 at Department of Electrical Engineering, Delhi Technological University, Delhi.
5. One week TEQIP-11 sponsored Short Term Training Programme on "Recent Advances and Challenges in Power and Energy for Sustainable Growth" held in June 1-5, 2015 at Department of Electrical Engineering, Delhi Technological University, Delhi.
6. Two week TEQIP-11 sponsored Short Term Training Programme on "Integrating Renewable Energy into Emerging Electrical Power Systems" held in Dec 8^{th} – 19^{th} , 2014 at Department of Electrical Engineering, Delhi Technological University, Delhi.
7. One week TEQIP-11 sponsored Short Term Training Programme on "Recent Trends in Switchgear and protection" held in July 21^{h} – 25^{th}, 2014 at Department of Electrical Engineering, Delhi Technological University, Delhi.
8. One week TEQIP-11 sponsored Short Term Training Programme on "Renewable Energy and Alternative Fuels (REAF-2014)" held in June 16-20, 2014 at Delhi Technological University, Delhi
9. One week UGC sponsored Short Term Training Programme on "Signal Processing in Modern Electrical Systems" held in December 09-13, 2013 at Department of Electrical Engineering, Delhi Technological University, Delhi

CONFERENCES/WORKSHOP/ SIGNIFICANT ACHIEVEMENT

- Presented Research paper in IEEE international Conference, **ICPEICES 2016**, 4-6^{th} JULY, Delhi, India
- Presented Research paper in IEEE international Conference, **ICPEC 2012**, 6-8^{th} Feb,2013,Tamilnadu, India
- Presented Research paper in IEEE international Conference, **IICPE 2012**, 6-8^{th} Dec, Delhi, India
- Attended one day Workshop on **Recent Trend and Advances in Power Electronics and Drives** at Guru Tegh Bahadur Institute of Technology on March 17, 2012.
- Attended "**IET INTERNATIONAL CONFERENCE ON SMART GRID**" in Delhi on 27^{th} Aug 2010.

- Awarded **VEL TECH** Merit **Scholarship** for excellence in academics at **BITS PILANI**.
- Awarded **GATE** Merit **Scholarship** in academics at **BITS PILANI**.

PERSONAL PROFILE

Name of Father	: Mr. Umeshwar Thakur
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