Major Project
Report

LOW PHASE NOISE OCTAVE BANDWIDTH FREQUENCY SYNTHESIZER UNDER VIBRATION CONDITION

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the requirements for the award of the degree of

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in
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Certificate

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Abstract

A frequency synthesizer is an electronic device that translates one (or more) input base (reference) frequency to a number of output frequencies. It can be treated as a "black box" containing individual components or building blocks such as voltage-controlled oscillators (VCOs), frequency dividers, multipliers, mixers, and phase detectors, which, when properly connected, perform this translation function. Its structure is defined by a system architecture that describes the organization and relationships among the individual components. Frequency synthesizer is a key component to virtually any Radio Frequency(RF) and communication and monitoring system, microwave test-and-measurement. Particular problems can occur for frequency synthesizers under vibration. This effects can cause failures. Vibration effects on frequency synthesizers can interfere with data links.Vibration increases phase noise in frequency synthesizers due to its effect on crystal oscillators which have a mechanical component.

In this research the idea is to design a Low phase noise octave bandwidth frequency synthesizer which can work under vibration conditions.We are generating a range of frequencies between 4GHz to 8GHz. Phase noise is very important in the PLL synthesizer because it determines several factors of the device in which it is included. An indirect multiple PLL approach is used in this research. The phase noise that is generated at different points around the loop and depending on how it is generated and in which component it affects the output in different ways.Thats why noise performance of each circuit block in the loop is observed while designing the synthesizer so that best noise performance is obtained. Measurements of the prototype synthesizers phase noise are made.Prototype is simulated and verified before fabricating. Finally module is fabricated and tested. All the results of simulation and testing are given in detail.

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Chapter 1

Introduction

Frequency synthesizers is an electronic circuit that provides a number of different frequencies by combining frequencies selected from group of independent crystal oscillators, frequency dividers, frequency multipliers. Until 1970's frequency synthesizers were not widely used because it requires a considerable amount of circuitry which makes the cost very high. This put them out of range of most applications. But with the introduction of RF cable integrated circuit technology, frequency synthesizer using PLL i.e.phase locked loop became feasible and with their advantages their use became global.
Synthesizers are used as sources of frequency-stable oscillation in radio transmitters, superheterodyne radio receivers, frequency meters and other devices that need to be set at different frequencies within the frequency range appropriate to the operation of the device. Frequency synthesis provides higher accuracy and stability than frequency adjustment by varying the inductance and capacitance of the oscillatory circuit.
There are different types of frequency synthesizers we can use.Each of them has its own advantages and disadvantages.

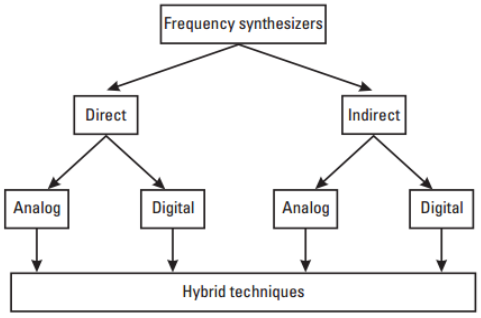


Figure 1.1: Frequency Synthesizer Classes

The two techniques for frequency synthesizer are Direct technique and Indirect technique.[1]-[2] In the direct form of Frequency Synthesizer is that, the waveform transforming element is implemented without any kind of wave formation. Direct techniques are used, including oscillator and mixer forms.

Direct Analogue Frequency synthesis

It is also called a mix-filter-divide architecture. It has several disadvantages, it required a considerable amount of circuitry which adds to the cost. That is why this type of frequency synthesis was only used when all else failed, before the introduction of RF ICs.

Direct Digital Frequency Synthesis

DDS i.e Direct Digital Synthesis are widely used now. It is a powerful technique to use in the generation of radio frequency signals for use in signal generators and many more applications from radio receivers. In recent years, this technique has become very widespread with the progress of IC technology that allows faster control of speed, which enables alternate high-frequency DDS chips.
Indirect frequency synthesis is based on PLL i.e. phase locked loop technology. In PLL the output signal is indirectly generated which means the final signal is generated by an oscillator which is controlled by other signals.

Indirect Analogue Frequency synthesis

In Indirect analogue frequency synthesis PLL has a mixer located between the voltage controlled oscillator and phase detector. This introduces the offset frequency into the loop.In the lock state, the signals entering the phase frequency detector are at exactly same phase and frequencies. The mixer adds an offset to the frequency of the signal coming in the other port of mixer.For an example if the reference frequency oscillator is operating at 100 MHz frequency and the external signal is at 3.9 GHz then the VCO must operate at either 4 GHz or 3.8 GHz. Normally the loop is set up so that the mixer changes the frequency down, therefore in that case the oscillator will be operating at 4 GHz.

Indirect Digital Frequency Synthesis

Indirect digital frequency synthesis uses phase locked loop technology with a frequency divider located between the voltage controlled oscillator and phase detector. Here the frequency of VCO is equal to the frequency divider times the phase frequency detector frequency. Fixed divider or Programmable divider both can be used in this technique. But with the help of programmable we can control the frequency of the VCO by controlling the division ratio. Programmable dividers or counters are used in many ares of electronics like in many radio frequency application. When the divider is added into the circuit, PLL tries to reduce the phase difference between the two signals entering the phase detector. And in the locked state both signal entering the detector are of the same frequencies. Also the VCO is operating at a frequency equal to the phase detector frequency times the division ratio. Nowadays frequency synthesizers use a variety of different techniques and technologies. Typically Direct Analogue Frequency Synthesizer are not used nowadays but the other three are used in variety of applications.

Chapter 2

Literature Review

Frequency Synthesizer is an important component in almost every radio frequency and microwave test and measurement, communication and monitoring system. It generates a stimulus signal and act as a local-oscillator source in a variety of upconversion and downconversion schemes. Synthesizer designs utilize various techniques and are almost as diverse as the number of their applications.
This chapter describes the brief introduction of frequency synthesis, PLL and specification of each building block. Further we are also going to discuss about Phase Noise of each component and how vibration affects it.
An electronic device that translates one (or more) input base (reference) frequency to a number of output frequencies is a frequency synthesizer, as illustrated in Figure 2.1. It can be viewed as a "black box" containing various components or building blocks such as voltage-controlled oscillators (VCOs), frequency dividers, multipliers, mixers, and phase detectors, which, when properly connected , perform this translation function. Its structure is defined by a system architecture that describes the organization and relationships between individual components.[2]

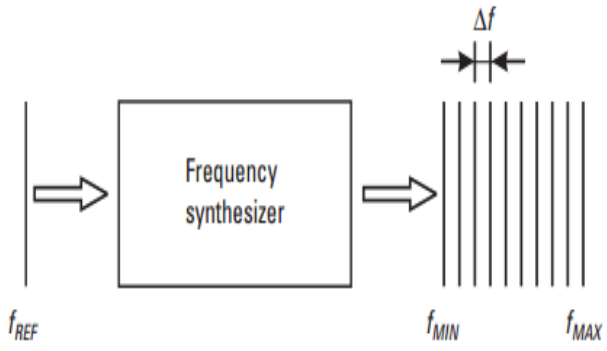


Figure 2.1: Frequency Synthesizer Concept

2.1 PLL Frequency Synthesizer

PLL is a closed loop frequency system that can be used as a frequency synthesizer for synchronizing purpose. In contrast with the past, the PLL Frequency Synthesizer is widely used in all types of radio communication devices. These frequency synthesizers range from cellular phones to various types of wireless products and in different types of home radios and TVs, such as professional radio frequency devices such as signal generators and spectrum analyzer, as well as commercial radio equipment and much more.
Some tasks that can be accomplished by PLL are carrier recovery, clock recovery, tracking filters, frequency and phase demodulation, phase modulation, frequency synthesis, and clock synchronization. PLLs find themselves into a huge set of applications, from radio and television, to virtually every type of communications like wireless communication, telecommunication and even datacommunication, to virtually every types of storage device, to noise cancellers. With the widespread use of these devices, one can claim that PLL is the most common form of feedback system built by engineers.[3]
PLL frequency synthesizers offer great benefits in using other forms of oscillators. The frequency synthesizer not only provides high levels of stability and accuracy, but it is also easly controlled with the help of digital circuits such as microprocessors. But most PLL frequency synthesizers are primarily used as radio frequency oscillators. Nowadays frequency synthesizers are used in many radio chipsets from radios and televisions to cellular phones.

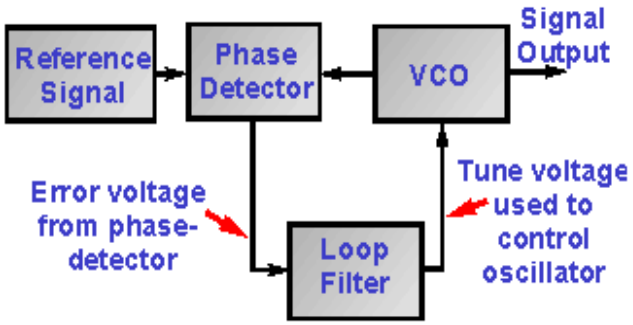


Figure 2.2: A general PLL block diagram

The most basic block diagram of a PLL is shown in Figure 2.2. Every PLL must have these components:

- **A phase detector (PD)**. This is a nonlinear device within the PLL compares the phase of two signals and generates a voltage according to the phase difference between the two signals.

- **A voltage controlled oscillator (VCO)**. This is another nonlinear device which produces an oscillation and its frequency is controlled by a lower frequency input voltage called tuning voltage.

- **A loop filter (LF)**. This filter is used to filter the output from the phase comparator in the PLL. It is used to remove any component of the signal, which is being compared to the VCO line. It also governs many of the characteristics of the loop and its stability.

- **A feedback interconnection**. Namely the phase detector takes as its input the reference signal and the output of the VCO. The output of the phase detector, the phase error, is used as the control voltage for the VCO. The phase error may or may not be filtered.

The main concept PLL operation is relatively simple, however the mathematical analysis of its operation can become more complicated.[4]
The basic phase locked loop is connected as shown Figure 2.2. The reference oscillator and the output from the voltage controlled oscillator are connected into the phase detector. The output from the phase detector is passed through the loop filter and then applied to the voltage controlled oscillator.The Voltage Controlled Oscillator, VCO, within the PLL produces a signal which enters the phase detector. Here error voltage is produced by comparing the phase of the signals from VCO and the incoming reference signal. This corresponds to the phase difference between the two signals.
The error signal from the phase detector passes through the low pass filter which controls many properties of the loop and removes any high frequency element on the signal. From the output of the filter the error signal i.e. the tuning voltage is applied to the control input terminal of the VCO. The effect of any change in this voltage is that it attempts to reduce the phase difference, thereby reducing the frequency between the two signals. Initially the loop is not locked and the tuning voltage will pull the frequency of the VCO towards the reference frequency , until the error cannot be reduced any further and the loop is locked.
When the PLL is locked, a steady state error voltage is generated. If an amplifier is used between the phase detector and the VCO, the error between the signals can be minimized. However there is always some voltage present at the terminal of the VCO as this is what puts onto the correct frequency. This means that if there is a steady error voltage, the phase difference does not change between the reference signal and the VCO. Since the phase between the two signals does not change, it means that the frequencies of the two signals are exactly the same.
With that one would think that the study of PLLs is mostly fill with control theory and that control theorists would have the more expertise in PLLs. In fact, most of the PLL text used in the control theory is a small amount of non-linear heuristic linear system design shown in [5]-[6]-[7]-[8]. The stability analysis and loop designing tends to be done by a combination of linear analysis, rule of thumb, and simulation.

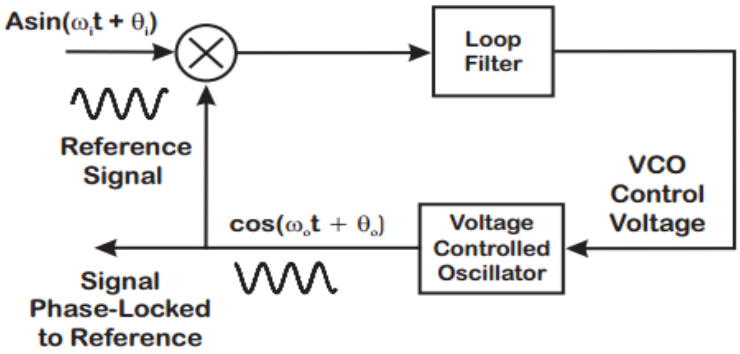


Figure 2.3: A classic mixing phase locked loop

Typical block diagrams of PLLs resembles Figure 2.3, however practical PLLs often more closely resemble Figure 2.4, in which a high frequency low pass filter is used to attenuate the double frequency term and a bandpass filter is used to limit the bandwidth of input signals to the loop.

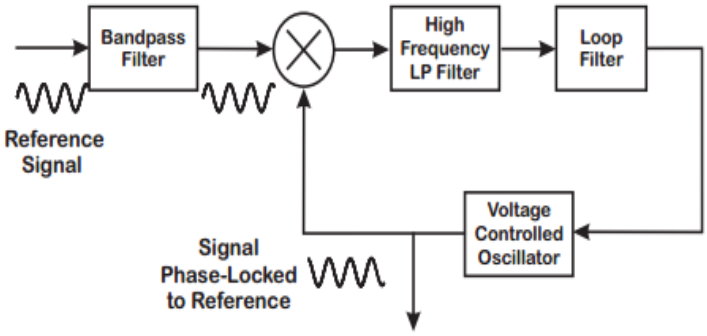


Figure 2.4: A practicle version of classic mixing phase locked loop

Here the bandpass filter is used outside the loop to limit the input noise and a high frequency low pass filter inside the loop to attenuate the 2x frequency component with minimum impact on loop dynamics.

2.2 Fractional N Synthesizer

Frequency N frequency synthesizers use a method of changing the division ratio within the digital PLL synthesizer to provide frequency, which are not integral multiples of the comparison frequency.In PLL frequency synthesizer, the output frequency is an integral multiple of the comparison frequency. If 'n' is the division ratio of the divider in the loop, then the output frequency will be n times the comparison frequency. It uses the basic digital PLL loop. It has a VCO, Phase Detector, Loop filter, divider and we can even use a mixer within the loop as well. However to explain the operation, the case we are using is of a simple digital loop with a divider added to the basic PLL.

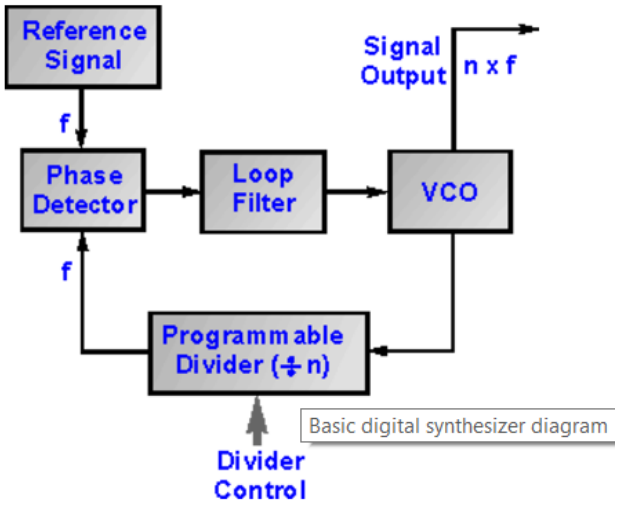


Figure 2.5: Basic Digital Frequency Synthesizer

In the above Figure 2.5 the phase detector compares the two input signals i.e. reference signal and divided VCO signal. Here if the two input signals of the detector are of same frequency the loop will be locked. This only means that the VCO is operating at a frequency equal to the division ratio times the phase comparison frequency.
But it has a certain disadvantage, for example if a loop operating at 10MHz and require a a 100 Hz step size thereforeit will need a division ratio of 100000 ans it affects the loop performance. As we know that loop bandwidth must be around one-tenth of reference comparison frequency, means for above example we get loop bandwidth of only 10Hz. This result in loss of performance.[9]
By using fractional-N architecture phase noise can be improved; however, switching speed and loop bandwidth improvement is possible by increasing f. The concept behind the Fractional N synthesis is as the name suggests the divider takes on a fractional division ratio rather than an integer one.To achieve this, the divider alternatives between division ratios.
Typically it will change between N and N+1, the proportion of the various division ratios determined to give the required frequency.

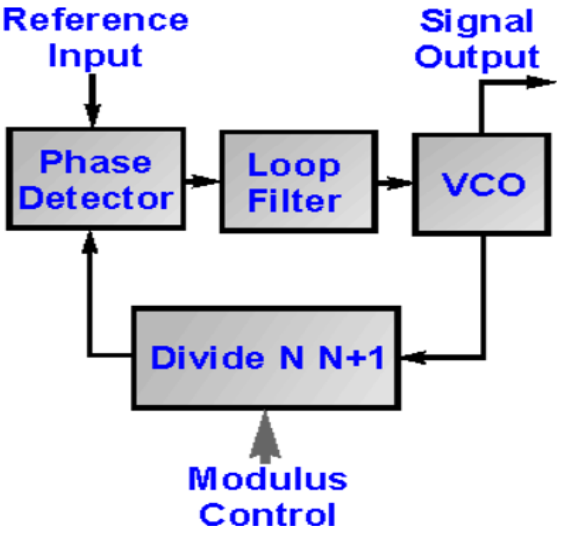


Figure 2.6: Fractional N Frequency Synthesizer

The output frequency in fractional-N designs is given by

$$F_{vco} = F_r \frac{N}{K/F} \tag{2.1}$$

where,
F = fractional resolution of the device with respect to the reference frequency.[10]. For example:- If we need a 30 kHz channel spacing and have a fractional resolution of 16, Fr will be 480 kHz and N is reduced by a factor of 16.
One of the advantage of using Fractional N synthesis is that the step frequency can be small while to improve the overall synthesizer performance high comparison frequency and loop bandwidth can be allowed. And also it is easy to calculate overall division ration if we use a dual modulus divider. To determine the effective division ratio, it is necessary to know the two division ratios and the number of VCO cycles for which each division ratio is effective. Therefore the effective division ratio can be calculated from the formula:[9]

$$N_{eff} = \frac{A+B}{\frac{A}{N} + \frac{B}{N+1}} \tag{2.2}$$

where,
N_{eff} = overall division ratio
A = number of cycle divided by N
B = number of VCO cycles dividedby $N+1$

2.3 Building Blocks

As we discussed in Chapter 1 that the The frequency synthesizer may be considered a black box containing all the necessary components for converting the input reference signal into a number of output frequencies. The performance of synthesizer depends solely on characteristic of individual components used in design. This section deals with the building blocks of frequency synthesizer that we already discussed in Section 2.1 but here we discuss it in detail.

2.3.1 Oscillators

Oscillators is an electronic circuit or electronic device that is used to generate periodically oscillating electronic signal such as sine wave or square wave. It converts the DC i.e. direct current signal into an AC i.e. alternating current signal. The radio and television transmitters are broadcasted using the signals generated by oscillators. The video game sounds & electronic beep sounds are generated by the oscillator signals. Principle of oscillation used by these oscillators to generate signalscan be find in[11].
There are different types of oscillator electronic circuits but our concern is in Crystal oscillator. **Crystal Oscillator** is an electronic circuit that is used to generate an electrical signal of precise frequency using mechanical resonance of vibrating crystal's made from piezoelectric material. Piezoelectric resonators are of different types but typically we use quartz crystal. That is why this type of electronic circuit is called Crystal oscillators.

Voltage Controlled Oscillator

It is a an oscillator which produces an outut signal that we can vary over a range and controlled by the input DC voltage. It is an essential component for frequency synthesizer. It has many other application other than frequency synthesizer like in function generator, electronic jamming equipment, production of music.
Normally, the frequency of oscillation in harmonic oscillators is decided by tank circuit because it manifest electrical resonance at a desired oscillation frequency.

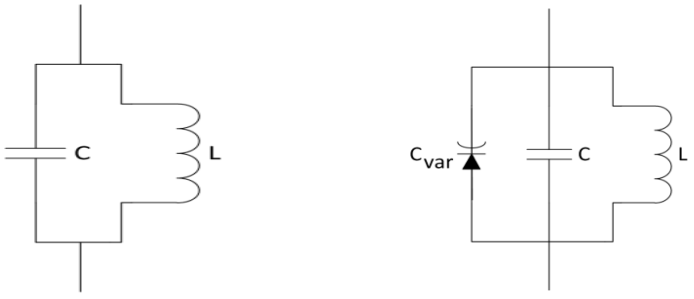


Figure 2.7: Regular LC Resonator & LC Resonator with Varactor

The oscillation frequency of above oscillator is :

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}} \tag{2.3}$$

where, L is the inductance & C is the capacitance. As we can see that by varying any one of them (L or C) it is possible to tune the oscillaton frequency. In VCO, tuning can be achieved by changing the capacitance varactor capacitor is used, which is voltage controlled capacitor. Variable inductor could also work but is difficult to manufacture. To tune the oscillation frequency, a controlled voltage is supplied which in turn tunes the varactor capacitance[**?**]. Output frequency of VCO is described as :

$$f_{out} = f_o + K_v v_{tune} \tag{2.4}$$

where, f_{out} is the output frequency, K_v is the VCO's tuning gain (MHz/V) and v_{tune} is the tuning voltage applied to the VCO's input.

VCO's that are used in this project are :-

- Coaxial Resonator Oscillator-CRO CVCO55CXT-6400-6400 from Crystek Microwave.
  Frequency Range 6400 MHz
- HMC431LP4/431LP4E VCO from Analog Devices.
  Frequency Range 5.5 - 6.1 GHz.
- HMC466LP4/466LP4E VCo from Analog Devices.
  Frequency Range 6.1 - 6.72 GHz.
- HMC1166 VCO with half frequency output from Analog Devices.
  Frequency Range 5.705 - 6.31 GHz.
- HMC585LC4B wideband VCO from Analog Devices.
  Frequency Range 4 - 8 GHz.

2.3.2 Frequency Multiplier

A frequency multiplier is an electronic device that produces harmonics of the input signal, we can also say that it produces a signal whose frequency is the harmonics of its input signal frequency. Frequency multiplication is achieved by introducing a component with non-linear behaviour that distorts a signal waveform and therefore generates harmonics.[12]-[13]. It is used mostly in frequency synthesizers to multiply reference signals or to extend operating frequency range.
Frequency multiplier produces an output signal whose which is N multiple frequency of input signal where N is an integer. If the frequency of the signal is multiply by N using an ideal frequency multiplier increases the phase noise of the multiplied signal by a factor of $20logN$dB.
Frequency multiplier that I am using in this project is to double the frequency range of DDS i.e. Direct Digital synthesizer about which we are going to discuss later in thesis.

2.3.3 Frequency Divider

A frequency divider is an electronic ciruit that produces an outpput signal which is 1/N frequency of the signal applied where N = integer value. It works in the exact opposite way as the frequency multiplier that means it brings phase noise and PM-spurious improvement at the same $20logN$ rate [13][14][15].
Frequency divider is of two types Digital divider and Analog divider. Frequency dividers are used for both analog and digital applications.They can be used to improve the performance of electronic countersmaker devices, laboratory equipments and communication systems. Frequency dividers and multipliers are the main components of modern RF and microwave systems. Their main application is to be used in frequency synthesizer. For applications like phase modulator or demodulator or in microwave multiplier frequency loops only fixed dividers are required. To control loop frequency divideract as phase dividers so that the factor 1/N is allowed in loop equations.The basic arrangement of high frequency programmable divider is shown in figure 2.8

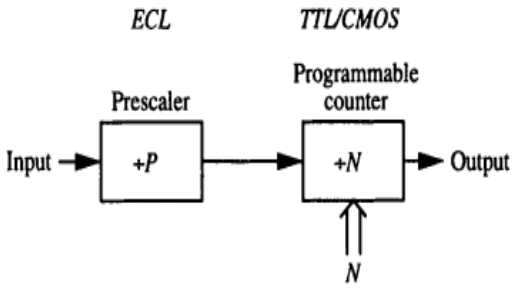


Figure 2.8: High frequency programmable divider using a fixed-ratio prescalar

In PLL circuit frequency divider is inserted in the feedback path between phase

frequency detector and voltage controlled oscillator.
The frequency divider that is used in this project is:-

- HMC434 Divided by 8 Prescalar from Analog Devices.
  Frequency Range is 0.2 GHz to 8 GHz.

2.3.4 Frequency Mixer

An electronic circuit that produces signals whose frequencies is the sum and difference of two input frequencies and its harmonics is a frequency mixer. Frequency mixers are used in direct analog synthesizer and also in the indirect synthesizer where mixing frequency is involved. Frequency mixers are available in ICs but can also be built from separate parts.

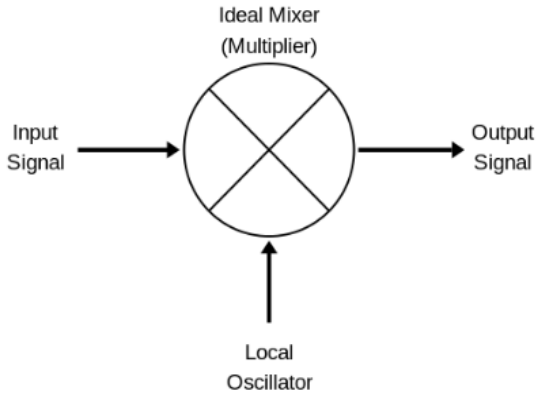


Figure 2.9: Frequency Mixer symbol

Frequency mixer is a key component in a superhetrodyne recevier. Frequency mixer that is used in this project is GaAs, MMIC fundamental mixer :-

- HMC787A from Analog Devices.
  Frequency Range 3GHz to 10GHz

2.3.5 Phase Detector

A phase detector is electronic device that compares the two input signals and the generates the output voltage signal which represents the phase difference between the two input signals. Phase detector is the main element of any PLL synthesizer.There are many types of phase detector but it may be split into two categories **Phase only sensitive detectors** & **Phase-Frequency detectors**.

Phase only sensitive detectors

As the name suggest Phase only sensitive detectors are the detectors that are only sensitive to phase. These are simplest detectors. They produces an output signal which is proportional to the phase differene between the two input signals and when that phase difference is steady, detector produces a constant voltage and when there is a frequency difference, detector produces a varying voltage.
Now it is quite possible that the difference frequency signal will fall outside the passband of loop filter. If that happens then there is no error voltage which can be fed back to lock the voltage controlled oscillator. This means the loop can be locked over a limited range[16].

Phase-Frequency detectors (PFD)

Phase of the signal and frequency of the signal are both sensitive in PFD. An error signal generated by PFD is feedback to (VCO) voltage controlled oscillator, if the phase and frequency of the input signal is same in PFD it gives a DC output voltage. Mixers can resolve the phase differences in $+/-\pi$ range whereas PFD can resolve phase differences in $+/-2\pi$ range, it describes the phase difference of more than 2π.
PFD consists of a pair of D-type flip-flops & an AND gate connected as shown in figure 2.10. At the AND gate output a time delay element is added to remove dead zone (uncertainty) in output when the signals are in-phase. PFD has two outputs marked as up & down. If at the up-output it gets logic high signal, it commands the VCO to increase the frequency and if it gets logic high signal at the down-output, it commands the VCO to decrease its frequency. And the lock is achieved when both the outputs is at zero [2]

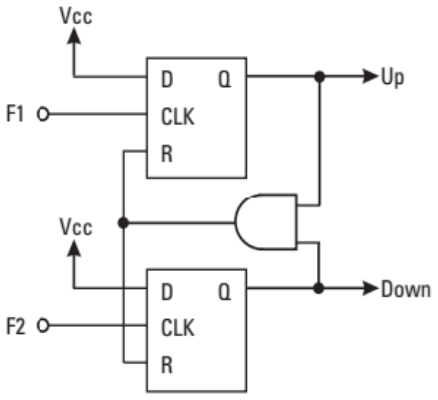


Figure 2.10: A phase frequency detector produces a frequency-sensitive signal when PLL is out of lock

The main advantage of PFD is that it is sensitive to frequency as well. Phase frequency detector are available as IC's and often combined with other PLL components on the same chip.

Typical applications are:-

- Point-to-Point Radios.
- Satellite Communication System.
- Military Applications.
- Sonet Clock Generation.

The PFD used in this project is:-

- HMC439QS16G/439QS16GE HBT Digital Phase-Frequency Detector. Frequency Range 10 - 1300 MHz.

2.3.6 Loop Filter

As all the other components of the PLL, loop filter also the important component while designing PLL. It is an important element for the performance of PLL.basic model of PLL is shown in Figure 2.11

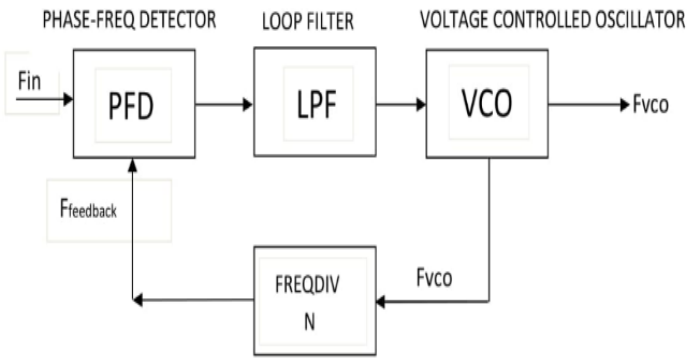


Figure 2.11: Basic model of PLL

Phase-frequency detector produces a error output signal and if there is no loop filter this error signal directly applied to voltage controlled oscillator. Error signal contains dc term and high frequency term which is undesirable. So loop fiter removes high frequency noise of the detector otherwise they will appear in the VCO tune line which eventually appears at the o/p of VCO as spurious signals.

It also influences the ability of the loop to change its frequencies. Tune voltage changes slowly, if the Loop filter has low cutoff frequency. Therefore VCO will not be able to change its frequency fast. This happens because filter with low cutoff frequency let only low frequency through and these results to slow changes in voltage level.[17][18]

Similarly filter having high cutoff frequency lets the tune voltage to change faster which enables the VCO to change its frequency accordingly, however care should be taken to stop the unwanted frequency to pass. Since the loop filter only allows to pass the low frequency signal and blocks high frequency it must be Low Pass Filter.

It also influences the stability of the loop and influences the hold and capture ranges.

Loop filters can be divided into two types **Passive loop filter** & **Active loop filter** and each one has certain advantages over other.

Passive loop filter

It has a certain advantage over Active loop filter and it is generally recommended, provided charge pump in PLL will supply enough voltage to operate the VCO tuning voltage. It cost is low, it requires comparatively less area, it has realtively low noise and has unlimited frequency range.

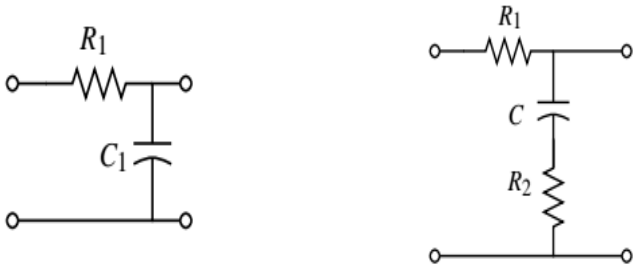


Figure 2.12: Passive Loop Filters

Transfer function of the filters in Figure 2.11 are :

$$F(s) = \frac{R_1}{R_1 + 1/sC_1} = \frac{1}{sR_1C_1 + 1} = \frac{1}{1 + s\tau_1} \tag{2.5}$$

where, $\tau_1 = R_1C_1$
and

$$F(s) = \frac{R_2 + 1/sC}{R_1 + R_2 + 1/sC} = \frac{sCR_2 + 1}{sC(R_1 + R_2) + 1} = \frac{1 + s\tau_2}{1 + s\tau_1} \tag{2.6}$$

where, $\tau_1 = C(R_1 + R_2)$ and $\tau_2 = R_2C$

When the values of C and R are large like $C > 100pF$ and $R > 100K\Omega$ it is hard to integrate. It is also difficult to get a pole at origin in passive loop filter.[17][18].

Active Loop Filter

It is superior in many aspects from Passive loop filter, it gives better spur performance, it can place the poles and zeroes closer to DC than a passive filter. It can be used to increase the loop gain of the overall circuit. The biggest advantage of active filter is that when the charge has a low compliance range and large one is required for VCO to work in a desired range, it eliminates the dependence between the charge pump compliance range and VCO control voltage.
Since its an active filter it also provides isolation in the loop filter. It can get poles at origin and can able to reduce the passive element size. One type of active filter is shown in Figure 2.13

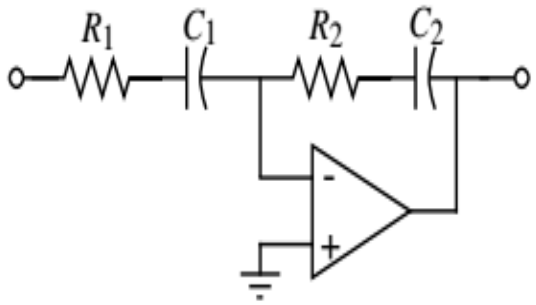


Figure 2.13: Active Loop Filter

But it has some disadvantage like it gives high noise than passive filter and also frequency range is limited in active loop filter[17][18].

The loop filter used in this project is :-

- Second order Active Loop Filter.
  Loop Bandwidth = $1MHz$
  Phase Margin = 75^o.
- Opamp IC used in filter is THS4031, THS4032.

Chapter 3

Phase Noise under Vibration Condition

In this chapter, the discussion is about phase noise, phase noise in VCO and PLL, effects of vibration in phase noise and what measures should be taken to reduce the effects of vibration in phase noise.

3.1 Phase Noise

Phase noise a.k.a phase jitter is the key element in radio and RF communication as it affects the performance of the systems. It is only possible in the ideal world to get a no phase noise signal but practically it is not possible. Every signal in practical have some phase noise.
Phase noise is defined as the noise caused by small phase fluctuations occurring in the signal. Typical phase noise profile of a signal source is shown in figure3.1

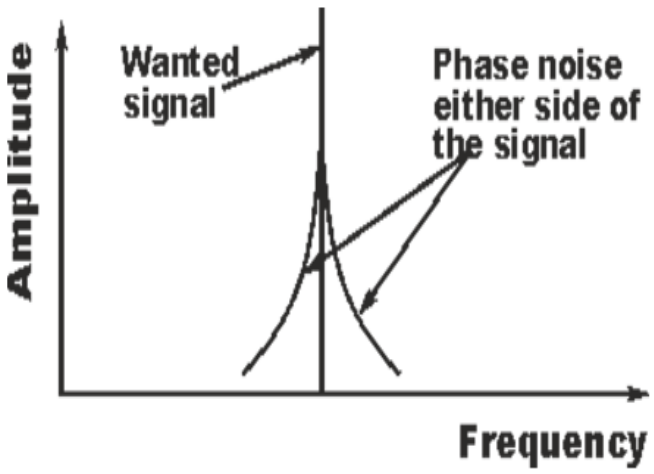


Figure 3.1: Typical phase noise profile of a signal source

Phase jitter is the small disturbances in the phase. In ideal conditions, spec-

trum analyzer shows single spectral line of the provided signal beacuse the signal generated by signal source has no phase noise. However in practical there is always some phase noise and these results in broadening the bandwidth of signal.
Ideally, output of an ideal oscillator is a pure sine wave. But in reality there is no ideal oscillators. All oscillators have certain noise which deviate it from its ideal behaviour, such deviation is called phase noise. The output of a practical oscillator can be described as :-

$$s(t) = A(t)cos(\omega_0 t + \phi(t)) \tag{3.1}$$

where,
$A(t)$ = Amplitude variations.
$\phi(t)$ = Phase variations.

Amplitude noise is much smaller than phase noise so its not a big problem and can be easily filtered using limiters. But on the other hand phase noise is difficult to get rid off.
Fundamental frequency broadening in a PSD signifies that the oscillator output energy is also at the nearby frequencies rather then only at the oscillation frequency. Phase noise which is near to the carrier is called close-in phase noise and phase noise which is further away is called broadband phase noise[**?**].
To specify a phase noise for an oscillator usually power spectral density plot is used referred as $L(f)$. Unit of phase noise is dBc/Hz.

According to IEEE phase noise is defined as :-

$$L(f) = \frac{S_\phi(f)}{2} \tag{3.2}$$

where,
$S_\phi(f)$ = single sideband power spectral density of $\phi(t)$

Phase noise can occurs in communication system and it affetcs its performance.It occurs in receivers when an RF signal is to be downmixed to an IF. If additional signals are available at nearby frequencies to RF input, and we get a leakage frequency space instead of desired signal on the IF side, it happens due to smearing caused by phase noise and if the that disturbing signal is stronger than it become the dominant one at the IF frequency.

3.2 Phase Noise in Frequency Synthesizer

Every components in frequency synthesizer produces noise and it will contribute to the overall noise at the output. And depends upon where the noise is produced this element in the loop contributes to the output. Phase noise produced in phase frequency detector will affect the output in a different way then the noise generated by VCO. For example:

3.2.1 Noise generated by VCO

Different mechanism like thermal noise, flicker noise and shot noise causes phase noise in VCO. A typical VCO noise spectrum shown in above figure 3.1. In addition to the phase noise shown in the figure, we also get a display of unwanted peaks at certain frequencies in the power spectral density plot of a VCO. These are called spurious frequencies or in short we call it "spurs". Some spurs are always present like the VCO harmonic frequencies but they are easy to filter since they generate far away from carrier frequency. Unfortunately some of them are not easy to filter like the ones which are caused caused by electromagnetic interference from a trace on the PCB.
Output of the VCO is connected to frequency divider and divider output is connected to the one input of PFD i.e. phase frequency detector, from detector output signal have to pass through loop filter which will only allow the noise below its loop cut off frequency to pass. It will cancel out the noise on VCO. It will also reduce the level of noise inside the loop bandwidth but have no effect on noise outside the loop bandwidth[19].

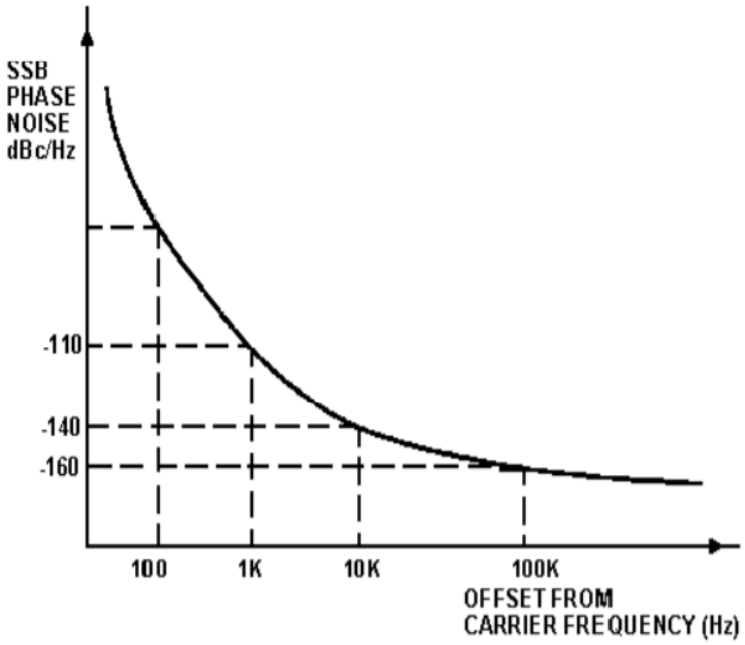


Figure 3.2: Single Sideband Phase Noise Representation

The Phase Noise generated by VCO is determined by :-

- High Quality factor of a resonant circuit.
- Choice of oscillator.
- Correct feedback level.
- Sufficient oscillator power output.
- Power line rejection.

By keeping in mind the above key elements optimum VCO phase noise performance is possible. Since phase noise is a key parameter in many situations, it is important that the performance of VCO phase noise meets its requirements. In this way, VCO phase noise performance will not affect the overall system performance[20].

3.2.2 Noise generated by PFD

Phase Noise generated by phase-frequency detector will affect the overall system in a different way then VCO. Here also the nosie component below loop bandwidth can pass through loop filter. These restricts the components outside loop bandwidth to appear on tuning voltage at control terminal of VCO. It reduces the level of noise inside loop bandwith as all this effect take place within loop bandwidth and therfore it has no effect outside loop bandwidth.
Phase detector dead zone is one other issue designer phase while designing low phase noise frequency synthesizer.
These occurs when designers used digital phase detectors. If there is a small phase difference between two signals and the loop is in locked state, phase detector logic gates produce a very short pulse. These short pulses do not charge the charge pump which reduces the loop gain and this forces up the phase noise/jitter. We can overcome this by adding delay in phase detector reset path[19].

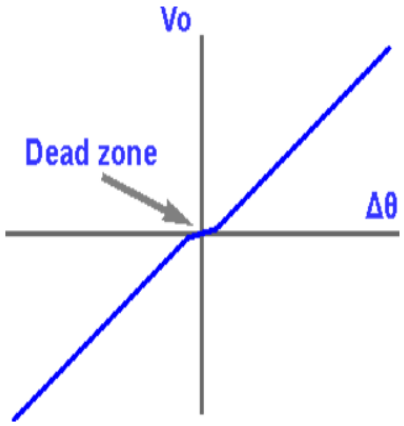


Figure 3.3: Phase detector output charactristics showing dead zone

3.2.3 Noise generated by frequency multiplier and divider

Matters are worse in the case of division ratio, since it has the effect of multiplying the noise level because the synthesizer has the effect of multiplying the reference frequency. As a result the noise level is also multiplied by $20logN$ factor, where N is the division ratio.
Specifically if frequency of the signal is increases by a factor N using ideal frequency multiplier in PLL then its phase noise is also increases by a factor $20logN$. Similarly if frequency of the signal is decreases by a factor N using ideal frequency divider in PLL then its phase noise is also decreases by a factor $20logN$.

3.2.4 Frequency Multiplier

Let the signal,

$$f(t) = cos(\omega t + \theta) \tag{3.3}$$

Frequency multiplication by N means the cosine augument $cos(\omega t + \theta)$ multiplied by N. N is also multiplied to phase noise term in θ. The phase noise is increased by $20logN$[21].

Frequency mutiplier with a frequency modulated input

For a frequency modulated signal

$f(t) = cos(\omega_c t + \beta sin(\omega_m t))$

for small β

$f(t) = cos(\omega_c t) + (\beta/2)[cos(\omega_c - \omega_m)t - cos(\omega_c + \omega_m)t]$

after N frequency multiplication

$f(t) = cos(N\omega_c t + N\beta sin(\omega_c t))$

for small $N\beta$

$f(t) = cos(N\omega_c t) + (N\beta/2)[cos(N\omega_c - \omega_m)t - cos(N\omega_c + \omega_m)t]$

- The sideband amplitude is increased by N. i.e by $20Log(N)dB$

3.2.5 Frequency Divider

For signal,

$$f(t) = cos(\omega t + \theta) \tag{3.4}$$

Frequency division by N means the cosine augument $cos(\omega t + \theta)$ divided by N. Also, any phase noise term in θ is also divided by N. The phase noise is decreased by $20logN$[21].

Frequency divider with a frequency modulated input

For a frequency modulated signal

$f(t) = cos(\omega_c t + \beta sin(\omega_m t))$

for small β

$f(t) = cos(\omega_c t) + (\beta/2)[cos(\omega_c - \omega_m)t - cos(\omega_c + \omega_m)t]$

becomes after frequency division by N

$f(t) = cos((\omega_c/N)t + (\beta/N)sin(\omega_c t))$

for small β/N

$f(t) = cos((\omega_c/N)t) + (\beta/2N)[cos(\omega_c/N - \omega_m)t - cos(\omega_c/N + \omega_m)t]$

- The sideband amplitude is decreased by N. i.e by $20Log(N)dB$

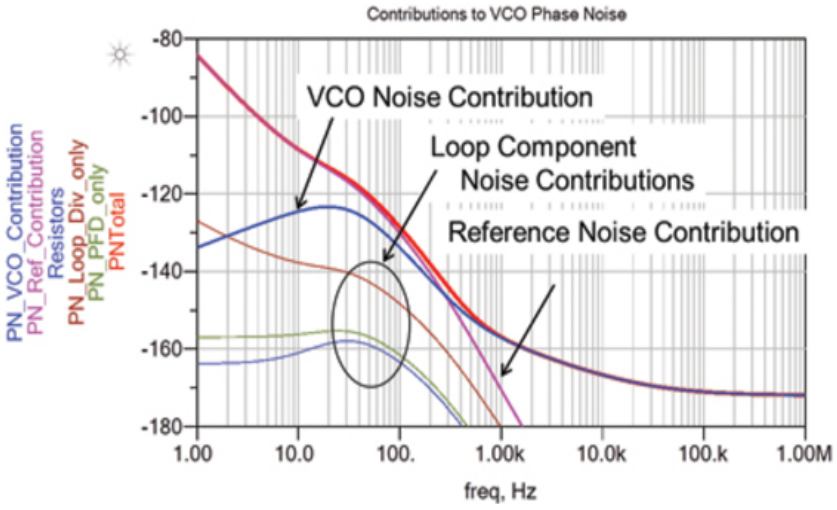


Figure 3.4: Loop component contribution to overall phase noise

3.3 Vibration Induced Phase Noise

Quartz crystal oscillator is the oscillator used as a reference frequency oscillator source for frequency synthesizer as well as for fixed local oscillators. It has many significant applications in communication, radars, sensors and navigation systems, also in missiles, helicopters and UAVs. Even in severe dynamic environmental conditions, these systems must give their required performance Crstal oscillators often provide low phase noise to in a static environment to satisfy particular system requirements[22][23].

There are different types of crystal cuts for different performance characteristics. The most oftenly used cuts are **AT cut** & **SC cut**.

AT cut
AT cut is the one the widely used cuts and is mostly used for electronic circuits. This cut is made from Y bar at 35^o theta rotation. AT is required when oscillator operates in a range 500KHz to 300MHz.

SC cut
The SC cut is also called stress compensated cut. It is defined by theta of value 34.11^o and phi of value 21.93^o. In SC cut, the stresses observed in AT cut is reduced or eliminated. SC cut provides good phase noise and aging characteristics. One of the difficulty that SC cut face is its cutting method of operation is difficult and labour cost is also high.
SC cut crystal oscillator is used in this project.

Other crystal cut types

BT cut
Another cut similar to AT cut is BT cut. In AT cut, angle from z axis is 49^o. Operates in a frequency ranges from 0.5 to $200MHz$. Tempreture stability characteristics is not as good as AT cut.

XY cut It is mostly used for low frequency operation. Comparatively less expensive then other oscillator which work in low frequencies. Ranges from 5 to $100KHz$. One common frequency used is 32.768KHz. It has a low impedance and low C0/C1 ratio.

GT cut
GT cut crystals cuts at an angle of $51^o7'$. Frequency ranges from 0.1 to $2.5MHz$.

IT cut Its cut is similar to SC cut. Has operating frequency ranges between 0.5 to $200MHz$. But it does not have the lower level of mechanical stress sensitivity like SC.

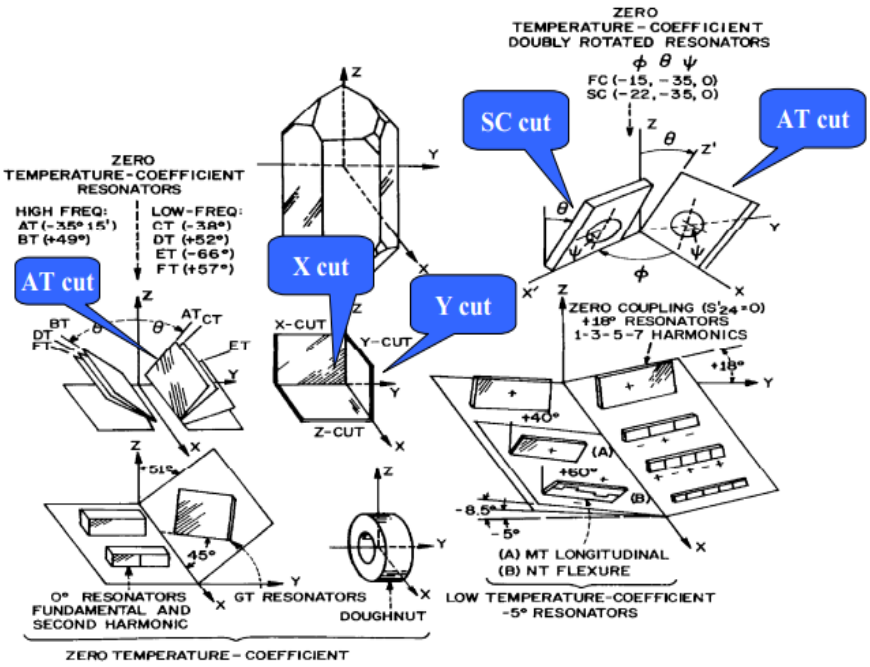


Figure 3.5: Most popular crystal cuts

Quartz crystal oscillators are acceleration sensitive and when accelerated its frequency changes to a small degree. Acceleration can be in the form of shock, steady accelartion and vibration. Using "two-g tipover" test stable oven oscillator sensitivity can be observed. In this test, force on the crytal changes by two 'g' when oscillator is turned upside-down. SC cut crytal is normally used for frequency synthesizer. Typically 10 MHz crystal will change about 0.02 Hz which provides sensitivity of about 0.01 Hz per g[24][25].
Acceleration sensitivity means phase noise induced in crystal oscillators because of random mechanical vibration in mechanical equipments. Vibration sensitivity originates mostly from phase fluctuations within the oscillators positive feedback loop. It usually happens due to physical deformation in non frequency determining components.
Factors responsible for high acceleration sensitivity of resonator are :-

- Sensitive or non-linear mechanical coupling effects.
- Lack of symmetry in mechanical resonator.

Portable electronic equipments that are exposed to vibrations for example in helicopters, jets or simlply trucks, buses and train. Stationary equipments are not safe either they can vibrates by nearby vibrating machinery .
Careful design and mount selection of crystal provides resonance in high frequency where mechanical dampning is more effective[22][24].

3.3.1 Acceleration Sensitivity

Let f_v be the vibration frequency from mechanical shock, the carrier frequency deviates by Δf at the rate of f_v from f_o nominal frequnecy because of vibration induced phase fluctuations. Therefore spurios sidebands will appear at $f_o \pm f_v$. In below figure 3.6 we can see the PM noise of test oscillator under 100Hz vibration along one axis.

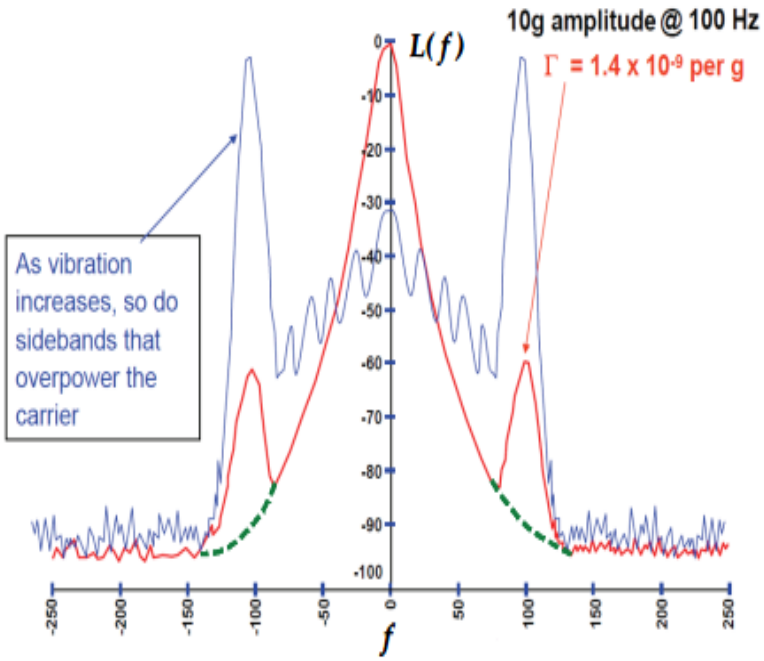


Figure 3.6: Phase noise of an oscillator at a vibration ($fv = 100Hz$)

where, f is the offset frequency from the carrier.
From the above figure 3.6 we can also see that sidebands exceeds the carrier power as the increase in vibration .
Acceleration sensitivity can be expressed by the magnitude and direrction as it is vector quantity but it can also be expressed as the sum of three orthogonal vectors alligned with the sides of oscillator.

Induced Phase Noise :-

$$L(f) = 20log((AccelerationSensitivity \times Acceleration \times OscillatorFrequency)/(2 \times VibrationFrequency)) \tag{3.5}$$

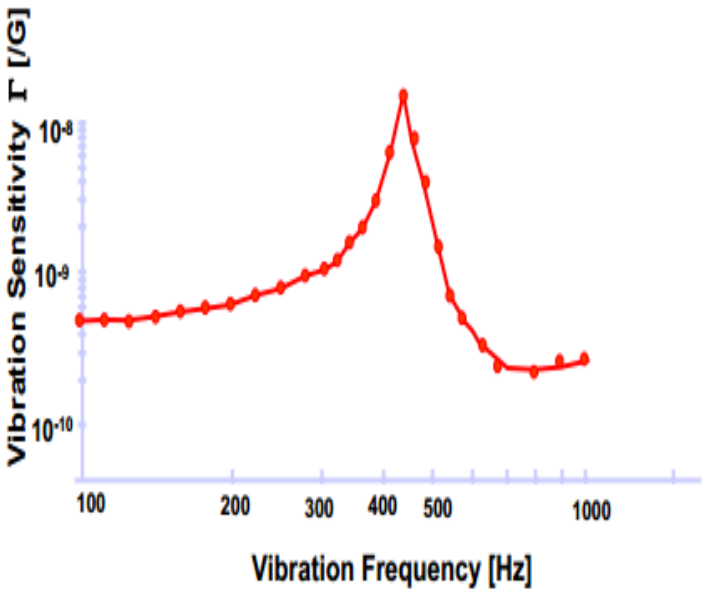


Figure 3.7: Acceleration Sensitivity with Resonance

In an ideal oscillator $\Gamma(f_v)$ is constant but practical oscillator manifest resonance which increases the Γ in a relevant frequency band.

Acceleration Sensitivity determined by the following factors :-

- Cut of crystal.
- Crystal holders.
- Mounting structure.
- Crystal design.
- G sensitivity of components.

Acceleration sensitivity is a vector quantity and the vector nature of it means it will be most sensitive to vibration in any particular direction and in any orthogonal direction to sensitive vector, sensitivity approaches to zero.
In critical systems, the oscillator is placed in a way that the sensitive vector points must be in the direction where vibration is less or in the direction of best isolation, when vibration isolator is used.

There have been many efforts to reduce the vibration induced phase noise. Most common method is to select low sensitive crystals & isolate the oscillators with a low frequency vibration isolators. An external vibration mount can be used to provide low natural frequency, omni-directional urethane shock mounts can also be used when small size mounts in required. The designers must choose vibration mounts very carefully as it is a very important part for vibration isolation systems.

3.3.2 Vibration Isolation

Vibration isolation system can only effectively reduce the system vibration when the vibration is above the systems resonant frequency. And the amplified response at resonant frequency rely on the isolator damping characteristics. While , Isolation systems has very less effect on vibration under resonant frequency.
In few cases, when vibration systems are poorly chosen it can make the matter worse and even damage the system. However in most of the cases, vibration isolation system is vey effective and reduce the most of the vibration level. Even low resonance frequency of the device protects high natural frequencies components. For example, Suppose we use a vibration isolation system whose natural frequency is lower then $200Hz$ and we know that PCBs resonance frequencies are above $1000Hz$. So vibration energy which have the potential to create trouble in the system will be attenutated.
It is usually difficult to attain a low frequency resonance below $100Hz$ when mounting small components for example crystal oscillators. There are more thsn one options for shock mounts and vibration isolation materials. Therefore the designers must keep in mind some important aspects before designing like materials lifetime, its effects on tempreture, availability of space and number of other applications specific considerations.
Aeroflex International Inc manufactured an isolator which is better in many aspects. It is a complete metal design its lifetime is high and provides good and consistent performance over tempreture. It also offers omni-directional isolation and excellant damping because of its stranded wire rope design[22].

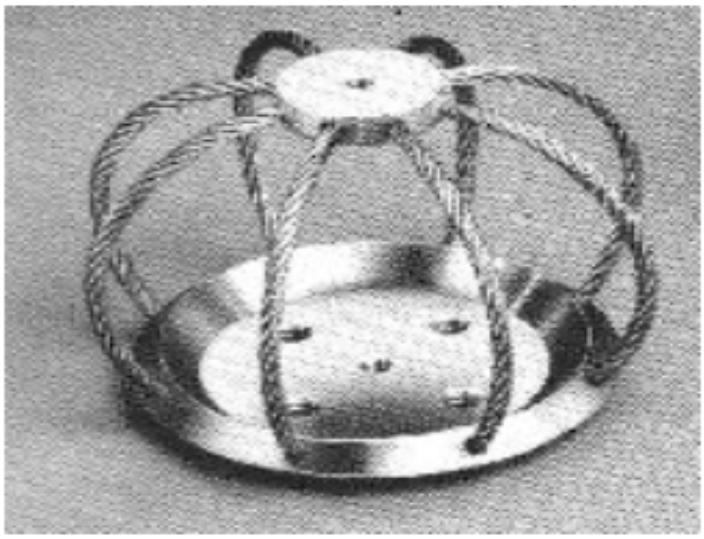


Figure 3.8: Aeroflex Isolator
Courtesy Aeroflex International, Inc.

Chapter 4

Design Process

We already discussed about the concepts that is needed for frequency synthesizer design is already discussed. In this chapter, practical applications are used to design. **Hittite PLL** design tool from Hittite Microwave Corporation and **ADIsimPLL** software from Analog Devices are used to design PLL first, to understand phase noise simulation. The aim of this project is to design a "Octave Bandwidth Frequency Synthesizer Under Vibration Condition" and To understand the overall design concept, firstly a block diagram is created as a high-level pictorial model.

After that, **Advanced Design System(ADS)** from keysight is used to transform this block diagram into a schematic that shows connections of every components required. After getting the desired simulation from ADS ,the design is laid out and implemented on a PCB. To do that we again design the schematic with proper ICs that are used and also design layout in **PADS PCB Design** software from Mentor Graphics.

We are also going to discuss about how to create the hardware model of proposed circuit. Finally, the circuit is properly tested in spectrum analyzer and obtained readings are documnented.Some minor changes are required to develop this design into a stable product that can finally released as a product.

4.1 Components Used

The components that are used to design frequency syntheszer of desired specifications are provided in below table 4.1

S.No.	Components	Model No.	Frequency Range
1	VCO	CVCO55CC	3.2 - 3.3 GHz
2	VCO	HMC431LP4	5.5 - 6.1 GHz
3	VCO	HMC1166	5.7 - 6.31 GHz
4	VCO	HMC466LP4	6.1 - 6.72 GHz
5	VCO	HMC586LC4B	4 - 8 GHz
6	FREQ. DIVIDER	HMC434	0.2 - 8 GHz
7	FREQ. MIXER	HMC787A	3 - 10 GHz
8	PFD	HMC439QS16G	10 - 1300 MHz
9	POWER DIVIDER	MAPD-011007	5 - 2150 MHz
10	SWITCH	HMC270 SPDT	DC - 8 GHz
11	SWITCH	HMC245 SP3T	DC - 3.5 GHz
12	SWITCH	HMC252 SP6T	DC - 3 GHz
13	OP-AMP	THS4031	100 MHz

Table 4.1: Required Components for Frequency Synthesizer Design

Obviously the specification are still not complete, but we have enough information to start designing the frequency synthesizer. One important thing that we still required is specification of Loop Filter. We are using active Loop filter whose specifications are :-

- Loop Bandwidth = 1MHz
- Phase Margin = 75^o.

4.2 Block Diagram

The block diagram advanced graphics model of the product, this model is very helpful in understanding the design concept. In first block Coaxial Resonator Oscillator-CRO CVCO55CC-3205-3317 is used to lock the VCO at 6400 MHz. Block diagram is shown in below figure 4.1

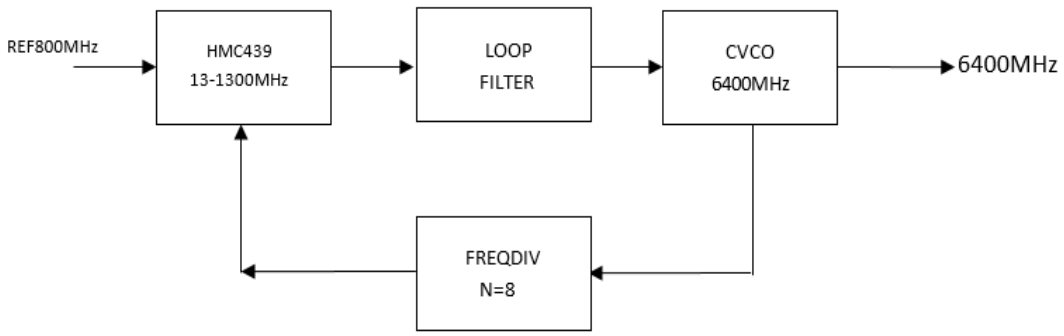


Figure 4.1: Single loop PLL
LOOP-1

The CVCO oscillator that used in the project ranges from 3205 to 3317 MHz.$\times$2 frequency multiplier is used at VCO output to increase the frequency range, then $\div$8 divder with 800MHz reference is used to lock the VCO in 6400MHz frequency.

The CVCO 6400 MHz oscillator that we used does not represent the most advanced technology, we can get better result with some other oscillators for example sapphire-cavity oscillator , this technology is thoroughly investigated in[26][27][28][29][30][31]. However it is sufficient for our design requirement.
The prototype of a triple offset loop synthesizer is shown in figure 4.2. The second offset loop is used to phase lock a Analog Devices VCO HMC1166 to a 6400MHz CVCO to achieve 200 MHz of synthesized tuning around 6 GHz while maintaining the phase noise of Coaxial Resonator oscillator. For better spurious performance DDS is used.
HMC1166 VCO is locked in frequency range 5900 to 6100 MHz, which is then used as a tunable reference for the third and the fourth offset loop. In the third offset loop it is act as reference to lock the Analog Devices VCO HMC431 at a frequency range 5500 - 6100 MHz and in the fourth offset loop it is act as a reference oscillator to lock the Analog Devices VCO HMC466 at frequency range 6000 - 6700 MHz.

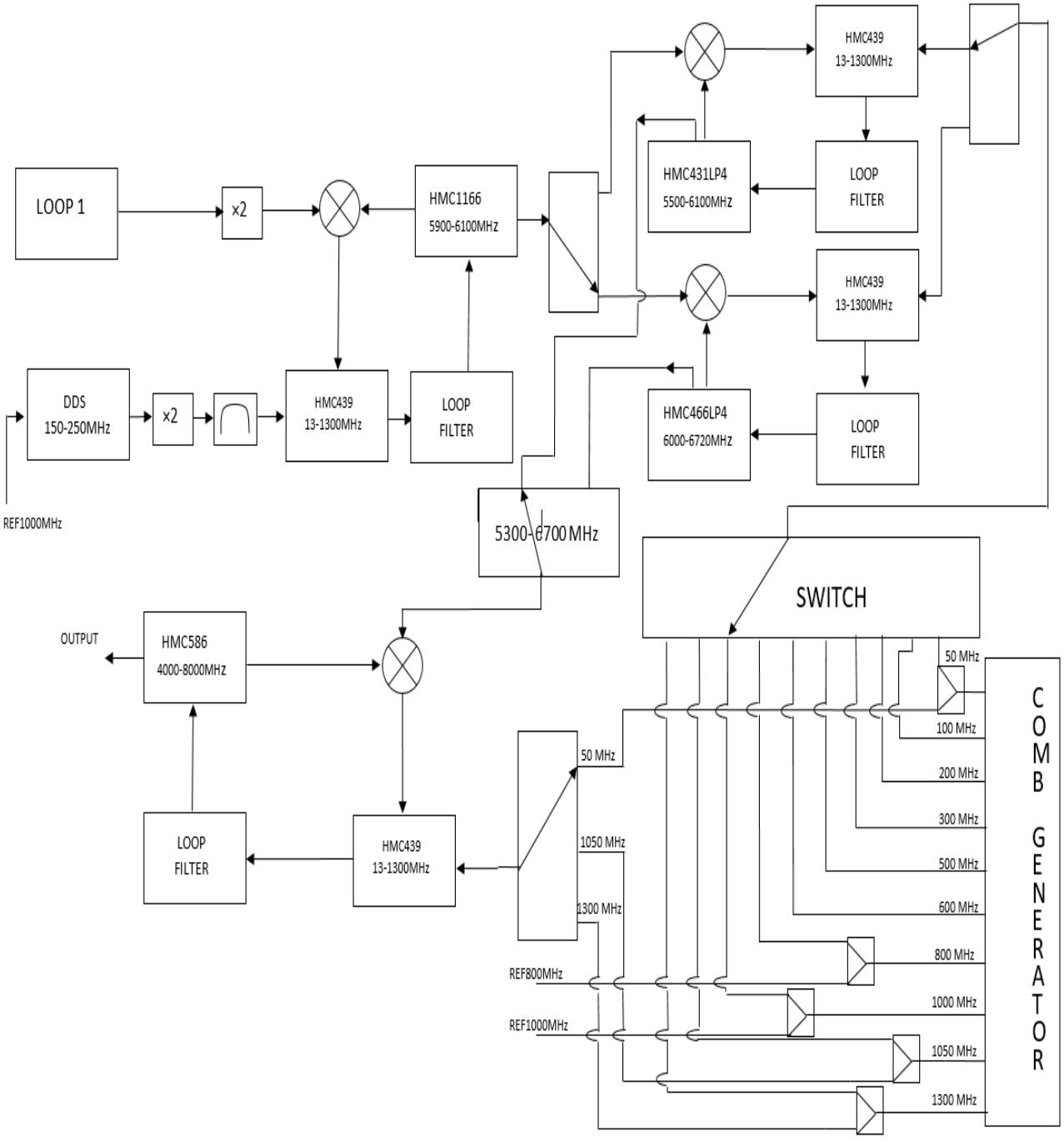


Figure 4.2: Block Diagram of Complete Circuit

The two offset VCOs used in loop 3 and loop 4 is of different frequency range and are used to increase the range of frequency. From loop 3 and loop 4 we get a frequency range of 5300 - 6700 MHz. To additionally lower the phase noise doubers are used. Range of frequencies obtained at the output of offset loop 3 and loop 4 are shown in below table 4.2.

TABLE 2

FREQUENCY AT DIFFERENT LOCATIONS IN CIRCUIT

S.No.	**VCO-2 after locking(MHz)**	**IF/REF frequency (MHz)**	**VCO-3 and VCO-4 (MHz)**
1	5900 - 6100	-600/600	5300 - 5500
2	5900 - 6100	-500/500	5400 - 5600
3	5900 - 6100	-400/400	5500 - 5700
4	5900 - 6100	-300/300	5600 - 5800
5	5900 - 6100	-200/200	5700 - 5900
6	5900 - 6100	-100/100	5800 - 6000
7	5900 - 6100	-50/50	5850 - 6050
8	5900 - 6100	100/100	6000 - 6200
9	5900 - 6100	200/200	6100 - 6300
10	5900 - 6100	300/300	6200 - 6400
11	5900 - 6100	400/400	6300 - 6500
12	5900 - 6100	500/500	6400 - 6600
13	5900 - 6100	600/600	6500 - 6700

Table 4.2: Frequency at Several Locations in Circuit

The fixed reference signals of 50, 100, 200, 300, 500, 600, 800, 1000, 1050 and 1300 MHz are all derived from an ultra-low noise 100 MHz Oven Controlled Crystal Oscillator which is also used to phase-lock the Coaxial Resonator Oscillator for better performance.
Since the aim of the project is to achieve an octave tuning range in microwave region. To do that the fifth offset loop of the circuit uses the third and fourth loop synthesizers as a tunable offset reference to lock the Analog Devices VCO HMC586 at 4 to 8 GHz. The frequency range that is obtained in the last loop is shown in table 4.3

TABLE 3

FREQUENCY RANGE IN THE LAST LOOP

S.No.	**VCO-2 & VCO-3 after locking(MHz)**	**IF/REF frequency (MHz)**	**OUTPUT (MHz)**
1	5300 - 6700	-1300/1300	4000 - 5400
2	6050 - 6650	-1050/1050	5000 - 5600
3	5050 - 6050	-50/50	5000 - 6000
4	5450 - 5950	1050/1050	6500 - 7000
5	5700 - 6700	1300/1300	7000 - 8000

Table 4.3: Frequency Range Obtained in Last Loop

From above figures and tables we get the basic idea of how the whole circuit should work and how to obtain the required octave bandwidth frequency, which is this project is 4GHz to 8GHz.

4.3 Simulation in ADS

Simulation of a PLL is possible in ADS. Loop filter synthesis by optimization, phase noise simulation, transisent response to see locked Vtune voltage are all can be done in ADS. However spurious signal is not possible to simulate in ADS [32][33][34].

4.3.1 Open and Closed loop simulation of CVCO55CC

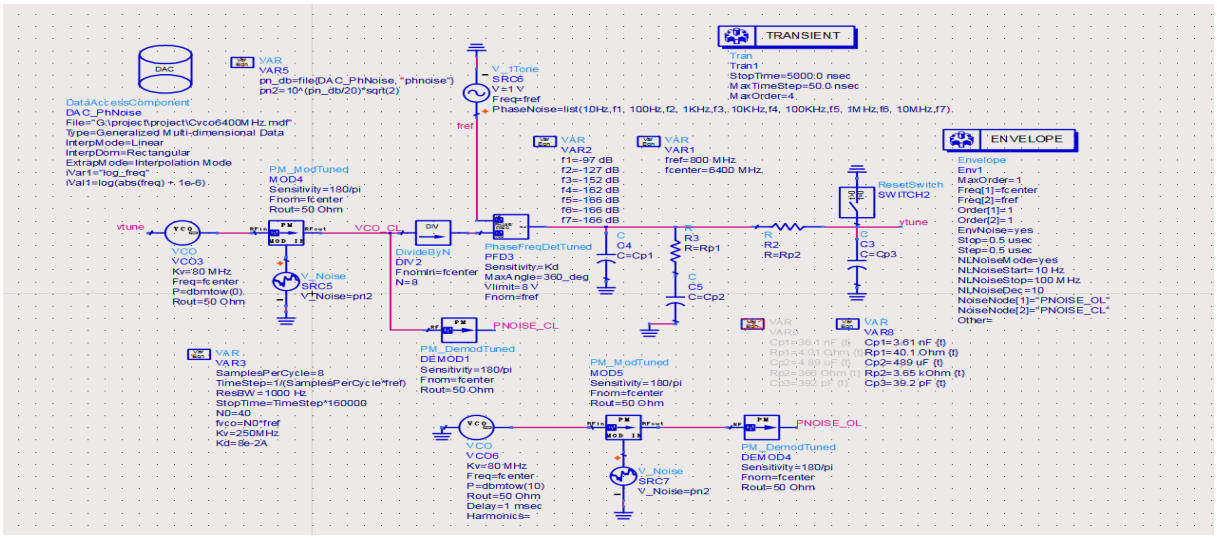


Figure 4.3: Open and Closed Loop Schematic in ADS

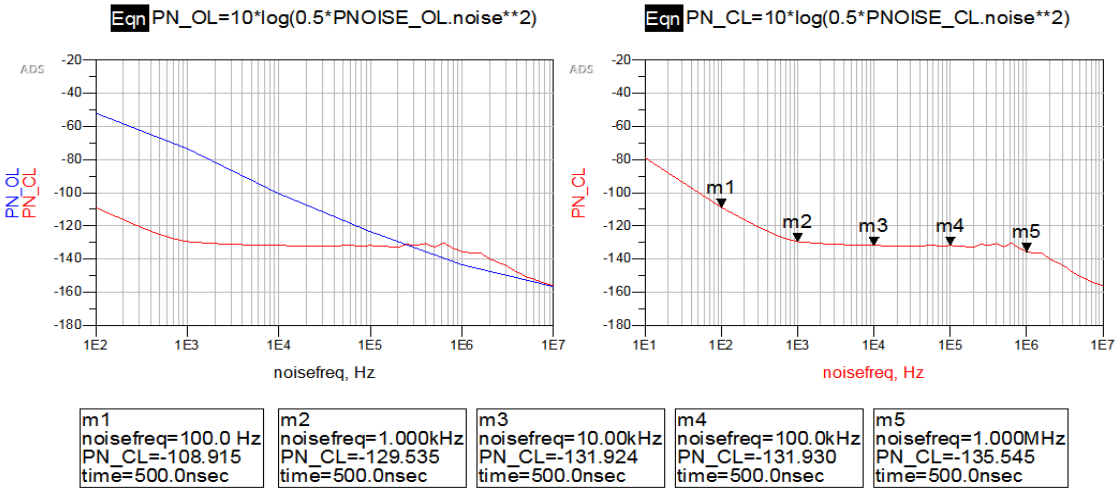


Figure 4.4: Simulated result in ADS

4.3.2 Lock-in time

Lock-in time is the time in which PLL reaches the steady state where both reference signal and VCO output signal will be in phase. It can be also said that PLL is locked at that particular voltage.

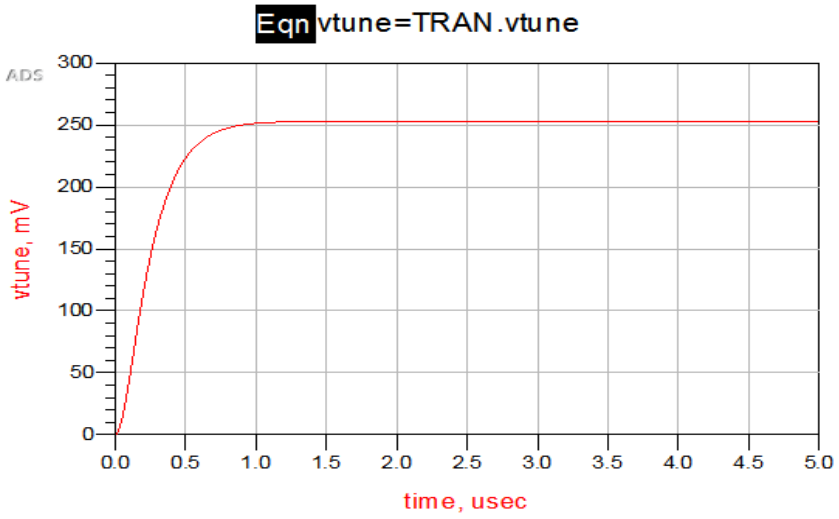


Figure 4.5: Data display window for lock-in time simulation.

CVCO55CC 6400MHz			
S.No.	**Noise Frequency(Hz)**	**OpenLoop Phase Noise**	**ClosedLoop Phase Noise**
1	10	-28.98	-79
2	100	-51.98	-108.915
3	1K	-73.4522	-129.535
4	10K	-100.5894	-131.924
5	100K	-123.5177	-131.930
6	1M	-143.5177	-135.545
7	10M	-156.642	-156.195
8	100M	-166	-166

Table 4.4: Phase Noise of CVCO 6400MHz

4.3.3 Locking HMC1166 with CVCO

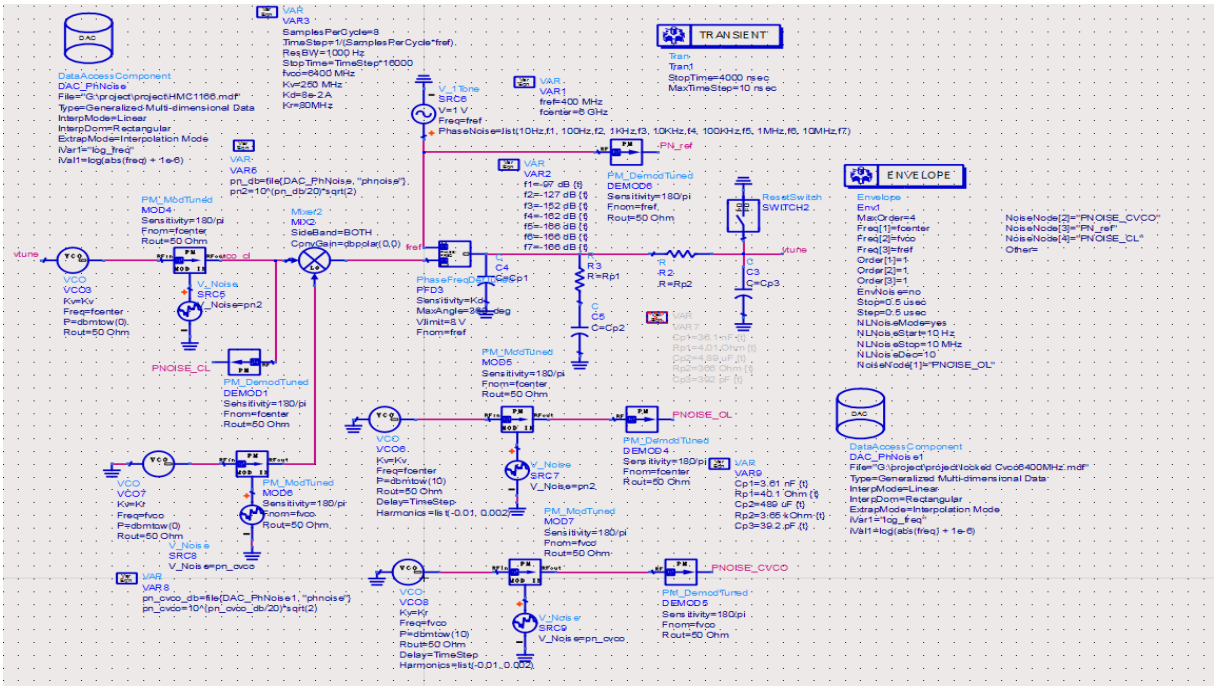


Figure 4.6: DDS of HMC1166 with CVCO

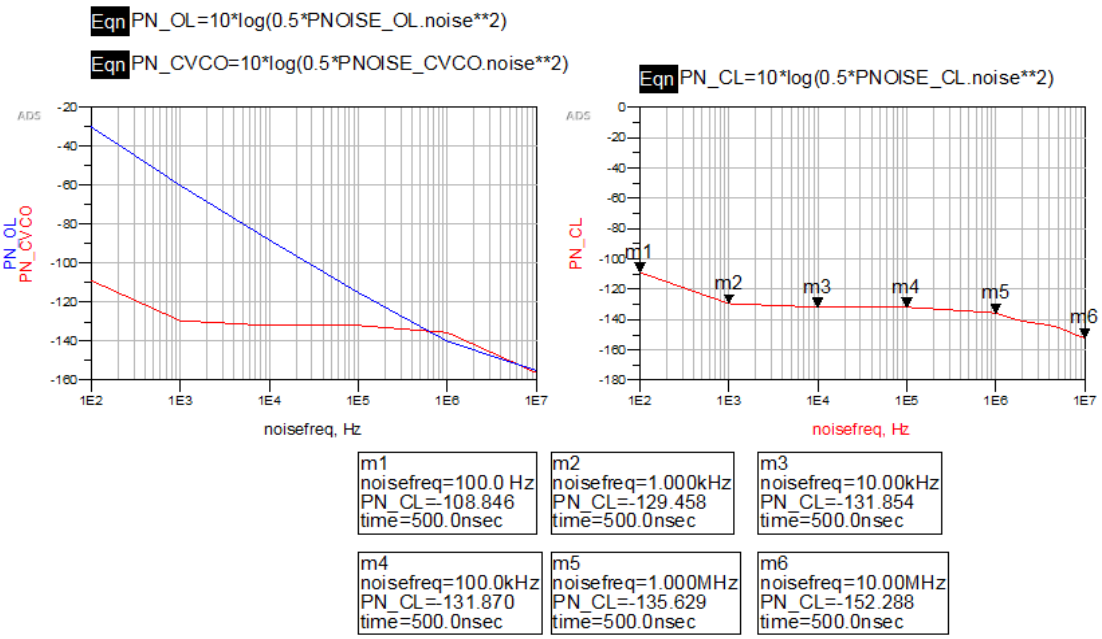


Figure 4.7: Locking HMC1166 with CVCO

4.3.4 Locking HMC431 for 5300MHz

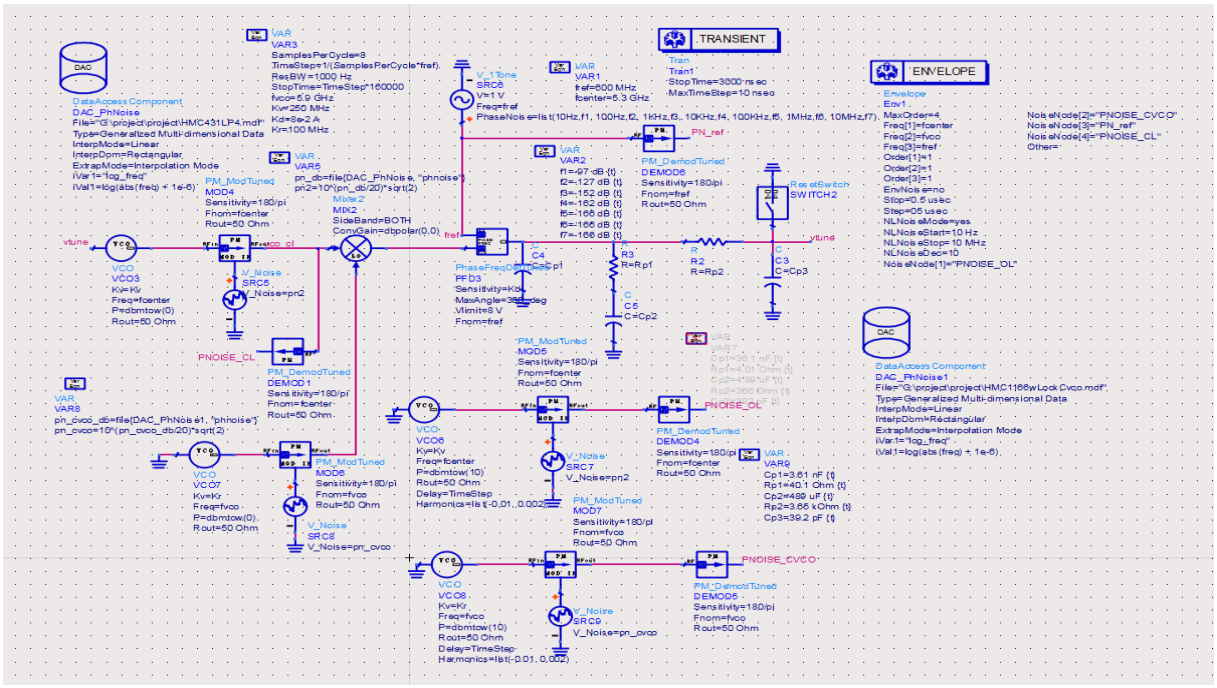


Figure 4.8: Locking HMC431 for 5300MHz

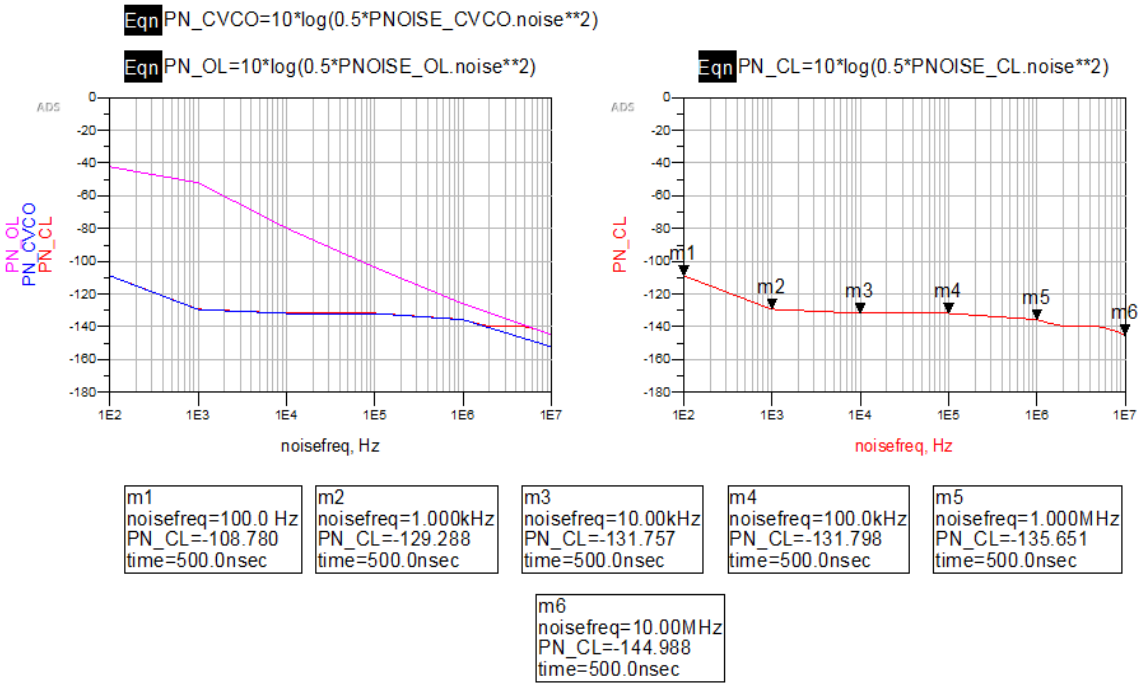


Figure 4.9: DDS of figure 4.8

4.3.5 Locking HMC431 for 5800MHz

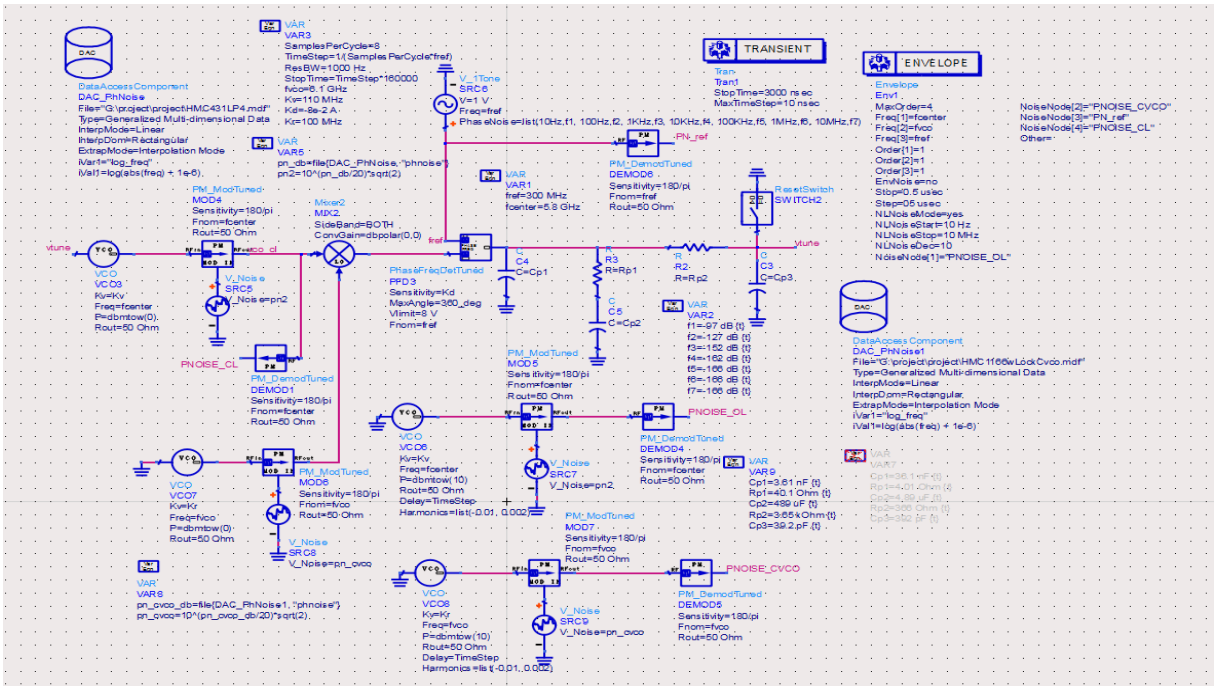


Figure 4.10: Locking HMC431 for 5800MHz

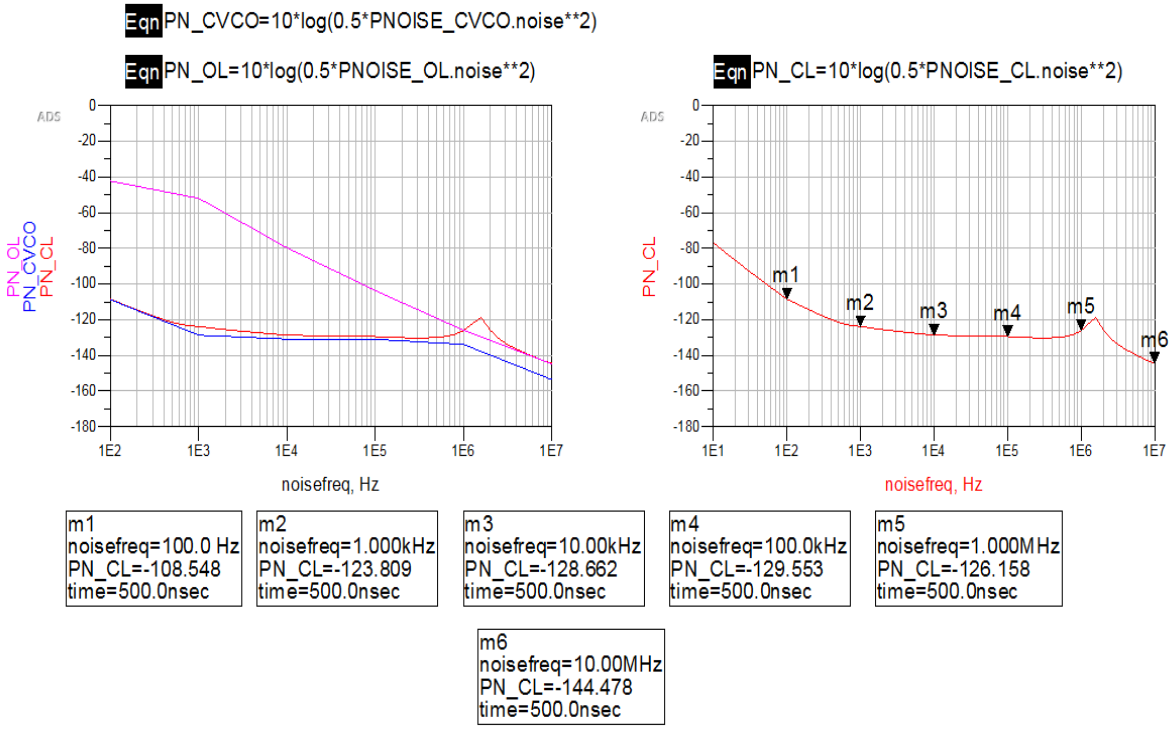


Figure 4.11: DDS of figure 4.10

4.3.6 Locking HMC466 for 6300MHz

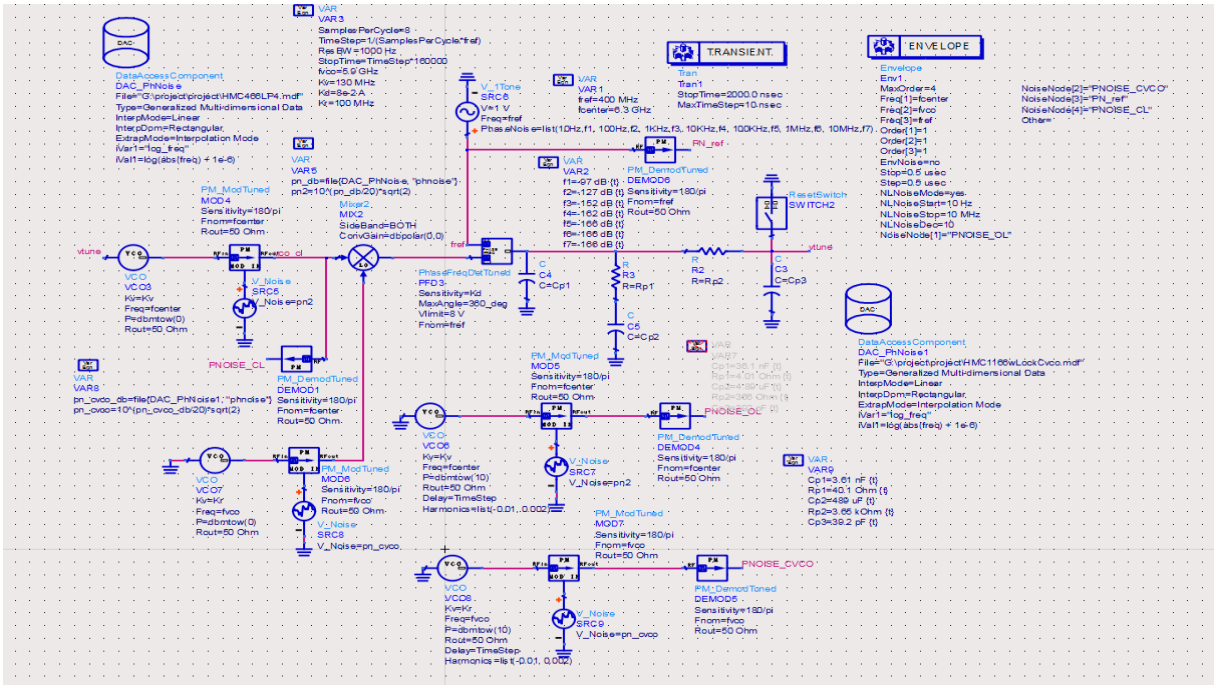


Figure 4.12: Locking HMC466 for 6300MHz

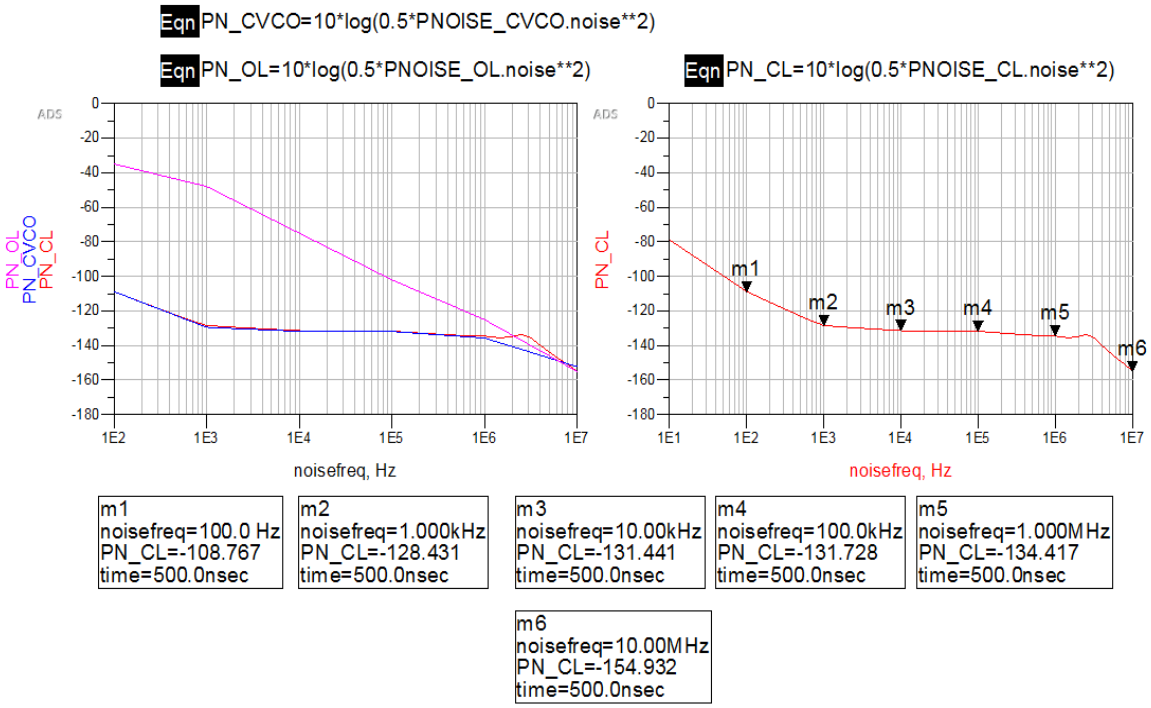


Figure 4.13: DDS of figure 4.12

4.3.7 Locking HMC466 for 6700MHz

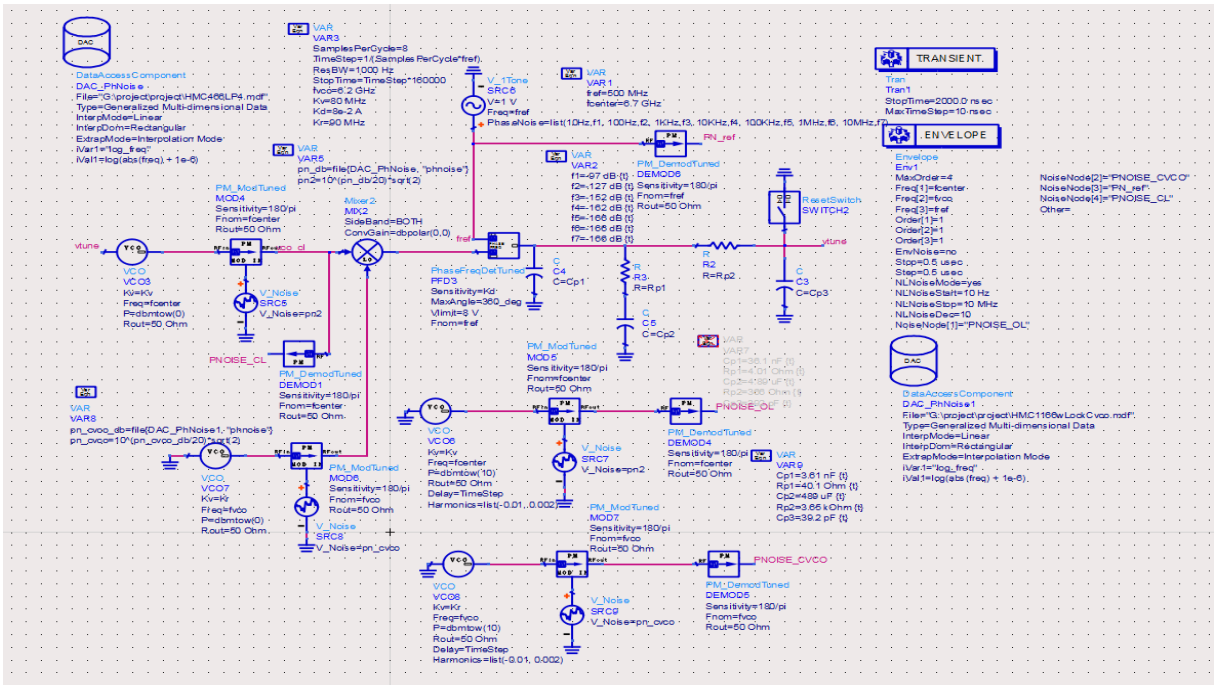


Figure 4.14: Locking HMC466 for 6700MHz

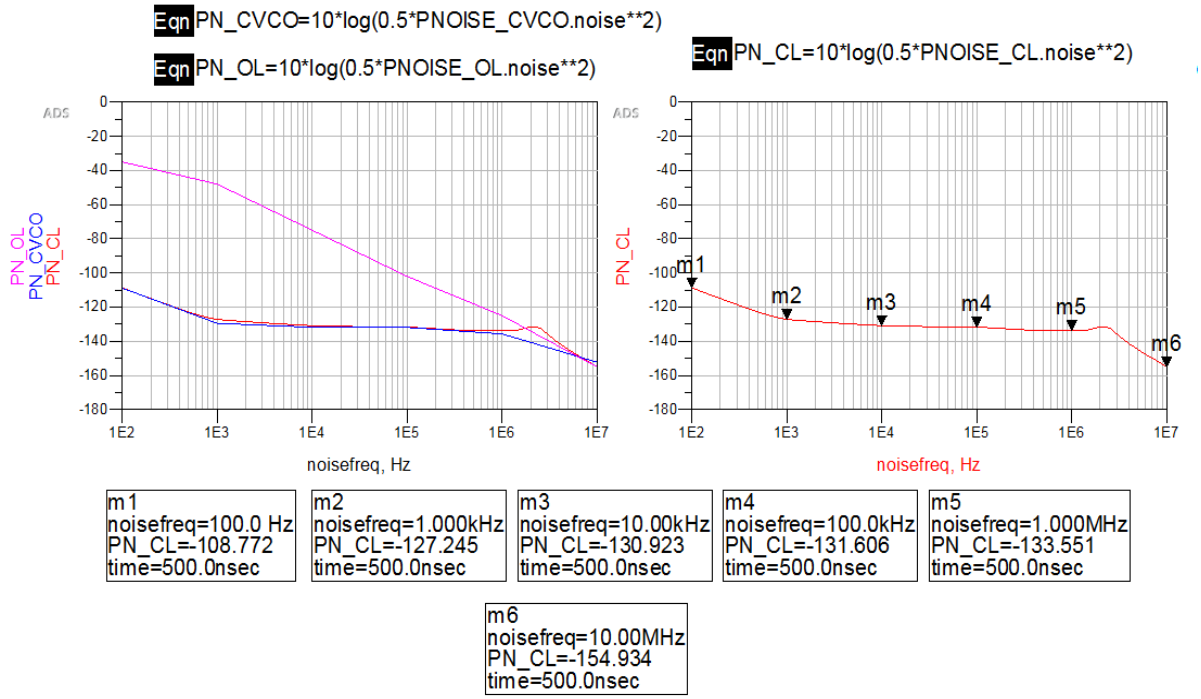


Figure 4.15: DDS of figure 4.14

4.3.8 Locking HMC486 for desired 4000MHz

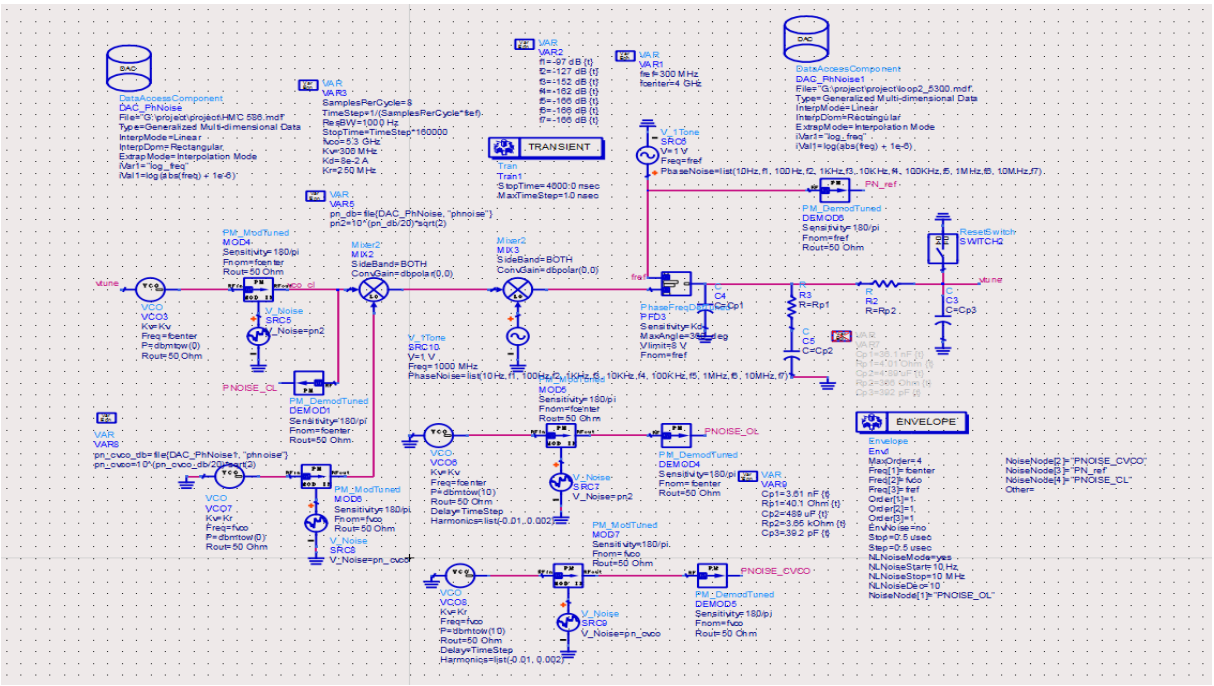


Figure 4.16: Locking HMC486 for 4000MHz

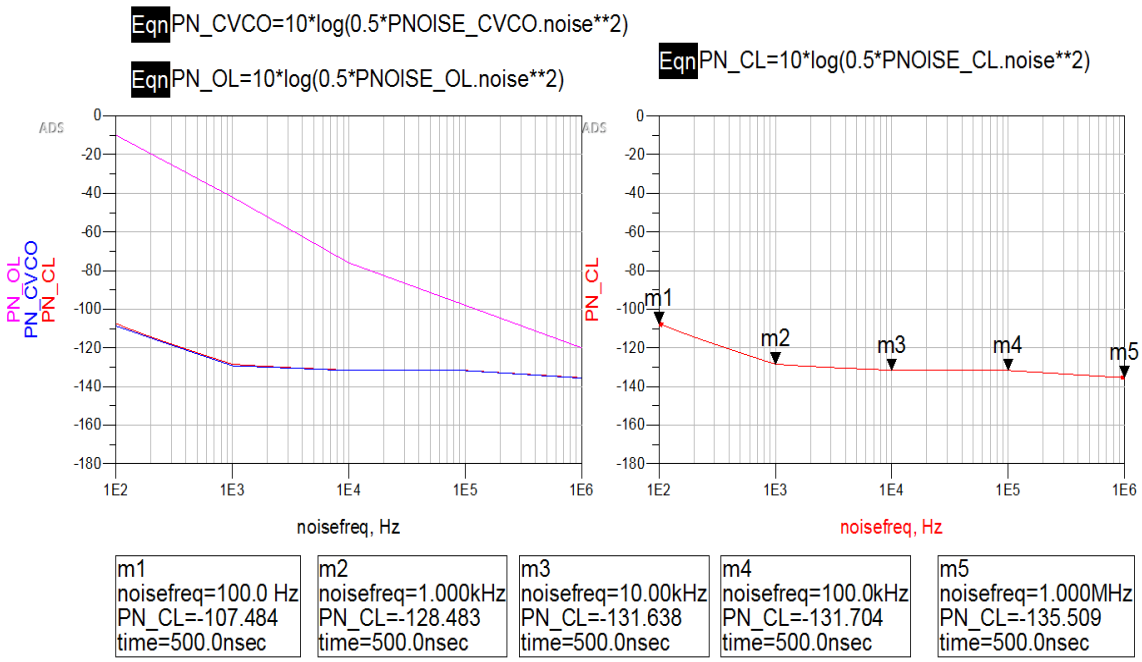


Figure 4.17: DDS of figure 4.16

4.3.9 Locking HMC486 for desired 8000MHz

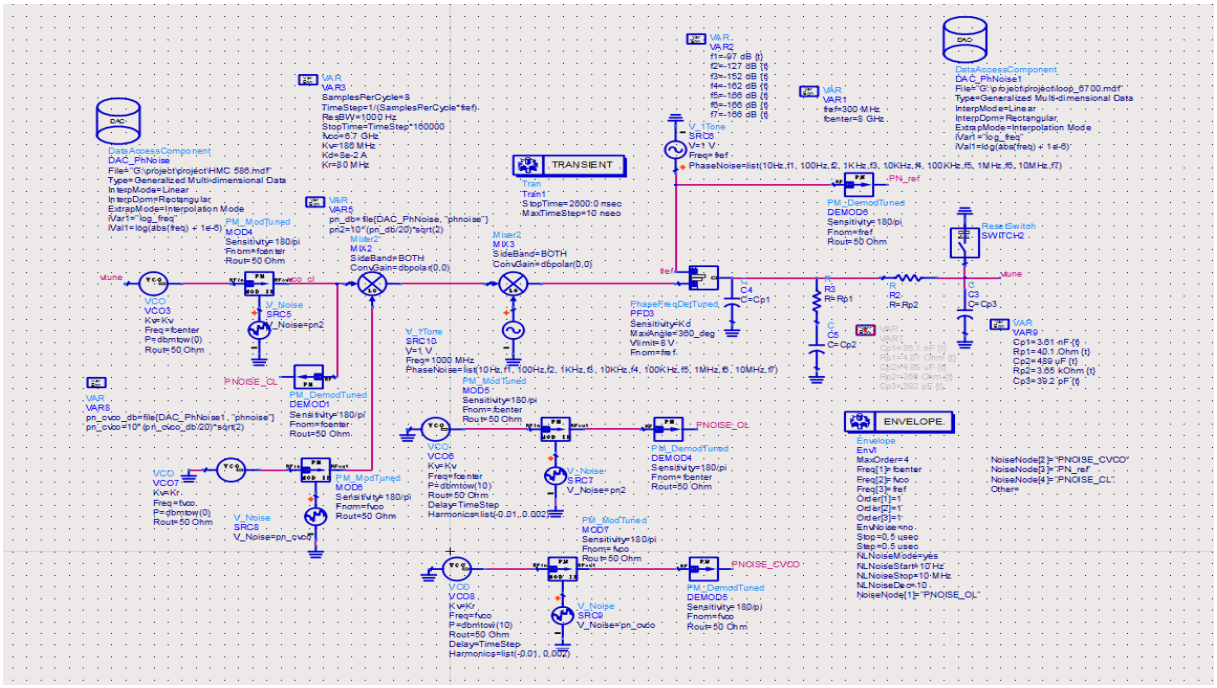


Figure 4.18: Locking HMC486 for 8000MHz

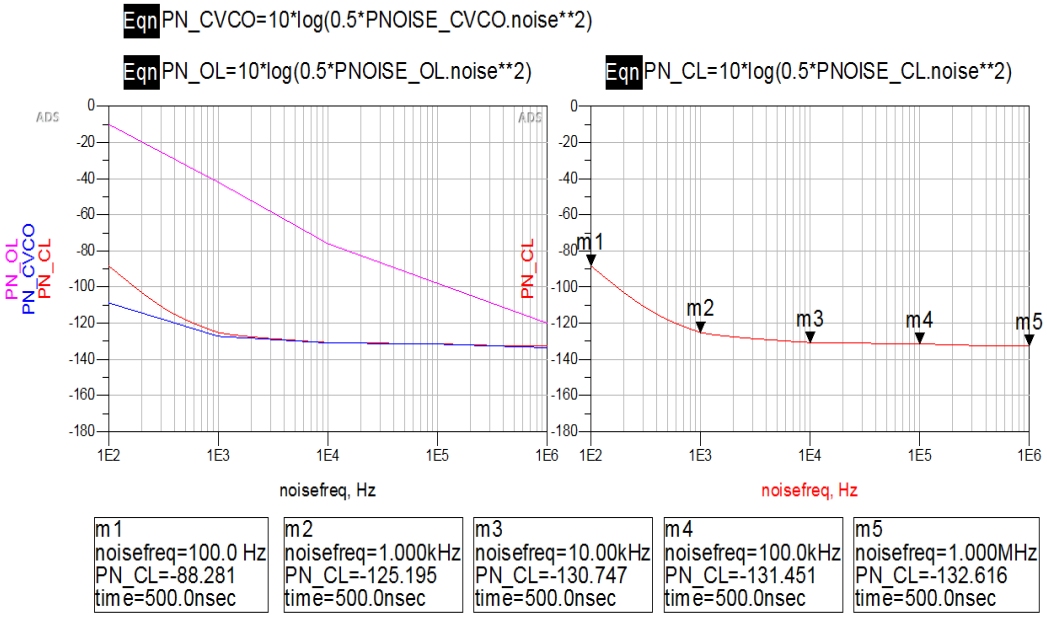


Figure 4.19: DDS of figure 4.18

Phase Noise Performance at 4 and 8 GHz Centre Frequency

S.No.	Offset Frequency(Hz)	Phase Noise at 4GHz Output	Phase Noise at 8GHz Output
1	100	-107.484	-88.281
2	1K	-128.483	-125.195
3	10K	-131.638	-130.747
4	100K	-131.704	-131.451
5	1M	-135.509	-132.616
6	10M	-155	-155

Table 4.5: Phase Noise Performance

The above result is when there is no vibration.

Next we are going to simulate the same under vibration condition. Vibration which degrade the crystal oscillator phase noise by 20dB.

4.4 Simulation in ADS under vibration(20dB)

Vibration condition affects the reference oscillator and degrade its phase noise which in turn affects the overall performance of the frequency synthesizer. Simulation of all under 20dB phase noise degradation are provided below.

4.4.1 Open and Closed loop simulation of CVCO55CC under 20dB phase noise degradation

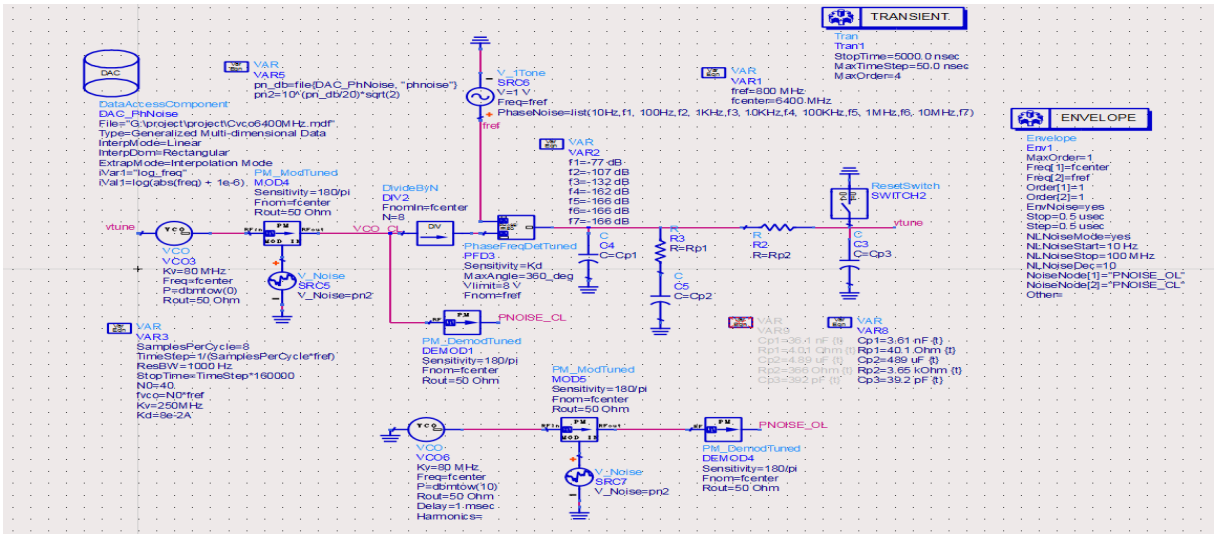


Figure 4.20: Open and Closed Loop Schematic in ADS under 20dB phase noise degradation

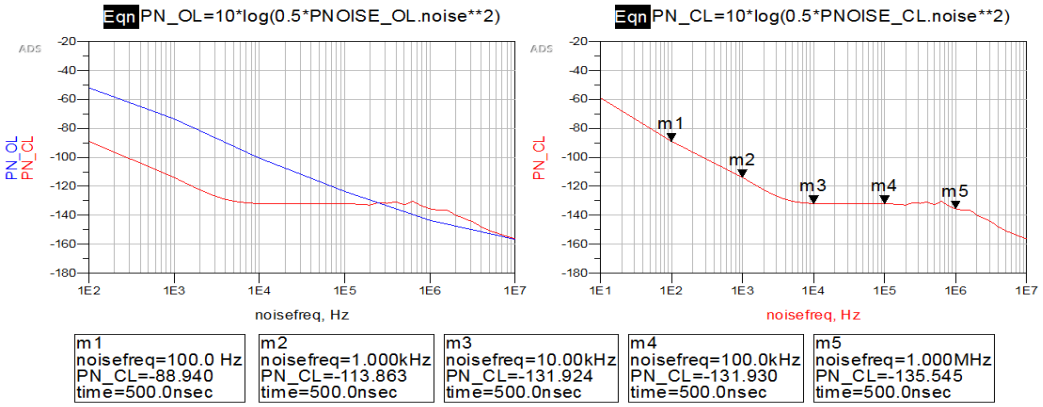


Figure 4.21: Simulated result in ADS under 20dB phase noise degradation

4.4.2 Locking HMC1166 with CVCO

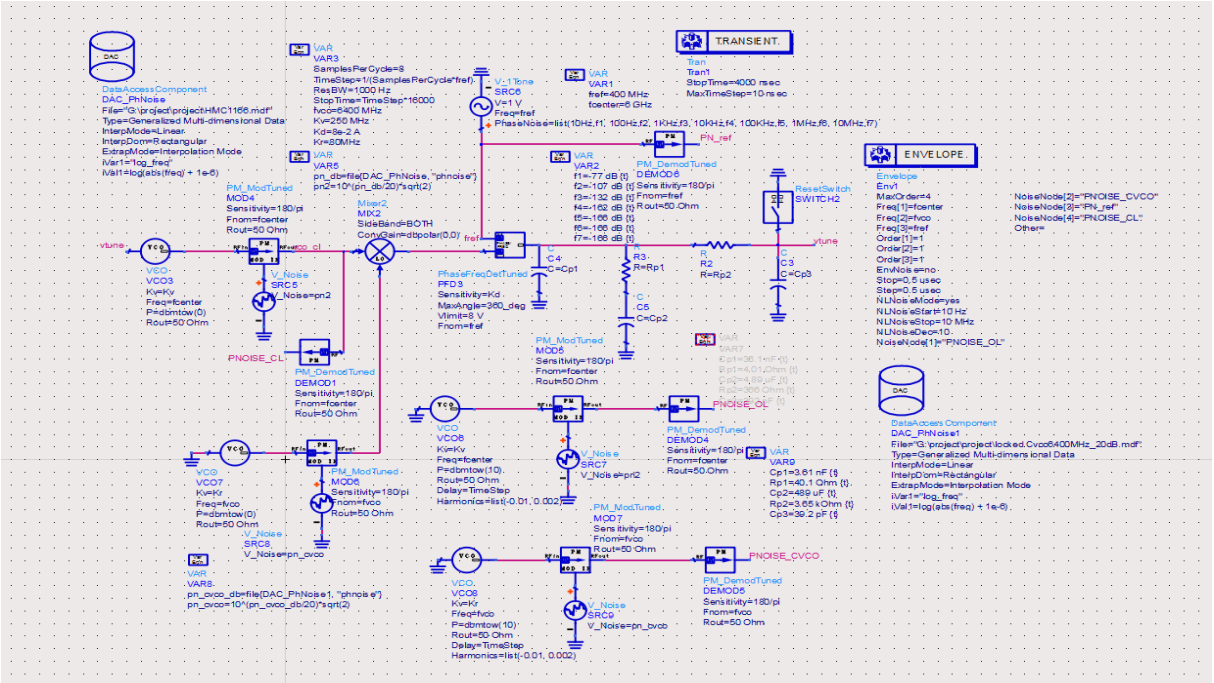


Figure 4.22: Locking HMC1166 with CVCO under 20dB phase noise degradation

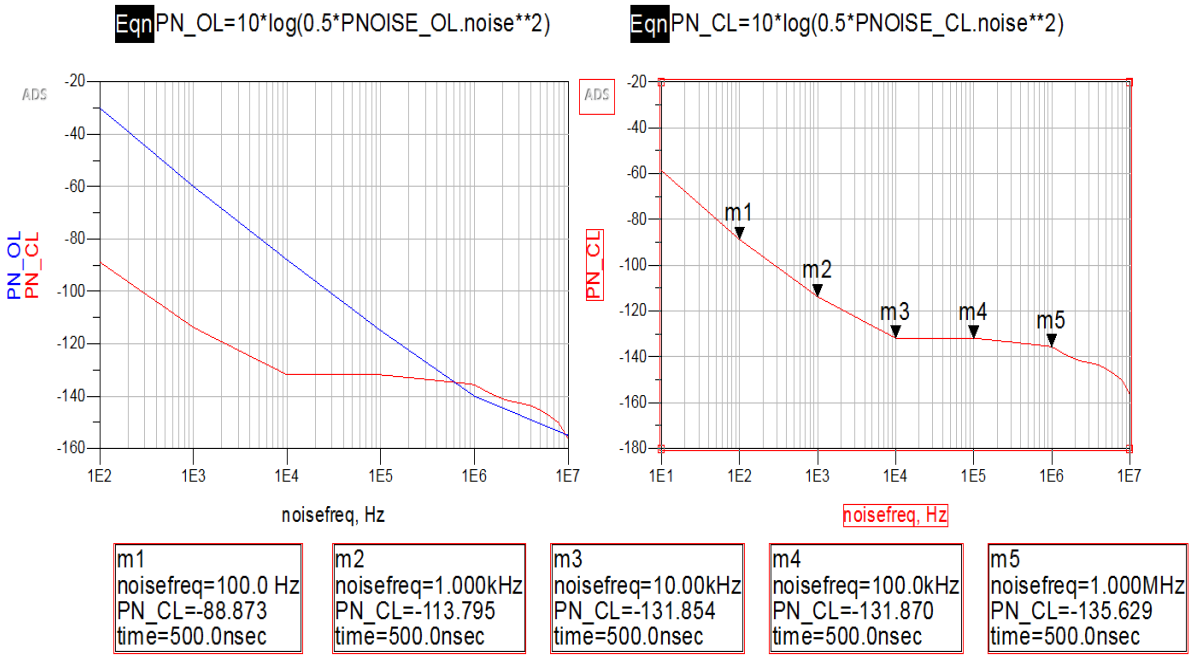


Figure 4.23: DDS of figure 4.22

4.4.3 Locking HMC431 for 5300MHz

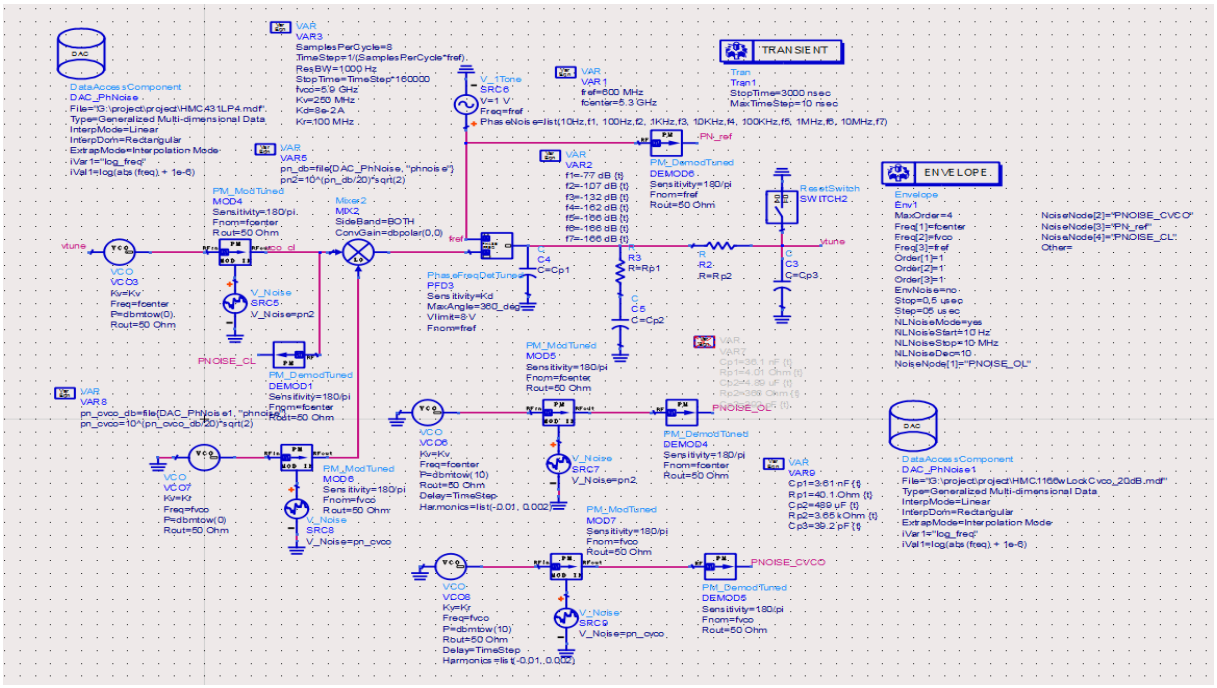


Figure 4.24: Locking HMC431 for 5300MHz under 20dB phase noise degradation

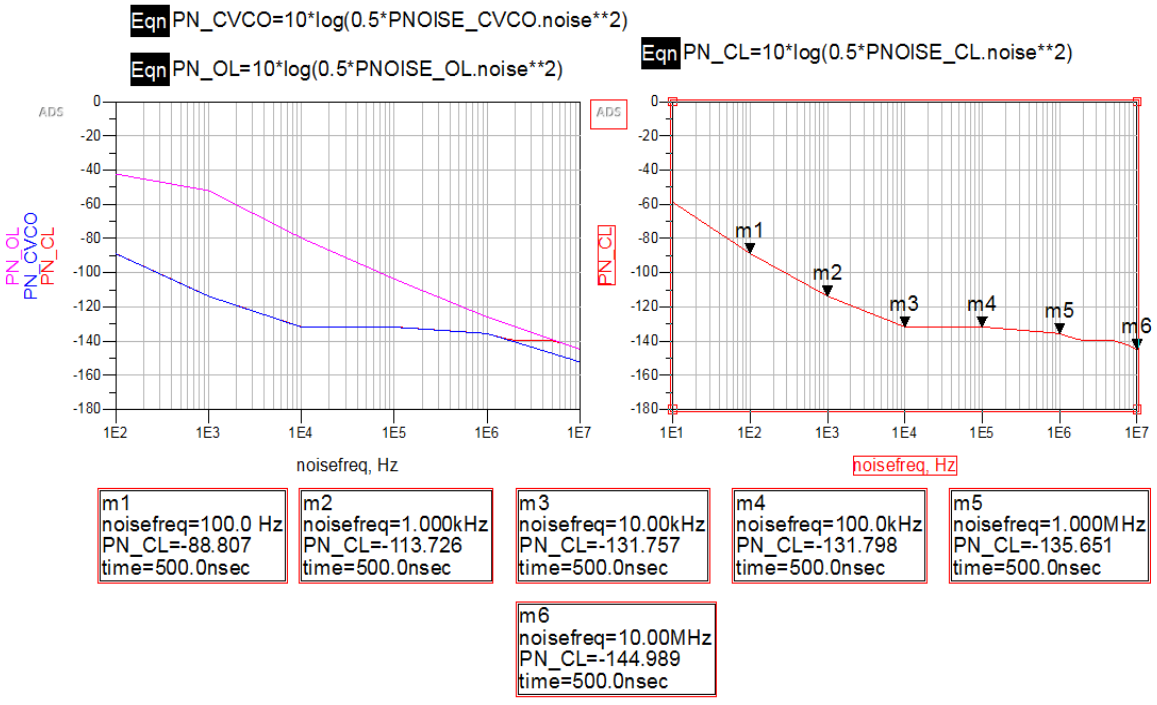


Figure 4.25: DDS of figure 4.24

4.4.4 Locking HMC431 for 5800MHz

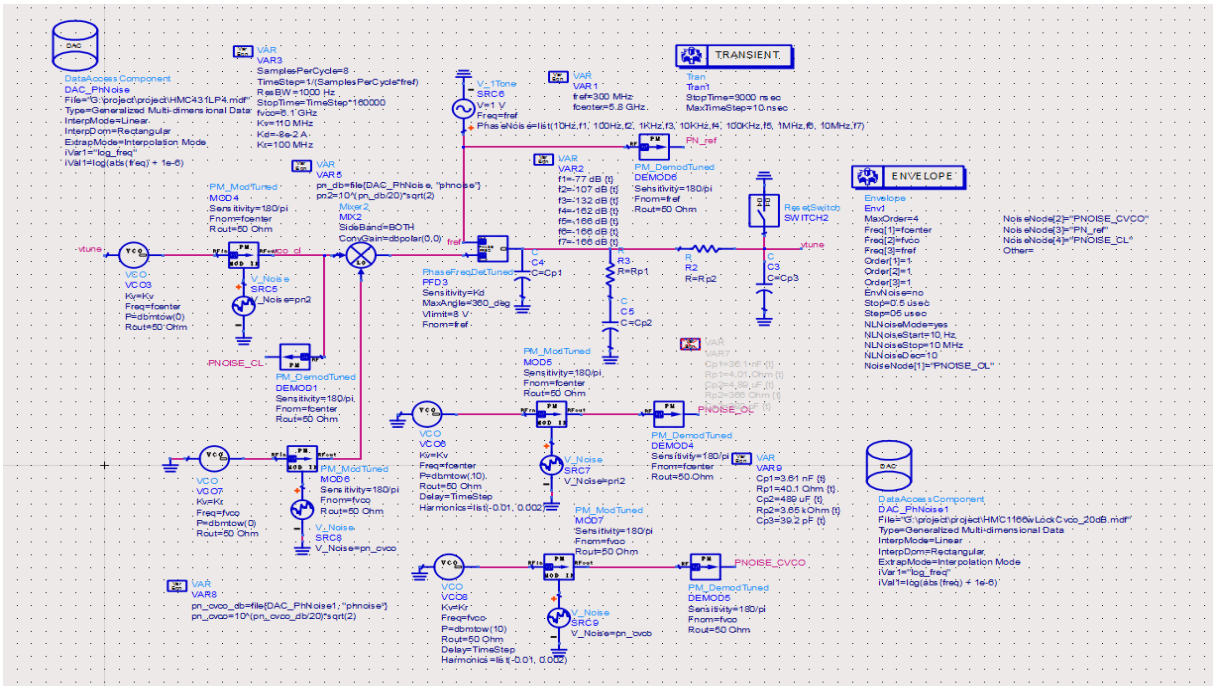


Figure 4.26: Locking HMC431 for 5800MHz under 20dB phase noise degradation

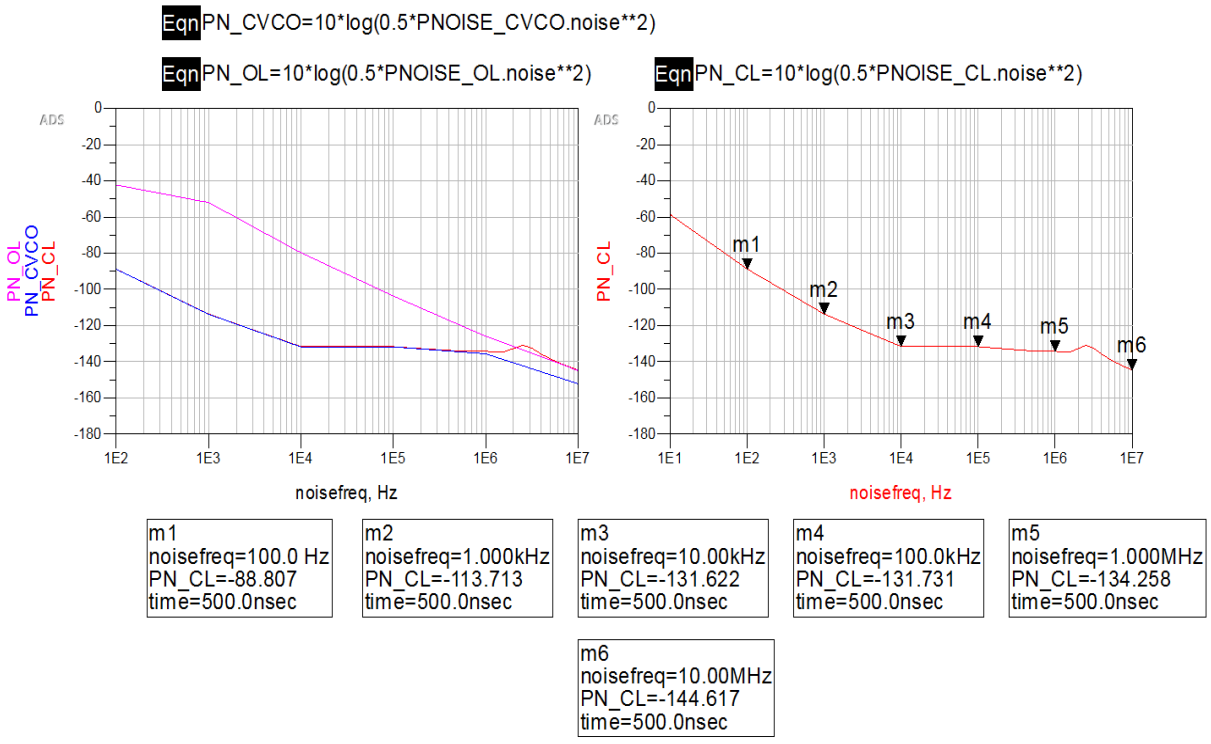


Figure 4.27: DDS of figure 4.26

4.4.5 Locking HMC466 for 6300MHz

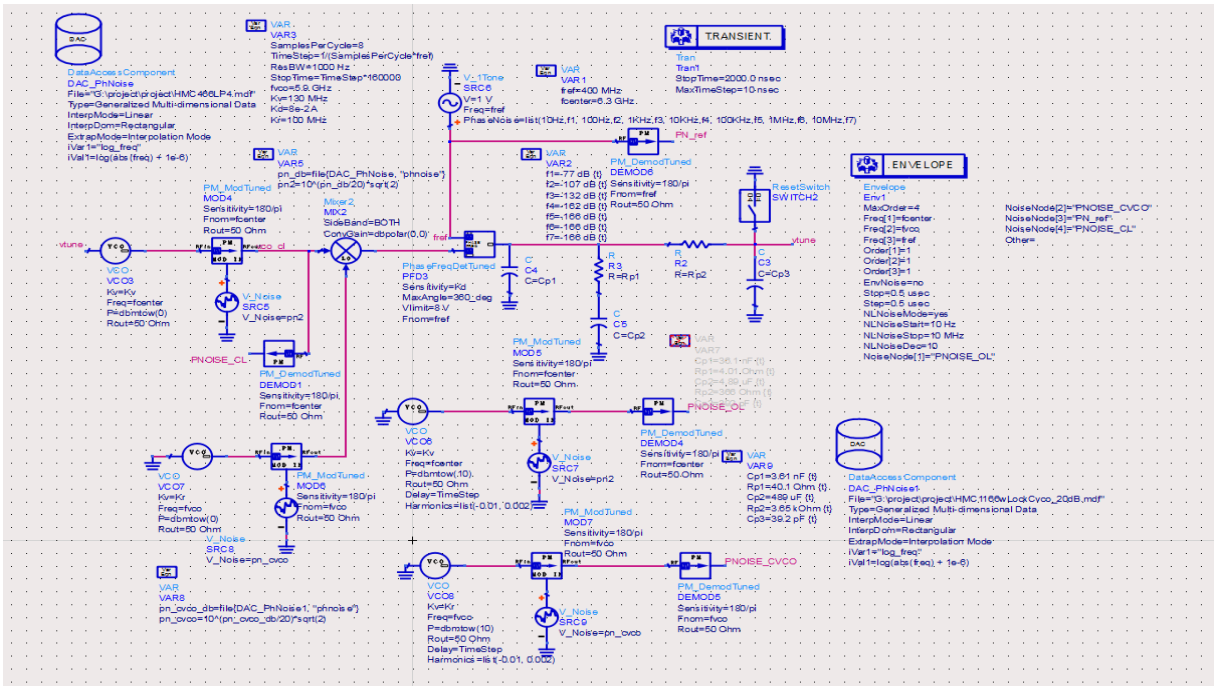


Figure 4.28: Locking HMC466 for 6300MHz under 20dB phase noise degradation

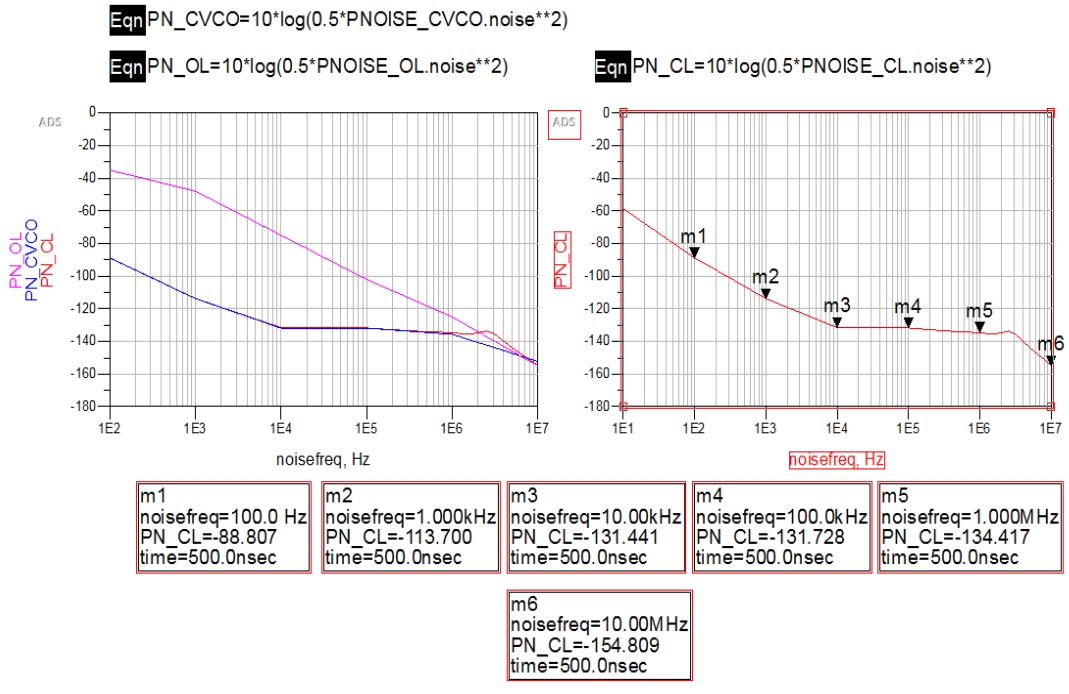


Figure 4.29: DDS of figure 4.28

4.4.6 Locking HMC466 for 6700MHz

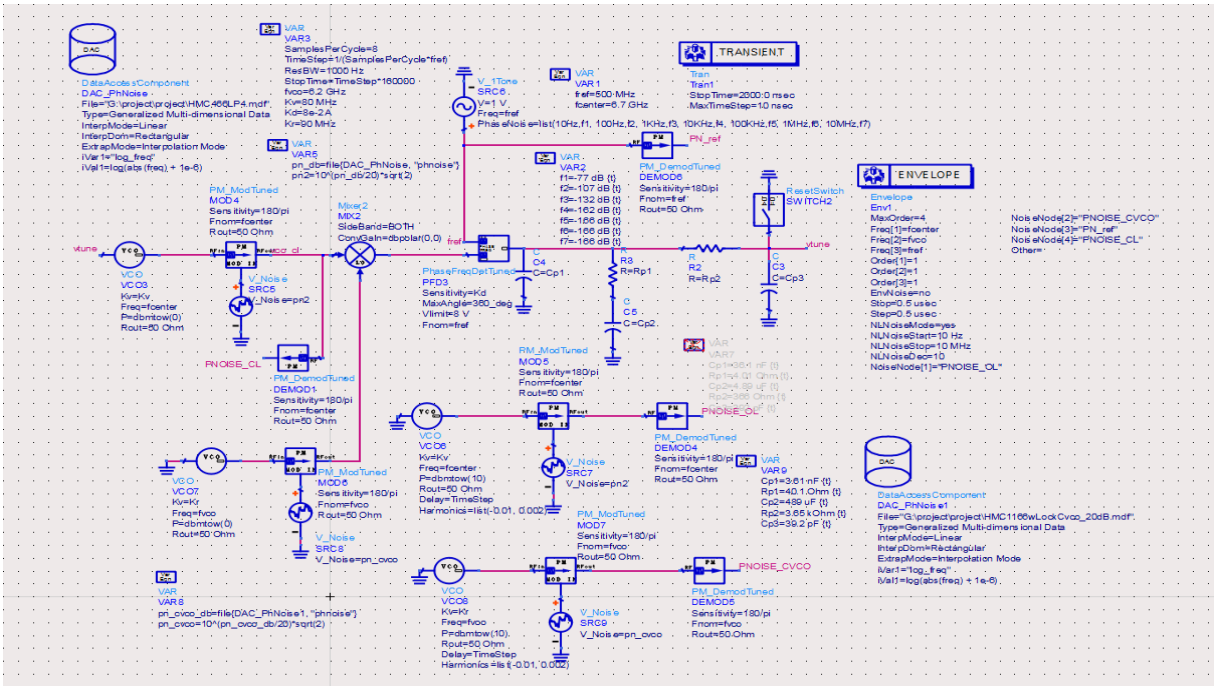


Figure 4.30: Locking HMC466 for 6700MHz under 20dB phase noise degradation

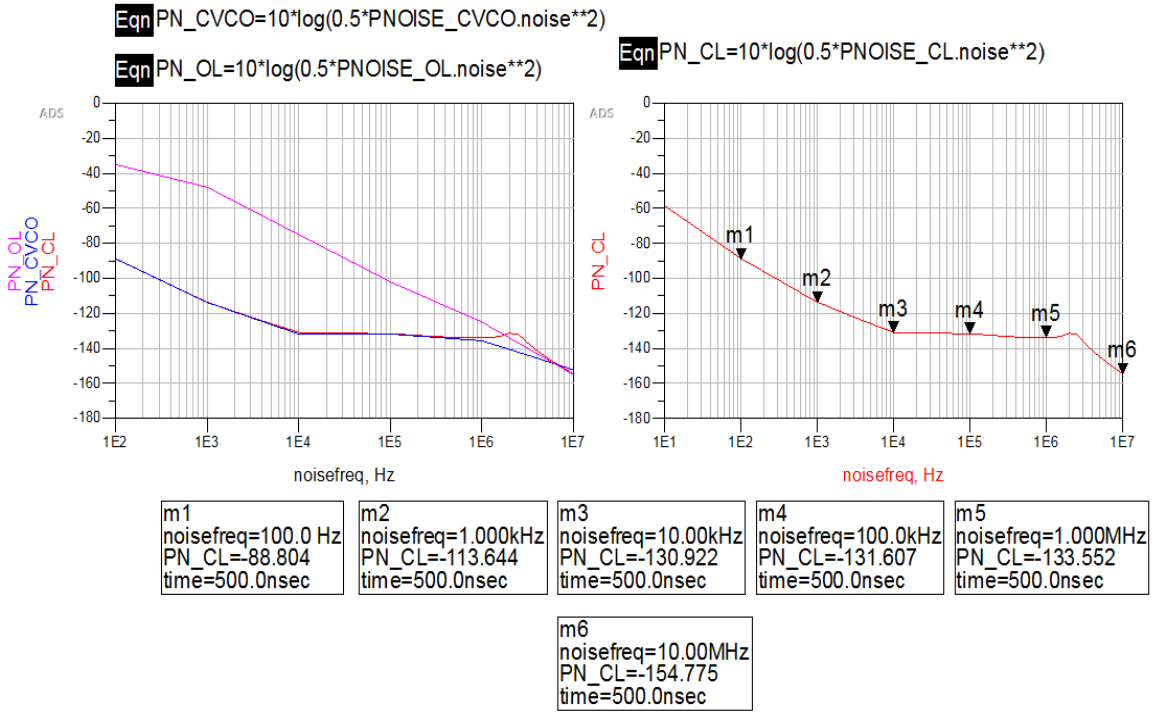


Figure 4.31: DDS of figure 4.30

4.4.7 Locking HMC486 for desired 4000MHz

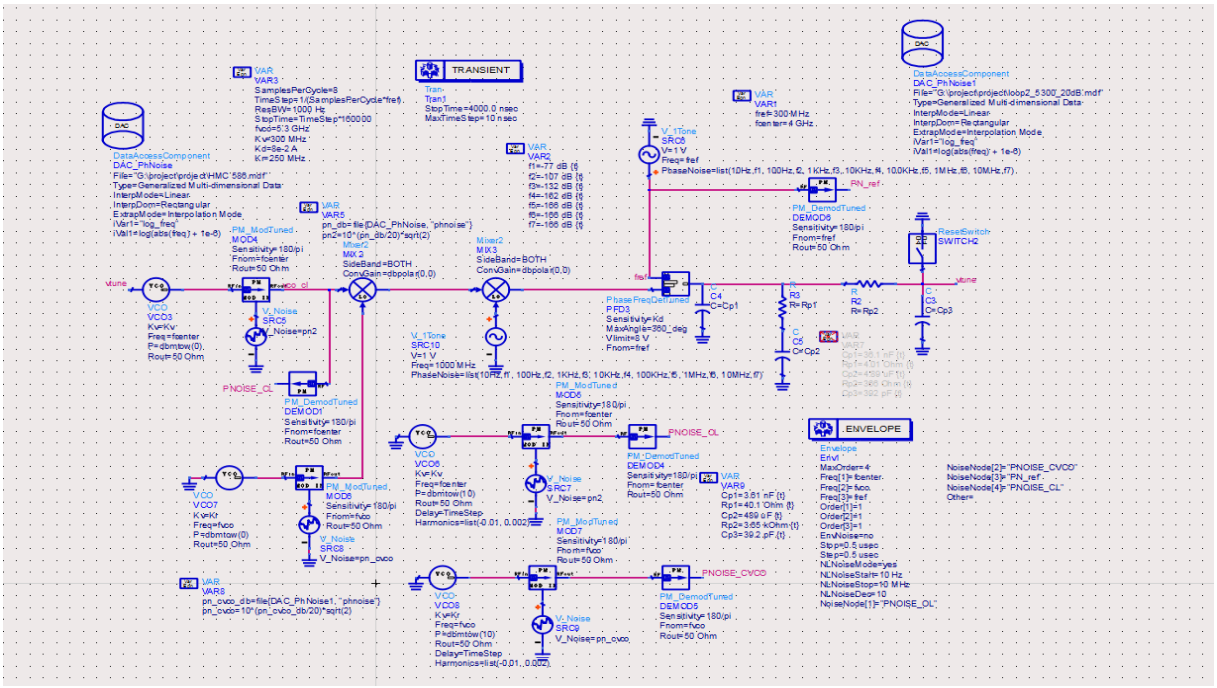


Figure 4.32: Locking HMC486 for 4000MHz under 20dB phase noise degradation

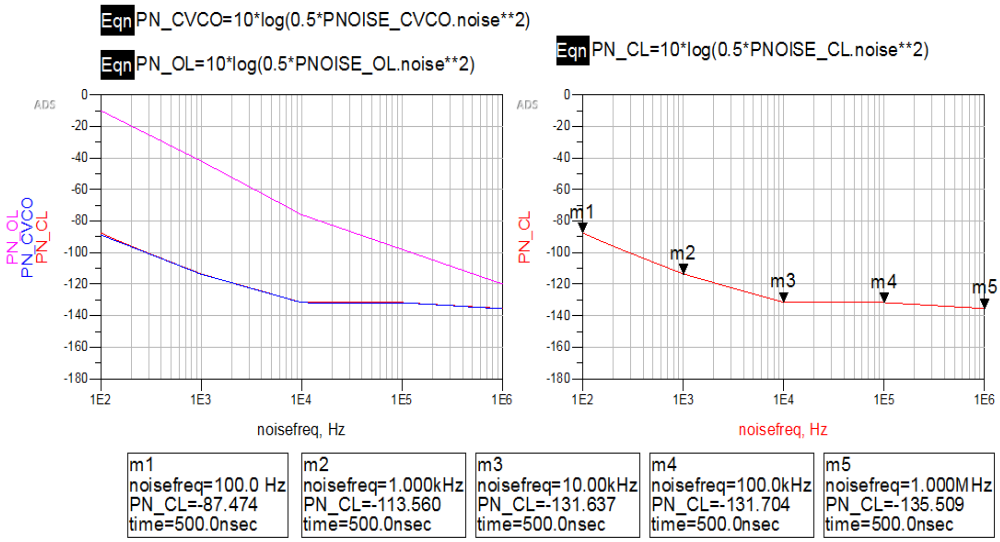


Figure 4.33: DDS of figure 4.32

4.4.8 Locking HMC486 for desired 8000MHz

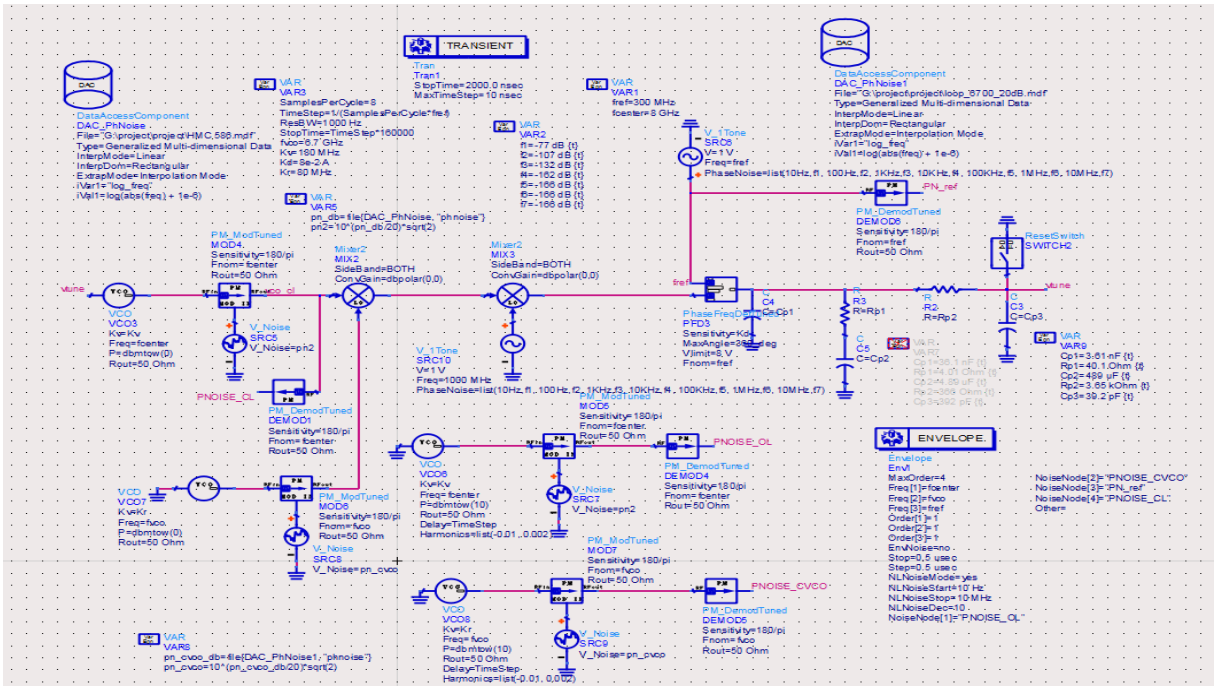


Figure 4.34: Locking HMC486 for 8000MHz under 20dB phase noise degradation

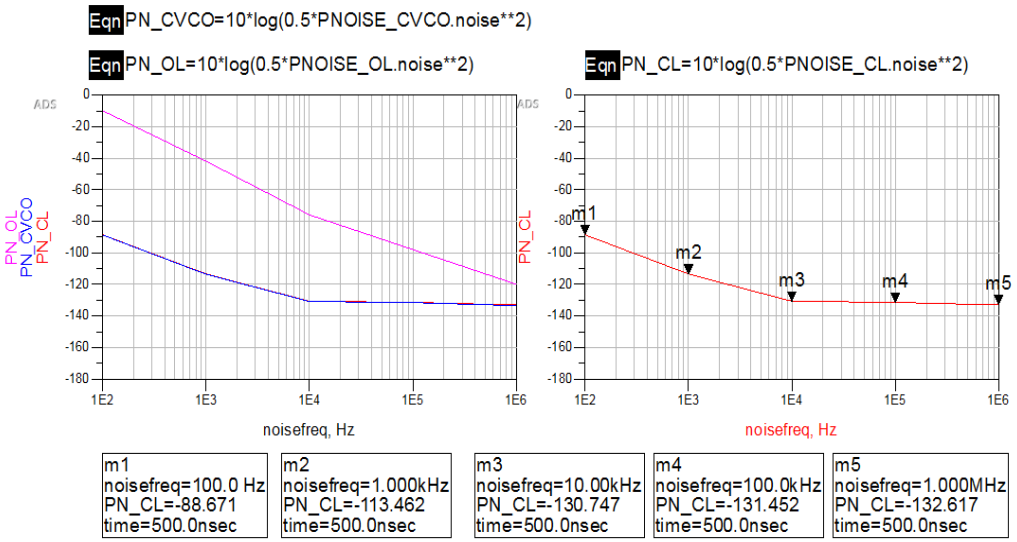


Figure 4.35: DDS of figure 4.34

4.4.9 Phase Noise Performance at 4 and 8 GHz centre frequency under 20dB phase noise degradation

S.No.	Offset Frequency(Hz)	Phase Noise at 4GHz Output	Phase Noise at 8GHz Output
1	100	-87.265	-88.373
2	1K	-113.558	-113.451
3	10K	-131.637	-130.746
4	100K	-131.704	-131.452
5	1M	-135.509	-132.616
6	10M	-155	-155

Table 4.6: Phase Noise Performance under 20dB phase noise degradation

The above result is under 20dB phase noise degradation.

Next we are going to simulate the same under 40dB phase noise degradation condition.
Vibration which degrade the crystal oscillator phase noise by 40dB.

4.5 Simulation in ADS under vibration(40dB)

Vibration condition affects the reference oscillator and degrade its phase noise which in turn affects the overall performance of the frequency synthesizer. Simulation of all under 20dB phase noise degradation are provided below.

4.5.1 Open and Closed loop simulation of CVCO55CC under 40dB phase noise degradation

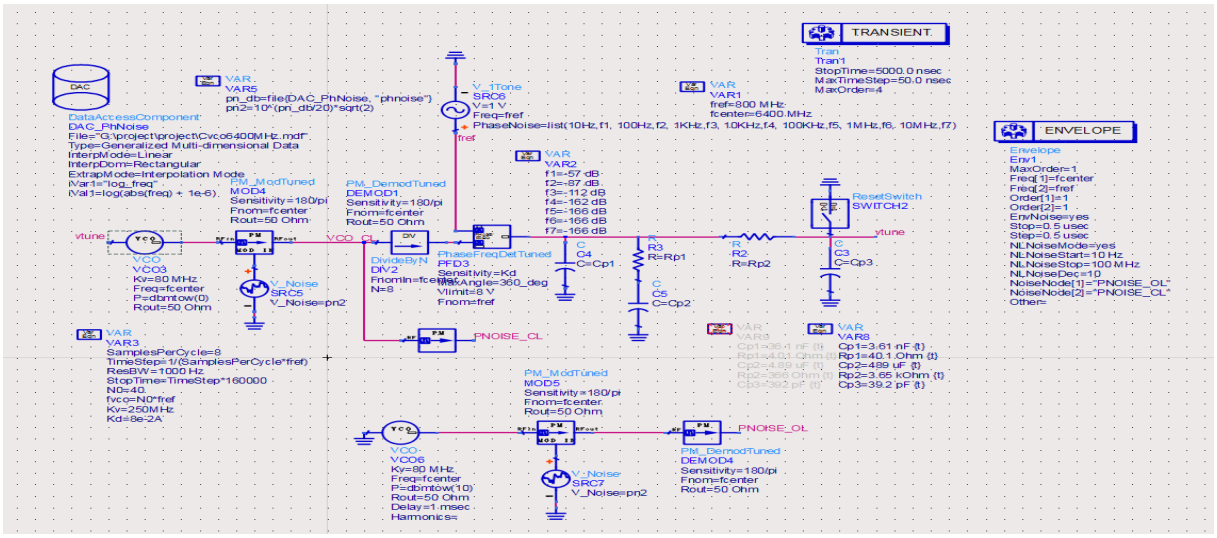


Figure 4.36: Open and Closed Loop Schematic in ADS under 40dB phase noise degradation

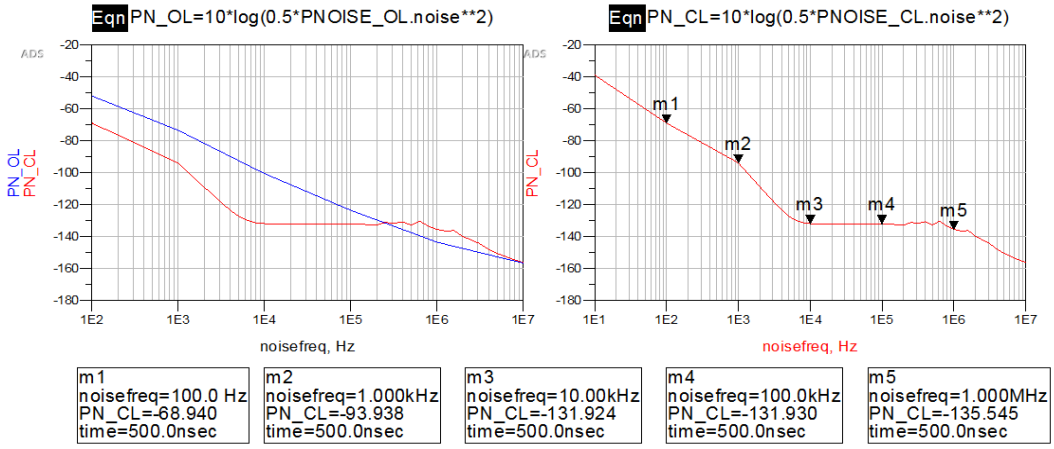


Figure 4.37: Simulated result in ADS under 40dB phase noise degradation

4.5.2 Locking HMC1166 with CVCO

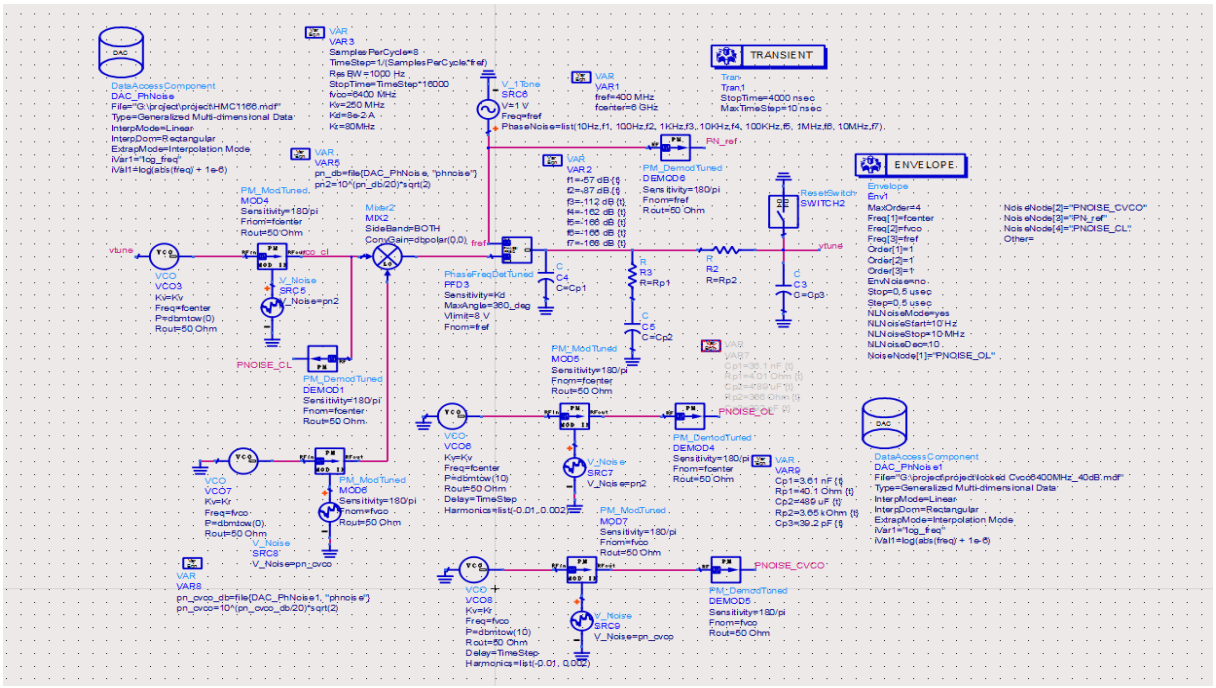


Figure 4.38: Locking HMC1166 with CVCO under 40dB phase noise degradation

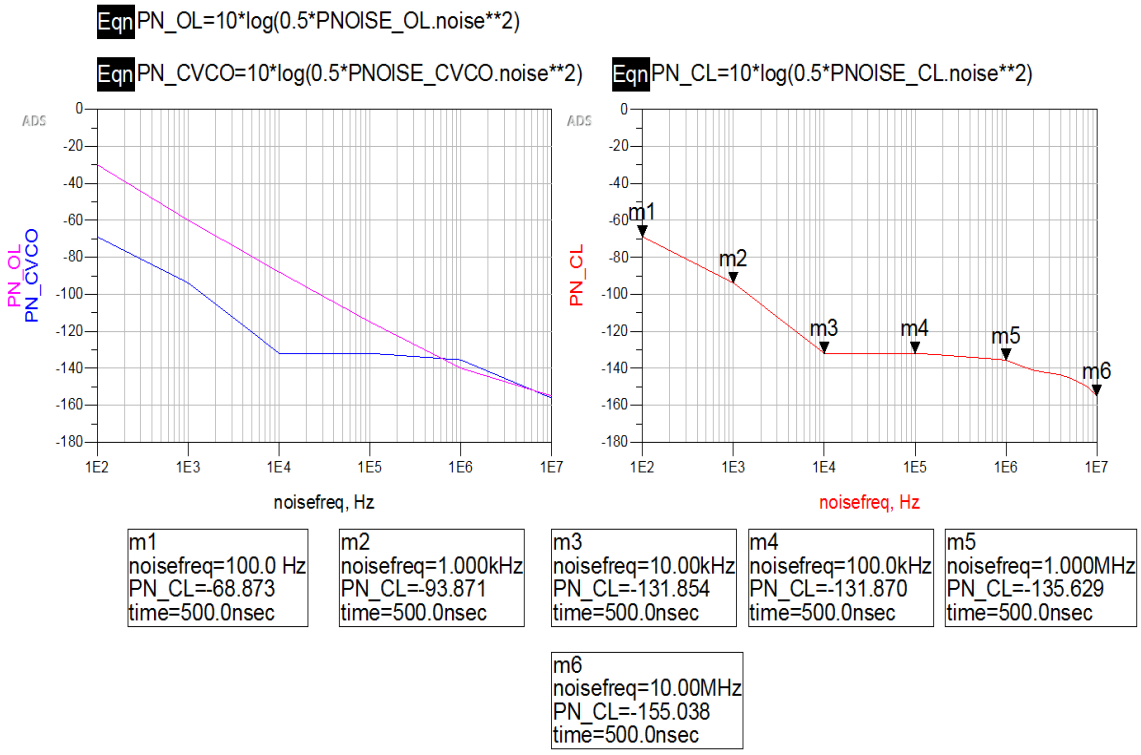


Figure 4.39: DDS of figure 4.38

4.5.3 Locking HMC431 for 5300MHz

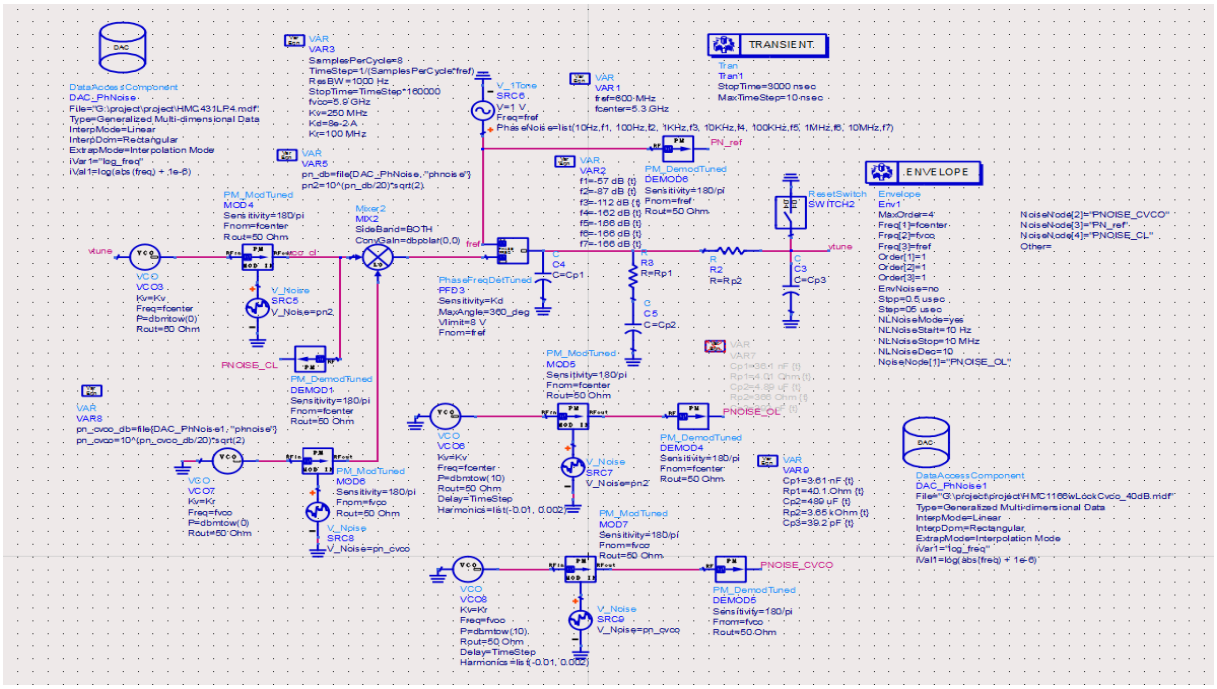


Figure 4.40: Locking HMC431 for 5300MHz under 40dB phase noise degradation

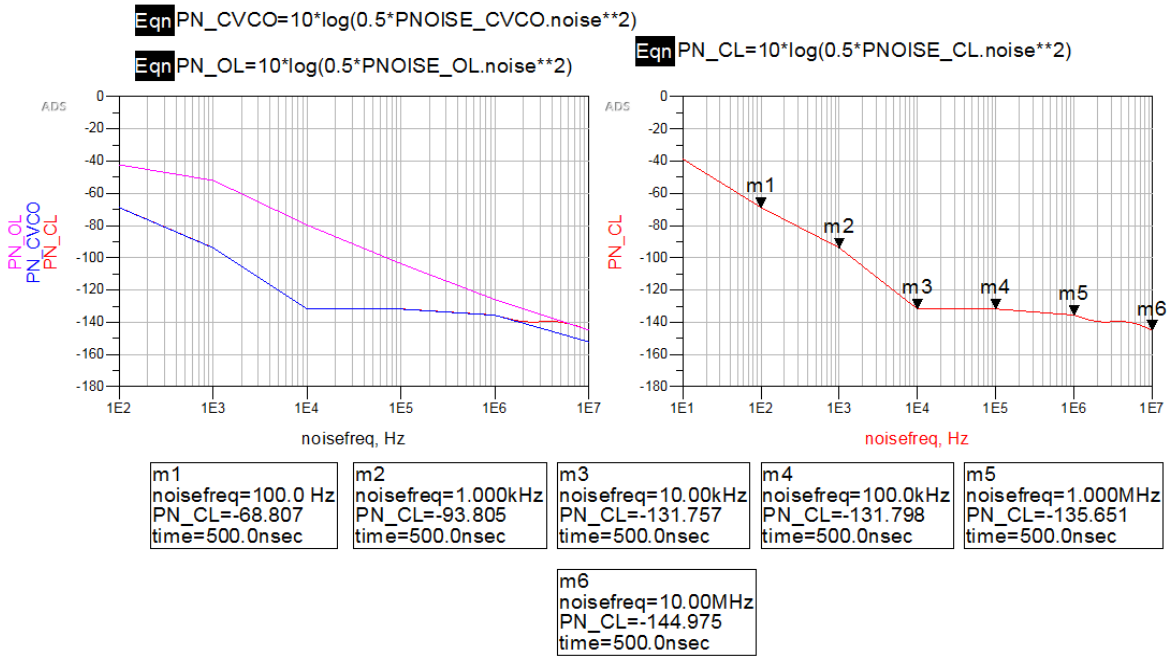


Figure 4.41: DDS of figure 4.40

4.5.4 Locking HMC431 for 5800MHz

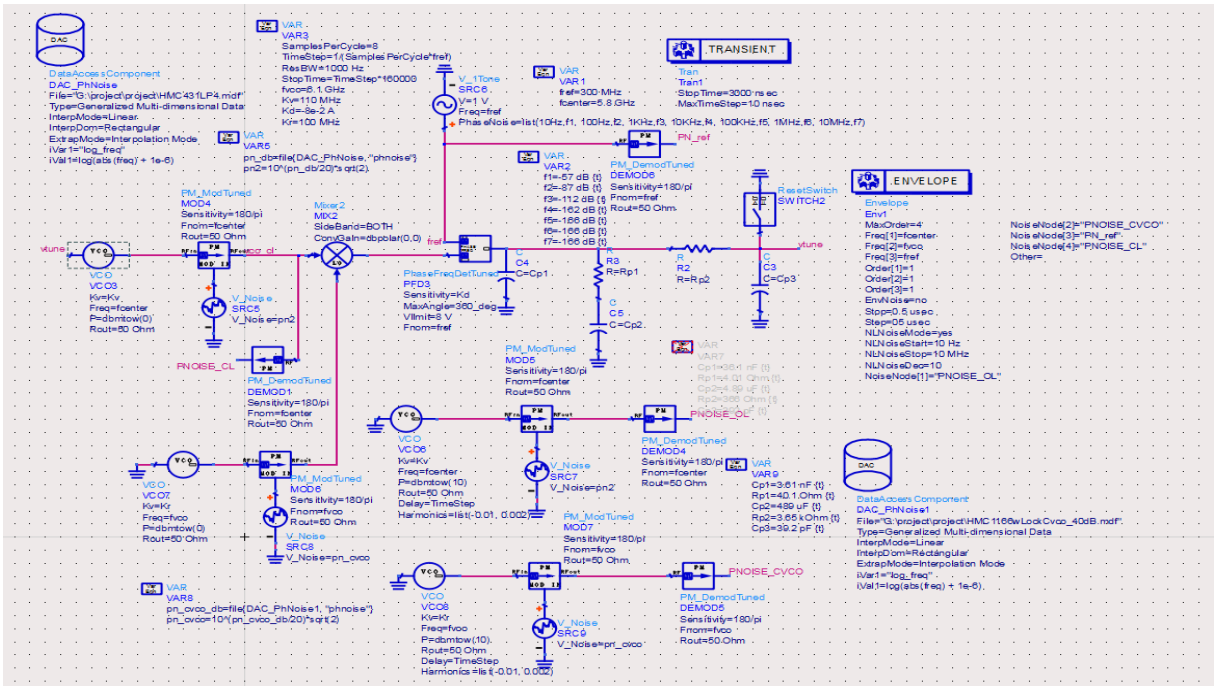


Figure 4.42: Locking HMC431 for 5800MHz under 40dB phase noise degradation

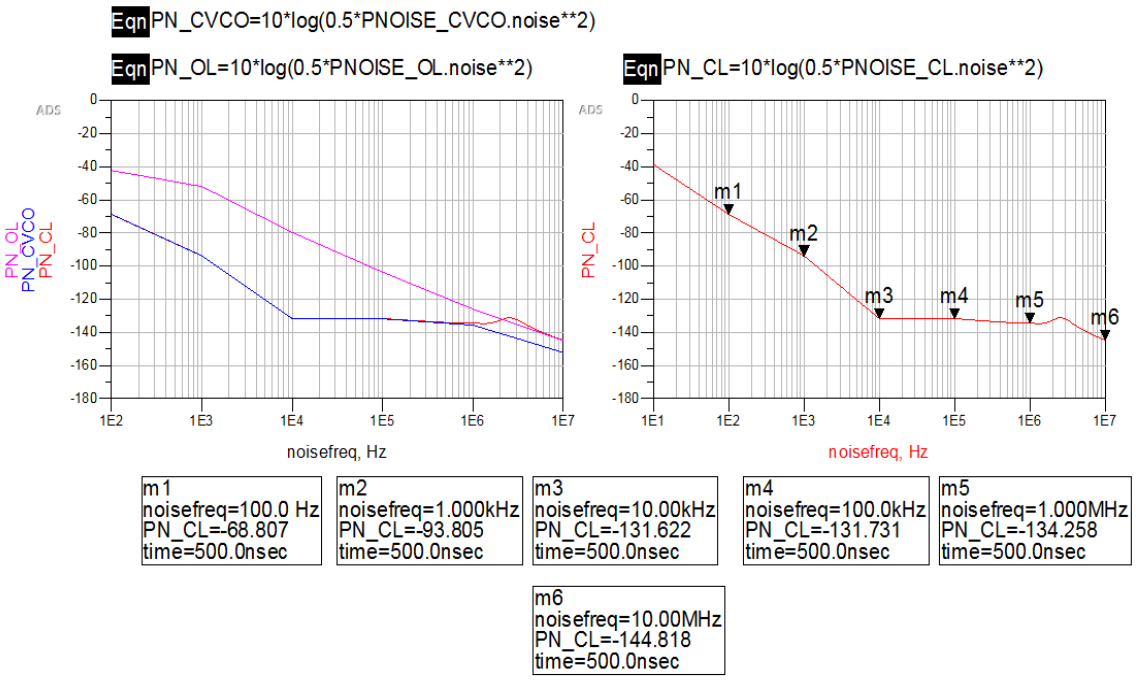


Figure 4.43: DDS of figure 4.42

4.5.5 Locking HMC466 for 6300MHz

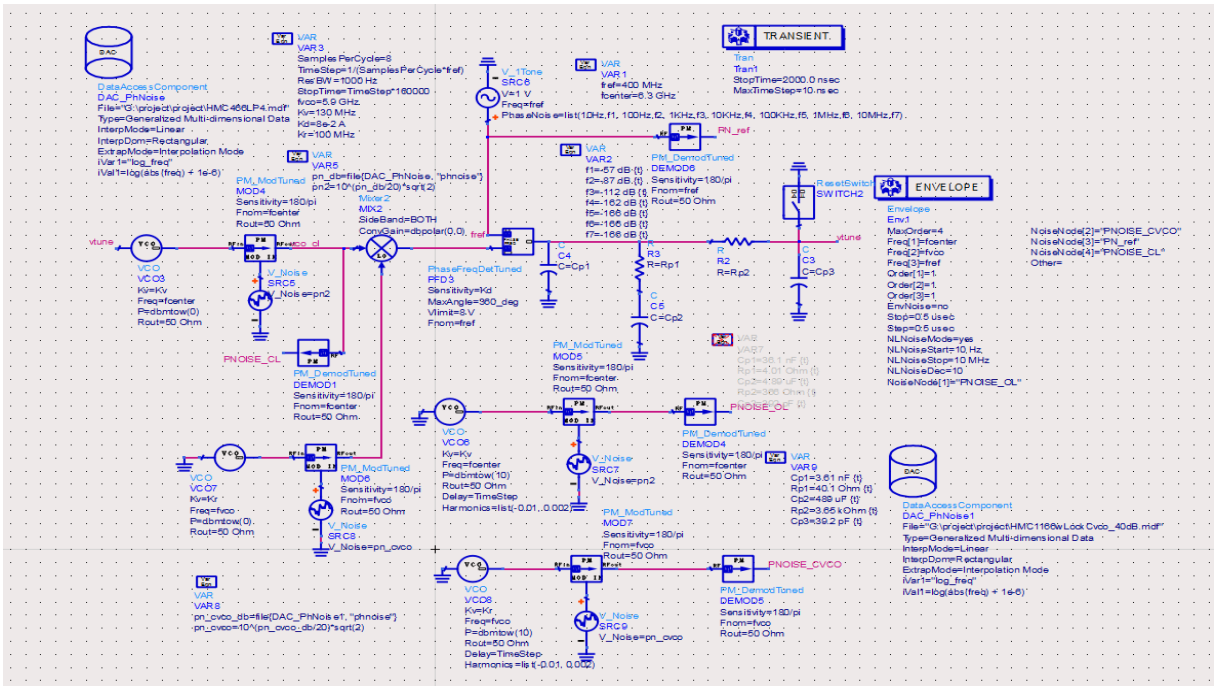


Figure 4.44: Locking HMC466 for 6300MHz under 40dB phase noise degradation

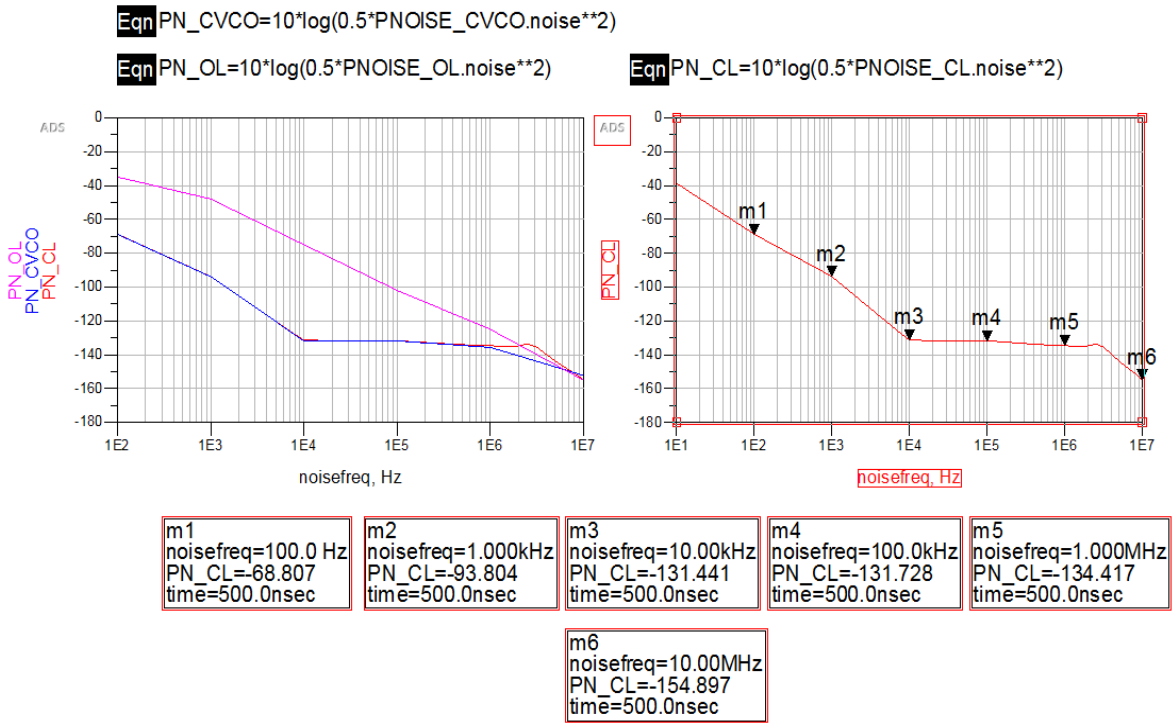


Figure 4.45: DDS of figure 4.44

4.5.6 Locking HMC466 for 6700MHz

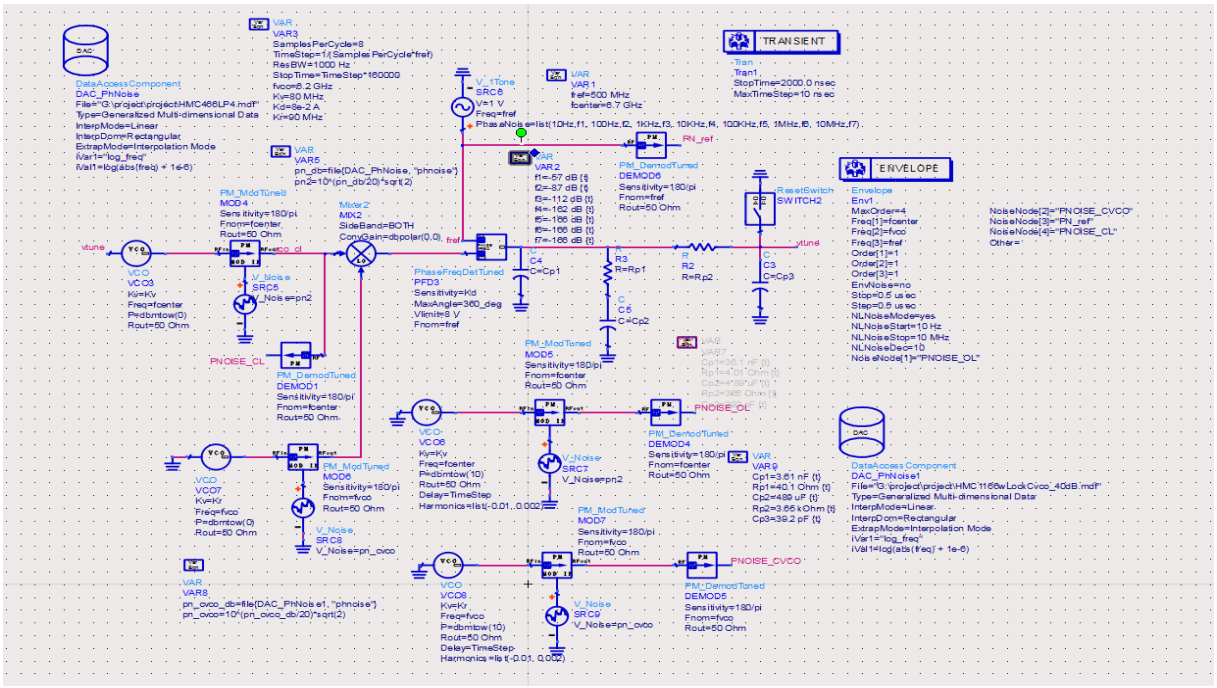


Figure 4.46: Locking HMC466 for 6700MHz under 40dB phase noise degradation

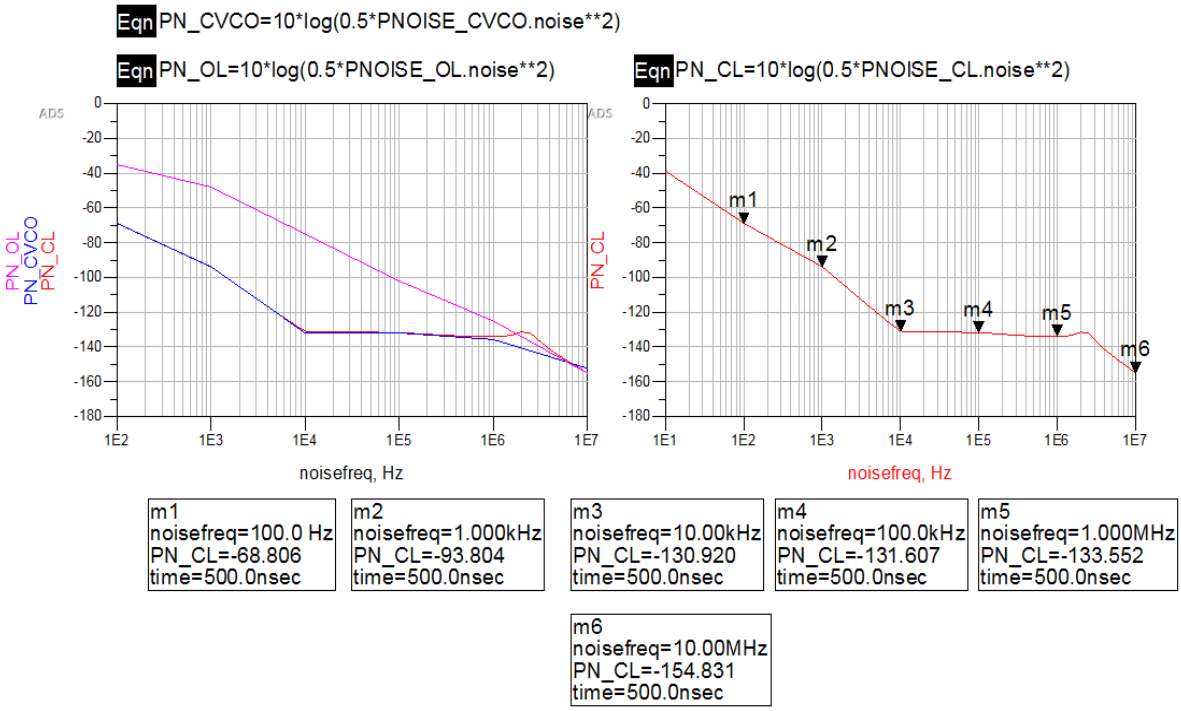


Figure 4.47: DDS of figure 4.46

4.5.7 Locking HMC486 for desired 4000MHz

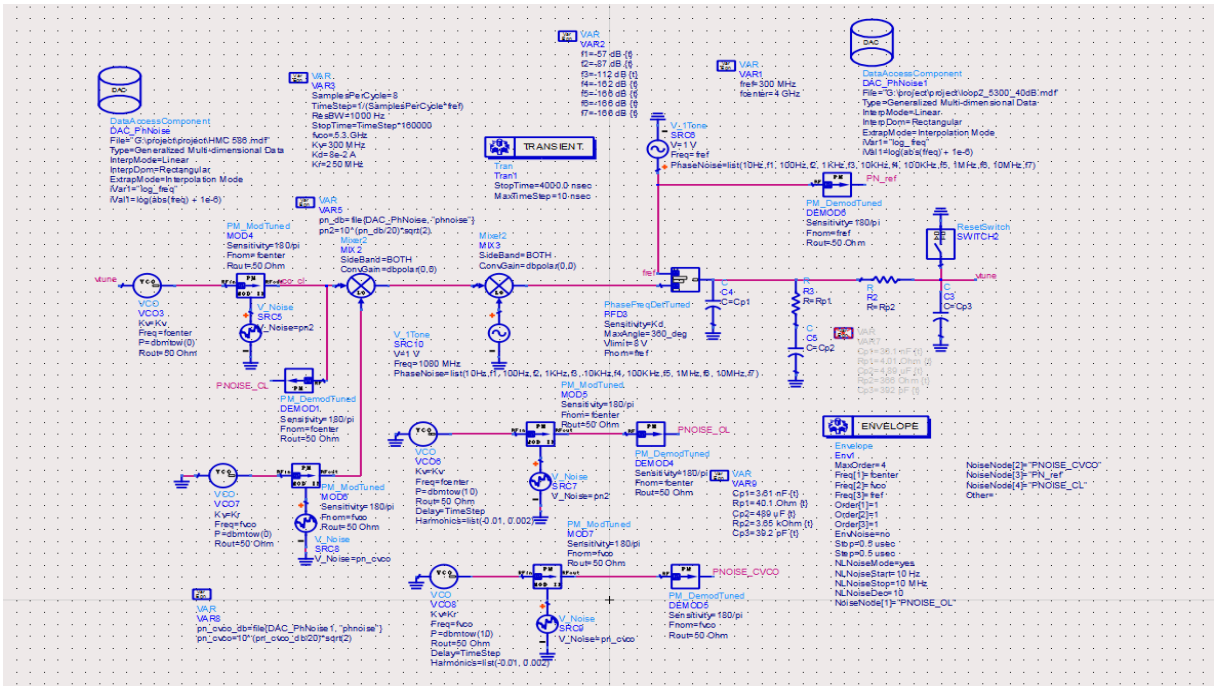


Figure 4.48: Locking HMC486 for 4000MHz under 40dB phase noise degradation

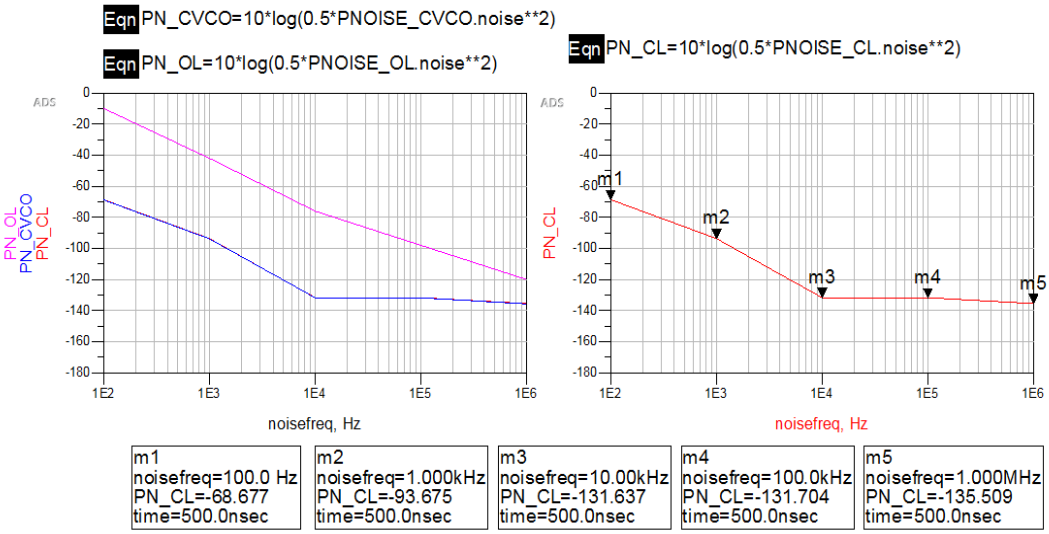


Figure 4.49: DDS of figure 4.48

4.5.8 Locking HMC486 for desired 8000MHz

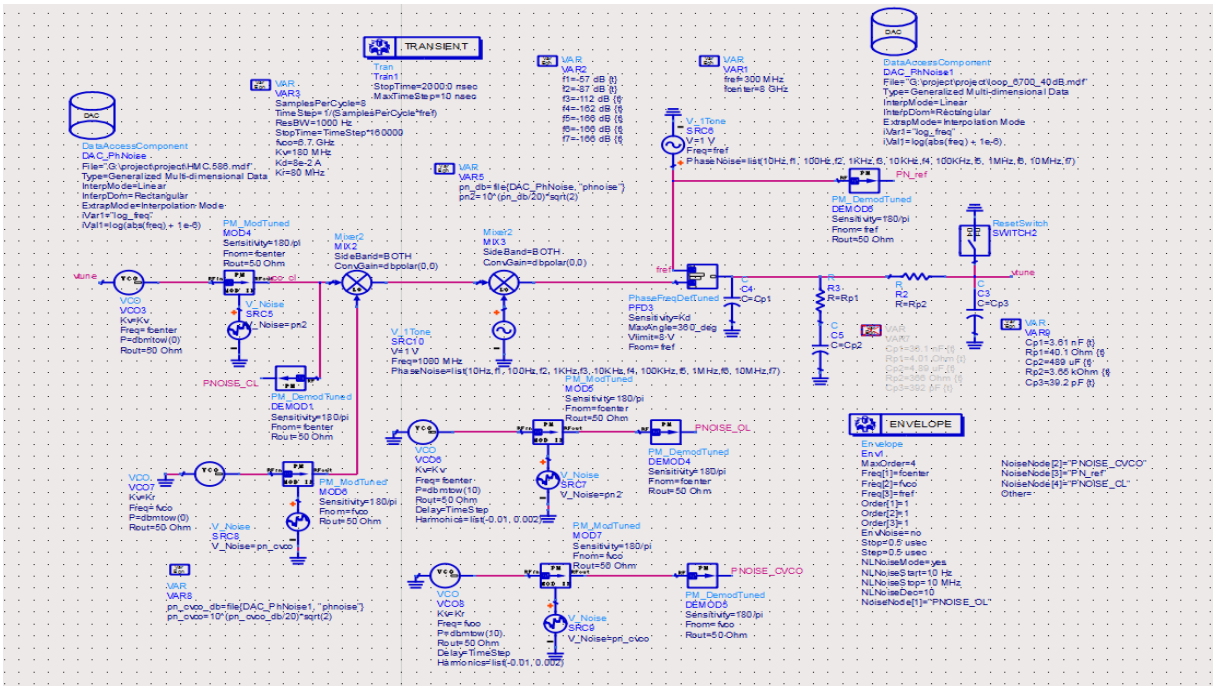


Figure 4.50: Locking HMC486 for 8000MHz under 40dB phase noise degradation

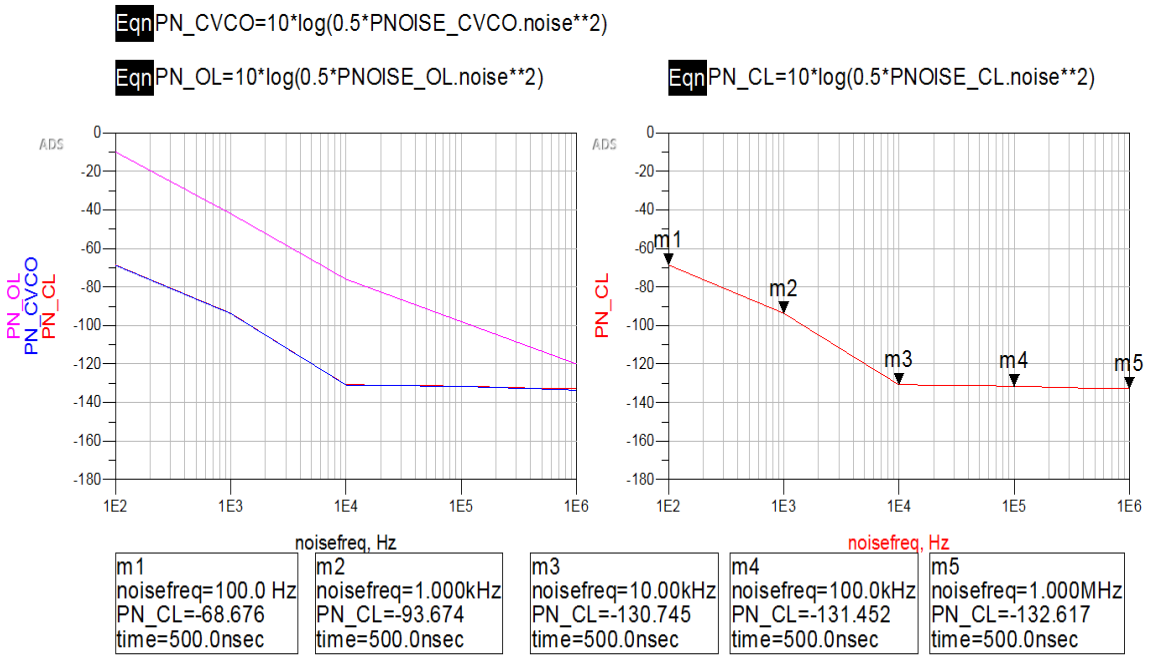


Figure 4.51: DDS of figure 4.50

4.5.9 Phase Noise Performance at 4 and 8 GHz centre frequency under 40dB phase noise degradation

S.No.	Offset Frequency(Hz)	Phase Noise at 4GHz Output	Phase Noise at 8GHz Output
1	100	-68.677	-68.676
2	1K	-93.675	-93.674
3	10K	-131.637	-130.745
4	100K	-131.704	-131.452
5	1M	-135.509	-132.617
6	10M	-155	-155

Table 4.7: Phase Noise Performance under 40dB phase noise degradation

The above result is under 40dB phase noise degradation condition.

4.5.10 Comparison of Phase Noise Performance under static and vibration condition(4GHz)

S. No.	Offset Frequency(Hz)	Static Condition	Vibration Condition(20dB)	Vibration Condition(40dB)
1	100	-107.484	-87.474	-68.677
2	1K	-128.483	-113.560	-93.675
3	10K	-131.638	-131.637	-131.637
4	100K	-131.704	-131.704	-131.704
5	1M	-135.509	-135.509	-135.509
6	10M	-155	-155	-155

Table 4.8: Phase Noise Performance comparison between static and vibration condition(4 GHz)

4.5.11 Comparison of Phase Noise Performance under static and vibration condition(8GHz)

S. No.	Offset Frequency(Hz)	Static Condition	Vibration Condition(20dB)	Vibration Condition(40dB)
1	100	-88.281	-88.671	-68.676
2	1K	-125.195	-113.462	-93.674
3	10K	-130.747	-130.747	-130.745
4	100K	-131.451	-131.452	-131.452
5	1M	-132.616	-132.617	-132.617
6	10M	-155	-155	-155

Table 4.9: Phase Noise Performance comparison between static and vibration condition(8 GHz)

4.6 Schematic Design in PADS

PADS is a design software by Mentor Graphics. PADS is a powerful software and very easy to design. After designing the schematic in Advanced Design Sysytem tool and simulating, we have to again design the schematic with proper ICs.
The very first method in developing a PCB is to create a schematic of the circuit. However we already create a schematic in ADS but not with ICs. With the help of PADS-PCB design tool another schematic of the complete circuit is made. The block diagram in figure 4.1 and 4.2 is divided into six loops and with the help of designed schematic in ADS, PDS schematic is created. After completing schematic design, electronic design is converted into netlist. It contains the information of the nodes to which each pin connects[35].

All schematics are provided from next page :-

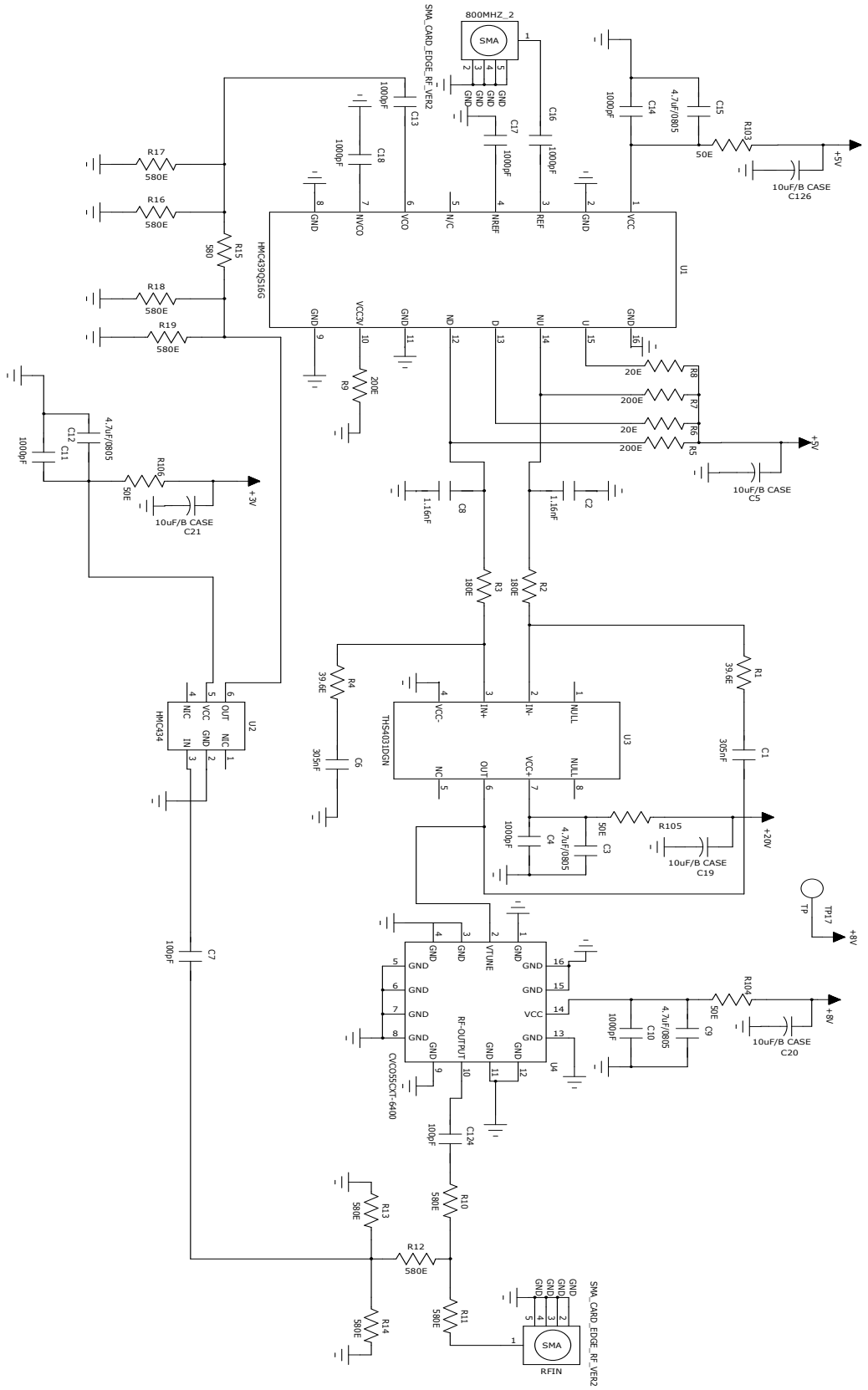


Figure 4.52: Schematic of loop-1

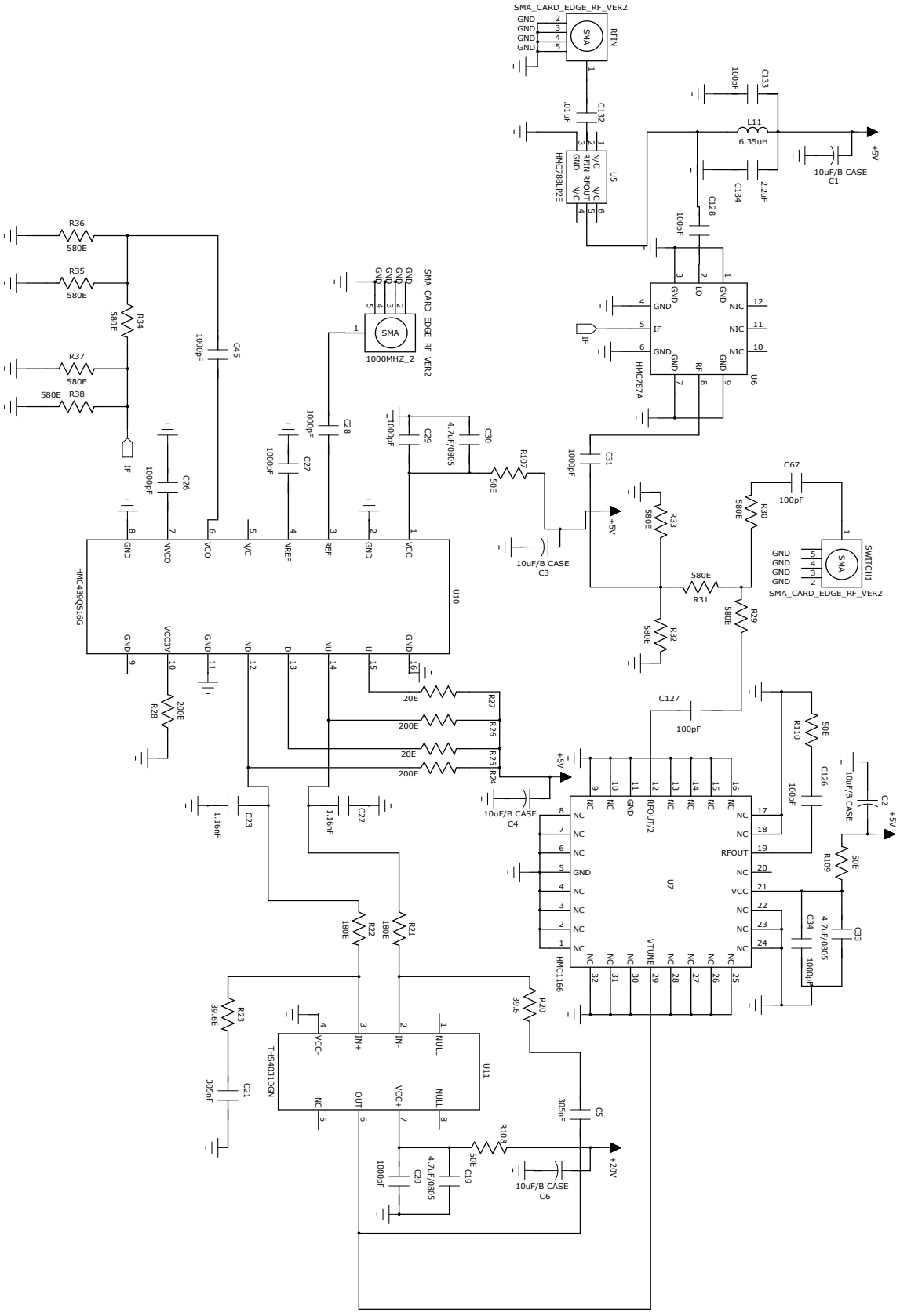


Figure 4.53: Schematic of loop-2

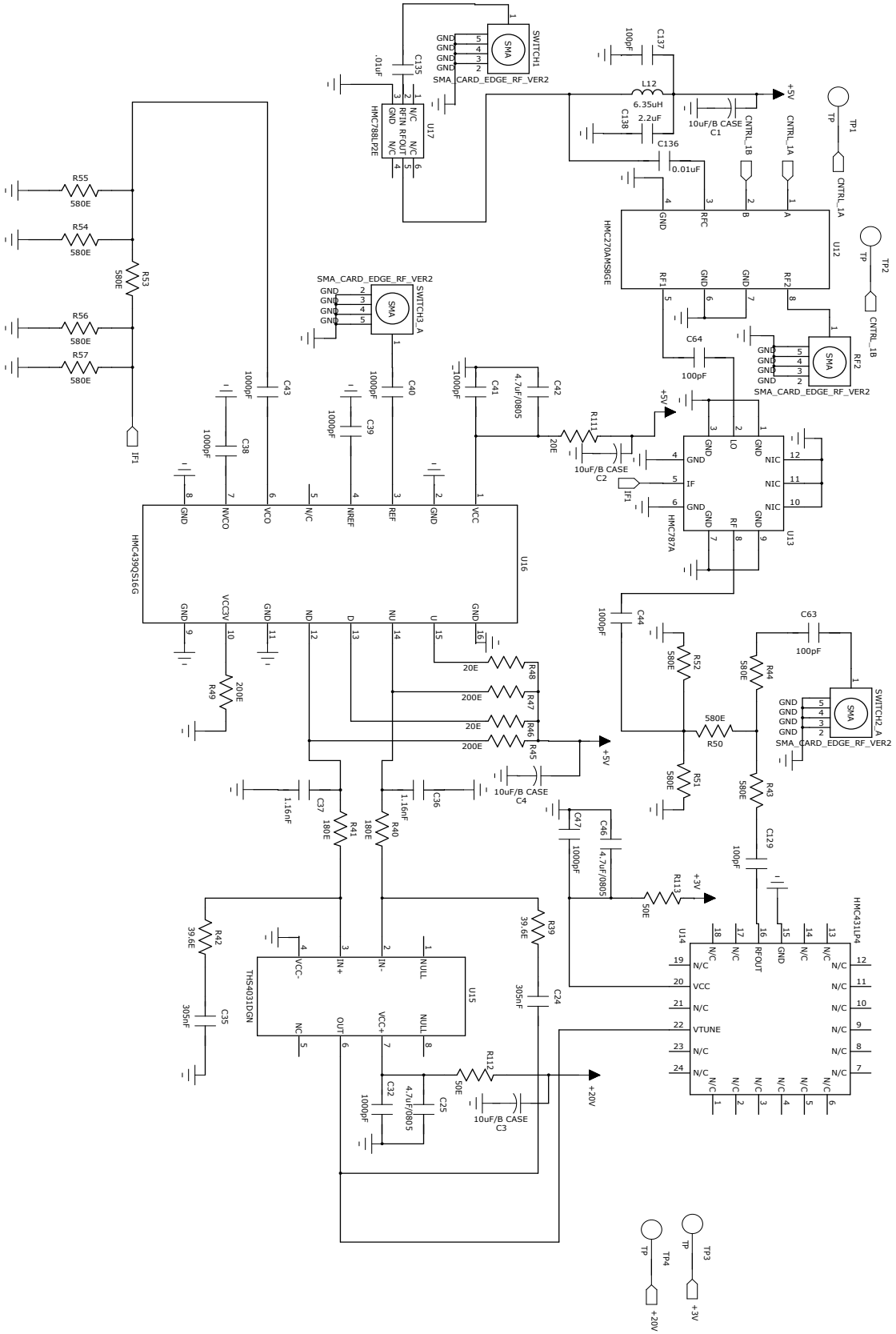


Figure 4.54: Schematic of loop-3

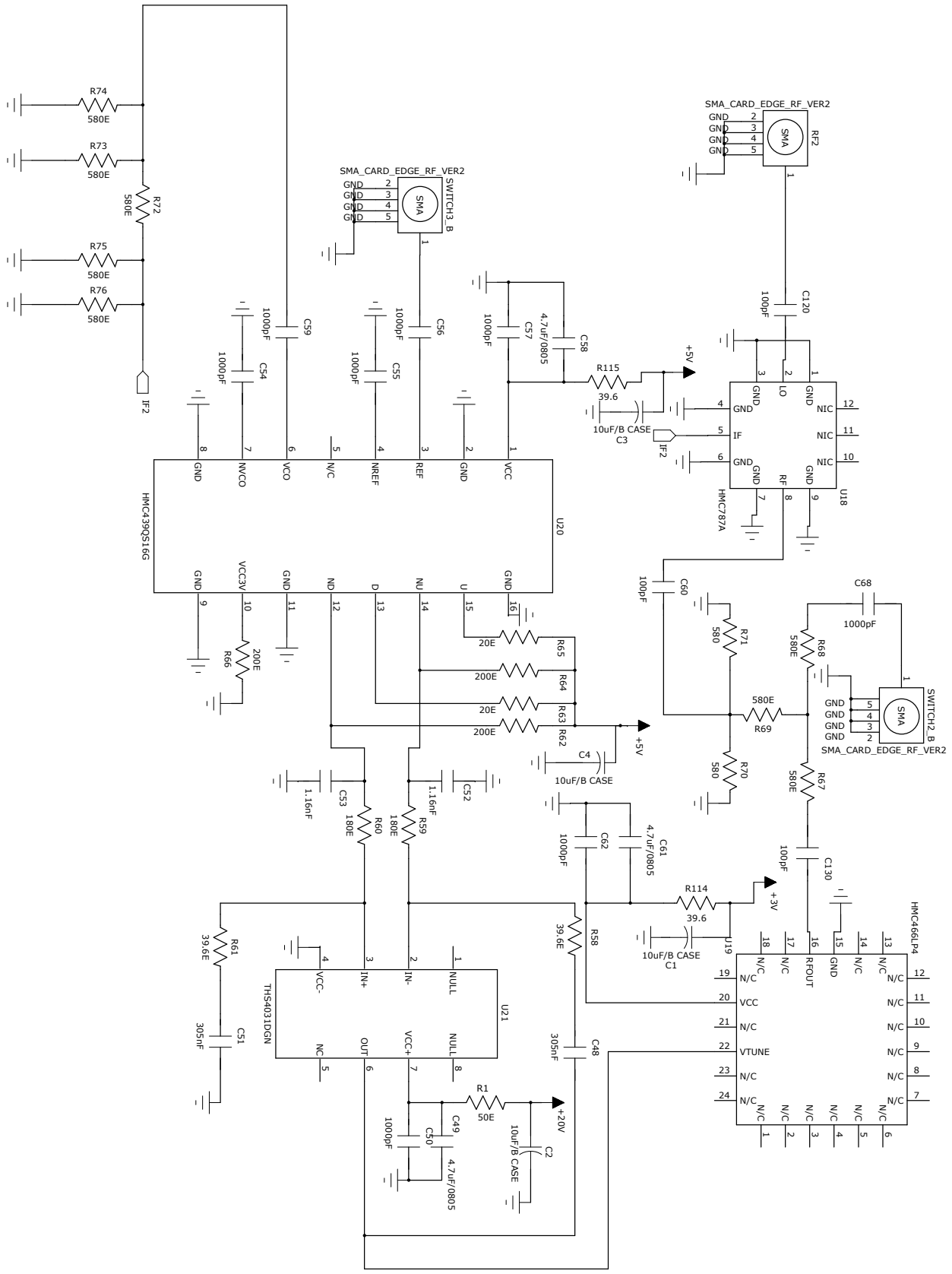


Figure 4.55: Schematic of loop-4

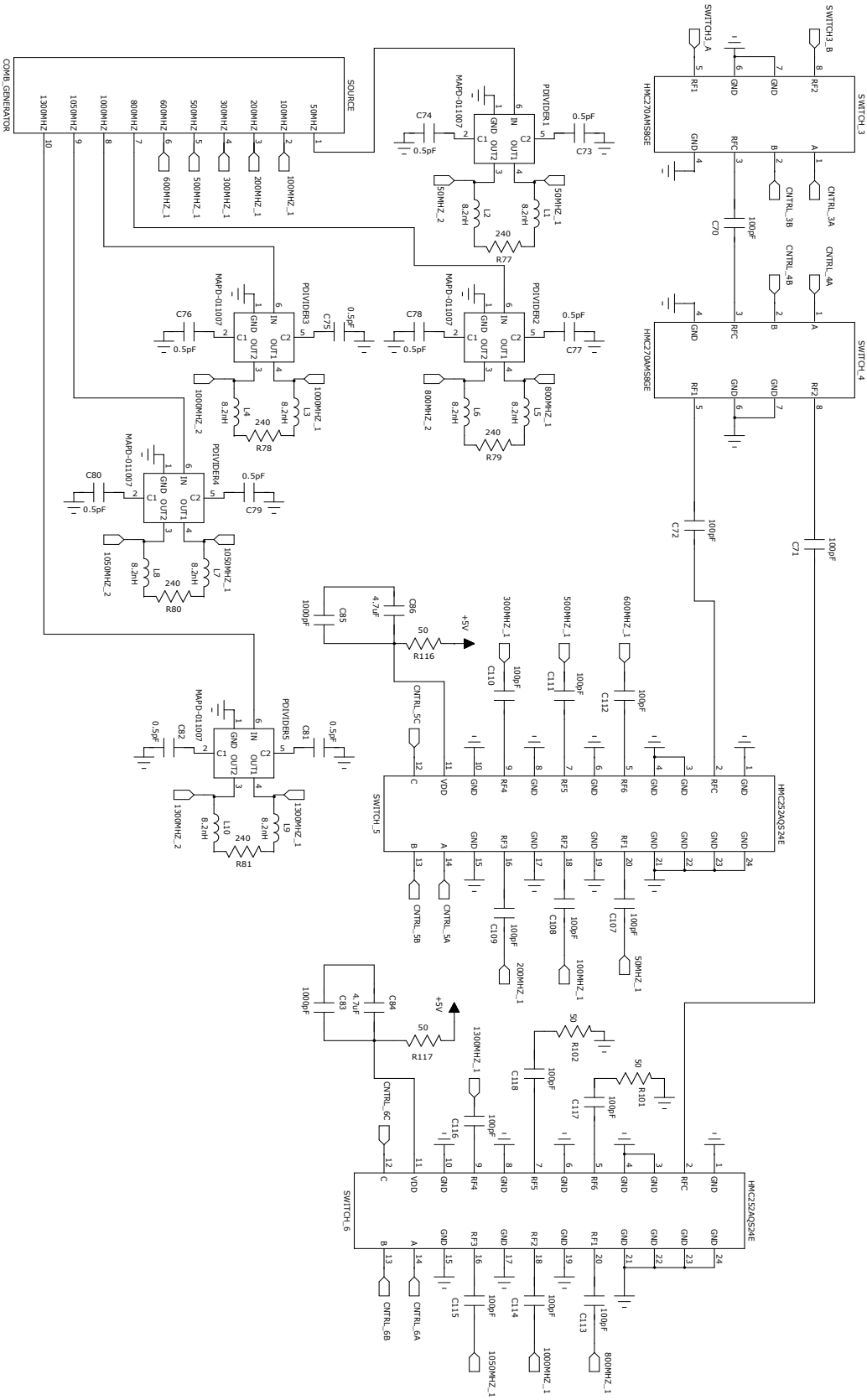


Figure 4.56: Schematic of loop-5

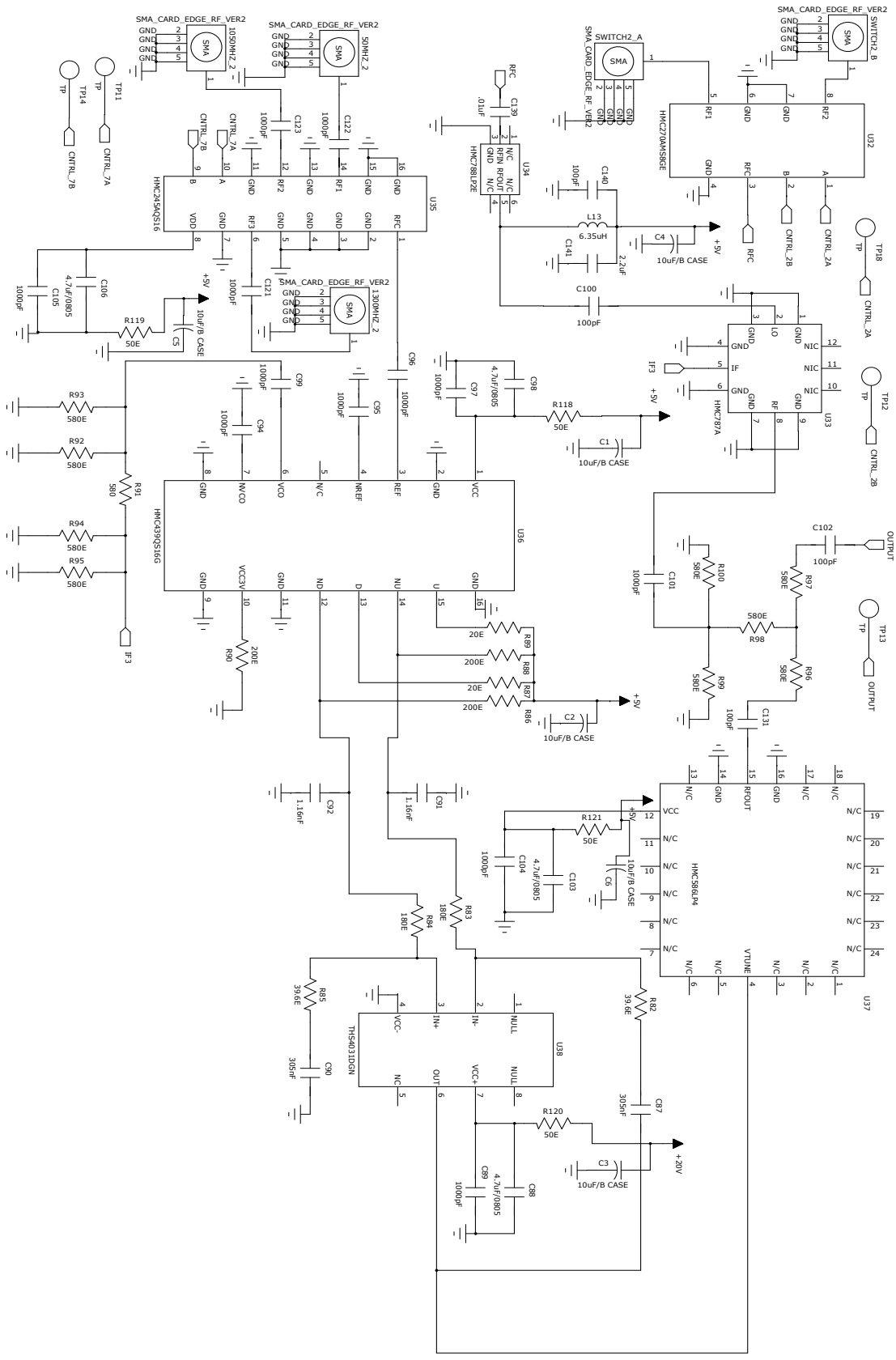


Figure 4.57: Schematic of loop-6

4.7 PCB Component Placement and Routing in PADS

Before proceeding to create layout and final PCB design. It is essential to have the rough idea of the components location and available space on the board to contain the complete circuitry. With the help of this, designers will able to decide whether double or multilayers are needed.
After that footprints for the all the ICs is made and layout is created for PCB design which contains all the relevant information. Now routing is done in PADS after completing the basic placement. With the help of netlist from schematic, PADS software routes the physical connection on the board[35].
RF board is fabricated on a 0.5mm thick Rogers 4350 substrate. Multilayer PCB is to be designed. With the help of W/L equation width of 50Ω RF line is calculated which comes 1.1mm.
Properly placed and routed layout of the above schematics are provided from next page:-

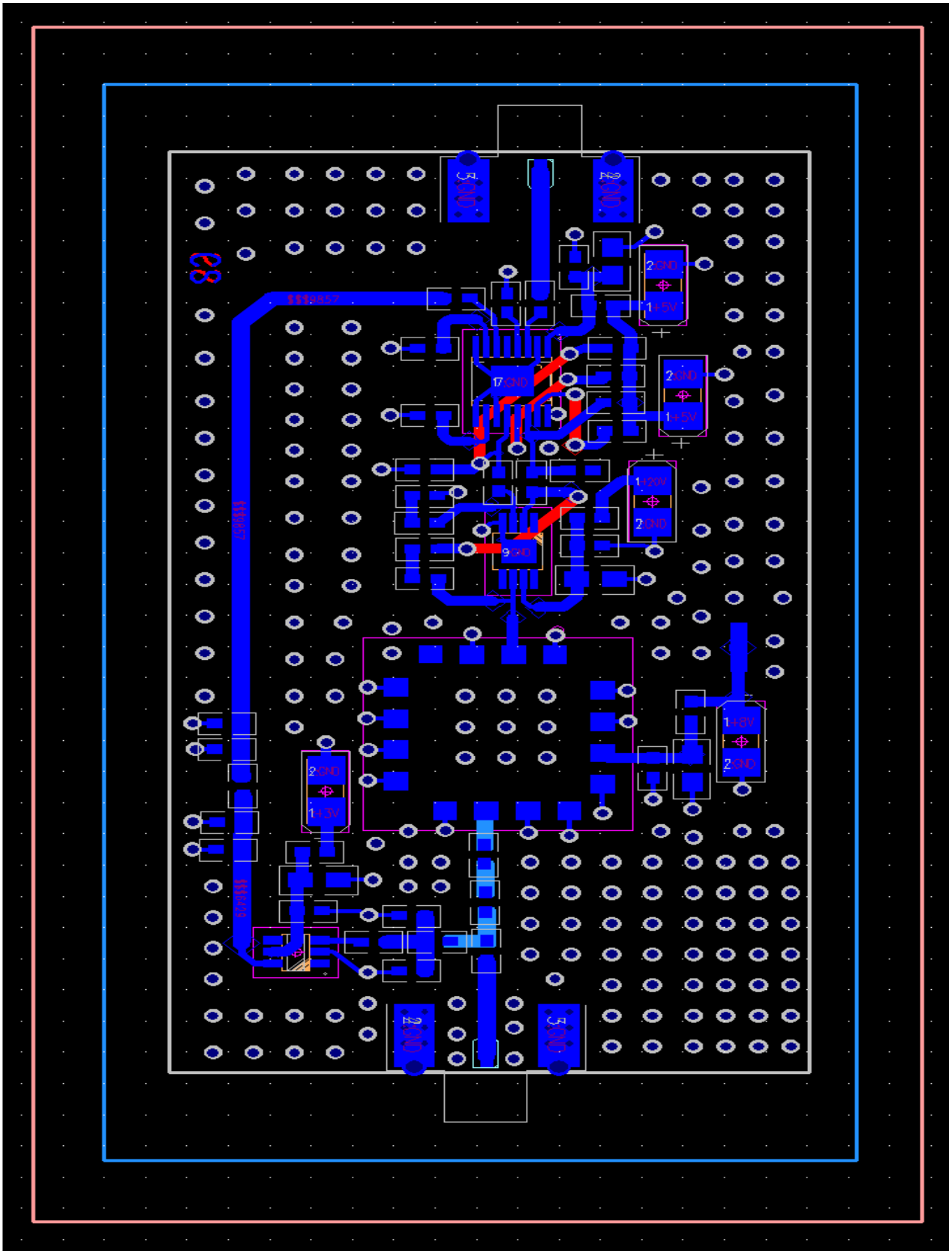


Figure 4.58: PCB Layout Design of loop-1

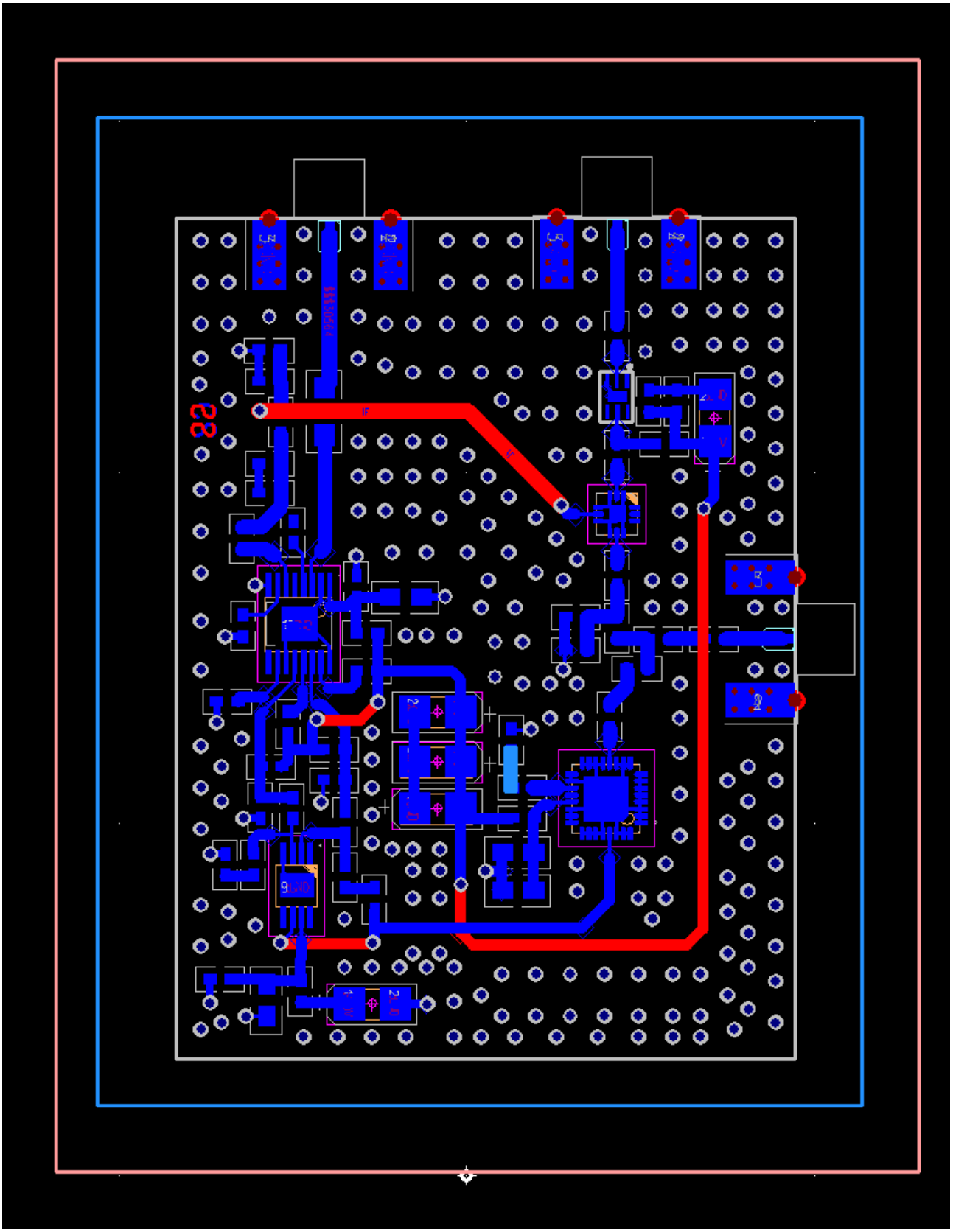


Figure 4.59: PCB Layout Design of loop-2

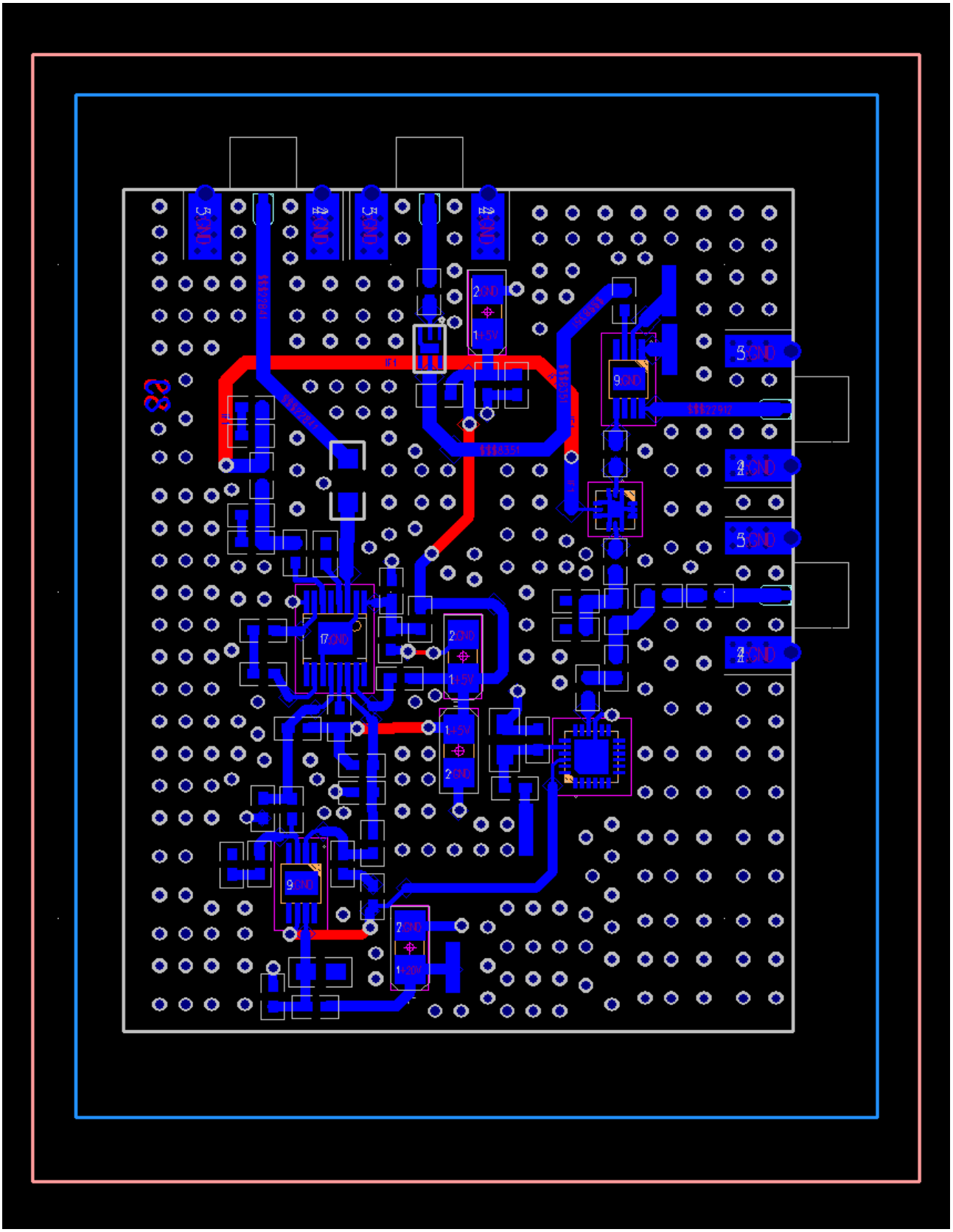


Figure 4.60: PCB Layout Design of loop-3

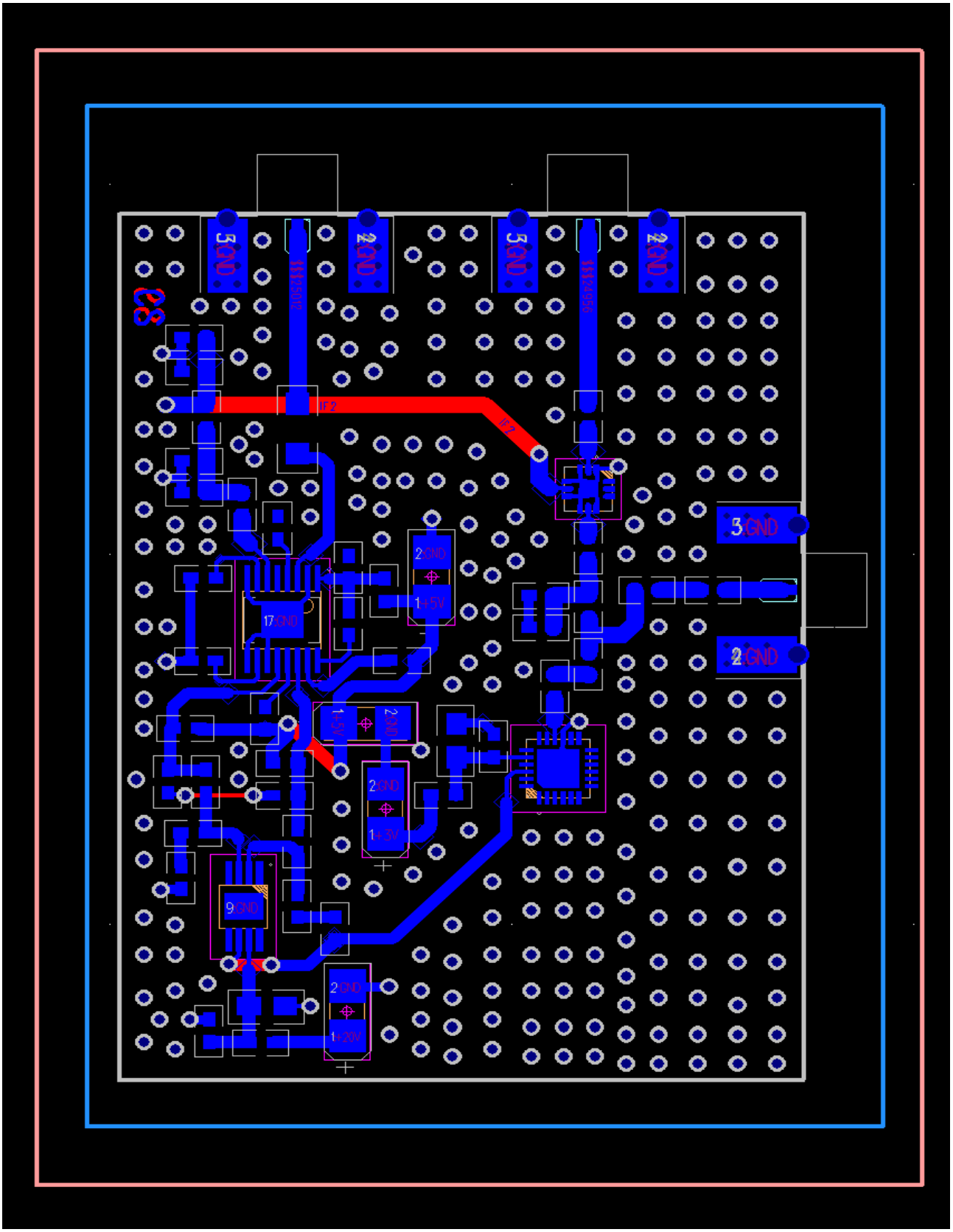


Figure 4.61: PCB Layout Design of loop-4

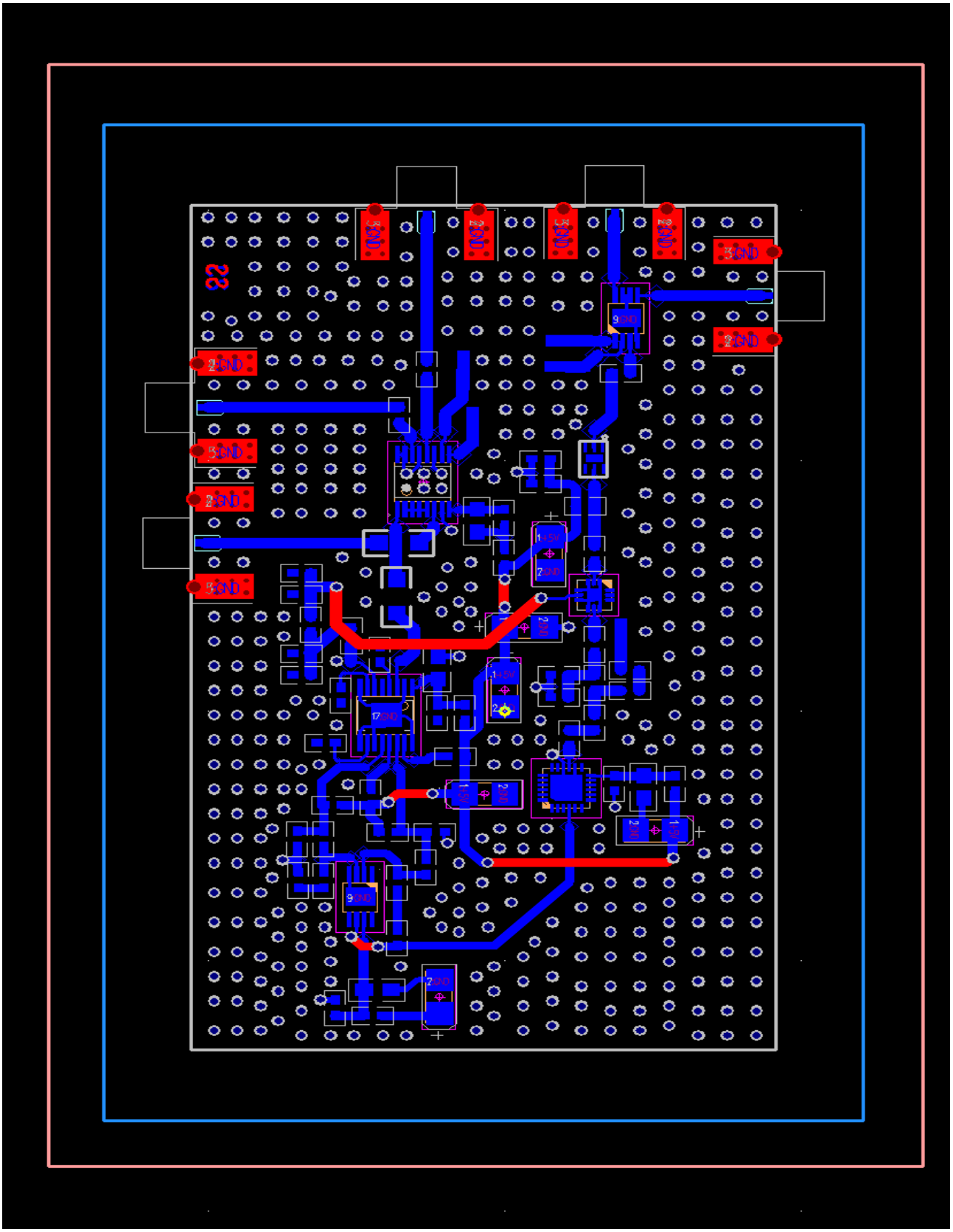


Figure 4.62: PCB Layout Design of loop-6

Chapter 5

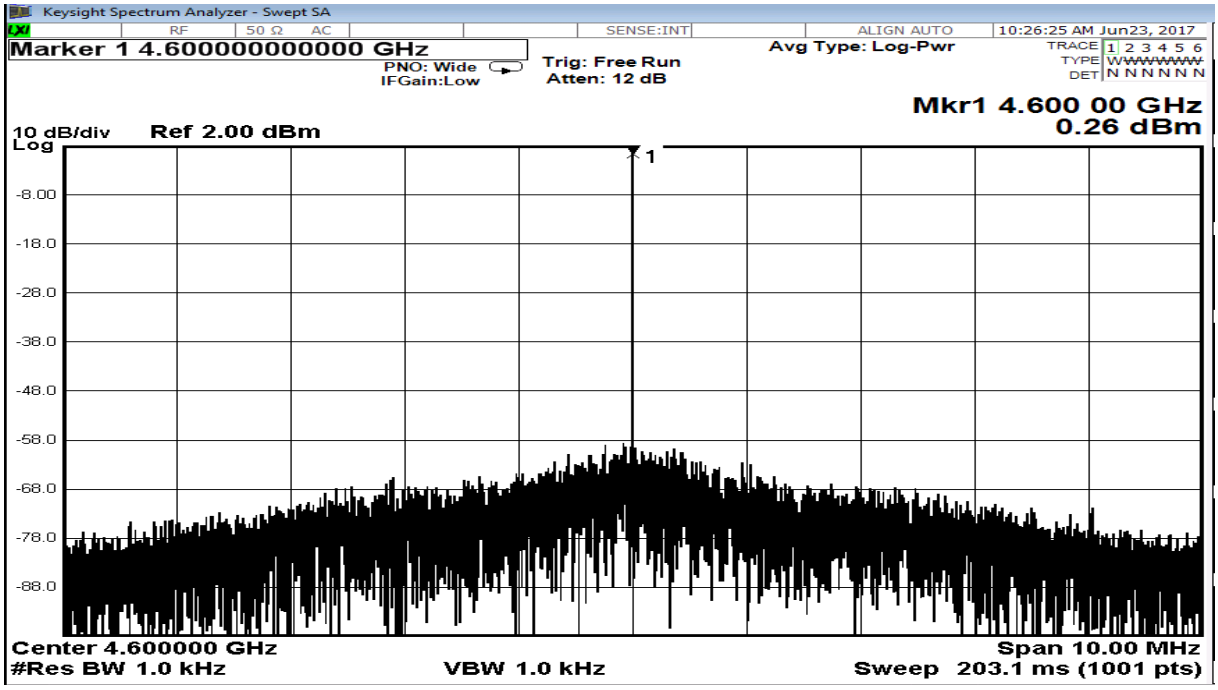
Results

Phase Noise Performance of the created frequency synthesizer is tested and measured in **Keysight N9020A MXA Signal Analyzer** whose frequency range is 10Hz to 26.5Hz, and the required 100MHz reference frequency signal is provided with **Oven Controlled Crystal Oscillator(OCXO)**. Coaxial cable is used to connect the prototype with spectrum analyzer.

To meet the required standards was very challenging and some compromises were also made to save time, money and reduce complexity. Many problems and challenges were faced and dealt with while designing. Phase noise of reference oscillator degrade drastically under vibration condition and to decrease the impact of vibration on OCXO vibration isolators were used. While testing we found out that the VCO power was not enough to drive the mixer, therefore amplifiers were used for every mixer. At the initial stages of designing the loop bandwidth we used was 1KHz, which was not giving the desired phase noise result. Therefore loop bandwidth was changed to 1MHz. It also decreases the lock time. Similarly charge pump of PFD were managed to get the better result.

The spectrum of the phase noise refers to the plot that would be obtained from a spectrum analyzer. The spectrum of the signal would show the centre wanted signal with the noise sidebands extending either side of the main carrier, and the phase noise plot from spectrum analyzer shoes the phase noise performance at a carrier frequency. It is a logarithmic plot with x axis be the log axis of offset frequencies from carrier frequency in Hz and y axis be the phase noise in decibels relative to carrier.

The measured phase noise performance screenshots and power spectrum screenshots from spectrum analyzer for output frequencies from 4GHz to 8GHz are provided from next page:-



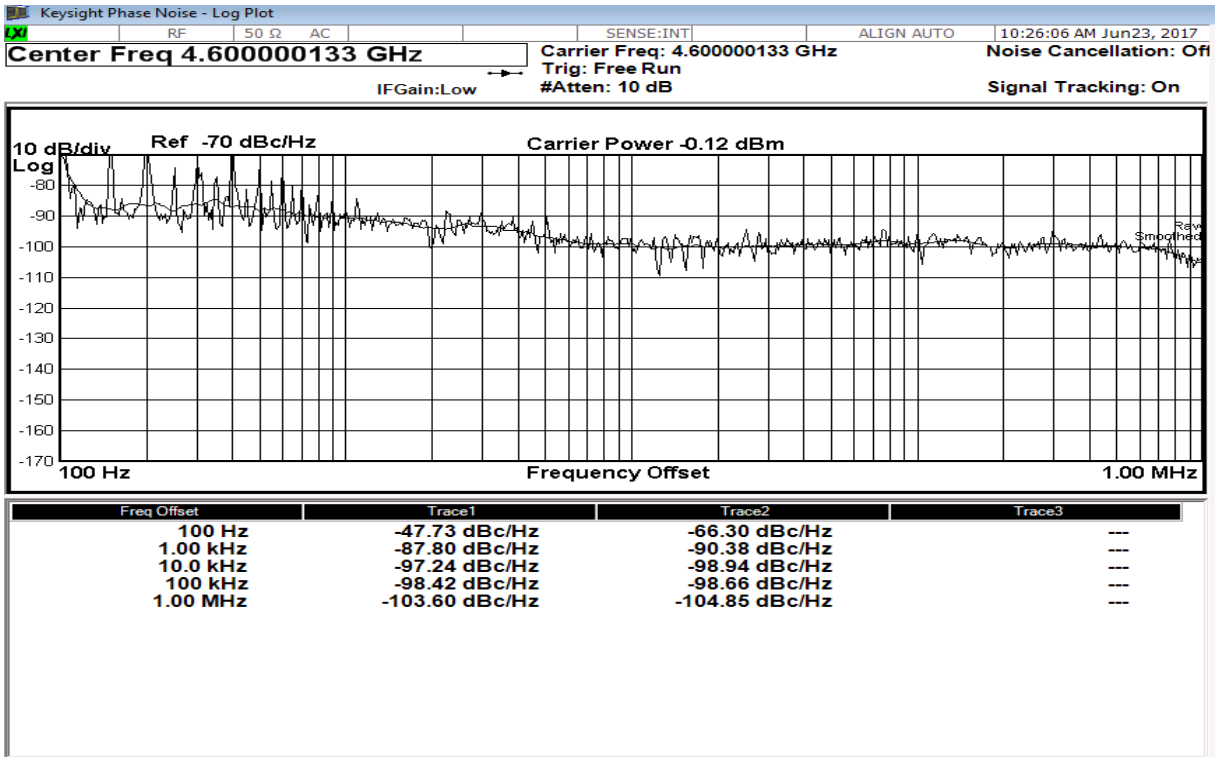
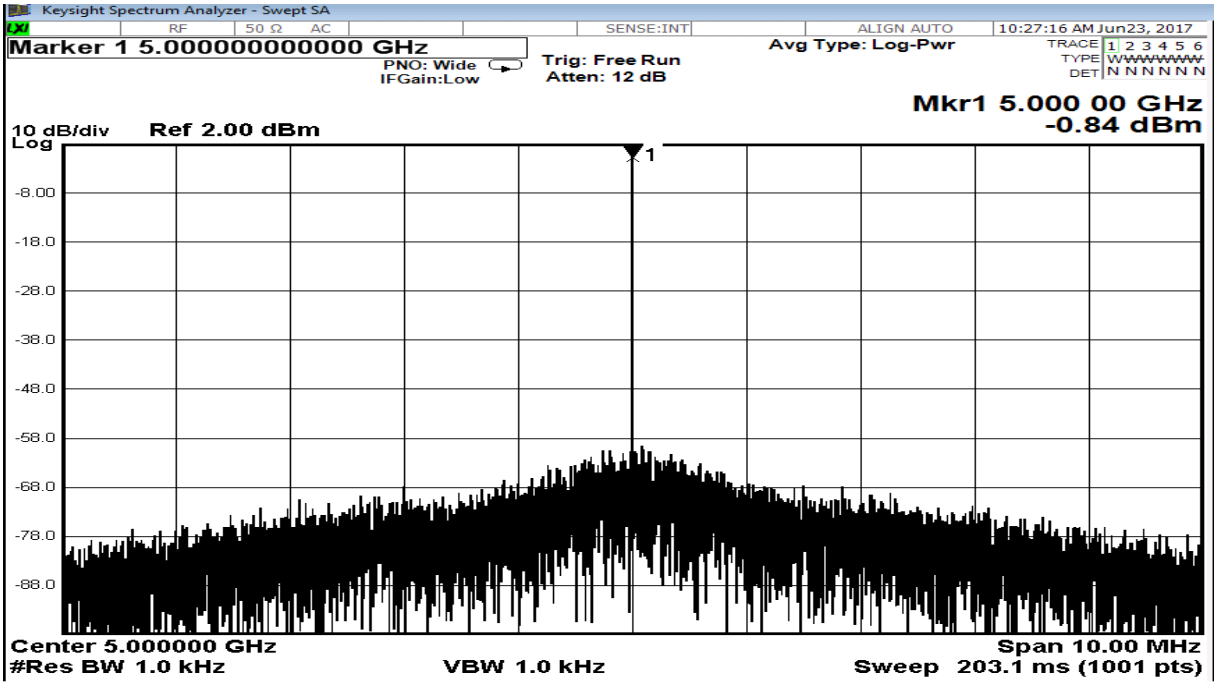


Figure 5.1: Measured Phase Noise Performance at 4.6 GHz



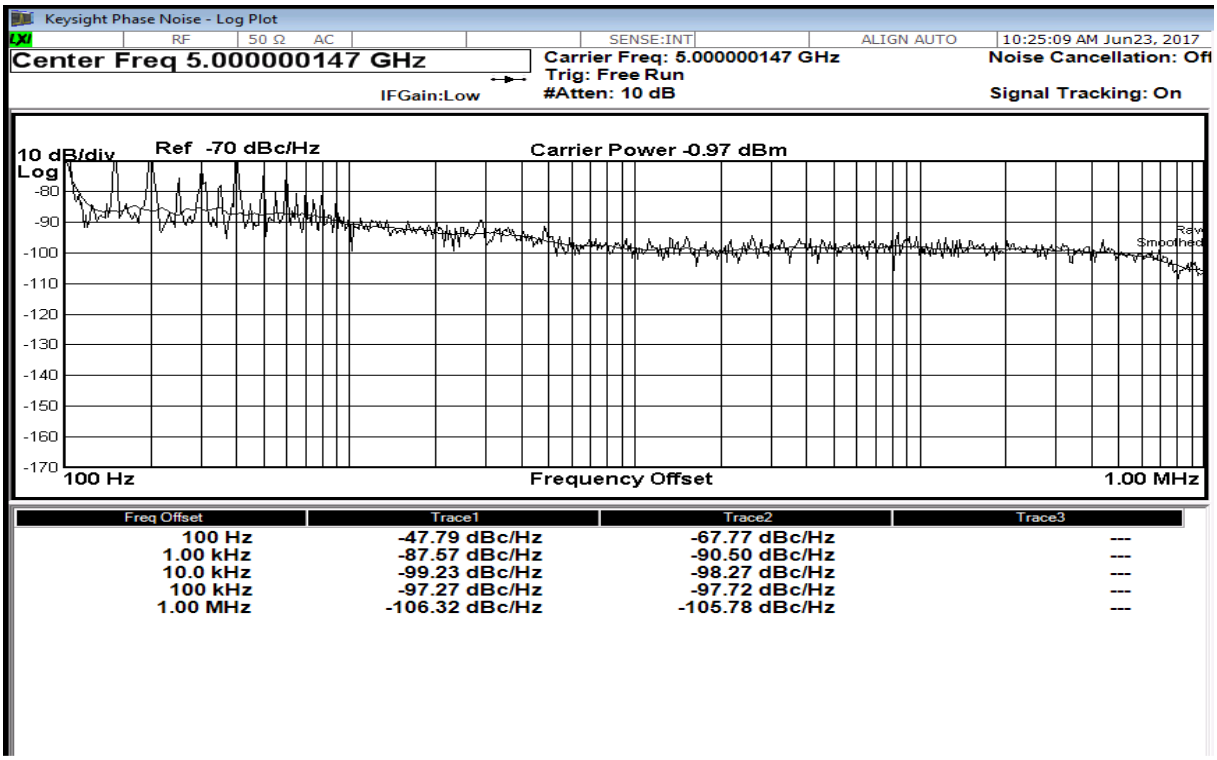
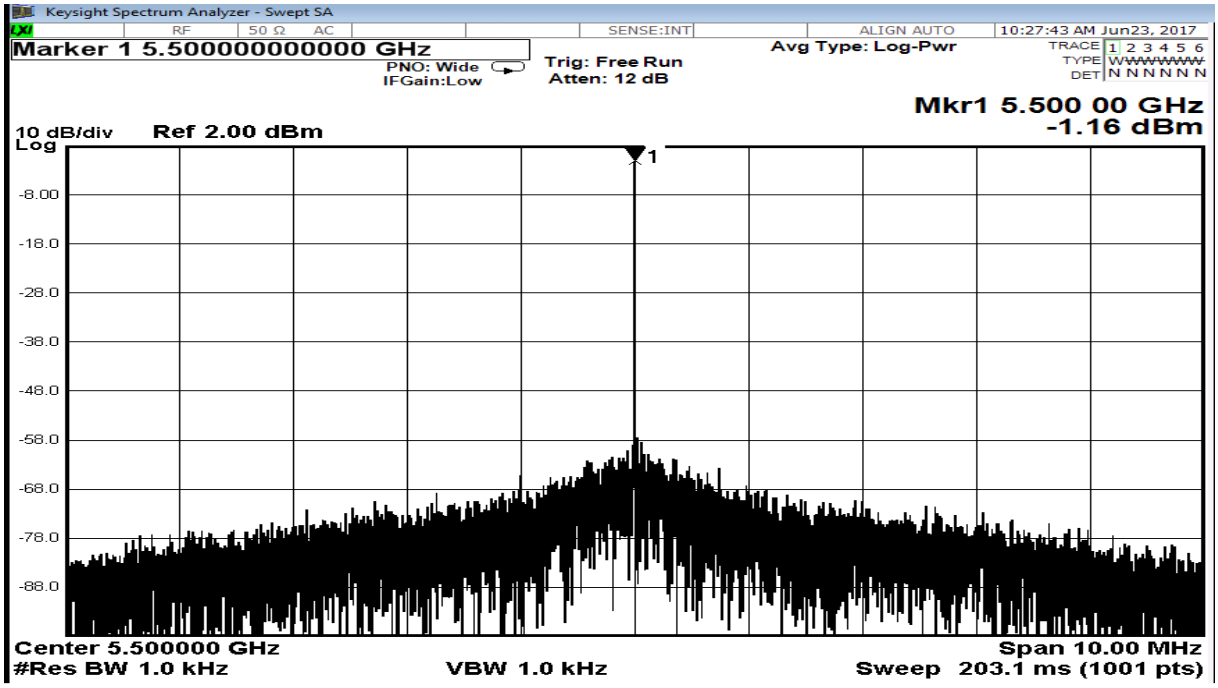


Figure 5.2: Measured Phase Noise Performance at 5 GHz



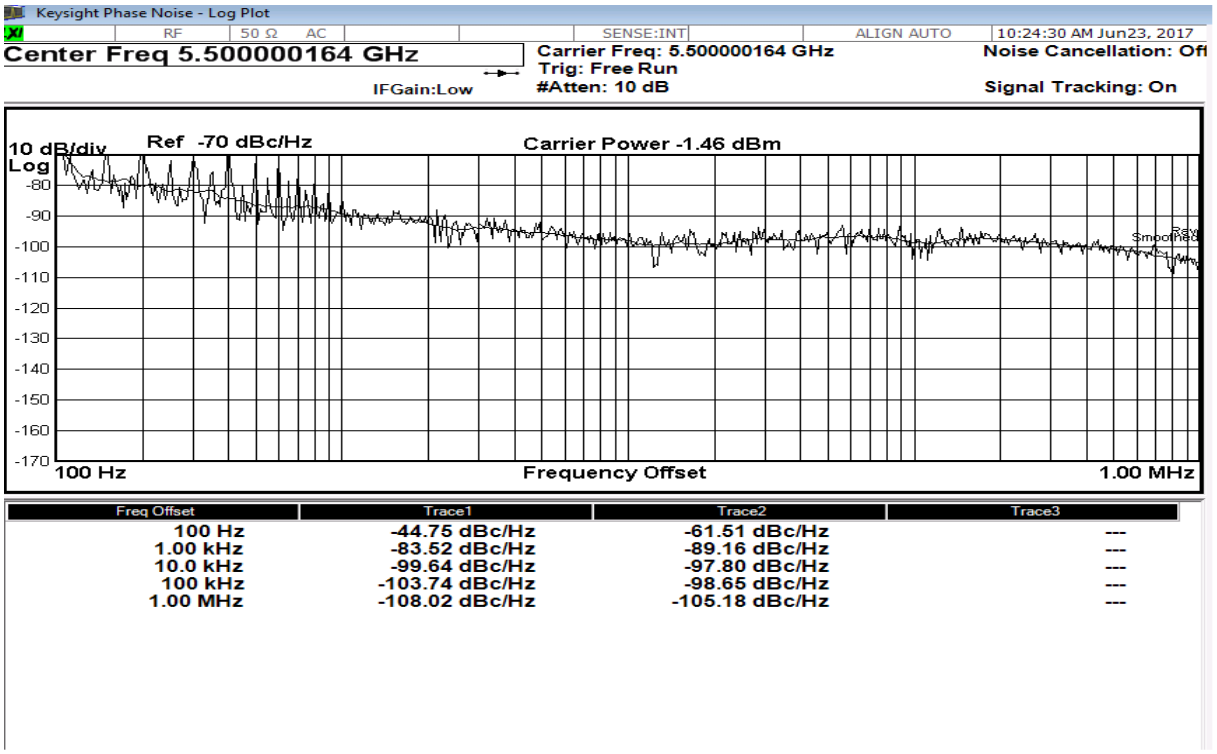
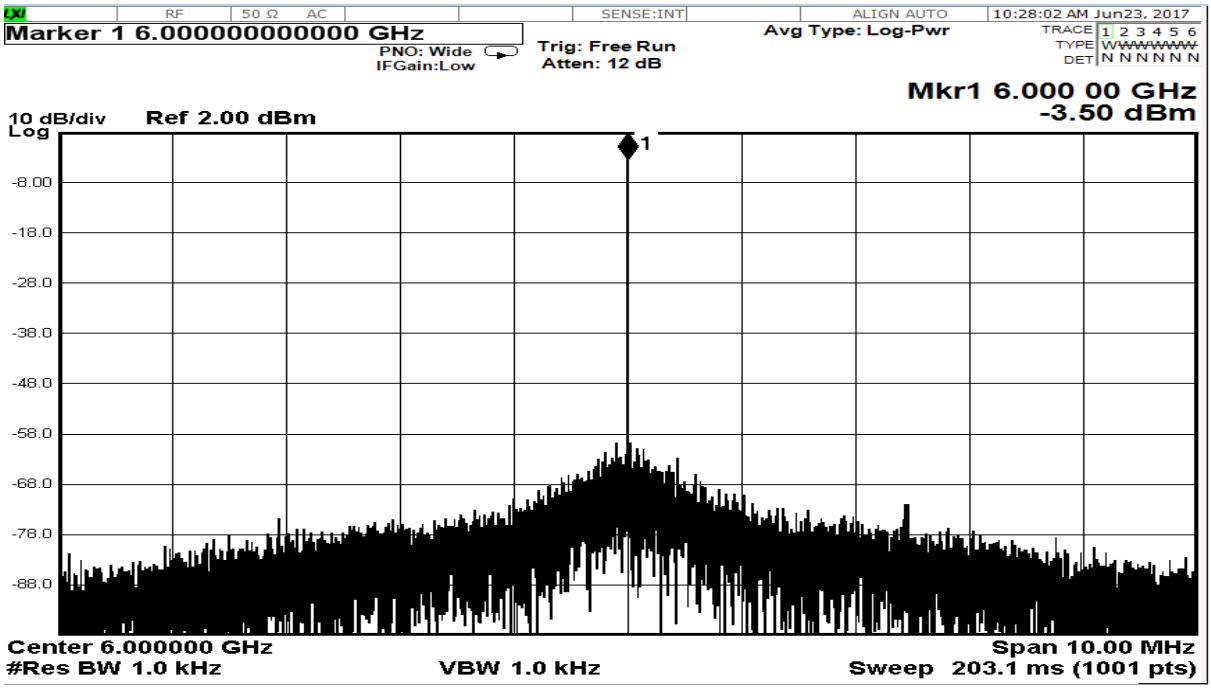


Figure 5.3: Measured Phase Noise Performance at 5.5 GHz



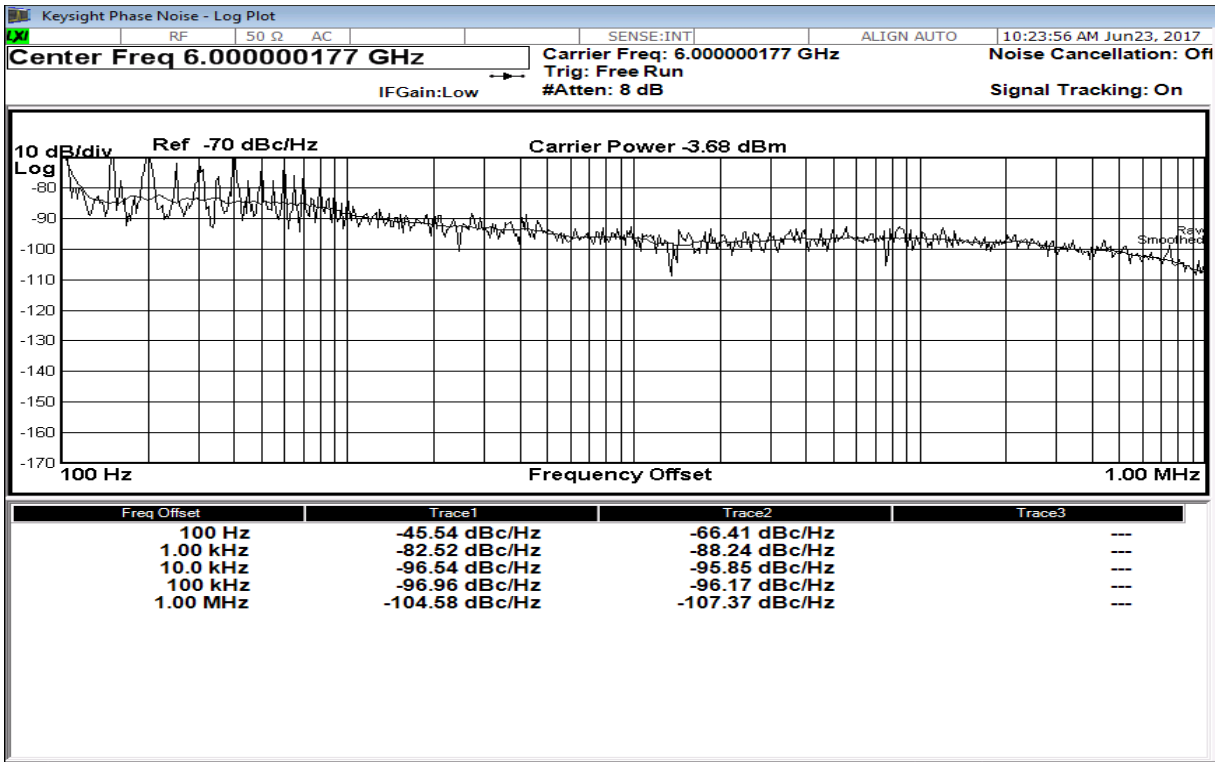
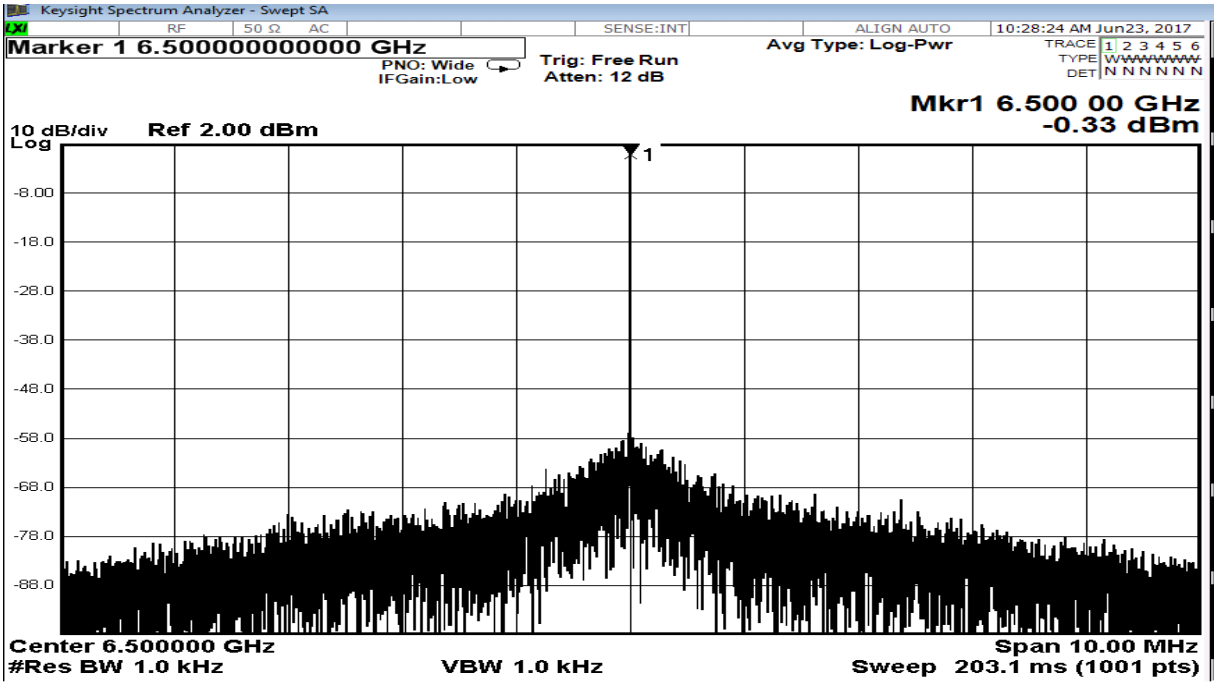


Figure 5.4: Measured Phase Noise Performance at 6 GHz



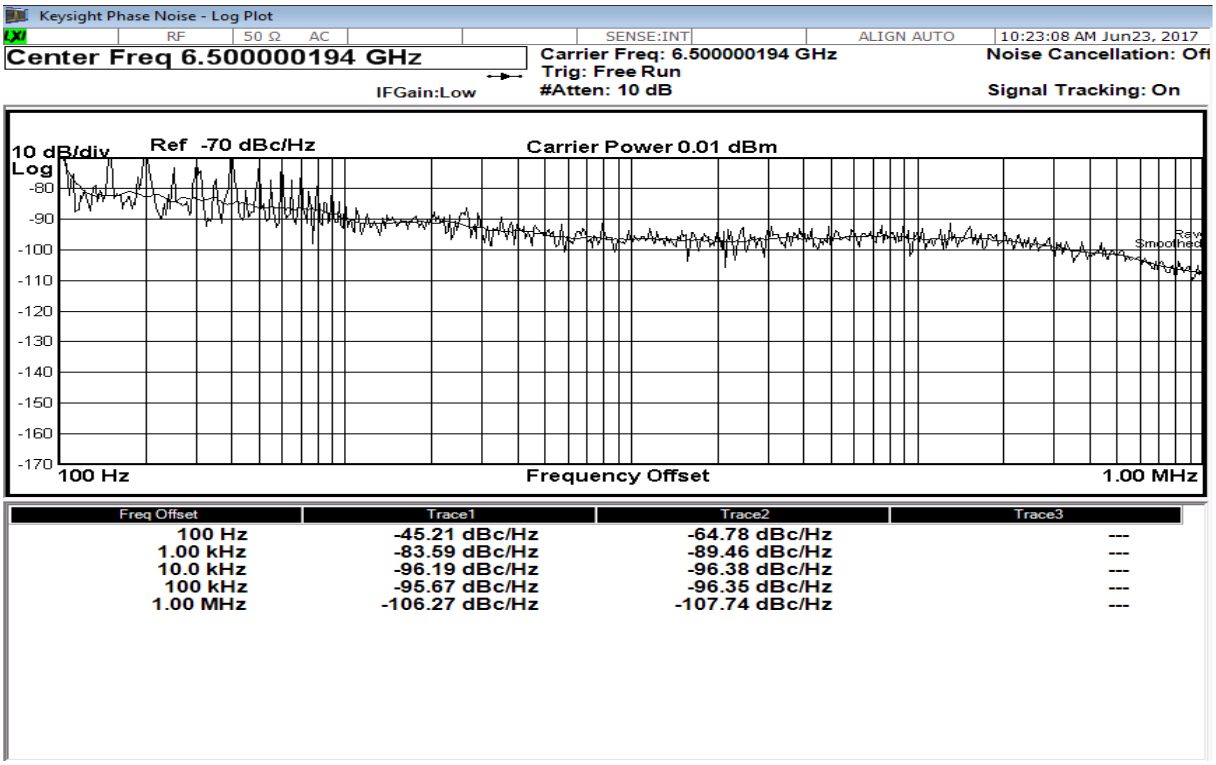
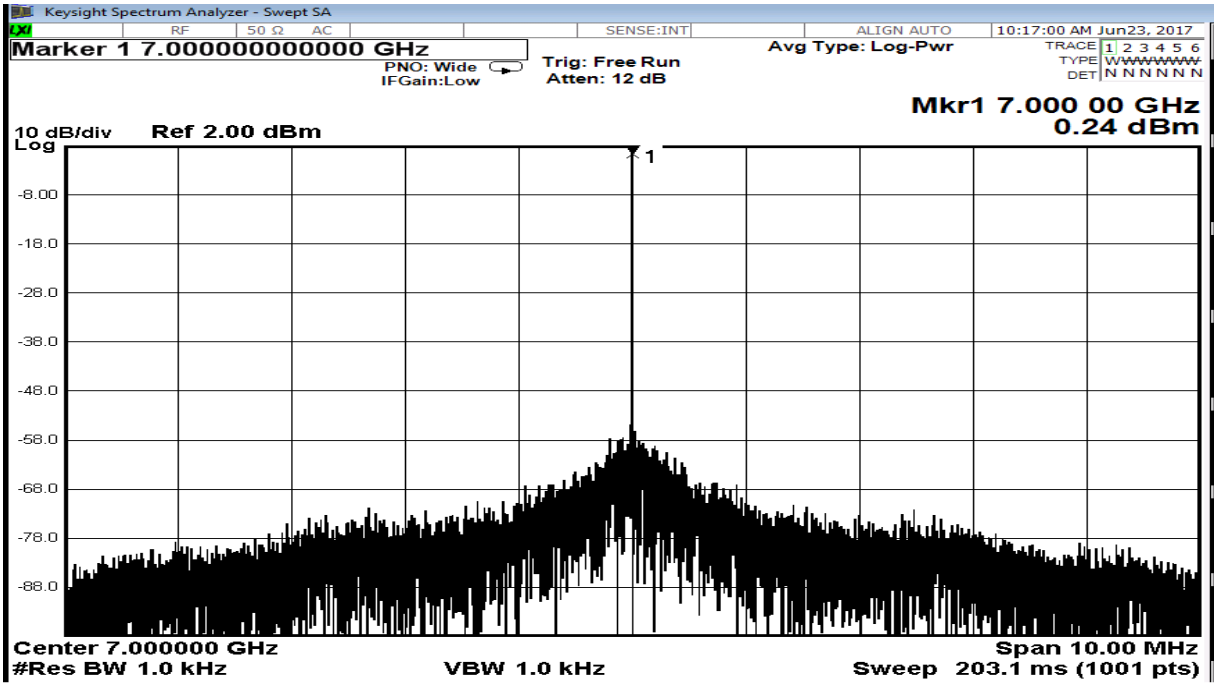


Figure 5.5: Measured Phase Noise Performance at 6.5 GHz



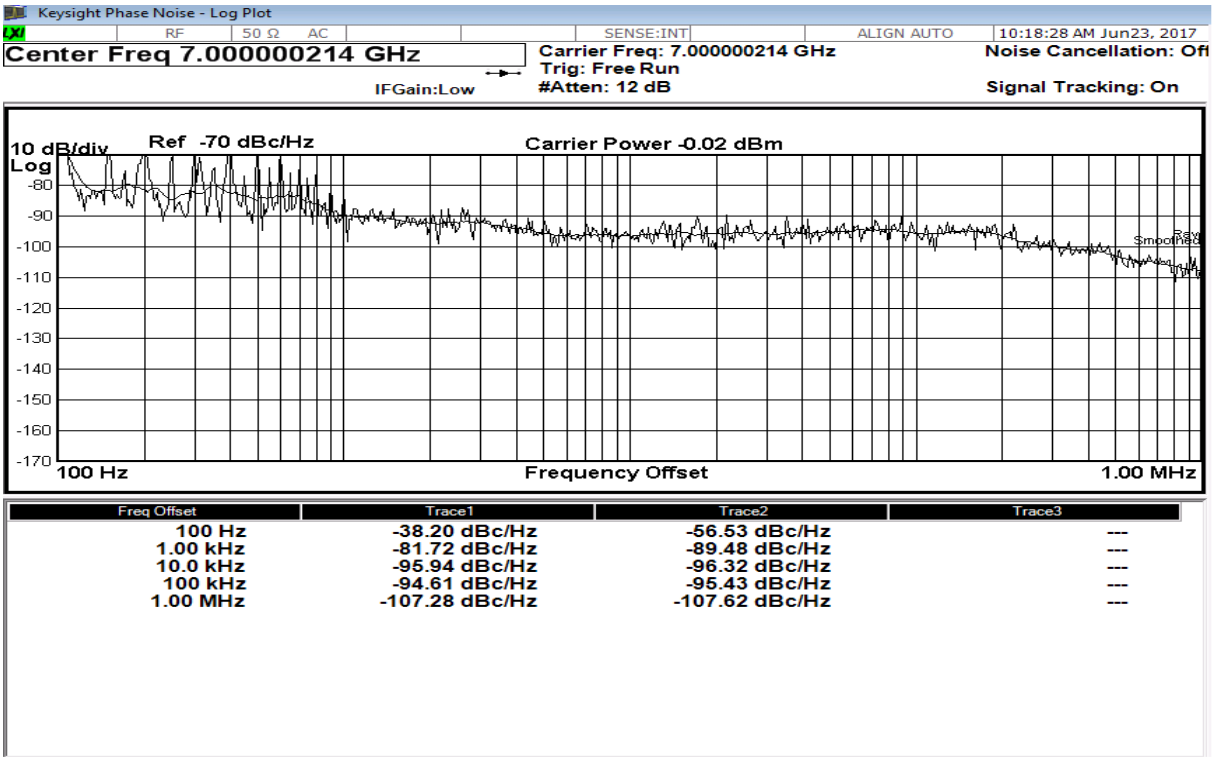
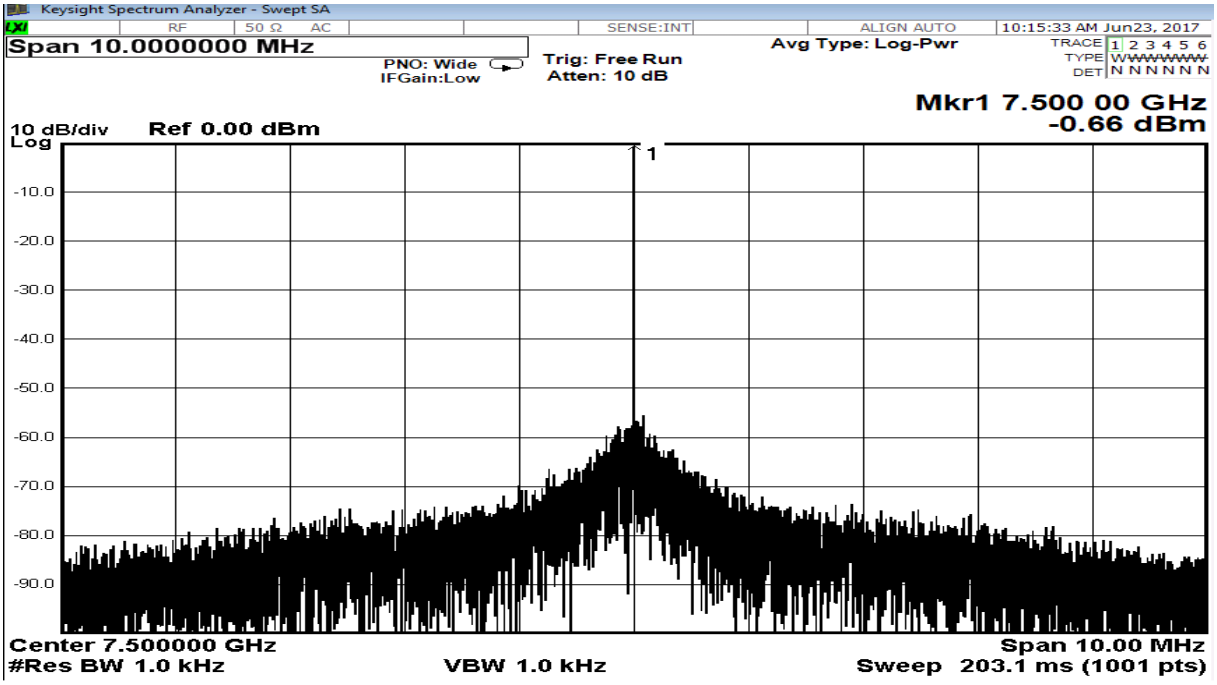


Figure 5.6: Measured Phase Noise Performance at 7 GHz



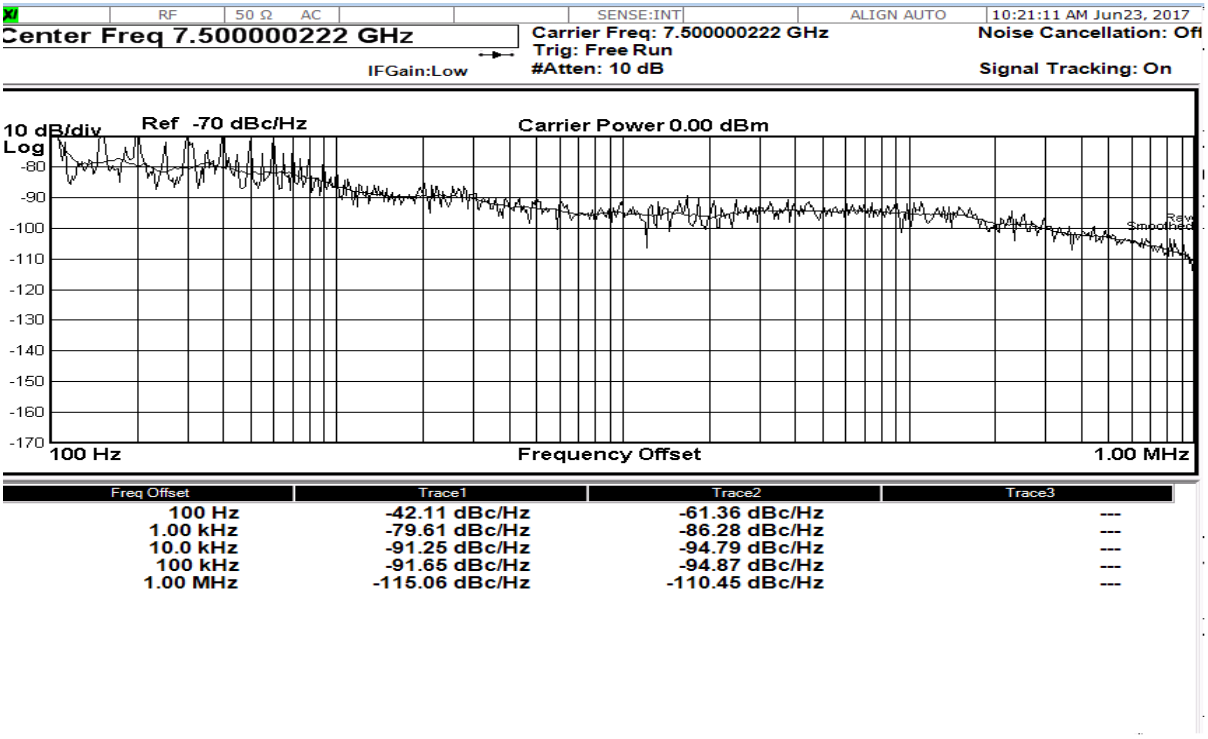


Figure 5.7: Measured Phase Noise Performance at 7.5 GHz

Phase noise that measured from spectrum analyzer is differnet from the phase noise simulated result from Advanced Design System. Spectrum analyzer phase noise results is some what degraded than the ADS phase noise result because of complexity in hardware and the power supply phase noise.
Its performance can be improved by taking proper measures, and phase noise that is present in power supply can be reduced to get better phase noise performance or even eliminated to get phase noise performance similar to Advance Design System Simulation.

Chapter 6

Conclusion and Future Work

The use of oven controlled crystal oscillator OCXO as a reference oscillator will give the better phase noise performance. The prototype here is just the first implementation of low noise frequency synthesizer, its performance can be improved. The intention behind this project is to made a frequency synthesizer that can be used in worst possible condition. Several designs were tested in ADS in the beginning and the simulation with best result is selected.
One of the important application of frequency synthesizer is in radio receivers. Radio receivers are mounted in aircrafts, helicopters and ships. Ships and Aircrafts undergoes lot of vibration and as we demonstrated in the thesis, vibration is the main cause of degradation in phase noise performancce of synthesizer which in results degrade the overall performance of the receiver. In worst condition phase noise in ships and aircrafts degrade by 20dB and 40dB for ships and aircrafts respectively. The proposed frequency synthesizer here will work just fine in under those condition.
Further performance can be improved in this prototype. The frequency synthesizer in this project is made in such a way that by only removing the Coaxial Resonator VCO in loop-1 the performance can be drastically improved. We can use sapphire loaded cavity oscillator SLCO or opto-electronic oscillator OEC instead of Coaxial resonator oscillator to improve the phase noise performance of overall circuit.

Appendix A

Datasheets

A.1 Voltage Controlled Oscillators

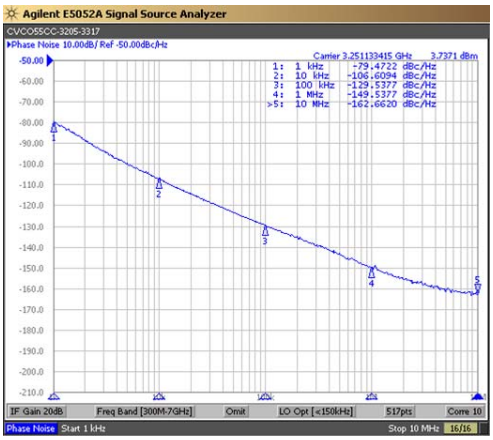
CRYSTEK MICROWAVE
A DIVISION OF CRYSTEK CORPORATION

Coaxial Resonator Oscillator-CRO
CVCO55CC-3205-3317

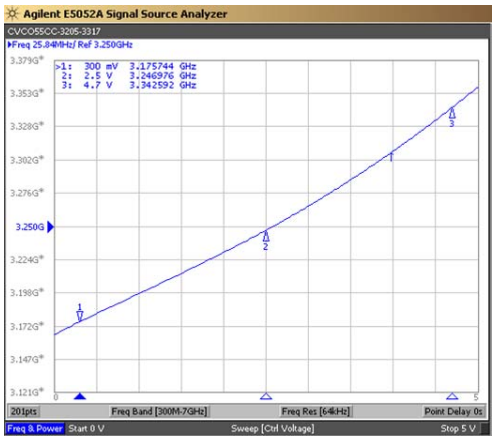
PERFORMANCE SPECIFICATION	MIN	TYP	MAX	UNITS
Lower Frequency:			3205	MHz
Upper Frequency:	3317			MHz
Tuning Voltage:	0.3		4.7	VDC
Supply Voltage:	4.75	5.0	5.25	VDC
Output Power:	0	+3.0	+6.0	dBm
Supply Current:		40		mA
Harmonic Suppression (2nd Harmonic)		-15		dBc
Pushing:			2.0	MHz/V
Pulling, all Phases:			3.0	MHz pk-pk
Tuning Sensitivity:		40		MHz/V
Phase Noise @ 10kHz offset:		-107	-102	dBc/Hz
Phase Noise @ 100kHz offset:		-127		dBc/Hz
Load Impedance:		50		Ω
Input Capacitance:			15	pF
Operating Temperature Range:	-40		+85	°C
Storage Temperature Range:	-45		+90	°C

RoHS Compliant

Phase Noise (1 Hz BW, Typical)



Tuning Curve (Typical)



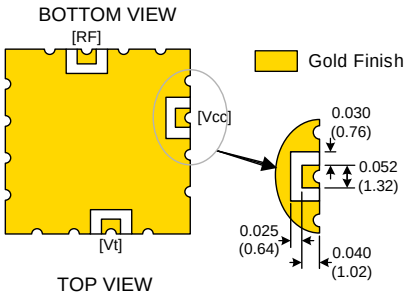
Product Control:			
Crystek Part Number:	CVCO55CC-3205-3317	Release Date:	06-May-2014
Revision Level:	C	Responsible:	C. Vales

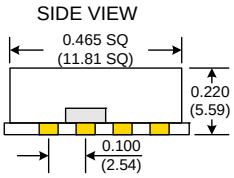
Page 1 of 2

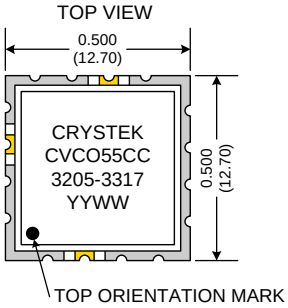
CRYSTEK CORPORATION
12730 Commonwealth Drive • Fort Myers, Florida 33913
Phone: 239-561-3311 • 800-237-3061
Fax: 239-561-1025 • www.crystek.com

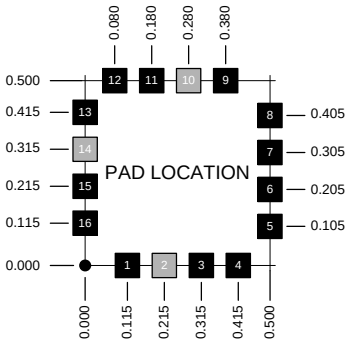
Coaxial Resonator Oscillator-CRO
CVCO55CC-3205-3317

CRYSTEK MICROWAVE
A DIVISION OF CRYSTEK CORPORATION





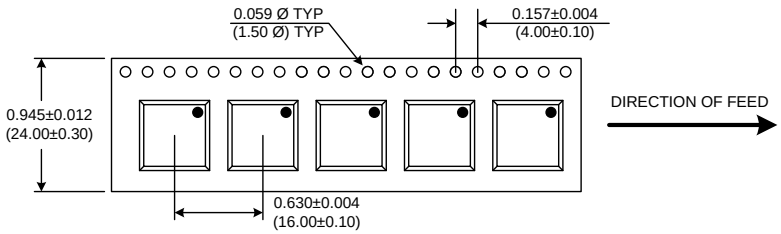




Pad	Connection
2	Vt
10	RF-OUTPUT
14	Vcc
Others	GROUND

- Unless otherwise specified, Dimensions are in: IN / (mm)
- Pad Location Dimensions are in: Inches

TAPE AND REEL



Drawing not to scale

Product Control:			
Crystek Part Number:	CVCO55CC-3205-3317	Release Date:	06-May-2014
Revision Level:	C	Responsible:	C. Vales

Specification is subject to change without notice

CRYSTEK CORPORATION
12730 COMMONWEALTH DRIVE • FORT MYERS, FLORIDA 33913
PHONE: 239-561-3311 • 800-237-3061
FAX: 239-561-1025 • WWW.CRYSTEK.COM

11.41 GHz to 12.62 GHz MMIC VCO with Half Frequency Output

Data Sheet **HMC1166**

FEATURES

- Dual output frequency range
  - f_{OUT} = 11.41 GHz to 12.62 GHz
  - $f_{OUT}/2$ = 5.705 GHz to 6.31 GHz
- Output power (P_{OUT}): 11 dBm
- Single-sideband (SSB) phase noise: −115 dBc/Hz at 100 kHz
- No external resonator needed
- RoHS compliant, 5 mm × 5 mm, 32-lead LFCSP: 25 mm²

APPLICATIONS

- Point to point and multipoint radios
- Test equipment and industrial controls
- Very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

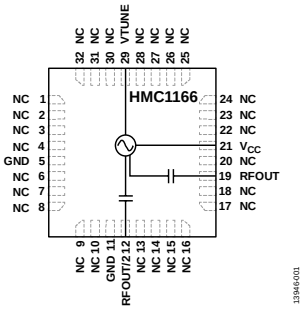


Figure 1.

GENERAL DESCRIPTION

The HMC1166 is a monolithic microwave integrated circuit (MMIC), voltage controlled oscillator (VCO) that integrates a resonator, a negative resistance device, and a varactor diode, and features a half frequency output.

Because of the monolithic construction of the oscillator, the output power and phase noise performance are excellent over temperature.

The output power is 11 dBm typical from a 5 V supply voltage. The VCO is housed in a RoHS compliant LFCSP and requires no external matching components.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

SPECIFICATIONS

T_A = −40°C to +85°C, V_{CC} = 5 V, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY					
Range					
Output Frequency (f_{OUT})	11.41		12.62	GHz	
Half Output Frequency (f_{OUT}/2)	5.705		6.31	GHz	
Drift Rate		1.0		MHz/°C	
Pulling		2		MHz p-p	Pulling into a 2.0:1 voltage standing wave ratio (VSWR)
Pushing		5		MHz/V	At VTUNE = 5 V
OUTPUT POWER (P_{OUT})					
RFOUT	7	11	15	dBm	
RFOUT/2	0	4	9	dBm	
Supply Current (I_{CC})		200		mA	V_{CC} = 4.75 V
		220	270	mA	V_{CC} = 5.00 V
		240		mA	V_{CC} = 5.25 V
HARMONICS, SUBHARMONICS					
1/2		40		dBc	
3/2		30		dBc	
Second		20		dBc	
Third		26		dBc	
TUNING					
Voltage (VTUNE)	2		13	V	
Sensitivity	75		325	MHz/V	
Tune Port Leakage Current			10	µA	VTUNE = 13 V
OUTPUT RETURN LOSS		5		dB	
SSB PHASE NOISE					
10 kHz Offset		−89	−85	dBc/Hz	
100 kHz Offset		−115	−112	dBc/Hz	

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

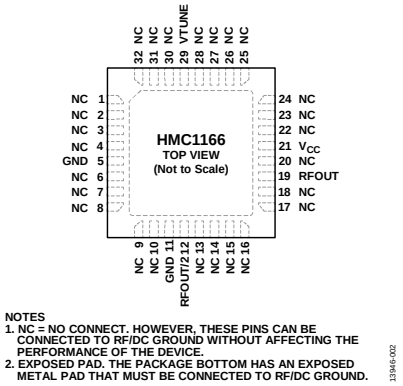


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4, 6 to 10, 13 to 18, 20, 22 to 28, 30 to 32	NC	No Connect. However, these pins can be connected to RF/dc ground without affecting the performance of the device.
5, 11	GND	Ground. These pins must be connected to RF/dc ground.
12	RFOUT/2	Half Radio Frequency Output. This pin is ac-coupled.
19	RFOUT	Radio Frequency Output. This pin is ac-coupled.
21	V_{CC}	Supply Voltage (5 V).
29	VTUNE	Control Voltage and Modulation Input. The modulation bandwidth is dependent on the drive source impedance.
	EP	Exposed Pad. The package bottom has an exposed metal pad that must be connected to RF/dc ground.

TYPICAL PERFORMANCE CHARACTERISTICS

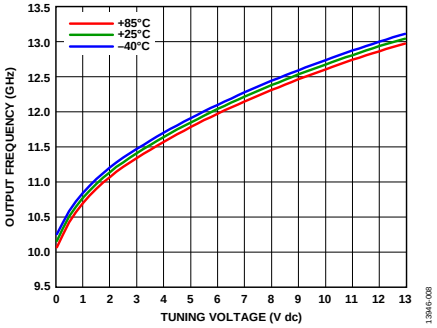


Figure 8. Output Frequency vs. Tuning Voltage

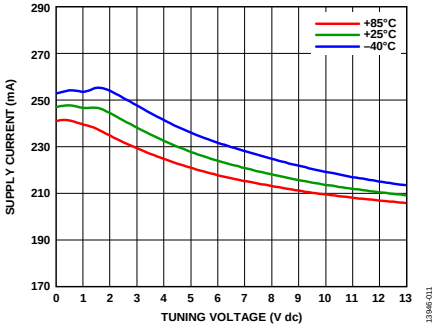


Figure 11. Supply Current (I_{CC}) vs. Tuning Voltage

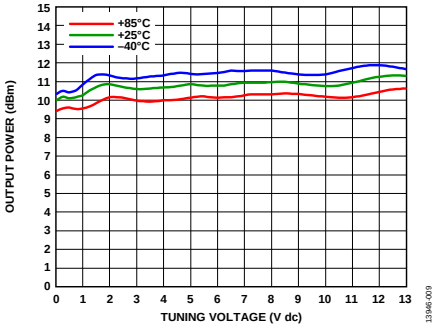


Figure 9. Output Power vs. Tuning Voltage

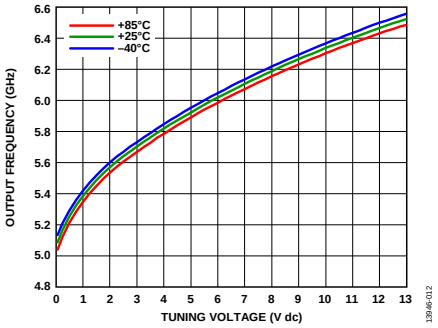


Figure 12. RFOUT/2 Output Frequency vs. Tuning Voltage

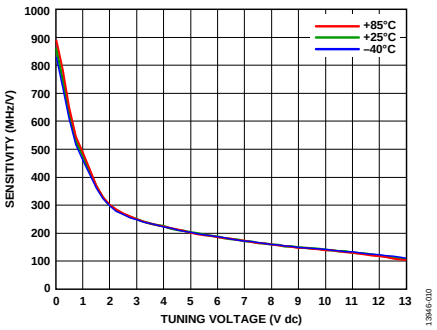


Figure 10. Sensitivity vs. Tuning Voltage

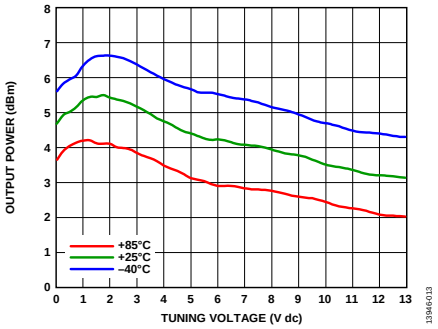


Figure 13. RFOUT/2 Output Power vs. Tuning Voltage

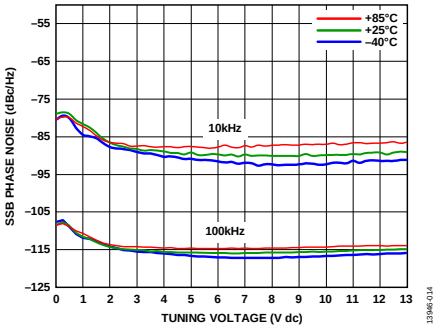


Figure 14. SSB Phase Noise vs. Tuning Voltage

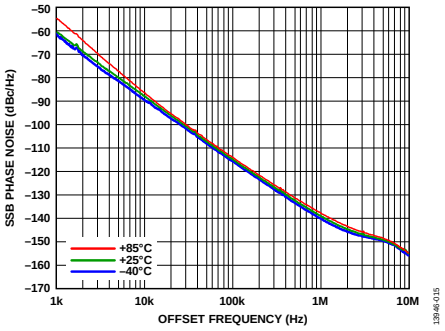


Figure 15. SSB Phase Noise vs. Offset Frequency at VTUNE = 5 V

HMC431LP4 / 431LP4E

v04.1106

MMIC VCO w/ BUFFER AMPLIFIER, 5.5 - 6.1 GHz

Typical Applications

Low noise MMIC VCO w/Buffer Amplifier for C-Band applications such as:

- 802.11a & HiperLAN WLAN
- VSAT Radios
- UNII & Point-to-Point Radios

Features

Pout: +2 dBm

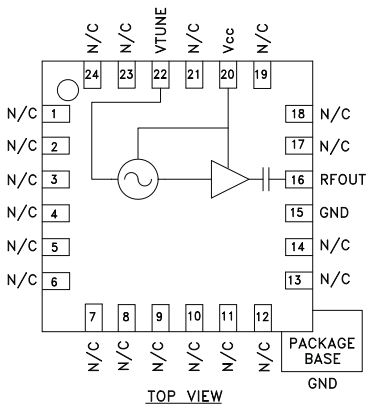
Phase Noise: -102 dBc/Hz @100 kHz

No External Resonator Needed

Single Supply: 3V @ 27 mA

16mm² Leadless SMT Package

Functional Diagram



General Description

The HMC431LP4 & HMC431LP4E are GaAs InGaP Heterojunction Bipolar Transistor (HBT) MMIC VCOs with integrated resonators, negative resistance devices, varactor diodes, and buffer amplifiers. The VCO's phase noise performance is excellent over temperature, shock, vibration and process due to the oscillator's monolithic structure. Power output is 2 dBm typical from a 3V supply voltage. The voltage controlled oscillator is packaged in a low cost leadless QFN 4 x 4 mm surface mount package.

Electrical Specifications, T_A = +25° C, Vcc = +3V

Parameter	Min.	Typ.	Max.	Units
Frequency Range		5.5 - 6.1		GHz
Power Output	-1	2		dBm
SSB Phase Noise @ 100 kHz Offset, Vtune= +5V @ RF Output		-102		dBc/Hz
Tune Voltage (Vtune)	0		10	V
Supply Current (Icc) (Vcc= 3.0V)		27		mA
Tune Port Leakage Current			10	µA
Output Return Loss		6		dB
Harmonics 2nd 3rd		 -15 -30		 dBc dBc
Pulling (into a 2.0:1 VSWR)		9		MHz pp
Pushing @ Vtune= +5V		12		MHz/V
Frequency Drift Rate		0.8		MHz/°C

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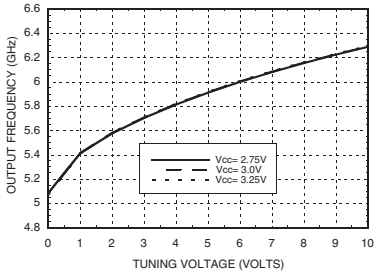
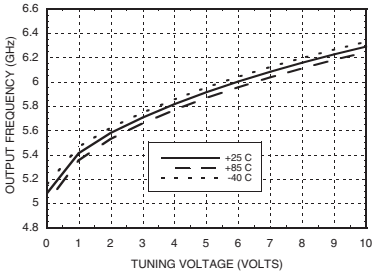
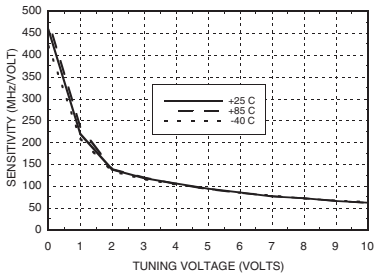
Frequency vs. Tuning Voltage, T= 25°C



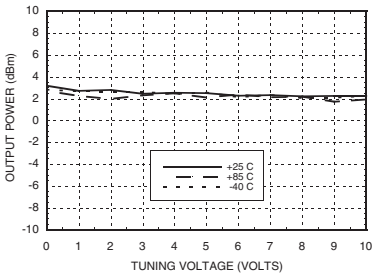
Frequency vs. Tuning Voltage, Vcc= +3V



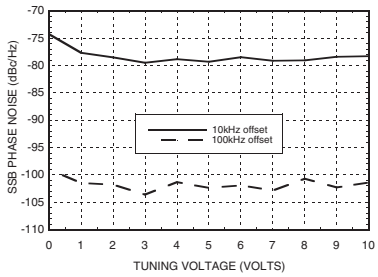
Sensitivity vs. Tuning Voltage, Vcc= +3V



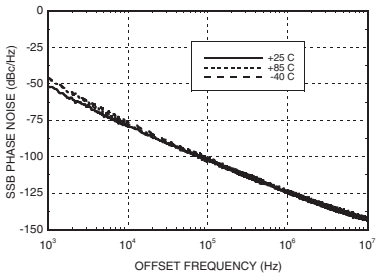
Output Power vs. Tuning Voltage, Vcc= +3V



Phase Noise vs. Tuning Voltage



Typical SSB Phase Noise @ Vtune= +5V



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HMC431LP4 / 431LP4E

v04.1106

MMIC VCO w/ BUFFER AMPLIFIER, 5.5 - 6.1 GHz

Absolute Maximum Ratings

Vcc	+3.5 Vdc
Vtune	0 to +11V
Channel Temperature	135 °C
Continuous Pdiss (T = 85°C) (derate 6.28 mW/°C above 85°C)	565 W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

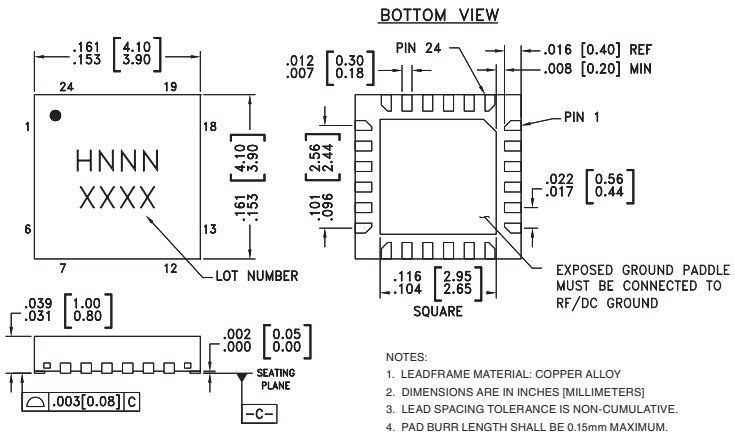
Typical Supply Current vs. Vcc

Vcc (V)	Icc (mA)
2.75	19
3.0	27
3.25	34

Note: VCO will operate over full voltage range shown above.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOT FOR SUGGESTED LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC431LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H431 XXXX
HMC431LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H431 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

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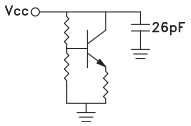
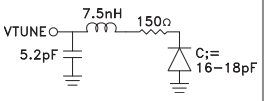
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1 - 14, 17 - 19, 21, 23, 24	N/C	No Connection	
15	GND	This pin must be connected to RF & DC ground.	
16	RFOUT	RF output (AC coupled)	
20	Vcc	Supply Voltage Vcc= 3V	
22	VTUNE	Control Voltage Input. Modulation port bandwidth dependent on drive source impedance.	
	GND	Package bottom has an exposed metal paddle that must be RF & DC grounded.	

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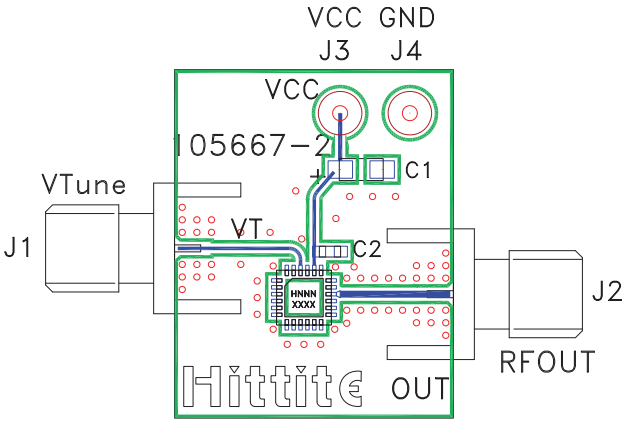
Evaluation PCB



List of Materials for Evaluation PCB 105706 [1]

Item	Description
J1 - J2	PCB Mount SMA RF Connector
J3 - J4	DC Pin
C1	4.7 µF Tantalum Capacitor
C2	10,000 pF Capacitor, 0603 Pkg.
U1	HMC431LP4 / HMC431LP4E VCO
PCB [2]	105667 Eval Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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Application Support: Phone: 1-800-ANALOG-D

HMC466LP4 / 466LP4E

v03.1109

MMIC VCO w/ BUFFER AMPLIFIER, 6.1 - 6.72 GHz

Typical Applications

Low noise MMIC VCO w/Buffer Amplifier for:

- VSAT & Microwave Radio
- CATV & Broadcast Relays
- Test Equipment & Industrial Controls
- Military

Features

Pout: +4.5 dBm

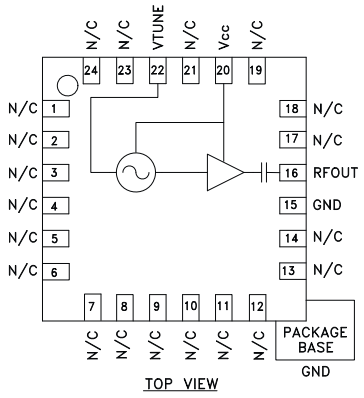
Phase Noise: -101 dBc/Hz @100 KHz

No External Resonator Needed

Single Supply: +3V @ 31 mA

24 Lead 4x4mm QFN Package: 16 mm^2

Functional Diagram



General Description

The HMC466LP4 & HMC466LP4E are GaAs InGaP Heterojunction Bipolar Transistor (HBT) MMIC VCOs with integrated resonators, negative resistance devices, varactor diodes, and buffer amplifiers. Covering 6.1 to 6.72 GHz, the VCO's phase noise performance is excellent over temperature, shock, vibration and process due to the oscillator's monolithic structure. Power output is 4.5 dBm typical from a single supply of 3V @31mA. The voltage controlled oscillator is packaged in a low cost leadless QFN 4 x 4 mm surface mount package.

Electrical Specifications, T_A = +25° C, Vcc = +3V

Parameter	Min.	Typ.	Max.	Units
Frequency Range		6.1 - 6.72		GHz
Power Output	1.5	4.5		dBm
SSB Phase Noise @ 100 kHz Offset, Vtune= +5V @ RF Output		-101		dBc/Hz
Tune Voltage (Vtune)	0		10	V
Supply Current (Icc) (Vcc = +3V)		31		mA
Tune Port Leakage Current			10	µA
Output Return Loss		7		dB
Harmonics 2nd 3rd		 -13 -24		 dBc dBc
Pulling (into a 2.0:1 VSWR)		11		MHz pp
Pushing @ Vtune= +5V		30		MHz/V
Frequency Drift Rate		0.8		MHz/°C

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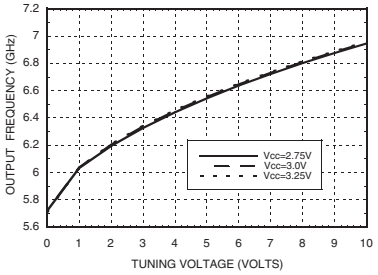
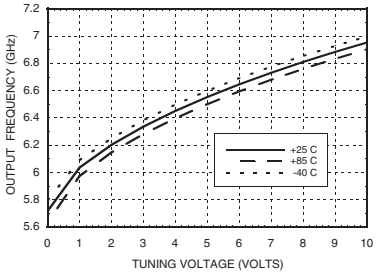
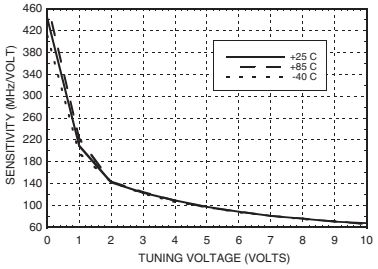
Frequency vs. Tuning Voltage, T= 25°C



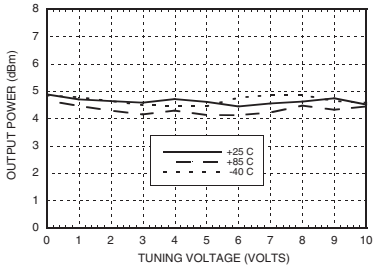
Frequency vs. Tuning Voltage, Vcc= +3V



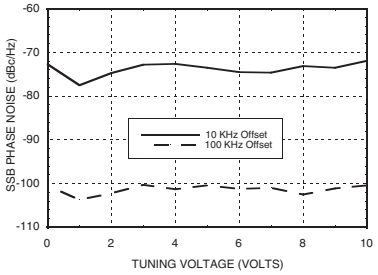
Sensitivity vs. Tuning Voltage, Vcc= +3V



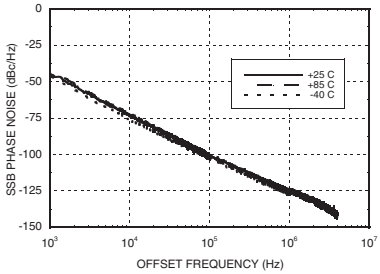
Output Power vs. Tuning Voltage, Vcc= +3V



Phase Noise vs. Tuning Voltage



Typical SSB Phase Noise @ Vtune= +5V



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Application Support: Phone: 1-800-ANALOG-D

HMC466LP4 / 466LP4E

v03.1109

MMIC VCO w/ BUFFER AMPLIFIER, 6.1 - 6.72 GHz

Absolute Maximum Ratings

Vcc	+3.5 Vdc
Vtune	0 to +11V
Channel Temperature	135 °C
Continuous Pdiss (T = 85°C) (derate 6.28 mW/°C above 85°C)	5.65 W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

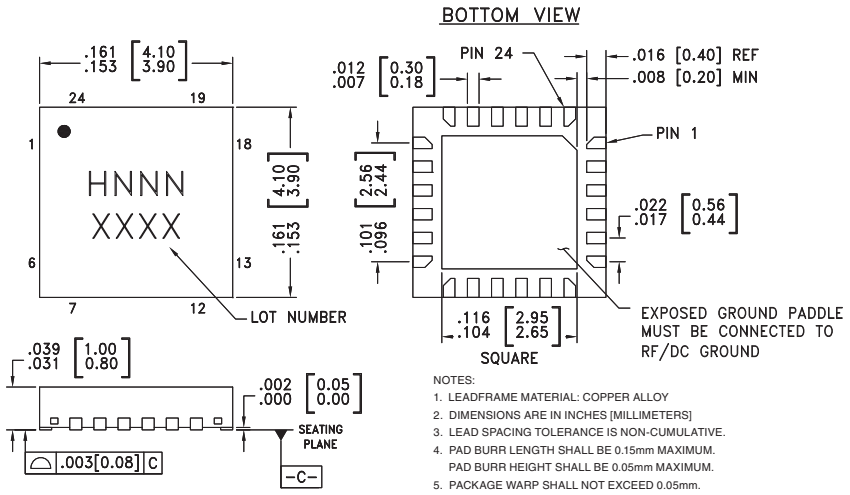
ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Typical Supply Current vs. Vcc

Vcc (V)	Icc (mA)
2.75	22
3.0	31
3.25	41

Note: VCO will operate over full voltage range shown above.

Outline Drawing



NOTES:
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOT FOR SUGGESTED LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC466LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H466 XXXX
HMC466LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H466 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

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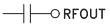
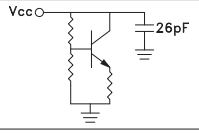
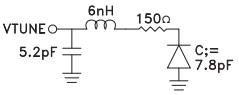
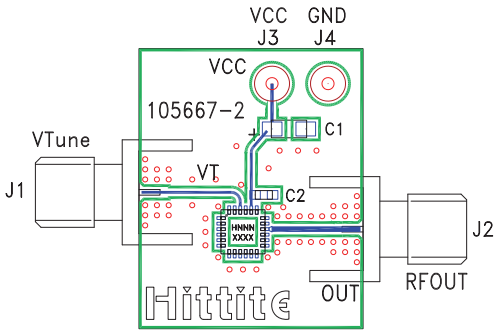
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1- 14, 17 - 19, 21, 23, 24	N/C	No Connection	
15	GND	This pin must be connected to RF & DC ground. Package bottom has an exposed metal paddle that must be RF & DC grounded.	
16	RFOUT	RF output (AC coupled)	
20	Vcc	Supply Voltage Vcc= 3V	
22	VTUNE	Control Voltage Input. Modulation port bandwidth dependent on drive source impedance.	

Evaluation PCB



List of Materials for Evaluation PCB 105706 [1]

Item	Description
J1 - J2	PCB Mount SMA RF Connector
J3 - J4	DC Pin
C1	4.7 µF Tantalum Capacitor
C2	10,000 pF Capacitor, 0603 Pkg.
U1	HMC466LP4 / HMC466LP4E VCO
PCB [2]	105667 Eval Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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HMC586LC4B

v03.0514

WIDEBAND MMIC VCO w/ BUFFER AMPLIFIER, 4 - 8 GHz

Typical Applications

Low Noise wideband MMIC VCO is ideal for:

- Industrial/Medical Equipment
- Test & Measurement Equipment
- Military Radar, EW & ECM

Features

Wide Tuning Bandwidth

Pout: +5 dBm

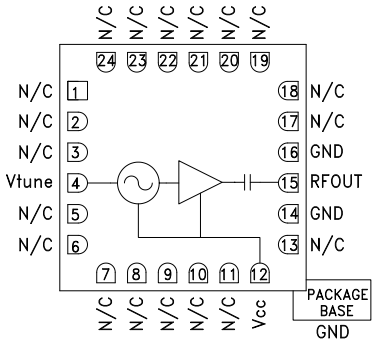
Low SSB Phase Noise: -100 dBc/Hz @100 kHz

No External Resonator Needed

Single Positive Supply: +5V @ 55 mA

RoHS Compliant 4 x 4 mm SMT Package

Functional Diagram



General Description

The HMC586LC4B is a wideband GaAs InGaP Voltage Controlled Oscillator which incorporates the resonator, negative resistance device, and varactor diode. Output power and phase noise performance are excellent over temperature due to the oscillator's monolithic construction. The Vtune port accepts an analog tuning voltage from 0 to +18V. The HMC586LC4B VCO operates from a single +5V supply, consumes only 55 mA of current, and is housed in a RoHS compliant SMT package. This wideband VCO uniquely combines the attributes of ultra small size, low phase noise, low power consumption, and wide tuning range.

Electrical Specifications, T_A = +25° C, Vcc = +5V

Parameter	Min.	Typ.	Max.	Units
Frequency Range		4 - 8		GHz
Power Output	2	5		dBm
SSB Phase Noise @ 100 kHz Offset		-100		dBc/Hz
SSB Phase Noise @ 10 kHz Offset		-75		dBc/Hz
Tune Voltage (Vtune)	0		18	V
Supply Current (Icc) (Vcc = +5.0V)	40		75	mA
Tune Port Leakage Current (Vtune = +15V)			10	µA
Output Return Loss		7		dB
2nd Harmonic		-14		dBc
Pulling (into a 2.0:1 VSWR)		4		MHz pp
Pushing @ Vtune= +5V		40		MHz/V
Frequency Drift Rate		0.8		MHz/°C

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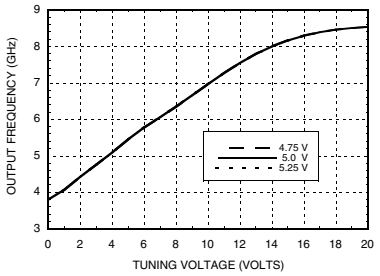
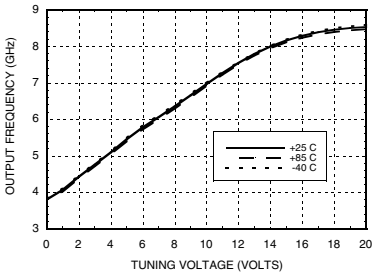
WIDEBAND MMIC VCO w/ BUFFER AMPLIFIER, 4 - 8 GHz

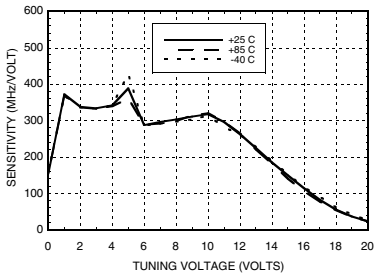
Frequency vs. Tuning Voltage, Vcc = +5V



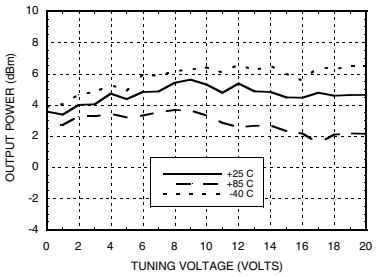
Frequency vs. Tuning Voltage, T = +25 C



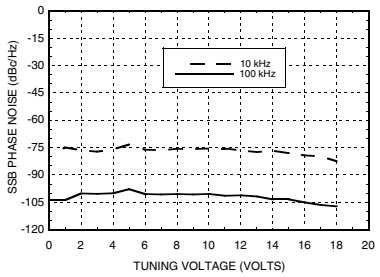
Sensitivity vs. Tuning Voltage, Vcc= +5V



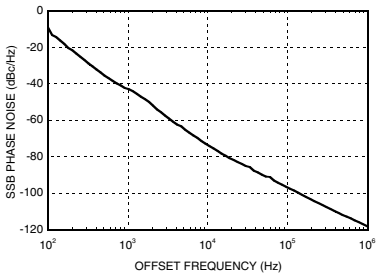
Output Power vs. Tuning Voltage, Vcc= +5V



SSB Phase Noise vs. Tuning Voltage



Typical SSB Phase Noise @ Vtune= +5V



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Application Support: Phone: 1-800-ANALOG-D

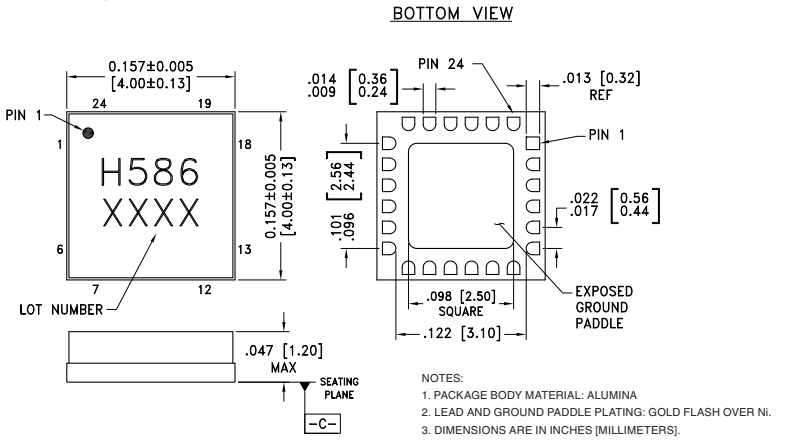
WIDEBAND MMIC VCO w/ BUFFER AMPLIFIER, 4 - 8 GHz

Absolute Maximum Ratings

Vcc	+5.5 Vdc
Vtune	0 to +22V
Junction Temperature	135 °C
Continuous Pdiss (T = 85°C) (derate 12.5 mW/°C above 85°C)	625 mW
Thermal Resistance (junction to ground paddle)	80 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING: GOLD FLASH OVER Ni.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC586LC4B	Alumina, White	Gold over Nickel	MSL3 [1]	H586 XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

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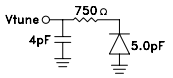
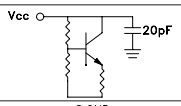
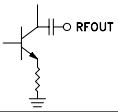
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1 - 3, 5 - 11, 13, 17 - 24	N/C	No Connection. These pins may be connected to RF/DC ground. Performance will not be affected.	
4	Vtune	Control Voltage and Modulation Input. Modulation bandwidth dependent on drive source impedance. See "Determining the FM Bandwidth of a Wideband Varactor Tuned VCO" application note.	
12	Vcc	Supply Voltage Vcc= +5V	
14, 16	GND	Package bottom has an exposed metal paddle that must also be RF & DC grounded.	
15	RFOUT	RF output (AC coupled)	

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A.2 Phase Frequency Detector

ANALOG DEVICES

HMC439QS16G / 439QS16GE

v02.0705

HBT DIGITAL PHASE-FREQUENCY DETECTOR, 10 - 1300 MHz

Typical Applications

This Phase Frequency Detector is a key component in low phase noise frequency synthesis applications such as:

- Point-to-Point Radios
- Satellite Communication Systems
- Military Applications
- Sonet Clock Generation

Features

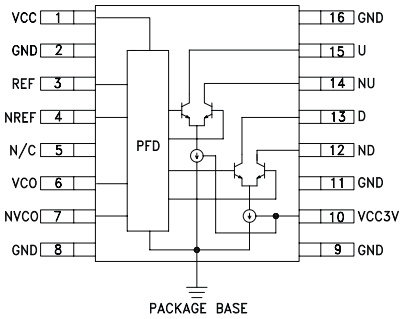
Ultra Low SSB Phase Noise Floor:
-153 dBc/Hz @ 10 kHz offset @ 100 MHz
Input up to 1300 MHz Fin.

Differential Input/Single Ended Output

Open Collector Output Buffer Amplifiers

QSOP16G SMT Package: 29.4 mm^2

Functional Diagram



General Description

The HMC439QS16G & HMC439QS16GE are digital phase-frequency detectors intended for use in low noise phase-locked loop applications for inputs from 10 to 1300 MHz. Its combination of high frequency of operation along with its ultra low phase noise floor make possible synthesizers with wide loop bandwidth and low N resulting in fast switching and very low phase noise. When used in conjunction with a differential loop amplifier, the HMC439QS16G & HMC439QS16GE generate output voltages that can be used to phase lock a VCO to a reference oscillator. The device is packaged in a low cost, surface mount 16 lead QSOP package with an exposed base for improved RF and thermal performance.

Electrical Specifications, T_A = +25° C, Vcc= 5V

Parameter	Conditions	Min.	Typ.	Max.	Units
Maximum Input Frequency		1300			MHz
Minimum Input Frequency	Sine Wave Input			10	MHz
Input Power Range	Fin= 10 to 1300 MHz	-10		+10	dBm
Output Voltage			2000		mV, Pk - Pk
SSB Phase Noise	@ 10 kHz Offset with 100 MHz Input & Pin= 0 dBm		-153		dBc/Hz
Supply Current (Icc)			96		mA

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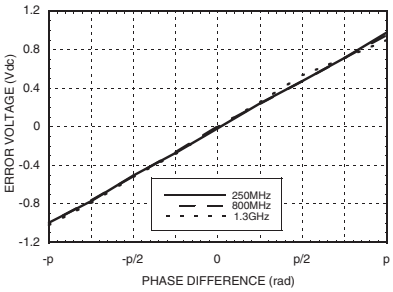
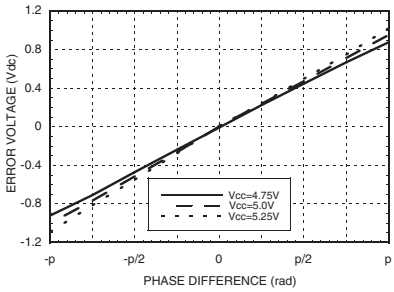
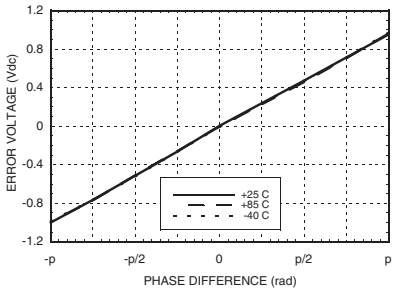
Error Voltage vs. Frequency, Pin= 0 dBm*



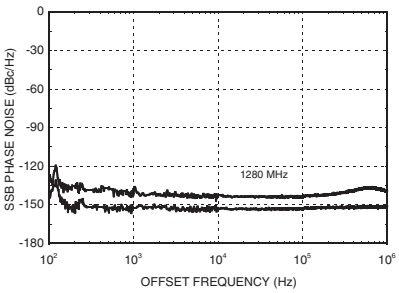
Error Voltage vs. Supply Voltage, Pin= 0 dBm, Fin= 250 MHz*



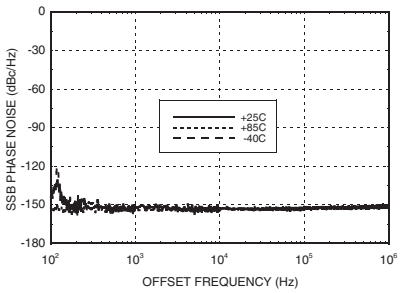
Error Voltage vs. Temperature, Pin= 0 dBm, Fin= 250 MHz*



SSB Phase Noise Performance, Pin= 0 dBm, T= 25 °C



SSB Phase Noise Performance, Pin= 0 dBm, Fin= 100 MHz



** See Gain & Error Voltage Test Circuit herein.*

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Application Support: Phone: 1-800-ANALOG-D

HMC439QS16G / 439QS16GE

v02.0705

HBT DIGITAL PHASE-FREQUENCY DETECTOR, 10 - 1300 MHz

Absolute Maximum Ratings

RF Input (Vcc= +5V)	+13 dBm
Supply Voltage (Vcc)	+5.5V
Channel Temperature (Tc)	135 °C
Continuous Pdiss (T = 85 °C) (derate 47.2 mW/° C above 85 °C)	4.25 W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Typical Supply Current vs. Vcc

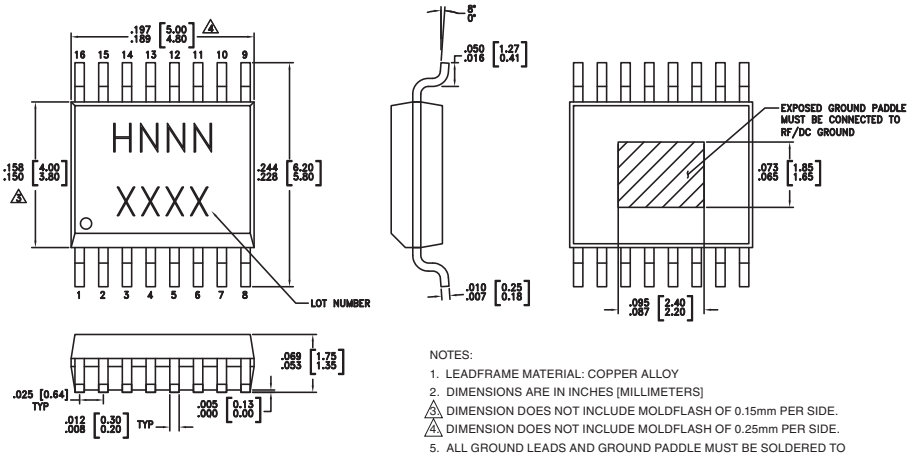
Vcc (Vdc)	Icc (mA)
4.8	90
5.0	96
5.2	102

Note: Detector will work over full voltage range above.

Typical DC Characteristics @ Vcc = +5V

Symbol	Characteristics	+25C			Units
		Min.	Typ.	Max.	
Icc	Power Supply Current	90	96	102	mA
Voh	Output High Voltage	5.0	5.0	5.0	V
Vol	Output Low Voltage	2.9	3	3.1	V

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
4. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
5. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC439QS16G	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H439 XXXX
HMC439QS16GE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H439 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

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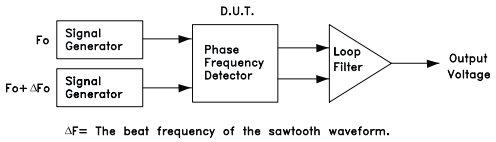
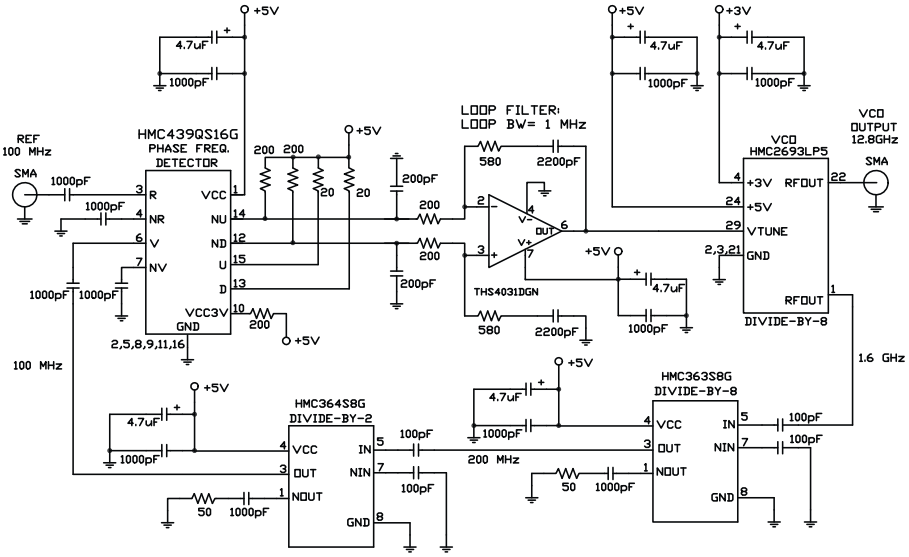
Gain & Error Voltage Test Circuit:

Gain & Error Voltage data taken using test circuit below. Loop filter gain has been subtracted from the result.



Typical PLL Application Circuit using HMC439QS16G

PLL application shown for a 12.8 GHz Fout. Contact HMC to discuss your specific application.



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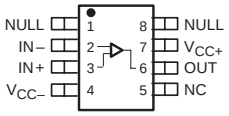
A.3 OPAMP

THS4031, THS4032
100-MHz LOW-NOISE HIGH-SPEED AMPLIFIERS

SLOS224C – JULY 1999 – REVISED APRIL 2000

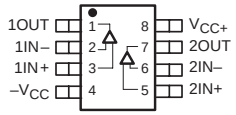
- **Ultra-low 1.6 nV/√Hz Voltage Noise**
- **High Speed**
  - **100 MHz Bandwidth (G = 2 (–1), –3 dB)**
  - **100 V/μs Slew Rate**
- **Stable in Gains of 2 (–1) or Greater**
- **Very Low Distortion**
  - **THD = –72 dBc (f = 1 MHz, R_L = 150 Ω)**
  - **THD = –90 dBc (f = 1 MHz, R_L = 1 kΩ)**
- **Low 0.5 mV (Typ) Input Offset Voltage**
- **90 mA Output Current Drive (Typical)**
- **±5 V to ±15 V Typical Operation**
- **Available in Standard SOIC, MSOP PowerPAD™, JG, or FK Package**
- **Evaluation Module Available**

THS4031
D, DGN, AND JG PACKAGE
(TOP VIEW)



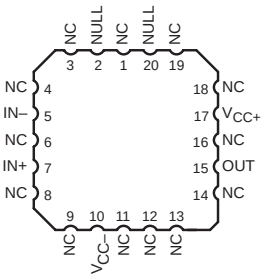
NC – No internal connection

THS4032
D AND DGN PACKAGE
(TOP VIEW)



Cross-Section View Showing
PowerPAD™ Option (DGN)

THS4031
FK PACKAGE
(TOP VIEW)



description

The THS4031 and THS4032 are ultralow-voltage noise, high-speed voltage feedback amplifiers that are ideal for applications requiring low voltage noise, including communication and imaging. The single-amplifier THS4031 and the dual-amplifier THS4032 offer very good ac performance with 100-MHz bandwidth, 100-V/μs slew rate, and 60-ns settling time (0.1%). The THS4031 and THS4032 are stable at gains of 2 (–1) or greater. These amplifiers have a high drive capability of 90 mA and draw only 8.5-mA supply current per channel. With total harmonic distortion (THD) of –72 dBc at f = 1 MHz, the THS4031 and THS4032 are ideally suited for applications requiring low distortion.

Related Devices

DEVICE	DESCRIPTION
THS4011/12	240-MHz Low Distortion High-Speed Amplifiers
THS4021/2	350-MHz Low Noise High-Speed Amplifiers
THS4081/2	175-MHz Low Power High-Speed Amplifiers

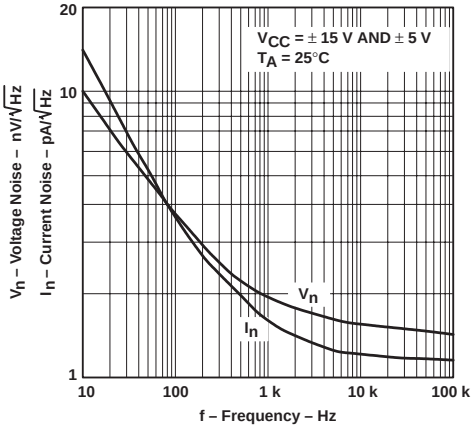
CAUTION: The THS4031 and THS4032 provide ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**VOLTAGE NOISE AND CURRENT NOISE
vs
FREQUENCY**



AVAILABLE OPTIONS

T_A	NUMBER OF CHANNELS	PACKAGED DEVICES					EVALUATION MODULE
		PLASTIC SMALL OUTLINE† (D)	PLASTIC MSOP† (DGN)		CERAMIC DIP (JG)	CHIP CARRIER (FK)	
			DEVICE	SYMBOL			
0°C to 70°C	1	THS4031CD	THS4031CDGN	TIACM	—	—	THS4031EVM
	2	THS4032CD	THS4032CDGN	TIABD	—	—	THS4032EVM
–40°C to 85°C	1	THS4031ID	THS4031IDGN	TIACN	—	—	—
	2	THS4032ID	THS4032IDGN	TIABG	—	—	—
–55°C to 125°C	1	—	—	—	THS4031MJG	THS4031MFK	—

† The D and DGN packages are available taped and reeled. Add an R suffix to the device type (i.e., THS4031CDGNR).

A.4 Frequency Divider

ANALOG DEVICES

0.2 GHz to 8 GHz, GaAs, HBT MMIC, Divide by 8 Prescaler

Data Sheet **HMC434**

FEATURES

- Ultralow SSB phase noise: −150 dBc/Hz typical
- Single-ended input/outputs
- Output power: −2 dBm typical
- Single supply operation: 3 V
- Ultrasmall, surface-mount, 2.90 mm × 2.80 mm, 6-lead SOT-23 package

APPLICATIONS

- DC to C band PLL prescalers
- Very small aperture terminal (VSAT) radios
- Unlicensed national information infrastructure (UNII) and point to point radios
- IEEE 802.11a and high performance radio local area network (HiperLAN) WLAN
- Fiber optics
- Cellular/3G infrastructure

FUNCTIONAL BLOCK DIAGRAM

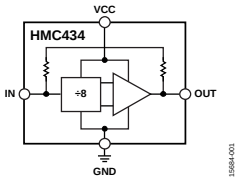


Figure 1.

GENERAL DESCRIPTION

The HMC434 is a low noise, static, divide by 8 prescaler monolithic microwave integrated circuit (MMIC) utilizing indium gallium phosphide/gallium arsenide (InGaP/GaAs) heterojunction bipolar transistor (HBT) technology in an ultrasmall surface-mount 6-lead SOT-23 package.

The HMC434 operates from near dc (square wave) or 200 MHz (sine wave) to 8 GHz input frequency with a single 3 V dc supply.

The HMC434 features single-ended inputs and outputs for reduced component count and cost. The low additive single sideband (SSB) phase noise of −150 dBc/Hz at 100 kHz offset helps the user maintain optimal system noise performance.

Rev. E Document Feedback

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SPECIFICATIONS

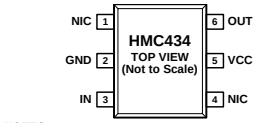
V_{CC} = 3 V, T_A = 25°C, 50 Ω system, unless otherwise noted. P_{IN} is input power.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions / Comments
RADIO FREQUENCY (RF) INPUT					
Frequency[1]	0.2		8	GHz	Sine wave input
Power	−10	0	+10	dBm	f_{IN} = 1.0 GHz to 3.0 GHz
	0	0	10	dBm	f_{IN} = 3.0 GHz to 8.0 GHz
RF OUTPUT					
SSB Phase Noise		−150		dBc/Hz	100 kHz offset, P_{IN} = 0 dBm, f_{IN} = 4.0 GHz
Power	−5	−2		dBm	f_{IN} = 1.0 GHz to 8.0 GHz
REVERSE LEAKAGE		−25		dBm	P_{IN} = 0 dBm, f_{IN} = 4.0 GHz, output terminated
SUPPLY					
Voltage (V_{CC})	2.85	3	3.15	V	
Current (I_{CC})		62	83	mA	

[1] Below 200 MHz, a square wave input is required.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NOT INTERNALLY CONNECTED. THESE PINS CAN BE CONNECTED TO RF AND DC GROUND WITHOUT AFFECTING PERFORMANCE. THE NIC PINS ARE TYPICALLY TIED TO GND FOR ENHANCED THERMAL PERFORMANCE (BUT NOT REQUIRED).

15684-002

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4	NIC	Not Internally Connected. These pins can be connected to RF and dc ground without affecting performance. The NIC pins are typically tied to GND for enhanced thermal performance (but not required).
2	GND	Ground. This pin must be connected to both RF and dc ground.
3	IN	RF Input. This pin must be dc blocked.
5	VCC	Supply Voltage (3 V).
6	OUT	RF Output. This pin must be dc blocked.

INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

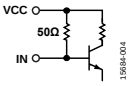


Figure 4. IN Interface Schematic

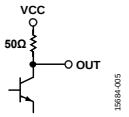


Figure 5. OUT Interface Schematic

Figure 6. VCC Interface Schematic

A.5 Frequency Mixer

ANALOG DEVICES

GaAs, MMIC, Fundamental Mixer, 3 GHz to 10 GHz

Data Sheet **HMC787A**

FEATURES

- Conversion loss: 9 dB typical at 3 GHz to 9 GHz
- Local oscillator (LO) to radio frequency (IF) isolation: 43 dB typical at 3 GHz to 9 GHz
- RF to intermediate frequency (IF) isolation: 26 dB typical at 3 GHz to 9 GHz
- Input third-order intercept (IP3): 24 dBm typical at 3 GHz to 9 GHz
- Input 1 dB compression point (P1dB): 17 dBm typical at 3 GHz to 9 GHz
- Input second-order intercept (IP2): 67 dBm typical at 3 GHz to 9 GHz
- Passive double-balanced topology
- Wide IF frequency range: dc to 4 GHz
- 12-terminal, ceramic, leadless chip carrier (LCC) package

APPLICATIONS

- Microwave radio
- Industrial, scientific, and medical (ISM) band and ultrawide band (UWB) radio
- Test equipment and sensors
- Military end use

FUNCTIONAL BLOCK DIAGRAM

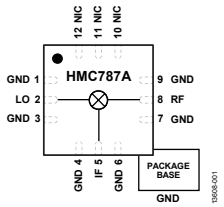


Figure 1.

GENERAL DESCRIPTION

The HMC787A is a general-purpose, double balanced mixer in a 12-terminal, RoHS compliant, ceramic leadless chip carrier (LCC) package that can be used as an upconverter or down-converter from 3 GHz to 10 GHz. This mixer is fabricated in a gallium arsenide (GaAs), metal semiconductor field effect transistor (MESFET) process and requires no external components or matching circuitry. The HMC787A provides excellent local oscillator (LO) to radio frequency (RF) and LO to intermediate frequency (IF) isolation due to optimized balun structures and operates with a LO drive level of 17 dBm. The ceramic LCC package eliminates the need for wire bonding and is compatible with high volume, surface-mount manufacturing techniques.

Rev. A Document Feedback

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SPECIFICATIONS

T_A = 25°C, IF = 100 MHz, LO = 17 dBm, and all measurements performed as downconverter, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
FREQUENCY RANGE				
RF	3		10	GHz
LO	3		10	GHz
IF	DC		4	GHz
LO DRIVE LEVEL		17		dBm
PERFORMANCE AT RF = 3 GHz to 9 GHz				
Conversion Loss		9	11	dB
Single Sideband (SSB) Noise Figure		9		dB
Input Third-Order Intercept (IP3)	15	24		dBm
Input 1 dB Compression Point (P1dB)		17		dBm
Input Second-Order Intercept (IP2)		67		dB
RF to IF Isolation	15	26		dB
LO to RF Isolation		48		dB
LO to IF Isolation	35	43		dB
PERFORMANCE AT RF = 9 GHz to 10 GHz				
Conversion Loss		9	11	dB
SSB Noise Figure		9		dB
Input IP3	15	24		dBm
Input P1dB		15		dBm
Input IP2		66		dB
RF to IF Isolation	15	26		dB
LO to RF Isolation		47		dB
LO to IF Isolation	25	42		dB

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

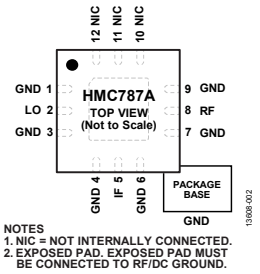


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 4, 6, 7, 9	GND	Ground. Connect the package bottom to RF/dc ground. See Figure 3 for the GND interface schematic.
2	LO	Local Oscillator. This pin is dc-coupled and matched to 50 Ω. See Figure 4 for the LO interface schematic.
5	IF	Intermediate Frequency. This pin is dc-coupled. For applications not requiring operation to dc, externally block this pin using a series capacitor whose value is chosen to pass the necessary IF frequency range. For operation to dc, this pin must not source or sink more than 12 mA of current or device nonfunction and possible device failure results. See for Figure 5 the IF interface schematic.
8	RF	Radio Frequency. This pin is dc-coupled and matched to 50 Ω. See Figure 6 for the RF interface schematic.
10 to 12	NIC	Not Internally Connected.
	EPAD	Exposed Pad. Exposed pad must be connected to RF/dc ground.

INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

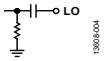


Figure 4. LO Interface Schematic

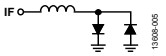


Figure 5. IF Interface Schematic

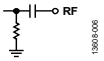


Figure 6. RF Interface Schematic

A.6 Switches

SWITCHES - SPDT - SMT

ANALOG DEVICES

HMC270AMS8GE

v02.0316

GAAS MMIC SPDT SWITCH NON-REFLECTIVE, DC -8 GHz

Typical Applications

The HMC270AMS8GE is ideal for DC - 8.0 GHz applications:

- CATV
- MMDS & WirelessLAN
- Wireless Local Loop

Features

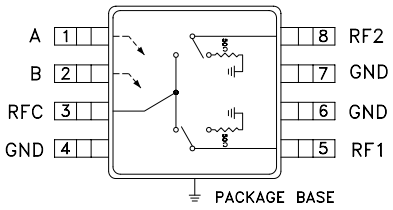
Broadband Performance: DC - 8 GHz

Very High Isolation: 45 dB @ 6 GHz

Non-Reflective Design

Low Cost MSOP-8 Package: 14.8 mm²

Functional Diagram



General Description

The HMC270AMS8GE are broad-band non-reflective GaAs SPDT switches in 8 lead MSOP grounded base surface mount plastic packages. Covering DC to 8 GHz, the switch offers excellent isolation from 70 to 35 dB. The negative control voltage of -5 volts allows operation down to DC. If positive control is required along with high isolation, see the DC to 3.5 GHz HMC284AMS8GE non-reflective SPDT.

Electrical Specifications, T_A = +25° C, With 0/-5V Control, 50 Ohm system

Parameter		Frequency	Min.	Typ.	Max.	Units
Insertion Loss		DC - 2.0 GHz DC - 6.0 GHz DC - 8.0 GHz		0.8 1.0 2.4	1.2 1.7 2.8	dB dB dB
Isolation		DC - 2.0 GHz DC - 4.0 GHz DC - 6.0 GHz DC - 8.0 GHz	43 42 37 28	53 52 45 33		dB dB dB dB
Return Loss	"On State"	DC - 2.0 GHz DC - 6.0 GHz DC - 8.0 GHz	11 9 7	14 12 10		dB dB dB
Return Loss RF1, RF2	"Off State"	DC - 2.0 GHz DC - 6.0 GHz DC - 8.0 GHz	15 13 10	20 18 15		dB dB dB
Input Power for 1 dB Compression		0.5 - 8.0 GHz	24	28		dBm
Input third Order Intercept (Two-Tone Input Power = +10 dBm Each Tone)		0.5 - 8.0 GHz	37	42		dBm
Switching Characteristics		DC - 8.0 GHz				
tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)				15 50		ns ns

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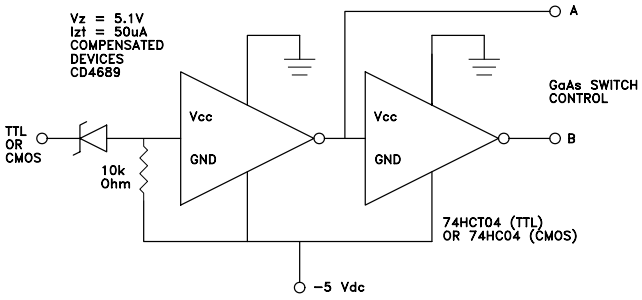
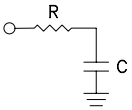
Suggested Driver Circuit



Simple driver using inexpensive standard logic ICs provides fast switching using minimum DC current while translating from standard positive voltage TTL or CMOS logic to negative voltage GaAs IC logic.

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	A	See truth table and control voltage table.	
2	B	See truth table and control voltage table.	
3, 5, 8	RFC, RF1, RF2	This pin is DC coupled and matched to 50 Ohm. Blocking capacitors are required if RF line potential is not equal to 0V.	
4, 6, 7	GND	This pin must be connected to RF/DC ground.	

HMC245AQS16 / 245AQS16E

v00.1213

GaAs MMIC SP3T Non-REFLECTIVE SWITCH, DC - 3.5 GHz

Typical Applications

The HMC245AQS16 / 245AQS16E is ideal for:

- Basestation Infrastructure
- CATV / DBS
- Wireless Local Loop
- Test Equipment

Features

Low Insertion Loss: 0.7 dB @ 2.0 GHz

Non-Reflective Design

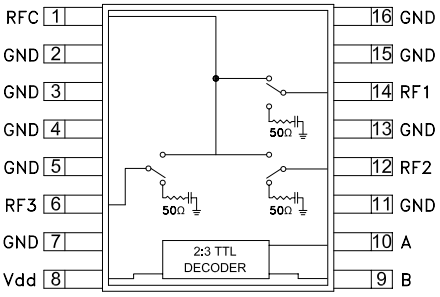
Integrated 2:3 TTL Decoder

"All Off" Isolation State

Single Positive Supply: Vdd = +5V

16 Lead QSOP SMT Package

Functional Diagram



General Description

The HMC245AQS16 & HMC245AQS16E are low cost non-reflective SP3T switches in 16-lead QSOP surface mount packages. Covering DC to 3.5 GHz, the switch offers 30 to 40 dB isolation and a low insertion loss of 0.7 dB. A 2:3 TTL/CMOS compatible decoder is integrated on the switch requiring only 2 control lines and a single +5V bias to select each path, replacing 6 control lines normally required by GaAs SP3T switches.

Electrical Specifications, T_A = +25° C, For TTL Control and Vdd= +5V in a 50 Ohm System

Parameter		Frequency	Min.	Typ.	Max.	Units
Insertion Loss		DC - 2.0 GHz DC - 3.0 GHz DC - 3.5 GHz		0.7 0.8 1.1	1.0 1.3 1.5	dB dB dB
Isolation		DC - 1.0 GHz DC - 2.0 GHz DC - 2.5 GHz DC - 3.5 GHz	40 35 31 26	46 42 40 32		dB dB dB dB
Return Loss	"On State"	DC - 1.5 GHz DC - 3.5 GHz		23 17		dB dB
Return Loss RF1 - 3	"Off State"	0.3 - 3.5 GHz 0.5 - 3.5 GHz		12 15		dB dB
Input Power for 1 dB Compression		0.3 - 2.5 GHz 0.3 - 3.5 GHz	26 25	29 28		dBm
Input Third Order Intercept (Two-tone Input Power = +10 dBm each tone)		0.3 - 2.5 GHz 0.3 - 3.5 GHz	44 40	48 44		dBm
Switching Characteristics tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)		0.3 - 3.5 GHz		40 150		ns ns

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Application Support: Phone: 1-800-ANALOG-D

GaAs MMIC SP3T Non-REFLECTIVE SWITCH, DC - 3.5 GHz

Bias Voltage & Current

Vdd Range= +5 Vdc ±10%		
Vdd (Vdc)	Idd (Typ) (mA)	Idd (Max) (mA)
+5	2.2	6.0

TTL/CMOS Control Voltages

State	Bias Condition
Low	0 to +0.8 Vdc @ 0.2 µA Typ.
High	+2.0 to +5 Vdc @ 35 µA Typ.

Truth Table

Control Input		Signal Path State
A	B	RF COM to:
Low	Low	RF1
High	Low	RF2
Low	High	RF3
High	High	All Off

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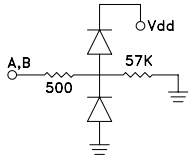
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

GaAs MMIC SP3T Non-REFLECTIVE SWITCH, DC - 3.5 GHz

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 6, 12, 14	RF3, RF2, RF1, RFC	This pin is DC coupled and matched to 50 Ohms. Blocking capacitors are required.	
2 - 5, 7, 11, 13, 15, 16	GND	This pin must be connected to PCB RF ground to maximize isolation.	
8	Vdd	Supply Voltage +5 Vdc ±10%	
9	B	See truth table and control voltage table.	
10	A	See truth table and control voltage table.	

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
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Application Support: Phone: 1-800-ANALOG-D

HMC252AQS24E

v01.0316

GaAs MMIC SP6T NON-REFLECTIVE SWITCH, DC - 3 GHz

Typical Applications

The HMC252AQS24E is ideal for:

- Base Station
- CATV / DBS
- MMDS & WirelessLAN
- Test Equipment

Features

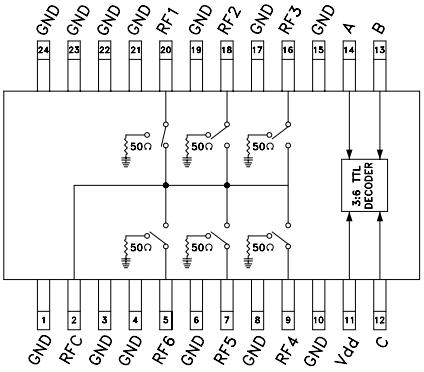
Low Insertion Loss (2 GHz): 1.0 dB

Single Positive Supply: V_{DD} = +3V to +5V

Integrated 3:6 TTL Decoder

24 Lead QSOP Package

Functional Diagram



General Description

The HMC252AQS24E is low-cost non-reflective SP6T switches in 24-lead QSOP packages featuring wideband operation from DC to 3.0 GHz. The switch offers a single positive bias and true TTL/CMOS compatibility. A 3:6 decoder is integrated on the switch requiring only 3 control lines and a positive bias to select each path. The HMC252AQS24E SP6T replaces multiple configurations of SP4T and SPDT MMIC switches and logic drivers.

Electrical Specifications, T_A = +25°C, For TTL Control and V_{DD} = +3.3V, 5V in a 50 Ohm System

Parameter	Frequency	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
		Vdd = +3.3V			Vdd = +5V			
Insertion Loss	DC - 1.0 GHz DC - 2.0 GHz DC - 2.5 GHz DC - 3.0 GHz		0.8 1.0 1.2 1.4			0.8 1.0 1.2 1.4	1.2 1.3 1.5 1.8	dB
Isolation	DC - 1.0 GHz DC - 2.0 GHz DC - 2.5 GHz DC - 3.0 GHz		45 40 38 32		38 32 29 26	45 40 38 32		dB
Return Loss "On State"	DC - 1 GHz DC - 2.5 GHz DC - 3.0 GHz		23 18 12		14 14 7	23 18 12		dB
Return Loss RF1-6 "Off State"	0.3 - 1 GHz 0.3 - 3.0 GHz 0.5 - 2.5 GHz		11 12 15		8 8 11	11 12 15		dB
Input Power for 1dB Compression	0.1 - 1.0 GHz 0.3 - 3.0 GHz		24 24		 21	30 28		dBm
Input Third Order Intercept (Two-Tone Input Power = +10 dBm Each Tone)	0.3 - 3.0 GHz		47		42	47		dBm
Switching Characteristics tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)	0.3 - 3.0 GHz		 20 70			 25 90		ns

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

HMC252AQS24E

v01.0316

GaAs MMIC SP6T NON-REFLECTIVE SWITCH, DC - 3 GHz

Absolute Maximum Ratings

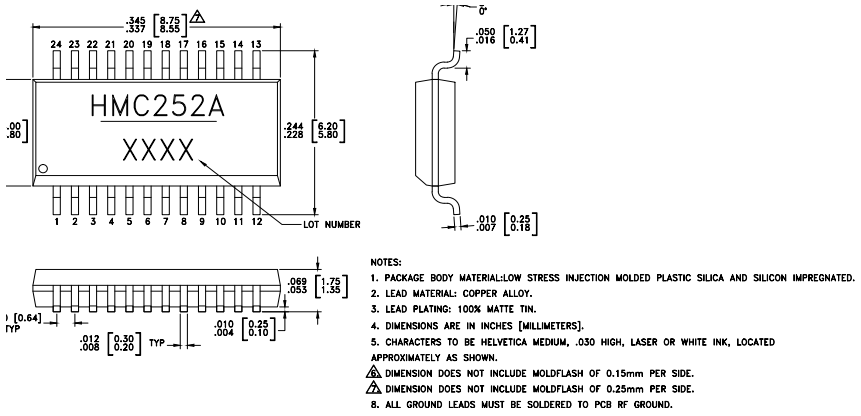
Bias Voltage Range (Port Vdd)	+7 Vdc
Control Voltage Range (A, B, C)	-0.5V to Vdd +1 Vdc
Channel Temperature	150 °C
Thermal Resistance Insertion Loss Path Terminated Path	 130 °C/W 236 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
Maximum Input Power Vdd = +5 Vdc Insertion Loss Path Terminated Path	 +29.8 dBm +24.4 dBm
ESD Sensitivity (HBM)	Class 1A

Truth Table

Control Input			Signal Path State
A	B	C	RFCOM to:
LOW	LOW	LOW	RF1
HIGH	LOW	LOW	RF2
LOW	HIGH	LOW	RF3
HIGH	HIGH	LOW	RF4
LOW	LOW	HIGH	RF5
HIGH	LOW	HIGH	RF6
LOW	HIGH	HIGH	ALL OFF
HIGH	HIGH	HIGH	ALL OFF

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC252AQS24E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [1]	HMC252A XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

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