CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

The work presented here deals with a new active building block, voltage differencing current conveyor, VDCC, and its application in analog circuit design. The analog circuit design or analog VLSI deals with the analog signal processing. Several major developments in the area of analog circuits and signal processing have taken place in the past four decades. There is a huge bulk of material available about the various active and building blocks developed post and prior to Current Conveyors. In the present work an attempt has been made to highlight some basic building blocks of analog circuit design, the developments that lead to the introduction of voltage differencing current conveyor (VDCC) and applications of this block in various analog circuits of signal processing.

The traditional operational amplifier (op-amp) is a highly versatile element [1] which was first introduced in the early 1940s. Op-amps were used for the realization of many circuits, both linear and non-linear. Extensive research had been carried out from mid-sixties to mid-eighties on the design of various linear and non-linear analog circuits using integrated circuit (IC) op-amps. The op-amp based circuits employ RC elements and since the precise tuning of the time constant RC was difficult to implement their monolithic IC implementation was difficult. The performance of these circuits was limited due to less bandwidth, slew rate etc. this forced the analog designers to look for other alternate active blocks [2]. Switched capacitor circuits was one solution where the resistor was replaced by a periodically switched capacitor but it again posed problems like aliasing and clock feed through [3].

The Operational Transconductance Amplifier (OTA) was introduced in the eighties. The OTA-C circuits employ only transconductors and capacitors to build various functional circuits and thus, do not require any resistors; moreover, their internal structure is also resistor-less, thus adding to its advantage list. The OTA circuits are gain variable (programmable) with their transconductance being controlled electronically through an external DC bias voltage/ current.

Past one decade has seen developments in digital circuit design, particularly CMOS digital circuits, which has had a deep influence on the developments in analog circuits as well, more precisely the mixed-mode circuit design which has both analog and digital circuits

integrated on the same chip using the same technology. Although the digital circuits and systems have many advantages over the analog type, the latter still cannot be avoided as the natural world is analog. The analog designers faced various challenges of matching the analog circuits and systems with their fast growing digital counterparts, due to the various developments in the field of integrated circuit (IC) technology. These requirements led to continued research to develop efficient analog circuit designs especially current-mode (CM) techniques and circuits as the solutions for the problems posed by the mixed-mode circuit design that is prevalent these days. The current mode approach to signal processing and circuit design definitely has its advantages like higher frequency range of operation, lower power consumption, higher slew rates, improved linearity and better accuracy, but still the voltage mode approach is also equally important because of the simpler solutions to given problems. Before describing the developments in analog signal processing and circuit designs we will first analyze some of the basics of signal processing.

1.2 ANALOG AND DIGITAL SIGNAL PROCESSING

The signal processing find application in various fields of engineering which include communication systems, control systems, instrumentation, measurement, bio-medical, etc. There are two different ways to implement signal processing, which are given as:

(1) Analog or continuous time method and

(2) Digital or discrete time method.

The analog signal processing was dominant for a long as the solutions were based on the fact that the real world is analog. It uses analog circuit constituents such as diodes, resistors, capacitors, transistors, etc. With the developments like growing influence of digital computer and microprocessor, the digital signal processing started edging its analog counterpart and has become dominant now a days. The analog signal processing is based on the natural ability of the system to solve differential equations that describe a physical system; the solutions thus obtained are in real time. On the other hand, digital signal processing relies on numeric calculations. The method may sometimes not give results in real time. The digital signal processing has some advantages over analog approach; two prominent among them are-

(1) Flexibility: Various kind of signal processing operation can be done using same hardware; while in the core of analog signal processing, a different hardware has to be designed for each kind of operation.

(2) Repeatability: A signal processing operation can be repeated again and again and we can get same results, while in analog systems if there is a parameter variation due to change in temperature or supply voltage, the results may change.

Apart from these, digital signal processing has many other advantages also like, better noise immunity than analog signals. They are compact and much cheaper than their analog counterpart. The digital systems also give the encryption facility so that the signals to be transmitted are encrypted and only the intended receiver can decode it. It enables transmission of signals over a long distance and it enables multi-directional transmission simultaneously.

As we see that digital systems and circuits have many advantages, so the designers try to look for digital solutions rather than analog for the problems of vlsi system design. All advantages apart, the analog circuits and systems are still fundamentally necessary in many complex and high performance systems. In reality, all signals in the physical world are continuous in both amplitude and time and hence for conditioning of such signals, before they can be processed by digital signal processing circuits, analog techniques will always be required. Another important reason for the existence of analog signal processing is the bandwidth, which can be some order of magnitudes higher, if the signal is processed in analog circuits than in digital.

1.3 CURRENT MODE AND VOLTAGE MODE SIGNAL PROCESSING

The signal processing done on electric or electronic circuits is performed by means of organized movement of charge, where voltages and currents are usually the variables and time, resistance, capacitances and inductances are parameters of the circuit defining the properties of the signal processing. The reason behind using only voltages and currents in analog signal processing is that the active devices, which are used in analog electronics, operate mostly with resistances (conductance), as parameters for controlling the signal processing. The signal is then processed by miscellaneous voltage-current and current-voltage conversions, amplification, weighted addition and multiplication, etc. [4]. In the past, due to the thinking that processing in terms of voltages is easier and simpler for the designers than in terms of currents, voltage had

been used as the main variable for signal processing. During the initial years of analog electronics only voltage mode processing was practical and most of the building blocks used in analog electronics (like op-amp) were typical voltage processing circuits.

As the time passed by, a necessity to increase speed of circuits for analog signal processing and also to decrease the supply voltages of integrated circuits aroused in front of the designers and thus they started devoting attention to the so-called current mode. In the current-mode the individual circuit elements were meant to interact by the means of current and not voltage.

The difference between voltage and current processing circuits is that a single output terminal of a current processing block is able to supply only a single input terminal, since the inputs of the current processing blocks can't be arranged into a serial connection. Therefore, if more input terminals are required to be supplied by the same input signal, it is necessary to design current processing building blocks with multiple outputs giving the same output signal while in voltage processing circuits a single voltage-output terminal can supply more voltage-input terminals connected in parallel.

As more and more advances in the field of analog system and circuits were made, need for some application specific modes also aroused. In certain circuits, the input was current and the output was needed to be voltage, these circuits were called trans-impedance mode circuits. Similarly, in some other circuits the input was voltage and the output was needed as current, such circuits are called trans-admittance mode circuits. These modes are however very application specific.

1.4 ANALOG CIRCUIT DESIGN

Principally, Digital circuits operate with only two values of voltage, while analog circuits process signals with continuous variation of voltage. We know that factually no macroscopic signal is truly quantized, so the digital circuit designers need some familiarity with analog electronics also. Therefore analog circuit design plays an important role in the present day integrated circuit technology. The basic analog electronic circuits are: filters, active filters, oscillators, active oscillators, multi-vibrators, rectifiers, mixers, etc.

Simple analog filters or passive filters consist of either all three or any two out of resistors, capacitors and inductors. Accordingly we have, RC, RL, LC and RLC circuits. These passive circuits can be used to filter a signal by blocking certain frequencies and passing others.

The active filters use active components like amplifiers in their circuit along with other passive elements. Inclusion of active components, like amplifiers, improves the performance and expectedness of a filter, while the requirement for inductors (inductors are typically expensive and bulky) is also avoided. An amplifier inhibits the load impedance of the succeeding stage from upsetting the characteristics of the filter. The active devices also bring in some limitations to the circuits like finite bandwidth, more power consumption, noise injection into the circuit, etc.

Another type of active filter is a biquadratic or biquad filter. This linear filter implements transfer function in the ratio of two quadratic equations. Biquad filters are active filters that are implemented using a single-amplifier biquad (SAB) or two integrator loop topology. The SAB topology uses feedback to generate complex poles and possibly complex zeros; to generate the proper filter characteristics, the feedback moves the real poles of an RC circuit. On the other hand, the two integrator loop topology is derived from rearranging a biquadratic transfer function. After rearrangement one signal is expressed as the sum of another signal, its integral, and the integral's integral.

An electronic oscillator yields oscillating electronic signal, often a sinusoidal wave or a square wave. Oscillators do the conversion of direct current (DC) from a power supply to an alternating current (AC) signal. A sinusoidal output is produced by a linear oscillator. These oscillators are comprised an amplifier and a frequency selective element, a filter. A feedback oscillator is the most common form of linear oscillator. In feedback oscillators, the frequency selective filter is generally of two types: RC and LC. In an RC oscillator circuit, the filter is a comprised of resistors and capacitors, it is a network of these two passive elements. RC oscillators are used to generate low frequencies, which lie in the audio range. In an LC oscillator circuit the filter comprises of a tuned circuit, also called tank circuit, containing inductor and capacitor connected together.

A multi-vibrator is an electronic circuit used to implement a various other simple two-state systems like oscillators, timers and flip-flops. It generally comprises of two amplifying devices cross-coupled by resistors and capacitors. There are basically three different types of

multi-vibrator circuits depending on the circuit operation: astable, monostable and bistable multivibrators. Multivibrators mainly find application in systems where square waves or timed intervals are required.

Rectifier circuits are used for converting AC supply into DC. However, simple diode circuits can perform rectification but since their efficiency is not very high so sometimes we need active rectifier circuits which utilize active analog blocks for their implementation. Mixer circuits form a very important part of the communication systems especially the receivers.

Similarly there are some other analog circuits that can be implemented by both active elements and passive elements or combination of both. A few of these circuits are implemented in this thesis work.[1]

1.5 ORGANIZATION OF THE THESIS

In this thesis, chapter 1 covers the basic concepts of signal processing and analog circuit design. Initially, the developments that led to the proposing of VDCC active analog block are discussed. Then a brief discussion about difference between analog and digital signal processing is given. The current-mode, voltage-mode, trans-impedance mode and trans-admittance mode of circuit operation are also discussed. Finally, an introduction to the most commonly used analog circuits and components is given at the end of the first chapter.

In chapter 2, basic components, blocks and circuits that are used to derive the active building blocks are described in detail. Basic building blocks in analog circuit design like differential amplifier, current mirror, voltage buffer, operational trans-conductance amplifier are introduced in this chapter. Current conveyors and its derivatives with symbolic notation and characteristics are also covered in the second chapter. Current conveyors are emphasized upon as the analog block VDCC is a derivative of CCII and working and implementation of VDCC is best understood through the understanding of the CCII.

In chapter 3, the Voltage Differencing Current Conveyor (VDCC) is introduced. Initially, the terminal equations of VDCC and the MOSFET model of VDCC are studied and the working of the VDCC active analog block is understood. After this some basic circuits are implemented using VDCC block like amplifier, integrator, differentiator, grounded/floating inductor etc. These circuits help us in understanding the working of VDCC block and we also study the terminal conditions to make them useful in some advanced circuits.

In chapter 4, we use VDCC block for some advanced applications like biquad filter realizations and oscillator realizations. In this chapter three categories of novel circuits have been realized using the VDCC active block. A voltage mode biquad with lowpass, bandpass and notch filter outputs is realized. After realization and analysis of biquad filters current mode oscillators are realized where 11 different configurations are given for RC-sinusoidal oscillators and finally voltage mode oscillators are realized and in this section we have realized two configurations for multi-phase sinusoidal oscillators.

Finally, in chapter 5 complete work of the thesis is summarized and some points are given for the future scope in this field of research.

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CHAPTER 2

LITERATURE SURVEY OF VARIOUS CONSTITUENT CIRCUITS IN ANALOG CIRCUIT DESIGN

In the past three four decades, a lot of work has been done in the field of integrated circuit technology and thus hundreds of bipolar/CMOS active building blocks have been proposed in the this field by different research groups and individuals. A comprehensive summary of some of these blocks has been given in [1]. After a brief study of these blocks and their circuital implementation, it can be observed that these blocks comprise of one or more of the following basic constituent blocks

(i) Differential pair
(ii) Current mirrors
(iii) Active loads
(iv) Voltage buffers
(v) Operational transconductance amplifier

As we see that, these blocks form the basis of many other active analog devices so a brief study of these blocks is compulsory and thus this chapter focuses on these constituent blocks and their important features.

2.1 DIFFERENTIAL PAIR

The differential pair as an active element is widely used as an input stage in many other analog blocks and analog circuits. In early days of analog circuit design, differential pair was used as the input stage for operational amplifier. Later on, many circuits mostly with voltage inputs used differential pair. In this thesis work the VDCC block also uses differential pair as input stage. With the evolution of integrated circuits, the popularity of differential amplifier has increased in both bipolar and MOS technologies [2], because of its common-mode signal rejection property and high gain as compared to its single ended counterpart.

The matching between the circuit parameters of the transistors on the two sides of the differential pair decides its performance. Thus the circuits using differential pair are much less

sensitive to interference and noise than those using single ended circuits. Apart from this, differential circuits enable designers to bias the amplifier and to couple successive amplifier stages without using bypass and coupling capacitors such as those used in the configurations not using differential pair like the discrete circuit amplifier [2]. We know that, in IC fabrication it is difficult to fabricate large capacitors economically, so by using differential pair we can overcome this limitation. A simple MOS based differential pair is shown in fig. 2.1. The two transistors, M_1 and M_2 are matched transistors and have their sources connected together and biased by a constant current source, I. The current source used here is ideal and thus has infinite output impedance. There are basically two modes of operation and they are as follows:

2.1.1 Operation in Common-Mode

In this mode of operation, the gate terminals of the two transistors are joined together and connected to the voltage V_{CM}, called the common-mode voltage. Since in fig. 2.1, both transistors are matched so $V_{CM} = V_{G1} = V_{G2}$, and by symmetry, it can be observed that the current *I* will be divided equally between the two MOS transistors [2]. Thus,

$$i_{D1} = i_{D2} = I/2 \tag{2.1}$$

Now, if we neglect the channel-length modulation, the relation between gate-to-source voltage and drain current is as follows:

$$\frac{I}{2} = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 \tag{2.2}$$

The voltage at both the drain nodes will be

$$V_{D1} = V_{D2} = V_{DD} - \frac{1}{2} R_D \tag{2.3}$$

Hence, the differential output voltage between the two drains will be ideally zero. In fig. 2.1 resistance, R_D is generally realized using active loads/current sources, etc.

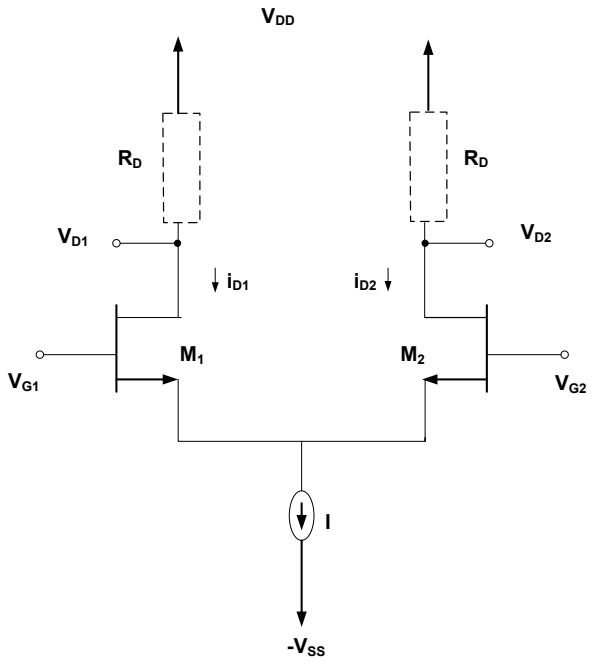


Fig.2.1 The basic MOS differential pair configuration [2]

2.1.2 Operation for Differential Input

For this mode, the differential input mode, input at one gate terminal of the MOS transistor in fig. 2.1, V_{G2} may be set to zero and the gate terminal of the other MOS transistor is applied with a signal V_{G1}. The characteristics of differential pair are depicted in fig. 2.2. The differential input voltage is as

$$V_{id} = V_{GS1} - V_{GS2} \tag{2.4}$$

When V_{id} is positive i.e. $V_{GS1}$is greater thanV_{GS2}, i_{D1} will be greater than i_{D2}. Hence the difference output voltage (V_{D1}- V_{D2}) will be positive. While, if V_{GS1} is lower than V_{GS2}, i_{D1} will be smaller than i_{D2} and corresponding to this V_{D1}will be greater than V_{D2}.

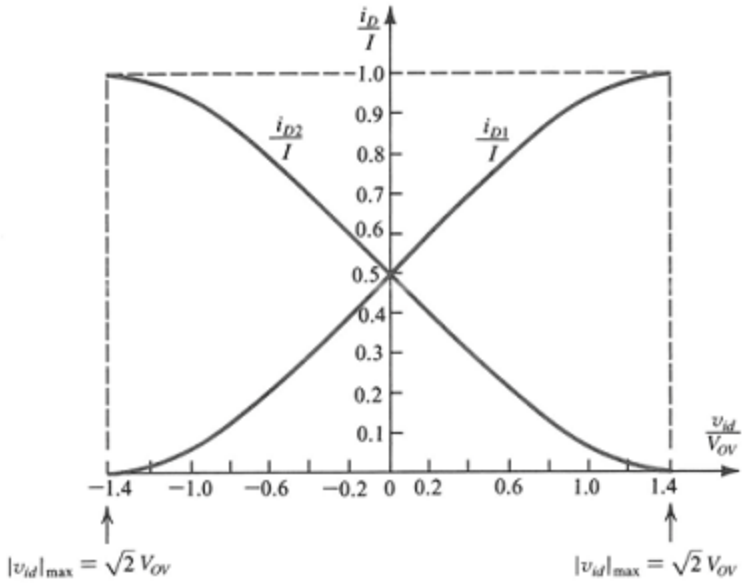


Fig. 2.2 Characteristic of CMOS based differential amplifier

2.2 CURRENT MIRROR

In the past two decades, due to the greater emphasis on current-mode circuits current sources are playing an important role to design the IC amplifier. The current mirrors are used to design current sources along with several other active building blocks as discussed in [1]. A basic BJT based NPN current mirror is shown in fig. 2.3 where $R_0 = r_{02}$ (output resistance of Q2). For the analysis, it is assumed that both the transistors in this circuit are identical and the Early effect is neglected. The input current of the circuit is I_{REF} and output current is I_0. the relation between input and output current is given as:

$$I_0 = \frac{I_{REF}}{1 + {}^{2}/_{\beta}} \tag{2.5}$$

From the equation above, I_0 and I_{REF} become equal only when $\beta \rightarrow \infty$.

Two performance parameters are there to determine the performance of the current mirror circuits, they are listed below:

- Accuracy of the current transfer ratio of the mirror circuit
- Output resistance of the current source

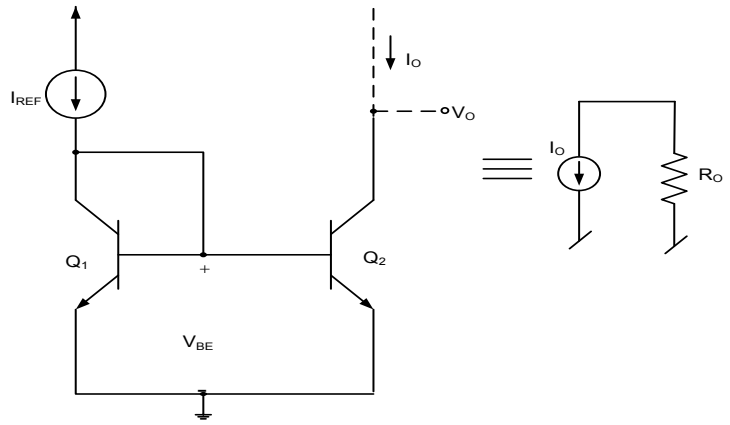


Fig. 2.3: The basic BJT current mirror [2]

Two performance parameters are there to determine the performance of the current mirror circuits, they are listed below:

- Accuracy of the current transfer ratio of the mirror circuit
- Output resistance of the current source

2.2.1 Base Current Compensated Current Mirror

The basic current mirror circuit shown in fig.2.3 faces some problems and the main problem is that the base current is finite. By adding current gain to the reference transistor Q_1, the base current error can be minimized. The base current compensated current mirror configuration is shown in fig.2.4. In this configuration, the base current of transistor Q_3 is equal to the difference of I_{ref} and I_{C1}. The R_0 of this configuration is same as in the basic current mirror which is r_{02} (output resistance of transistor Q_2).

For large values of beta, the base current term can be neglected. So the output current is defined as:

$$I_2 \approx I_{ref} \frac{1}{1 + {}^{4}/_{\beta}} \tag{2.6}$$

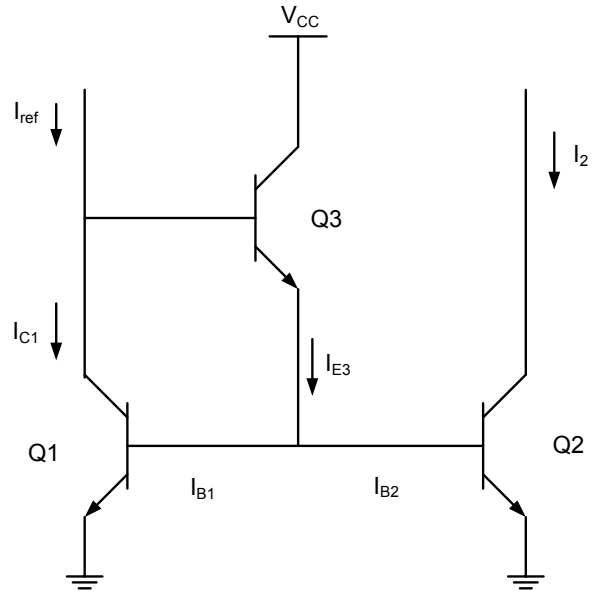


Fig.2.4 Base current compensated current mirror [2]

2.2.2 Cascode Current Source

Due to the finite output resistance of the current source transistors, another error arises in current sources. The finite output resistance results in a variation in output current with voltage in basic current mirror. The cascode current source configuration is shown in fig.2.5. In this configuration, output resistance ($\approx \beta\, r_{02}/2$) is higher than the basic current mirror shown in fig.2.3. The cascode current source comprises of two basic current mirror circuits which are configured using Q3, Q4 transistors and Q1, Q2 respectively, the constituent current mirror circuits are connected in series. In this configuration Q2 and Q4 form a common-base, common-emitter cascode pair.

The input and output current relation is derived as:

$$I_2 \approx I_{ref} \frac{1}{1 + {}^{4}/_{\beta}} \tag{2.7}$$

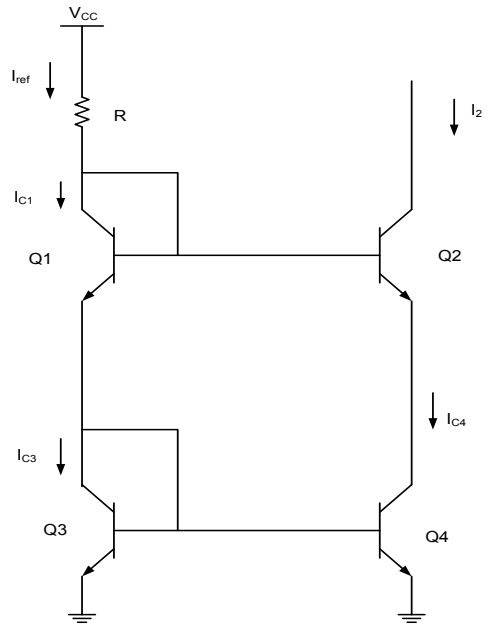


Fig.2.5 Cascode current source using BJTs [2]

2.2.3 The Wilson Current Mirror

The circuit of Wilson Current Mirror is shown in fig.2.6. In the analysis it is assumed that the transistors have identical parameters and the Early effect is neglected. The relation between input and output currents are defined as:

$$\frac{I_0}{I_{REF}} = \frac{1}{1 + \frac{2}{\beta(\beta + 2)}} \tag{2.8}$$

If β becomes much high then the input current (I_{REF}) will be equal to output current (I_0). The advantage of Wilson Current Mirror over the basic current mirror is that it has high output resistance ($\approx \beta r_{02}/2$). This is because of two positive feedback effects.

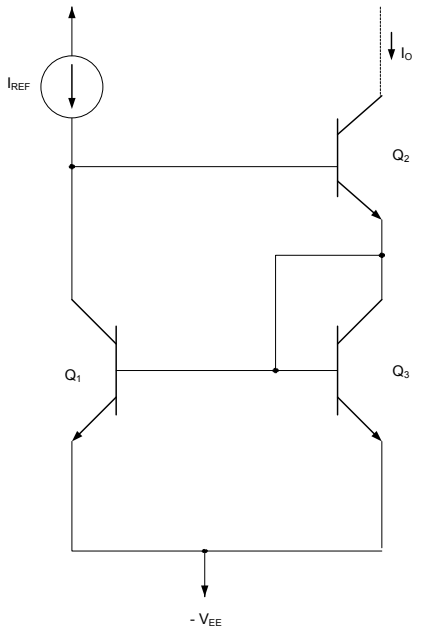


Fig.2.6 Wilson current mirror [2]

2.2.4 Generation of Complementary Current Outputs Using Cross Coupled Current Mirrors

In analog circuit design, various active blocks are designed using cross coupled current mirror which is shown in fig. 2.7. The attractive feature of this configuration is that it gives

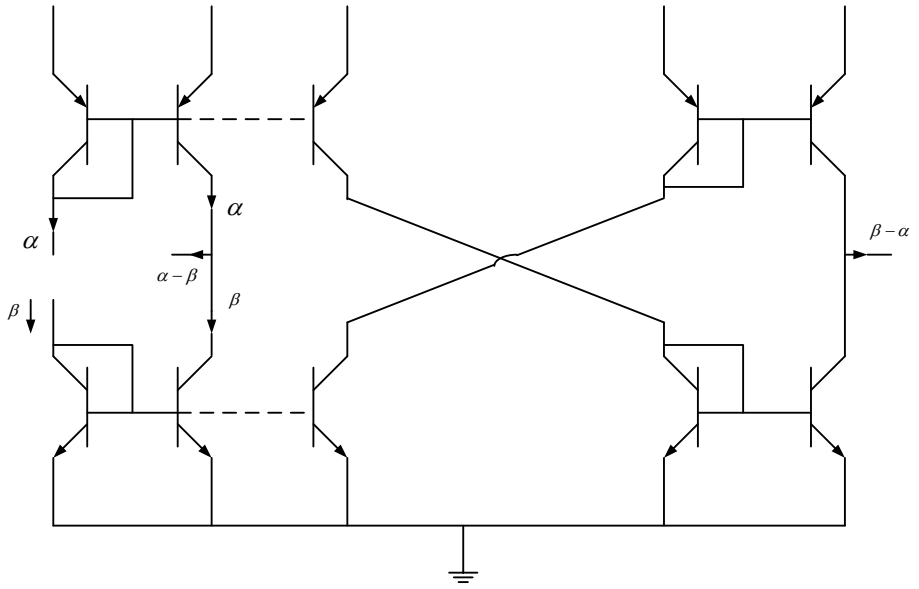


Fig. 2.7 Complementary current output using cross coupled current mirror

complementary outputs. This configuration is used in second generation current conveyors, it provides two current outputs which have opposite polarity to each other.

2.3 ACTIVE LOADS

In IC technology as chip area is a constraint, so resistor is simulated using CMOS and other active blocks such as OTA, this reduces the chip area and circuit efficiency. Such type of active loads also provides the electronic tunability which is the other advantage. A single ended differential amplifier is shown in fig.2.8 with active load (PMOS current mirror).

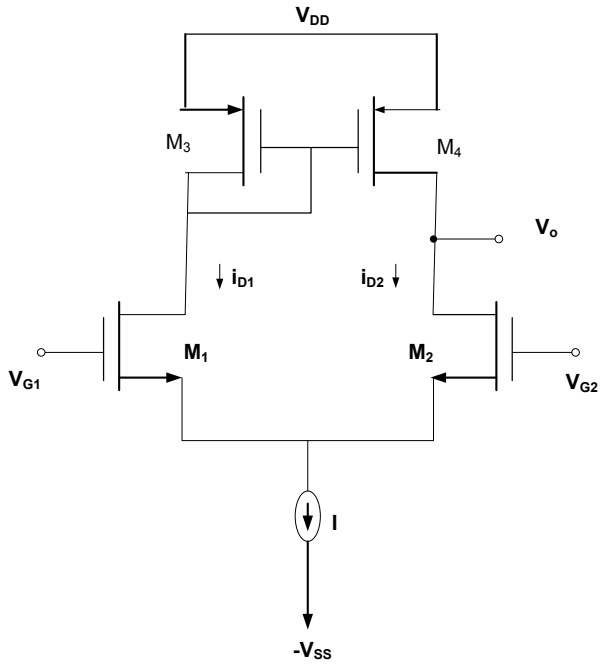
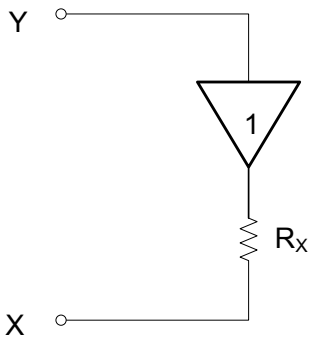


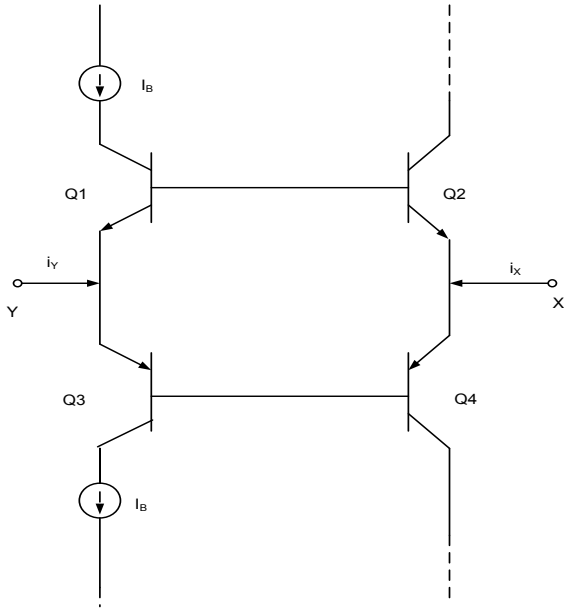
Fig. 2.8 Single ended differential amplifier using active load

2.4 VOLTAGE BUFFERS (TRANSLINEAR)

A voltage buffer is a very useful constitutive block and has the schematic diagram as shown in fig.2.9. In an ideal voltage buffer the input impedance is infinite and the output impedance is zero. Many active building blocks use emitter follower as a voltage buffer. A configuration of a voltage buffer that works on the trans-linear circuit principle [29] is shown in fig.2.9. The value of Rx for this buffer is given by $I_B/2V_T$.



(a)



(b)

Fig.2.9 Trans-linear buffer (a) Equivalent diagram

(b) Realization using BJTs

2.5 OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

Operational transconductance amplifiers (OTA) are the extensions of the basic differential amplifiers which are loaded with active load [7, 8]. Though the transconductance amplifiers are available as off-the-shelf components (LM 3080, LM 13600), these amplifiers can also be found as constitutive blocks in many of the recently proposed active building blocks such as Voltage Differencing Buffered Amplifier [27], Current Differencing Transconductance

Amplifier [28], Voltage Differencing Current Conveyor, etc. In the following we summarize the operational transconductance amplifiers and its features.

OTA is a differential VCCS (Voltage Controlled Current Source) in which output current is controlled by input voltage source and it is characterized by a transconductance gain (g_m). The output of OTA is given by [9]

$$I_0 = g_m(V_1 - V_2) \tag{2.9}$$

where, V_1 and V_2 are voltages as non-inverting and inverting input terminal of OTA. The symbol of OTA is shown in fig.2.10.

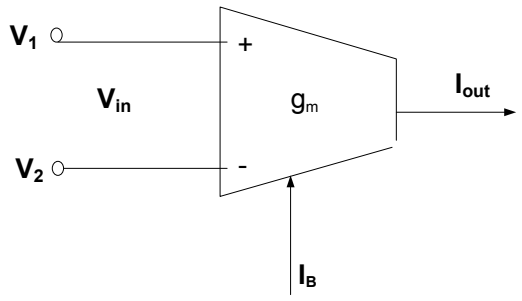


Fig. 2.10 Symbol of OTA

The transconductance is as given below:

$$g_m = \sqrt{\left(\mu_n C_{ox} \frac{W}{L} I_b\right)} \tag{2.10}$$

where, μ_n = the electron mobility of NMOS

C_{ox} = gate oxide capacitance per unit area,

$\frac{W}{L}$ = transistor aspect ratio

I_b = bias current of the OTA.

In the above equation it can be observed that the transconductance g_m is adjustable by a supplied bias current (I_b).

2.5.1 Ideal Characteristics

Characteristics of ideal OTA are summarized below [3, 4]:

Input impedance (Z_{in}) = ∞, Output Impedance (Z_0) = ∞, bandwidth = ∞.

2.5.2 Schematic Circuit Diagram

The MOS transistors implementation of OTA is shown in fig. 2.11 below. The circuit is formed by a differential pair M_1, M_2, a current mirror M_3, M_4 with active load and constant current source derived from M_5. The output current is given by:

$$i_{out} = \frac{i_B}{(V_{GS} - V_t)}(V_{in1} - V_{in2}) = g_m(V_{in1} - V_{in2}) \tag{2.11}$$

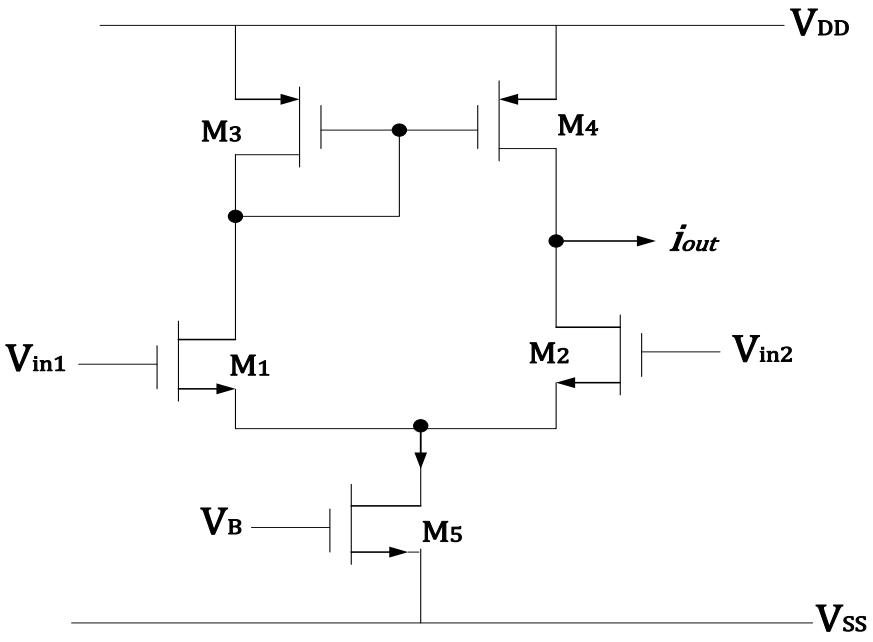


Fig.2 .11 CMOS realization of operational transconductance amplifier

2.6 CURRENT CONVEYOR

In analog circuit design, current conveyor (CC) is one of the fundamental building blocks in current mode techniques. Basically a three terminal device, it can be used for basic analog signal processing functions by using proper circuitry [12]. In the same way as the conventional operational amplifier, the current conveyor also simplifies the circuit design in many manners. The current conveyor extends an alternative manner of abstracting complex circuit functions,

thus adding in the introduction of new and useful implementation. Being a general active building block the current conveyor can replace classical operational amplifier in the voltage mode applications and in addition to this we can also transform those typical voltage mode applications to current mode. The functioning of current conveyor has attracted many researchers and thus many derivatives of the basic current conveyor have been introduced in the last two decades. Here in this literature, we have presented the basics of current conveyor and its derivatives.

The principle of the current conveyor first generation was published by Smith and Sedra in 1968 [10]. After that many different applications of current conveyors have been published by different people. Still after so much research, current conveyors are not available in the form of IC and due to this reason this active block could not be used in many analog circuit and system design applications by many developers. Some op-amps based on current conveyors are available, which have high speed and wide band, in the form of integrated circuits such as OPA660, AD840, AD844. Some common types of current conveyors are discussed in the following text.

2.6.1 First Generation Current Conveyor (CCI)

The principle of the current conveyor of first generation was published by Smith and Sedra in 1968. The current conveyor as a grounded three port network and represented as black box is shown in fig. 2.12. The CMOS realization of current conveyor first generation is shown in fig.2.13. In CC, if some potential 'v' is applied at input terminal 'y' then this same voltage appears at the other input terminal 'x'. In a dual manner, if a current 'I' is forced through terminal 'x' an equal current flows through input 'y'. This same current is also conveyed through output terminal 'z' at high impedance level which can be used as current source. The following equations show input output relationship in CC.

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{2.12}$$

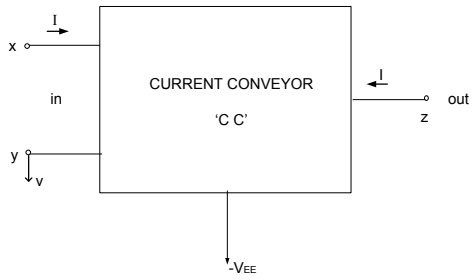


Fig. 2.12 Black box of basic current conveyor

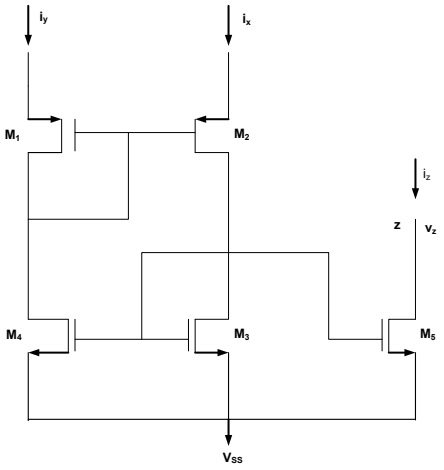


Fig.2.13 CMOS implementation of CCI [12]

2.6.2 Second Generation Current conveyor (CCII)

The second generation current conveyor (CCII) evolved in 1970 [11]. The second generation current conveyor has different and more versatile terminal characteristics. Its symbol is shown in fig.2.14. This active block is further classified into two sub-types based on direction of output current at z terminal termed as CCII+ and CCII-. In CCII, the applied input potential at terminal y is appeared on terminal x as same value and input terminal y has high input impedance. The input current i_x will be conveyed through output terminal z which is used as high impedance as a current source. Following matrix represents CCII terminal equations:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{2.13}$$

The CCII has been introduced as a block that is convenient and provides an easy approach to design general linear analog circuits and systems.

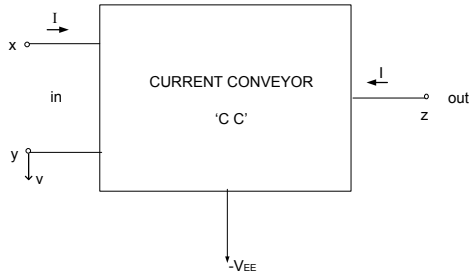
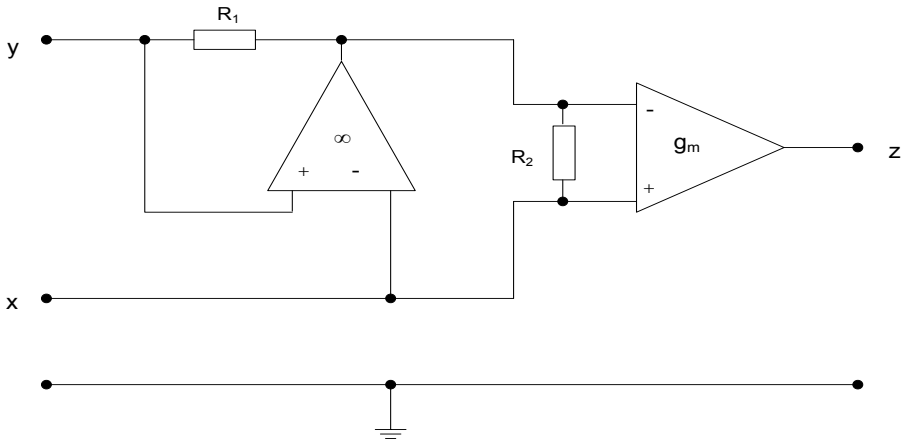


Fig. 2.14 Symbol for CCII

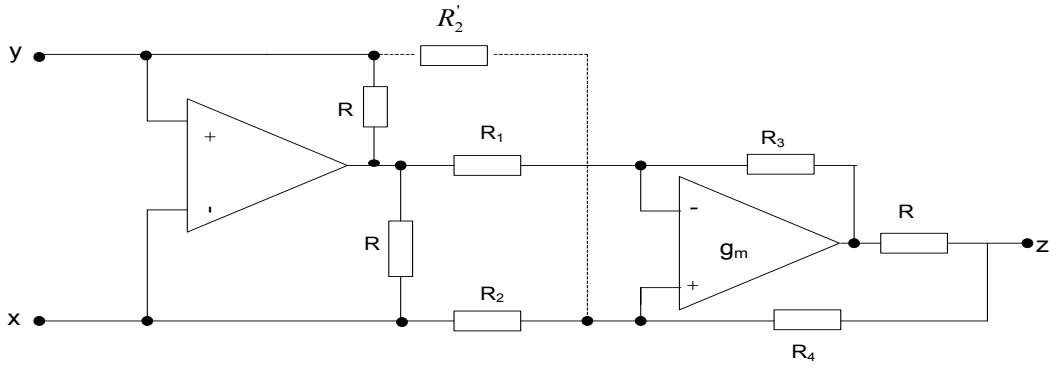
2.6.2.1 Circuit Implementation of CCII

After the bipolar implementation of CCII proposed by proposed by Sedra and Smith [11], some other implementations of CCII using off-the-shelf available ICs have been proposed in various literature [15-17]. The implementations proposed by Senani [16] and Heurtas [17] are notable and given in fig.2.15.

The fig.2.15 (a) shows a working model of CCII. If R_1 is deleted and $R_2 = 1/g_m$, then the circuit can be used as CCII+. On the other hand for CCII-, while the previous conditions for CCII+ are kept same, the input terminals are interchanged. A simplified circuit is presented in fig.2.15 (b), in this circuit the x and y terminals are not identical so it exhibits unsymmetrical nature. This circuit can be more balanced by connecting R_2 and selected as $R_2 = R_2' = 2R_1$.



(a)



(b)

Fig.2.15 (a) Implementation of CCII+ and CCII- [16]

(b)Simplified circuit for current conveyor [17]

2.6.3 Third Generation Current Conveyors

The third generation current conveyor (CCIII) has been introduced by Fabre [13]. CCIII can be used as current controlled current source with unity gain. It can be used to design filters, inductance simulation, etc. because of its terminal properties. It has certain features favorable for cascadability such as good dynamic swing and high output resistance. The main advantages of CCIII are low gain error (high accuracy), high linearity and wide frequency response. Fig.2.16 shows symbol of CCIII and fig.2.17 shows CMOS realization of CCIII and the matrix below gives its terminal equations:

$$\begin{bmatrix} i_y \\ v_x \\ i_{z+} \\ i_{z-} \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_{z-} \\ v_{z+} \end{bmatrix} \tag{2.14}$$

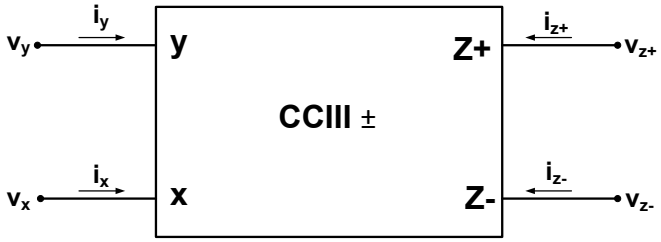


Fig. 2.16 Symbol of the CCIII [14]

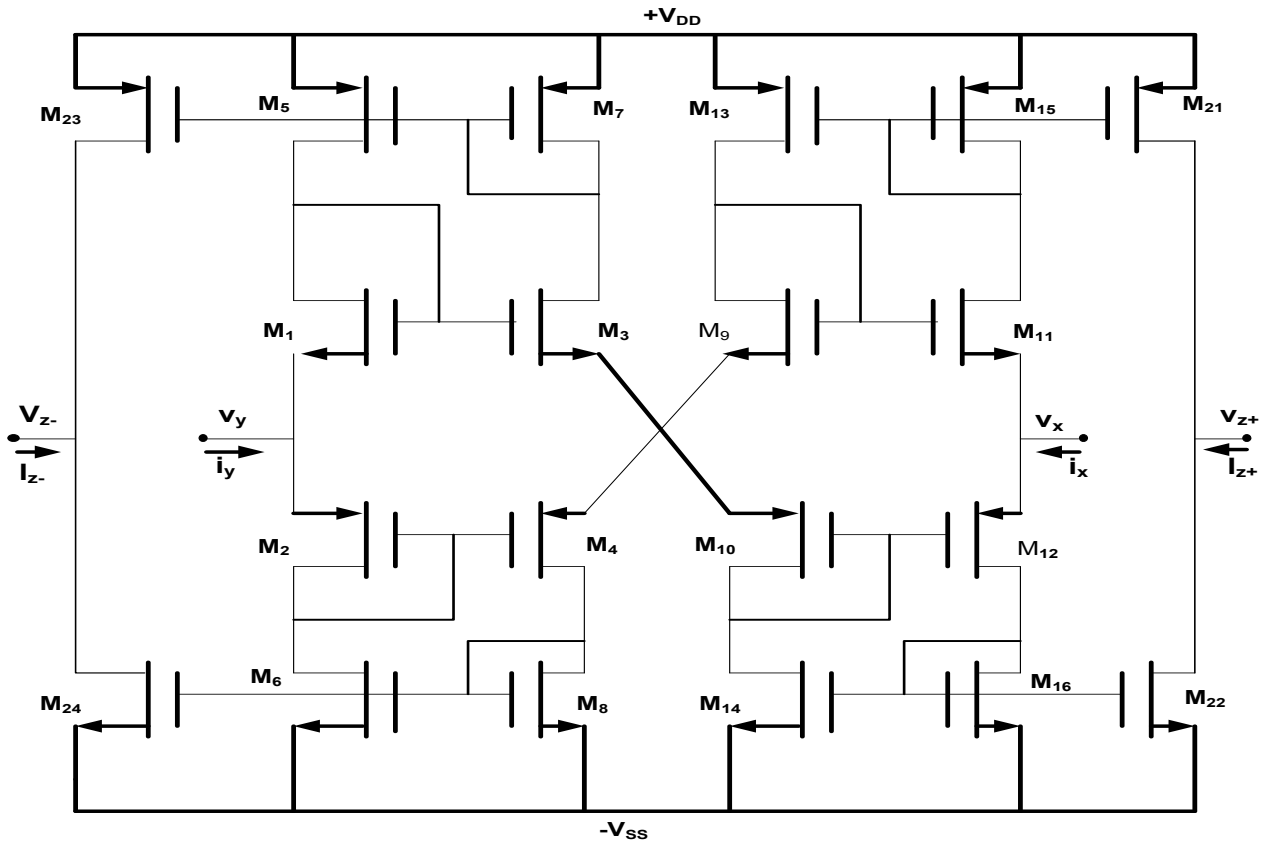


Fig. 2.17 CMOS realization of third generation current conveyor (CCIII) [14]

2.7 DERIVATIVES OF CURRENT CONVEYORS

Modifying the basic structure of current conveyors (CCs) or adding some more functionality enhances the versatility of CCs. It makes CCs more useful in realization of various analog signal processing circuits in both voltage and current mode. Some derivatives of current conveyors are presented in the following text.

2.7.1 Fully Differential Current Conveyors (FDCCII)

The FDCCII is an extended version of CCII. It was proposed in 2000 [18]. Its characteristics are combination of differential pair and current conveyors. FDCCII is an eight terminal active building block and its symbolic diagram is shown in fig.2.18. The Y_1 and Y_2 terminals are high impedance terminals whereas the X+ and X- terminals show low impedances.

The terminal equations are as given below:

$$\begin{bmatrix} V_{x+} \\ V_{X-} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & -1 & 1 & 0 \\ 0 & 0 & -1 & 1 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{X+} \\ I_{X-} \\ V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \end{bmatrix} \quad (2.15)$$

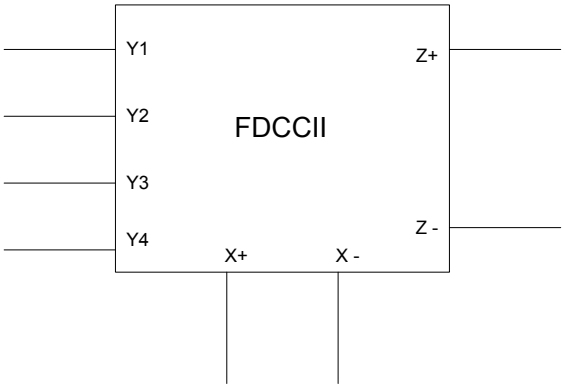


Fig. 2.18 Symbolic notation of FDCCII [18]

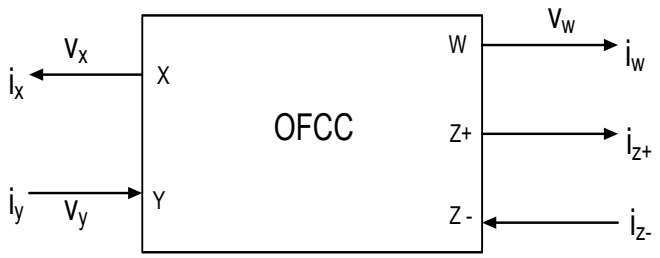
The CMOS implementation of FDCCII and its various applications in the area of analog circuit design are discussed in [18]. This active building block can mainly be used in mixed mode applications where fully differential signals can be processed.

2.7.2 Operational Floating Current Conveyor (OFCC)

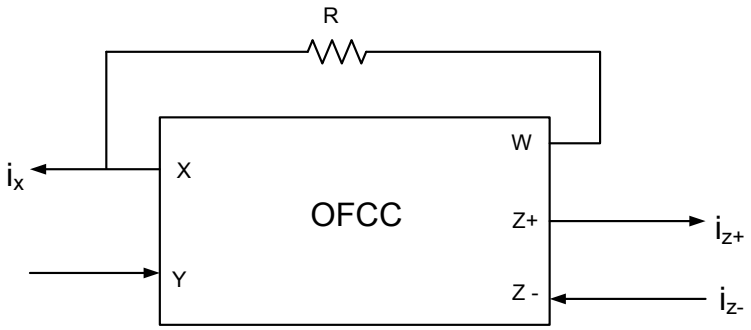
Operational floating current conveyor is a five terminal active building block. It is shown in fig.2.19 (a). OFCC combines the features of current conveyor (CC), current feedback operational amplifier (CFOA) and operational floating conveyor (OFC) [19]. It has two input terminals X, Y and three output terminals W, Z+, Z-. The X terminal has low impedance and is used as current input, while Y terminal shows high impedance and is used as input voltage terminal. The high output impedance output terminals Z+ and Z- give opposite polarity currents as output. The matrix defining the terminal equations of OFCC is given below:

$$\begin{bmatrix} i_Y \\ V_X \\ V_W \\ i_{Z+} \\ i_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & Z_t & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ i_X \\ i_W \\ V_{Z+} \\ V_{Z-} \end{bmatrix}$$

(2.16)



(a)



(b)

Fig. 2.19 (a) Operational floating current conveyor

(b) The OFCC configured as CCII- and CCII+ [19]

The OFCC can also be configured as second generation current conveyor (CCII) is shown in fig.2.19 (b). The applied input voltage V_Y appears at terminal X while current i_X is conveyed to the nodes Z+ and Z- with opposite polarity. So it can be used to configure both mode of CCII as CCII- and CCII+.

2.7.3 Current Controlled Conveyor (CCCII)

The CCCII was implemented using BJT in 1996 [20]. It is the derivative of second generation current conveyor (CCII) but it has the electronic tunability which is an advantage over the CCII. The CCCII as a circuit symbol is shown in fig.2.20. An inbuilt electronic tunability is absent in basic CCII but present in CCCII, by varying the bias current the parasitic resistance at terminal X can be controlled, this parasitic resistance is given as:

$$R_X = V_T/2I_b \tag{2.17}$$

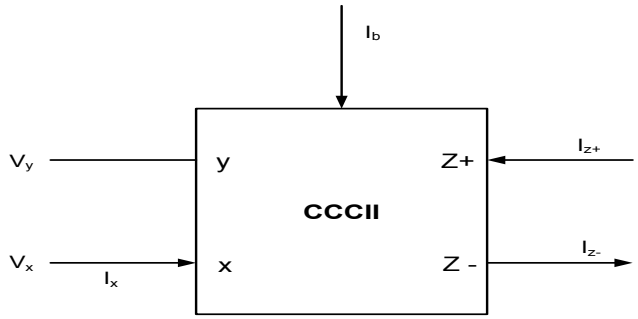


Fig. 2.20 Symbol of CCCII

The matrix defining the terminal equations of CCCII is given below:

$$\begin{bmatrix} V_x \\ I_y \\ I_z \end{bmatrix} = \begin{bmatrix} R_x & 1 & 0 \\ 0 & 0 & 0 \\ \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_x \\ I_z \end{bmatrix} \tag{2.18}$$

CCCII active block is extensively used in current mode filters, oscillators, amplifiers, radio frequency oscillators and low noise amplifiers, ASK/FSK modulators and various other analog signal processing applications. Several CMOS implementations of CCCII are discussed in [21]; each different configuration has different application specific advantages over classical CCII.

2.7.4 Current Controlled Fully Balanced Current Conveyor (CFBCCII)

The CFBCCII as a circuit symbol is shown in fig.2.21, here to provide electronic tunability bias current I_B is used. The Y input terminals exhibit high input impedance, where two

pairs of differential input terminals are configured by Y_1, Y_2, Y_3 and Y_4. X- and X+ terminals are used as voltage tracking terminals and current of X terminal is conveyed to Z port [22].

The ideal port characteristics of CFBCCII are expressed as follows:

$$I_{Y1} = I_{Y2} = I_{Y3} = I_{Y4} = 0$$

$$V_{X+} - V_{X-} = (V_{Y1} - V_{Y2}) + (V_{Y3} - V_{Y4}) + (I_{X+} - I_{X-})$$

$$I_{Z+} - I_{Z-} = I_{X+} - I_{X-} \tag{2.19}$$

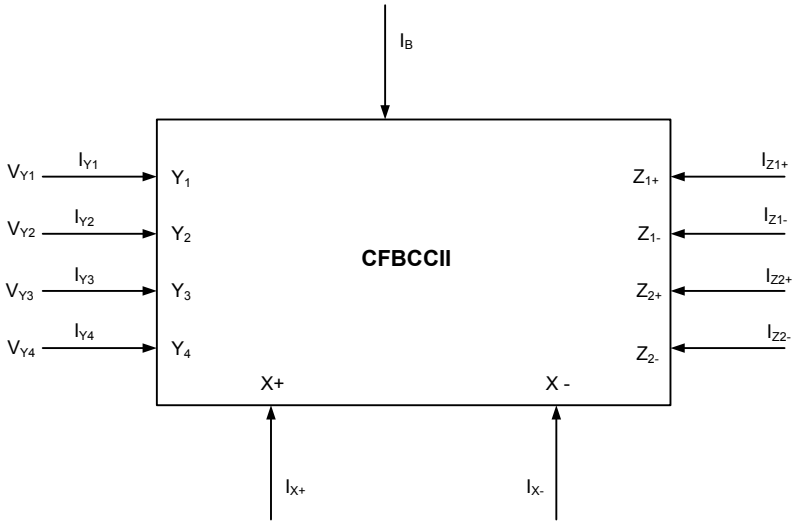


Fig. 2.21 Symbol of CFBCCII [22]

where, $R_X=f(I_B)$ is current controlled resistance which can be tuned by varying bias current I_B. CFBCCII consists of differential architecture and current controllability which are the two main properties that make it a more versatile active building block.

2.7.5 Universal Current Conveyor (UCC)

Universal current conveyor (UCC) is a versatile building block that is able to replace any type of existing current conveyors [23]. UCC is an eight port active building block where three input terminals (differential Y1, Y2 and summing Y3) show high impedance whereas X terminal shows mow-impedance. The UCC as a circuit symbol is given in fig.2.22 where currents on node Z1 and Z2 have their complementary currents also present.

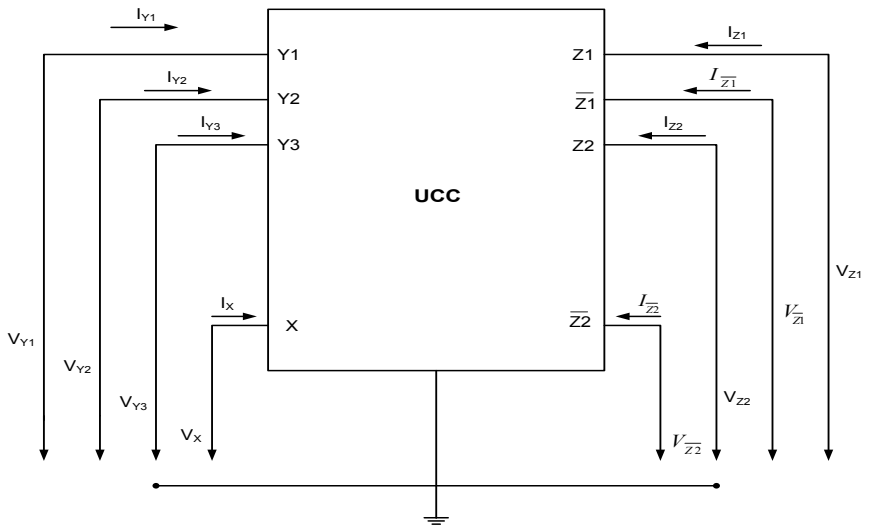


Fig. 2.22 Symbol of UCC [23]

$$\begin{bmatrix} i_{Y1} \\ i_{Y2} \\ i_{Y3} \\ V_X \\ i_{Z1} \\ i_{Z2} \\ i_{Z1'} \\ i_{Z2'} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ i_X \\ V_{Z1} \\ V_{Z2} \\ V_{Z1'} \\ V_{Z2'} \end{bmatrix} \tag{2.20}$$

The UCC can be used to derive several CC derivatives with appropriate connections. The procedure to realize CC derivatives has been explained in [23].

2.7.6 Dual-X Current Conveyor (DXCCII)

The DXCCII active building block combines the structures of basic CCII and Inverting Current Conveyor (ICCII). The DXCCII as a circuit symbol is shown in fig.2.23. It has a Y terminal and two X terminals, namely non-inverting terminal (X_P) and inverting terminal (X_N), as input terminals and I_{ZP} and I_{ZN} as output terminals.

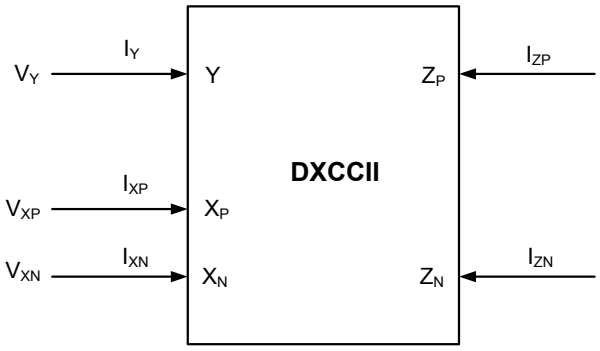


Fig. 2.23 Symbol of DXCCII [26]

The matrix showing terminal characteristic equations is given below:

$$\begin{bmatrix} I_Y \\ V_{XP} \\ V_{XN} \\ I_{ZP} \\ I_{ZN} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{XP} \\ I_{XN} \end{bmatrix} \tag{2.21}$$

The practical realization of DXCCII was done using only AD844 and rest with AD844 and op-amps [25]. This realization was used to design quadrature oscillator.

2.8 CONCLUSION

This chapter covers all the basic components which are used to design the almost several active building blocks, are as differential pair, active loads, current mirror, trans-linear buffer, current conveyor and OTA. Current conveyor is the mostly used active block to derive others. Types of current conveyors are mainly CCI, CCII and CCIII. Some derivatives of current conveyor are discussed such as FDCCII, OFCC, CCCII, CFBCCII, UCC and DXCCII. These active blocks are used to various analog signal processing applications as filters, oscillator, amplifier etc.

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CHAPTER 3

VDCC AND ITS BASIC APPLICATIONS

3.1 INTRODUCTION

In this chapter the focus of our discussion will be Voltage Differencing Current Conveyor (VDCC) and its application in signal processing. This block was introduced for the first time by Biolek, Senani, Biolkova and Kolka [1]. Till date only a few circuit applications of this building block have appeared in literature. The CMOS implementation of VDCC has been proposed by Kacar, Yesil, Minaei and Kuntman [2]. Till date only grounded inductor simulation [2] and floating inductor simulation [3] with their filter applications have been proposed in the written literature.

In this chapter we will discuss the applications of VDCC active block that have been proposed by Kacar, Yesil, Minaei and Kuntman [2] and Prasad and Ahmad [3]. This discussion forms the base for the work further done in this thesis in the field of applications of VDCC active block. The complete characterization of VDCC using 0.18μm CMOS technology has been presented in PSPICE. PSPICE simulations have been carried out to verify the workability of all these circuits.

3.2 VOLTAGE DIFFERENCING CURRENT CONVEYOR

3.2.1 Circuit Description

The circuit symbol of the active block, VDCC, is shown in Fig.3.1, where p and n are input terminals and z, x, W_p and W_n are output terminals.

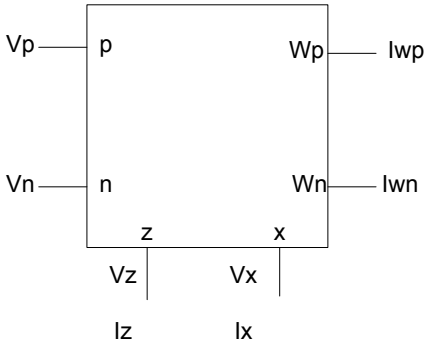


Fig.3.1: Symbol of VDCC

All of the terminals exhibit high impedance, except the x terminal. Using standard notation, the port relations of an ideal VDCC shown in the matrix below:

$$\begin{bmatrix} I_n \\ I_p \\ I_z \\ V_x \\ I_{Wp} \\ I_{Wn} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_p \\ V_n \\ V_z \\ I_x \end{bmatrix} \tag{3.1}$$

The behavioral model of Voltage Differencing Current Conveyor is shown in fig.3.2. From the behavioral model of VDCC we can see that the VDCC consists of an Operational Trans-conductance amplifier (OTA) on the input side and a Multiple Output Second Generation Current Conveyor (MO-CCII) on the output side [1-2].

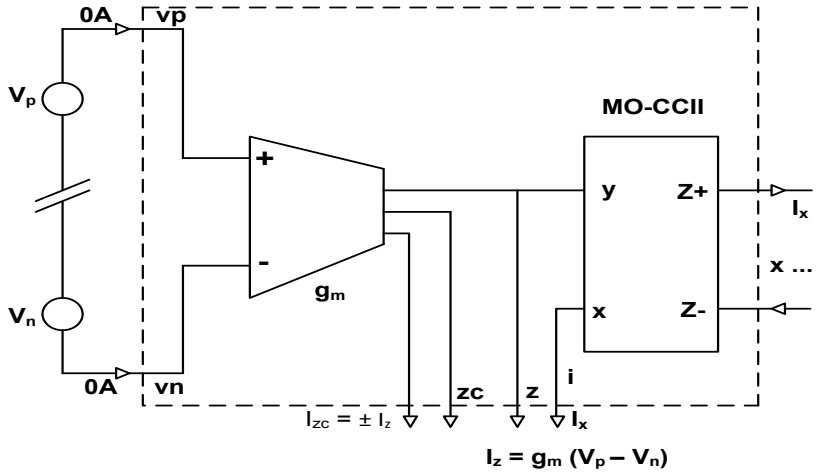


Fig.3.2 The behavioral model of VDCC [1]

The CMOS realization of VDCC is shown in fig.3.3.

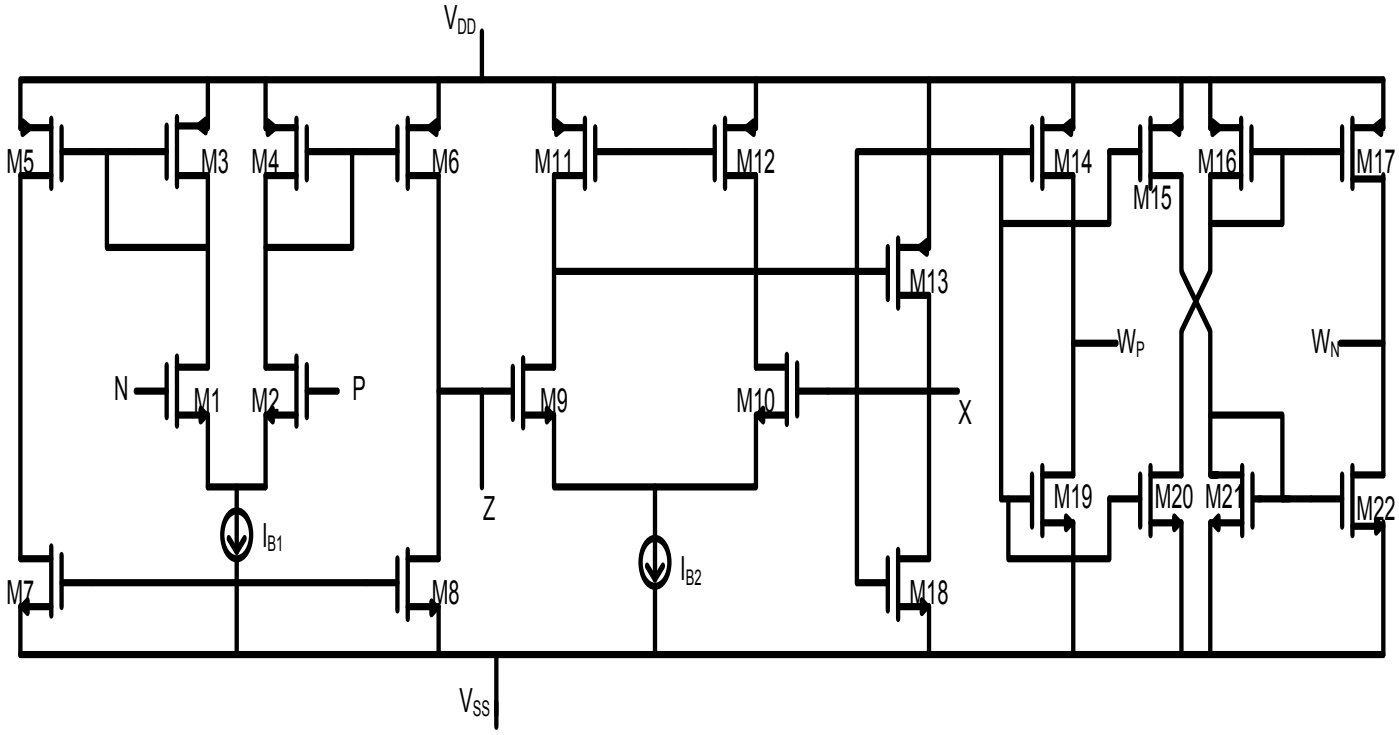


Fig.3.3: CMOS realization of VDCC [2]

3.2.2 Simulation Results

The CMOS schematic of VDCC shown in fig.3.3 was simulated in PSPICE using TSMC CMOS 0.18μm model parameters [2]. The aspect ratios of the transistors used are given in Table 1. The supply voltages are chosen as $V_{DD} = -V_{SS} = 0.9V$, $I_{B1} = 50\mu A$ and $I_{B2} = -100\mu A$. The following analysis has been carried out:

(i) DC sweep (to obtain the linear voltage for various current and voltage transfers),

(ii) AC sweep (to obtain the bandwidth of the device).

The following terminating impedances were used in characterization of the VDCC as Rz= 9kΩ, Rx= 100Ω, Rwp= 100Ω, Rwn= 100Ω. The input signal for AC sweep was taken as 3 mV with frequency 10MHz.

Table: 3.1 Transistors aspect ratios for the VDCC of fig.3.3

Transistors	W/L (μm)
$M_1 - M_4$	3.6/1.8
$M_5 - M_6$	7.2/1.8
$M_7 - M_8$	2.4/1.8
$M_9 - M_{10}$	3.06/0.72
$M_{11} - M_{12}$	9/0.72
$M_{13} - M_{17}$	14.4/0.72
$M_{18} - M_{22}$	0.72/0.72

Different parameters obtained by PSPICE simulations of VDCC are listed as:

Transconductance g_m= 277μA/V

Power consumption = 0.90mW

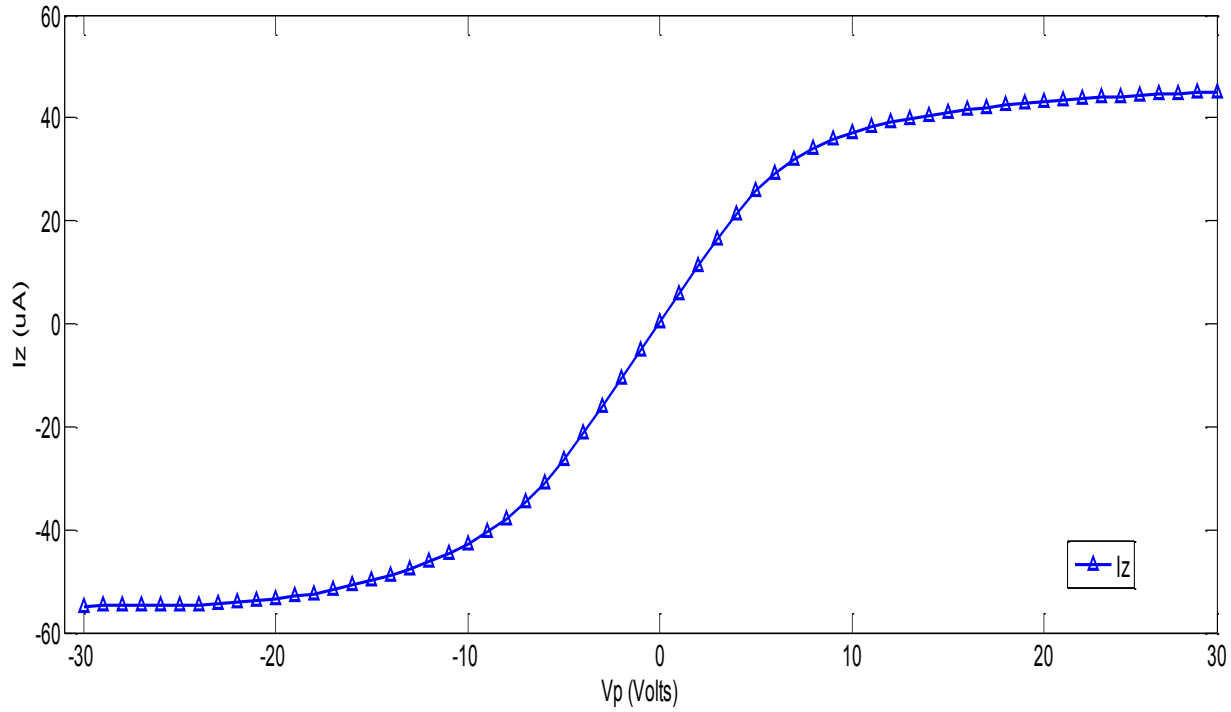


Fig. 3.4 Input DC characteristic of VDCC

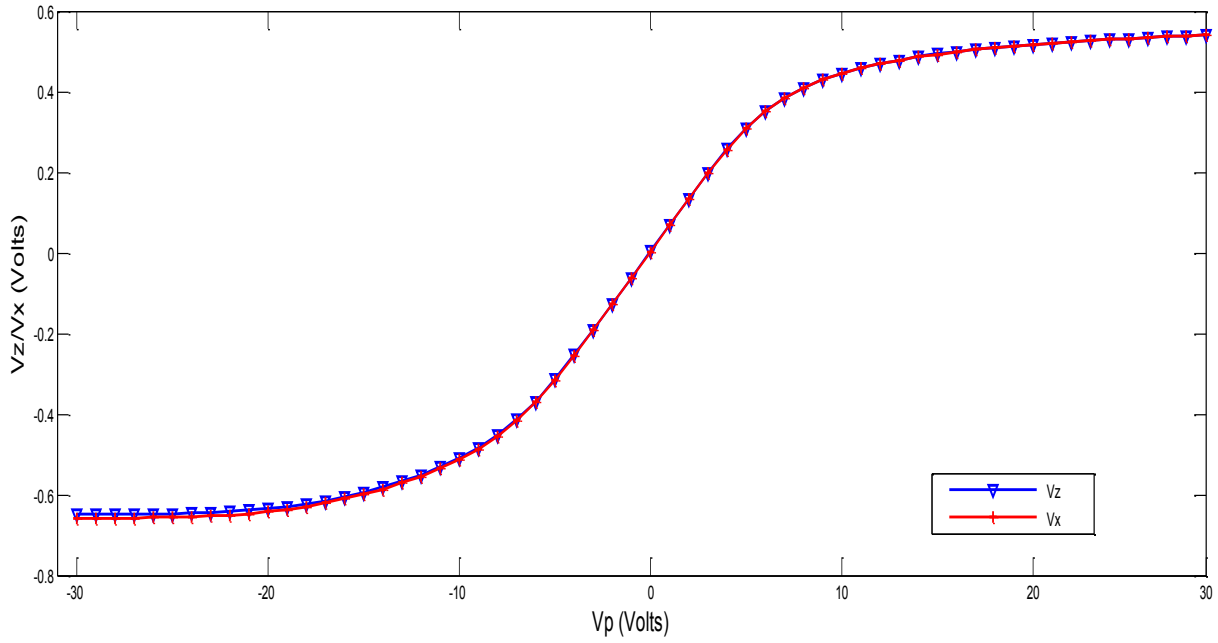


Fig. 3.5 DC characteristic of Vz and Vx terminal of VDCC

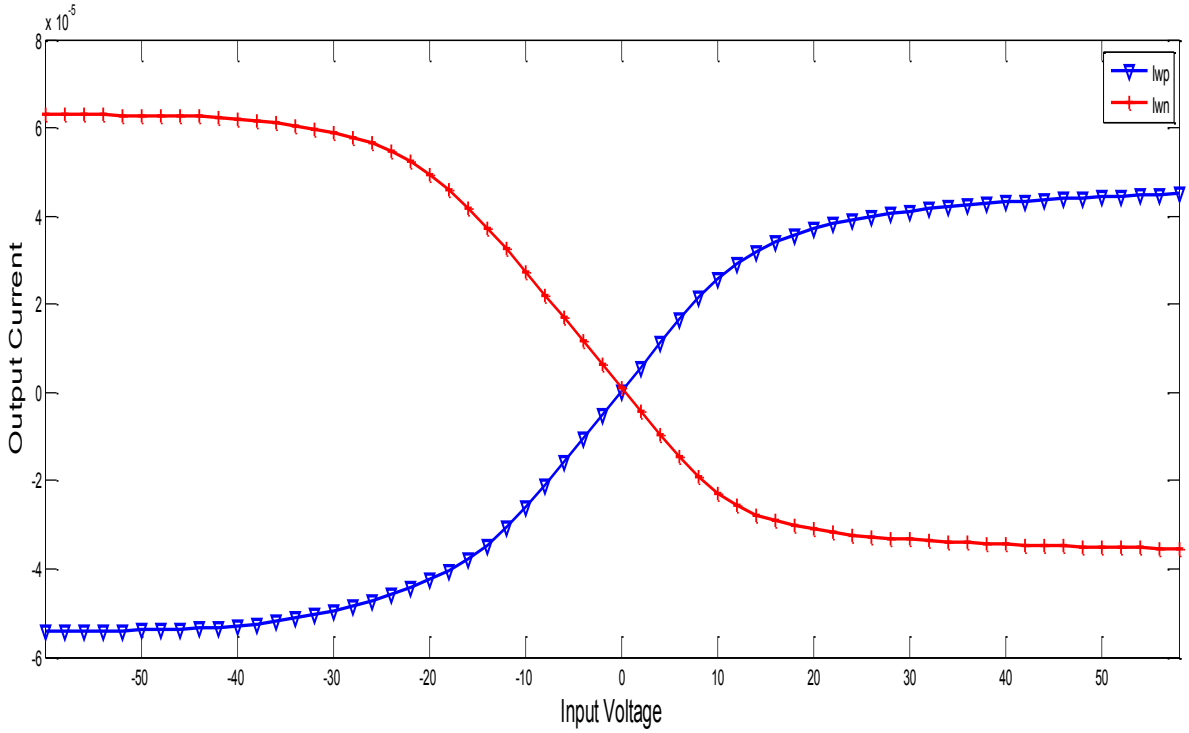


Fig. 3.6 Output DC characteristic of VDCC

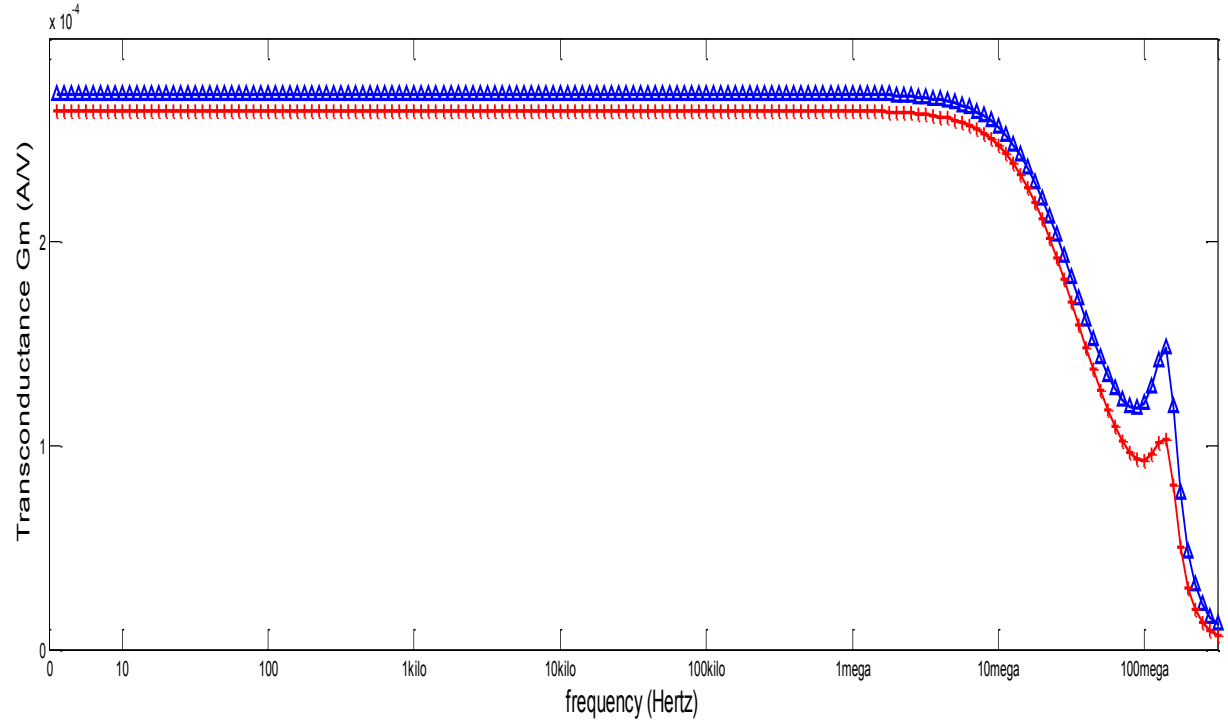


Fig. 3.7 Input AC characteristic of VDCC

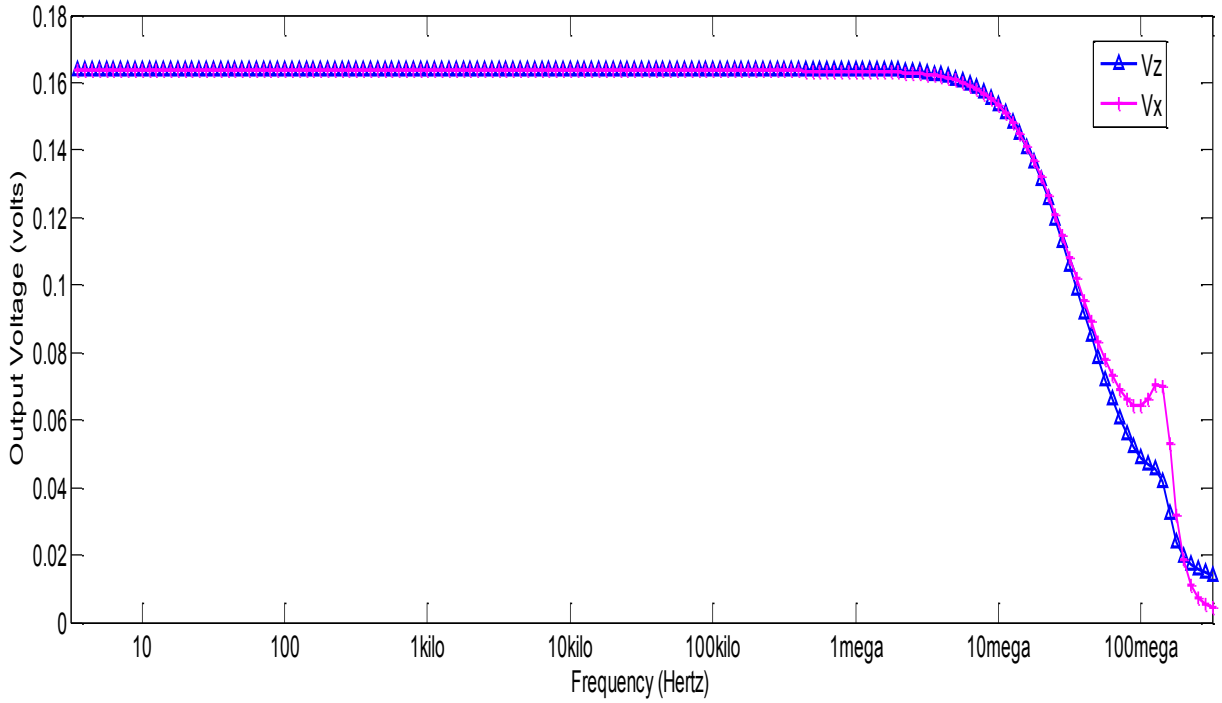


Fig. 3.8 AC characteristic of Vz and Vx terminal of VDCC

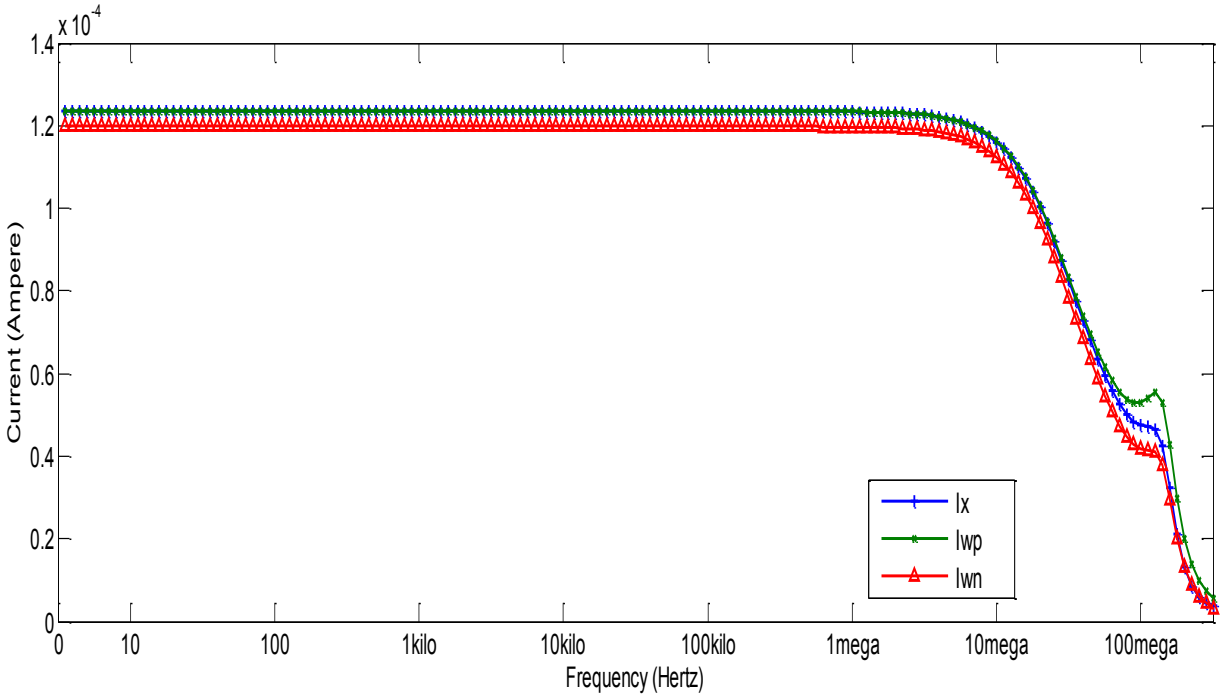


Fig. 3.9 Output AC characteristics of VDCC

3.3 APPLICATION OF VDCC IN CURRENT MODE SIGNAL PROCESSING

3.3.1 Amplifier

An amplifier gives the output that is scaled version of an input current signal. Broadly amplifiers can be classified on the basis of their circuit configuration and methods of operation. In real world, sensors like piezo-electric, thermocouple etc. have small output signal. So by using amplifier their outputs can be amplified to drive the further circuitry such as lamp. Gain is basically ratio of the output divided by the input thus a unit-less quantity. In electronics, three types of amplifier gain can be measured such as Voltage Gain (Av), Current Gain (Ai) and Power Gain (Ap) [5]. Further amplifier can be classified on the basis of polarity of input and output. In inverting amplifier, output signal has opposite sign to the input signal. On the other hand, non-inverting amplifier gives output signal same as input signal polarity. VDCC based amplifier is shown in fig.3.10 which gives current gain. In this circuitry, if Wp is used as a output terminal then it is called as non-inverting amplifier. In contrast, if Wn is used as the output then its characteristic shows as inverting amplifier. By using single VDCC, it can be designed for the

both inverting and non-inverting amplifier but this case is not found in the Op-amp. In the case of Op-amp, separate circuit is designed for both types of amplifier. So, the beauty of VDCC based amplifier is that only choosing the output terminal which gives the opposite polarity, inverting and non-inverting. VDCC based amplifier has also some advantages over Op-amp based amplifier such as large bandwidth, less power supply, less power consumption and high slew rate etc. [2]. A simplified amplifier circuit of Fig. 3.10 is shown in Fig. 3.11. In this, OTA is used as a resistor which gives the less use of passive elements and also provides electronic tunability. The current gain for the Fig. 3.10 is described as follows:

For non-inverting amplifier

$$\frac{I_{Wp}}{I_{in}} = \frac{R_1 R_2 g_m}{R_3} \tag{3.2}$$

And inverting amplifier

$$\frac{I_{Wn}}{I_{in}} = -\frac{R_1 R_2 g_m}{R_3} \tag{3.3}$$

The current gain for the fig.3.11 is defined as follows

For non-inverting amplifier

$$\frac{I_{Wp}}{I_{in}} = A_i = \frac{1}{g_m R_1} \tag{3.4}$$

Inverting amplifier

$$\frac{I_{Wn}}{I_{in}} = A_i = -\frac{1}{g_m R_1} \tag{3.5}$$

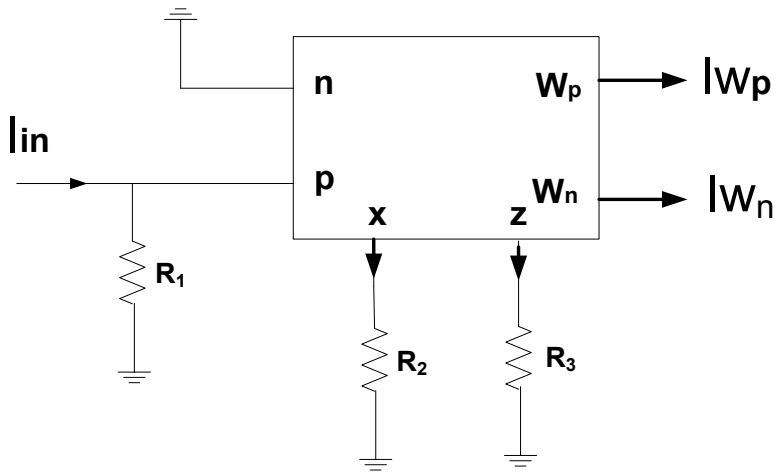


Fig. 3.10 VDCC based amplifier

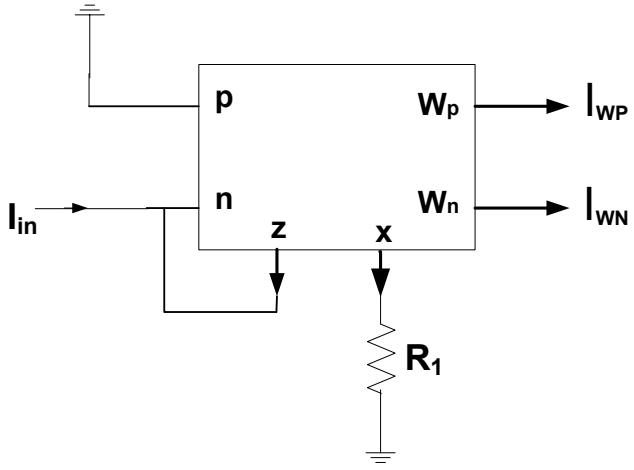


Fig. 3.11 Simplified amplifier using VDCC

3.3.1.1 Simulation Results

The amplifier is shown in Fig. 3.11 was simulated in PSPICE. The supply voltages, were selected as V_{DD} = - V_{SS} = 0.9V and bias currents I_{B1} = 50μA and I_{B2} = 100μA. The grounded resistor's value was selected as R_1 = 11k, R_2=3k, R_3=8k. The time and frequency responses of the Fig. 3.11 are shown in Fig. 3.12 and Fig. 3.13 respectively.

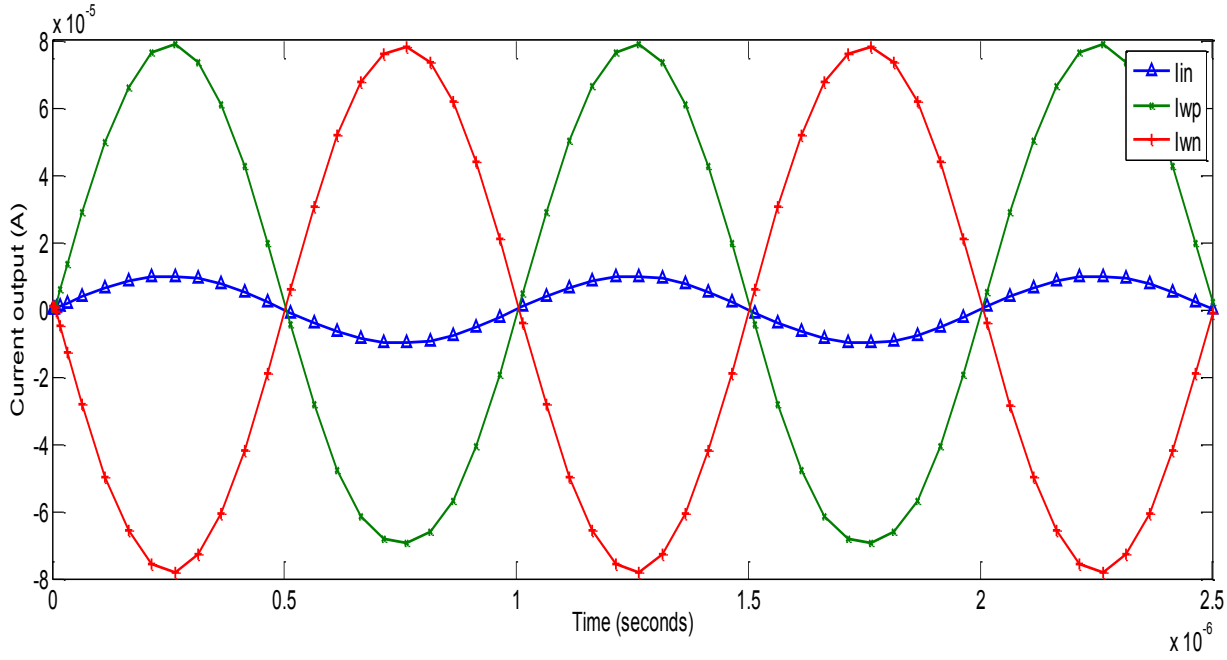


Fig. 3.12 Time response of amplifier circuit shown in Fig. 3.10

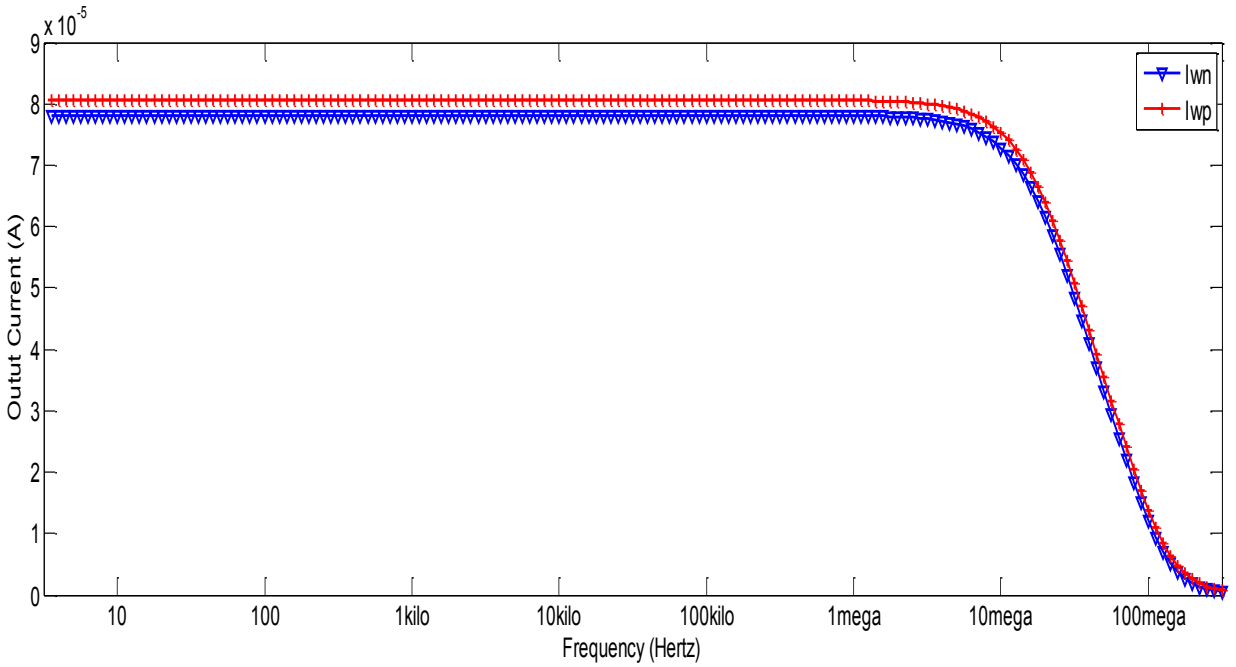


Fig. 3.13 Frequency response of the amplifier shown in Fig. 3.10

3.3.2 Differentiation

Differentiation is a linear operation in analog signal processing that gives the derivative of the signal processed. Differentiation can be used as peak detector: the derivative of a signal gives a zero crossing whenever the analog signal attains a peak value. If a signal is filtered and then passed through the differentiator, this method is more robust then detecting the peak amplitude because added noise could give erratic outcomes [5]. A current mode VDCC [2] based differentiator is shown in Fig. 3.14. In which one grounded capacitor and two grounded resistors are used to realize this circuit. The input-output relation can be characterized as:

$$\frac{I_{Wp}}{I_{in}} = R_1 R_2 g_m C_3 s \tag{3.6}$$

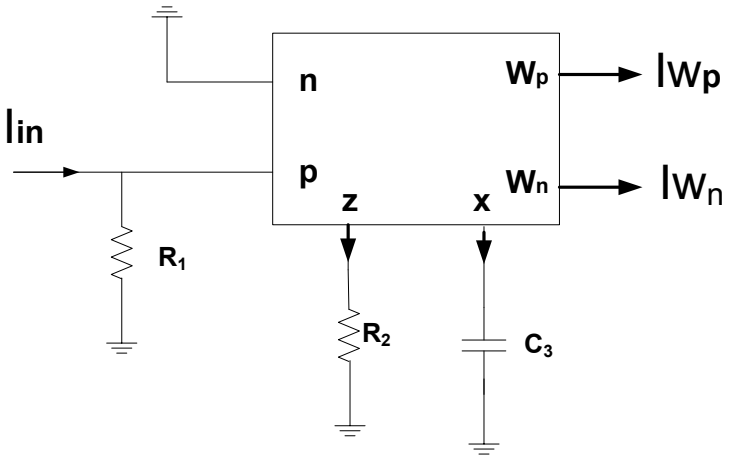


Fig. 3.14 Circuit diagram of differentiator using VDCC

3.3.2.1 Simulation Results

The integrator is shown in Fig. 3.14 was simulated using PSPICE. The supply voltages, were selected as V_{DD} = - V_{SS} = 0.9V and bias currents I_{B1} = 34.5µA and I_{B2} = 100µA. The passive elements were selected as R_1 = 500, R_2 = 1k and C_3= 13pF. The time response of the Fig. 3.14 is shown in Fig. 3.15.

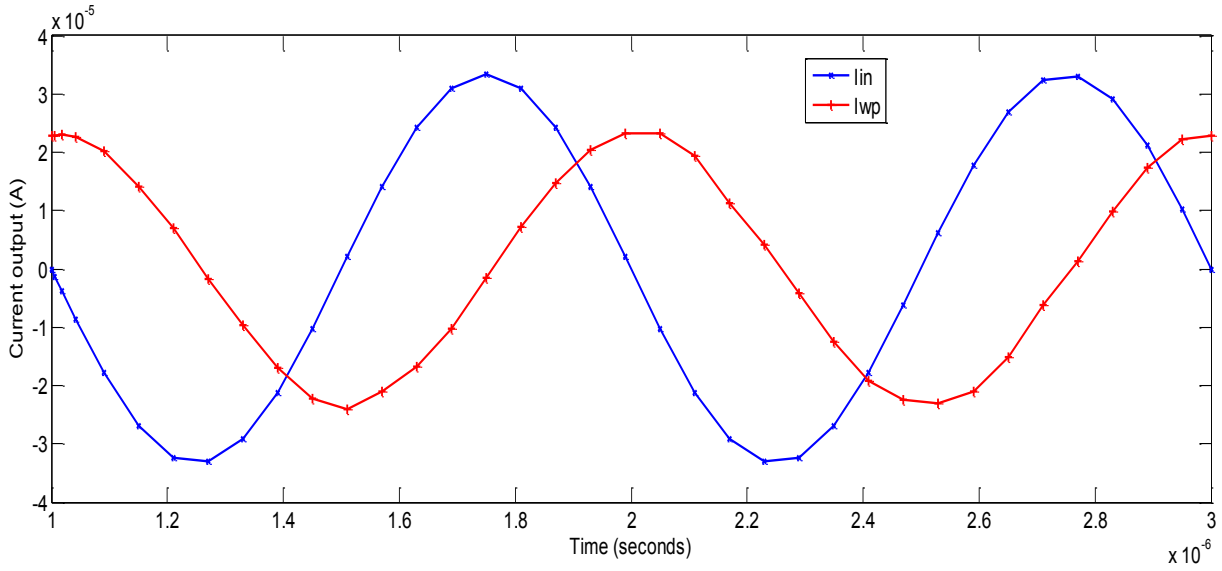


Fig. 3.15 Time response of differentiator circuit shown in Fig. 3.20

3.3.3 Integration

Integration is a basic linear function in analog signal processing. Mathematically, the integral give the area under the waveform or analog signal. In frequency domain, integration is defined by a transfer characteristic whose slope decreases by 20dB/decade. VDCC based Integrator circuit is shown in Fig. 3.22 and its transfer function is defined as:

$$\frac{I_{Wp}}{I_{in}} = \frac{R_1 g_m}{R_3 C_2 s} \tag{3.7}$$

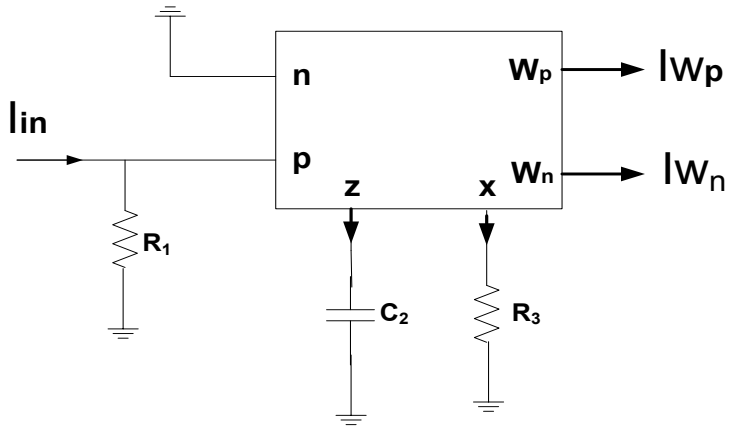


Fig. 3.16 VDCC based ideal integrator

3.3.3.1 Simulation Results

The integrator is shown in Fig. 3.22 was simulated using PSPICE. The supply voltages, were selected as V_{DD} = - V_{SS} = 0.9V and bias currents I_{B1} = 34.2µA and I_{B2} = 100µA. The passive elements were selected as R_1 = 500Ω, R_3 = 1k Ω and C_2= 13pF. The time response of the Fig. 3.22 is shown in Fig. 3.23.

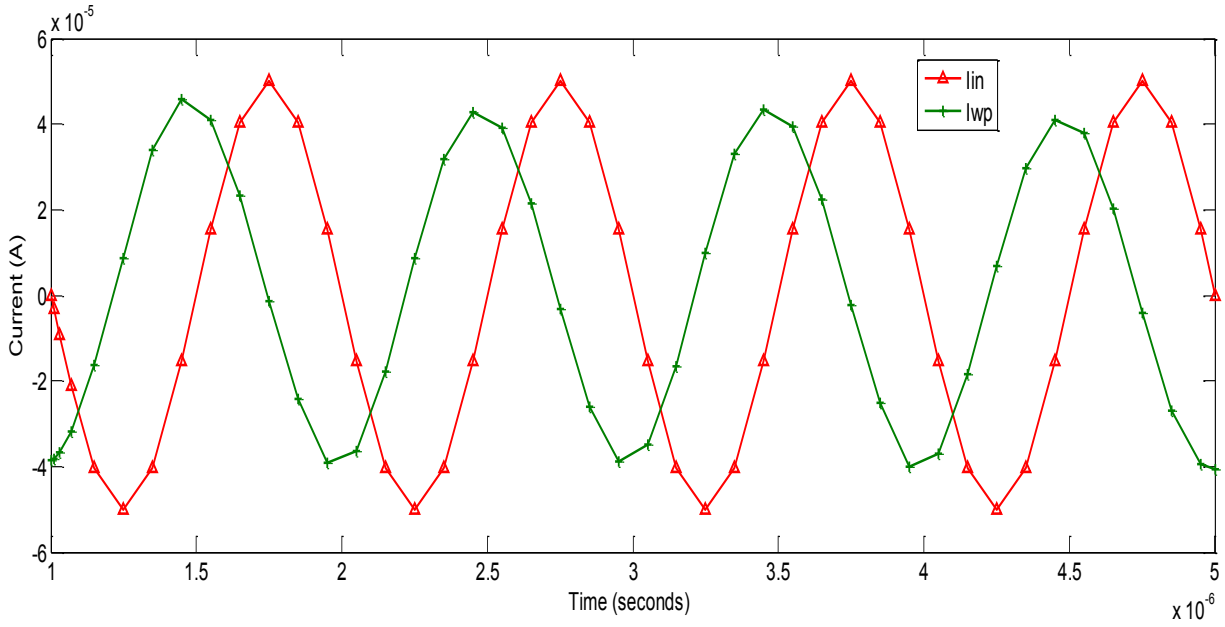


Fig 3.17 Time response of integrator circuit is shown in Fig. 3.22

3.4 VDCC BASED GROUNDED INDUCTANCE SIMULATION

VDCC based grounded inductance simulator circuit was proposed by Kacar, Yesil, Minaei and Kuntman [2]. The circuits for realization of grounded inductance are shown in Fig. 3.18. The entire configurations are designed with single VDCC, one grounded resistor and one grounded capacitor. By circuit analysis of these simulated inductor configuration, the input impedance, equivalent inductance and equivalent resistance are given in Table 3.2. Negative simulated inductor is used for many applications like designing of oscillators, active filters, impedance matching and analog phase shifter.

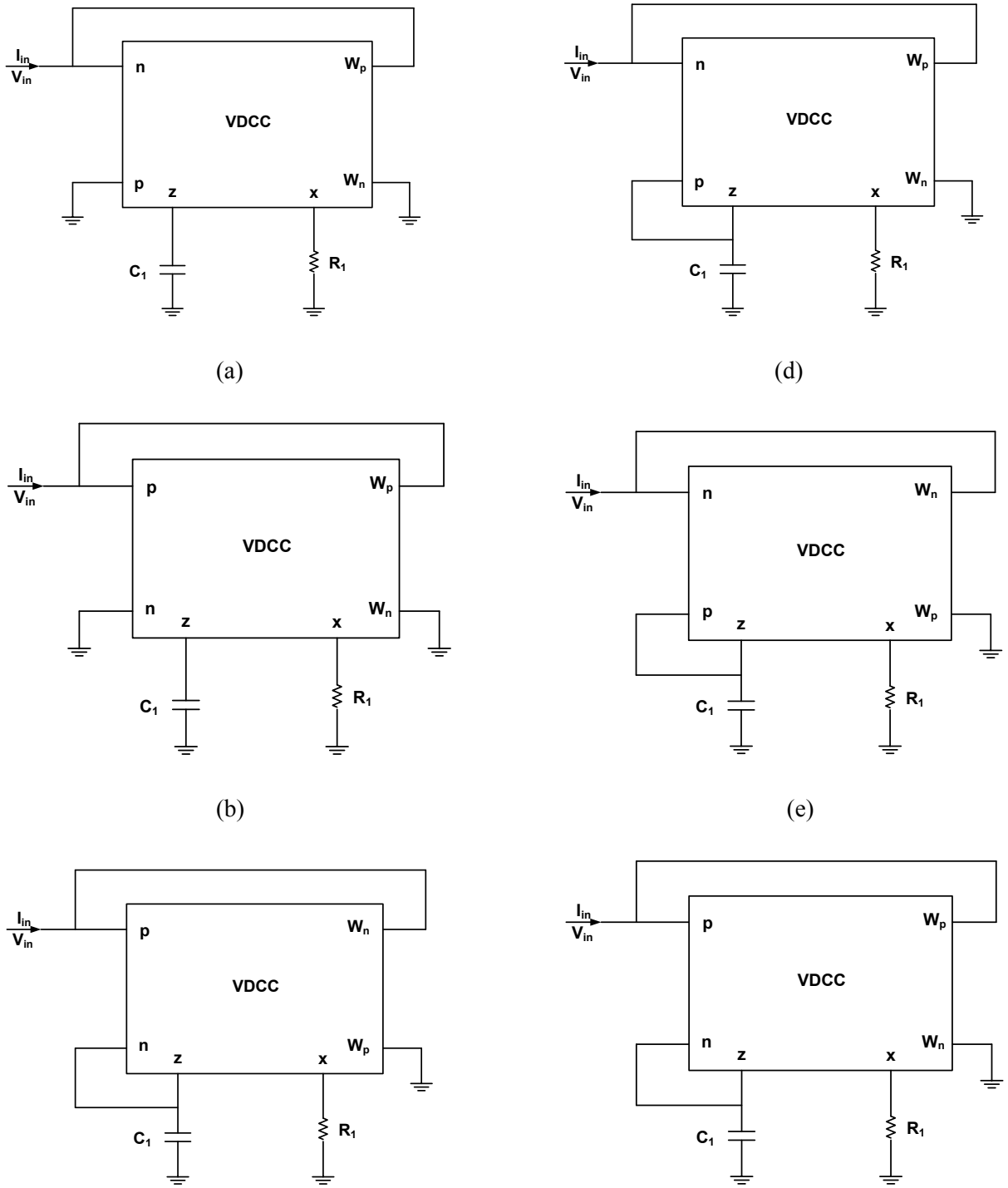


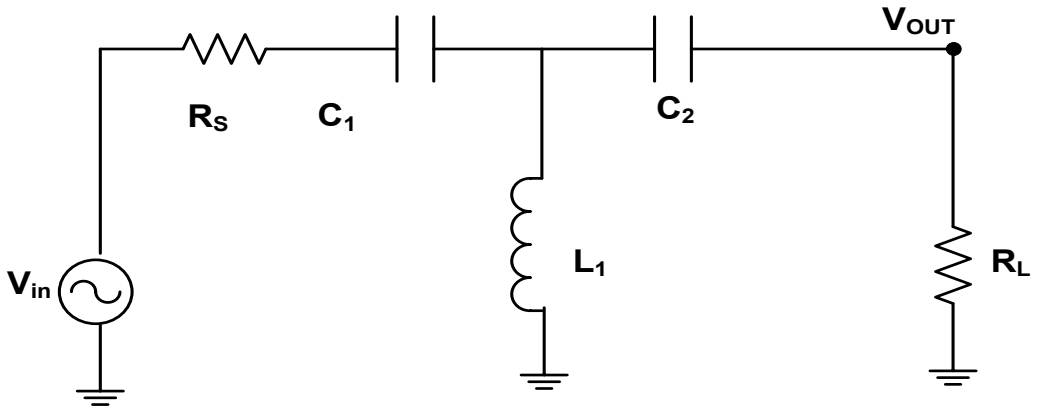
Fig. 3.18 Inductance simulators realized using VDCC [2]

Table 3.2: The actively realizable inductance forms.

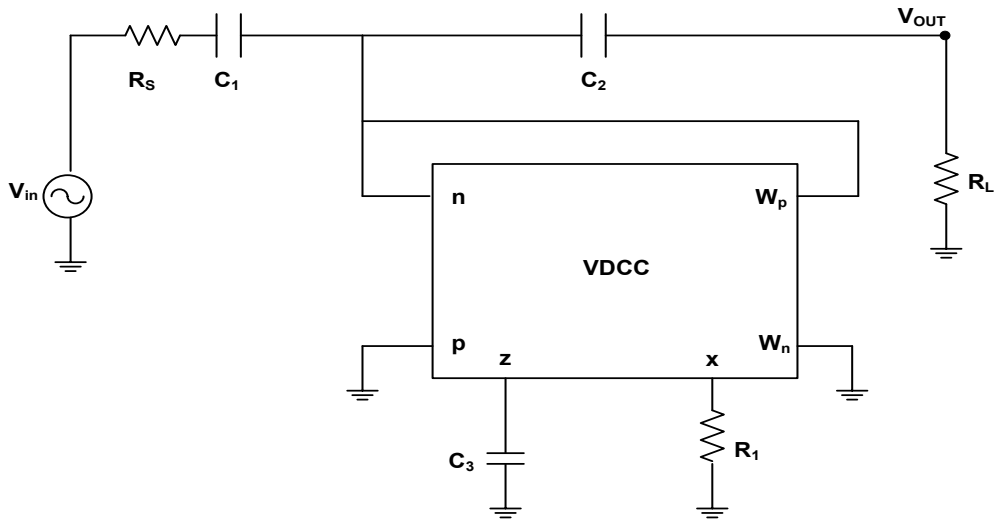
Circuit	Z_{eq} input impedance	L_{eq} input impedance	R_{eq} input resistance	Type
Fig.3.18a	$s\frac{C_1R_1}{g_m}$	$\frac{C_1R_1}{g_m}$	–	Pure L
Fig.3.18b	$-s\frac{C_1R_1}{g_m}$	$-\frac{C_1R_1}{g_m}$	–	Pure -L
Fig.3.18c	$s\frac{C_1R_1}{g_m}+R_1$	$\frac{C_1R_1}{g_m}$	R_1	+L series with +R
Fig.3.18d	$s\frac{C_1R_1}{g_m}-R_1$	$\frac{C_1R_1}{g_m}$	$-R_1$	+L series with -R
Fig.3.18e	$-s\frac{C_1R_1}{g_m}+R_1$	$-\frac{C_1R_1}{g_m}$	R_1	-L series with +R
Fig.3.18f	$-s\frac{C_1R_1}{g_m}-R_1$	$-\frac{C_1R_1}{g_m}$	$-R_1$	-L series with -R

3.4.1 Application Example of New Grounded Inductance

Passive prototype of the third order Butterworth high-pass filter is shown in Fig. 3.19(a). In this circuit, grounded inductance is used which can be replaced by the simulated inductance. The VDCC based simulated grounded inductance is used in Fig. 3.19(b) to design a HPF where for pure inductance is taken from Fig. 3.18(a).



(a)



(b)

Fig. 3.19 3rd order high pass Butterworth filter (a) Passive realization

(b) Realization with VDCC based inductance simulator [2]

3.4.2 Simulation Results

The simulated inductance (Fig. 3.18a) was used to design a 3rd order high-pass filter and verified the performance of simulated grounded inductance. The supply voltages, were selected as $V_{DD} = -V_{SS} = 0.9V$ and constant bias currents are $I_{B1} = 37\mu A$ ($g_m = 100.5\mu A/V$), $I_{B2} = 50\mu A$. The passive elements are selected as $R_S = R_L = 10k\Omega$, $C_1 = C_2 = 15.9pF$, $R_1 = 4k\Omega$ and $C_3 = 20pF$, which results in $L_{eq} = 796\mu H$. The frequency response of 3rd order HPF is shown in Fig. 3.20.

To find out the input range of the 3rd order HPF a sinusoidal signal of $f_0 = 1MHz$ with different amplitudes of input are applied. The THD of the output signal versus amplitude of input is shown in Fig. 3.21. By PSPICE simulation, the power dissipation of the filter was calculated as 0.845mW which is acceptable to design an IC implementation.

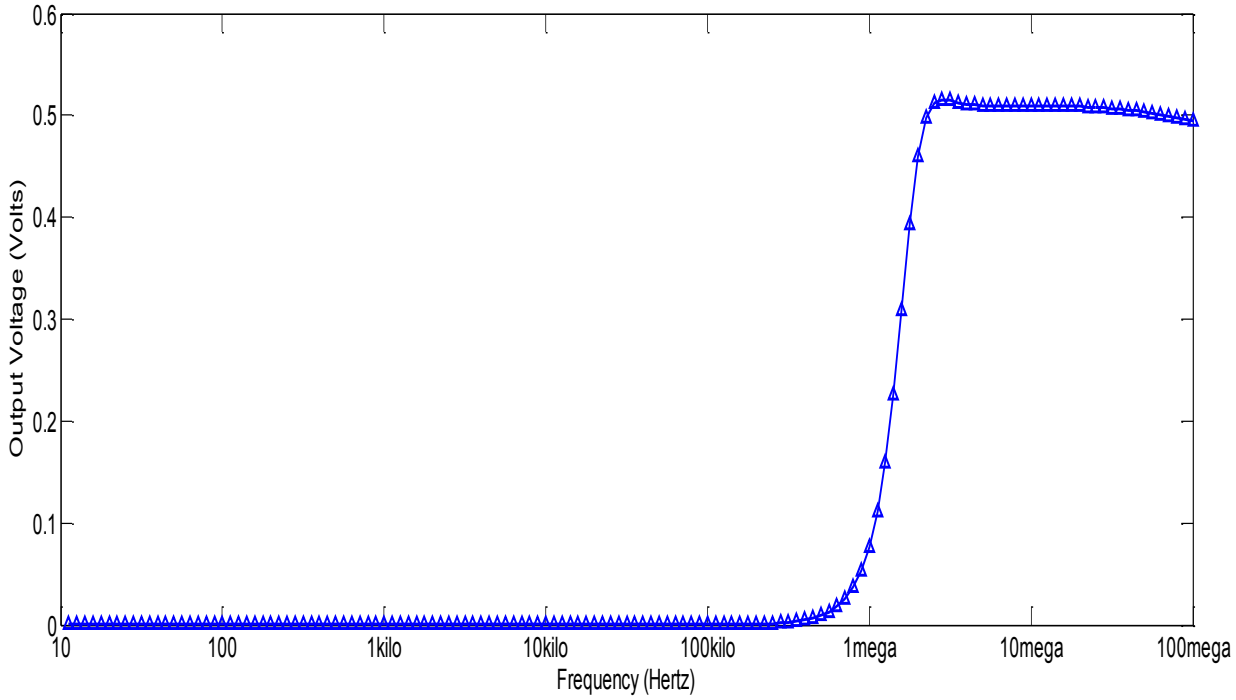


Fig. 3.20 Frequency response of 3rd order Butterworth high-pass filter

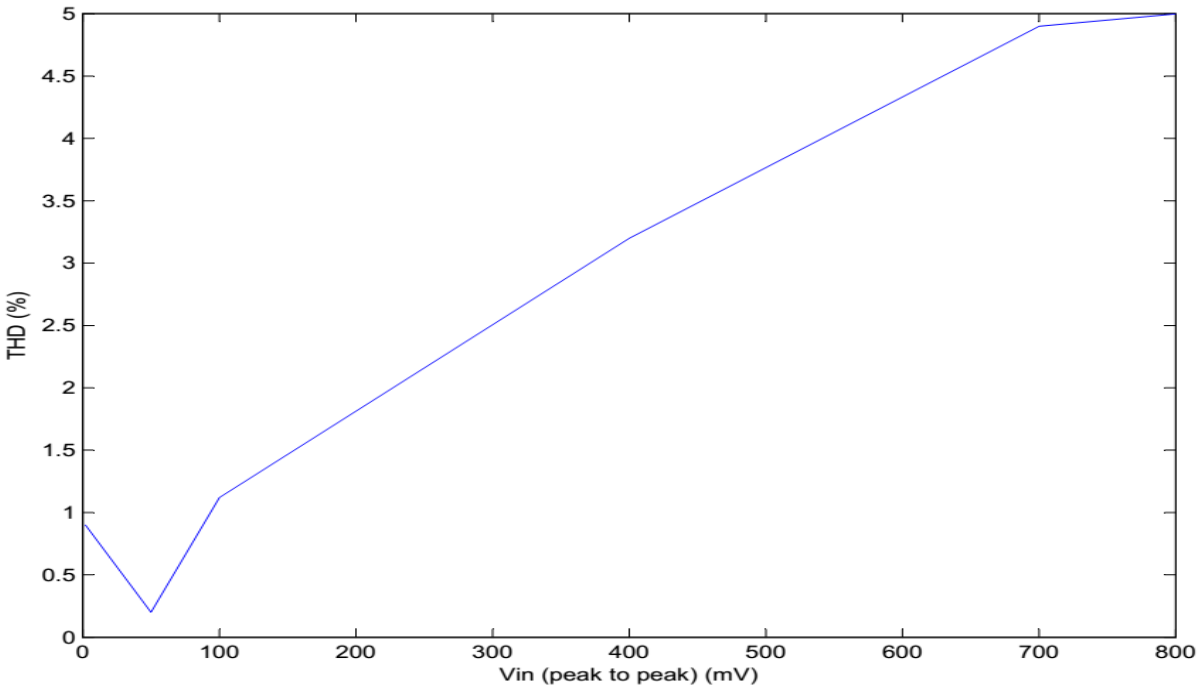


Fig. 3.21 Total harmonic distortion of high pass filter

3.5 ELECTRONICALLY CONTROLLABLE SYNTHETIC FLOATHING INDUCTANCE USING VDCC

The floating inductance simulator was proposed by Prasad and Ahmad [3]. The block diagram of VDCC based floating inductance simulator is shown in Fig. 3.22. This floating inductance (FI) is realized only using single VDCC active building block, one grounded resistor and one grounded capacitor (as desired for IC implementation). The circuit analysis of Fig. 3.22 is defined as

$$\begin{matrix} I_1 \\ I_2 \end{matrix} = \frac{g_m}{sCR} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \begin{matrix} V_1 \\ V_2 \end{matrix} \tag{3.8}$$

The equivalent inductance value is given as

$$L_{eq} = \frac{CR}{g_m} \tag{3.9}$$

where g_m is defined as transconductance gain which can be controlled by bias current [2]. So FI is called electronically-controlled FI.

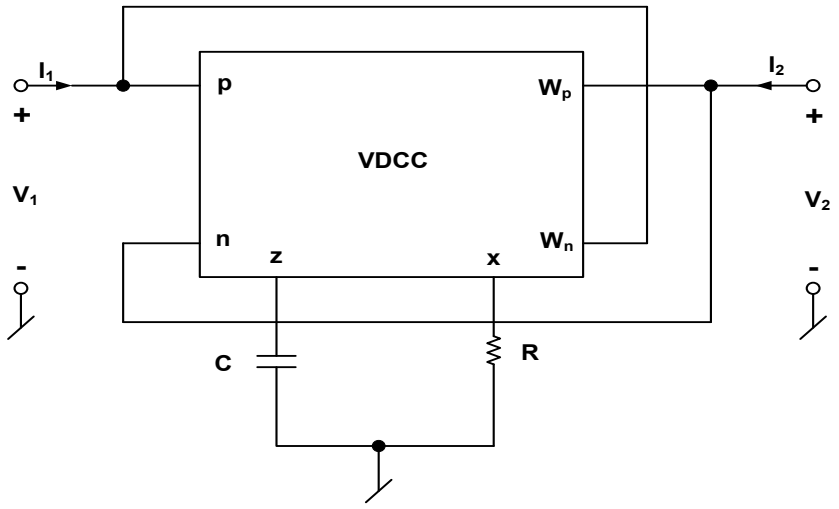


Fig. 3.22 VDCC based Floating Inductance [3]

3.5.1 Application Example of Floating Inductance Circuit

Floating inductor is used in many applications such as designing of ladder circuits, filters and oscillators etc. The filter application of FI circuit is demonstrated to implement band pass filter (BPF). The transfer function for the band pass filter is given below as was defined in [2, 3]:

$$\frac{V_0}{V_{in}} = \frac{s\left(\frac{g_m}{C_1}\right)}{s^2 + s\left(\frac{g_m}{C_1}\right) + \frac{g_m}{C_1 C_2 R_2}} \tag{3.18}$$

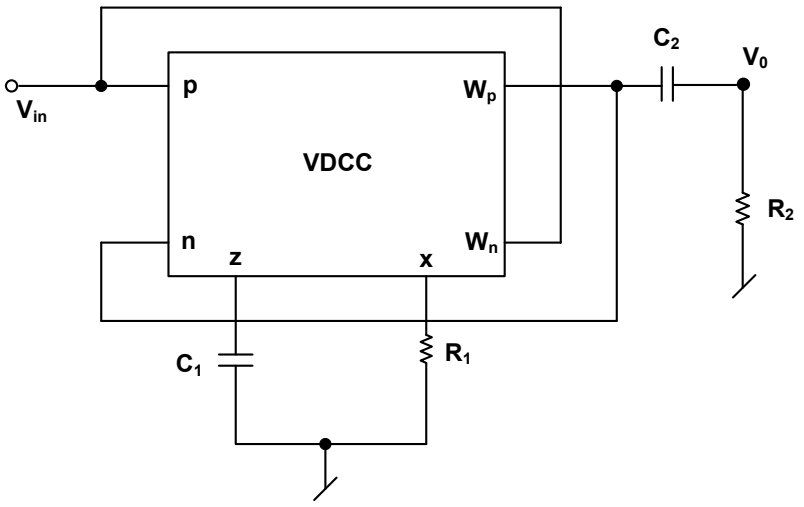


Fig. 3.23 Band pass filter implemented using FI circuit of Fig. 3.22

3.5.2 Simulation Results

The VDCC based simulated floating inductance (FI) (Fig. 3.22) is used to design a band-pass filter and verified the performance of floating inductance. The supply voltages, are selected as $V_{DD} = -V_{SS} = 0.9V$ and constant bias currents are $I_{B1}= 50\mu A$ ($g_m = 277\mu A/V$), $I_{B2} = 100\mu A$. The passive elements are selected as $R_1= 10k\Omega$, C1= 0.01nF, $R_2= 3.6k\Omega$ and $C_2= 0.02nF$. The frequency response and time response are shown in Fig. 3.24 and Fig. 3.25 respectively. The simulated center frequency (f_0) was found 1.99MHz. The other filter parameters were calculated using PSPICE simulation as below:

Total harmonic distortion at input frequency 2MHz = 2.91%

Total power dissipation = 0.845mW

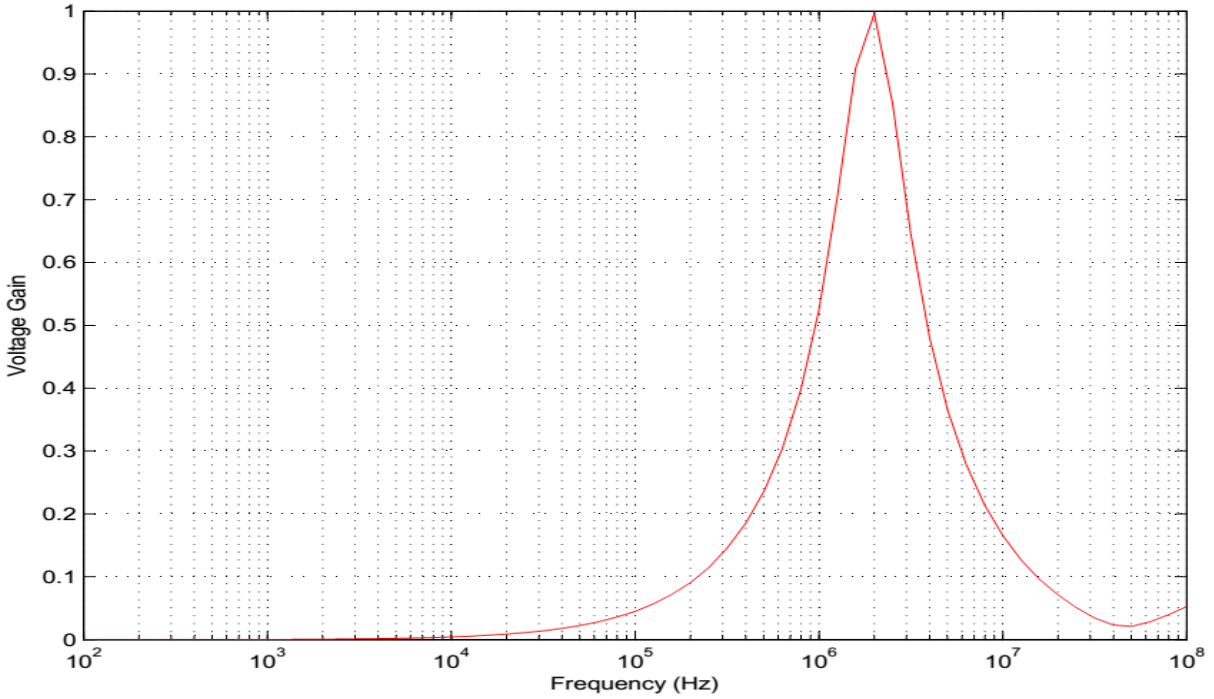


Fig. 3.24 Frequency response of band-pass filter

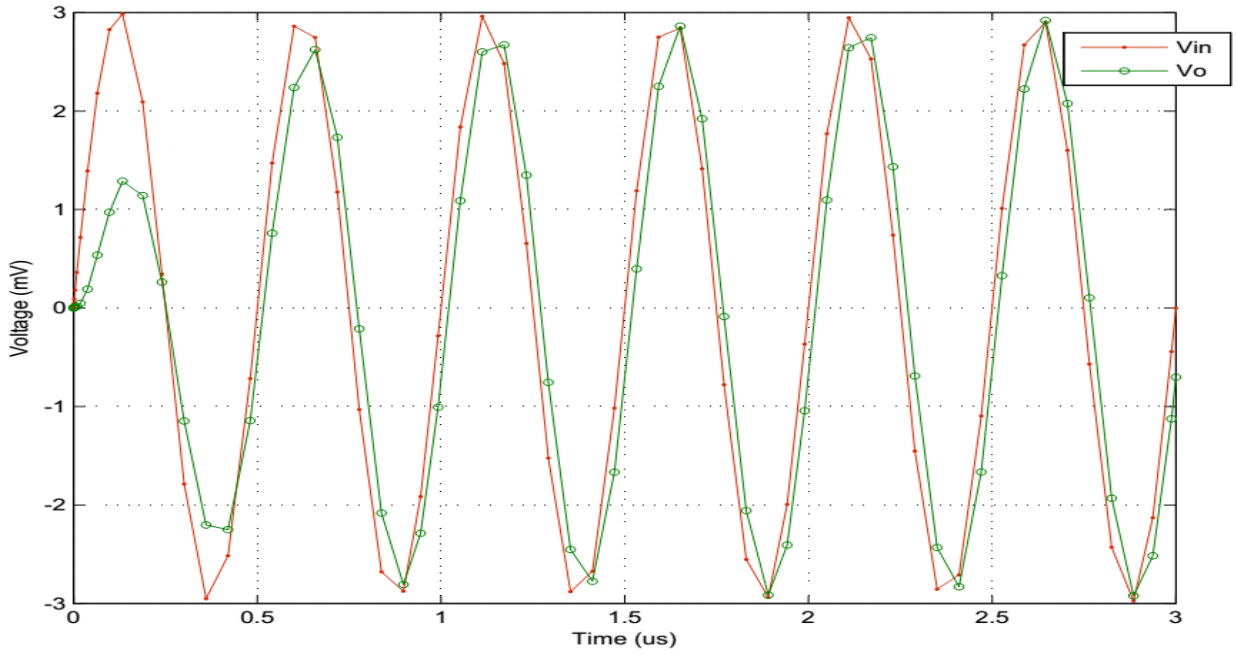


Fig. 3.25 Transient response of band-pass filter

3.6 CONCLUSION

In this chapter, a novel active building block namely the VDCC is discussed in detail. Its MOSFET model is implemented as was proposed earlier. The DC and AC characteristics of input-output of the MOSFET model were verified using PSPICE simulation with TSMC 0.18μm parameters. The basic signal processing applications such as differentiator, integrator and amplifier were designed using VDCC which helped in the thorough understanding of the VDCC as an active block and simulated in PSPICE.

In the section 3.4, grounded inductance simulation was described and applied to design a high-pass filter. In yet another application, floating inductance was designed and simulated in PSPICE. The floating inductance was verified using PSPICE simulation of the band pass filter (BPF) with specified central frequency. The inductors form the basis for the realization of filters and oscillators.

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CHAPTER 4

ADVANCED APPLICATIONS OF VDCC: PROPOSED CONFIGURATIONS

4.1 INTRODUCTION

In the previous chapter some basic applications of VDCC in current mode signal processing have been discussed. The VDCC as an active building block appears to be very versatile similar to other derivatives of current conveyors which were presented in chapter-2. A VDCC combines the features of a current conveyor (CC) and an operational transconductance amplifier (OTA). In the present chapter we have proposed some novel applications of VDCC in the realization of voltage mode and current mode universal biquad filters and voltage mode and current mode oscillators.

Before we present the circuit of the multifunction filter it is worthwhile to have a review of multifunction/universal filters and oscillators.

Realization of filters, particularly biquad filters is always one of the prominent applications of any active building block. Out of different filter configurations implemented using these blocks universal / multifunction filter realizations are preferred as they provide multiple filter function from the single structure. Their usual application is as standard second-order building blocks for higher order filters, apart from this multifunction biquad filters (e.g. those realizing any three out of lowpass (LP), bandpass (BP), notch and high-pass (HP) simultaneously from three different output terminals) find applications in phase locked loop FM stereo demodulators, touch tone telephone systems and crossover networks used in three-way high fidelity loud speakers.

Multifunction filters can either be of fixed topology type in which the number and nature of the active and passive elements remain fixed and usually at least three out of the five generic filtering functions namely HP, LP, BP, band elimination (BE)/notch and All-pass (AP) are simultaneously available in current-mode/ voltage-mode or both, or of variable topology type in

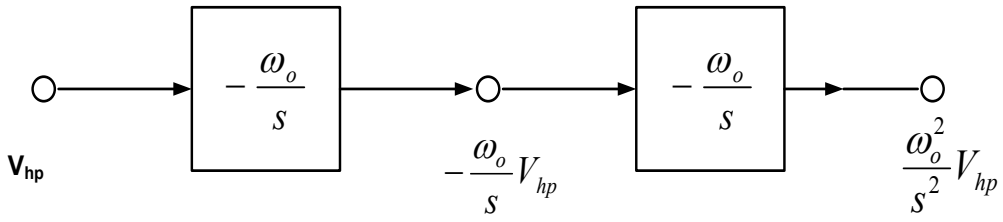
which the nature and number of elements vary for different output responses. A multifunction biquad is said to be 'Universal' if it is capable of realizing all the five standard filter functions.

Yet another classification can be made on the basis of the number of inputs and number of outputs present in a particular realization. In single-input single-output (SISO) universal biquads there is one input and only one output response is available at a time. This type of filter belongs to the variable topology class. In multiple-input single-output (MISO) type universal filters, multiple inputs are required and a single output response is available at a time. This type of filter will also be classified under variable topology. In single-input multiple-outputs (SIMO) type universal filters only one input is required and different output responses are simultaneously available at different nodes of the circuit. Lastly, under multiple-inputs multiple-output (MIMO) class, more than one input is applied and a particular output response is obtained by judicious choice of inputs or combinations thereof.

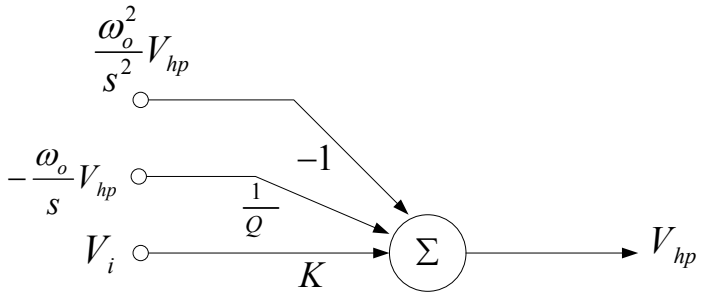
Mostly the current mode multifunction filters are based on the two integrator loop topology first proposed by Kerwin Huelsman and Newcomb and in the following we give a brief introduction of the two integrators in a loop topology before we present the proposed multifunction filter.

4.1.1 Kerwin-Huelsman-Newcomb (KHN) Biquad Filter

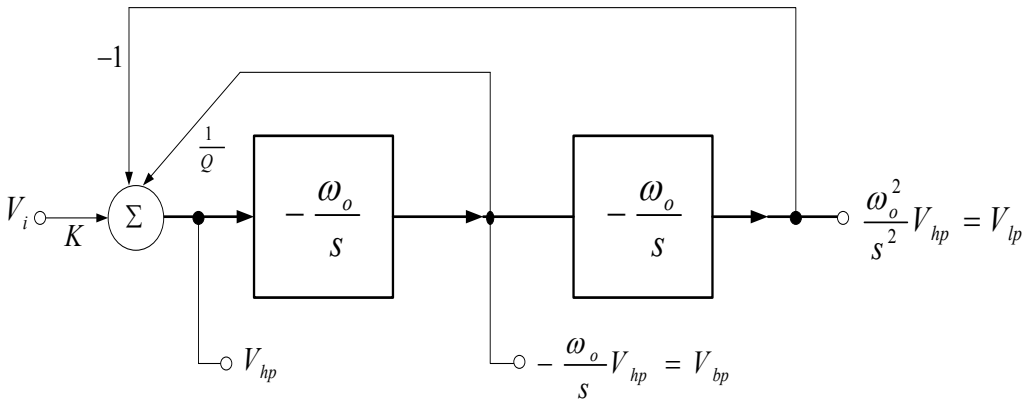
The Kerwin-Huelsman-Newcomb (KHN) biquad filter is also known as state-variable filter which is used for multifunction filtering structures. This structure is realized using two integrators in the feedback loops. The most important feature of this structure is to provide second order low-pass filter (LPF), high-pass filter (HPF) and band-pass filter (BPF) simultaneously. KHN-biquad filter is normally used because it provides some advantages like low component spread, low active and passive sensitivities and sufficient stable response. In literature, different active blocks are used to design KHN biquad filter. Some of them operate in current mode and others in voltage mode. Current mode circuits have some advantages over voltage mode such as linearity, less power consumption, wider bandwidth, larger dynamic range and simplicity in the circuit realization. The block diagram of KHN-biquad filter is shown in Fig. 4.1.



(a)



(b)



(c)

Fig 4.1 Block diagram of KHN biquad filter using two integrators in feedback loop

Consider a second order high-pass filter (HPF) as

$$T(s) = \frac{V_{hp}}{V_i} = \frac{Ks^2}{s^2 + s\frac{w_0}{Q} + w_0^2} \qquad (4.1)$$

where K is the gain at high frequency. To rearrange the Eq. 4.1, the expression as follows

$$V_{hp} + \frac{1}{Q}\left(\frac{w_0}{s}V_{hp}\right) + \left(\frac{w_0^2}{s^2}V_{hp}\right) = KV_i$$

(4.2)

The output signal V_{hp} can be obtained by summing three signals which is shown in Fig. 4.1(b) from which two input signals can be generated which is shown by Fig. 4.1(a) where two integrators are used. The V_{hp} signal is derived from Eq. 4.2 which is found as follows

$$V_{hp} = KV_i - \frac{1}{Q}\left(\frac{w_0}{s}V_{hp}\right) - \left(\frac{w_0^2}{s^2}V_{hp}\right)$$

(4.3)

The transfer function of BPF which can be defined as

$$T_{BP}(s) = -Kw_0\frac{s}{s^2 + s\frac{w_0}{Q} + w_0^2}$$

(4.4)

Similarly, the transfer function of low pass filter (LPF) is derived as

$$T_{LP}(s) = -Kw_0^2\frac{1}{s^2 + s\frac{w_0}{Q} + w_0^2}$$

(4.5)

The two integrator-loop biquad filter realizes three basic second order filter functions HP, BP and LP simultaneously. This circuit is most popular and it is commonly known as universal active filter (the Kerwin-Huelsman-Newcomb biquad).

4.1.2 Tow–Thomas Biquad Filter

The block diagram of Tow-Thomas (TT) biquad filter is shown in Fig. 4.2. In TT based filters, two outputs can be taken simultaneously such as band-pass filter and low pass filter

responses. Two negative integrator loops are used in which one is lossy integrator and other one is ideal integrator. The integrators can be realized by active building blocks [1]. One active building block is used to realize difference circuit. So a TT biquad filter can be implemented by using three active building blocks. In literature, TT biquad filter was implemented using Op-amp, OTRA, CCII and DVCC [2]. For high quality factor (Q) and high center frequency the Tow-Thomas filter may be no longer right choice to implement a high Q based band pass filter.

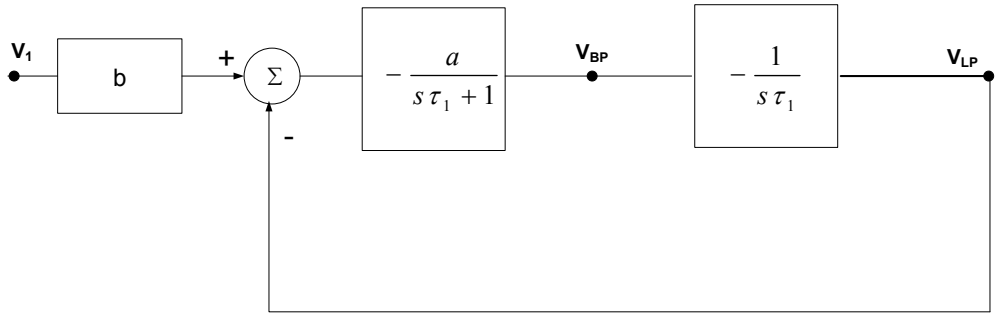


Fig. 4.2 Equivalent block diagram of the Tow-Thomas Filter [2]

4.2 THE PROPOSED VOLTAGE MODE BIQUAD

4.2.1 Introduction and Description

The block diagram of the proposed voltage mode multifunction biquad filter is shown in fig. 4.3. It contains two lossless integrators, one summer and proportional gain blocks. It is similar in configuration to the filter based on CCII proposed in [4]. In this configuration, most important thing is that all the passive elements are used as grounded elements [5]. So, it is easy to fabricate in the form of IC. By analysis of the circuit shown in fig.4.3, the transfer function expressions are given as

$$\frac{V_{out1}}{V_{in}} = \frac{\frac{G_1 G^2}{C_1 C_2 (G_1 + G - G_2)}}{D(s)} \tag{4.6}$$

$$\frac{V_{out2}}{V_{in}} = \frac{\frac{-sG_1 G}{C_2 (G_1 + G - G_2)}}{D(s)} \tag{4.7}$$

$$\frac{V_{out3}}{V_{in}} = \frac{\frac{s^2}{(G_1 + G - G_2)} + \frac{G_1 G^2}{C_1 C_2 (G_1 + G - G_2)}}{D(s)} \tag{4.8}$$

$$D(s) = s^2 + \frac{G^2}{C_1(G_1 + G - G_2)} s + \frac{G^2}{C_1 C_2} \tag{4.9}$$

From equations (1)-(4) it can be seen that a lowpass response is obtained from V_{out1}, a bandpass response is obtained from V_{out2} and a notch response is obtained fromV_{out3}. The proposed circuit uses three VDCCs, two grounded capacitors and eight resistors. The design methodology of using only grounded capacitors is attractive, because grounded capacitor can be implemented on a smaller area than the floating counterpart and it can absorb equivalent shunt capacitive parasitics [7-9].

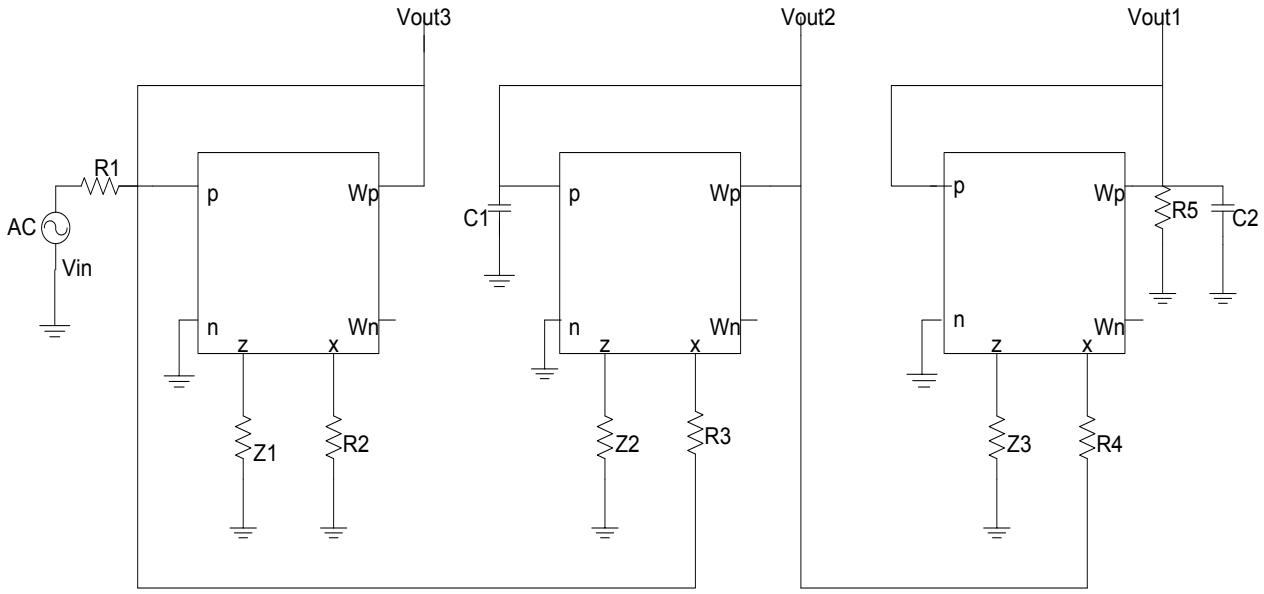


Fig: 4.3: Block Diagram of Proposed Biquad Filter

In all cases, the resonance angular frequency ω_o and the quality factor Q are given by

$$w_0 = G\sqrt{\frac{1}{C_1 C_2}} \tag{4.10}$$

$$Q = \frac{(G_1 + G - G_2)}{G}\sqrt{\frac{C_1}{C_2}} \tag{4.11}$$

The resonance angular frequency can be controlled by *G*. The quality factor can be orthogonally controlled by *G*1 or *G*2.

4.2.2 Sensitivity Analysis

The sensitivities of the proposed circuit are given as:

$$S_G^{w_0} = 1\ ;\ S_{C_1}^{w_0} = S_{C_2}^{w_0} = -\frac{1}{2}$$

$$S_{G_1}^{Q} = \frac{G_1}{G + G_1 - G_2}\ ;\ S_{G_2}^{Q} = \frac{G_1}{G + G_1 - G_2}$$

$$S_G^{Q} = \frac{-G_1 + G_2}{G + G_1 - G_2}$$

$$S_{C_1}^{Q} = -S_{C_2}^{Q} = \frac{1}{2}$$

4.2.3 Simulation Results

The proposed circuit was simulated using PSPICE. The VDCC was implemented using the MOSFET model proposed in [1] using TSMC 0.18μm parameters. The supply voltages are chosen as ± 0.9 V. The following setting was selected to obtain the lowpass, bandpass and notch filters: *R*1 = *R*2 = *R*3 = *R*4 = *R*5 = 1kΩ, *C*1 = *C*2 = 1nF with *Q* = 1 and f_o = 159.15 KHz. We have taken g_m = 277μA/V and this makes $Z_1 = Z_2 = Z_3 = 3.6$kΩ. Fig. 4.4 and fig.4.5 represent the simulated frequency responses for the lowpass (*Vout*1), bandpass (*Vout*2) and notch (*Vout*3) filters of fig.4.3, respectively. While fig. 4.4 shows the low-pass, band-pass and notch responses, fig.4.5 shows the phase response for the three outputs. The simulation results are coherent with the theoretical analyses.

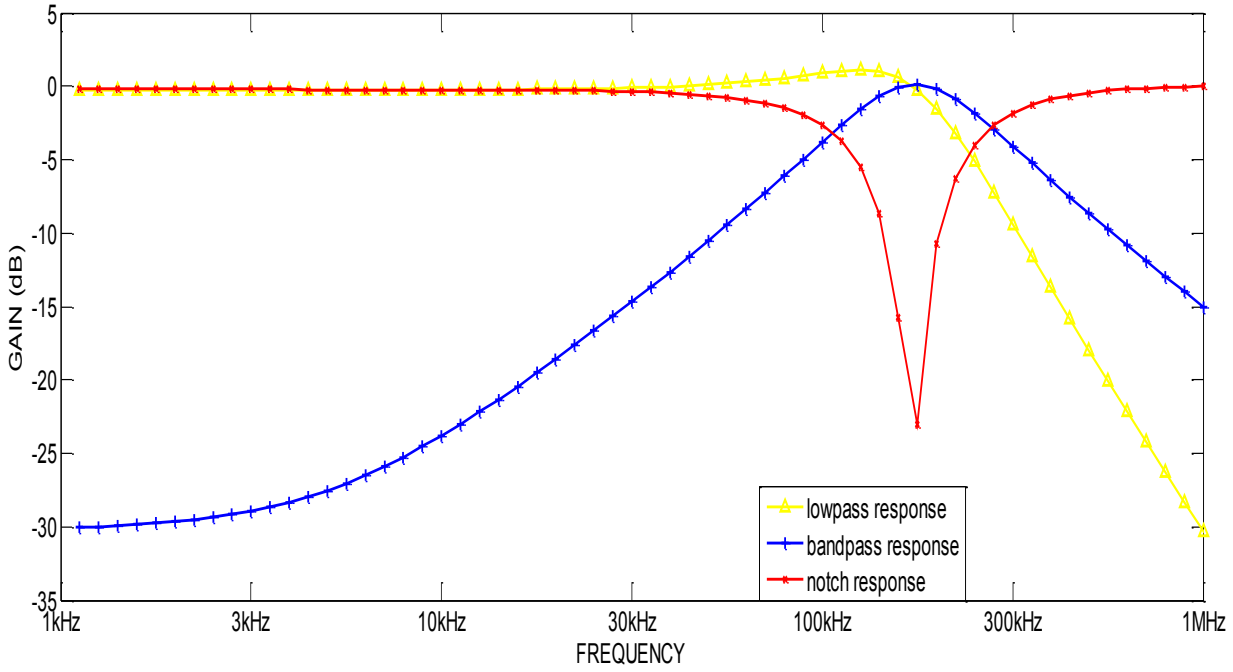


Fig.4.4: Magnitude response of the proposed biquad filter showing low-pass, band-pass and notch outputs

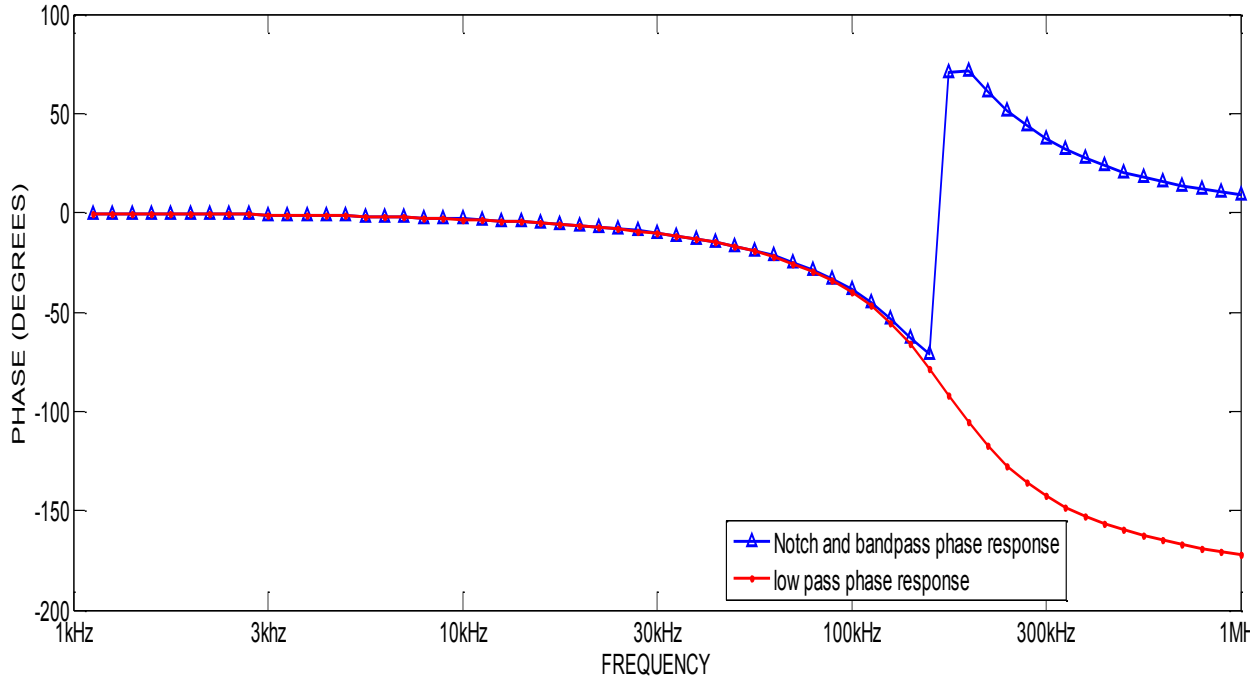


Fig.4.5: Phase response of the proposed biquad filter

4.3 THE PROPOSED CURRENT MODE OSCILLATOR CONFIGURATIONS

4.3.1 Introduction

The sinusoidal oscillators play a very important role in the electronics systems. They find application in communications, instrumentation and measurements, control systems, signal processing, etc., out of which their role in the field of communications is unbendable. RC- active oscillators are preferred for their monolithic integration, rather than LC or RLC oscillators as for IC fabrication in the present day scenario the realization of inductors is not advisable.[16]

In the past works, RC-active oscillators have been implemented using various voltage-mode and current mode active blocks. However, the oscillators based on voltage-mode active blocks are limited to low-medium frequency applications, owing to inherent limitations such as slew-rate limiting, dominant pole, etc.

In last two decades, current-mode signal processing has grown, providing classy solutions for analog circuit problems. The main advantages of this mode of operation are wide bandwidth and usually large dynamic ranges. Although, CCII is claimed to be the standard building block for current-mode operation, the newly proposed block presents a good alternate as a multi-mode operation block.[10]

4.3.2 Circuit Description

Here we have given 11 different configurations for single frequency oscillators using VDCC, the circuits of these oscillators are given in fig. 4.6. The characteristic equations of the various oscillator configurations can be easily determined by the analysis of the respective circuits and are given as:

$$s^2C_2C_7 + s\{(C_2 + C_7)G_5 - C_2G_8\} + G_5G_8 = 0 \tag{4.12}$$

$$s^2C_5C_8 + s\{(C_5 + C_8)G_2 - C_5G_7\} + G_2G_7 = 0 \tag{4.13}$$

$$s^2C_2C_5 + s(C_5G_8 + C_2G_5 - C_2G_8) + G_5G_8 = 0 \tag{4.14}$$

$$s^2C_6C_3 + s\{C_3(G_6 - G_4) + 2G_1C_6\} + 2G_1G_6 = 0$$

(4.15)

$$s^2C_6C_3 + s\{C_6G_5 + C_3(G_6 + G_5 - G_4)\} + G_6G_5 = 0$$

(4.16)

$$s^2C_5C_3 + s\{C_5G_6 + C_3(G_6 + G_5 - G_4)\} + G_6G_5 = 0$$

(4.17)

$$2s^2C_1C_2G_6 + s(2C_1G_6G_8 + C_2G_6G_8 - C_2G_3G_8) + G_3G_6G_8 = 0$$

(4.18)

$$2s^2C_7C_8G_6 + s(C_8G_6G_3 + C_7G_6(G_2 + G_3) + C_7G_2G_3 - C_8G_3G_2) + G_3G_2G_6 = 0$$

(4.19)

$$s^2C_5C_8G_3 + s\{C_5G_2G_3 + G_2G_9(G_2 + G_3) - C_8G_2G_3\} + G_2G_3G_9 = 0$$

(4.20)

$$s^2C_2C_9 + s(2C_1G_6G_8 + C_2G_6G_8 - C_2G_3G_8) + G_3G_6G_8 = 0$$

(4.21)

$$s^2C_3C_5R_1R_4R_6 + s\{(C_3 + C_5)R_1R_4 - C_3R_1R_6\} + 2R_4 = 0$$

(4.22)

From these characteristics we can determine the oscillation frequencies and the conditions of oscillation of the various circuit configurations. Among these configurations, the first three configurations are single frequency oscillator (SFO) fully coupled (FC) configurations. Three more configurations similar to the first three configurations are possible but they are unstable and hence are not included. The tenth and the eleventh configurations are single resistor controlled oscillator (SRCO) configurations. The eleventh configuration is also fully uncoupled (FU) configuration.

The configurations fourth, fifth, sixth and eleventh are canonic four-node oscillators and apart from these configurations no other configurations are possible. Detailed explanation of passive four-node and five-node circuits is given in [10].

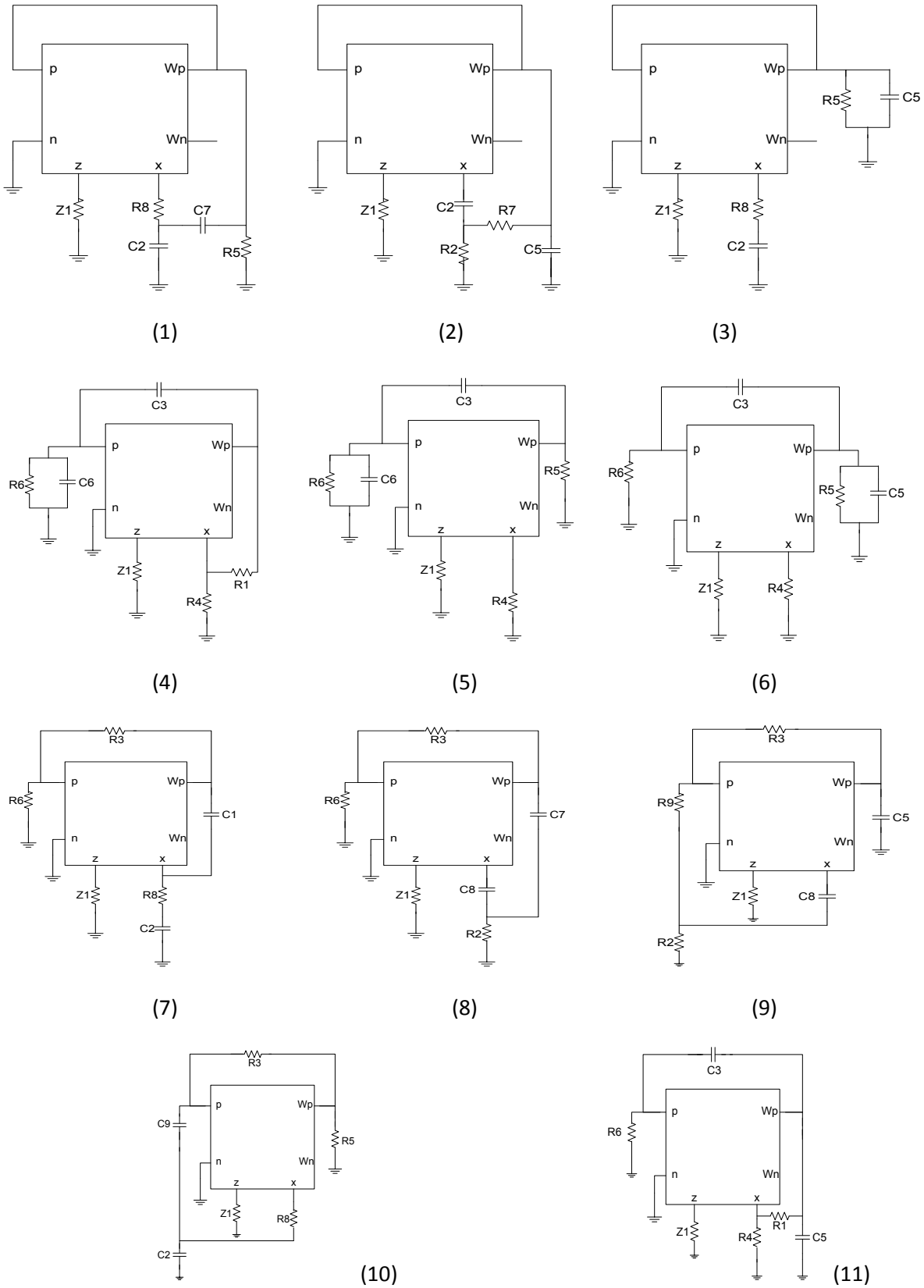


Fig. 4.6: Different single frequency RC- canonic oscillator configuration

TABLE 4.1: Characteristic equation, oscillation frequency and condition of oscillation of different oscillator configurations.

Circuit no	Characteristic Equation no.	Oscillation Frequency, w_0^2	Condition of oscillation
1	(4.12)	$\frac{G_8G_5}{C_7C_2}$	$\frac{G_5}{G_8}\left(1+\frac{C_7}{C_2}\right)=1$
2	(4.13)	$\frac{G_7G_2}{C_8C_5}$	$\frac{G_2}{G_7}\left(1+\frac{C_8}{C_5}\right)=1$
3	(4.14)	$\frac{G_8G_5}{C_2C_5}$	$\frac{C_5}{C_2}+\frac{G_5}{G_8}=1$
4	(4.15)	$2\frac{G_6G_1}{C_6C_3}$	$\frac{1}{G_4}\left(2\frac{C_6}{C_3}G_1+G_6\right)=1$
5	(4.16)	$\frac{G_6G_5}{C_6C_3}$	$\frac{1}{G_4}\left\{\left(\frac{C_6}{C_3}+1\right)G_5+G_6\right\}=1$
6	(4.17)	$\frac{G_6G_5}{C_5C_3}$	$\frac{1}{G_4}\left\{\left(\frac{C_5}{C_3}+1\right)G_6+G_5\right\}=1$
7	(4.18)	$\frac{1}{2}\frac{G_8G_3}{C_2C_1}$	$\frac{G_6}{G_8}+2\frac{C_1}{C_2}\frac{G_6}{G_3}=1$
8	(4.19)	$\frac{1}{2}\frac{G_3G_2}{C_8C_7}$	$\frac{G_6}{G_2}+2\frac{C_7}{C_8}\left(\frac{G_6}{G_2}+\frac{G_6}{G_3}+1\right)=1$
9	(4.20)	$\frac{G_9G_2}{C_8C_5}$	$\frac{C_5}{C_8}\left(\frac{G_9}{G_2}+\frac{G_9}{G_3}+1\right)=1$
10	(4.21)	$\frac{G_8G_5G_3}{C_9C_2(G_5+G_3)}$	$\frac{G_5}{G_8}\left(1+\frac{C_9}{C_2}\right)=1$
11	(4.22)	$2\frac{G_6G_1}{C_5C_3}$	$\frac{G_6}{G_4}\left(1+\frac{C_5}{C_3}\right)=1$

4.3.3 Simulation Results

Simulation was performed using a CMOS realization of VDCC given in [3]. To prove the theoretical validity of the proposed oscillator of fig.4.6 for pole frequency (f_0) = 1.5MHz, the oscillator was simulated with PSPICE program. We have taken g_m = 277µA/V and this makes Z_1= Z_2 = Z_3= 3.6kΩ. The passive elements are selected as R_8 = 45kΩ, R_8 = 100kΩ, Z_1 = 3.6kΩ and C_1 = C_2 = 1pF. The bias current are selected as I_{B1} = 50µA (g_m = 277.13µA/V) and I_{B2} = 100µA in [3]. The FFT analysis is shown in fig.4.8 and the transient analysis is shown in fig.4.7.

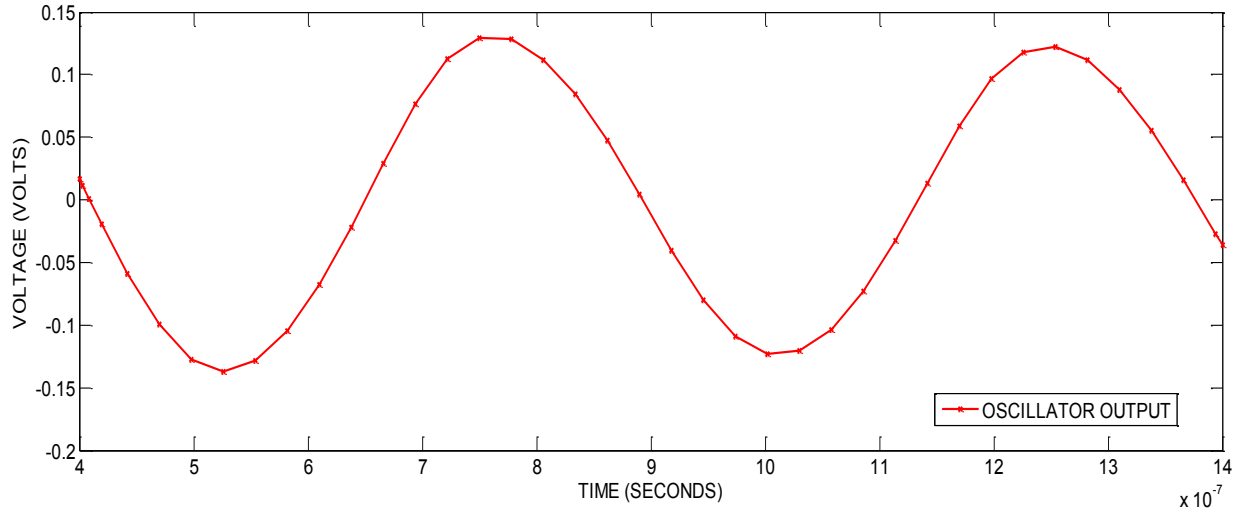


Fig 4.7: Oscillator output for configuration 1

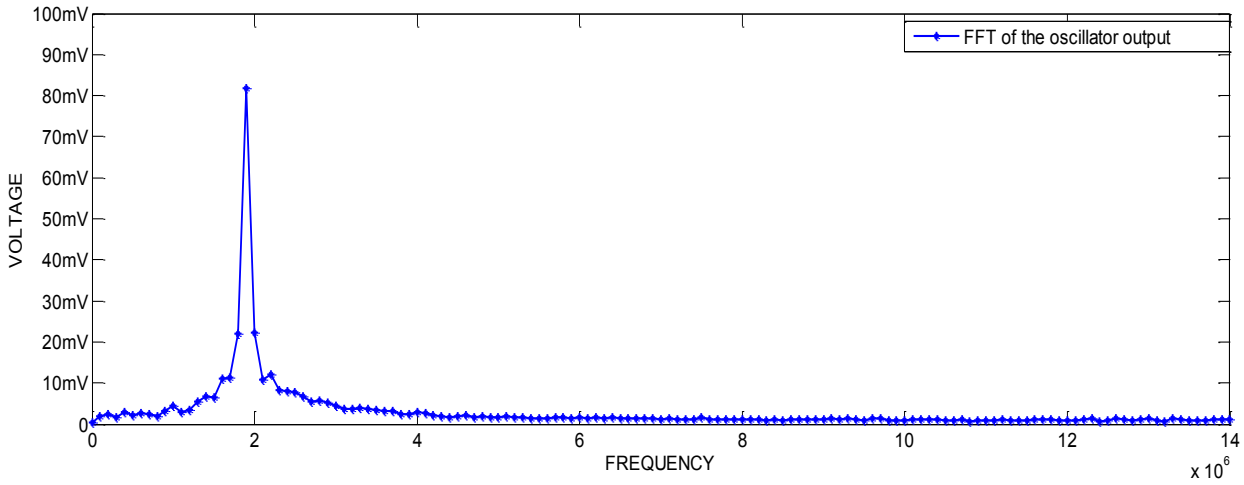


Fig.4.8: FFT of the oscillator output for configuration 1

4.4 THE PROPOSED VOLTAGE MODE OSCILLATOR

4.4.1 Introduction and description

The scheme for realization of the four-phase sinusoidal oscillator is shown in fig.4.9. The basic building block for this scheme consists of an oscillator with two outputs which are 135° apart in phase (two-φ oscillator), along with one non-inverting non-ideal integrator and one non-inverting non-ideal differentiator. The oscillator with the two 135° apart outputs (two-φ oscillator) is realized using a band-pass filter (BPF) shown in fig.4.10. This BPF uses two active VDCC blocks and some passive elements. [11-15]

The transfer gain of this BPF is given as

$$\frac{V_4}{V_{in}} = \frac{s\left[\frac{C_1}{C_2C_4R_3}\right]}{s^2 + s\left[\frac{1}{R_2C_4} + \frac{1}{R_4C_4}\right] + \frac{1}{C_2C_4R_2R_4}} \tag{4.23}$$

Using this BPF the two-φ oscillator is realized by providing a direct feedback from output terminal V_4 to the input V_{in}.

The characteristic equation of this circuit is given as:

$$s^2 + s\left[\frac{1}{R_2C_4} + \frac{1}{R_4C_4} - \frac{C_1}{C_2C_4R_3}\right] + \frac{1}{C_2C_4R_2R_4} = 0 \tag{4.24}$$

Hence, the condition of oscillation is given as:

$$\frac{1}{R_2C_4} + \frac{1}{R_4C_4} = \frac{C_1}{C_2C_4R_3} \tag{4.25}$$

And the frequency of oscillation is given as:

$$w_0 = \sqrt{\frac{1}{C_2 C_4 R_2 R_4}}$$

(4.26)

For $R_2 = R_4 = R \; and \; C_1 = C_2 = C_4 = C$

The oscillation condition and frequency of oscillation respectively becomes:

$$R_3 = \frac{R}{2}$$

$$w_0 = \frac{1}{RC}$$

(4.27)

From fig.4.11, the phase relationship between output voltages V_1 and V_2, at oscillation frequency is obtained as:

$$V_4 = -\frac{R_4}{(sC_4R_4 + 1)R_3} V_1 \;\; for \; s = jw_0$$

$$V_4 = V_1 \angle 135°$$

(4.28)

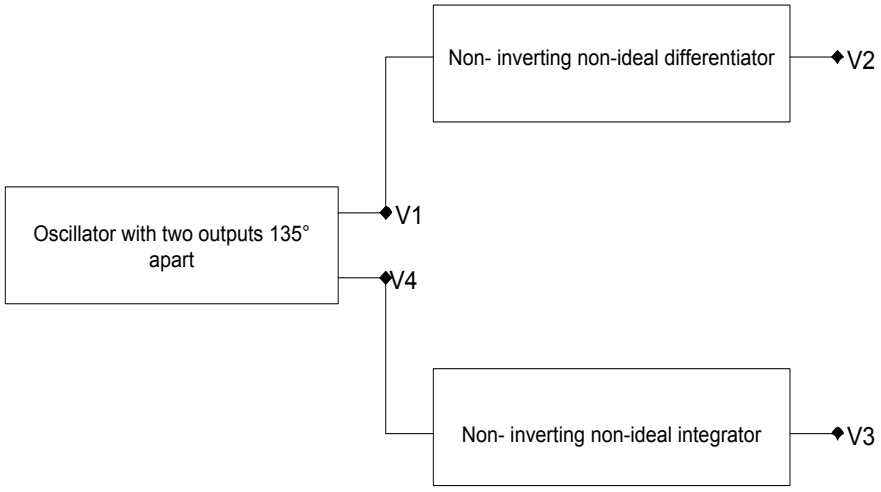


Fig.4.9: Scheme for realization of oscillators[12]

Equation (4.28) shows that the two output voltages are 135° apart. From fig.4.12, for a non-inverting non-ideal differentiator, the output voltage V_2 leads the input voltage V_1 by 45°, which is obtained as:

$$V_2 = \frac{(sC_3R_6 + 1)R_7}{R_6} V_1 \ \ for\ s = jw_0$$

$$V_2 = V_1 \angle 45°$$

(4.29)

For non-inverting integrator, the output voltage V_3 lags behind the input voltage V_4 by 45°. The phase relationship between V_4 and V_3 is obtained as:

$$V_3 = -\frac{R_5}{(sC_5R_5 + 1)R_1} V_4 \ \ for\ s = jw_0$$

$$V_3 = V_4 \angle -45°$$

(4.30)

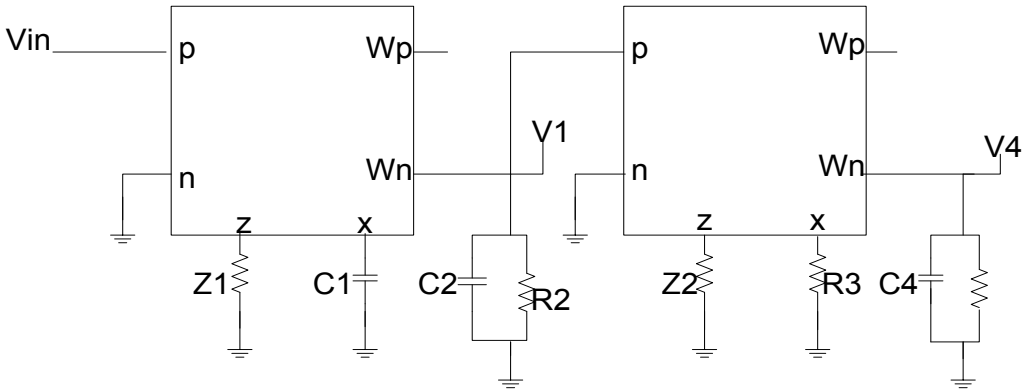
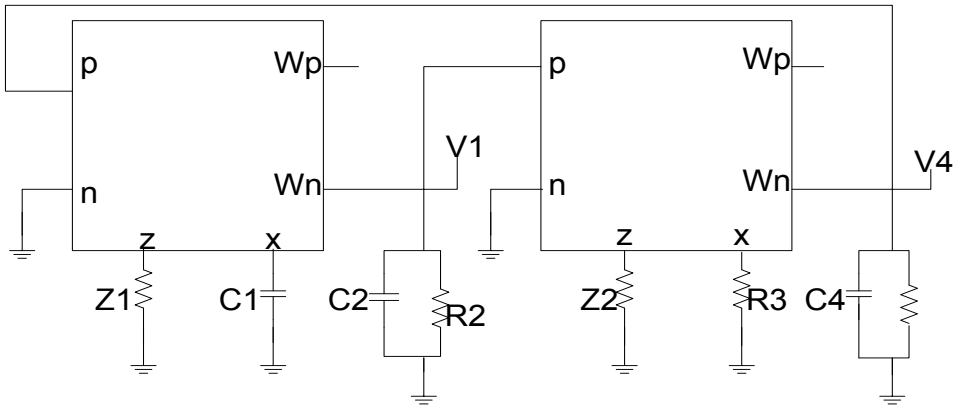
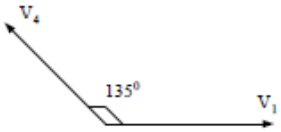


Fig.4.10: Band-pass filter, the basic building block



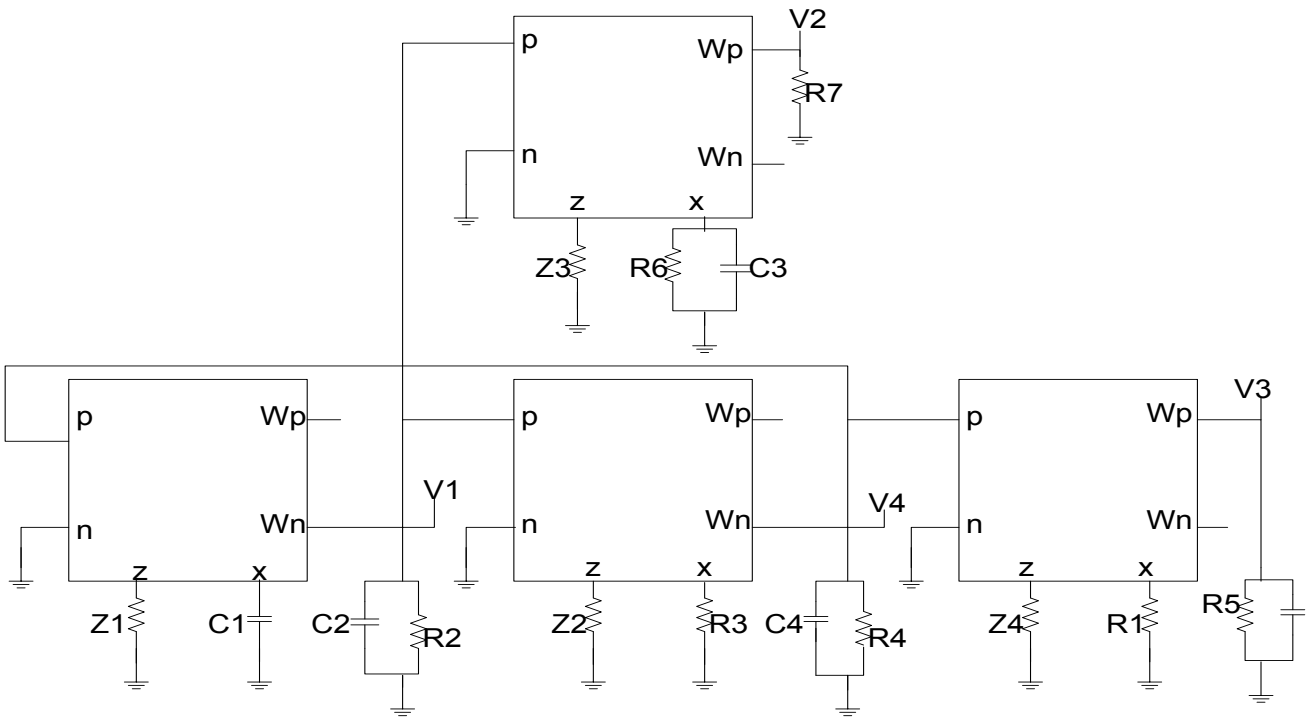
(a)



(b)

Fig.4.11: Proposed (a) VDCC based 2-φ sinusoidal oscillator (b) its phasor diagram

Fig.4.11 and fig.4.12 show the phasor diagrams of the 2-φ sinusoidal oscillator and 4-φ sinusoidal oscillator, respectively. It is evident from fig.4.11, that the 2-φ sinusoidal oscillator gives two consecutive outputs with a phase shift of 135°. Similarly, fig.4.12 shows that the 4-φ sinusoidal oscillator can provide four consecutive outputs with phase shift of 45°. [12]



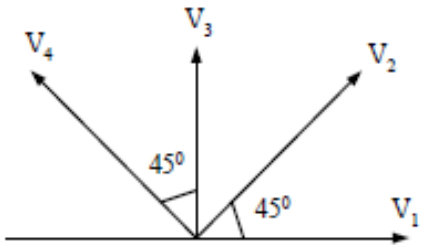


Fig.4.12: Proposed VDCC based 4-φ sinusoidal oscillator with its phasor diagram

4.4.2 Sensitivity Analysis

The passive sensitivities of the oscillators are obtained to be as follows:

$$S_{R_2}^{w_0} = S_{R_4}^{w_0} = S_{C_2}^{w_0} = S_{C_4}^{w_0} = -\frac{1}{2} \tag{4.31}$$

$$S_{R_3}^{w_0} = S_{C_1}^{w_0} = 0 \tag{4.32}$$

4.4.3 Simulation Results

The VDCC block was simulated using the MOSFET model of VDCC given in [1]. The PSPICE simulations were done using TSMC 0.18μm parameters. The VDCC based voltage mode 2-φ sinusoidal oscillator and 4-φ sinusoidal oscillator were designed for an oscillating frequency 10kHz using equation (4.27). We have taken g_m = 277μA/V and this makes Z_1= Z_2 = Z_3= 3.6kΩ

The values of passive components are as follows:

$$R_1 = R_2 = R_4 = R_5 = R_6 = R_7 = 10K, R_3 = 4.4K$$

$$C_1 = C_2 = C_3 = C_4 = C_5 = 1.59nF.$$

The value of Z_1, Z_2, Z_3 is determined by the transconductance gain of the VDCC, g_m, which is equal to 277μA/V [2], and from this value we get

$$Z_1 = Z_2 = Z_3 = 3.6K$$

The output waveform of the 2-φ sinusoidal oscillator is shown in fig.4.13, where the two sinusoidal outputs are in 135° phase difference. The output waveform of the 4-φ sinusoidal oscillator is shown in fig.4.14, where the four sinusoidal outputs are in 45° phase difference.

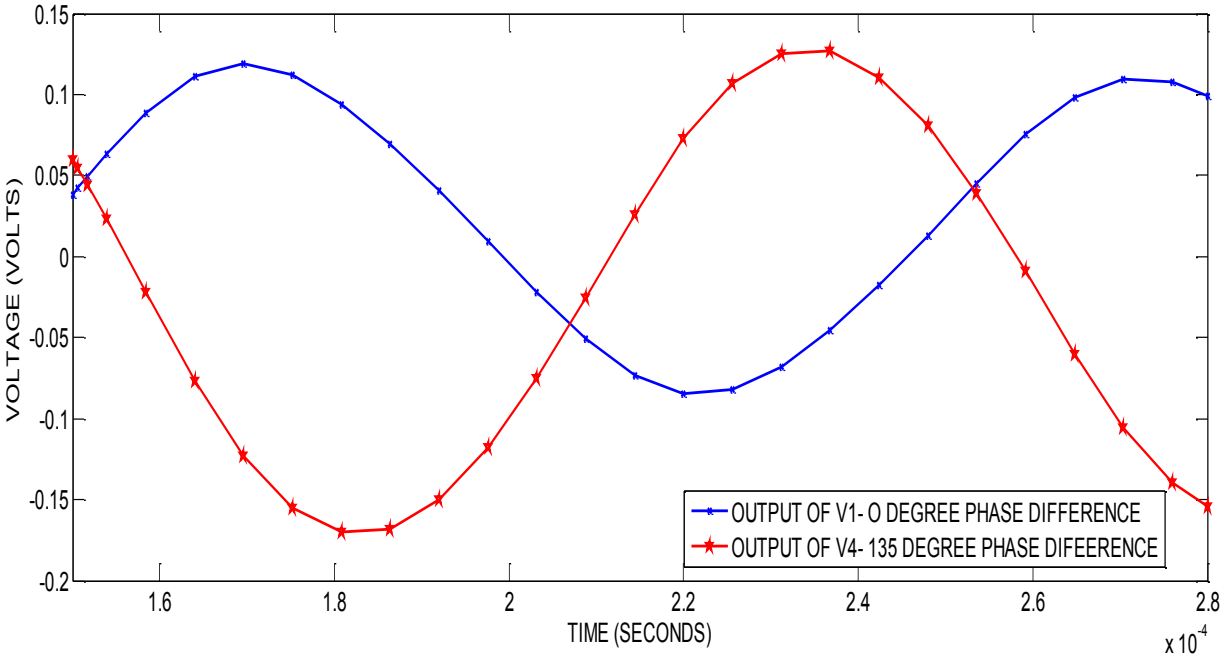


Fig.4.13: Output of the proposed VDCC based 2-φ sinusoidal oscillator

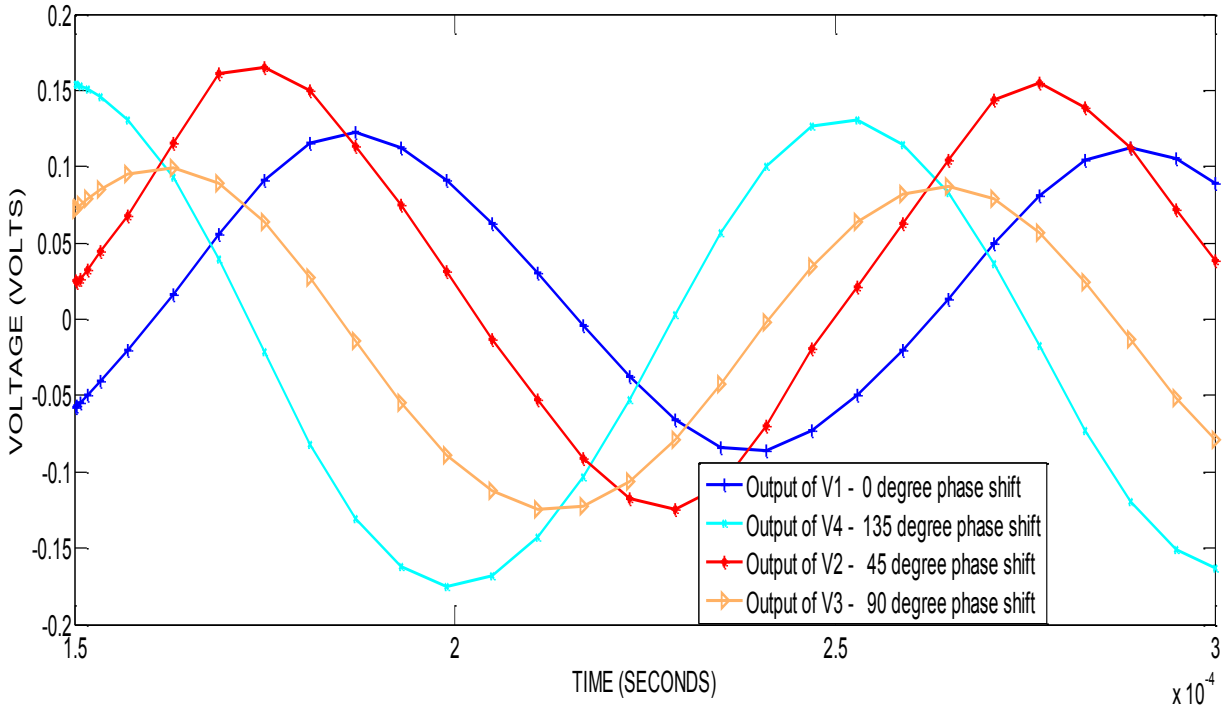


Fig.4.14: Output of the proposed VDCC based 4-φ sinusoidal oscillator

4.5 CONCLUSIONS

First a new single input and three outputs voltage- mode biquadratic filter is presented. The proposed circuit uses three VDCCs, two grounded capacitors and eight resistors. The new circuit offers several advantages, such as the realization of lowpass, bandpass, and notch filter functions, simultaneously, in the same circuit configuration; the use of only three VDCCs; orthogonally controllable resonance angular frequency and quality factor and the use of only grounded capacitors.

Secondly VDCC based voltage mode multi-phase sinusoidal oscillator is realized. In this first the realization of VDCC- based Voltage mode 2-phase sinusoidal oscillator is done. The VDCC- based Voltage mode 2-phase sinusoidal oscillator is then transformed into a VDCC-based Voltage mode 4-phase sinusoidal oscillator. All the realized oscillators provide the voltages of almost equal magnitude and equal phase shift. The circuits have attractive sensitivity performance, use of grounded passive components and are suitable for modern IC technologies. The simulation results of the proposed oscillators verify the proposed theory.

Finally, current mode oscillators are realized where 11 different configurations are given for RC-sinusoidal oscillators are realized. The VDCC based sinusoidal oscillator configurations have been proposed and simulated which verified the usability of VDCC in the analog signal processing among the novel active building blocks. The circuit described is simpler. Using PSPICE simulation, the results have been verified.

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CHAPTER 5

CONCLUSIONS AND FUTURE DIRECTIONS

5.1 CONCLUSION

Chapter 2 covers all the basic components namely differential pair, current mirror, active loads, trans-linear buffer and current conveyor which are used to design several active building blocks, are as. Current conveyor is the commonly used active block to derive others. Types of current conveyors are mainly CCI, CCII and CCIII. Some derivatives of current conveyor are discussed such as FDCCII, OFCC, CCCII, CFBCCII, UCC and DXCCII. In this chapter OTA has also been described. These active blocks are used to realize various analog signal processing applications such as filters, oscillator, amplifier etc.

In the chapter 3, a novel active building block namely the VDCC is discussed in detail. Its DC and AC characteristics of input-output were verified using PSPICE simulation. The basic signal processing applications such as adder, subtractor, differentiator, integrator and amplifier were designed using VDCC and simulated in PSPICE. The application of grounded inductance simulation was described and applied to design a high-pass filter. In yet another application, floating inductance was designed and simulated in PSPICE. The floating inductance was used to implement a band pass filter (BPF) with specified central frequency.

In chapter 4 a brief introduction of multifunction biquad filter design using the two-integrator in a loop methodology has been presented. Finally some novel filters and oscillator configurations are proposed using the VDCC active block. First one is a voltage mode biquad filter which gives low-pass, band-pass and notch outputs. The circuit for this biquad employs two grounded capacitors and seven grounded resistors. The oscillation frequency and the Q-factor of the circuit are independently tunable. Second one is a current mode single input multiple output type multifunction biquad filter using the voltage differencing current conveyor. The filter has high pass, band pass and low pass outputs in current mode. The filter employs two grounded capacitors. All the outputs are at high impedance nodes. The pole frequency and bandwidth of filter are independently tunable. After the proposition of filter configurations oscillator configurations are proposed. First some canonic RC oscillator configurations are proposed for

sinusoidal oscillators. These oscillator configurations work in current mode and are single frequency oscillators. After the current mode oscillators, voltage mode oscillator configurations are proposed using VDCC active block. In voltage mode we have proposed configurations for two-phase and four-phase oscillators. All the filters and oscillators have been simulated in PSPICE using 0.18 um TSMC CMOS technology.

5.2 SCOPE FOR FUTURE WORK

In the present work the application of VDCC for biquad filter application has been presented. VDCC is a very versatile block as it combines the features of both Operational Trans-Conductance Amplifier (OTA) as well as Current Conveyor Second Generation (CCII). It can be used for realization of various filters and oscillators with different properties.

There is scope for improvement in the basic MOSFET structure of VDCC. A MOSFET structure which uses lesser transistors than the presently available MOSFET structure can improve the performance of the VDCC in terms of Power Dissipation. Also it can make the implementation of the VDCC block much easier.

Implementation of VDCC block using the ICs available in the market like AD 844, etc., is also one area where a lot of work can be done. Implementing VDCC using commercially available ICs will make it more versatile and more acceptable to the designers. Similarly, a lot of work can also be done in determining possible realizations of VDCC using other discrete and commercially available components like Operational Trans-conductance Amplifiers (OTA), Transistor arrays, CFOA etc.

Similarly filter circuits with electronically tunable parameters can also be realized with VDCC. Moreover designers can try to make filters and oscillators that give similar outputs using lesser number of components which can make the VDCC a good choice for IC implementation.

Appendix A: MODEL PARAMETER FILES

PSPICE model file used for simulation is TSMC CMOS 0.18 µm process which has following model parameters -

.MODEL nmos_transistor **NMOS** (LEVEL=7 VERSION=3.1 TNOM=27 TOX=4.1E-9 XJ=1E-7 +NCH=2.3549E17 VTH0=0.354505 K1=0.5733393 K2=3.177172E-3 K3=27.3563303 +K3B=-10 W0=2.341477E-5 NLX=1.906617E-7 DVT0W=0 DVT1W=0 DVT2W=0 +DVT0=1.6751718 DVT1=0.4282625 DVT2=0.036004 U0=327.3736992 UA=-4.52726E-11 +UB=4.46532E-19 UC=-4.74051E-11 VSAT=8.785346E4 A0=1.6897405 AGS=0.2908676 +B0=-8.224961E-9 B1=-1E-7 KETA=0.021238 A1=8.00349E-4 A2=1 RDSW=105 PRWG=0.5 +PRWB=-0.2 WR=1 WINT=0 LINT=1.351737E-8 XL=-2E-8 XW=-1E-8 DWG=1.610448E-9 +DWB=-5.108595E-9 VOFF=-0.0652968 NFACTOR=2.4901845 CIT=0 CDSC=2.4E-4 +CDSCD=0 CDSCB=0 ETA0=0.0231564 ETAB=-0.058499 DSUB=0.9467118 +PCLM=0.8512348 PDIBLC1=0.0929526 PDIBLC2=0.01 PDIBLCB=-0.1 DROUT=0.5224026 +PSCBE1=7.979323E10 PSCBE2=1.522921E-9 PVAG=0.01 DELTA=0.01 RSH=6.8 +MOBMOD=1 PRT=0 UTE=-1.5 KT1=-0.11 KT1L=0 KT2=0.022 UA1=4.31E-9 UB1=-7.61E-+18 UC1=-5.6E-11 AT=3.3E4 WL=0 WLN=1 WW=0 WWN=1 WWL=0 LL=0 LLN=1 LW=0 +LWN=1 LWL=0 CAPMOD=2 XPART=0.5 CGDO=7.7E-10 CGSO=7.7E-10 CGBO=1E-12 +CJ=1.010083E-3 PB=0.7344298 MJ=0.3565066 CJSW=2.441707E-10 PBSW=0.8005503 +MJSW=0.1327842 CJSWG=3.3E-10 PBSWG=0.8005503 MJSWG=0.1327842 CF=0 +PVTH0=1.307195E-3 PRDSW=-5 PK2=-1.022757E-3 WKETA=-4.466285E-4 +LKETA=9.715157E-3 PU0=12.2704847 PUA=4.421816E-11 PUB=0 PVSAT=1.707461E3 +PETA0=1E-4 PKETA=2.348777E-3)

.MODEL pmos_transistor **PMOS** (LEVEL=7 VERSION=3.1 TNOM=27 TOX=4.1E-9 XJ=1E-7 +NCH=4.1589E17 VTH0=-0.4120614 K1=0.5590154 K2=0.0353896 K3=0 K3B=7.3774572 +W0=1E-6 NLX=1.103367E-7 DVT0W=0 DVT1W=0 DVT2W=0 DVT0=0.4301522 +DVT1=0.2156888 DVT2=0.1 U0=128.7704538 UA=1.908676E-9 UB=1.686179E-21 +UC=-9.31329E-11 VSAT=1.658944E5 A0=1.6076505 AGS=0.3740519 B0=1.711294E-6 +B1=4.946873E-6 KETA=0.0210951 A1=0.0244939 A2=1 RDSW=127.0442882 PRWG=0.5

+PRWB=-0.5 WR=1 WINT=5.428484E-10 LINT=2.468805E-8 XL=-2E-8 XW=-1E-8
+DWG=-2.453074E-8 DWB=6.408778E-9 VOFF=-0.0974174 NFACTOR=1.9740447 CIT=0
+CDSC=2.4E-4 CDSCD=0 CDSCB=0 ETA0=0.1847491 ETAB=-0.2531172 DSUB=1.5
+PCLM=4.8842961 PDIBLC1=0.0156227 PDIBLC2=0.1 PDIBLCB=-1E-3 DROUT=0
+PSCBE1=1.733878E9 PSCBE2=5.002842E-10 PVAG=15 DELTA=0.01 RSH=7.7
+MOBMOD=1 PRT=0 UTE=-1.5 KT1=-0.11 KT1L=0 KT2=0.022 UA1=4.31E-9
+UB1=-7.61E-18 UC1=-5.6E-11 AT=3.3E4 WL=0 WLN=1 WW=0 WWN=1 WWL=0 LL=0
+LLN=1 LW=0 LWN=1 LWL=0 CAPMOD=2 XPART=0.5 CGDO=7.11E-10 CGSO=7.11E-10
+CGBO=1E-12 CJ=1.179334E-3 PB=0.8545261 MJ=0.4117753 CJSW=2.215877E-10
+PBSW=0.6162997 MJSW=0.2678074 CJSWG=4.22E-10 PBSWG=0.6162997
+MJSWG=0.2678074 CF=0 PVTH0=2.283319E-3 PRDSW=5.6431992 PK2=2.813503E-3
+WKETA=2.438158E-3 LKETA=-0.0116078 PU0=-2.2514581 PUA=-7.62392E-11
+PUB=4.502298E-24 PVSAT=-50 +PETA0=1E-4 PKETA=-1.047892E-4)

APPENDIX B:

Certificate from IJARECE and the published paper

APPENDIX C:

Certificate from IJARCCE and the published paper