A

Dissertation

On

 **Layout Area Optimization of 1-Bit CMOS Full Adder Using Genetic Algorithm**

Submitted in Partial fulfillment of the requirement

For the award of Degree of

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**DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING**

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**CERTIFICATE**

*This is to Certify that the major project work entitled,* “**Layout Area Optimization of 1-Bit CMOS Full Adder Using Genetic Algorithm**”submitted by **Mayank Kumar (08/VLSI/2k10)** *in partial fulfilment of the requirements for the award of degree of* **Master of Technology** *in* **VLSI Design and Embedded System** *at* **Delhi Technological University** *is an original work carried out under my supervision and has not been submitted for the award of any other degree to the best of my knowledge and belief.*

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**ABSTRACT**

As the world is moving ahead, the electronic devices have become compact and portable. This gives birth to an additional challenge of reducing the size of the electronic circuits that have been incorporated inside these gadgets.

Here we have used genetic algorithm to further reduce the area of the VLSI circuits. We vary the W/L ratio of the CMOS transistors so as to reduce the area occupied by the CMOS transistors and thus resulting in reduction of area on the whole. While we try to minimize the area, the delay has to be taken care off. As we reduce the area the delay get increased and may affect the normal operation of the circuit.

The circuit under consideration is a simple full adder implemented using CMOS technology. The circuit utilizes 28 transistors and runs on a high frequency in the range of MHz. The circuit has three inputs (A,B & C) and two outputs(Sum and Carry).

We utilized the cadence virtuoso-4 to find the acceptable range of values of width and length for which delay are well within the permissible limits. This range is then utilized to act as upper bound and lower bound for the genetic algorithm. Genetic algorithm was implemented using the genetic algorithm toolbox of MATLAB. Genetic algorithm may not give us the ideal solution but helps us to find results which are quite satisfactory.